# STUDY AND DESIGN OF LOW POWER TECHNIQUES FOR CMOS CIRCUITS

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE
OF

**MASTER OF TECHNOLOGY**

IN

**VLSI DESIGN AND EMBEDDED SYSTEM**


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## CANDIDATE'S DECLARATION

I, Abhay Anokha Bansal (2K21/VLS/01) student of MTech (VLSI Design & Embedded System), hereby declare that the project report titled "**STUDY AND DESIGN OF LOW POWER TECHNIQUES FOR CMOS CIRCUITS**" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Masterof Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

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## CERTIFICATE

We hereby certify that the Major Project – II Report titled "STUDY AND DESIGN OF LOW POWER TECHNIQUES FOR CMOS CIRCUITS" which is submitted by Abhay Anokha Bansal, (2K21/VLS/01) of Electronics and Communication Engineering Department, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Masterof Technology, is a record of the project work carried out by the student under our supervision. To the best of our knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

**SUPERVISOR**

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## ABSTRACT

This thesis addresses a significant challenge faced by the VLSI industry today, namely low power designs. The pursuit of low power design has been a driving force for the industry for a considerable period. However, the emergence of high-performance portable battery-operated devices has introduced a new dimension to the design perspective of designers. While CMOS design has been widely adopted due to its robustness and low static power consumption, the increase in transistor density and the reduction of transistor size below the sub-micron level have compromised CMOS's low power characteristics. Consequently, there is a critical need for enhancing CMOS circuits for low power applications.

This thesis investigates two approaches for reducing leakage in CMOS designs. The first approach involves a hardware-based solution, where a 4×4 multiplier is designed incorporating leakage reduction techniques such as stacking, ON/OFF IC, LECTOR, and MTCMOS. By comparing the effectiveness and efficiency of these techniques in reducing leakage power, the most suitable approach within the hardware domain can be identified. The second approach focuses on a software-based solution known as Input Vector Control (IVC). IVC capitalizes on the varying levels of activity exhibited by different input patterns, resulting in different levels of leakage power consumption. This thesis proposes a novel Python-based input vector control algorithm that enhances the accuracy and efficiency of the IVC technique in real-world scenarios. As a future direction, these two approaches can be combined for even better results.

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## CONTENT

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# CHAPTER 1: INTRODUCTION

The rapid advancement of Very Large Scale Integration (VLSI) technology has led to the integration of more transistors onto a single chip. However, this integration has resulted in increased leakage power dissipation due to the reduction in transistor size below the sub-micron level. Consequently, the demand for low power circuits has emerged to meet the needs of portable electronics with longer battery life. Researchers and industries have shifted their focus from high performance to low power circuits, exploring techniques that reduce leakage power consumption, ultimately decreasing overall power and battery size.

Additionally, the increasing demand for high-performance battery-operated digital systems necessitates addressing the issue of leakage power. Leakage power, which refers to the power dissipated by transistors when they are not actively switching, significantly contributes to a circuit's power consumption. Therefore, reducing leakage power has become a crucial objective in the design of energy-efficient digital circuits.

This thesis aims to investigate two approaches for leakage reduction. The first approach involves a hardware-based solution, where a 4×4 multiplier is designed incorporating leakage reduction techniques such as stacking, ON/OFF IC, LECTOR, and MTCMOS. The multiplier, commonly found in Arithmetic Logic Unit (ALU) architectures and utilizing a substantial number of transistors, provides an effective platform to highlight the impact of leakage power reduction techniques. Comparing the effectiveness and efficiency of these techniques in reducing leakage power will help identify the most suitable approach within the hardware domain.

The second approach focuses on a software-based solution known as Input Vector Control (IVC). IVC leverages the varying levels of activity exhibited by different input patterns, leading to different levels of leakage power consumption. This thesis proposes a novel Python-based input vector control algorithm that enhances the accuracy and efficiency of the IVC technique in real-world scenarios. The algorithm's effectiveness is validated through simulation results and experimental evaluation conducted on various NAND-based digital circuits using LTspice. The experimental findings demonstrate the algorithm's

capability to achieve leakage power reductions of up to 50%. Consequently, the proposed IVC algorithm presents a promising solution for low-power design in digital circuits, particularly for battery-operated devices operating within limited power budgets.

## 1.1 BACKGROUND

Low power circuit design has become a crucial aspect of modern electronics due to the exponential increase in demand for battery-operated devices with extended battery life. In recent years, design that consumed less power as compare to power hungry design has gained significant attention from the research community, reducing the power consumption of electronic devices without compromising their performance is the ultimate goal for any low power circuit. The low power circuit design is particularly important in portable devices such as smartphones, tablets, and wearable's that require long battery life to maintain their functionality throughout the day.

The evolution of the VLSI industry has been guided by Moore's law from the starting of the semiconductor industry. VLSI industry have been scaling the transistors in accordance with the Moore's law. From the start of semiconductor industry scaling have been the important concern of design, as it enhances the performance of a chip by many folds with each evolution of VLSI industry. But this enhancement come with a cost that is power. With the scaling, power dissipation increases exponentially which is unavoidable and has become an important concern for the designers.

The main aim of this thesis is to explore a novel algorithm for an IVC input vector control technique and generate a comparative study with other leakage reduction techniques and also validate the proposed algorithm with simulation results. The thesis will also cover the fundamental concepts of low power circuit design, such as power management, energy-efficient design, and optimization techniques.

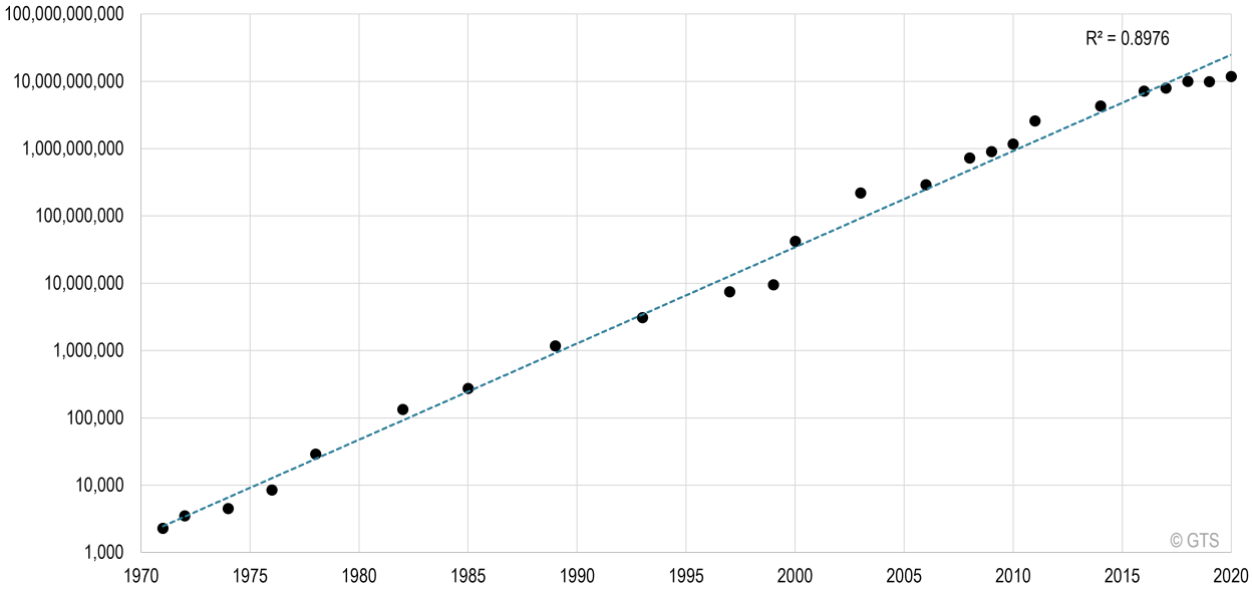

Figure 1.1: Moore's law transistor per microprocessor.

The thesis will begin with an introduction to the basic concepts of low power circuit design and the challenges involved in designing low power circuits. Then a detail discussion of sources of leakage in CMOS circuits and various technique available for leakage reduction is done. The thesis will then discuss IVC in detail and its advantage over other techniques. The thesis will also present a python based algorithm that can be implemented on any NAND based combinational circuit to find input vector that leads to minimum leakage state . Then the proposed algorithm is validated with the help of simulating tool LTspice, by comparing both the results. Finally at the end future scope of IVE and conclusion is given.

In summary, this thesis aims to provide a comprehensive understanding of low power circuit design and its applications in modern electronics. By the end of the thesis, the reader will have a thorough understanding of the principles of IVC for low power circuit design and scope of application of the technique.

## 1.2 NEED OF LOW POWER.

With the exponential increase in demand for portable and battery-operated electronic devices, low power design has become a crucial aspect of modern electronics. This need for low power design arises due to the limitations of capacity of battery and the increasing power dissipation due to reduction in technology node. The low power circuit design is

essential to reduce the power consumption of electronic devices without compromising their performance. This section will explore the need for low power design and its applications in modern electronics.

Why do we need low power design?

The demand for portable electronic devices such as smartphones, tablets, and wearables has increased significantly in recent years. These devices require long battery life to maintain their functionality throughout the day. However, battery technology has not advanced at the same pace as the development of these devices. As a result, the battery life of portable devices has become a major concern for consumers. This is where low power design comes in. By reducing the power consumption of electronic devices, low power design can help extend battery life, providing consumers with a better user experience.

Another reason for the need for low power design is the increasing demand for energy-efficient electronics. With the rising concerns over climate change and the depletion of fossil fuels, the need for energy-efficient electronics has become more critical than ever. Low power design can help reduce the power consumption of electronic devices, resulting in lower energy consumption and reduced greenhouse gas emissions.

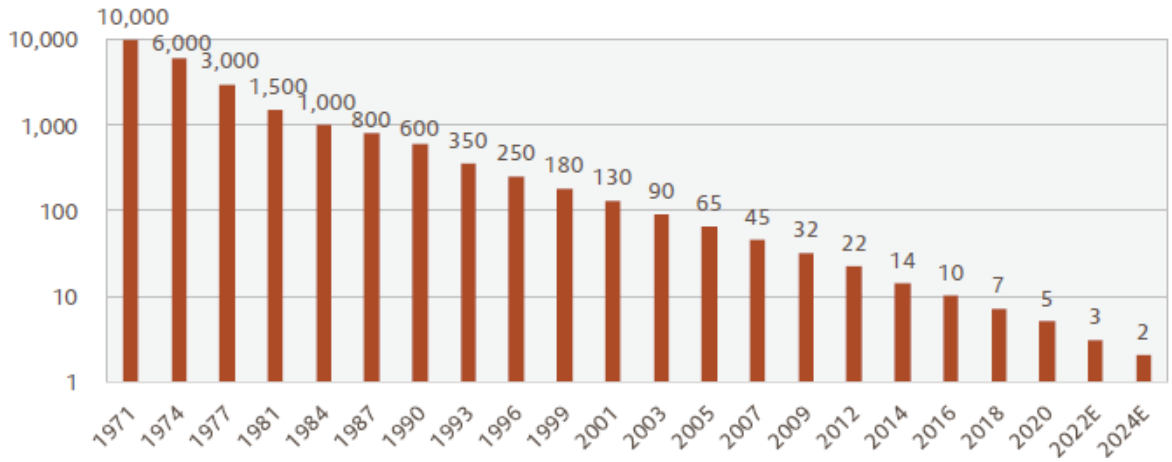

Figure 1.2 the incredible shrinking universe (device size in nm, log scale)

### 1.2.1 Applications of low power design:

There are wide range of application of low power in modern electronics. Some of the most significant applications are discussed below.

- Portable devices:

  As mentioned earlier, portable devices such as smartphones, tablets, and wearable's require long battery life to maintain their functionality throughout the day. Low power design is essential in these devices to reduce the power consumption of their components, such as the processor, display, and sensors, to extend battery life.

- Internet of Things (IoT):

  The Internet of Things is an assembly of devices that are interconnected and that can communicate with each other to perform various tasks. These devices are contains various sensors which are usually battery-operated and these sensors are not active always hence require low power design to decrease their power consumption to extend their battery life.

- Medical devices:

  Medical devices such as insulin pumps, pacemakers, and blood glucose meter are often implanted or worn by patients. These devices require long battery life and low power consumption to ensure their safe and continuous operation. Low power design is essential in these devices to reduce their power consumption and extend their battery life.

- Automotive electronics:

  Modern vehicles have a large number of electronic components, such as engine control units, infotainment systems, and advanced driver-assistance systems (ADAS). These components require low power consumption to reduce the unwanted power consumption and improve fuel efficiency. Low power design is essential in automotive electronics to reduce their power consumption and improve their performance.

## 1.3 LITERATURE SURVEY

The thesis aims to investigate low power CMOS VLSI design and power optimization techniques. The literature survey provide a comprehensive examination of relevant research papers across different aspects of low power CMOS VLSI design. Firstly, Dr. B.T. Geetha, B. Padmavathi, and V. Perumal's in [1] paper provides insights into various strategies for power reduction. Secondly, Asif Jahangir Chowdhury, Md. Shahriar Rizwan, Shahriar Jalal Nibir, and Md. Rifat Alam Siddique address the challenge of leakage power in portable applications with their paper [2]. Varsha Bendre and A. K. Qureshi in [3] offer, providing a comprehensive overview of leakage power reduction techniques.

Additionally, the thesis explores power optimization techniques in CMOS VLSI design through various research papers. A. Majumder, P. Deb, S. K. Yadav presents work on power and energy-efficient logic design utilizing the stacking effect of transistors in [4]. Malik and Sharma conduct a study on low-power SR-flip-flop design with ONOFIC implementation in [5]. S. M. Sharroush, Y. S. Abdalla investigate optimum sizing of sleep transistors in MTCMOS technology in [6]. S. Akashel, N. K. Tiwari2, J. Shrivas3,R. Sharma4 proposes a high-speed and power-efficient half adder design using MTCMOS technique in [7]. V. R. Nandyala* and K. K. Mahapatra contribute a circuit technique for leakage power reduction in CMOS VLSI circuits in [8]. N. V. Pramoda research focuses on advanced low power CMOS design for power consumption reduction in [9]. These papers collectively provide insights into various methodologies and techniques for power optimization in CMOS VLSI design.

Furthermore, the thesis explores the design of low-power CMOS multipliers using advanced technologies. Chalamalla R. P. B. Rajeshwari, and D. Laksmaiah present the design of a low-power CMOS array and tree multiplier using DSM technology in [10]. S. Rani, A. Kumar, V. Singla, and R. Singla conduct a performance analysis of different 8x8 bit CMOS multipliers implemented in 65nm technology, evaluating their efficiency and speed in [11]. R. S. Guindi and F. N. Najm investigate design techniques for gate-leakage reduction in CMOS circuits, focusing on minimizing leakage power consumption in [12]. These papers contribute valuable insights into the design methodologies, performance

evaluation, and power optimization techniques for low-power CMOS multipliers.

In the field of deep sub-micron CMOS circuits, several research papers have focused on reducing leakage current to enhance the performance and power efficiency of VLSI applications. M. Done, U. Panwar, K. Khare in [13] proposed an algorithmic approach for leakage current reduction, aiming to mitigate the leakage power dissipation in deep sub-micron CMOS circuits. S. Banu, S. Gupta in [14] explored leakage minimization techniques in semiconductor circuits specifically for VLSI applications. Their study emphasized the importance of reducing leakage current to improve the overall efficiency of semiconductor circuits. B. Deepikaa, D. Umamakeshwari in [15] investigated the use of a genetic algorithm for leakage reduction, offering an alternative approach to address this issue. They demonstrated the potential of genetic algorithms in optimizing circuit parameters for leakage power reduction. Furthermore, X.Chang, D. Fan, Y. Han, Z. Zhang in [16] proposed an algorithm that focuses on reducing leakage power in System-on-Chip (SoC) designs through input vector control. Their work aimed to minimize leakage power consumption during idle periods by manipulating input vectors. These papers collectively provide valuable insights into leakage current reduction techniques, highlighting algorithmic approaches, genetic algorithms, and input vector control as potential solutions for improving power efficiency in deep sub-micron CMOS circuits and VLSI applications

## 1.4 OBJECTIVE

Low power design encompasses various techniques that aim to reduce the power consumption of electronic circuits. The main objective of this thesis is to study the effectiveness and drawbacks of various leakage reduction techniques available, and to propose a software approach algorithm to overcome the drawbacks of hardware approach techniques. Another objective is to highlight the effectiveness of combining these approaches in the future to achieve even better results. Some of the commonly used techniques are:

1. Power gating: Power gating involves shutting off the power supply to inactive parts of a circuit. This technique reduces the power consumption of circuits by eliminating leakage current in idle parts of the circuit. The entire power of the given circuit cannot

be switched of as it might leads to high impedance state at the output of the circuit. So rather than shutting the entire supply we reduce the supply voltage to avoid unwanted high impedance state.

2. Clock gating: Clock gating is a technique that involves stopping the clock signal to inactive parts of a circuit. This technique can reduce dynamic power consumption by preventing unnecessary clock cycles in idle parts of the circuit.
3. Voltage scaling: In this technique we reduce the supply voltage of a circuit. This technique can significantly reduce the power consumption of circuits, as power consumption decreases exponentially with the reduction in supply voltage.
4. Energy-efficient design: Energy-efficient design involves designing circuits that use less power while maintaining their performance. This technique can be achieved by optimizing the circuit architecture, reducing unnecessary operations, and reducing the number of transitions in the circuit.
5. Adaptive voltage scaling: Adaptive voltage scaling is a technique that involves dynamically adjusting the supply voltage to a circuit based on its workload. This technique can reduce power consumption without compromising the performance of the circuit.

These techniques can be applied individually or in combination to achieve low power design. The choice of technique depends on the application and the level of power reduction required.

All of these techniques requires modification in the hardware i.e. we need to add extra steps in the fabrication process or need extra transistors. We are exploring only the hardware approach till now, though these are very effective but requires through knowledge of the hardware and are costly. So we need to change our perspective and consider software approach towards leakage reduction. Thus in this thesis we will try a software approach to deal with the problem of leakage power dissipation. We will be using IVC for the purpose. Another motivation behind this thesis is that, when a circuit is not in use i.e. it is in static state we assume that keeping all the inputs to zero's which is default state our circuit is minimum leakage state. But this is not always true minimum leakage state can correspond

to any input vector and there is no compulsion that all zero's will give a minimum leakage state as all zero's means all PMOS will be on and conducting which might increase leakage current. This can be easily demonstrated with the help of a basic CMOS NAND gate circuit. The below figure demonstrate the 4 transistor based CMOS NAND gate and transistors that facilitates leakage current or leaky transistors corresponding to each input vector combination.

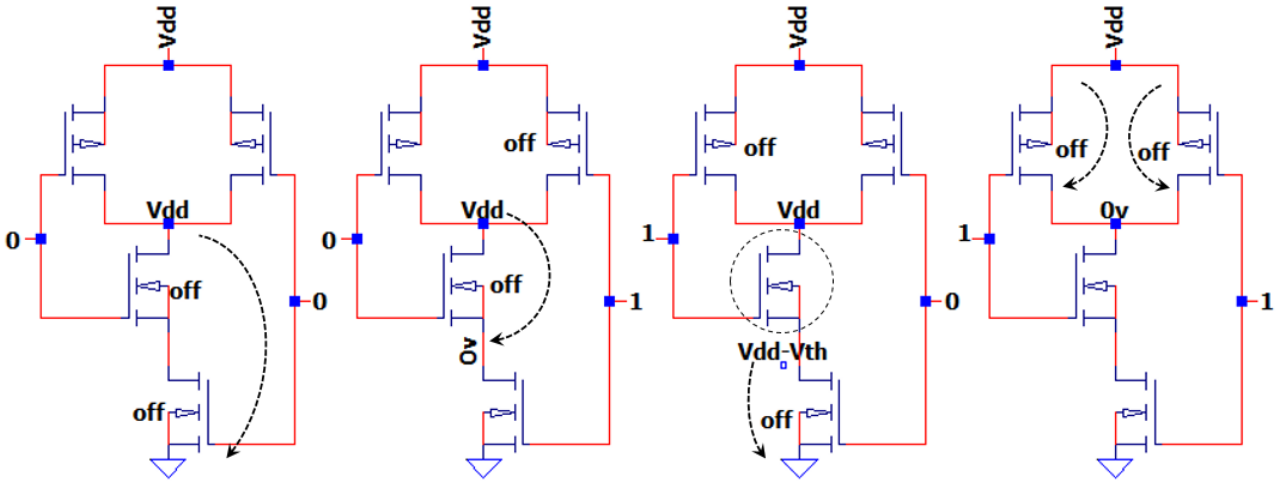


Figure 1.3 Transistors contributing to leakage in a 2 input NAND gate for all input combination.

# Chapter 2: Basic Terminologies

This chapter will provide a brief description of the basic terminologies that are used throughout the thesis.

## 2.1 TYPE OF POWER DISSIPATIONS

When we consider power utilization as a factor of design, power per MHz becomes an important parameter. Understanding the type of power dissipation becomes important to calculate power that is been used in driving the circuit and power that is been dissipated uselessly. Power minimization is possible only if we have a clear idea of where the total power consumed by the circuit is been utilized.

The total power consumed by an inverter can be can be categorized into 2 basic classes

1. Static power
2. Dynamic power

### 2.1.1 Static

CMOS circuits are based on the principle that either one network in on a given point of time and the other part of the network is off and offers infinite resistance to flow of current Leakage current exists as a natural phenomenon in semiconductor devices due to the presence of minority carriers and formation of PN junction. Generally, leakage current serves no useful purpose and increases power dissipation. Although, the leakage current is negligible compared to total current but becomes a matter of concern when we are dealing with low power applications and the number of transistors is huge. The major sources of leakage current are: A) Reverse biased PN junction and, B) Sub threshold leakage current..

### 2.1.2 Dynamic

The dynamic power dissipation arises due to two factor firstly due to charging and discharging of parasitic capacitor, secondly due to short circuit current.

1. Charging and discharging of capacitor: When a CMOS circuit is design the parasitic capacitor and capacitance offer by nextstage is cumulatively modeled as load capacitor C load at the output node as shown in figure 3.2.1.Whenever the input switches

depending upon the logic this output Capacitors charges or discharges. This capacitor is charges through pull up networkand discharges through pull down network. During charging this capacitor draws current from the voltage source hence consumes power which is stored in form of output voltage on capacitor and half of the power drawn is dissipated in form of heatin the Pull Up network due to finite non zero resistance, and during discharging thisstored power is discharged to ground through NMOS circuit. Thus whenever the output switches some amount of power is consumed by the circuit which is given by:

$$P = CVdd^2f$$

2. Another source of power dissipation is short circuit power. When the input switchesdue to finite rise and fall time of the signal the NMOS and PMOS circuit are on simultaneously which is quite against the basic principal of CMOS circuit design, thus leads to a direct path between Vdd to ground. This direct path leads to a flow of unwanted spike of current hence consumes power.

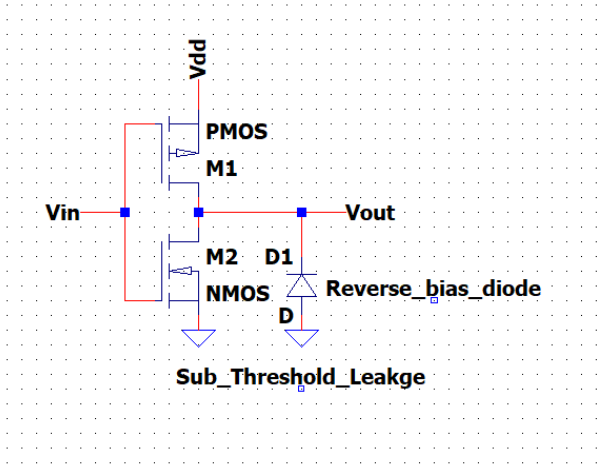


Figure 2.1: CMOS Inverter Dynamic power.

## 2.2 SOURCES OF LEAKAGE POWER

### 2.2.1 Sub threshold

The second major source of leakage in CMOS circuit is sub threshold leakage through MOS device. The basic condition for a MOS device to turn ON is to apply a gate voltage exceeding the threshold voltage, if this condition is not satisfied the device is supposed to

be OFF that is no current flows through the channel. But, in practical case a very small amount of current flows through the device. This current is mainly due to minority charge carriers. This sub threshold current is the major contributor of the leakage current in the circuit. The magnitude of the sub threshold current depends upon Vgs, Vds and ambient temperature which makes it a complex function of the mentioned parameter. Hence it, become problematic to estimate the leakage current.

### 2.2.2 Reverse biased diodes

Complementary metal oxide semiconductor (CMOS) circuit's work on the principle that only one part of the network either pull-up or pull-down is active at a time and the other is switched off. At that point when the transistor is off, junction leakage occurs due to the formation of reverse bias condition. The reverse bias junction facilitates the flow of reverse bias current due to generation of electron hole pair in the depletion region. The generated electron hole pairs that drift to the nearest depletion region causing junction leakage current. For instance, in the event of an inverter, when input is high, the NMOS is ON, the PMOS is OFF and the yield voltage is low. Thus, the voltage across OFF PMOS is equivalent to supply voltage, this causes a leakage current from drain to source.

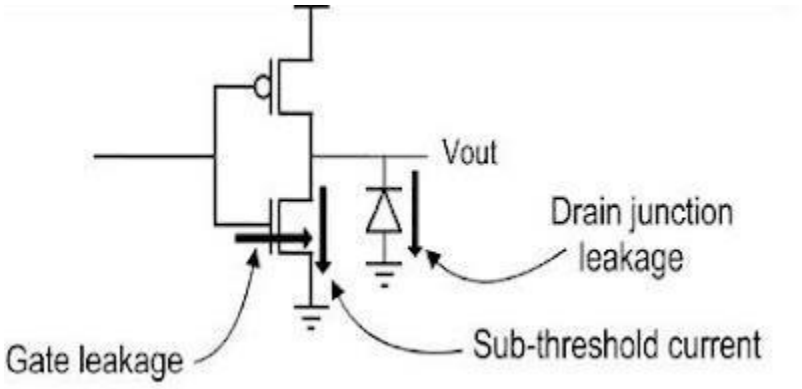


Figure 2.2: CMOS Inverter with sources of leakage power [17].

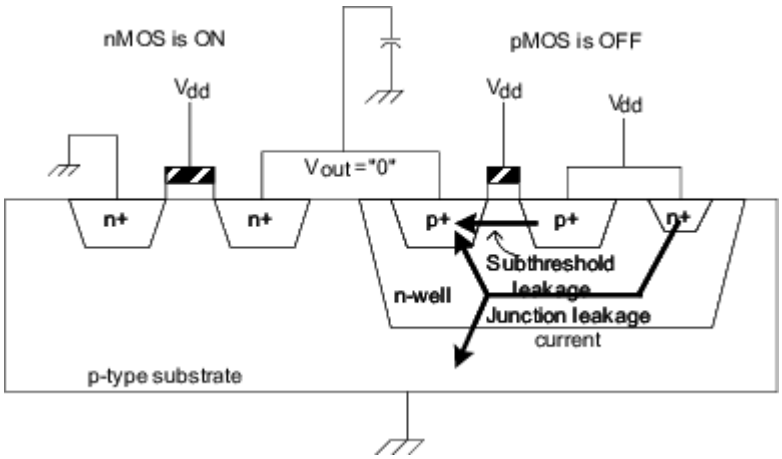


Figure 2.3: CMOS inverter sources of leakage (layout) [17]

## 2.3 CONVENTIONAL LEAKAGE REDUCTON TECHNIQUE

Conventional CMOS: In this technique of circuit design complementary pull up and pull down network is design in such a way that only one network conducts at a time. Pull up network comprises of PMOS and whereas pull down network comprises of NMOS. The output is taken in between this two network as shown in figure 2.4

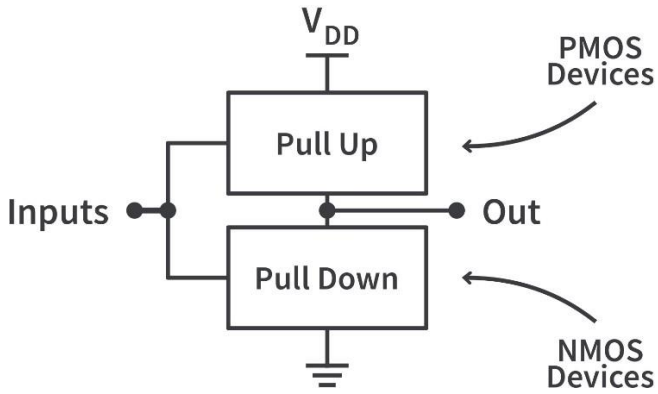


Figure 2.4: Conventional CMOS circuit [17].

The design of leakage power technique at circuit level is an important approach for any design as at circuit level thing can be handled much more efficiently as compare to other level of abstraction. Many methods and technique are available for low power reduction, in this project we are mainly focused on leakage power and technique related to it are discussed and compare to conventional CMOS.

Few key circuit level methods in low power VLSI describe below.

### 2.3.1 Stacking

As current is inversely proportional to the resistance by increasing the resistanceand keeping the voltage constant, an effective reduction in the current can be observed. The stacking technique uses the above principle to reduce the static current [1]. In this technique a transistor is replaced by two transistors of half dimension (W/L) ratio. As the W/L ratio of individual transistors are reduced by 50%, the resistance is increased by four times keeping the capacitance same. Both the associated transistors are killed together, hence, reducing the leakage current. The above method reduces the sub-threshold overflow exponentially hence, saving a lot of overflow power. Figure-1 demonstrate a circuit schematic for the same.

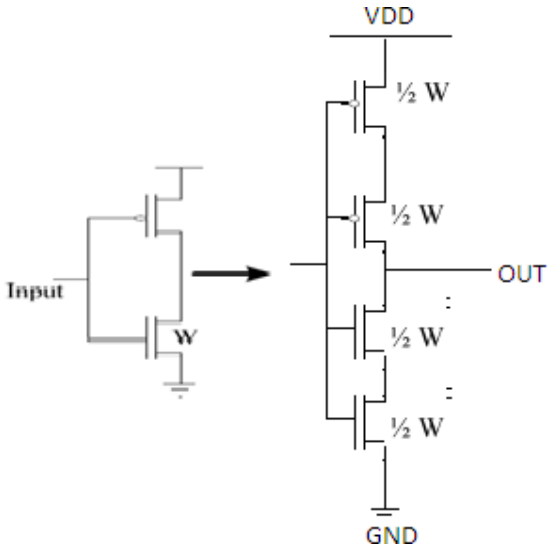


Figure 2.5: Stacking technique for leakage reduction [1]

### 2.3.2 ONOFIC

The ON/OFF (ONOFIC), aims to deliver the same functional logic network which considerably reduces leakage current and hence less leakage powerdissipation. In this approach we insert a separate logic block containing a NMOS and a PMOS transistor which is placed in the core of the circuit where output node is connected, which focusses on providing a better on/off propertythan the conventional CMOS. In this logic block, the gate terminal of NMOS is tied to the drain terminal of the PMOS and gate terminal of the PMOS transistor is connected to the output of the circuit. The source of the NMOS is tied to the

drain terminal of the PDN of the circuit. The drain terminal of NMOS transistor is connected to the output of the circuit [2].

When the input is at logic low, both the NMOS and PMOS devices of ONOFICblock turn off and provides an extra isolation to prevent any charge leakage to the PDN. Conversely, when the input is at logic high, the ONOFIC block turns on and provides a conducting path for the charge stored in capacitor to flow to ground through PDN [3]. Therefore, it produces the correct logic level at output without any degradation in quality and minimized the leakage current in both active and static modes. Figure-2.6 depicts a circuit schematic for the same.

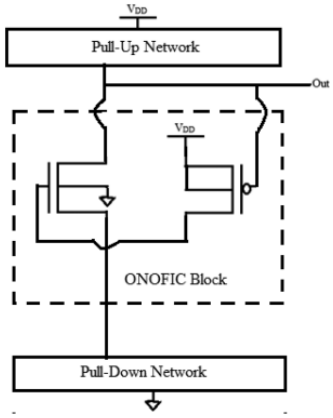


Figure 2.6: ONOFIC technique for CMOS circuits [2].

### 2.3.3 MTCMOS

As we have already discussed in the previous sections, the leakage current shares an inverse relation with the threshold voltage. In order to reduce the leakage current, the threshold voltage of the device can be increased but as a consequence, the device becomes slower. Hence, we observe a clear trade-off between power and delay. The Multiple Threshold CMOS (MTCMOS) technique tries to balance the above trade off [9] .In this approach, we use two sleep transistors with higher threshold voltage in series with the PDN and PUN, which reduces the leakage current.

The threshold voltage of the core transistor circuit is reduced below the normal value to compensate the delay introduced due to sleep transistors with high threshold voltage. A sleep signal is required for controlling the sleep transistors. During the active phase, the

sleep transistors are turned ON which provides virtual ground and virtual power to the core circuit. Whereas during inactive phase the sleep signal is de asserted, forcing the sleep transistors to turn OFF. These two turned-off sleep transistors offer high resistance to the leakage current as compared to the normal transistors.

Thus, a circuit with multiple threshold voltage is designed which enhances the performance and provides low power dissipation. The figure-2.7 depicts an LTSpice implementation of MTCMOS inverter.

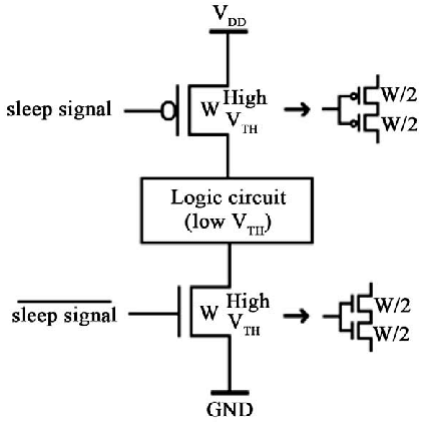


Figure 2.7: MTCMOS technique for CMOS circuits [9].

### 2.3.4 LECTOR

Principal used in above technique to reduce the leakage is to increase the resistanceof the off path by stacking the number of transistor. But these transistor need to becontrolled according to input i.e. these transistor should be on whenever requiredand off whenever not in use. To do so we need to use an extra external signal tocontrol the transistor or we have to attaches them to input, but both of this approachposse their own drawback thus to solve this problem we use LECTOR technique. Figure 2.8 shows a simple CMOS circuit implemented by using lector technique.

In this approach, we use two transistor LCTs (leakage control transistor) in the coreof the network. As these transistor are self-controlled lector overcome the drawbackof use of external signal to control them. In this technique one PMOS is used to pullup the output and one NMOS is used to pull down the output, and both of the transistor are controlled by wellspring of each other. Therefore one of the LCTs are always close hence offer extra

resistance from Vdd to ground hence helps in controlling the sub threshold leakage.

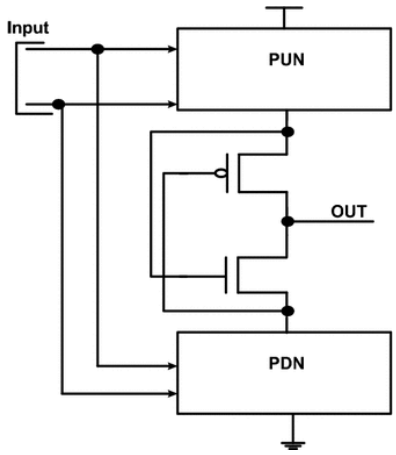


Figure 2.8: Lector technique in CMOS [10].

## 2.4 ARRAY MULTIPLIER

Digital signal processing and other fields, major applications make use of multipliers. In response to advancements in modern technology, a lot of researchers have focused mostly on design elements to improve performance, high speed, accuracy, low power consumption, layout regularity, and minimal size [14]. The fundamental components computational block of a DSP processor include multiplexers, adders, and MACs. To increase the speed of the DSP processor these blocks needs to operate and execute promptly. The factors affecting how quickly multipliers operate are semiconductor technology and multiplier architecture. The fundamental component of digital multiplexers are adders, which are used to do a series of repeated adds and And gate to obtain the partial product. By speeding up the adder action, the multiplier function can be completed more quickly. There are different topology of multiplier are available namely Booth multiplier, combinational multiplier, Wallace tree multiplier, array multiplier, sequential multiplier, which have their own advantages and disadvantages. In this project I have used array multiplier to implement a low power multiplier.

### 2.4.1 Construction and Working of a 4×4 Array Multiplier

The design structure of the array Multiplier is regular, it is based on the add shift algorithm principle. Array multiplier is a structured combination of and gates and Adder block (1-bit

half adder and 1-bit full adder) to generate product of two numbers. It accepts all the inputs simultaneously to generate the partial product and these partial product are added to obtain the final result, thus the delay of the entire process completely depends on the addition process. An array multiplier consists of two stages. First, all the bits of input are Anded to get $n^2$ partial products, second all the partial products are combined and added to get either next set of partial product or final bits of the output. An n x n array multiplier consists of $n^2$ And gates and n*(n-2) 1-bit full adders and n 1-bit half adder.

Thus, the above structure forms an array of and gate and adders hence it is known as array multiplier.

Partial product = the multiplicand * multiplier bit……. (2)

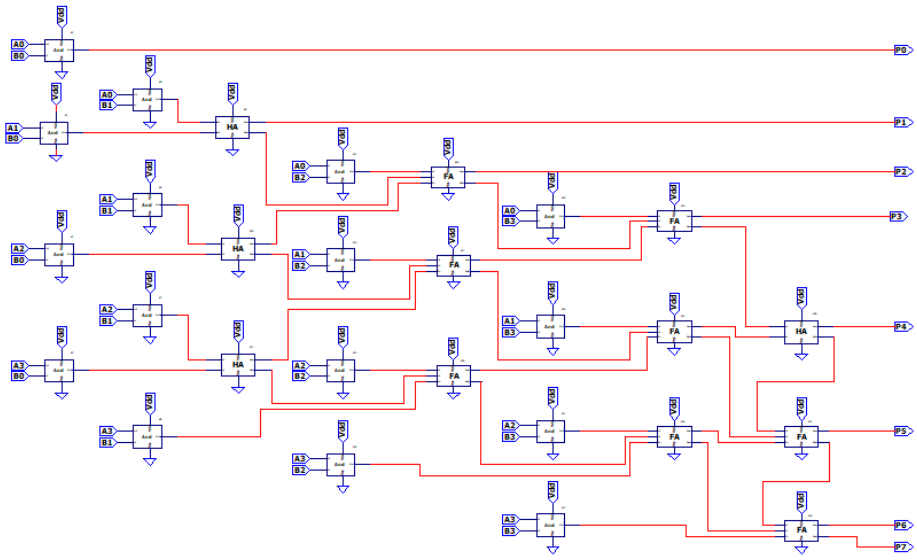


Figure 2.9: 4X4 Array multiplier

## 2.5 IVC

The leakage power has become a crucial contributor in total power consumption in modern CMOS circuits due to the scaling down of device dimensions and increasing transistor densities. Ideally when the transistor is not switching i.e. the circuit is in static state, it should not consume power but a small amount of current known as leakage current still flows to the circuit due to reverse-biased junctions of transistors and this current contributes to static power dissipation.. As the size of transistors shrinks, the doping levels in the junctions must also decrease to maintain the same electric field strength. This results in

higher leakage currents, which can lead to significant power dissipation in the off-state. To mitigate the effects of leakage power, several techniques have been proposed, including input vector control.

Input vector control is a technique that involves controlling the input pattern of a circuit to reduce leakage power consumption. The idea behind this approach is to manipulate the input vectors such that the transistors in the off-state are biased in such a way that their leakage currents are minimized. The basic principle behind input vector control is to avoid activating transistors that are not needed for the desired output response of the circuit.

In this chapter, we will discuss the input vector control (IVC) technique in detail, its type and efficiency in reducing leakage power consumption in CMOS circuits.

### 2.5.1. Input Vector Control Technique:

The input vector control technique involves controlling the input patterns of a circuit to reduce leakage power consumption. This technique works by biasing the transistors in such a way that their leakage currents are minimized. The basic principle behind input vector control is to avoid activating transistors that are not needed for the desired output response of the circuit.

There are two methods to apply the input vector control technique: static input vector control and dynamic input vector control. Static input vector control involves designing input patterns that decrease the amount of power lost while the device is off. In dynamic input vector control, the input patterns are modified dynamically based on the circuit's output response.

Static Input Vector Control:

In static input vector control, the input patterns are designed to reduce the leakage power consumption in the off-state. The basic idea behind static input vector control is to identify the inactive transistors in a circuit and avoid activating them in the input pattern. This can be achieved by analyzing the circuit's structure and identifying the transistors that are not necessary for the desired output response.

One common approach for static input vector control is to use a test pattern generator (TPG) to generate input patterns that minimize the leakage power consumption. The TPG

analyzes the circuit's structure and generates input patterns that activate only the necessary transistors. This approach is effective in reducing leakage power consumption but may not be practical for larger circuits.

Another approach for static input vector control is to use a Boolean (SAT) solver to find an optimal input pattern that minimizes the leakage power consumption. The SAT solver analyzes the circuit's structure and finds an input pattern that activates only the necessary transistors. This approach is more flexible and can handle larger circuits, but it may not be as efficient as using a TPG.

Dynamic Input Vector Control:

In dynamic input vector control, the input patterns are modified dynamically based on the circuit's output response. The basic idea behind dynamic input vector control is to analyze the output response of the circuit and modify the input patterns to reduce the leakage power consumption.

One common approach for dynamic input vector control is to use a feedback mechanism to adjust the input patterns. The feedback mechanism monitors the circuit's output response and adjusts the input patterns to minimize the leakage power consumption. This approach is effective in reducing leakage power consumption but may introduce additional overhead in the circuit.

Another approach for dynamic input vector control is to use a neural network to predict the optimal input patterns based on the circuit's output response. The neural network analyzes the circuit's structure and output response and predicts the optimal input pattern that minimizes the leakage power consumption. This approach is more flexible and can handle.

# Chapter 3: HARDWARE APPROACH

In this chapter, the hardware approach for leakage reduction is discussed. All the techniques mentioned in this section require extra hardware (transistors), which is why they are referred to as hardware approaches. The techniques discussed operate on the principle of increasing the resistance of the circuit to reduce leakage current. Some of the techniques discussed below include stacking, lector, ONOFIC, and MTCMOS. To showcase the effectiveness and the various trade-offs related to these techniques, they are being used on multipliers, which are large circuits that require a large number of transistors. All of the above-mentioned techniques are used to design a 4x4 multiplier, and static power and maximum delay are calculated for various combinations of inputs. The average of all these inputs is considered for power, and the maximum value of delay is also considered. All of these multipliers are designed using a hierarchy approach and by using AND gates, Half Adders, and Full Adders

## 3.1 CMOS MULTIPLIER

Multiplier is implemented using LTSpice with level 54. model file.

Table 01: Aspect ratio of CMOS Inverter.

| Parameters | NMOS | PMOs |
|---|---|---|
| Width | 72nm | 144nm |
| Length | 36nm | 36nm |
| Vth | 0.501 | -0.452 |

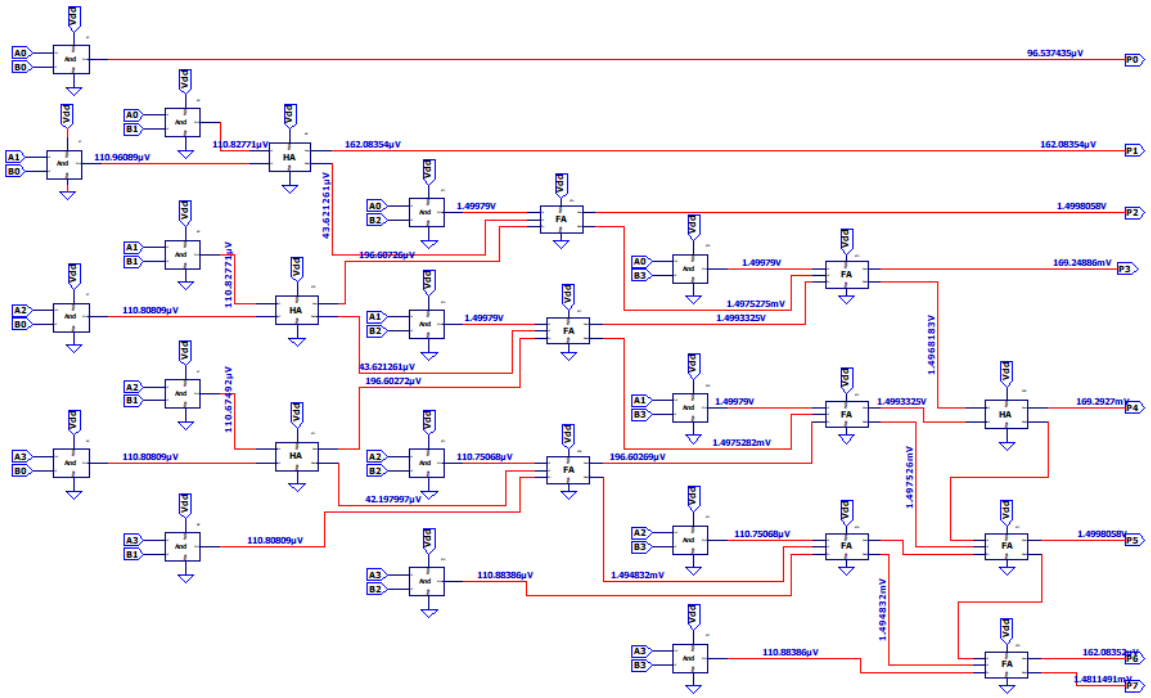


Figure 3.1: CMOS Multiplier Lt Spice Schematic.

The screenshot above shows a 4x4 CMOS array multiplier which uses 16 AND gates, 8 1-bit full adders, and 4 1-bit half adders. It has 4-bit 2-input (A3, A2, A1, A0) and (B3, B2, B1, B0) and an 8-bit output (P7, P6, P5, P4, P3, P2, P1, P0).

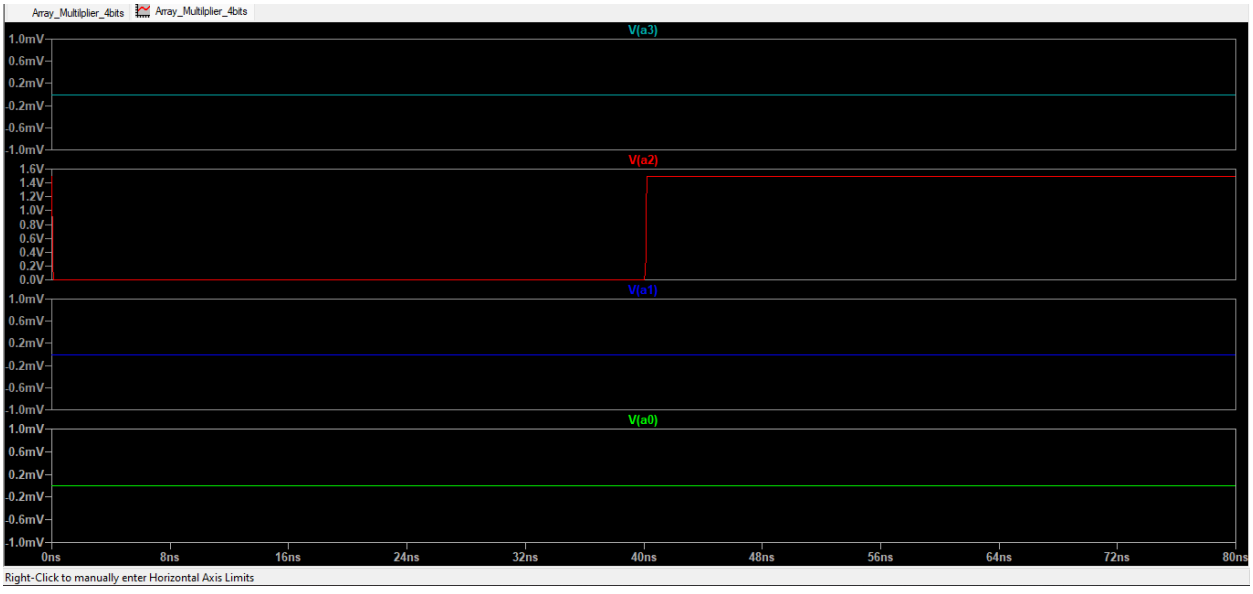


Figure 3.2: CMOS 4x4 Multiplier 1st Input (0100 = 4).

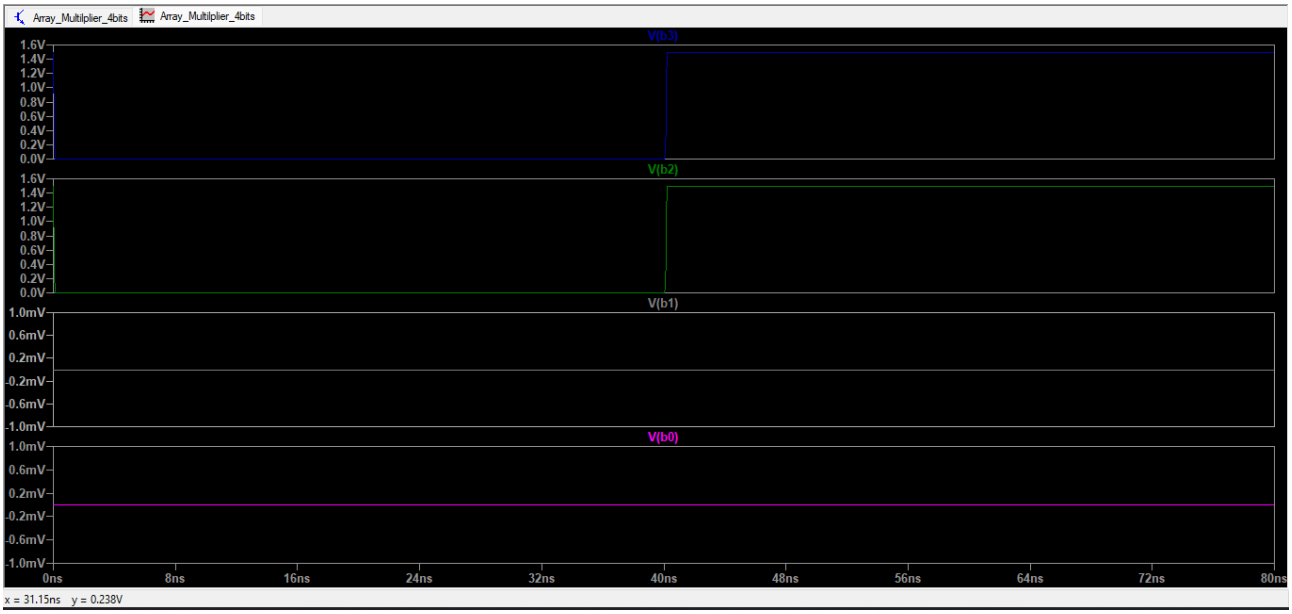


Figure 3.3: CMOS 4x4 Multiplier 2nd Input (1100 = 12).

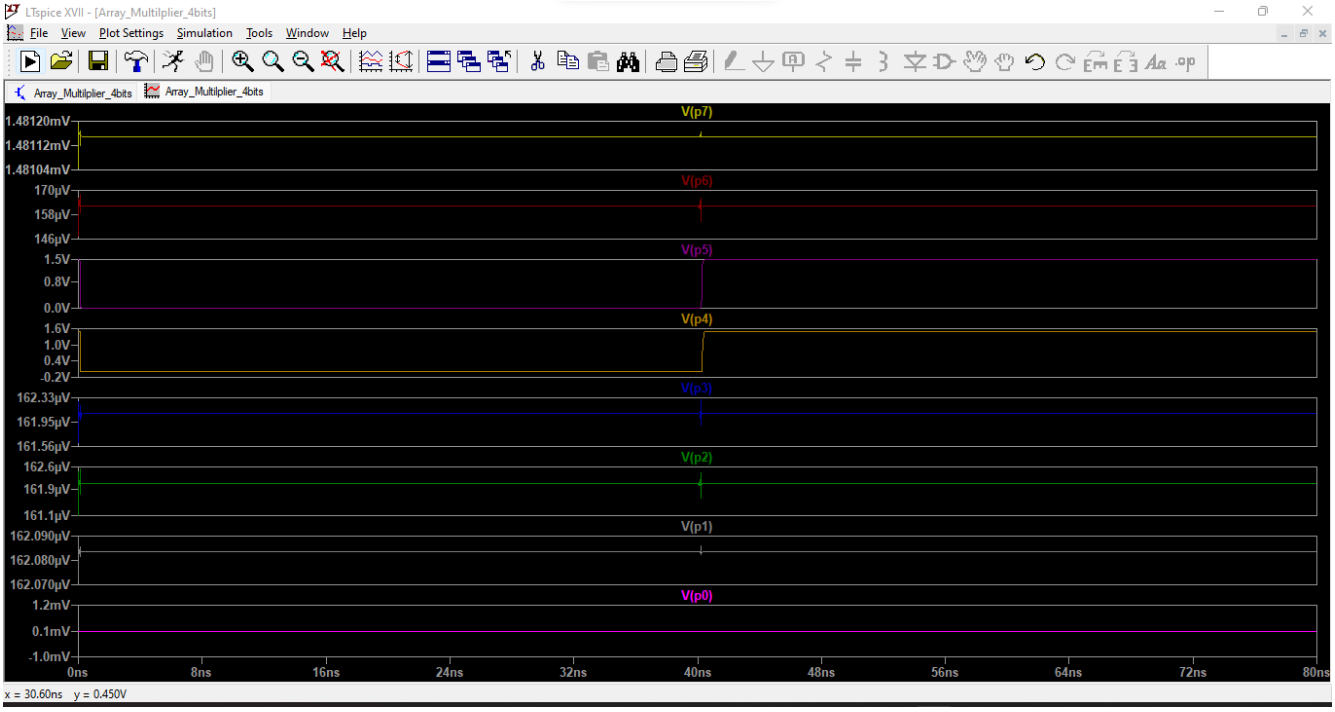


Figure 3.4: CMOS 4x4 Multiplier output (00110000 = 48).

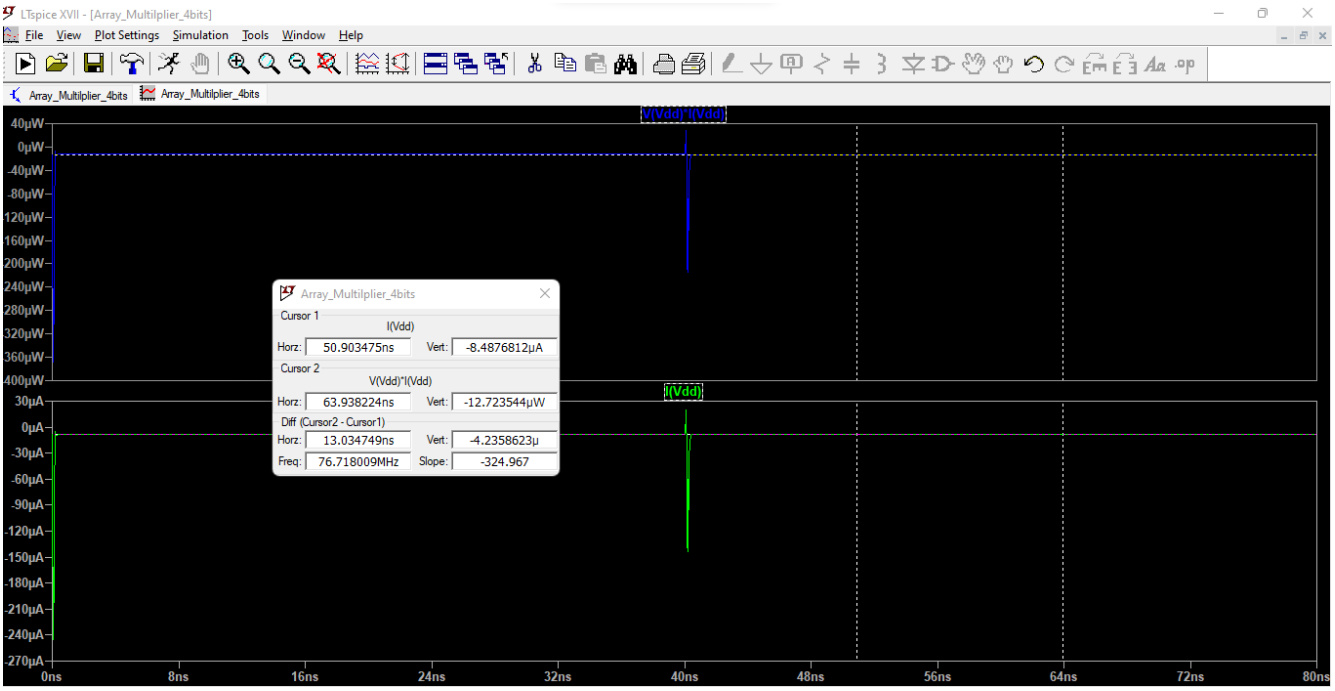


Figure 3.5: CMOS 4x4 Multiplier I static and static Power.

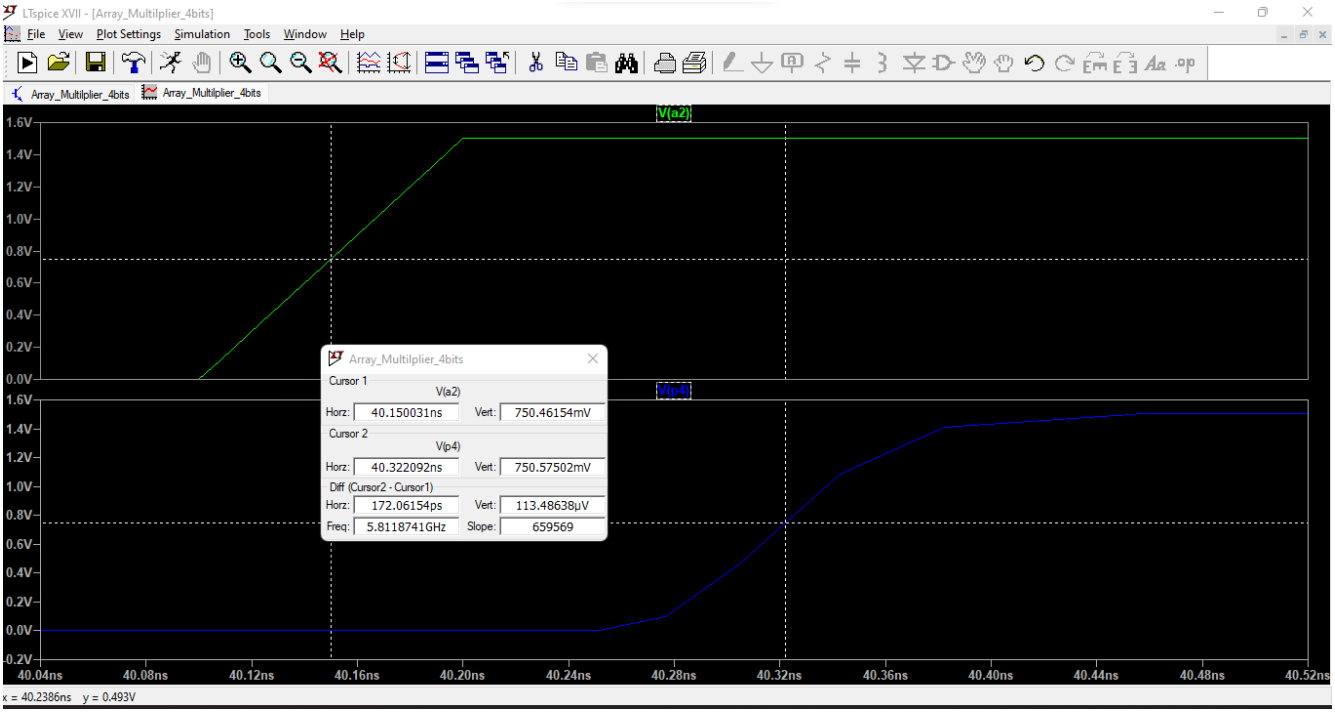


Figure 3.6: CMOS 4x4 Multiplier input to output delay.

**Results:**

Table 02: Istatic and Power dissipation

| Sl. No. | Product | $I_{static}(\mu A)$ | Power ( $I_{static} \times V_{dd}$ )($\mu W$) | Delay(psec ) |
|---|---|---|---|---|
| 1. | 15x15 | 336.29214 | 504.43821 | 192.06923 |
| 2. | 15x10 | 117.64559 | 176.46839 | 232.19231 |
| 3. | 10x10 | 35.702906 | 53.554359 | 157.98462 |
| 4. | 4X12 | 8.478627 | 12.717941 | 172.06154 |
| 5. | 0x0 | 7.8968669 | 11.8453 | 0.0 |

Table 03: Delay and Average Power dissipation

| Parameter | $I_{static}(\mu A$ ) avg | *Pstatic(*$\mu W$*) avg* | $\text{Delay}_{\text{Max}}$(*psec*) |
|---|---|---|---|
| CMOS | 101.203226 | 151.80484 | 232.19231 |

All of the mentioned techniques were applied using the above approach, and the results were consolidated into a table presented below.

Table 04: Comparison table of various technique of CMOS Inverter.

| Parameter /Techniques | CMOS | Stacking | LECTOR | ONOFIC | MTCMOS Active | MTCMOS Sleep |
|---|---|---|---|---|---|---|
| **No. of transistor** | 464 | 928 | 800 | 800 | 466 | 466 |
| **I Static (Avg) (µA)** | 101.203 | 2.142 | 2.762 | 6.335 | 27.998 | 0.0216 |
| **Power Static (Avg) (µW)** | 151.804 | 3.213 | 4.143 | 9.503 | 41.993 | 0.0324 |
| **Delay (Max) (psec)** | 232.192ps | 514.461ps | 429.777ps | 270.276ps | 409.707ps | N/A |

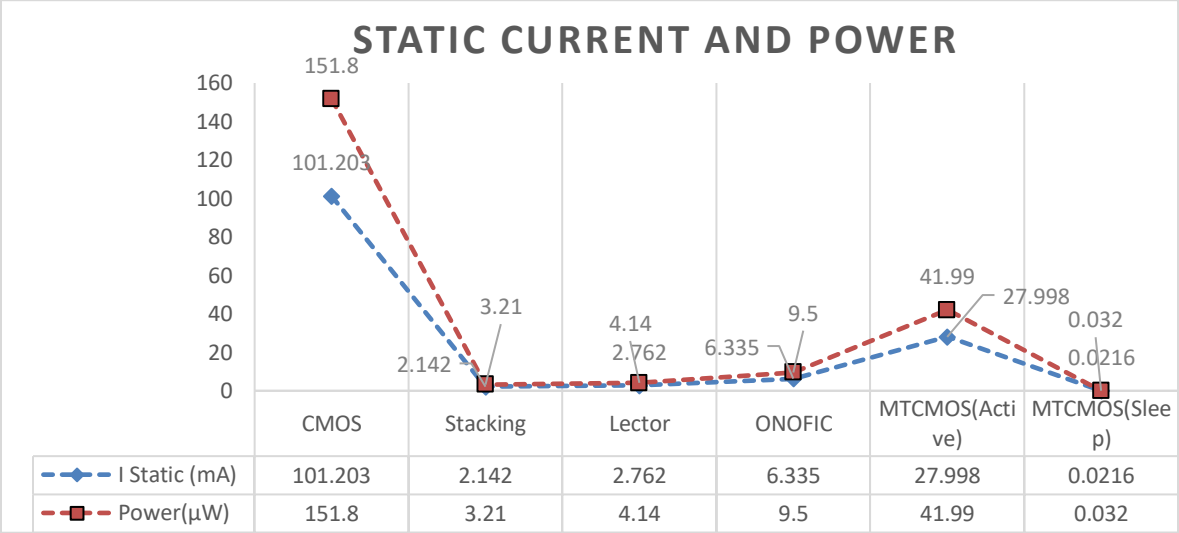


Fig 3.7: Graph representing Technique Vs I static & Power

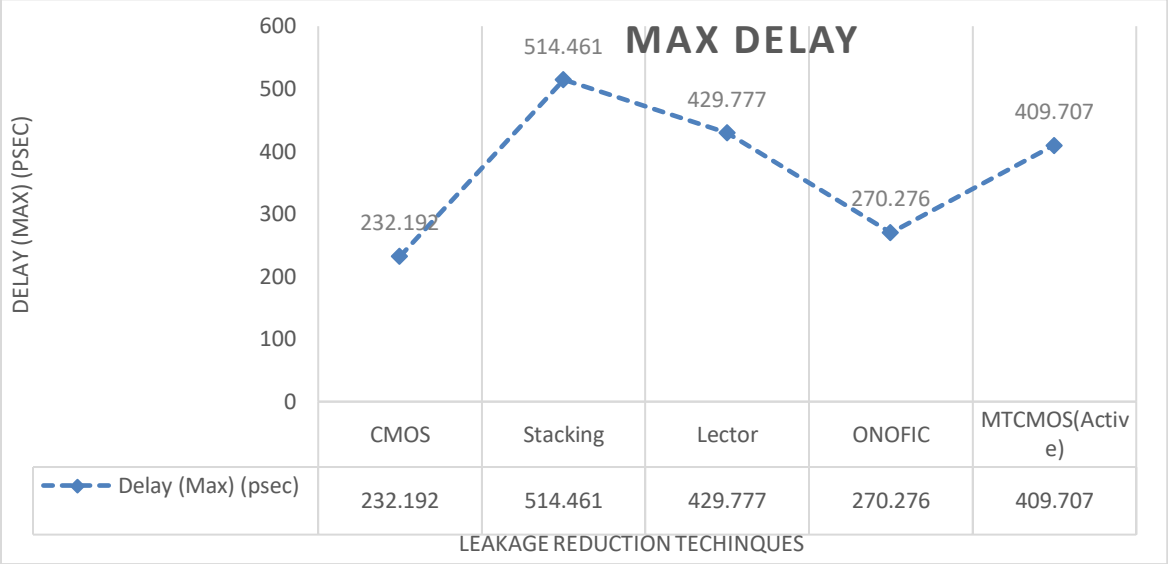


Fig 3.8: Graph representing Technique Vs Max Delay

# Chapter 4: IVC

In this section we will discuss about the proposed algorithm to find IVC for any given NAND based circuit. Later we will validate the output of the algorithm with the help of LTspice simulation of the same circuit with all input vector and by measuring the corresponding static current and static power dissipation. By measuring static current and static power for all the combination of input vector will help us validate our algorithm efficiency and we will also be able to calculate the percentage save in power from the default state i.e. all zero input.

The proposed algorithm is based on the fact that when the circuit is not in use

## 4.1 PROPOSED ALGORITHM

The proposed algorithm was developed using python as it has inbuilt libraries and functions which are quite handy for these kind of operations. We will divide this section into 3 part that will help us to understand the correct flow of and intent of the algorithm.

### I. Input

Our algorithm accepts the text description of the NAND based combinational circuit. In the text document the circuit is described using the key word NAND and then its 2 input nodes are listed followed by its output node. The below format shows an example of single NAND gate.

*Netlist as input(NAND based circuit)*

*Input the circuit in the form of:*

*"""Nand {NAND gate number} I{1st input in number} I{2nd input in number} n{same as nand gate in number}"""*

*Ix 'I' represents input & 'x' input number*

*ny 'n' represents output & 'y'th nand gate*

*"""""""""""""""""""""""""""""""""""""""""*

*Nand1 I1 I2 n1*

*"""""""""""""""""""""""""""""""""""""""""*

Next text format is for a 2 input XOR gate

*Netlist as input(NAND based circuit)*

*Input the circuit in the form of:*

*"""Nand {NAND gate number} I{1st input in number} I{2nd input in number} n{same as nand gate in number}"""*

*Ix 'I' represents input & 'x' input number*

*ny 'n' represents output & 'y'th nand gate*

*""""""""""""""""""""""""""""""""""""""""*

*Nand1 I1 I2 n1*

*Nand2 I1 n1 n2*

*Nand3 I2 n1 n3*

*Nand4 n2 n3 n4*

*""""""""""""""""""""""""""""""""""""""""*

**II** Algorithm

The above mentioned text format is given input as a .txt file to the python code for further process. The algorithm is divided into steps wise process for generating the result.

Step 1. Scan the given text file for number of NAND gates and number of inputs.

Step 2. Create a logical NAND gate for generating the output.

Step 3. Generate the all possible combination of input vector.

Step 4. Each input vector is then applied to circuit to find the states of every input node of the each NAND gate and generate a list.

Step 5. Now each pair of input for each NAND gate is assign a weighted score depending on the amount leakage caused by that pair of input, as shone in table no.04.

Step 6. Now all the weighted score for each NAND gate is sum up to find the final score corresponding to each that input vector. And score corresponding to each input vector is then saved in a list.

Step 7. After the step 6 we have a list of score corresponding to each input vector and hence the input vector with least score corresponds to least leakage state for that circuit.

Below given flow represents the flow diagram of the proposed algorithm.

Table No. 05 weight score according to leakage current

| Input Vector | $I_{STATIC}$ in nA | Weighted Score |
|---|---|---|
| 00 | 6.11 | 2 |
| 01 | 15.50 | 5 |
| 10 | 3.33 | 1 |
| 11 | 42.08 | 4 |

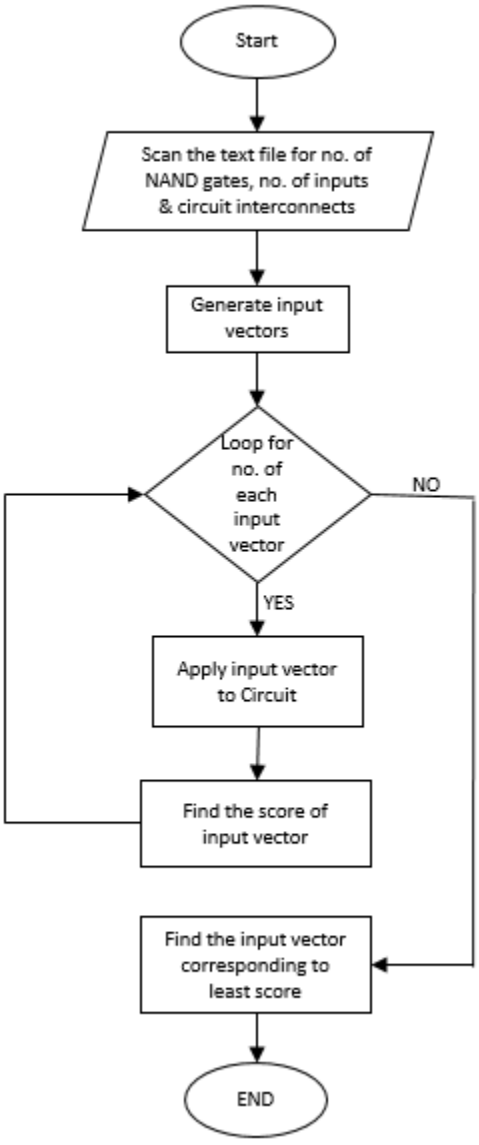


Figure 4.1: Flow chat for proposed algorithm.

III Output

Finally the core displays the score of each input vector and input vector corresponding to minimum leakage state. Hence when the given circuit is not in uses i.e. circuit is in static state then the given input vector will result in minimum leakage state.

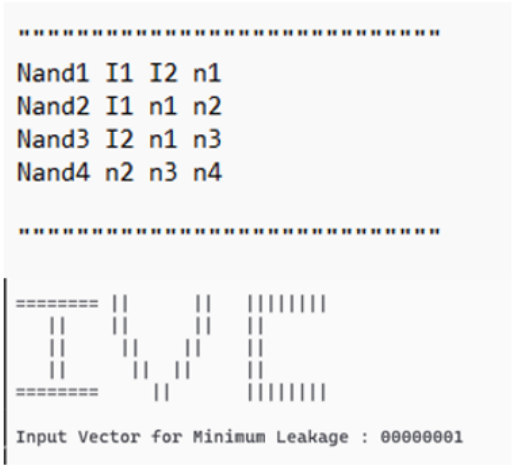


Figure 4.2: Input for the algorithm, a textual representation of NAND circuit and the output from the code.

## 4.2 Ltspice SIMULATION.

Ltspice tool was used to simulate the NAND based circuit for verification of the proposed algorithm. Symbol based approach was used to create a symbol of a NAND gate and it was further used to design NAND based combinational circuit. And the same circuit schematic was converted to text file and was used as an input to the algorithm to generate IVC for minimum leakage state.

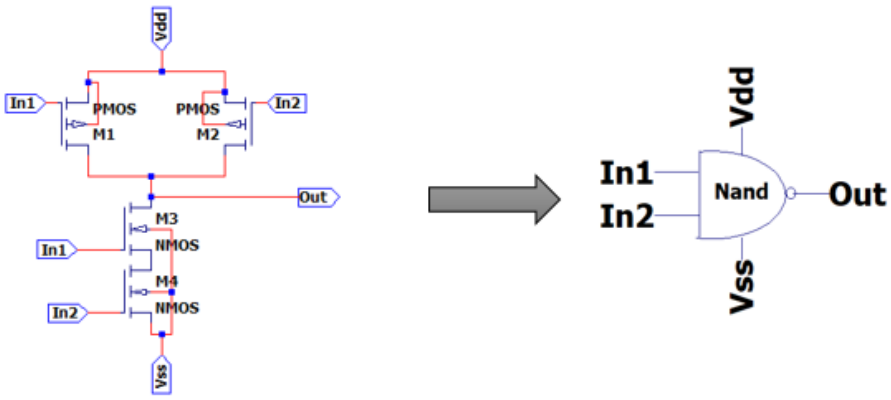


Figure 4.3: Ltspice simulation of NAND gate and Symbol created for the same.

NAND symbol was creates using CMOS approach as shown in the figure 4.3. Two PMOS and two NMOS transistors was used was used where for pull up network two PMOS transistor was connected in a parallel and for pull down network two NMOS are connected in series to form a complementary structure. NAND gate is implemented using LTSpice with level 54. model file.

Table 06: Aspect ratio of CMOS Inverter.

| Parameters | NMOS | PMOs |
|---|---|---|
| Width | 72nm | 144nm |
| Length | 36nm | 36nm |
| Vth | 0.501 | -0.452 |

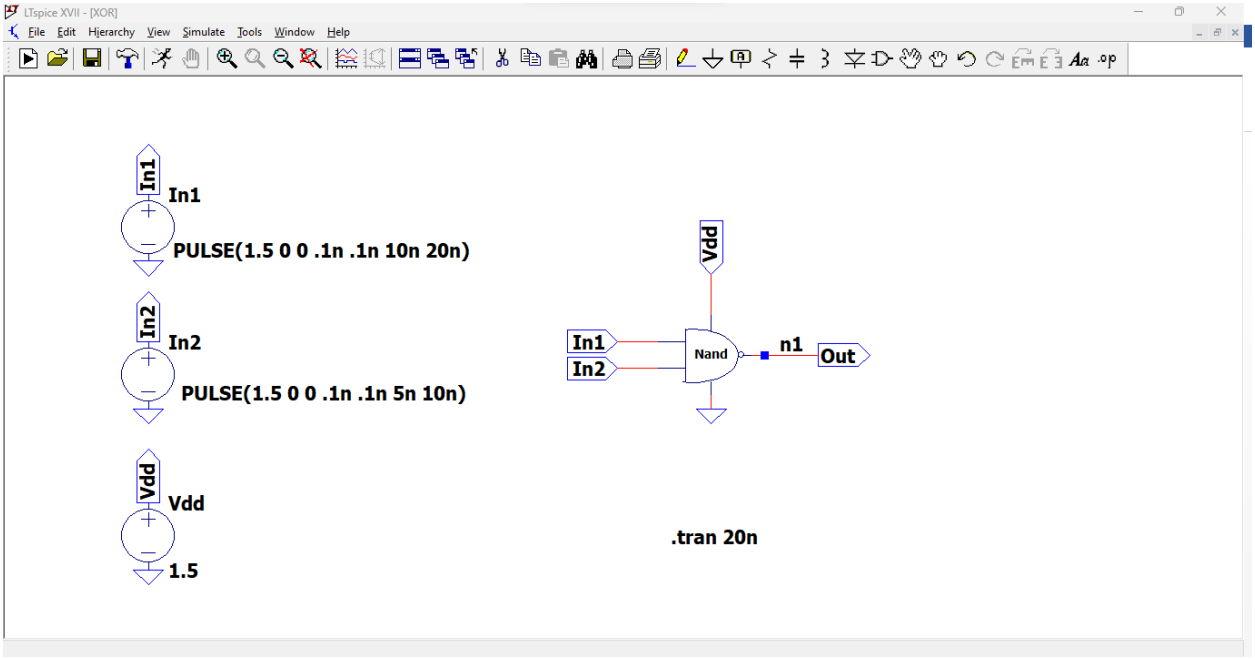


Figure 4.4: Ltspice simulation of NAND gate.

The below snapshot shows the functional working and leakage current waveform of a NAND gate. The first waveform (green) represents the first input IN1 of the NAND gate, with values 0 -> 0 -> 1 -> 1. The second waveform (red) represents the second input IN2 of the NAND gate, with values 0 -> 1 -> 0 -> 1, forming all four combinations of the two-input gate. The third waveform (red) shows the output of the NAND gate, while the fourth waveform (light-blue) shows the corresponding leakage current in nA for each input

combination.


Figure 4.5: The output waveform for the simulation of a two-input NAND gate with leakage current for each input combinations.

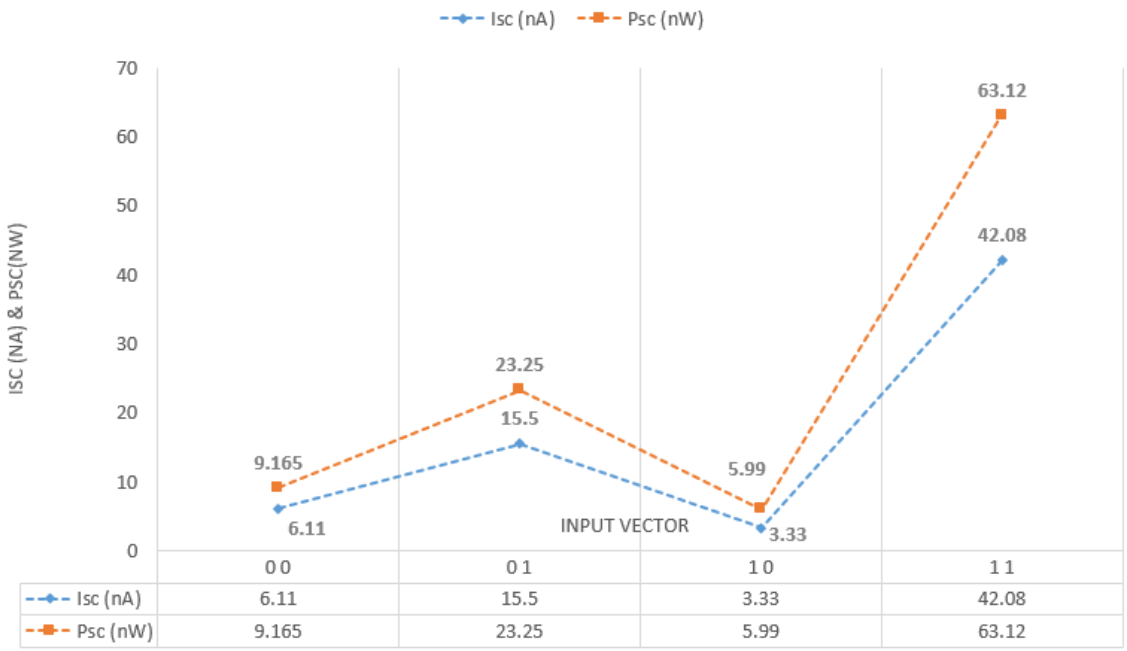


Figure 4.6: I static and P static for all combination of input for a two-input NAND gate.

Now the above process is repeated for a XOR gate which is formed by using 4 NAND gates as shown in the figure 4.6.

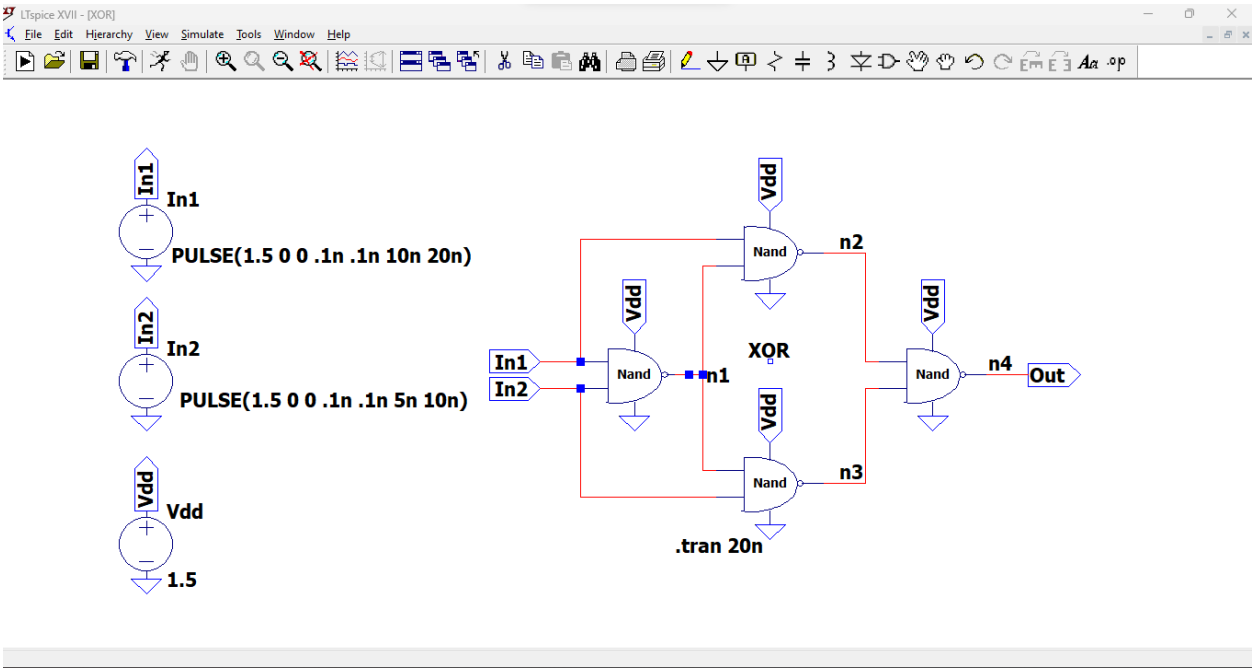


Figure 4.7: Ltspice simulation of XOR gate.

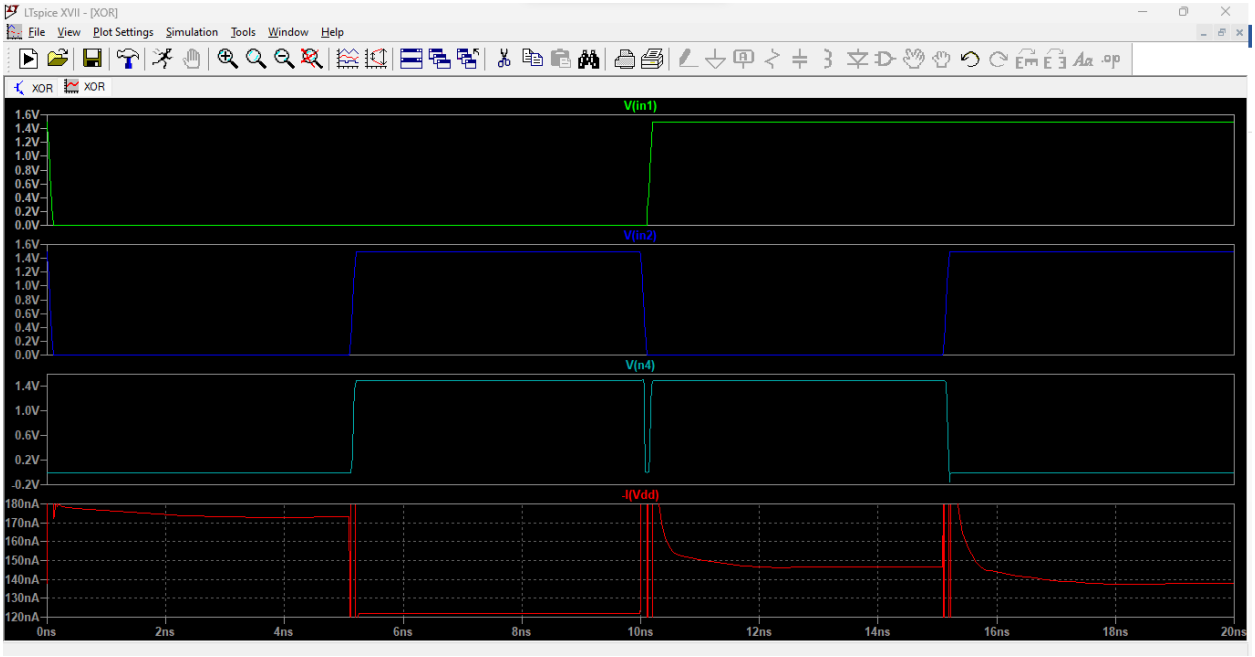


Figure 4.8: The output waveform for the simulation of a two-input XOR gate and static current for all input combination.

The above snapshot shows the functional working and leakage current waveform of a XOR

gate. The first waveform (light-green) represents the first input IN1 of the XOR gate, with values 0 -> 0 -> 1 -> 1. The second waveform (blue) represents the second input IN2 of the XOR gate, with values 0 -> 1 -> 0 -> 1, forming all four combinations of the two-input XOR gate. The third waveform (green) shows the output of the XOR gate, while the fourth waveform (red) shows the corresponding leakage current in nA for each input combination.

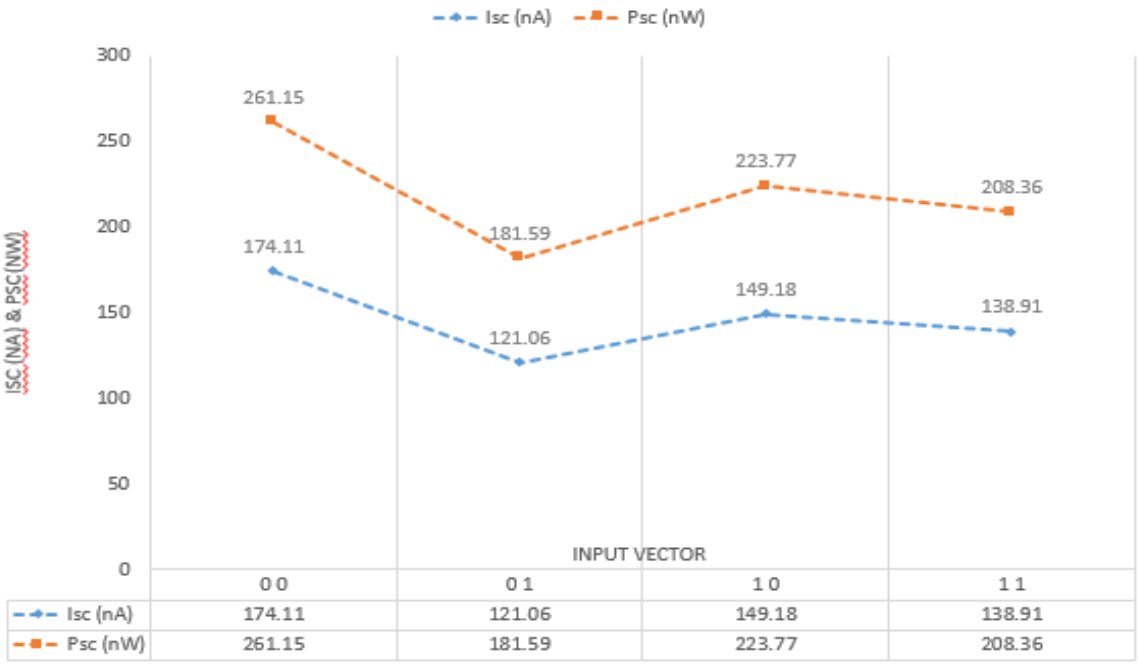


Figure 4.9: I static and P static for all combination of input for a two-input XOR gate.

Finally, the above process is repeated once again for a full adder, which utilizes 9 NAND gates with 3 inputs (IN1, IN2, and IN3) and 2 outputs (sum and carry).

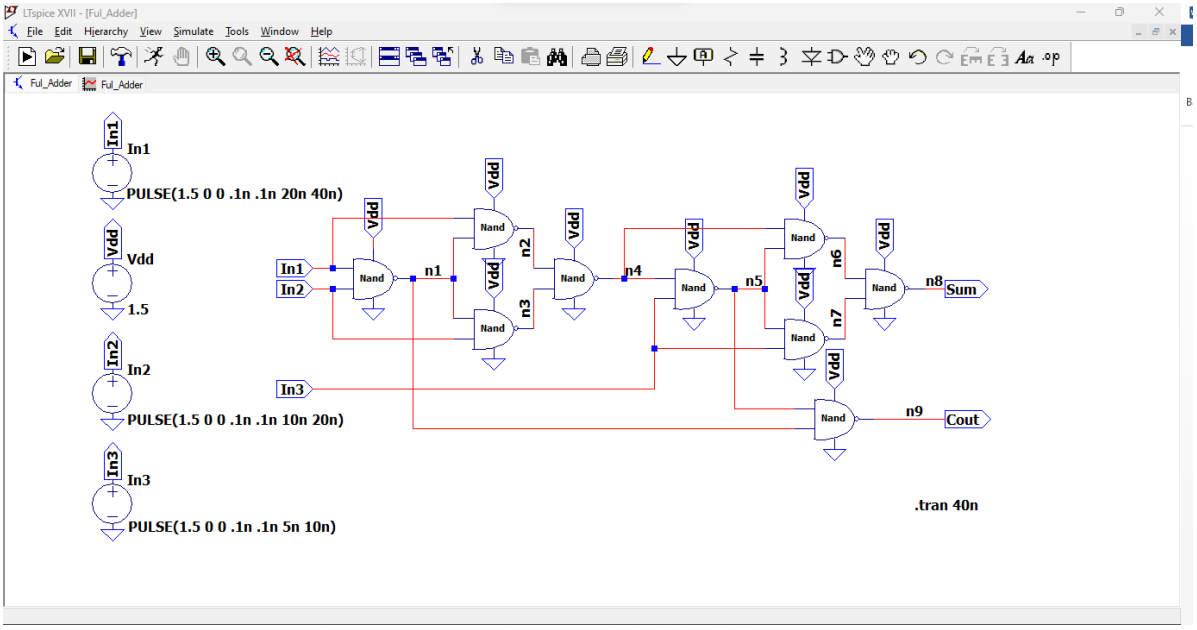


Figure 4.10: Ltspice simulation of Full Adder gate.

The snapshot below shows the functional working waveform of a full adder with 9 NAND gates. The first waveform (light-green) represents the first input IN1 of the adder gate, with values (0, 0, 0, 0, 1, 1, 1, and 1). The second waveform (red) represents the second input IN2, with values (0, 0, 1, 1, 0, 0, 1, and 1), forming all eight combinations of the full adder. The third waveform (green) represents the carry input (CIN) of the full adder with values (0, 0, 0, 1, 0, 1, 1, and 1). The fourth waveform (blue) shows the Sum output of the full adder, while the fifth waveform (pink) shows the Carry output of the full adder.

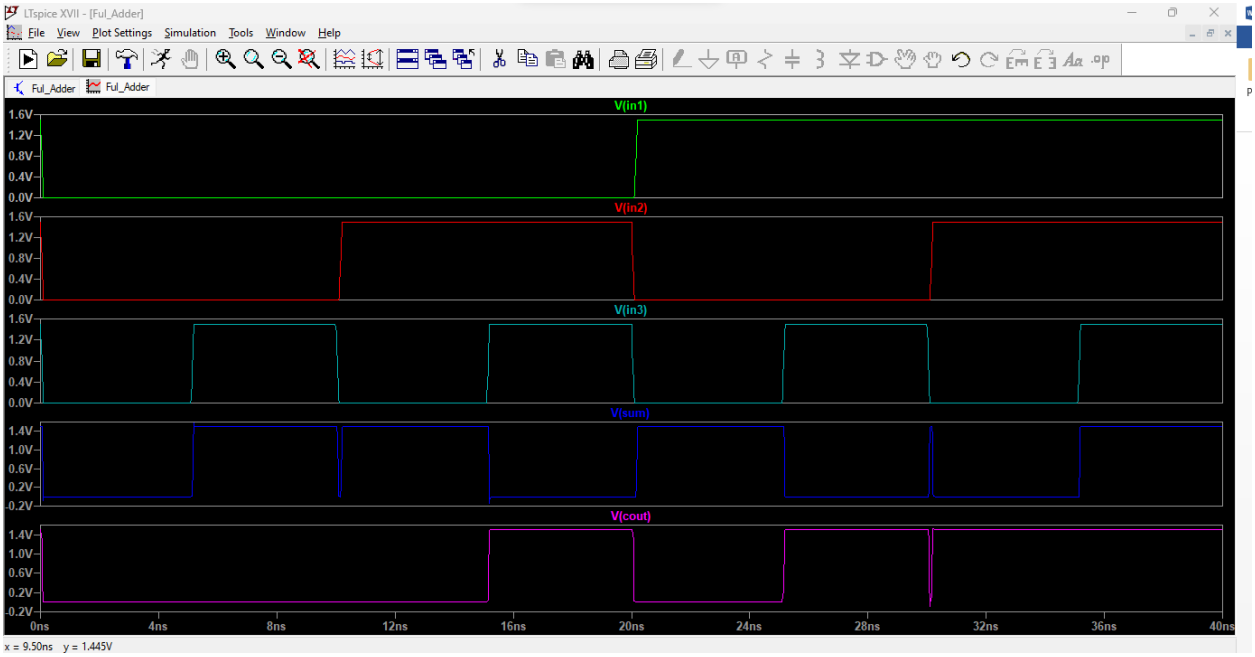


Figure 4.11: The output waveform for the simulation of a two-input Full Adder gate.

The snapshot below shows the Static current waveform of a full adder with 9 NAND gates for all possible combination of inputs. The first waveform (light-green) represents the first input IN1 of the adder gate, with values (0, 0, 0, 0, 1, 1, 1, and 1). The second waveform (red) represents the second input IN2, with values (0, 0, 1, 1, 0, 0, 1, and 1), forming all eight combinations of the full adder. The third waveform (green) represents the carry input (CIN) of the full adder with values (0, 0, 0, 1, 0, 1, 1, and 1). The fourth waveform (blue) shows static current in nano Ampere.

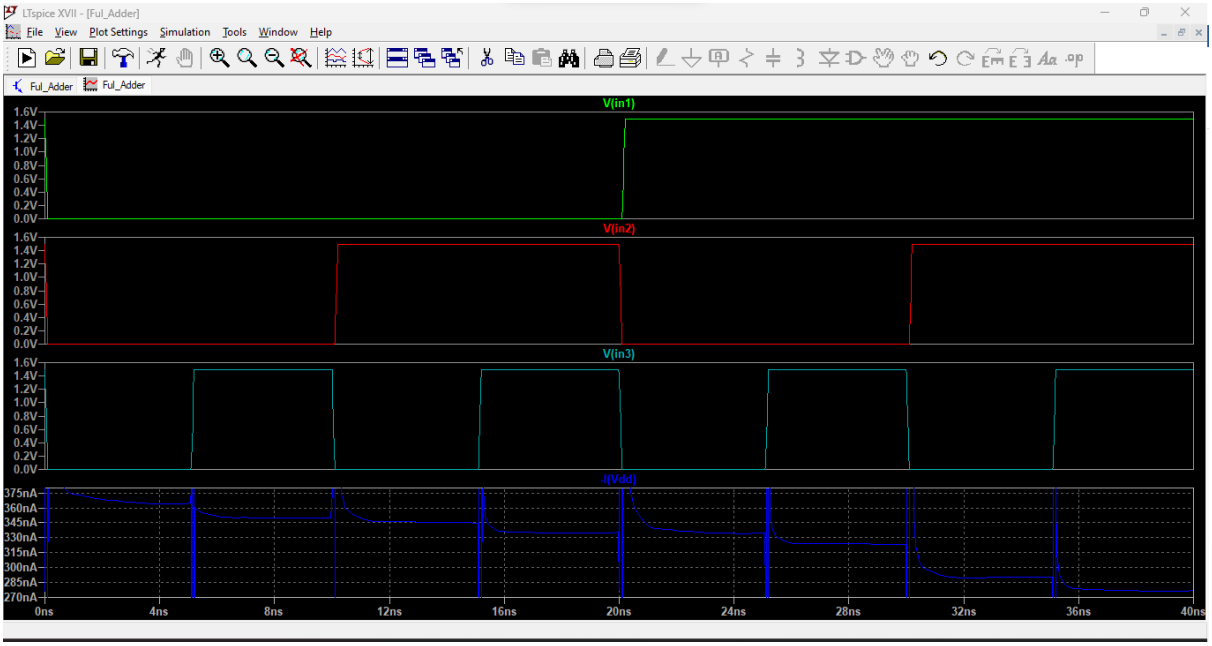


Figure 4.12: Static current corresponding to all input combination of Full Adder.

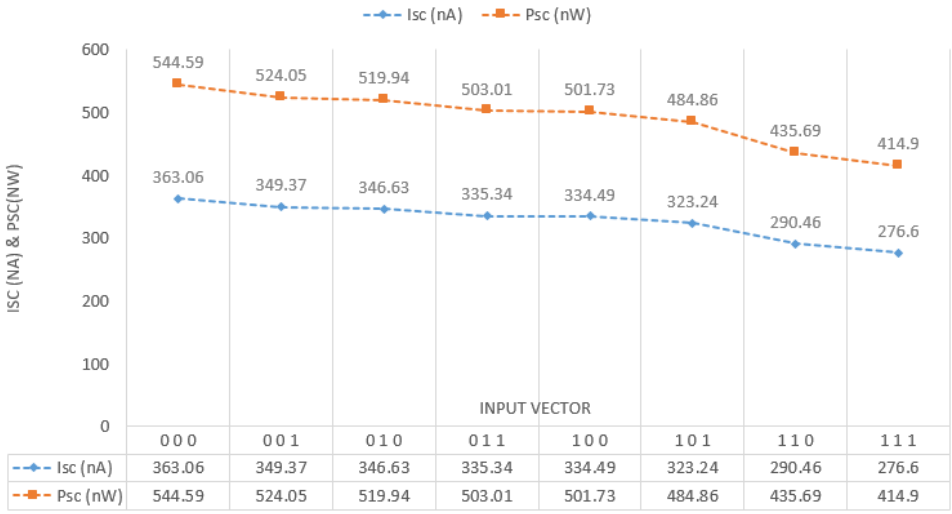


Figure 4.13: I static and P static for all combination of input for a two-input NAND gate.

## 4.3 ALGOITHM VERIFICATION.

In this section, the above derived result from the simulation of various circuits will be verified. The textual representation of the circuitry will be given as input to the algorithm, and as per the expectation, the text file will be traversed by the algorithm to give the output, which corresponds to the minimum leakage state of the input circuit.

Part A of the below figures represents the static power and static current for various combinations of input for the circuitry, while Part B shows the textual representation of the circuit input and the output of the algorithm.

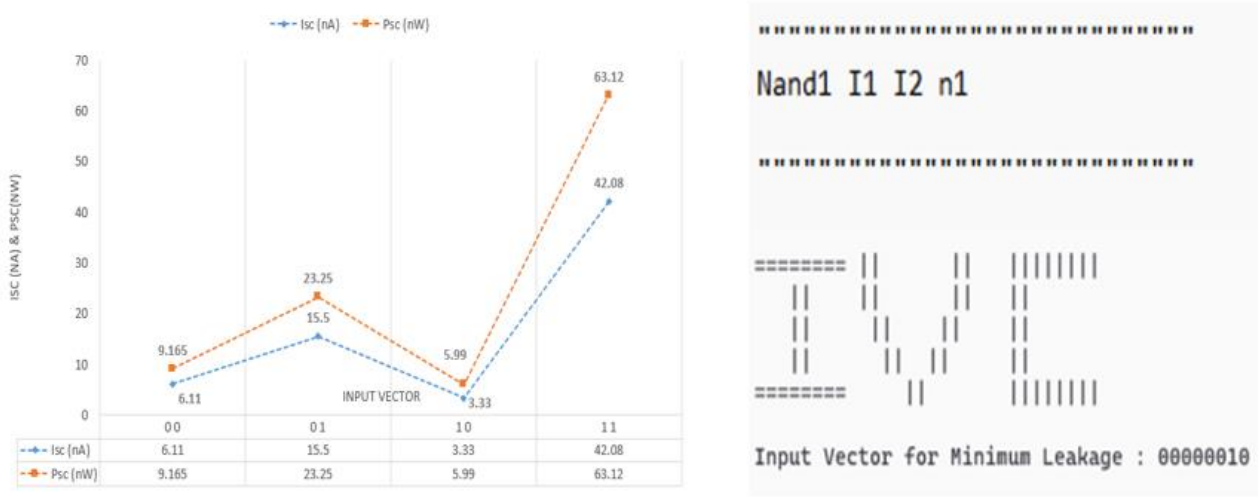


Figure 4.14: a) Static and dynamic power consumption for all combinations of inputs for a two-input NAND gate. b) Textual representation of the circuit input and the output of the algorithm.

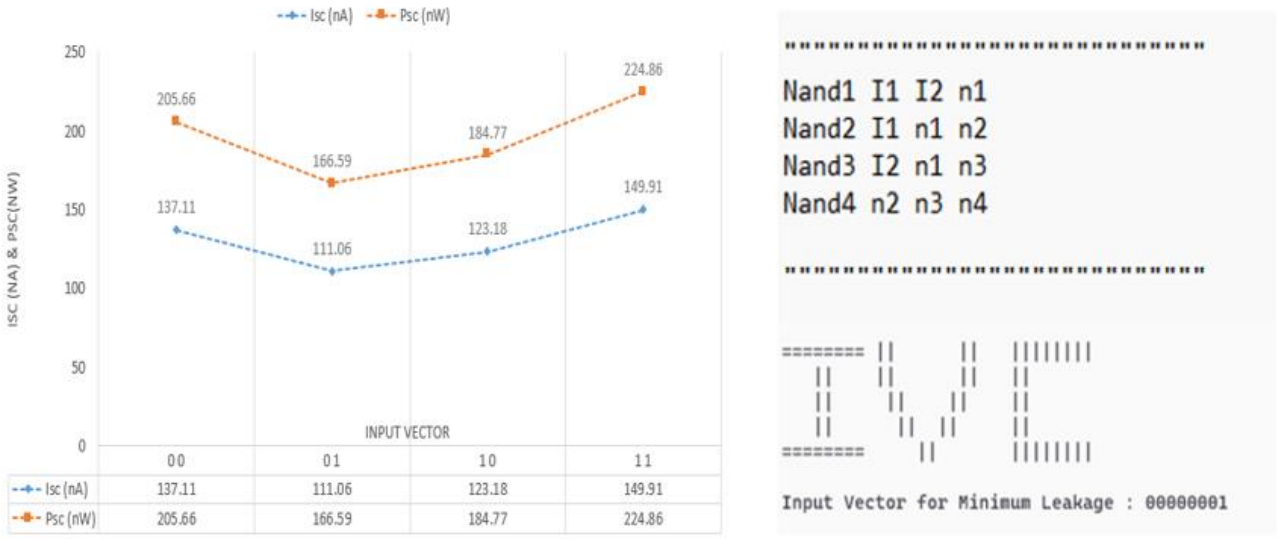


Figure 4.15: a) Static and dynamic power consumption for all combinations of inputs for a two-input XOR gate. b) Textual representation of the circuit as input and the output of the algorithm.

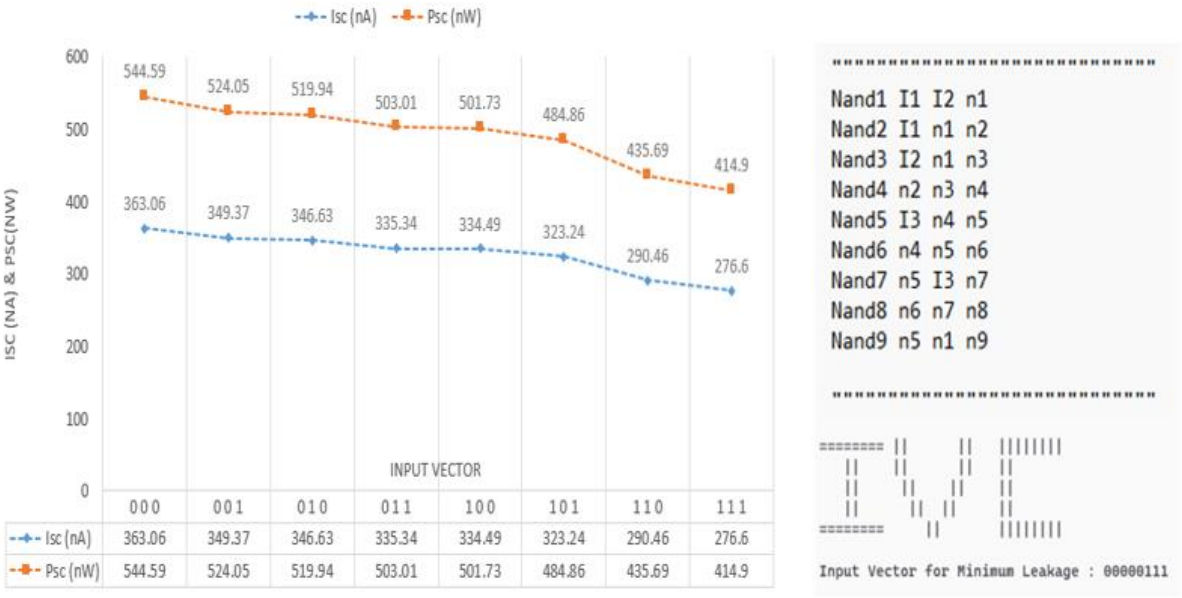


Figure 4.16: a) Static and dynamic power consumption for all combinations of inputs for a three-input Full Adder. b) Textual representation of the circuit input and the output of the algorithm.

In all three figures above, it can be seen that the algorithm is able to correctly find the IVC, which corresponds to the minimum leakage state. Therefore, the algorithm is working accurately as expected. Below table consolidates the amount and percentage of power saved from the default value i.e. all zero's.

Table No. 7 Percentage save in power by using IVC

| Circuit | Static Power with default input 00 | Static Power with IVC input | Per. Of power saved |
|---|---|---|---|
| NAND | 9.165 | 5.99 | 34.64% |
| XOR | 261.15 | 181.59 | 30.46% |
| Full Adder | 544.59 | 414.9 | 23.81% |

# Chapter 5: Future Scope

The leakage reduction approaches discussed in this thesis can be a very efficient technique for reducing CMOS leakage power consumption in CMOS circuits without much or no overhead. As technology nodes continue to shrink and power consumption becomes an increasingly important concern, the future scope of IVC and other leakage reduction technique is significant. In this section, we will discuss the future scope of the discussed leakage reduction techniques.

i. Techniques with hardware approach and software approach can be combined together for much better results.

ii. IVC can be used in sequential circuits to reduce the leakage in basic building block that is flip flop. The above algorithm can be restructure with flip flop as a basic building block, and can be scaled to any sequential circuit. Thus combining both the algorithm can be used to cover entire digital circuitry.

iii. The above algorithm can be scale to IP level and can be used at industry level to reduce the static power consumption of SOC. And hence can be used at processor level and can be implemented on server data centers reducing the power consumption, will help in reducing the overall cost for cooling.

iv. Another promising future application of IVC is in the field of electric vehicles (EVs). As the demand for electric vehicles continues to grow, the need for efficient power conversion and control becomes increasingly important. IVC can be very effective in reducing the leakage power consumption in the power electronics systems used in electric vehicles, improving their range and reducing their environmental impact.

v. IVC also has potential applications in the field of data centers. Data centers consume significant amounts of energy, and reducing their power consumption is a major concern. IVC can be effective in reducing the leakage power consumption in the power electronics systems used in data centers, improving their efficiency and reducing their environmental impact.

vi. IVC also has the potential to be used in emerging technologies such as the Internet of Things (IoT) and edge computing. As these technologies continue to grow, the need for efficient power conversion and control becomes increasingly important. IVC can be effective in reducing the leakage power consumption in the IoT system as these system are small and battery operated thus, improving their efficiency with respect to charging frequency and time.

vii. Finally, the future scope of IVC also includes the development of new algorithms and techniques for leakage reduction. While IVC has shown promise in reducing leakage power consumption, there is still room for improvement. Research in this area is ongoing, and new algorithms and techniques for IVC are expected to emerge in the future.

viii. Future research could explore the impact of IVC on different types of digital circuits, as well as investigate the potential for combining IVC with other low-power design techniques to achieve even greater power savings.

Thus the future scope of IVC and other hardware techniques for leakage reduction is significant. IVC has the potential to improve the efficiency and reduce the environmental impact of a wide range of digital systems, including renewable energy systems, electric vehicles, and data centers. Additionally, the development of new algorithms and techniques for IVC is expected to further improve its effectiveness in reducing leakage power consumption. As technology continues to advance, IVC is expected to become an increasingly important technique for reducing CMOS leakage power consumption in power electronic systems.

# Chapter 6: Conclusion

In today's world, the attention towards using small portable devices with long battery life is increasing rapidly. Scaling down these devices comes with a tradeoff in leakage power dissipation which causes instability and affects the device's performance. Implementation and technology are the two significant aspects on which these tradeoff factors majorly depend. Conventionally, we use complementary MOS (CMOS) devices to synthesize and implement logic networks. But due to scaling, these suffer from the above mentioned complications such as leakage power.

In this thesis, presents a detailed discussion of various low-power leakage reduction techniques is presented, by dividing all conventional techniques into two broad categories of hardware and software approaches. The first half is dedicated to the hardware approach, which covers all the traditional techniques to reduce the leakage power using extra hardware (transistors). In the second half, we investigate a software approach to decrease the leakage power consumption, i.e. IVC.

In the first half we have implemented five 4x4 array multipliers in the hardware approach with different leakage reduction techniques. As we saw, all of the above multipliers have their own tradeoffs. We get a low power multiplier with the stacking technique, but the delay overhead is almost double, so it is not fit for high-speed operations, and the same is applicable to LECTOR and MTCMOS. Whereas multiplier with ONOFIC technique gives us the best result compared to CMOS decrease in leakage power is almost per cent with very less delay overhead. Thus the multiplier with the ONOFIC technique can be used for low-power applications, but the number of transistors used is almost doubled. So in places where area is not a limiting factor, ONOFIC multiplier can be used effectively to reduce power consumption.

Hardware techniques reviewed in this paper have their own advantages and disadvantages, which entirely depends upon the primary requirement of the designer: ease of design, robustness, are, and speed or power dissipation. No single technique optimizes all these measures at the same time.

In the second half, Input Vector Control (IVC) is discussed which is a promising technique for reducing CMOS leakage power consumption in power electronic systems. This thesis has presented an overview of the IVC technique and its applications in various digital systems. The thesis has also discussed the advantages of IVC over other CMOS leakage reduction techniques and its future scope for leakage reduction. The thesis has highlighted that IVC uses a combination of a pre-determined input vector and a control algorithm to reduce the power consumption of a system. IVC can achieve high-performance control by carefully selecting the input vector and control algorithm while minimizing power consumption. In conclusion, this thesis has investigated the algorithm's efficiency in finding Input Vectors for reducing the static power consumption of CMOS circuits. The results of the experiments demonstrate that IVC can significantly reduce the static power consumption of digital circuits without compromising circuit performance.

Overall, the findings of this thesis demonstrate that IVC is a promising low-power design technique that can be used to reduce static power consumption in CMOS circuits. IVC can be used on top of all the techniques mentioned in the first part to achieve even better results. A major limitation of the proposed algorithm is that it should be able to read the netlist provided by industry standardized tool for design. The above-proposed algorithm can also be modified to incorporate gate-leakage for finding a low leakage state that considers both forms of leakage. The future scope of IVC for leakage reduction is significant, and research in this area is ongoing, with the potential to further improve the effectiveness of IVC by combining it with other leakage reduction techniques. As technology advances, IVC, combined with other techniques, is expected to become an increasingly important technique for reducing CMOS leakage power consumption. With the growing demand for low-power devices, the continued development, refinement and uniting of these techniques will be critical to meeting the power consumption requirements of modern circuits.

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