Power, Performance and Area Metrics in VLSI Design: An Analytical Approach

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IN
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Submitted by

Juned Altaf Mulani
(2K21/VLS/10)

Under supervision of

Dr. Harikesh (ECE)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bhawana Road, Rohini, Delhi- 110042

CANDIDATE'S DECLARATION

I, Juned Altaf Mulani (2K21/VLS/10), student of MTech (VLSI Design and EMBEDDED SYSTEM), hereby declare that the MAJOR Project report "**Power ,Performance and Area Metrics of VLSI Design : An Analytical Approach"** which is submitted by me to the department of Electronics and Communication Engineering, DELHI TECHNOLOGICAL UNIVERSITY, DELHI in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, fellowship or other similar title or recognition.

Juned Altaf Mulani (2k21/VLS/10)
MTech (VLSI Design and EMBEDDED SYSTEM)
Department of Electronics & Communication Engineering

Date: __-05-2023
Place: Delhi

CERTIFICATE

I hereby certify that the **MAJOR** Project report titled "**Power,Performance and Area Metrics of VLSI Design : An Analytical Approach"** which is submitted by Juned Altaf Mulani Roll No. 2K21/VLS/10 to the department of Electronics and Communication Engineering, Delhi Technological University, Delhi in the partial fulfilment of the requirement for the award of the degree of Master of Technology, is record work of the report work carried out by student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Dr. Harikesh
(Project Supervisor)
Department of Electronics & Communication Engineering

Date: __ -05-2023
Place: Delhi

ABSTRACT

Power consumption, performance, and area utilization are critical considerations in VLSI design. This paper presents an analytical approach to optimize these metrics using a proposed clock gating technique. The objective is to achieve power-efficient and high-performance VLSI designs while minimizing the area overhead. The proposed clock gating technique utilizes a sophisticated control logic that selectively enables clock signals to the circuit components based on their activity. By dynamically controlling the clock distribution, unnecessary switching and power dissipation are reduced, resulting in significant power savings. The technique is analyzed and compared with conventional clock gating approaches in terms of power reduction and performance enhancement.

Experimental results demonstrate the effectiveness of the proposed clock gating technique in reducing power consumption while maintaining the desired performance levels. The analysis reveals that the proposed technique outperforms conventional methods in terms of power savings, with minimal impact on performance. However, it is noted that the proposed clock gating technique may introduce a slight increase in area overhead due to the additional control logic.

Keywords- Power, Timing, Area, Optimization, Performance enhancement, Circuit Architecture, Conventional Clock Gating.

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Juned Altaf Mulani (2k21/VLS/10)
MTech (VLSI Design and EMBEDDED SYSTEM)
Department of Electronics & Communication Engineering

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CHAPTER 1: INTRODUCTION

1.1 Introduction

This paper focuses on important digital design concepts such as power, performance and area with considering the low power technique clock gating and proposing new advanced modified clock gating technique and its analysis on design. The power is important aspect of electronic component and as nowadays more electronic devices are reducing its size considering portability it's very essential to consider the power aspect of design .In designing electronic component optimizing power, area & performance is critical task .The power being an most important aspect using it wisely and minimising its utilization is very important .The increased power consumption has several adverse effects like heating the design becomes less reliable and the efficiency also is affected .Thus power has emerged as the most important aspect ranging from electronic design equipment , portable gadgets to data centres. There are several techniques to reduce power consumption of design like signal gating ,clock gating ,pin ,using adiabatic logic pin reordering , etc. in this paper the clock gating technique is utilised and advanced clock gating is proposed .Clock gating is technique in which logic gates are added to clock paths which acts as enabling signal or control signal to turn on circuitry depending on desired operations .By utilising clock gating the logical blocks which consumes more power can be turned off when required without affecting the working of design which in turns reflects in dynamic power consumption of design ,thus clock gating is widely used technique for dealing with dynamic power utilisation of circuit. The clock gating technique also have advantage of reducing size or area utilization of design as the technique remove unnecessary logic and the design uses less elements at given instance .This paper discuss the advancement in conventional clock gating technique for more efficient implementation on digital filter and does comparative analysis with conventional technique as an application of method the technique is implemented on digital filter of type second-order Infinite Impulse Response (IIR) filter and the paper discusses the effect of clock gating and proposed clock gating in analytic approach for optimising power, performance and area and considering the best optimal value considering the trade-off .This paper demonstrates the principles of power utilization with low power technique known as clock gating the benefits associated and implementation strategies.

Thus this paper helps in designers to achieve a perfect balance between power, performance and area of design by adopting the implementation methodologies explained which is been obtained from thorough examination of case studies, literature surveys and practical examples. Dynamic power dissipation, also known as switching power, refers to the power consumed by a digital circuit due to the charging and discharging of capacitive loads during switching transitions. It is one of the major contributors to total power consumption in digital systems. Dynamic power dissipation can be explained in terms of the components that contribute to it.

1.2 Dynamic Power

The most dominant type of power to contribute for total power is dynamic power which is also referred as switching power which is result of charging and discharging of capacitive elements in design which are as a result of switching transistors. The Capacitance during charging and discharging these happens during transitions of stages i.e. switching of states energy is consumed also digital circuits comprises of lots of capacitive loads across input pins, output pins, gates of transistors and interconnects. Also the switching activity of digital circuit impacts the dynamic power dissipation switching activity refers to frequency of transition of states in digital circuit also amplitude of vibrations in designed digital implemented circuits. The switching activities have higher values when the transitions from 0 to 1 or 1 to 0 are more or more frequent transitions. Also if numbers of elements in design are higher the higher is switching factor. The supply voltage to a design is also an important parameter on which the dynamic power is dependent the dynamic power is related to supply voltage as square of voltage value so is very important to be considered. Thus the voltage supplied can significantly affect the dynamic power dissipation. The dynamic power dissipation is calculated by below equation:

$$Pdyn = Cload * Vsupply^2 * frequency * activity\_factor \quad (1)$$

Where: $Pdyn$ = dynamic power

- Cload capacitive load.
- Vsupply is the supply voltage.
- f is operating frequency.
-activity factor is switching factor for design

Thus from equation we can state that out of four factors (capacitance, voltage, frequency, switching factor) optimising it can reduce dynamic power significantly.

1.3 Conventional Techniques to reduce dynamic power.

The following are well known techniques for reducing the dynamic power dissipation.

1. Clock gating: In this technique the clock to circuit is disabled in case when circuit is in idle case this causes unnecessary switching of elements and saved power in design.

2. Voltage Scaling: The methodologies like Adaptive voltage scaling and dynamic voltage scale can be introduced in design to scale voltage by adjusting the voltage based on desired dependencies on the design and workload of performance analysis. As lowering the voltage leads to reduction in dynamic power consumption as we know power is related to voltage as squared value of voltage.

3. Activity depending Power utilization: This technique involves optimizing the power depending on dynamically adapting and adjusting voltage and frequency depending on circuit performance and utilization of circuit elements.

4. Pipelining and Parallelism: This technique involves use of parallel architecture which results in redistribution of work across the design stages causing in reduction of power because of reduction in switching activity.

5. Low-power circuit design: This technique involves the low power circuit using transistor which uses transistors having low leakage, deceasing size of transistors, making the size of load capacitances small can significantly reduce power consumption.

The important aspect while considering the reduction of dynamic power dissipation to maintain the correct balance between power, performance and area of design and cost and designing the best optimal design accordingly.

CHAPTER 2: OVERVIEW OF EXISTTING CLOCK GATING TECHNIQUE.

The clock gating technique is incorporated to limit the dynamic power utilization some logical blocks are power hungry circuits clock gating is used to deactivate those circuits when they have no involvement in performing the relevant task at those instance by considering the design implementation and logical output the gating of clock is done based on some conditions and enabling and disabling of clocks occurs accordingly which results in improved performance. The basic idea of its working is when the clock gating signal is high or active high (enabled) the clock is allowed to propagate via circuit elements to desired logical block .When clock signal is active low (disabled) the clock is not allowed to propagate as the gate which is incorporated with clock does not allow the passing of clock signal to logical blocks. This is achieved by adding new logic gates in between the path traced by clock signal .This gates can be clock gating cells or elements which acts as control signal to provide the gating of clock by enabling or disabling.

2.1 Clock gating involves following key aspects.

1. Clock gating cells: It can consists of logical gates like of AND, logical flip-flops ,multiplexers. These are needed to add separately in design in clock paths which can be controlled by enable signal.

2.Clock Enable Signal: This is basically determining or decision making of clock gating cells that should they be activate or deactivate the clock signal they are typically obtained from status or flag signals such as activity detectors or enable signal from higher logical module.

3. Control Logic: The control logic is one which provides the enable signal to activate or deactivate depending on the analysis of designs.

2.2 Clock gating provides following benefits:

1. Power Reduction: The clock gating enable and disable the power hungry circuits depending on their idle behaviour or inactive periods by activating clock when required thus reducing dynamic power consumption.

2. Timing Improvement: Clock gating can improve overall system performance by reducing unnecessary clock cycles and improving critical path timing. This can lead to faster operation and better timing closure.

3. Area Optimization: Clock gating results in removal of redundant logic and the active elements in design are restricted. This results in power utilization, improved area efficiency..

4. Design Flexibility: Clock gating provides good flexibility for designers considering the power aspect and area aspect which can be reduced according to design considering trade-off and other strategies.

While designing clock gating the important factor needed to be considered is Design Verification, as the clock gating addition adds complexity to the initial design and thorough validation and verification is required as so to maintain correct functionality of circuits.

2.3 Architecture of digital filter with clock gating.

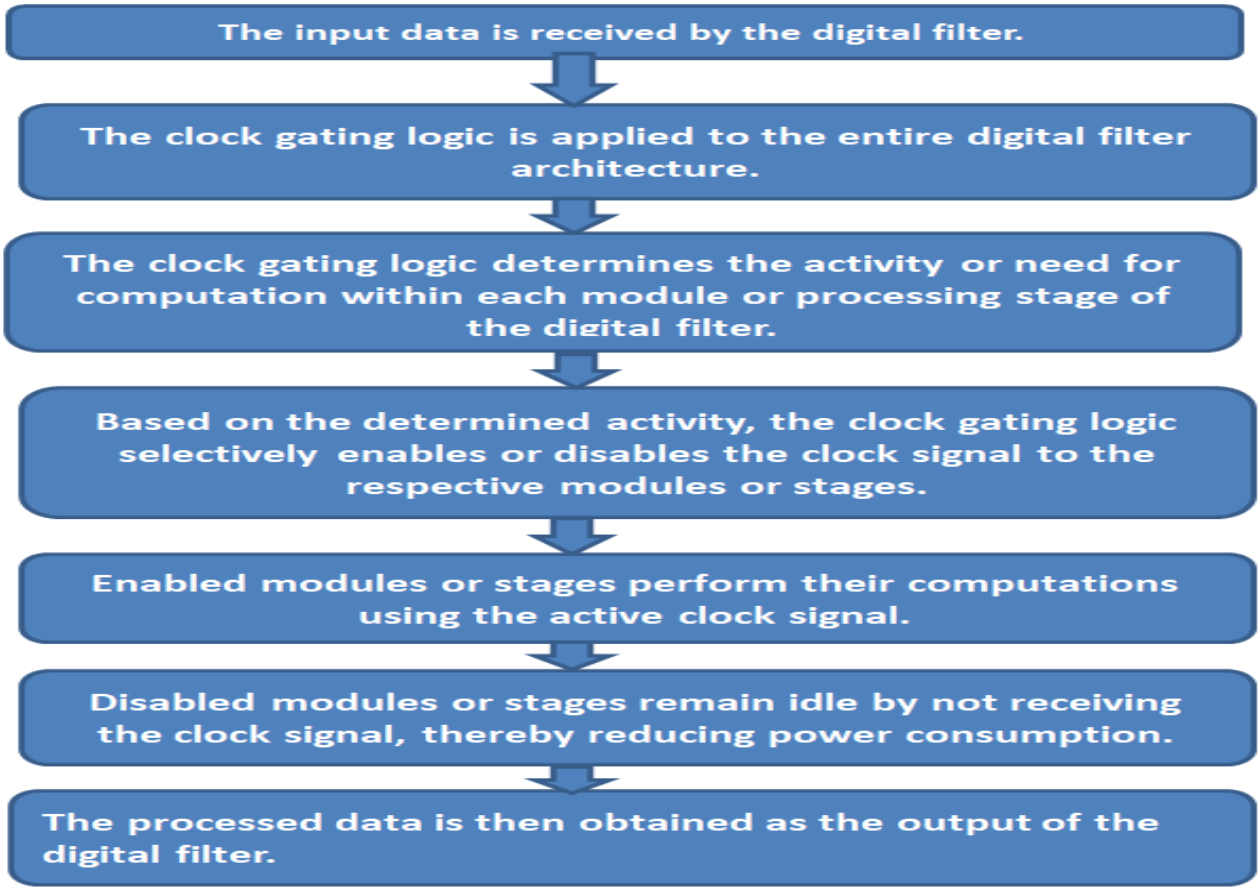

Figure 2.1 Architecture of Digital filter with clock gating.

As seen from above is flow chart to understand the working of conventional clock gating as an application on digital filter i.e second-order Infinite Impulse Response (IIR) filter the first step

takes the input and passed to digital filter and in second step the clock gating logic is applied to entire digital filter in third step the computation is done within each module to find the activity of each block or processing stage of filter in next step depending upon the activity of modules the enabling or disabling of block takes place those blocks which are enabled took active participation in computing the filtering process and receive clocking signal the disabled modules which are kept idle at the instance of execution and does not receive clock and thus reduce power consumption and thus the processed data is obtained at output of digital filter.[3]

2.4 Architecture of implemented clock gating on design.

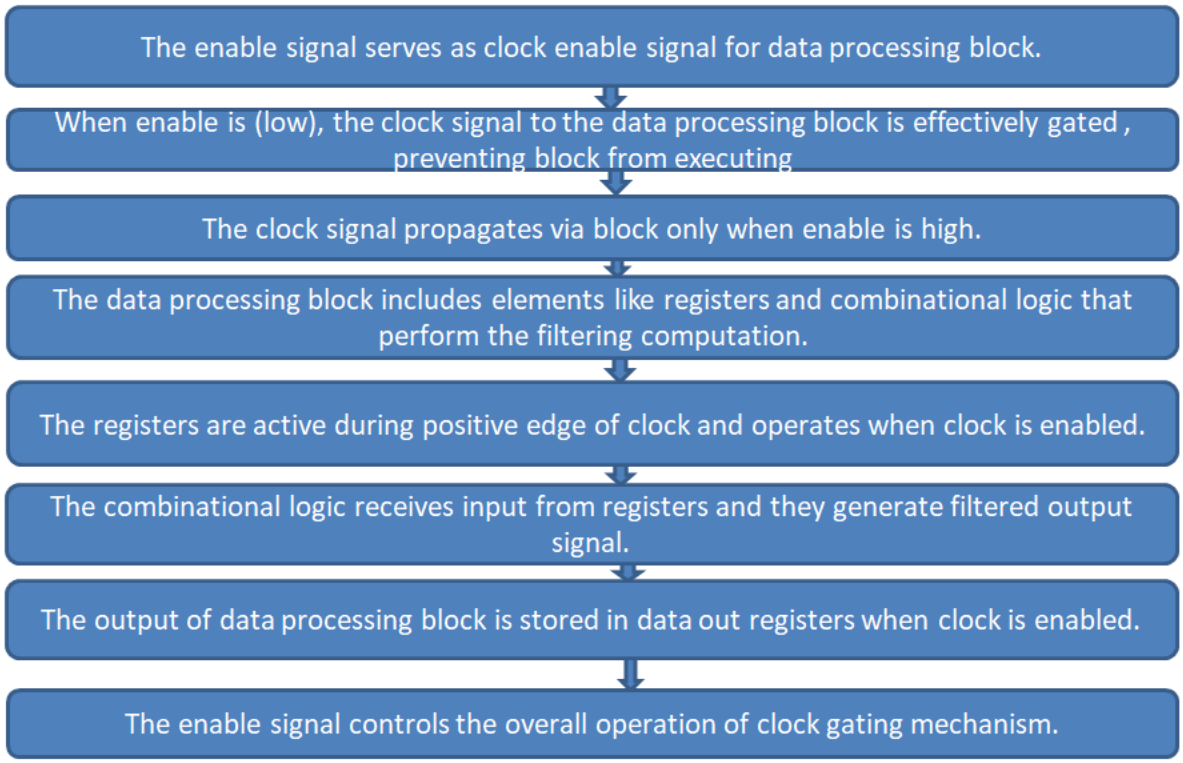

Figure 2.2 Architecture of Digital filter with implemented clock gating.

Above is flowchart for clock gating technique implemented on digital filter in more detail and stepwise manner the clock gating technique execution starts with enable signal which acts as enable signal for data processing block when enable is low the data processing block is made inactive that means it is prevented from participating in execution of filtering the clock signal propagates via different blocks upon application of clock the data processing block comprises of sequential elements like registers and combinational logic that performs filtering computation.

The registers in block are active during positive edge of clock and operate when clock is enabled .The combinational logic receives signals from registers and they generate filtered output. This output is stored in data out when clock is enabled.

CHAPTER 3: PROPOSED CLOCK GATING TECHNIQUE.

Optimized clock gating is a technique used in digital designs to reduce power consumption by selectively enabling or disabling the clock signal to specific circuit elements based on their operational requirements. This technique ensures that clock signals are active only when necessary, minimizing unnecessary switching activities and saving power. In proposed clock gating in advanced version of conventional clock gating which is used in digital circuit designs with functionality of enabling or disabling the clock depending on design analysis but in more efficient and productive way. The conventional clock gating is useful but had problems like were the entire clock tree and clock distribution network continues to operate even when clock was gated this caused the problems like static power dissipation which is result of clock tree capacitance and leakage power .As the conventional clocking involves the gating of clock with a simple logic gate like AND ,NOR etc. which is used to gate the clock to module it saves the power by eliminating clock of particular module or block but had limitations like leakage power ,improper gating on clock distribution network and clock tree. The proposed clock gating technique stops clock signals at clock tree and clock distribution network too thus saving more power and problem of leakage power is also removed. This can be achieved with improved methodology of gating clock domains like fine clock gating that means disabling clocks to individual circuit elements or registers within domain which gives advantages like more control over design and reducing any possible chances of toggling and consumption of power .The other important addition is using clock gating at multi levels the application of this clocks on clock tree which provide more control and results in power savings .The use of clock domain power gating also can be used in addition to gating blocks which results in shutting down power to entire logic and memory elements which saves more power also dynamic clock gating can also be used this is method in which the clock gating is made in real time working of designs and thus depending on activity of power blocks the circuit behaviour the power can be optimised even further.

3.1 The Key point in designing of proposed clock gating:

3.1.1. Clock Enable Signal Generation:

The signals of clock types are generated depending on special conditions or the signal which acts as control those which are relevant to design. These control signals work depending upon signal

coming from computed inputs the different circuit's states of design or signals from top modules. Thus depending on this signals the clock enable signals are generated and applied to control logic. For instance in digital circuits involving of digital processing the enable signal for clock is given depending on whether the data is valid which is available or the processing is involved. If there is absence of data then enable is turned off and clock can be gated to save power.

3.1.2. Clock Enable Distribution:

The circuit element to be targeted in design associated with clock gating cells which are distributed in design are of clock signal are enabled.

The gating cells of clock type which are appropriate for design are clock enabled which are routed using clock distribution network via direct connection for desired result. Thus each state which is computed for desired results which controls the propagation of clock is enabled with clock gating cells.

3.1.3. Clock Gating Cell:

Depending on state of enable signal the clock is passed to cell and is gated depending on specific desirable condition thus clock is gated which is achieved by clock gating cell. This configuration basically consists of targeted circuit of which receives the signal which is clock from output of clock enable. And thus when clock enable is high clock gating cells allows the clock signal to flow to desired destined logical block. And vice versa when clock enable is low the clock gating cell stops the propagation of clock signal to that particular block of logic.

3.1.4. Power Saving Benefits:

This proposed method saves more power by avoiding toggling of circuit elements and unnecessary switching which are not contributing to the desired which is achieved by selectively clock gating those design circuit elements. Thus by selectively enabling signals when required power utilization is achieved. The proposed method will be more effective in design in which there are circuit elements which are operating irregularly and are periodically in active states..

3.1.5. Performance Impact:

The trade-off between power and performance affects the systems as the proposed clock gating system has advantage of saving the power but affects the timing part of design due to inclusion logic and gating logic ,the overhead delay can be introduced in design in clock path which can cause impact to overall design of system also in timing paths specifically critical paths these are all included because of control logic and clock gating cells thus designer need to focus in these things and analyse accordingly how much power is to be saved against the performance

parameter while using the above proposed methodology and main point to consider is the introduced delay doesn't affect the overall timing requirements. Hence the proposed optimised clock gating technique is good at optimising power that gates the logical modules and circuits depending on enable signal selectively but the operational functionality is to be preserved it reduced redundant logic and improves power but designer need also take into consideration trade -off between power ,performance and area of design .

3.2 Architecture of digital filter with proposed clock gating:

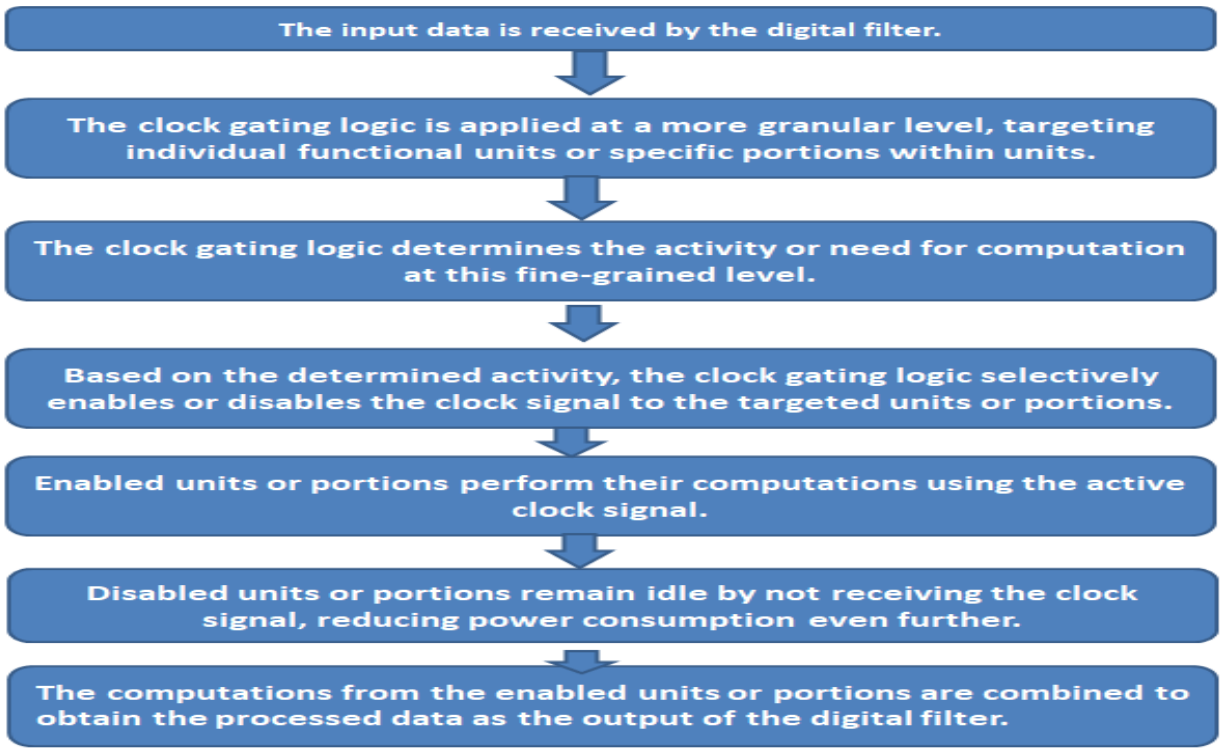

Figure 3.1 Architecture of Digital filter with proposed clock gating.

The above is flow chart of architecture of integration of proposed clock gating in digital filter i.e. type second-order Infinite Impulse Response (IIR) filter the working starts from the input data which is received from digital filter then the clock gating is applied in more specified way to organized logic which targets every functional logic and some dedicated functional units. Then proposed methodology looks for the operational activity of logical blocks or circuits and does

computation accordingly at each and every individual block on granular level. Thus depending on this computation and activity of circuit elements the clock gating is applied and enable or disable functionality of circuital elements is decided .The enabled signals means the logical block receives the clock signal and the circuit elements take participation in producing filtered results. Likewise when the logical block or circuit elements receives disabled signal then the clock signal is gated to those elements and those elements are exempted from participating in the evaluation of filtering. And lastly commutated results obtained from enable signal is executed and combined together and processed as output of digital filter.

3.3 Architecture of proposed methodology of clock gating on design.

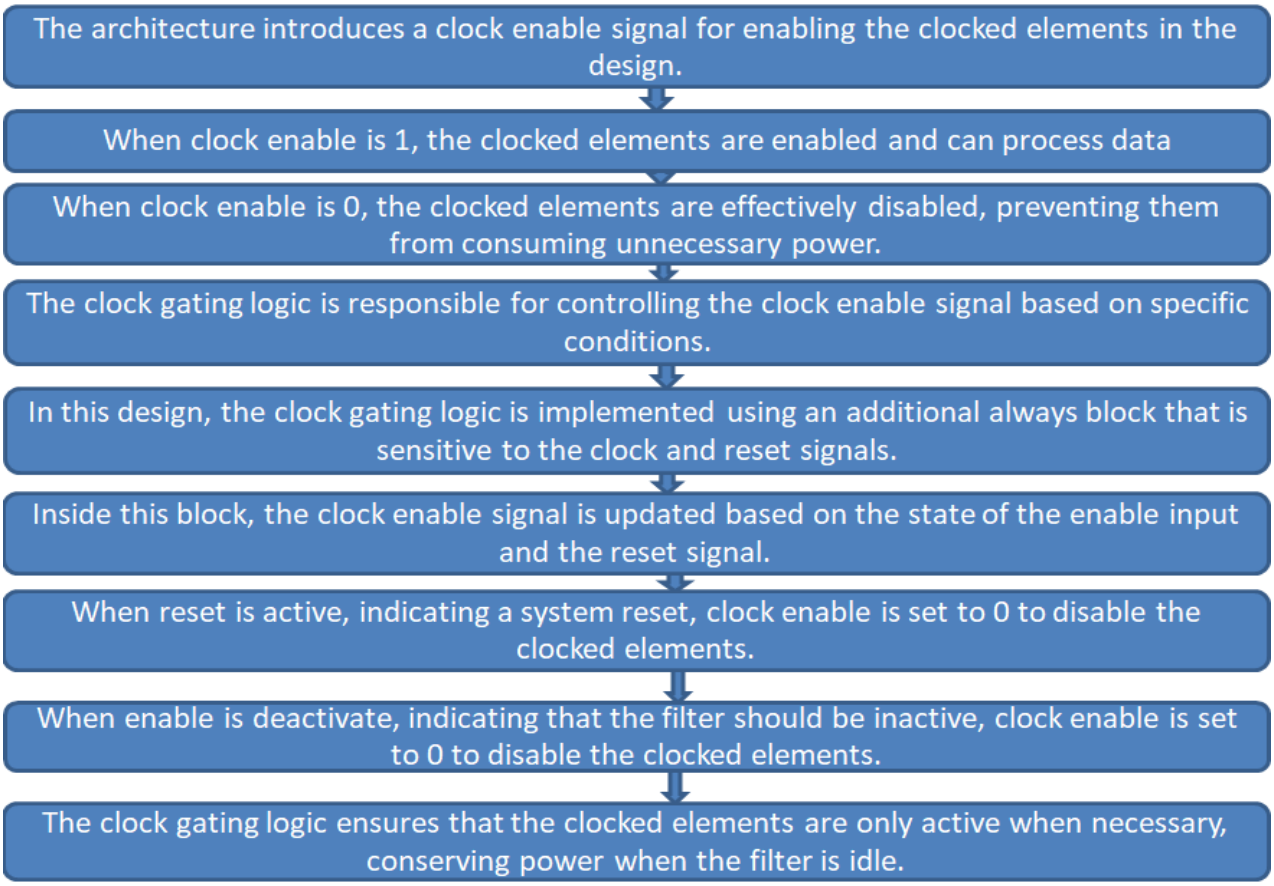

Figure 3.2 Architecture of Digital filter with proposed implemented clock gating.

Above is the flow chart of architecture of implemented proposed clock gating technique on digital filter the architecture starts with clock enable signal which acts as triggering input to

clocked circuit elements in design when clock enable is having value as 1 the clocked elements in design are activated and process the desired data and contribute in processing output data , when clock enable is 0 the circuit elements are made deactivated and the clock signal is not applied to logical block causing the logical block disconnect from clock signal and hence they don’t contribute in operation of desired logical implementation the clock enable signal is controlled by clock gating logic implemented based on specific conditions . In implementation of proposed design the clock gating logic is implemented using additional block of always type which responds to signals of kind reset and active this block serves as dedicated block for working of enable clock signal depending on the input of enable and reset type. When reset signal is made active in the always block the clock enable is made 0 and the clock is removed from circuit elements [4]. The filter is made inactive or disabled depending on clock enable status if status is deactivate the clock enable reads the same and disable the circuit elements respectively. Thus the proposed technique makes sure that filter is made active depending on situational changes and only when necessary by preserving overall balance and functionality [5].

CHAPTER 4: LITERATURE REVIEW

4.1 Introduction:

In field of biomedical, wireless media communication, audio processing and many more digital filters play an important role and have wide range of application use .Of digital filter type Infinite Impulse Response type of filters which have high sharp cut-off frequency and which provide perfect filtering has a vital role in area of Digital signal processing. The implementation of power efficient digital filters is very important task the overall power of designed system can be optimised of communication designed systems which can give benefits like extended battery life with high efficiency and eventually optimised energy consumption. The power is very crucial aspect to look in devices like mobile phones battery operated systems like IOT based modules. The digital filters have perfect tolerance to distortions and have minimum impact to interference and have great response for extraction of desired signal. The systems like wireless systems have huge dependencies on filters for task which involves the complicated applications like noise improvement, equalization of channel, avoiding interference between channels. The power utilized by devices in applications of design of communication systems which uses digital filter should be optimized for better performance and efficiency of system. The usage of filters in portable applications like headphones, speakers and audio signal processors the usage of these and effective implementation of the IIR filter is very crucial task as noise cancellation ,the better sound effects and better design is to be produced.

In medical applications of digital filter the implementation of design should be such that utilizes power wisely as power efficient model serves for longer duration in medical applications which requires continuous monitoring of data without finding a need for battery replacement in frequent manner. As the medical applications of filter needs to be precisely accurate as these filters are incorporated in task which needs high extraction of data from noisy signals of medical applications which provides doctors with perfect data for accurate treatment of patients. The applications of filter in biomedical applications like monitoring the blood pressure of individual monitoring the data from filtering of electrocardiogram. The parameters like power, area and performance of design constitutes for overall design of system the area of design should be efficient which enables the cost efficiency and make the idea of small portable devices a success

which makes it possible for designers to implement desired functionality using filters in complex systems in single chip. As the area constituted by design on silicon chip is physically the dimensions of systems which constitute the exact space occupancy of design which uses filter as design element .As the a designing of power efficient IIR filters are desirable the power is element that can directly create a difference in implemented design considering the efficiency, durability and life of devices. Thus for meeting the requirements like cost efficient, the occupied area, the implemented functionality of design in the desired applications which have the implemented use of filter thus optimizing power ,performance and area is very important to meet the perfect combination of these elements in design.

4.2 Related Work:

The paper [1] tells about the application of digital filter in hearing aid as digital filters are used in processing of speech audio type of signals and enhance the hearing aid by enhancing specific frequency. The authors were successful in improving hearing aid by using high quality signal processing methodology and the implemented IIR filter was successful in implementing the desired model .The research demonstrates the usage of digital filter as an application of FPGA in field of hearing aids. The addition of technique of fixed point arithmetic in order to utilize its functionality in relevant manner and considering the performance of filter and by using so the optimized usage of FPGA. The problem with conventional floating point arithmetic was overcomes by using fixed point method of implementation with the use of fixed number of fractional bits of design which makes the hardware implementation of design more efficient. This is an important aspect that was discussed in paper. The design implemented which was proposed of reducing power was successfully achieved by author as low power design makes it more durable and design more efficient especially in design of hearing aids which operates on small battery. The paper was also successful in designing filter with high speed of operation which was achieved with help of high sampling rate which was highly accurate as in hearing aid of application in real time should be fast and precise. As speed is crucial or latency is important aspect to consider. This implemented design on FPGA serves above many advantages. By reducing the computation of design and maintaining the desired functionally is important task and bit difficult to which can be achieved by optimizing design of filter which makes it suitable

for design of resources which are limited .The author extensively designed the methodology in finding coefficients of filters. In order to reduce the coefficients complexity author proposes special calculation technique. The author also proposes the cascading of filter which is chooses as infinite impulse response filter .The cascading structures serves many advantages as it provides flexibility by adding filter and design is named as biquad type of structures and the type of filter was considered as second order impulse infinite response filter as this filter has advantage of simple design and makes use of less coefficients as compared to finite impulse response filter.

The paper [2] highlights the use of carry select adder as an integral part of designing infinite impulse response filter the paper concludes use of digital filters in digital signal processing application as base of carry select adder which improves efficiency and enhance power by optimizing also paper talks about the speed or the delay factor of design while implementing digital IIR filter. The analysis of results from experiments the paper showcases the important results of optimizing power of architectural design while reducing power by not affecting the performance of filter which is designed. The paper by performing numerous simulations and designs and by doing comparative analysis of circuits the filtered design of better quality in terms of power. The results obtained by analysing the experimental results which validates the overall functionality of design using optimized carry select adder which achieved desired results without affecting or disturbing the functionality of design. The paper also demonstrates from analysing simulation results and experiments proposed design of infinite impulse response filter achieves relevant improvement in performance of design also improves accuracy. This improves response of filter. In this paper author does thorough analysis of power consumed by design, area utilized by design also speed? The detailed analysis of propose digital filter by author focuses on filter type of structure correct usage of quantized coefficient values and the architecture of implemented carry select adder of implemented design .The paper also talks how the speed of design as compared to earlier design using the proposed filter design methodology and in implemented design. The paper speaks about the power performance and issues in earlier designs which is needed in digital filter which are very important in modern digital filter of digital filters implementation in earlier available methods. The author has proposed this paper in 45 nm technology.

4.3 Methodology

4.3.1. Coarse auto density control

Is a feature in design that helps to ensure that the layout of a chip meets certain density requirements? It is a tool used to optimize the placement of components on the chip to minimize the amount of wasted space and improve the overall performance of the circuit.The density of a chip refers to the amount of silicon area used by a design compared to the total available silicon area on the chip. In order to make the most efficient use of the available space, designers use a variety of techniques to optimize the placement of components. Coarse auto density control is one such technique. The process of coarse auto density control involves dividing the layout area of the chip into small regions and then comparing the density of each region to a predetermined target density. If the density of a particular region is below the target density, the placement tool will automatically move components closer together in order to increase the density. Conversely, if the density of a region is above the target density, the tool will move components further apart in order to reduce the density [5]. Coarse auto density control is typically used in the early stages of the design process to quickly achieve a rough density distribution of the layout. It is often followed by a more detailed, fine-grained density optimization process to further refine the placement of components and improve the overall chip performance.

4.3.2. Timing based Path optimization

Path-based time optimization techniques involve analysing the critical path of a circuit and making changes to reduce the delay on that path. Some common path-based optimization techniques include:

i) This involves reducing the delay of individual gates on the critical path by optimizing their size, delay, or placement. Techniques like gate sizing and buffer insertion can be used to improve the performance of gates on the critical path.

ii). Retiming: This involves shifting the registers in a circuit to different locations to reduce the critical path delay. By moving registers closer to the critical path, the timing performance of the path can be improved [7]

Overall, path-based time optimization techniques are used to ensure that the critical path of a digital circuit meets its timing requirements, and the circuit can operate at the required speed.

4.3.3. Logic Restructuring

Logic restructuring is a low-power reduction technique used in VLSI design to optimize the combinational logic in a circuit to reduce its power consumption. This technique involves modifying the logic structure of the circuit to reduce its switching activity, thereby reducing dynamic power consumption.

The logic restructuring technique can be classified into two categories: gate-level and RTL-level.

1 .Gate-level Logic Restructuring:

i) Gate-level logic restructuring involves modifying the logic gates in the circuit to reduce the power consumption. The following are some common techniques used in gate-level logic restructuring:

ii)Boolean Logic Optimization: Boolean logic optimization is a technique used to simplify the Boolean expressions in the circuit. The simplified Boolean expression reduces the number of gates required in the circuit, which in turn reduces the power consumption.

iii)Gate Replacement: Gate replacement involves replacing the high-power gates such as NAND and NOR gates with low-power gates such as AND and OR gates. This technique reduces the power consumption of the circuit without affecting its functionality.

iv) Gate Merging: Gate merging involves combining two or more gates in the circuit to reduce the number of gates required. This technique reduces the power consumption of the circuit by reducing the number of gates that need to switch during operation.

2 .RTL-level Logic Restructuring

i)RTL-level logic restructuring involves modifying the RTL (Register Transfer Level) code to reduce the power consumption of the circuit. The following are some common techniques used in RTL-level logic restructuring [10].

ii)Combinational Logic Optimization: Combinational logic optimization involves simplifying the combinational logic in the RTL code. This technique reduces the number of gates required in the circuit, which in turn reduces the power consumption.

iii) Retiming: Retiming involves moving the registers in the circuit to optimize the timing of the circuit. This technique reduces the number of gates that need to switch during operation, which reduces the power consumption.

iv) Data path Optimization: Data path optimization involves optimizing the datapath in the circuit to reduce the power consumption. This technique involves modifying the number and size of the registers and the operations performed on them to reduce the power consumption.
In conclusion, logic restructuring is a low-power reduction technique used in VLSI design to optimize the combinational logic in a circuit to reduce its power consumption. This technique involves modifying the logic structure of the circuit at the gate-level or RTL-level to reduce the switching activity and thereby reduce the dynamic power consumption. The gate-level logic restructuring involves modifying the logic gates in the circuit, while the RTL-level logic restructuring involves modifying the RTL code.

4. Self Gating

Self-gating is a technique used in circuit design to reduce power consumption by dynamically controlling the power supply based on the activity of the circuit. It involves the implementation of a gating circuit that is directly influenced by the input signal of the circuit. By monitoring the input signal, the gating circuit selectively cuts off the power supply to inactive portions of the circuit, effectively reducing leakage current and conserving power.The gating circuit is typically composed of a low-power transistor that is connected in series with the power supply. When the input signal is low or when the circuit is not in use, the gating circuit turns off the transistor, interrupting the power supply to the circuit. This prevents unnecessary power consumption and reduces static power dissipation.The key advantage of self-gating is its ability to adaptively control the power supply based on the circuit's activity. By dynamically adjusting the power supply, power savings can be achieved without sacrificing the circuit's functionality or performance. This is particularly beneficial in scenarios where the circuit operates in intermittent or bursty patterns, as the power supply can be deactivated during idle periods.Implementing self-gating requires careful consideration of the circuit's operational requirements and the characteristics of the input signal. The gating circuit must be designed to accurately detect the circuit's activity and respond quickly to changes in the input signal. Additionally, appropriate control logic must be implemented to ensure the proper synchronization between the gating circuit and the circuit's operation. Overall, self-gating is an effective technique to reduce power consumption in integrated circuits.

4.4 Results and analysis

In this section the paper proposed the detailed analysis in analytical and graphical manner of different parameters like leakage power, switching power and delay analysis.

1. Comparison of Leakage power

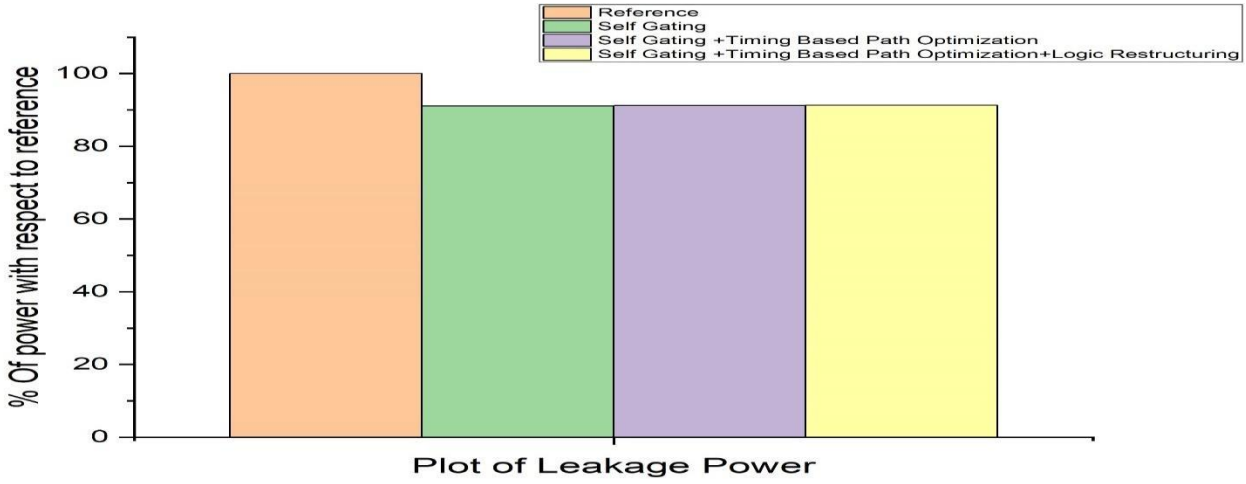

Figure 4.1 Plot of Leakage Power

As seen from above graph we see that after applying self-gating technique we see decrease in percentage in leakage power which is nearly 10% .

2 .Switching power

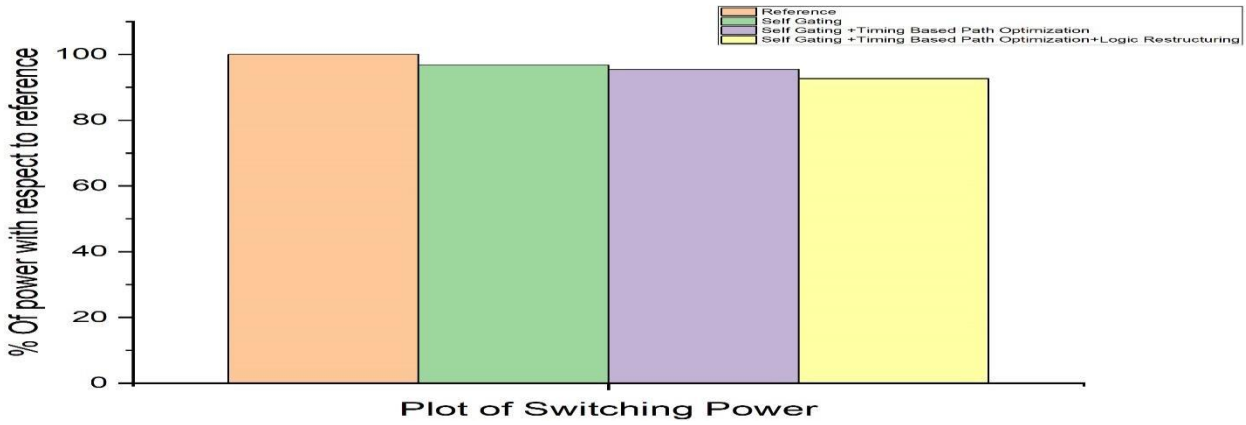

Figure 4.2.Plot of Switching Power

As seen from above graph we see gradual decrease in switching power the power decreased with self-gating and when added with path optimization we see more decrease and further after inclusion of logic restructuring, we see more decrease in switching power.

3 .Total power

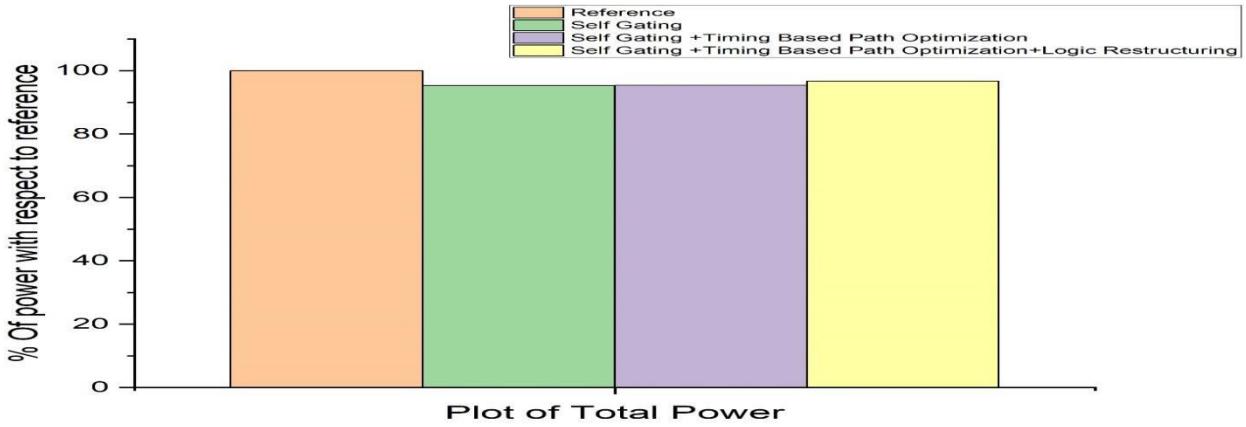

Figure 4.3 Plot of Total Power

As we can see from above graph the total power decreases in self gating and with inclusion of logic restructuring the power is relatively higher than earlier 2 methods so if total power is important factor to consider than self-gating and self-gating with timing based optimization is desired one.

4 .Total Dynamic Power

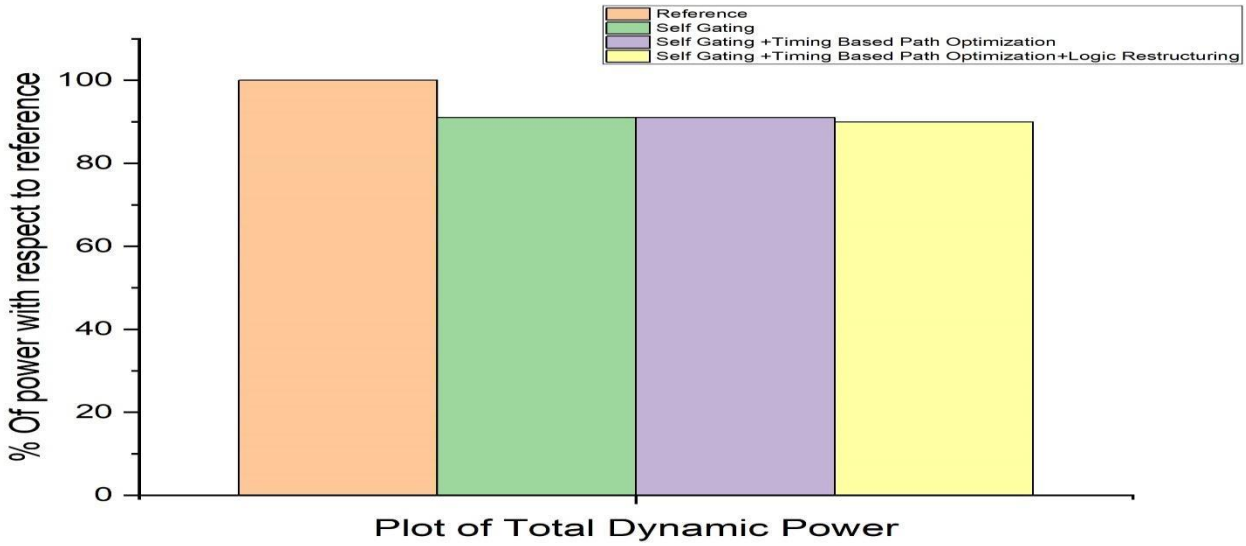

Figure 4.4 Plot of Total Dynamic Power

As seen from above graph the dynamic power is reducing considerably and best option is logic restructuring and timing-based optimization.

5 .Total Negative slack

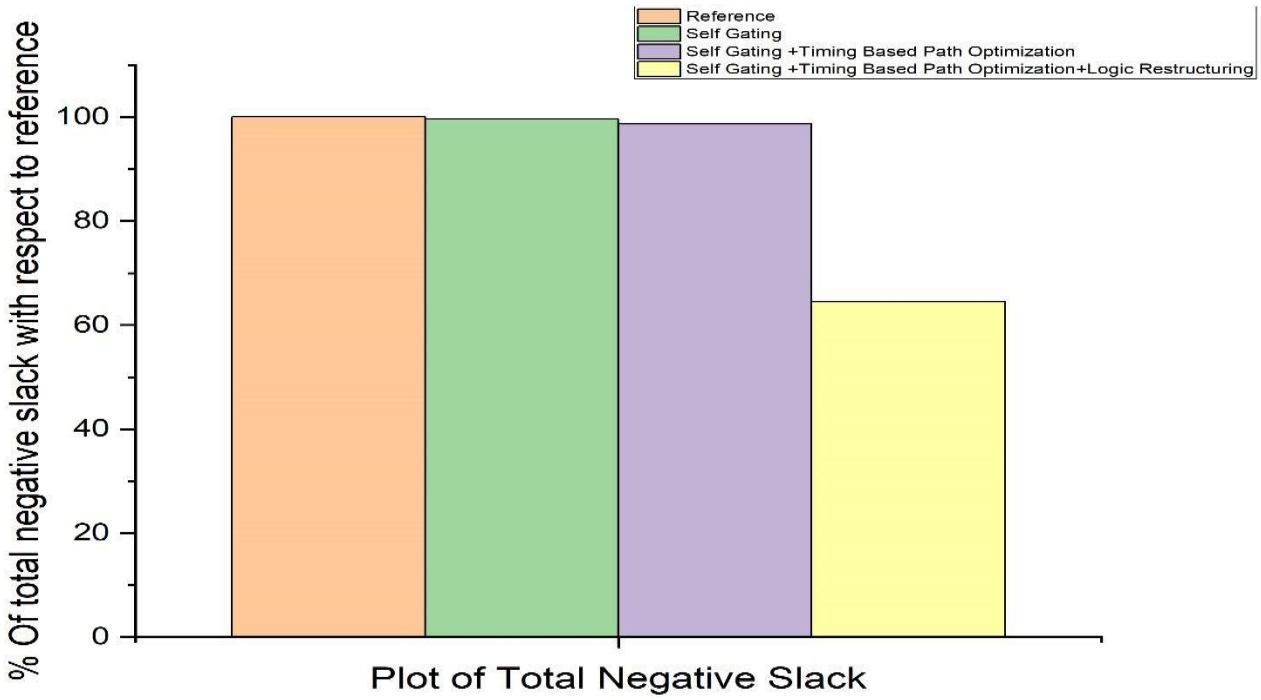

Figure 4.5 Plot of Total Negative Slack

As seen from above plot we see that the negative slack goes on decreasing after inclusion of self-gating than it reduces more after inclusion of timing-based path optimization and is reduced nearly 40 % after use of logic restructuring.

CHAPTER 5: SIMULATION AND RESULTS

This section demonstrates the actual working of implemented model and its verification of functionality using waveform analysis and also the different results of timing, power and area of design respectively.

5.1 Basic Digital Filter

5.1.1 Waveform

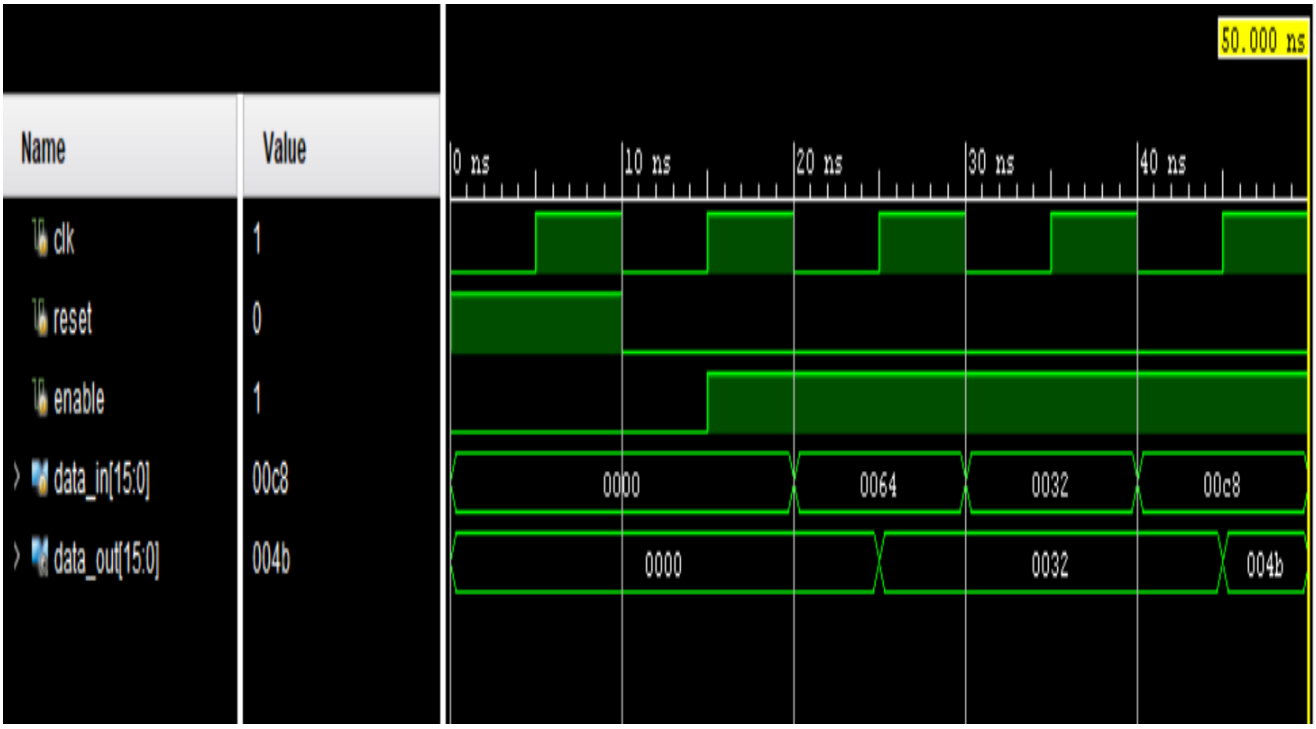

Figure 5.1 Waveform of Basic Digital Filter

The filter equation in designed code is given as

$sum\_1 = (coeff_b * x1 + coeff_a * x2 - coeff_a * y1 - coeff_b * y2) >> 16$ (2)

Hence to evaluate the output value for an instance of value 64 the block goes via following steps

1) Initially all registers values are assigned as 0 due to reset condition.

2)When enable is activated the values of data_in register is transferred to ‘x1’ the earlier stored value of ‘x1’ is stored in ‘x2’. Similarly for ‘y1’ and ‘y2’.

3) Then the equation (2) is evaluated the values of coeff_a and coeff_b are assigned as 0.5 and are replaced by value 32768 to represent in fixed point arithmetic format. The evaluated result is then right shifted by 16 bits as the equation. The equation is evaluated in fixed point arithmetic form.

4) Lastly the evaluated value is of sum_1 is passed to data_out.

For instance for value of 64 the expression will be for first clock cycle values of registers are 'x1' =64, 'x2','y1' and 'y2' =0 the eqn 2 will be modified as

sum_1 = (coeff_b *64 +coeff_a *0 – coeff_a * 0 – coeff_b *0) >> 16

= 32768 *64 +0 – 0) >> 16

=32

Thus for input value of 64 output value will be 32.

5.1.2 RTL Schematic

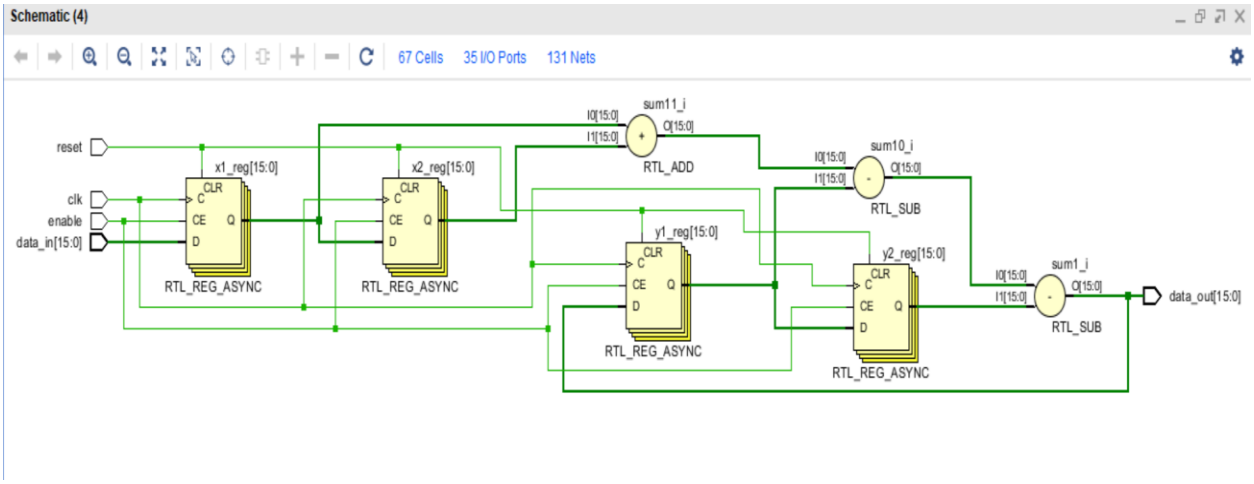

Figure 5.2 RTL Schematic of Basic Digital Filter

As seen from above we see the RTL schematic of basic digital filter as no new hardware for power and timing optimisation is implemented the schematic is very basic and small with less circuit elements involved the schematic comprises of cells with count of 67 cells of type input /output having 35 count the nets comprises of 131 counts.

5.1.3 Synthesized Schematic

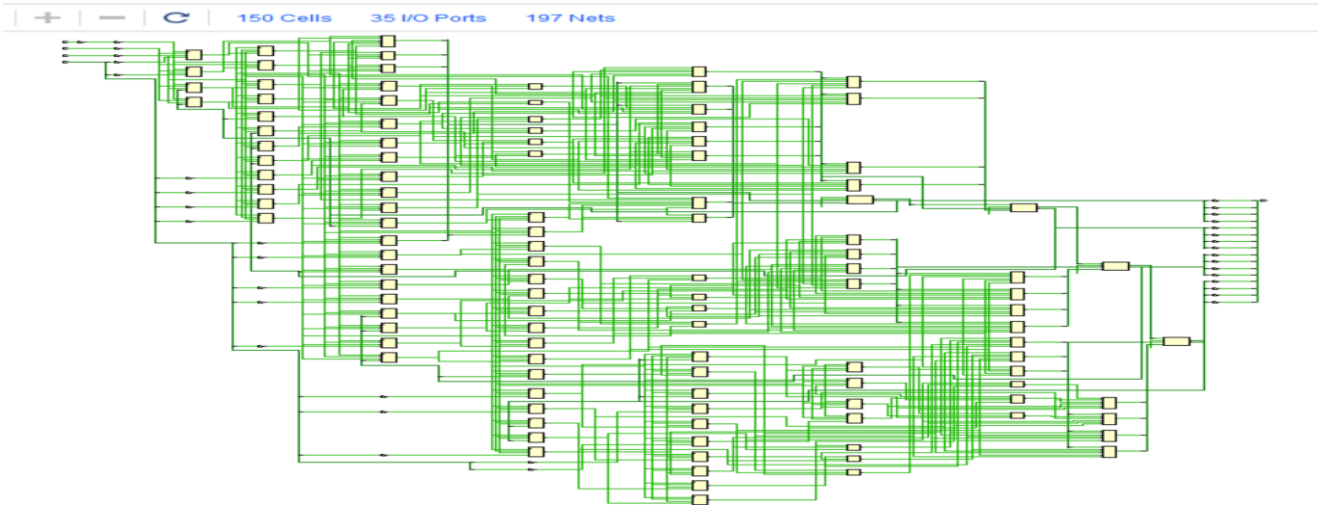

Figure 5.3 Synthesized Schematic of Basic Digital Filter

The above is synthesized schematic of basic digital filter which is more abstracted level of implementation of RTL schematic from above we can see that the design have more elements as compared to RTL one as it is more detailed representation of RTL which have detailed analysis of logic implemented and timing paths the schematic comprises of 150 count of cells, 35 count of Input/output type of ports and 197 count of nets.

5.2 Digital Filter with conventional Clock Gating:

5.2.1 Waveform:

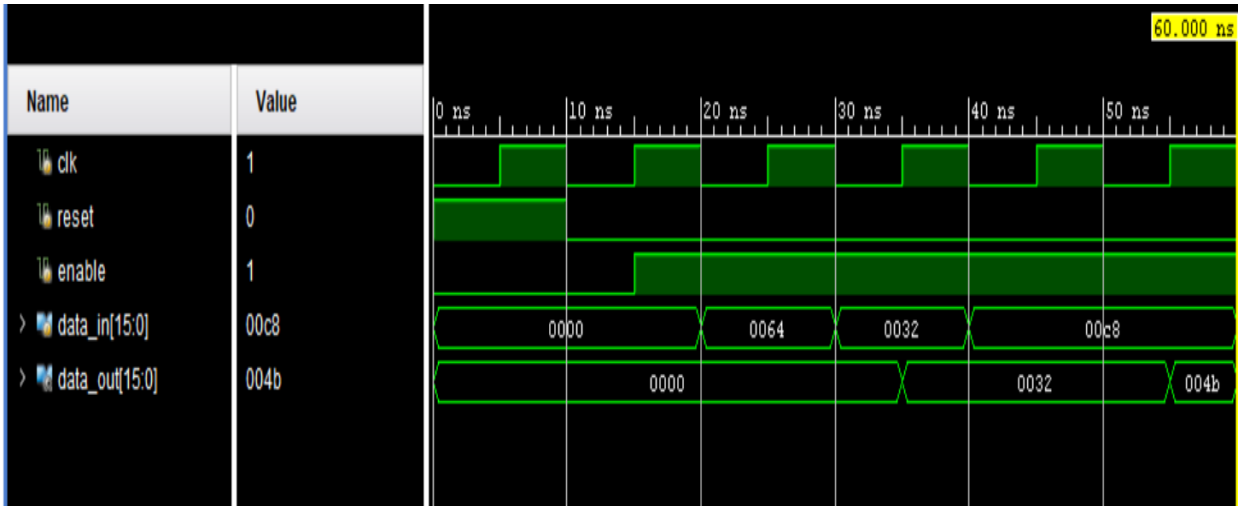

Figure 5.4 Waveform of Basic Digital Filter with Conventional Clock Gating

The filter equation in designed code is given as

$$sum\_1 = (coeff_b * x1 + coeff_a * x2 - coeff_a * y1 - coeff_b * y2) >> 16 \quad (2)$$

Hence to evaluate the output value for an instance of value 64 the block goes via following steps

1) Initially all registers values are assigned as 0 due to reset condition.

2)When enable is activated the values of data_in register is transferred to ‘x1’ the earlier stored value of ‘x1’ is stored in ‘x2’. Similarly for ‘y1’ and ‘y2’.

3) Then the equation (2) is evaluated the values of coeff_a and coeff_b are assigned as 0.5 and are replaced by value 32768 to represent in fixed point arithmetic format. The evaluated result is then right shifted by 16 bits as the equation. The equation is evaluated in fixed point arithmetic form.

4) Lastly the evaluated value is of sum_1 is passed to data_out.

For instance for value of 64 the expression will be for first clock cycle values of registers are ‘x1’ =64, ‘x2’,’y1’ and ‘y2’ =0 the eqn 2 will be modified as

sum_1 = (coeff_b *64 +coeff_a *0 – coeff_a * 0 – coeff_b *0) >> 16

= 32768 *64 +0 – 0) >> 16

=32

Thus for input value of 64 output value will be 32.

5.2.2 RTL Schematic

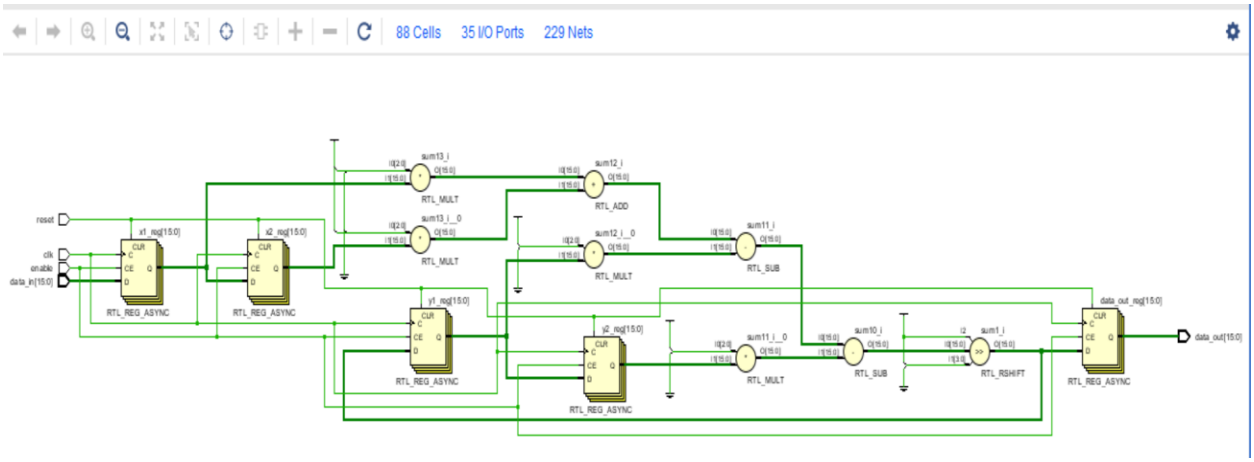

Figure 5.5 RTL Schematic of Basic Digital Filter with Conventional Clock Gating

As seen from above we see the RTL schematic of basic digital filter with conventional clock gating as this adds hardware for power and timing optimisation is implemented the schematic is

basically more elements than basic filter schematic comprises of cells with count of 67 ports of type input /output having 35 count the nets comprises of 131 counts.

5.2.3 Synthesized Schematic

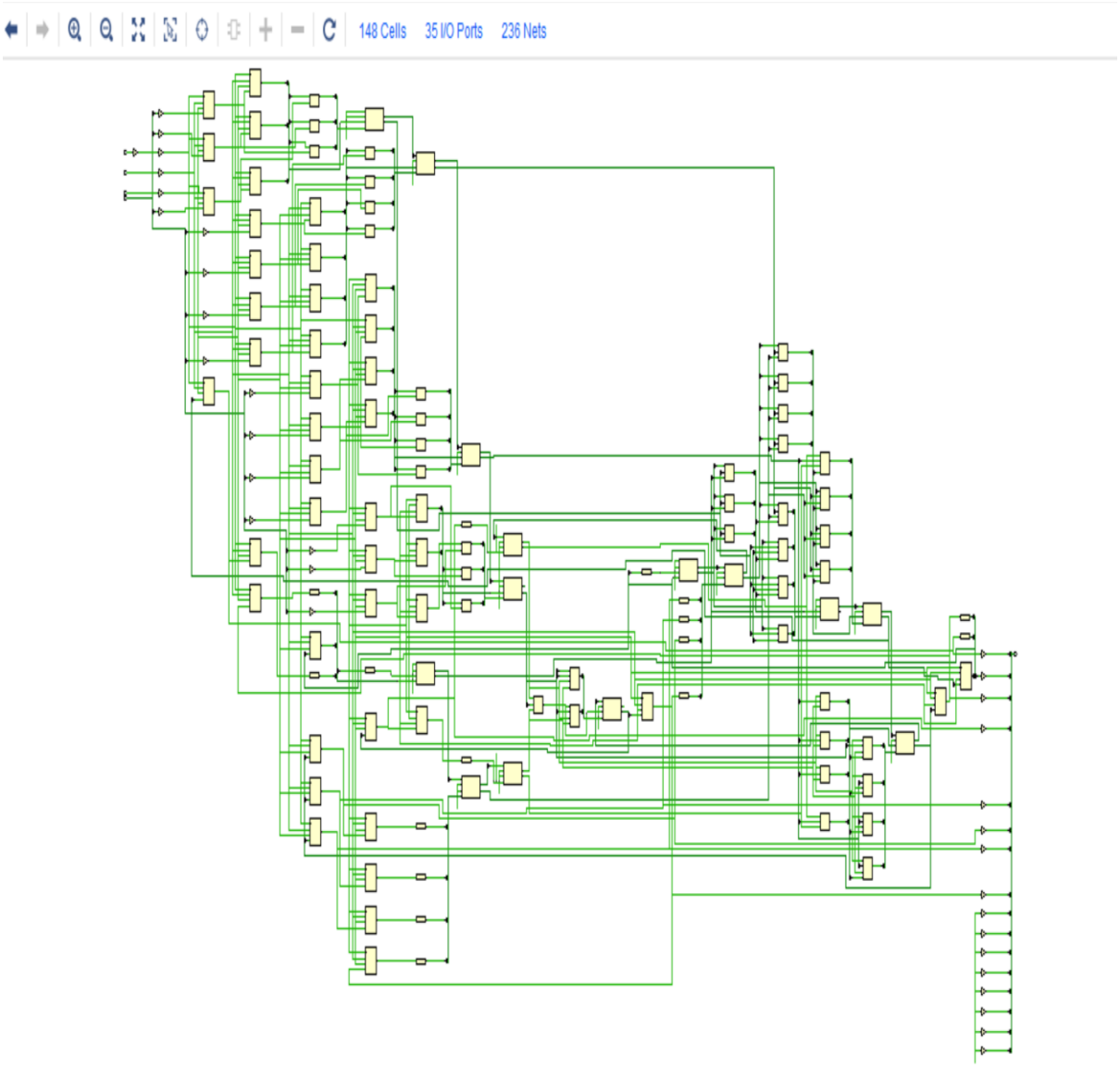

Figure 5.6 Synthesized Schematic of Basic Digital Filter with Conventional Clock Gating

The above is synthesized schematic of basic digital filter with clock gating which is more abstracted level of implementation of RTL schematic from above we can see that the design have more elements as compared to RTL one as it is more detailed representation of RTL which have

detailed analysis of logic implemented and timing paths the schematic comprises of 148 count of cells, 35 count of Input/output type of ports and 236 count of nets.

5.3 Digital Filter with Proposed Clock Gating:

5.3.1 Waveform

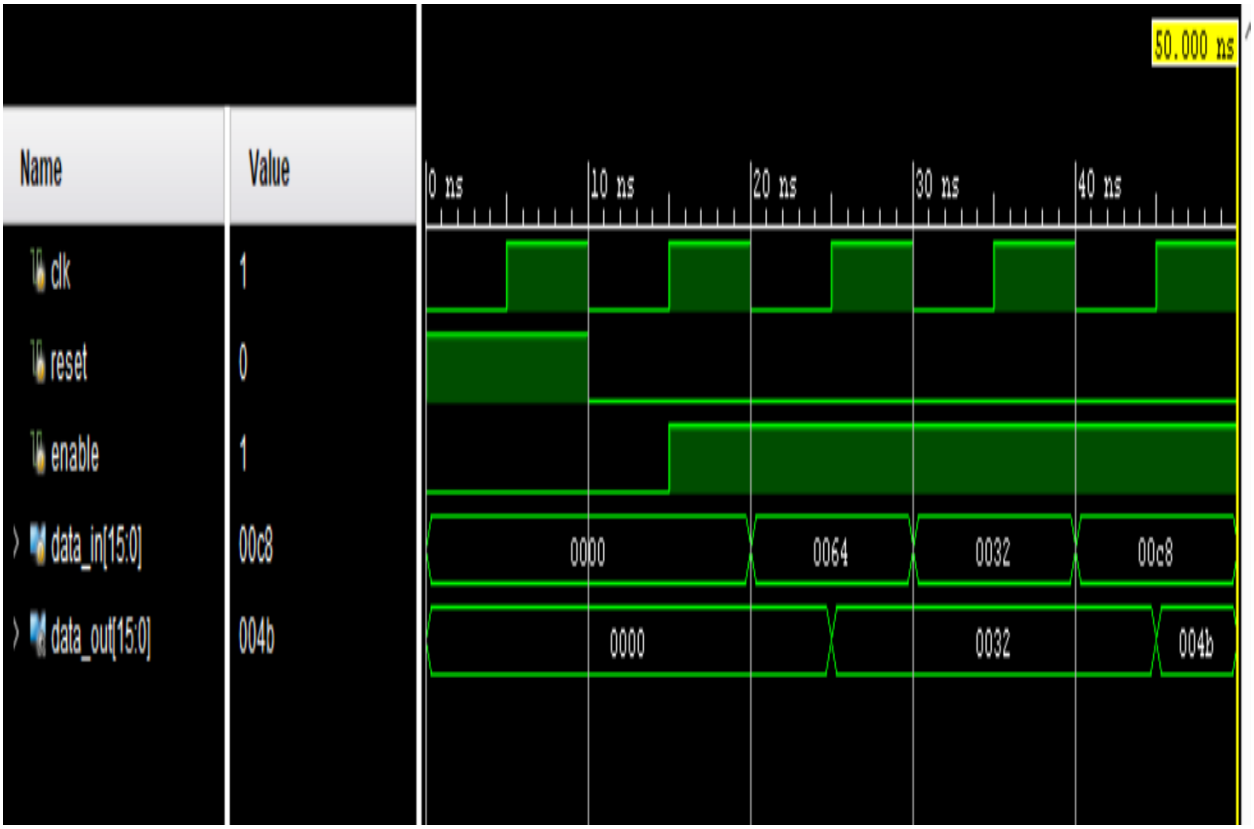

Figure 5.7 Waveform of Digital Filter with Proposed Clock Gating

The filter equation in designed code is given as

$$sum\_1 = (coeff_b * x1 + coeff_a * x2 - coeff_a * y1 - coeff_b * y2) >> 16 \quad (2)$$

Hence to evaluate the output value for an instance of value 64 the block goes via following steps

1) Initially all registers values are assigned as 0 due to reset condition.

2)When enable is activated the values of data_in register is transferred to ‘x1’ the earlier stored value of ‘x1’ is stored in ‘x2’. Similarly for ‘y1’ and ‘y2’.

3) Then the equation (2) is evaluated the values of coeff_a and coeff_b are assigned as 0.5 and are replaced by value 32768 to represent in fixed point arithmetic format. The evaluated result is

then right shifted by 16 bits as the equation. The equation is evaluated in fixed point arithmetic form.

4) Lastly the evaluated value is of sum_1 is passed to data_out.

For instance at time when input is 32

Given the updated input value of 32 and the previous register values will be updated as

x1 = 32 , x2 = 64 ,y1 = 32 ,y2 = 0

We can compute the value of `sum1` as follows:

sum1 = (coeff_b * x1 + coeff_a * x2 - coeff_a * y1 - coeff_b * y2) >> 16

= (32768 * 32 + 32768 * 64 - 32768 * 32 - 32768 * 0) >> 16

= (1048576 + 2097152 - 1048576 - 0) >> 16

= 2097152 >> 16

= 32

Therefore, for an input value of 32 in the current iteration, the output value will indeed be 32.

5.3.2 RTL Schematic

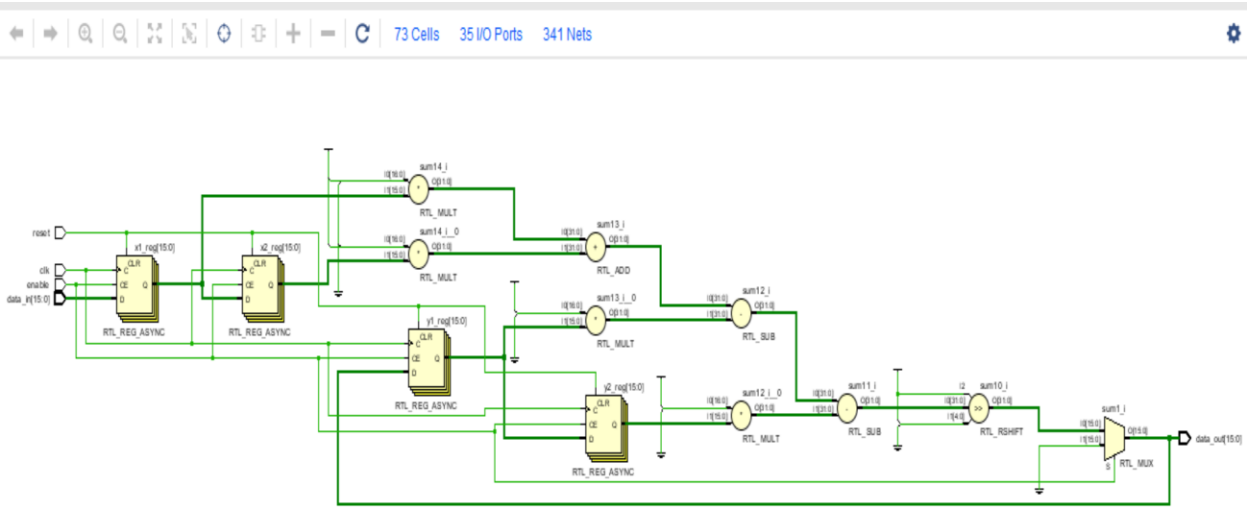

Figure 5.8 RTL Schematic of Digital Filter with Proposed Clock Gating

As seen from above we see the RTL schematic of digital filter with proposed clock gating as this adds hardware for power and timing optimisation is implemented the schematic is basically more elements than basic filter schematic comprises of cells with count of 73 ports of type input output having 35 count the nets comprises of 341 counts.

5.3.3 Synthesized Schematic

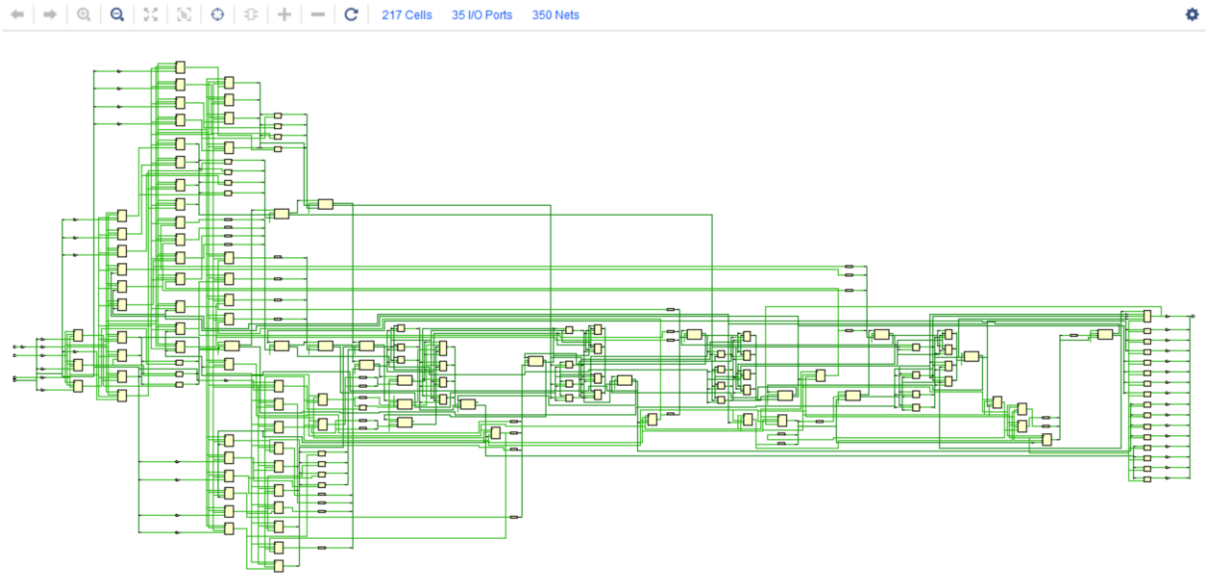

Figure 5.9 Synthesized Schematic of Digital Filter with Proposed Clock Gating

The above is synthesized schematic of basic digital filter with proposed clock gating which is more abstracted level of implementation of RTL schematic from above we can see that the design have more elements as compared to RTL one as it is more detailed representation of RTL which have detailed analysis of logic implemented and timing paths the schematic comprises of 217 count of cells, 35 count of Input/output type of ports and 350 count of nets.

CHAPTER 6: POWER, AREA AND TIME OF DESIGN

In this section the analysis of Power, Performance and Area of design are done by graphical and analytic method the designs are plotted comparatively to get a good understanding of overall performance of design the analysis shows the desired results in terms of Power and timing considerations while causing trade-off in area consideration.

6.1 Area of Design:

Area utilization is a critical factor in VLSI design as it directly impacts the physical size and manufacturing cost of the integrated circuit. In the context of the analyzed design, the observations reveal that the proposed clock gating technique utilizes more area compared to the conventional clock gating technique and the basic digital filter.The increase in area utilization in the proposed clock gating technique can be attributed to the additional circuitry required to implement the advanced gating mechanism. The gating circuitry, control logic, and associated interconnections contribute to the overall increase in area. These additional components are necessary to achieve the desired power savings and improved performance offered by the proposed clock gating technique. While the increased area utilization may be a drawback in terms of circuit size and manufacturing cost, it is important to consider the trade-off between area and the benefits gained in power reduction and performance improvement. In many cases, the potential power savings and performance enhancements outweigh the increase in area, making the proposed clock gating technique a favorable choice.

	RTL Schematic			Synthesized Schematic		
	cells	i/o ports	nets	cells	i/o ports	nets
Basic Digital filter	67	35	131	150	35	197
Digital filter with clock gating	88	35	229	148	35	236
Digital filter with proposed clock gating	73	35	341	217	35	350

Table 6.1 Numbers of Elements in RTL & Synthesized Design

6.1.1 RTL schematic

6.1.1.1 Cells

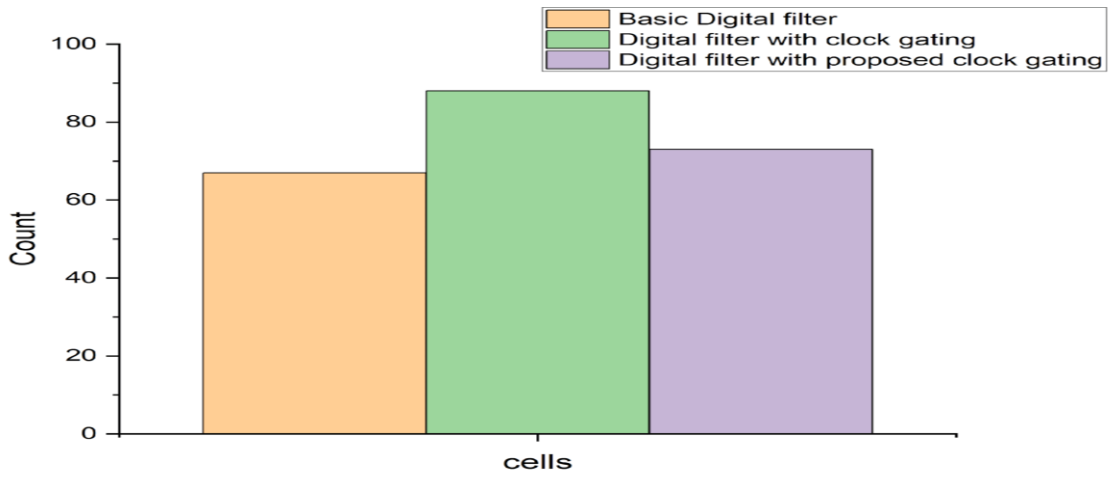

Figure 6.1 Bar graph of comparative analysis of Cells utilized in all RTL designs

The above is bar graph of analysis of cells utilized by design in RTL schematic from which we conclude that the cells in design were lesser in basic digital filter whereas the digital filter with clock gating have maximum count of cells and proposed digital filter has less count than conventional method clock gating with digital filter.

6.1.1.2 I/O Ports

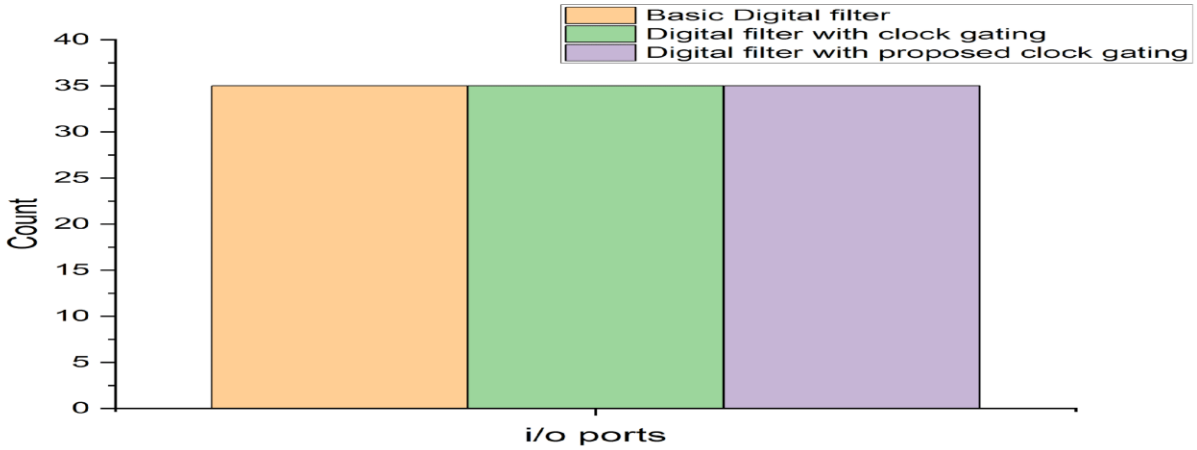

Figure 6.2 Bar graph of comparative analysis of Ports utilized in all RTL designs

The above is bar graph of analysis of input/output ports utilized by design in RTL schematic from which we conclude that the ports count is not hindered from which we conclude that the architectural design for functionality is not affected.

6.1.1.3 Nets

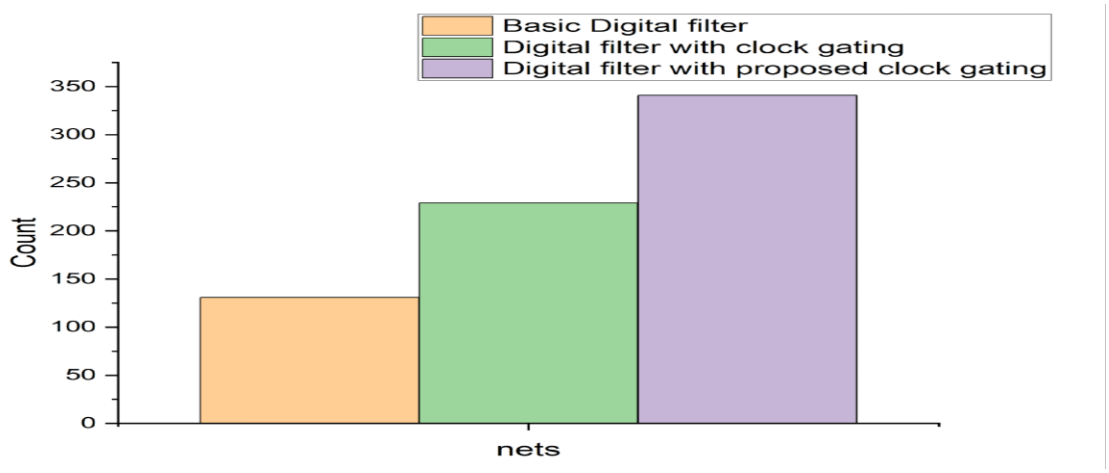

Figure 6.3 Bar graph of comparative analysis of Nets utilized in all RTL designs

The above is bar graph of analysis of nets utilized by design in RTL schematic from which we conclude that the nets in design were lesser in basic digital filter whereas the digital filter with clock gating have more in count of cells and proposed digital filter has maximum count than conventional method clock gating with digital filter the design is supposed to be bringing parallel operation in design.

6.1.2 Synthesized Schematic

6.1.2.1 Cells

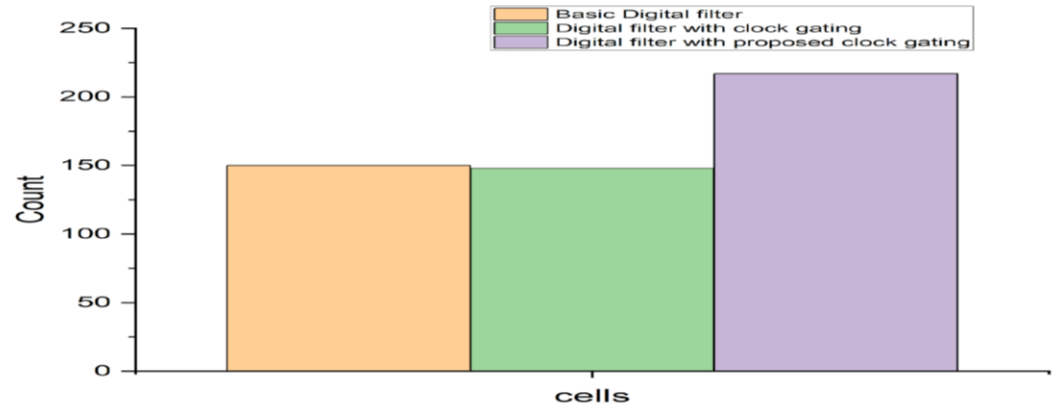

Figure 6.4 Bar graph of comparative analysis of Cells utilized in all Synthesized designs

The above is bar graph of analysis of cells utilized by design in Synthesized schematic from which we conclude that the cells in design were lesser in basic digital filter whereas the digital filter with clock gating have more count of cells and proposed digital filter has maximum count than conventional method clock gating with digital filter.

6.1.2.2 I/O Ports

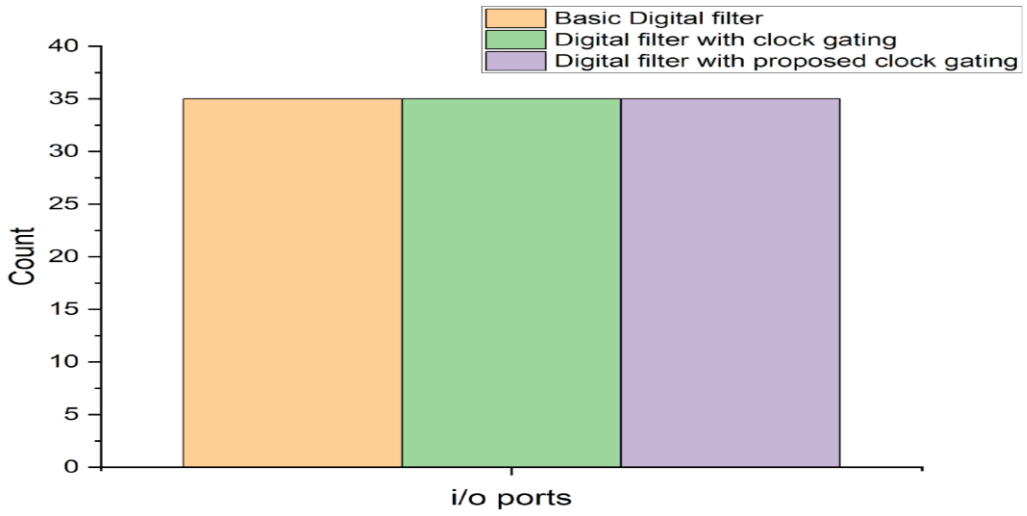

Figure 6.5 Bar graph of comparative analysis of Ports utilized in all Synthesized designs

The above is bar graph of analysis of input/output ports utilized by design in Synthesized schematic from which we conclude that the ports count is not hindered from which we conclude that the architectural design for functionality is not affected.

6.1.2.3 Nets

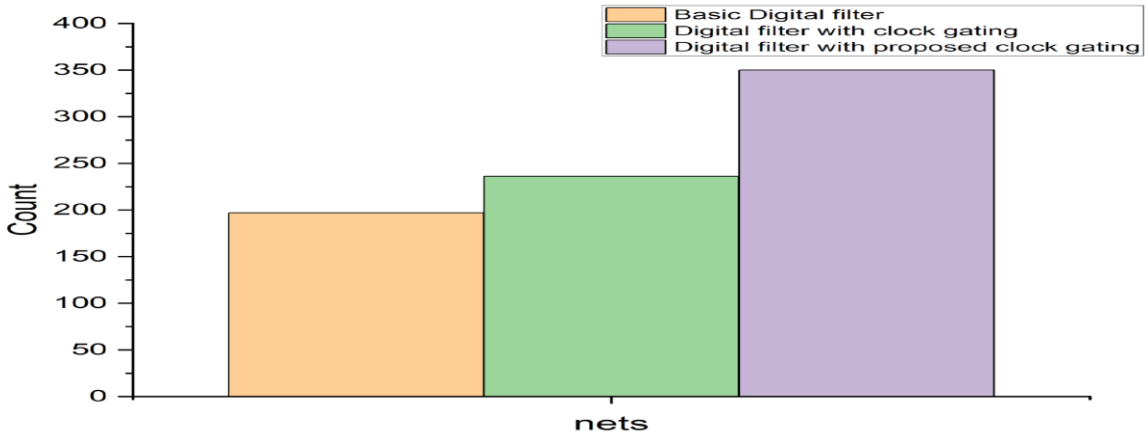

Figure 6.6 Bar graph of comparative analysis of Nets utilized in all synthesized designs

The above is bar graph of analysis of nets utilized by design in Synthesized schematic from which we conclude that the nets in design were lesser in basic digital filter whereas the digital filter with clock gating have more in count of cells and proposed digital filter has maximum count than conventional method clock gating with digital filter the design is supposed to be bringing parallel operation in design.

6.2 Power

Power optimization plays a crucial role in VLSI design, aiming to minimize power consumption in integrated circuits. In modern electronic devices, such as smartphones, wearable's, and IoT devices, power efficiency is of utmost importance to enhance battery life and reduce heat dissipation. Various techniques are employed to achieve power reduction. Dynamic power consumption can be minimized by optimizing circuit activity and reducing switching capacitances. This can be achieved through techniques like voltage scaling, where the operating voltage is reduced during periods of low activity [11]. Clock gating is another method that selectively enables clock signals to only active portions of the circuit, effectively reducing unnecessary switching. Static power, also known as leakage power, is the power consumed even when the circuit is idle. To minimize static power, power gating techniques are employed, where inactive portions of the circuit are completely powered off. Additionally, advanced fabrication processes and circuit design methodologies are used to reduce leakage currents.Power analysis and optimization are performed at various stages of the design process, starting from architectural exploration to physical implementation. Efficient power management strategies not only improve energy efficiency but also ensure system reliability, thermal management, and overall performance.

Overall, power optimization in VLSI design is vital for creating energy-efficient and high-performance integrated circuits that meet the power constraints of modern electronic devices.

Power	Basic Digital Filter	Digital Filter with clock gating	Digital Filter with proposed clock gating
	17.467w	16.99w	8.312w

Table 6.2 Power Analysis of design in RTL & Synthesized Design

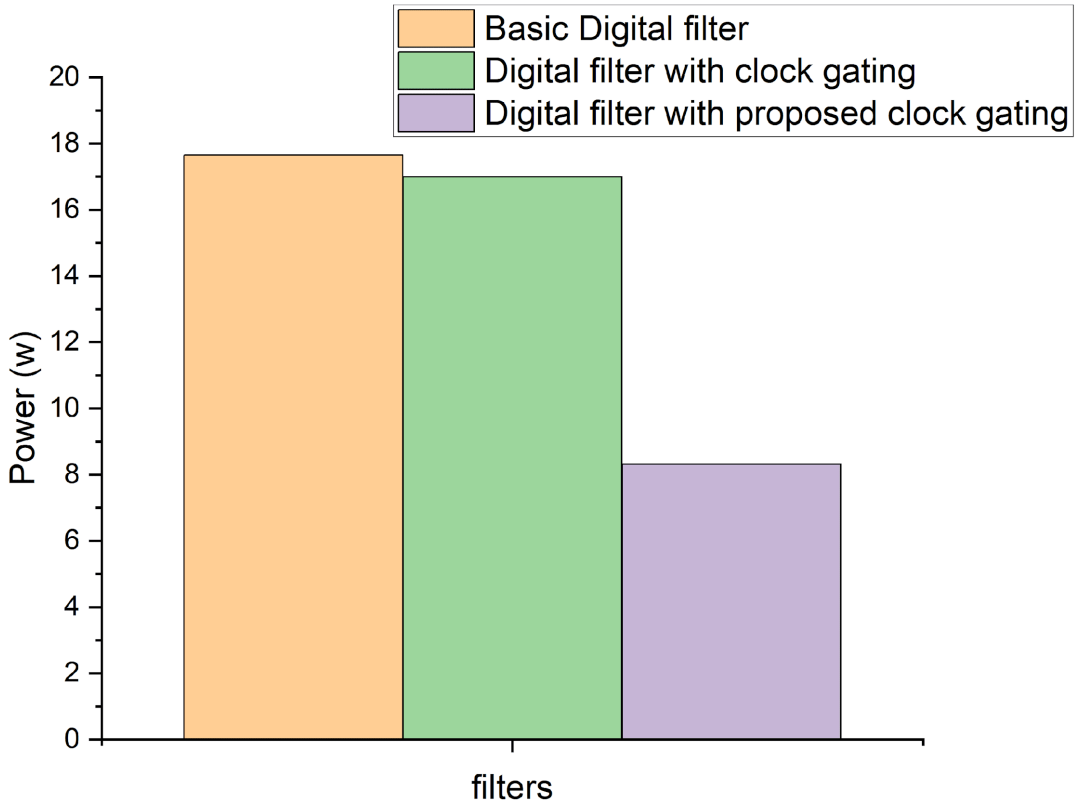

Figure 6.7 Bar graph of comparative analysis of Total Power utilized in all designs

The above is bar graph of analysis of total power utilized by design in RTL schematic from which we conclude that the power in design is highest in basic digital filter whereas the digital filter with clock gating have less power which is just slightly less as compared to basic digital filter and proposed digital filter has minimum power than conventional method clock gating with digital filter and basic digital filter the design is supposed to be bringing parallel operation in design the power is almost saved by 52 % as compared to basic design of filter.

6.3 Timing

Timing plays a critical role in VLSI design as it determines the performance and functionality of integrated circuits. Timing analysis ensures that all signals propagate through the circuit within the specified time constraints, maintaining proper synchronization and avoiding signal integrity issues. In VLSI design, timing analysis involves evaluating the delays of various paths in the circuit, including combinational logic paths and sequential elements like flip-flops and registers. It ensures that signals arrive at their intended destinations at the correct time, preventing setup

and hold violations. Timing optimization techniques are employed to meet timing requirements. These include buffer insertion, wire sizing, and clock tree optimization. Buffer insertion helps in reducing signal delays and balancing the load along critical paths. Wire sizing involves adjusting the widths of interconnect wires to minimize delay variations. Clock tree optimization aims to distribute the clock signal efficiently across the circuit to minimize clock skew and ensure reliable clock synchronization.

Timing slack	Basic Digital Filter	Digital Filter with clock gating	Digital Filter with proposed clock gating
	1297ps	1484ps	1350ps

Table 6.3 Timing analysis of design s in RTL & Synthesized Design

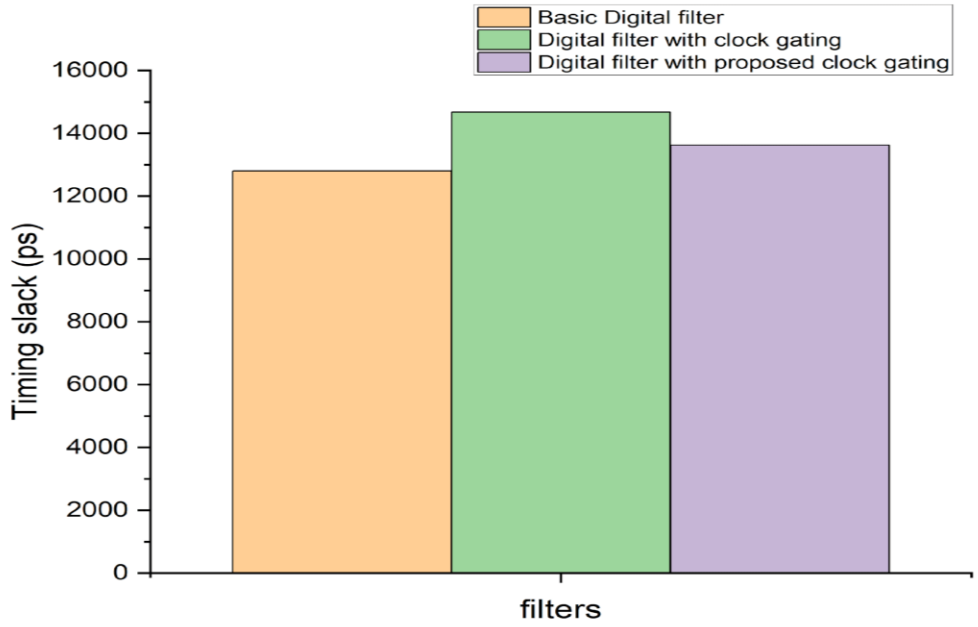

Figure 6.8 Bar graph of comparative analysis of Timing in all designs

The above is bar graph of analysis of timing slack utilized by design which we conclude that the delay in design were lesser in basic digital filter whereas the digital filter with clock gating have more delay and proposed digital filter has less than digital filter with conventional clock gating but more than basic digital filter.

CHAPTER 7: CONCLUSION

This paper presents a comprehensive analysis of the power, performance, and area metrics in the design of second-order infinite impulse response (IIR) digital filters. The importance of these filters in various applications, such as wireless communication, audio processing, and biomedical signal processing, is highlighted, emphasizing the need for optimizing their power consumption, enhancing performance, and efficiently utilizing the available area resources. Through a meticulous examination of schematics and careful observation of data, the paper demonstrates significant improvements in power efficiency when employing the proposed digital filter design compared to conventional methodologies. The proposed techniques, including the incorporation of a clock gating technique, effectively reduce unnecessary switching activities and conserve power during idle periods, leading to substantial power savings. This improvement in power consumption is of utmost importance in power-constrained applications, where energy efficiency is a critical factor. Moreover, the implemented clock gating technique not only improves power efficiency but also enhances the timing performance of the design. By minimizing propagation delays and optimizing the clock distribution network, the proposed methodology ensures faster and more efficient signal processing, enabling real-time and high-speed applications. However, it is important to note that the proposed methodology results in a significant increase in the area of the design. This is due to the additional circuitry required to implement the desired methodologies and optimize power and timing performance. Future work could focus on exploring methods to mitigate the impact on area utilization while preserving the efficiency and performance of the design. Techniques such as circuit-level optimizations, algorithmic improvements, and architectural enhancements could be investigated to achieve a more balanced trade-off between power, performance, and area metrics.

In conclusion, this paper provides valuable insights into the power, performance, and area considerations in the design of second-order IIR digital filters. The proposed methodologies demonstrate significant improvements in power efficiency and timing performance, highlighting their relevance and potential in practical applications. By addressing the challenge of increased area utilization, future research can pave the way for more optimized designs that achieve a well-balanced trade-off between power, performance, and area metrics, enabling the deployment of efficient and high-performance digital filter solutions in various domains.

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