M. Tech (VLSI Design and Embedded System)

Puneet Yadav

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DESIGN AND ANALYSIS OF A LOW POWER AND HIGH PERFORMANCE 10T SRAM CELL AT 32 NM TECHNOLOGY NODE

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SUBMITTED BY:

PUNEET YADAV

2K21/VLS/21

UNDER THE SUPERVISION OF

Prof. POORNIMA MITTAL

ELECTRONICS & COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)Bawana Road, Delhi-110042

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ELECTRONICS & COMMUNICATION

ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, Puneet Yadav, Roll No. 2K21/VLS/21 student of M. Tech (VLSI & Embedded systems), hereby declare that the project Dissertation titled **"Design and Analysis of a Low Power and High Performance 10T SRAM Cell at 32 nm Technology node"** which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology is unique and has not been copied without proper citation. This work has never been used to give a degree, diploma associateship, fellowship, or other equivalent title or recognition.

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(Formerly Delhi College of Engineering)Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled **"Design and Analysis of a Low Power and High Performance 10T SRAM Cell at 32 nm Technology node"** which is submitted by **Puneet Yadav, 2K21/VLS/21**, to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the prerequisite for the award of the degree of Master of Technology, is a documentation of the student's projectwork completed under my supervision. To the best of my knowledge, this work has never been submitted in part or in full for any degree or diploma at this university or anywhere else.

Place: Delhi

Date**:** May 30, 2023

Prof. Poornima Mittal

Supervisor, ECE, DTU

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MTech: VLSI Design and Embedded System

(2021-2023)

ABSTRACT

Memory is known to be one of the most crucial parts of any electronic system. However, a class of memory called the cache memory is even more crucial among the type of memories since it is the one working closely in synchronization with the central processing unit. There are millions of SRAM cells inside cache memory. SRAM cells must therefore possess a few essential attributes for cache memory to be reliable, including low dynamic and static power consumption, high data stability, and low read latency.

A comprehensive review of the design and analysis of SRAM cells are performed, focusing on the fundamental building block, the SRAM cell, and its critical performance parameters. The aim is to provide a concise overview of the key concepts and challenges involved in SRAM cell design, highlighting recent advancements and future directions. The review begins with an introduction to SRAM and its significance in various applications. It explores the basic structure and operation of an SRAM cell, emphasizing the importance of stability, read and write capabilities, and power consumption. The different SRAM cell topologies are discussed, along with their advantages and trade-offs. The critical design considerations of SRAM cells, including noise immunity, process variations, and leakage current. Various techniques for improving the stability of SRAM cells, such as the use of feedback and assist circuits, are examined. Moreover, the impact of scaling technologies, such as process technology nodes and transistor scaling, on SRAM cell performance is explored.

Additionally, the analysis of SRAM cell performance metrics, including read and write access times, write margin, stability, and power dissipation have been studied. The influence of key parameters, such as supply voltage, transistor sizing, and load capacitance, on these metrics is discussed. Furthermore, the impact of process variations on yield and reliability is addressed, along with reliability-enhancement techniques. To successfully incorporate these qualities, a comparative analysis of different 10T and 11T SRAM cells has been performed. The performance of the conventional TG10T and 11T SRAM models are compared to the 10T SRAM to showcase enhancements obtained. TG10T SRAM cell deploys two transmission gates instead of two NMOS access

transistors to strengthen writing ability. It also employs two additional buffer transistors so that read stability can be enhanced. The TG10T SRAM cell is proven to be more enhanced in almost every aspect but it consumes more power. The read SNM and write SNM are found to be the largest in the TG10T SRAM cell. The power dissipated by the TG10T cell (i.e., 233.69nW) is approximately two times as compared to the 10T SRAM cell (i.e., 108.65nW) and 11T SRAM cell (i.e., 88.491nW). The analysis also shows that both read and write delay is minimal in TG10T SRAM cells. The read delay is 343.3 psec and the write delay is 494 psec respectively.

A 10T SRAM cell has been proposed and comparison between of different existing 10T and 11T SRAM cells has been performed. The power consumption and read-write behaviors of all the SRAM cells are studied. The power consumed by the TG10T cell (i.e., 233.69nW) is approximately two times in contrast to the 10T SRAM cell (i.e., 108.65nW) and five times when collated to the proposed 10T SRAM cell (i.e., 44.794nW). The analysis associated depicts that the read and write delay is minimum in the proposed 10T SRAM (i.e., 97.7psec & 154.3psec) respectively. All simulations are carried out using LTSPICE software operating at 0.5 Volt in 32 nm CMOS process technology. The proposed transmission gate based 10T SRAM cell consumes minimum power and has better overall read stability as compared to the other designs. The review concludes by highlighting emerging trends and challenges in SRAM cell design, including the exploration of novel device architectures, non-volatile SRAM, and low-power designs for energy-efficient computing systems. It emphasizes the need for continued research and innovation to address the increasing demands for higher density, lower power consumption, and improved reliability in future SRAM cell designs.

A comprehensive overview of the design and analysis of SRAM cells serves as a valuable resource for researchers, engineers, and students working in the field of digital integrated circuit design, offering insights into the current state of SRAM cell technology and potential future directions.

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LIST OF ABBREVIATIONS

S. No.	Abbreviation	Full Name
1.	SRAM	Static Random Access Memory
2.	BL	Bit Line
3.	BLB	Bit Line Bar
4.	WL	Word Line
5	WLB	Word Line Bar
6.	SNM	Static Noise Margin
7.	HSNM	Hold Static Noise Margin
8.	RSNM	Read Static Noise Margin
9.	TG	Transmission Gate
10.	EN	Enable
11.	MOS	Metal Oxide Semiconductor
12.	IC	Integrated Circuit
13.	SA	Sense Amplifier
14.	P	Power
15.	T	Transistor
16.	ROM	Read Only Memory
17.	DRAM	Dynamic Random Access Memory
18.	SoC	System on Chip
19.	IoT	Internet of Things
20	GND	Ground

21.	CMOS	Complementary Metal Oxide Semiconductor
22.	PMOS	P-type Metal Oxide Semiconductor
23.	NMOS	N- type Metal Oxide Semiconductor
24.	WL	Word Line
25	WLB	Word Line Bar

CHAPTER 1
INTRODUCTION

SRAM (Static Random-Access Memory) cell is a fundamental building block of computer memory systems. It is a type of volatile memory that can store data as long as power is supplied to the system. The SRAM cell is known for its high speed and low power consumption, making it an essential component in various electronic devices, such as microprocessors, cache memories, and graphics cards. As the demand for faster and more efficient computing continues to rise in the future, SRAM cells are expected to play a crucial role in meeting these requirements[1]. With the increasing adoption of artificial intelligence, Internet of Things, and edge computing applications, the demand for SRAM cells is expected to grow even further, driven by the need for high-speed data processing, low-latency access, and power efficiency. Additionally, emerging technologies such as self-driving cars, smart cities, and advanced robotics will also contribute to the increased demand for SRAM cells in the future, making them a vital component in the evolving landscape of computing and information technology[2].

The chapter is divided into five sections. The first section (1.1) is about an SRAM array which is a key component of memory systems, consisting of multiple SRAM cells organized in a grid-like structure. It also contains multiple subsections describing a classical 6T SRAM cell with the hold, read, and write process explained in brief. The second section (1.2) is the motivation, which highlights this field being the area of interest for research. The third section (1.3) deals with the primary objectives of this research work. The fourth section (1.4) highlights the methodology. Lastly, the detailed organization of the thesis is presented in the fifth section (1.5).

1.1 SRAM ARRAY

An SRAM array refers to the organization and structure of static random access memory cells within a memory module or chip. The SRAM array is responsible for storing and retrieving data in a random access manner, allowing for fast read and write operations.

The basic building block of an SRAM array is a single SRAM cell, which typically consists of six transistors[1]. These transistors form a flip-flop circuit that can store one bit of data. The SRAM array is constructed by arranging multiple SRAM cells in a grid-like pattern, with rows and columns forming the addressable locations of the memory.

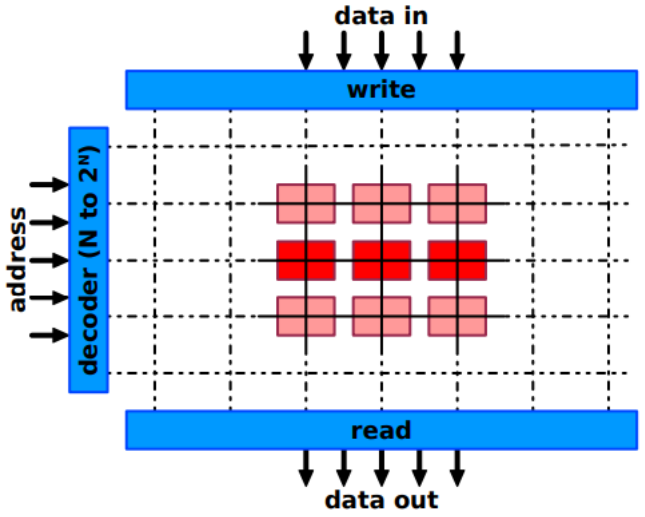


Fig. 1.1 Typical arrangement of an SRAM array, showing the periphery (in blue) and the cells (in red), with one row of cells accessed (dark red)

The size of an SRAM array is defined by the number of rows and columns of SRAM cells. Each row represents a word line, and each column represents a bit line. The intersection of a row and column represents a specific memory location, where data can be stored or retrieved.

To read data from an SRAM array, the desired address is provided, activating the corresponding word line and allowing the stored data in the selected column to be accessed and read out. Similarly, writing data involves providing the address and data to be written, and activating the appropriate word line and bit line to store the new data in the desired memory location.

The organization and design of the SRAM array play a crucial role in determining the overall capacity, speed, and power consumption of the SRAM chip. Various techniques, such as hierarchical organization, pipelining, and multiplexing, can be employed to optimize the performance of the SRAM array and meet the requirements of different applications[3].

1.1.1 Conventional Six-transistor Cell

The cell design is responsible for several vertical and horizontal control lines per cell. The most usual SRAM which consists of 6 transistors wants one horizontal line termed as word-line and one vertical line per cell named bit-line.

The conventional 6T cell is a crucial component of modern memory systems, widely used in processors, cache memories, and other digital circuits. It consists of six transistors organized in a cross-coupled latch configuration. The cross-coupled inverters form a feedback loop that allows the cell to retain its stored data without the need for constant refreshing.

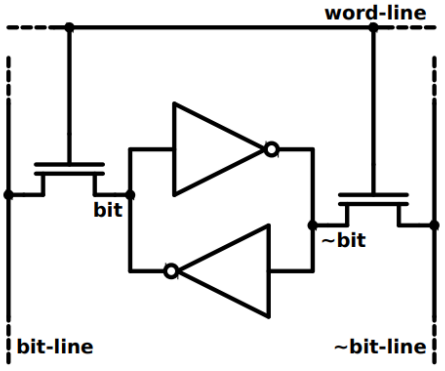


Fig. 1.2 Typical 6T SRAM cell

The 6T cells involves of two twisted inverters, the output of each inverter being coupled to the input of the supplementary one, as demonstrated in figure 1.2 . This establishes dual internal nodes of the cell, bit and bitline_bar. Every inverter is made up of one PMOS and one NMOS transistor named pull-up and pull-down transistor correspondingly. Along with the two inverters, additional two NMOS transistors called pass-gates link the interior nodes to the bit lines.

The 6T SRAM cell offers several advantages, including fast access times, low power consumption, and the ability to retain data if the power supply is maintained. However, it also has certain limitations, such as a larger area footprint compared to other memory technologies and increased vulnerability to noise and process variations. Despite these drawbacks, the conventional 6T SRAM cell remains a widely used and important component in digital systems due to its speed, reliability, and versatility.

1.1.2 Data Hold Operation

The capacity of an SRAM cell to accumulate data depends on on the two twisted inverters. If WL= 0, the pass-gates are cut and can be ignored. If there is a 1 in bit, then the upper inverter will initialize bit_bar to 0 and finally, the bottom inverter will initialise 1 in bit, emphasizing the original data, thus confirming a specified value is hold. The similar perceptive can be functional assuming that the original data kept in bit is a 0.

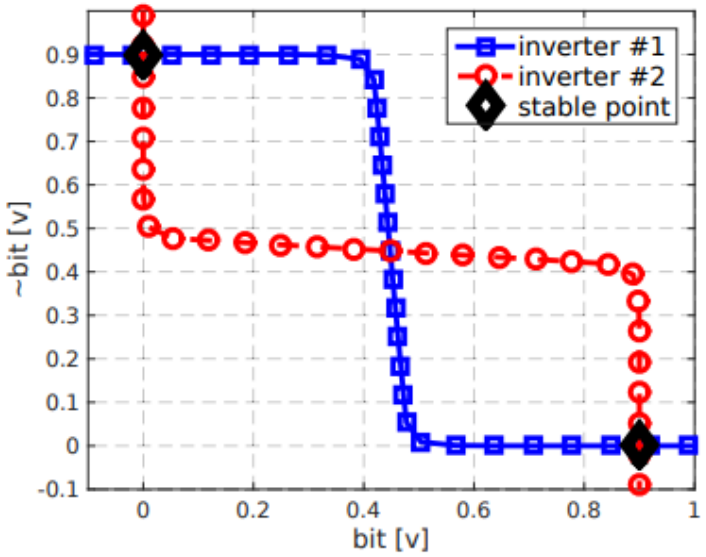


Fig. 1.3 Transfer curves of the two inverters in an SRAM cell

If the transfer curves are plotted, as seen in Figure 1.3, three intersections can be realized. The intersection in the center is not stable. The two additional points resemble the two likely values stored by the cell, either a zero or one.

The 6T cell depends on two transistor inverters to hold the data as this will produce the least area. However, the classic inverters could be substituted by supplementary designs, that will be also able to reserve two possible values. These diverse designs can be based on varying the dimensions of pull-up and pull-down transistors or dissimilar circuits including inverters with extra transistors such as Schmitt trigger, in order to boost features of the cell, like noise resilience and stability.

1.1.3 Write Operation

The two-looped inverters at the core of the cell can accumulate both probable data. The need to trigger the wanted value to behold in the cells, which is called as the write operation.

The write operation begins by setting the word line to V_{DD}, which stimulates the pass gates. In the meantime, the edge on the top of Figure 1.1 sets the bitlines to the value to be written in the interior nodes of the cell. When an inverse value is written than the one being kept, the pass gate is imposing a value while the inverter is trying to hold the opposite one. The transistors must be sized so that the pass gate surpasses the inverter in order to attain a effective write.

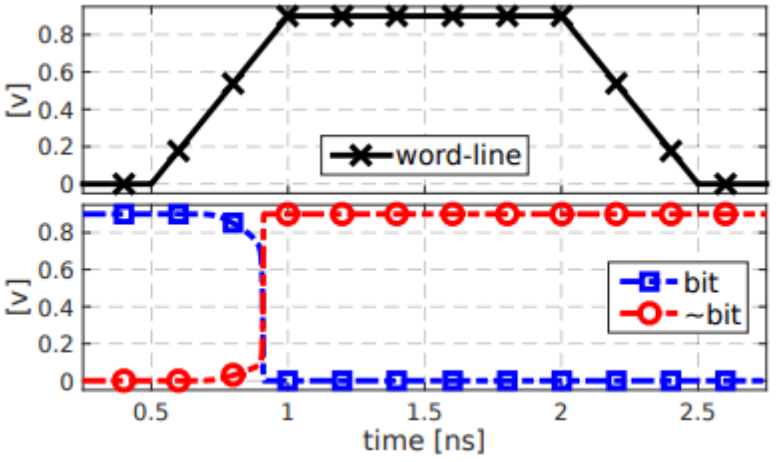
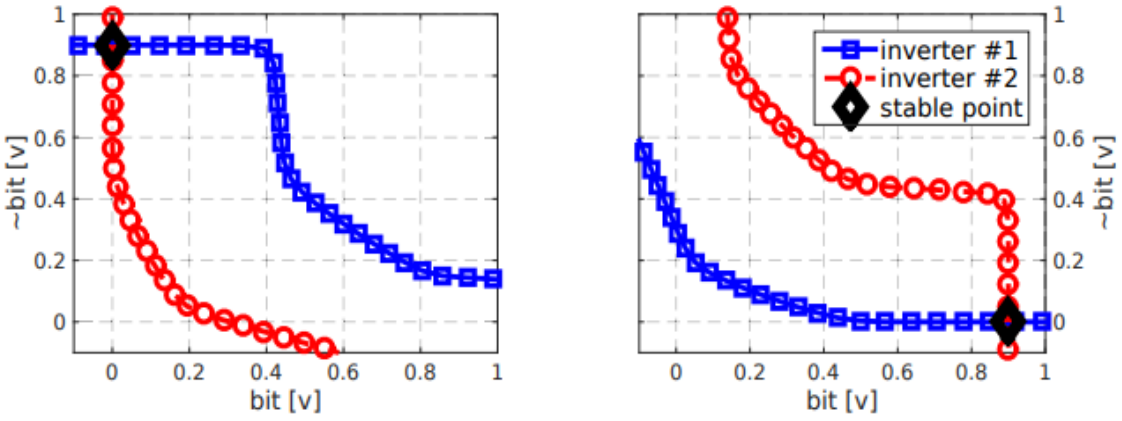


Fig. 1.4 Transient simulation of a write operation in a 6T SRAM cell



(a) (b)

Fig.1.5 Modified transfer curves of the inverter while writing (a) Write Zero (b) Write One

A transient simulation of the write operation is illustrated Figure 1.4. The cell starts holding a one, as given by the initial values of interior nodes, bit = V_{DD} and bit_bar = 0, whereas the inverse values need to be written, setting bitline = 0 and bitline_bar = $V_{DD.}$ By rising the word line from 0 to V_{DD} at t = 1 ns, the pass gates are initiated, writing the values in the bit lines to the interior nodes, swapping the voltage in bit and bit_bar. After the word lines are tied back to ground, the cell holds the new value in the internal nodes.

The activated pass gates have the effect of changing the transfer curves of the inverter to the ones shown in Figure 1.4, leaving only one stable point where the transfer curves cross. This forces the cell to keep holding the data corresponding to that of the point after the write operation is finished. The voltage in the bit lines during the write operation, determines which stable point of the cell is selected, having the bit-line tied to the ground while bitline_bar is set to V_{DD} forces a 0 as shown in figure 1.5 (a) while setting the opposite voltage forces a one as shown in Figure 1.5 (b).

1.1.4 Read Operation

Once a value is written to the cell and the cell is able to hold it, the remaining operation consists in retrieving the data stored in the cell. In addition to correctly reading the data, it's equally important to ensure the contents of the cell are not altered during the read operation.

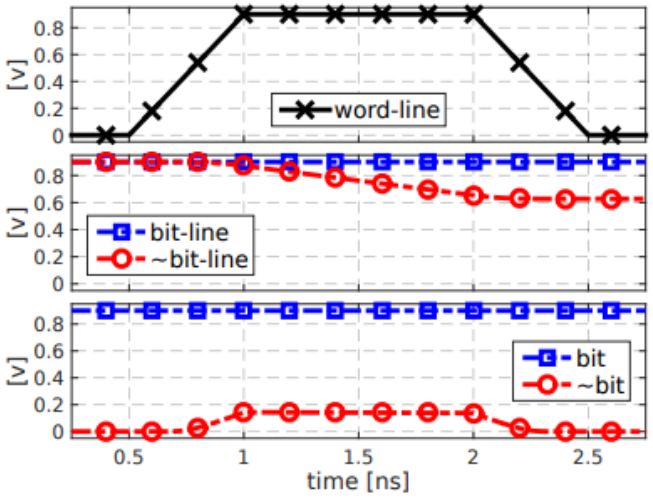


Fig.1.6 Transient Simulation of a Read Operation

In the case of a 6T cell, as for the write, the read operation is triggered by rising the voltage of the word line from ground to V_{DD} which activates the pass gates. Instead of forcing the voltages of the bit lines, those are now pre charged to V_{DD} but then left floating. The pass gate connected to the internal node set to the ground will sink current from the bit line to which is connected, progressively discharging as shown in Figure 1.6.

The voltage difference between the two bit lines is sensed by the read periphery at the bottom in the figure 1.1 amplifying the difference to retrieve the data stored in the cell. The circuit is in charge of this is called sense amplifier, it usually needs a small voltage difference between the bit lines, typically about 10% of the supply voltage.

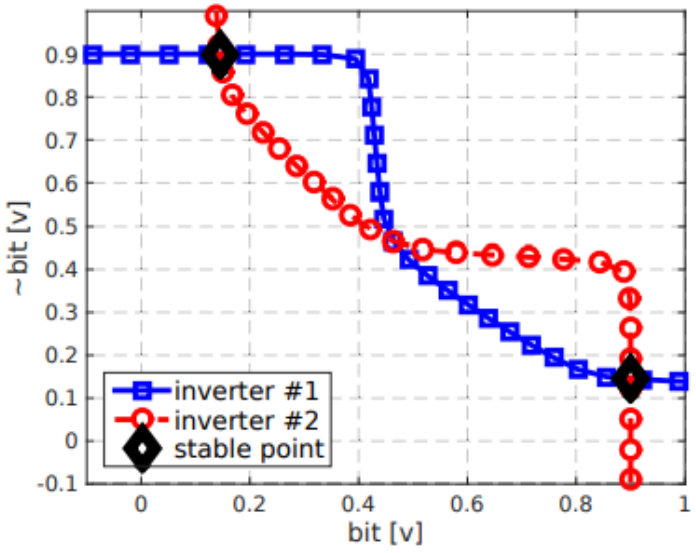


Fig.1.7 Modified transfer curves during a Read Operation

The transfer curves of the inverter are also altered during a read operation as shown in figure 1.7. The two curves cross three times with two stable points, which indicates that the contents will not be altered. However, the curves are much closer to each other compared to those in figure 1.3, which means that the stability is degraded and more vulnerable to noise, this can be seen too in figure 1.6 as the voltage of the internal nodes bit_bar is altered during the read access.

1.2 MOTIVATION

The motivation for conducting research in 10T SRAM cells stems from the ever-growing need for high-performance and low-power memory solutions in modern computing systems. As technology advances and the demand for data-intensive applications such as artificial intelligence, virtual reality, and big data analytics increases, traditional 6T SRAM cells face limitations in terms of stability, leakage current, and power consumption. The 10T SRAM cell architecture offers a promising alternative, with its additional transistors providing enhanced stability, reduced leakage, and improved read and write capabilities. By investigating and understanding the characteristics of 10T SRAM cells, we can uncover their potential advantages and limitations, paving the way for more efficient and reliable memory designs for future computing systems.

The research in 10T SRAM cells is driven by the need to address the scaling challenges faced by conventional SRAM designs. As technology nodes continue to shrink, scaling down 6T SRAM cells becomes increasingly difficult due to various physical and electrical limitations. The introduction of additional transistors in the 10T SRAM cell architecture offers opportunities for better scalability and improved performance in advanced technology nodes. Exploring the behavior of 10T SRAM cells through static and dynamic analysis, circuit simulations, and characterization enables us to assess their feasibility in future technology generations. The research on 10T SRAM cells is motivated by the desire to overcome the limitations of current memory technologies and pave the way for more advanced and reliable memory solutions in the future.

1.3 OBJECTIVE

The objective of this research is to investigate and analyze the performance characteristics of SRAM cells. SRAM cells are integral components of modern digital systems, playing a crucial role in memory storage and data retrieval. With the increasing demand for high-speed and low-power memory solutions, it is essential to explore and understand the behavior of advanced cell designs. By focusing specifically on 10T cells, this research aims to explore their advantages, limitations, and potential applications. Through rigorous experimentation and analysis, the objective is to provide valuable insights and contribute to the advancement of SRAM technology for future computing systems.

Primary objectives of this research project are as follows:

- To Compare multiple SRAM designs for the same technology nodes, power supply, and transient time. This also helped to determine the trend of SRAM being used for low-power applications.

- To understand the working of SRAM cell and which one o u t performs the others, a comparison is done between existing structures and modified SRAM cell structure. A mathematical calculation is also performed for the PDP analysis. To establish which circuit had the best performance, SRAMs are compared, and their findings are illustrated.

- To design and analyze a modified SRAM cell structure that includes a back-to-back inverter, buffer transistors, and access transistors. For optimal performance, power analysis, delay analysis, and the data stability are all performed.

The emphasis of this research is to create an up-to-date better SRAM cell structure that uses low-energy and low-power components and may be used in low-power applications. Multiple SRAM cell topologies on the same technology node, with the same aspect ratios and transient times, were compared for this. Then, for the best performance, the existing SRAM cell designs are compared to the modified design.

1.4 METHODOLOGY

Comparative performance of the three SRAM cells have been performed which comprises of a 10T SRAM cell with source biased inverter, a transmission gate based 10T SRAM cell and a 11T SRAM cell. The TG10T SRAM cell is proven to be enhanced in almost every aspect but it consumes more power. The comparison is also performed for three different 10T SRAM cells which consist of a 10T cell with source biased inverter, a TG10T cell, and a proposed TG based 10T SRAM cell. The data stability, power consumption, and read delay along with the write delay of all the SRAM cells are studied.

A modified design is implemented and analyzed with several analyses. The proposed design has 10 transistors, four PMOS and six NMOS, and is divided into pull-up transistor, pull-down transistors and access transistors. The data stability, power consumption, and read delay along with the write delay of the proposed cell is studied. This thesis focuses into the standard SRAM structures. A variety of sense amplifier

parameters have also been defined and researched. The 10T SRAM cell offers improved stability, reduced write disturbance, and better noise immunity compared to the 6T SRAM cell. However, the increased complexity and additional transistors result in a larger cell area and higher power consumption. Therefore, the choice between the 6T and 10T SRAM cell depends on the specific design requirements and trade-offs in terms of area, power, and performance.

1.5 THESIS ORGANIZATION

This thesis is divided into five chapters. An SRAM array and classical 6T cell is defined in Chapter 1 as an introduction. The motivation, objective, methodology, and thesis organization are also included in Chapter 1. The literature review and the technology gap are discussed in Chapter 2. The third chapter examines a significant comparative analysis of different 10T and 11T SRAM cell. Chapter 4 examines the design and analysis of a proposed 10T SRAM cell, as well as its parameters and performance. In Chapter 5, a comparison of the previously reported SRAM cells from Chapter 3 is done with a modified design to demonstrate its enhanced performance as compared to other cells used for comparison. The conclusion and future scope are presented in Chapter 6.

CHAPTER 1 - Provides a basic overview of SRAM array and SRAM cells which are closely interconnected in memory systems, as well as how they operate at low power and low voltage. This chapter discusses the objective, motivation, methodology, and detailed organization of the thesis.

CHAPTER 2 - The prior research on SRAM was detailed in this chapter. In the literature, every parameter is critically analyzed and summarizes existing academic literature and publications relevant to SRAM cells. The purpose of a literature review is to gain a comprehensive understanding of the current state of knowledge, identify gaps or inconsistencies in existing research, and provide a foundation for the researcher's own study.

CHAPTER 3 - This chapter covers the comparative analysis of different 10T and 11T SRAM cell as well as their functionality, operation, and parameters. They were examined at 32nm technology nodes and 0.5V supply, depending on their structures, their

parameters such as static noise margin, read/write delay, and power consumption were compared.

CHAPTER 4 - This chapter illustrates a proposed design of the 10T SRAM cell. It describes the design, and how it works. For this cell, major factors such as data stability, read/write delay, and power dissipation are determined. The Monte Carlo analysis is also performed for accessing the performance and reliability of proposed cell. All these analyses are performed to highlight the performance of the proposed cell.

CHAPTER 5 - This chapter presents a detailed comparative analysis between the proposed 10T SRAM cell and other four existing 10T and 11T SRAM cells to demonstrate the higher action of the proposed design. The comparison is done on three parameters such as static noise margins, access delays, and power consumption.

CHAPTER 6 - The dissertation is concluded with the overall conclusions and data of results drawn from the research work. It also includes future scopes of improvement related to the topic of research.

Finally, the list of publications contingent on the work carried out in this thesis isattached Later, the detailed list of references is presented which is used to refer to and site the previous research work to explore the directions for our present work.

CHAPTER 2
LITERATURE REVIEW

Reviewing the reported work is always necessary. The aim of a literature review is to:

- Establish a foundation of knowledge about the topic

- Identify areas of previous expertise to minimize repetition and to give credit to other scholars

- Recognize previous studies contradictions, research gaps, main research conflicts, and unsolved concerns

This chapter is categorized into two sections. The first section (2.1) comprehensive summary of past work, and the technical gaps are covered in section 2.2.

2.1 COMPREHENSIVE SUMMARY OF PAST WORK

- **Low leakage 10T SRAM cell with improved data stability in deep sub-micron technologies, 2021**

R. Krishna and P. Duraiswamy [1], Proposed a low leakage 10T SRAM cell with a source-biased inverter in deep sub-micron technologies. The source-biased inverter utilizes two extra transistors to alleviate the leakage power without raising the dynamic power. The extra transistors increase the source voltage decreasing the drain to source voltage. It gives limitation in leakage power consumption. Here, the assist techniques are also applied to enhance the stability.

- **Robust transmission gate-based 10T subthreshold SRAM for internet-of-things applications, 2022**

E. Abbasian and M. Gholipour [2], Presented a transmission gate based 10T SRAM cell used in IoT applications. It is compared with 6T, TG-8T, and fully differential 8T cells when subjected to extreme PVT variations. The proposed cell uses a differential scheme to amplify the sense margin. It strengthens the write-ability by utilizing two TGs instead of two NMOS access transistors. It also employs two extra buffer transistors to improve

read stability. The proposed TG10T cell minimizes leakage power dissipation by means of a greater number of PMOS devices. The proposed cell renders better overall performance compared to other SRAMs which makes it appropriate for IoT applications.

- **A reliable low standby power 10T SRAM cell with expanded static noise margins, 2022**

E. Abbasian, F. Izadinasab, and M. Gholipour [3], Proposed a reliable low standby power 10T SRAM cell with high read stability and write-ability. The proposed cell consists of a cross-coupled layout comprising of standard inverter with a stacked transistor and a Schmitt-trigger inverter with a double-length pull-up transistor. The cell eradicates the read disturbance as the read path is segregated from true internal storage nodes. The cell executes its write operation in pseudo differential form through a write bit line and control signal with a write-assist technique. The leakage power consumption shrinks in the proposed design.

- **A low power single bit-line configuration dependent 7T SRAM bit cell with process-variation-tolerant enhanced read performance, 2023**

B. Rawat and P. Mittal [4], "Proposed a 7T bit cell for 32nm technology node at 0.3V supply voltage. The enhancement in performance of the presented cell is seen when compared with the pre-existing 6T, 7T, 8T, 9T, and 10T cells. The power analysis revealed that the 7T cell has the least read/write power dissipation. The layout of the presented design also occupies the least area compared to other counterparts. The tolerant analysis also depicts that the proposed cell sustains a decent performance under PVT variations.

- **Energy-Efficient Single-Ended Read/Write 10T Near-Threshold SRAM, 2023**

E. Abbasian and S. Sofimowloodi [5], Presented an energy efficient single-ended 10T near-threshold SRAM. The proposed design enhances read stability and write-ability through the aid of built in read-assist scheme and a power-gating technique. The energy and power consumption are reduced by using single-ended read/write operation and stacking of transistors in the core of cell. The simulation results for the proposed cell shows enhancement in read stability/writability, reduction in leakage power, improvement in read/write power and energy in comparison to conventional 6T cell. The area of the proposed design was larger than the conventional 6T SRAM.

- **A Novel Low-Power and Soft Error Recovery 10T SRAM Cell, 2023**

C. Liu, H. Liu and J. Yang [6], Proposed a low power SRAM cell for soft error recovery. The proposed cell is compared to standard 6T cell which shows all the sensitive nodes can recover their data even when nodes flip at the same time. The proposed cell is free from read intervention. The presented cell consumes very low-holding power due to slight leakage current of the circuit. The problem in the presented unit is that it uses PMOS to drive '0' which causes the line voltage change to not to be in full swing. The simulation results show the proposed cell has good balance between performance, power, reliability and area and it is good choice for anti- radiation application.

- **A comprehensive analysis of different 7T SRAM topologies to design a 1R1 W bit interleaving enabled and half select the free cell for 32 nm technology node, 2022**

B. Rawat and P. Mittal [7], Presented a single-ended, dual port, 1R1W 7T SRAM cell which is designed after a detailed review of various counterparts. The static analysis discloses that the hold/read noise margins. Its performance is validated by Monte Carlo analysis and temperature variation analysis. When compared to other single-ended 5T, 6T, 7T, 8T, 9T, and 10T SRAM cells, the cell is proven to perform better. In comparison to the other cells, the ION/IOFF ratio is high since the leakage current is low.

- **Low power self-controllable voltage level and low swing logic based 11T SRAM cell for high-speed CMOS circuits, 2018**

K. Gavaskar and U.S. Ragupathy [8], Designed a lower-power 11T SRAM cell where two voltage sources are used, one is connected to bitline_bar whereas the other is connected to bit line. The dynamic power could be reduced by decreasing the swing voltage. The reduction in leakage current causes a decrease in static power dissipation. The voltage supplied is maximum to avoid the data retention difficulty to the circuit during the active mode. Also, reduced voltage is supplied during the standby mode. The simulation demonstrates SRAM cell dissipates lesser dynamic power as well as leakage current. The remarkable advancements procured in the results by the employment of SVL and low-swing logic will be applicable for future low power memory designs.

- **Single-bit line accessed high-performance ultra-low-voltage operating 7T static random-access memory cell with improved read stability, 2021**

B. Rawat and P. Mittal [9], Proposed a single-bit line 7T bit cell designed at 32nm technology node at 0.3V supply voltage. On comparing the performance of the proposed cell against different 6T, 7T, 8T, and 10T SRAM bit cells, the hold static noise margin and read static noise margin were found to be better than the 6T cell. The writability also improved decreasing the leakage current compared to the 6T cell. Hence, it can be inferred that the proposed cell manifests all essential enhancements in performance compared to the other counterparts demonstrated in the paper.

- **Low-power and high-speed SRAM cells for double-node-upset recovery, 2023**

S.Cai, Y. Wen, C. Xie, W. Wang and F Yu [10], Presented radiation-hardened SRAM (i.e., LPDNUR and HSDNUR) which can self-recover from single-node and double-node upsets. LPDNUR uses a two-input C-element structure, which reduces the average power consumption because the stacked effect. Moreover, in order to reduce read access time (RAT) and write access time (WAT), the paper proposes HSDNUR, which uses a combination of NMOS and PMOS as the transistor for one-node data transmission, an approach that increases the current drive capability and reduces transmission delays.

- **Design of highly reliable radiation hardened 10T SRAM cell for low voltage applications, 2022**

R. Shekhar and C.I. Kumar [11], Presented a novel 10T SRAM cell that has an energy-efficient operation and is radiation-hardened with high static noise margins. The proposed cell reduces area as compared to other counterparts used in the paper for comparison. The cell also enhances the hold and read static noise margin whereas the write static noise margin remains almost the same. The memory cells are more open to single event upset (SEU) because of a reduction in supply voltage, decrease in critical charge, and dense ICs.

- **A reliable and temperature variation tolerant 7T SRAM cell with single bit line configuration for low voltage application, 2022**

B. Rawat and P. Mittal [12], Proposed a 7T cell which is of single-ended configuration. The hold/read static noise margin is fairly good for this cell. The reliability of this cell can be measured using Monte Carlo process variation and temperature variation. The

results obtained for the proposed design are compared against various pre-existing 5T, 6T, 7T, and 8T cells to showcase the enhancements obtained by the proposed 7T cell. The power dissipation was found to be minimum in the proposed design as it requires a pulse width of a few nanoseconds to perform write and read operations successfully. Thus, the proposed cell shows advancement in performance when compared to its counterparts discussed in the paper.

- **Comparative analysis of 90 nm MOSFET and 18 nm FinFET based different multiplexers for low power digital circuits, 2020**

N. Kumar, P. Mittal [13], In terms of latency, average power dissipation, and Power delay product, a comparison is done between FINFET-based Gate Diffusion Input and Pass Transistor based 2:1 Multiplexers. The power dissipation of a GDI-based mux is relatively low. GDI-based Mux has superior performance and lower power consumption. Because multiplexers can be employed in a variety of combinational circuits, improving the performance of the multiplexer is increase the overall performance of the circuit.

- **Design and performance improvement of low power SRAM using deep submicron technology, 2022**

U. R. Shirode and R. D. Kanphade [14], Presented a design with performance improvement of low-power SRAM working at deep submicron technology to control the issues by employing a novel modified lector-based foot-driven stacked transistor domino logic SRAM cell design in which the modified lector technique uses both keeper and lector technique to reduce the leakage power in both modes i.e active mode and standby mode, thereby reducing layout area and the propagation delay. It is designed to improve the noise margin of SRAM and to overcome the zero output in AND gate thereby increasing the speed of the SRAM cell. The proposed cell attains a high read and write stability along with a high SRAM speed. The leakage current is reduced. Thus, the proposed design outperforms the existing method with greater stability and speed of cells.

- **Static Noise Margin Analysis of 6T SRAM Cell, 2016**

A. A. Jose and N. C. Balan [15], Presented a design with the SNM calculation and analysis of SRAM cells based on simulations performed in Cadence Virtuoso. The proposed cell has the compact structure of six transistors. The static noise margin is found with the help of butterfly curves for read, hold, and write operations.

- **Sizing-priority based low-power embedded memory for mobile video applications, 2016**

S. A. Pourbakhsh, X. Chen, D. Chen, X. Wang, N. Gong and J. Wang [16], Presented a sizing-priority based memory design methodology for low-power mobile video applications. The investigation of size-dependent memory failure characteristics was performed and memory failure rate overhead was effectively reduced with low area utilization. A model was designed between memory failure and output quality, while introducing application output into the hardware design process.

- **A single-ended low leakage and low voltage 10T SRAM cell with high yield, 2020**

N. Eslami, B. Ebrahimi, E. Shakouri and D. Najafi [17], Presented a low leakage 10T single-ended SRAM cell in the sub-threshold region using FINFET technology that enhances the hold, read, and write stability. At low voltage the write-ability is raised by temporarily floating the data node, and the stability of the read operation is maintained approximately equal to the hold state by separating the data storage node from the read bit line (RBL) while using only a single transistor. The read stability is found to be higher than conventional 6T cell. Also, the proposed cell has the lowest static power dissipation.

- **A 32 nm read disturb-free 11T SRAM cell with improved write ability, 2020**

S. R. Mansore, R. S. Gamad and D. K. Mishra [18], Presented 11T SRAM cell with single read and differential write which has improved write-ability by interrupting its ground connection during a write operation. There is a separate read buffer that provides disturb-free read operation. The simulation results show that the proposed cell achieves a higher read static noise margin as compared to conventional 6T cell and PNN based 10T cell. The write static noise margin of the proposed design was found to be higher than 6T cell. The Proposed design consumes lesser read power as compared to PPN10T cell. Also, the leakage power is lesser. The Proposed 11T cell occupies larger area as compared to that of conventional 6T.

- **Low power SRAM design with reduced read/write time, 2013**

S. Yadav, N. Malik, A. Gupta, S. Rajput [19], Presented the design and analysis of Static Random-Access Memories (SRAMs), with a focus on minimizing delay and power consumption. Also, implemented the 6T SRAM cell which has a Read and write time, power consumption and delay have all been lowered. Bit-line parasitic capacitance

increases as memory capacity grows, delaying voltage sensing. To prevent this problem, apply efficient scaling approaches and further improve design performance.

- **Design and analysis of a 32 nm PVT tolerant CMOS SRAM cell for low leakage and high stability, 2010**

S. Lin, K. Yong-Bin and F. Lombardi [22] proposed a 9T SRAM cell that is primarily aimed at providing a robust and process-voltage-temperature variation tolerant cell with minimum leakage power consumption. The cell is also designed in such a way that the data stored on the cell is protected by high stability. The simulation findings validated that the tolerance and robustness. The results also revealed that the reported SRAM design consumes 33% lesser leakage power. It also showed that the delay being exhibited by the reported SRAM is on the lower side.

Table 2.1: Parametric Analysis of various 9T and 11T SRAM cells

S. No.	Authors	Tr. Count	No. of Bitlines	Technology node (nm)	Supply Voltage (V)	Access Delay (psec)	Leakage power (nW)	SNM in mV (RSNM/HSNM/WM)
1.	Lin *et al.* [5]	9	2	32	0.6	82.04	-	-
2.	Gavaskar *et al*. [10]	11	2	30	0.8	21.3	7.15	-
3.	Mansore *et al.* [21]	11	2	32	0.4	723.9	8.27	-/113/254.5
4.	Oh *et al.* [34]	9	1	22 (FinFET)	0.32	256000	740	164/-/-
5.	Lorenzo *et al*. [38]	11	1	65	1.2	778.3	46.42	179/179/331

The table 2.1 titled Parametric review of various 9T and 11T SRAM cells presents a summary of relevant studies investigating 9T and 11T SRAM cells that are either single ended or differential ended. These results align with previous research in the field, supporting the theory. The table underscores the importance of SRAM cells in the field of electronics and provides valuable insights for future studies.

Table 2.2: Parametric Analysis of various 10T differential ended SRAM cells

S. No.	Authors	Technology node (nm)	Supply Voltage (V)	Access Delay (psec)	Leakage power (nW)	SNM in mV (RSNM/HSNM/WM)
1.	Krishna *et al.* [1]	32	1	916.7	0.00937	201/-/463
2.	Abbasian *et al.* [2]	16	0.36	340	1.15	29.8/87.3/
3.	Abbasian *et al.* [3]	16	0.7	299	11.79	225.5/225.5/356.6
4.	Abbasian *et al.* [5]	32	0.6	414	4.90	197/209/263
5.	Liu *et al*. [6]	22	0.8	17.9	2.92	340/510/270
6.	Shekhar *et al*. [17]	65	0.4	278	3.38	117/57/220
7.	Eslami *et al*. [20]	10 (FINFET)	0.2	150	2	63.5/63.5/107.8

The table 2.2 titled Parametric review of various 10T differential ended SRAM cells presents a summary of relevant studies investigating 10T SRAM cells that are differential ended. These results align with previous research in the field, supporting the theory. The table underscores the importance of SRAM cells in the field of electronics and provides valuable insights for future studies.

2.2 RESEARCH GAP

The 10T SRAM cells have gained attention as a promising alternative to conventional 6T SRAM cells due to their improved read stability and write ability but several research gaps still exist in this area. One significant research gap pertains to the area of write stability. While 10T SRAM cells offer improved read stability compared to conventional 6T SRAM cells, challenges remain in achieving robust write stability. The write operation in 10T SRAM cells is more susceptible to various noise sources. Exploring innovative techniques to enhance the write stability of 10T SRAM cells, while maintaining their improved read stability, is an active area of research. Addressing this research gap will not only improve the overall reliability of 10T SRAM cells but also facilitate their integration into high-performance memory subsystems.

A notable research gap in the 10T SRAM cells is the exploration of power-efficient design methodologies. While 10T SRAM cells exhibit desirable read stability characteristics, they often consume more power compared to traditional 6T SRAM cells due to the additional transistors and complex circuitry involved. Developing power-efficient design techniques specific to 10T SRAM cells is crucial for enabling their wider adoption in low-power and energy-constrained applications, such as mobile devices and Internet of Things (IoT) devices. Exploring new circuit architectures, voltage scaling techniques, and power management strategies tailored for 10T SRAM cells can help mitigate their power consumption while maintaining their performance and reliability. Bridging this research gap will unlock the full potential of 10T SRAM cells in power-sensitive applications, furthering the advancement of energy-efficient memory technologies.

CHAPTER 3
CHARACTERISTIC COMPARISON FOR DIFFERENT 10T AND 11T SRAM CELLS

The specific performance and characteristics of SRAM cells can vary depending on the implementation, process technology, and design considerations. These comparisons provide a general understanding of the differences between the 10T and 11T SRAM cells. The additional transistor in the 11T cell is usually used as an access transistor to improve read and write stability. The 11T SRAM cell offers better stability compared to the 10T SRAM cell. The additional access transistor in the 11T cell helps reduce the leakage current and improves the robustness of the stored data. The 10T SRAM cell typically exhibits faster read access times compared to the 11T SRAM cell.

The additional transistor in the 11T cell introduces additional capacitance, which can slightly slow down the read operation. Both the 10T and 11T SRAM cells provide similar write performance. However, the 11T SRAM cell may have a slight advantage due to improved stability, resulting in better write margin and reduced write-induced disturbances. The 10T SRAM cell generally consumes less power compared to the 11T SRAM cell. The additional transistor in the 11T cell increases the static power dissipation, contributing to higher overall power consumption. The 10T SRAM cell is more area-efficient than the 11T SRAM cell due to its simpler structure and fewer transistors.

The chapter is divided into seven sections. The first section (3.1) elaborates overview of SRAM cells in which conventional 10T cell, TG 10T cell, and 11T cell are discussed. The second section (3.2) mentions the dimension of all four cells, which highlights the technology node being used and the varying dimensions of pull-down, pull-up, and access transistors. The third section (3.3) deals with transient analysis to evaluate the behavior of SRAM cells during dynamic operations such as read and write operations. The fourth section (3.4) features data stability in which the butterfly curves HSNM, RSNM, and WSNM have been shown to evaluate robustness against noise and ensure reliable operation. The fifth section (3.5) shows the power comparison for each cell. The sixth section (3.6) demonstrates the comparison between the read and write delay respectively.

3.1 OVERVIEW OF SRAM CELLS

SRAM cells are a type of semiconductor memory used in computer systems, microprocessors, and other digital devices. Unlike dynamic RAM (DRAM), which requires periodic refreshing, SRAM is designed to retain data as long as power is supplied to the circuit. SRAM is known for its fast access times, low power consumption, and non-volatility.

An SRAM cell typically consists of transistors arranged in a flip-flop configuration. A brief overview of the components and operation of an SRAM cell are illustrated below:

a) Cross-Coupled Inverter Pair: The heart of an SRAM cell is a pair of cross-coupled inverters, which form a flip-flop. Each inverter consists of a PMOS (P-channel Metal-Oxide-Semiconductor) transistor and an NMOS (N-channel Metal-Oxide-Semiconductor) transistor.

b) Bitlines: The flip-flop is connected to two bitlines, namely a "bitline" and a "bitline bar" (complementary bitline). These lines are used to read and write data to the SRAM cell.

c) Wordlines: A wordline is used to control the access to the SRAM cell. When the wordline is activated, it enables the transfer of data between the bitlines and the flip-flop.

d) Access Transistors: Access transistors are fundamental components of SRAM, which are widely used for high-speed, volatile data storage in electronic devices. The access transistors act as switches that control the connection between the storage nodes and the storage capacitors. These transistors provide the means to read/write data in the cell. During a read operation, the access transistors connect the stored data to the bitlines, allowing the voltage levels to be sensed and retrieved. During a write operation, the access transistors enable the data to be written onto the storage capacitors by providing a path for the current flow. Access transistors in SRAM are designed to have fast switching characteristics and low leakage currents, ensuring reliable and efficient access to stored data.

SRAM cells are typically organized into arrays, forming larger memory banks with multiple cells. The size of an SRAM cell can vary depending on the technology node and design constraints. Smaller cell sizes enable higher memory density but may introduce challenges in terms of power consumption and stability. SRAM cells offer fast and efficient random access to data, making them suitable for cache memory, register files, and other applications where speed and low power consumption are crucial.

3.1.1 10T SRAM Cell with Source Biased Inverter

An SRAM cell is a circuit component capable of storing a single data bit which may either be 0 or 1. Also, it must be capable to read or write data, while there is a power supply. The 10T cell with a source-biased inverter, which consists of 10 transistors, will be utilized as a baseline for comparison with the other two models. A back-to-back CMOS inverter is used for storing data, and two access transistors are placed on either side of the inverter to facilitate reading from and writing to the cell [1]. Figure 3.1 illustrates the circuit.

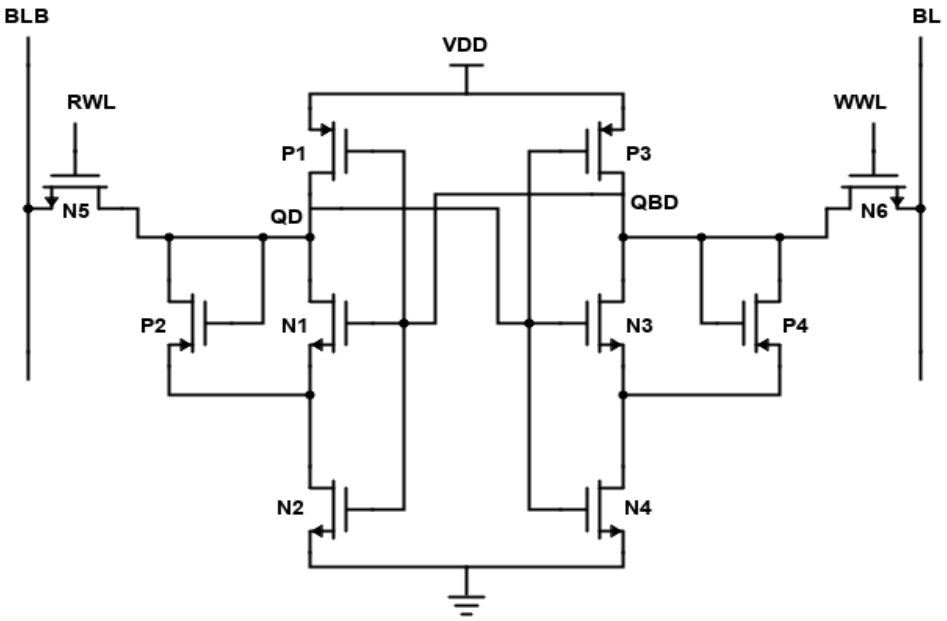


Fig. 3.1 Schematic of 10T SRAM cell with source biased inverter

Even before turning on access transistors N5 & N6, the word line is triggered to '1'. The bit line is set the same as the data bit. The bitline_bar is set the same as the complement of the data bit. This pulls data onto the two different nodes of in cross-coupled inverter.

Here, by utilizing a precharge circuit BL & BLB are pre-charged ‘1’ to successfully read data from the SRAM cell [1]. Following this operation, for turning on access transistors N5 & N6, the word line is triggered to 1 according to the data on the nodes, so that either the BL or BLB is discharged to the GND. During hold mode, WWL and RWL are grounded to turn the access transistor OFF. Hence, the core of this cell is separated from bit lines. So, no read or write operation is performed.

3.1.2 Transmission Gate based 10T SRAM Cell

Figure 3.2 displays a TG10T SRAM Cell. The right inverter, which consists of M1 & M2, is constricted by QB, while the left inverter, which consists of M3 & M4, is by Q. Both Q and QB are storage nodes. A latch is created by the back to back inverters for holding data gathered in the cell. In addition, the TG10T cell consists of 2 transmission gates, TG 1 (MN1-MP1) and TG 2 (MN2-MP2), controlled by both word lines to the write capability [2]. The Read stability is improved by two buffer transistors, M6 & M5, which are gated by Q & QB [2]. The MS transistor which is driven by the Word line connects the source of the above transistor to GND. The nodes Q=0 and QB=1.

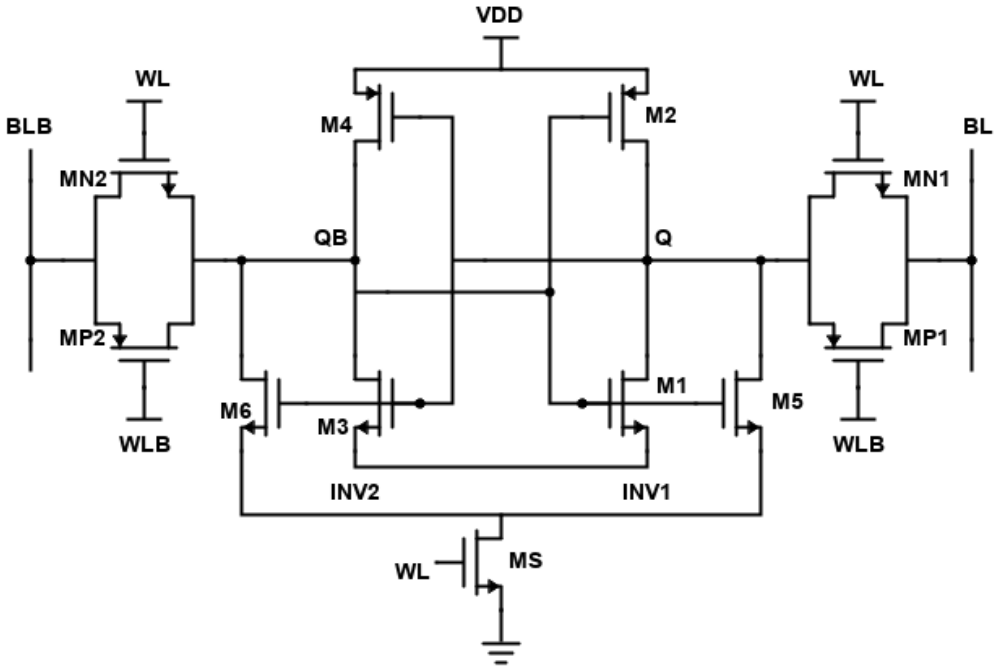


Fig. 3.2 Schematic of TG10T SRAM cell

When WL is 1 and WLB is 0, the bit lines can be accessed by switching the transmission gates. The MS transistor is also ON. Here, BL is at V_{DD} and BLB at GND, which writes

a '0'/'1' to QB/Q. The write operation is quicker because both strong logic "0" and strong "1" values are passed through the transmission gates. Through M1 & M5, node Q discharges whereas MS is initially brought to GND for a small duration of time. During this process, QB discharges via M3 & M6, where MS is ‘0’. The required data is thus successfully written to the storage nodes.

The BLB along with BL is precharged high before the read operation. Next, WLB is set to GND and WL is set to V_{DD}. This turns on the MS and transmission gates and discharges either of the bit lines to the ground. The other bit line remains at a precharged value of ‘1’ initially in storage nodes QB and Q depending on the data stored [1]. Consider that node QB stores '1' and node Q stores '0'. The additional pull-down path makes the read operation faster, thus improving the RSNM, which helps discharge the voltage at the Q node [2]. During hold mode, WLB is V_{DD} and WL is GND for turning off the transistor MS and transmission gates. Thus, cell core is disconnected from the bit lines, and no reading or writing takes place.

3.1.3 Fully Differential 11T SRAM Cell

The 11T cell demonstrated in figure 3.3 is made up of the smallest-sized devices for reducing area overhead up to a maximum extent. Here, the read buffer of the cell (MN7-MN9) consists of oversized transistors to achieve minimum read latency as well as maximum stability in the read operation. are driven by bit lines. The bit lines drive the gate electrodes of transistors MN 5 & MN 6 which are serially connected [8]. The node X1 is high during the write operation. If 1 is to be written at QB, BLB is high and BL is GND. The transistor MN 5 turns OFF. So, the pull-down path of the left inverter is disconnected and node QB attains a higher value due to quick charging.

For a stack of two devices, if the bottom device is OFF and the top device is ON, a voltage is built at the internal node. Hence, node X1 is raised. The VX1 (positive) offers body effect and stacking which helps in diminishing the delay of the write signal during a write operation on rapidly charging node QB. The write operation mainly consists of a write driver, pull-up devices, and access devices while RWL is deactivated and WWL is activated [8]. Furthermore, BL turns OFF transistor MN 5 disconnecting the pull-down path while 1 is written at QB. This improves the write-ability of the cell by making the

write operation faster.

Before the read operation, bit lines are precharged, transistor MN 1 is ON, QB stores a 0 and Q stores a 1. The bitline_bar drops through transistor MN 1 and MN 3, when WL is activated. Before the read operation, QB and Q are separated by disconnecting WWL, 0 in QB turns transistor MN 7 OFF, and 1 in Q turns transistor MN8 ON, which increases the internal node voltage X3 to a value larger than 0. When the word line for read is activated node X3 offers a body effect to transistor MN 8 [8].

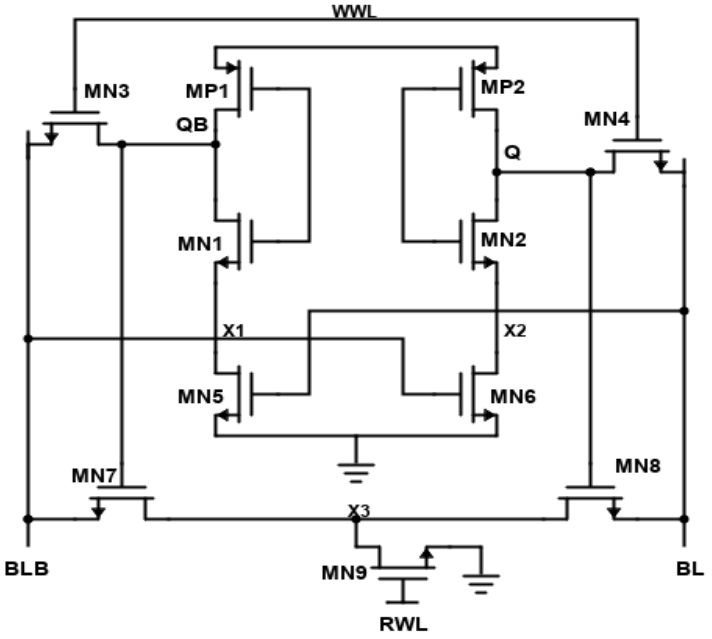


Fig. 3.3 Schematic of Fully differential 11T SRAM cell

Due to positive VX3, the body-to-source voltage of transistor MN 8 becomes negative. This results in an increase in V_{th} of MN 8 which causes the drive strength to decrease. So, the time taken to discharge BL is more. Hence, the body effect offered to transistor MN 3 is much smaller comparably. During hold mode, RWL and WWL are grounded to switch OFF the access transistor. Hence, the core of the cell is deactivated from bit lines, and no read or write operation occurs.

3.1.4 PPNN 11T SRAM cell

The schematic of the proposed cell is shown in Fig. 3.4. It comprises two cross-coupled inverters (M1–M2–M3–M10 and M4–M5–M6–M11) to store one-bit data. Transistor M7 connects true

storage node Q and bit line BL when write word line WWL is asserted. Transistor M8 connects pseudo storage node pQB and bit line BLB when word line WL (row based) is enabled. Transistors M8 and M9 form a read buffer which discharges BLB when WL is high and virtual ground VGND (row based) is low. Note that, transistor M8 is kept ON during read as well as during write operations. Transistor M10 (M11) is controlled by BL (BLB) to disconnect storage node QB (Q) from ground terminal during write “0" (write “1").

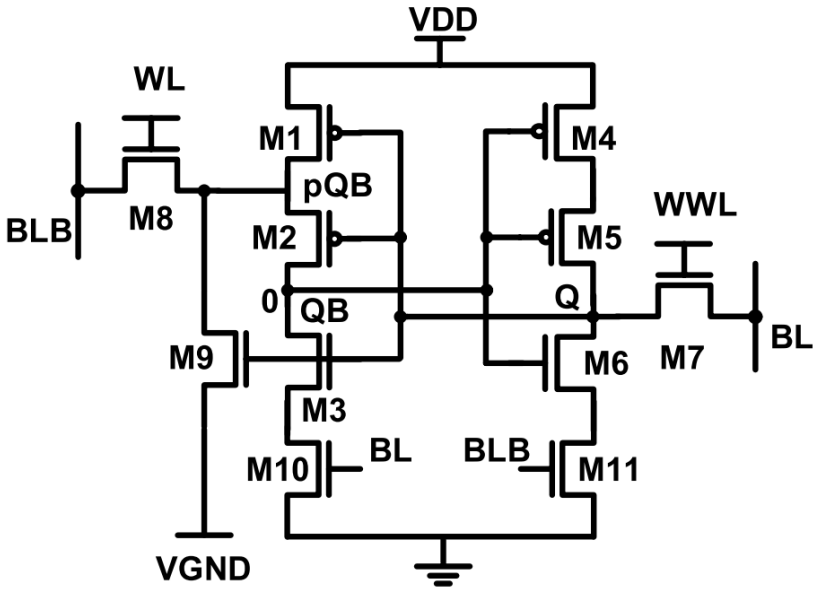


Fig. 3.4 Schematic of PPNN 11T SRAM cell

In the hold mode, WL and WWL are disabled while BL, BLB and VGND are forced to V_{DD}. Data are held by the cross-coupled inverters and is decoupled from BL/BLB [18].

For reading the cell content, bit line BLB must be pre-charged to V_{DD}, WL is set high whereas WWL and VGND are kept low. As a result, BLB is discharged through M8 and M9 or remains at pre-charged value V_{DD} depending upon the data stored. For example, if a logic “1" is stored in the cell (Q = “1"), then BLB is discharged through M8 and M9 as shown in Fig. 3.4. However, BLB remains at a pre-charged level if a logic “0" (Q = “0") is stored in the cell.

For writing the data into the cell, WWL and WL are enabled while VGND is kept floating. Suppose that initially logic “1" is stored in the cell. Now, to write a “0” in the cell, bit lines BL and BLB are loaded with “0” and “1”, respectively. As a result, node Q is discharged by BL through ON transistor M7. During the write “0” operation, OFF transistor M10 (BL = “0”) leaves node QB isolated from the ground terminal resulting in

a faster charge accumulation process at node QB. As a result, internal feedback eliminates charges rapidly from node Q and write “0” operation (Q = “0” and QB= “1”) is performed. To understand the write “1” operation, let us assume that initially logic “0” (Q = “0”) is stored in the cell. Now, to write a “1” in the cell, bit lines BL and BLB are loaded with “1” and “0”, respectively, as shown in Fig. 3.4. This causes node QB is discharged by BL through ON transistors M2 and M8. During write “1” operation, OFF transistor M11 (BL B= “0”) leaves node Q isolated from the ground terminal resulting in a faster charge accumulation process at node Q. Consequently, successful write “1” operation (Q = “1” and QB = “0”) is performed

3.2 CELL SIZING

The LTSPICE tool was used to perform simulations by constructing schematics of all three SRAM cells for comparison. Tables show the transistor sizes used in the 10T SRAM cell, TG10T SRAM cell, and 11T SRAM cell.

Table 3.1 Dimensions for 10T cell

	Width (W)	Length (L)
P1, P3 (Pull-Up Transistors)	36n	32n
N1, N2, N3, N4 (Pull-Down Transistors)	72n	32n
N5, N6 (Access Transistors)	36n	32n
P2, P4 (Buffer Transistors)	72n	32n

Table 3.2 Dimensions for TG10T cell

	Width (W)	Length (L)
M2, M4(Pull-Up Transistors)	128n	32n
M1, M3 (Pull-Down Transistors)	128n	32n
MN1-MP1, MN2-MP2 (Access Transistors)	36n	32n
M5, M6 (Buffer Transistors)	320n	32n

The dimensions of an SRAM cell are critical in determining its overall performance, density, and power consumption. The size of an SRAM cell is typically measured in terms of its area, which is determined by the dimensions of the transistors and the storage capacitors within the cell. Shrinking the dimensions of the transistors, such as the gate length and width, allows for higher cell density and increased memory capacity. Since every other transistor is the smallest size feasible, the overall area of the circuit is significantly smaller.

Table 3.3 Dimensions for 11T cell

	Width (W)	Length (L)
MP1, MP2 (Pull-Up Transistors)	32n	32n
MN1, MN2, MN5, MN6 (Pull-Down Transistors)	32n	32n
MN3, MN4 (Access Transistors)	32n	32n
MN7, MN8 (Buffer Transistors)	50n	32n
MN9 (Buffer Transistor)	64n	32n

Table 3.4 Dimensions for PPNN 11T cell

	Width (W)	Length (L)
M1, M2, M4, M5 (Pull-Up Transistors)	32n	32n
M3, M6, M10, M11 (Pull-Down Transistors)	64n	32n
M7, M8 (Access Transistors)	64n	32n
M9 (Buffer Transistor)	64n	32n

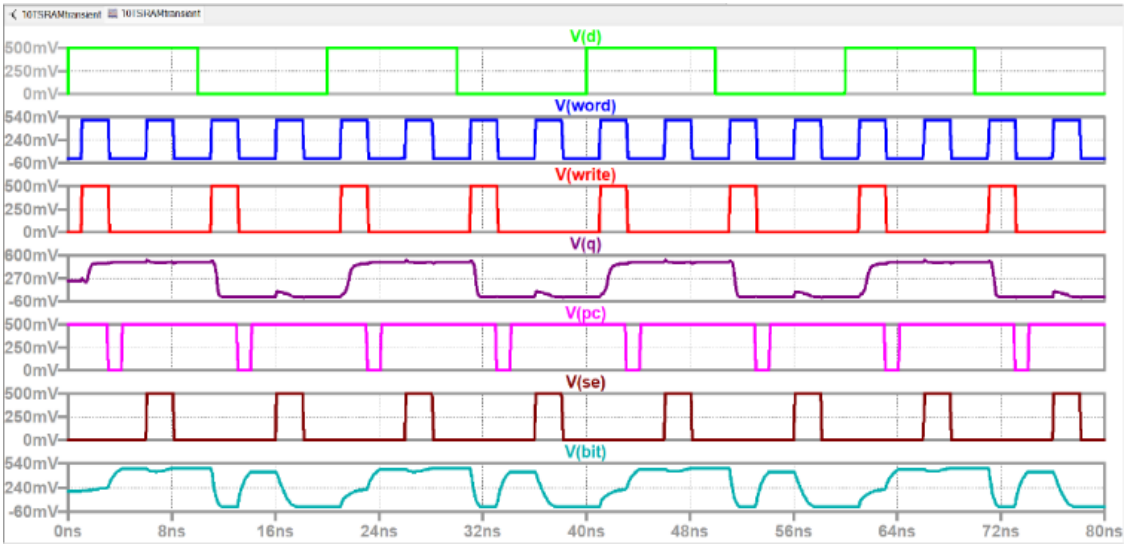
However, reducing the dimensions also brings challenges, such as increased leakage currents and reduced noise margins. Therefore, there is a constant trade-off between cell size, performance, and reliability. Advancements in semiconductor manufacturing

processes have enabled the scaling of SRAM cells, leading to smaller dimensions and higher integration levels, contributing to the continuous improvement of memory capacity and speed in modern electronic devices.

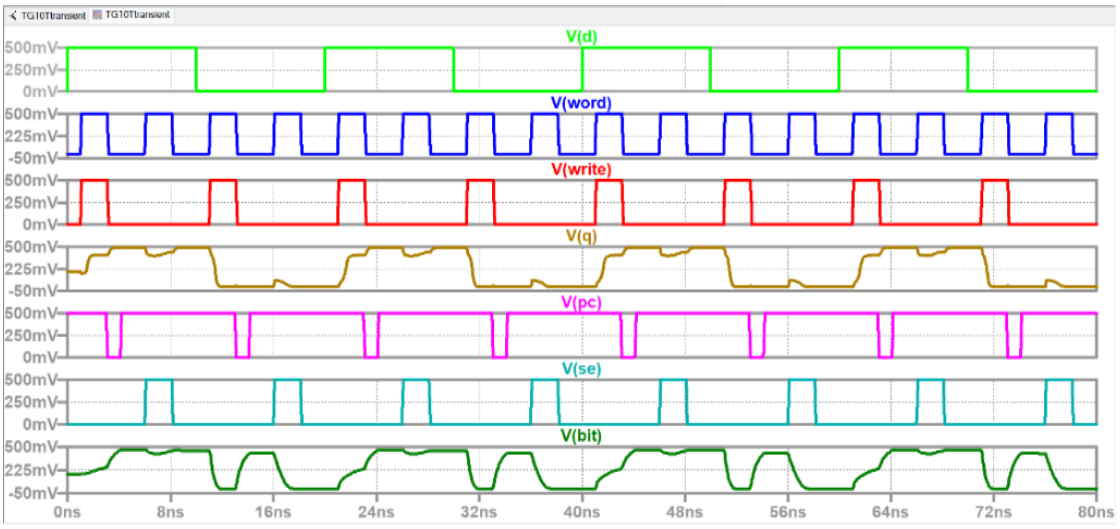
3.3 TRANSIENT ANALYSIS

To ensure that the hold, read and write operations worked correctly, transient analysis was performed on all three models. Similar read/write signals, identical input data signals, and precharge signals for read and write bit lines were employed to simulate the models. For all models, identical sense amplifiers, precharge circuits and write drivers were adopted to ensure the reliability of performance comparison. The results of the simulation are demonstrated in Fig 3.5.

Transient analysis of an SRAM cell is a crucial step in understanding its dynamic behavior during read and write operations. During a read operation, the transient analysis focuses on the voltage and current responses of the cell as the stored data is accessed. The analysis considers factors such as the access transistor's switching characteristics, the voltage levels applied to the bitlines, and the capacitance of the storage nodes. By analyzing the transient response, it is possible to determine the read access time, which is the time taken for the stored data to stabilize on the bitlines and be correctly sensed.



(a)



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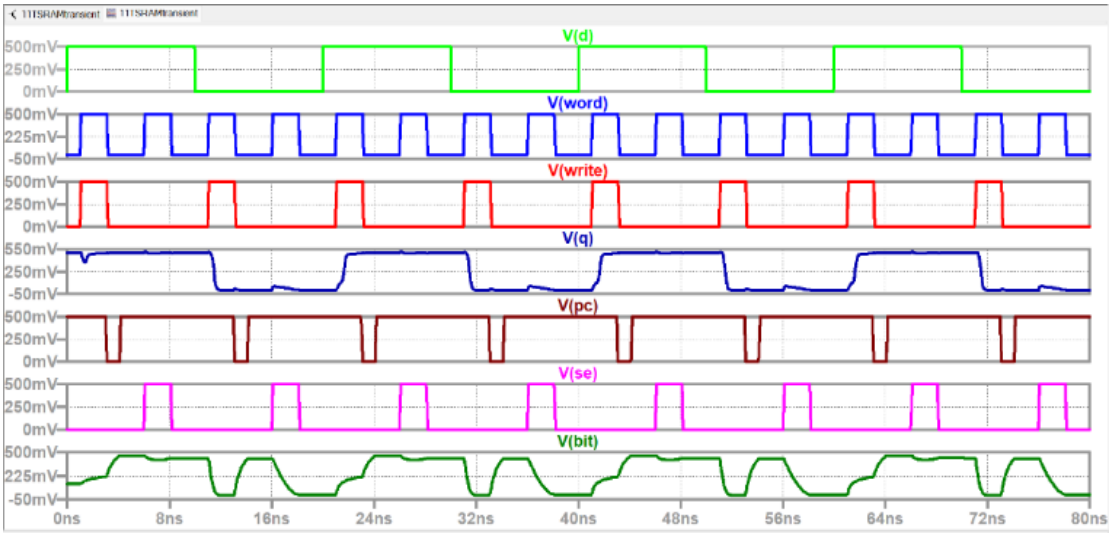

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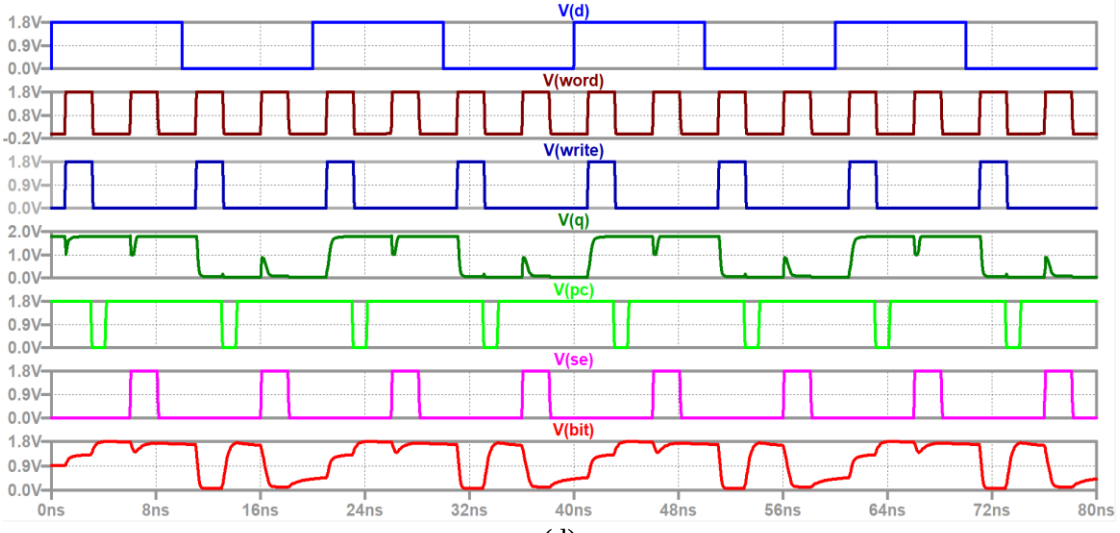

(d)

Fig. 3.5 Transient analysis of (a) 10T SRAM cell, (b) TG10T SRAM cell, (c) 11T SRAM cell, and (d) PPNN11T Cell

According to the outcomes of the transient analysis, hold, read, and write operations are performed satisfactorily in all three models. Here, it is observed when both word and write are high, it writes onto the cell i.e., whatever data is there in D is transferred to Q. When both Word and SE are high, it reads from the cell. So, whatever data is there in Q is reflected in the bit line.

In a write operation, transient analysis examines the behavior of the SRAM cell as new data is written into it. It considers the voltage levels applied to the bitlines, the access transistor's switching behavior, and the charging or discharging of the storage capacitors. Transient analysis helps evaluate parameters such as the write access time, which is the time required for the cell to stabilize and store the new data accurately. Additionally, it provides insights into potential issues such as write disturbances, which can occur due to the coupling between adjacent memory cells during the write process.

3.4 DATA STABILITY

The Static Noise Margin is calculated for all three operating modes. It is used to evaluate the SRAM cell’s data stability during the operations like hold, read, and write. SNM, which is pertinent to all three operating modes, is defined as noise that applies to storage nodes before the stored state gets reversed. The specifics of measuring SNM using butterfly curves are described in this study.

3.4.1 Hold static noise margin (HSNM)

It is a critical parameter in the design and characterization of Static Random Access Memory (SRAM) cells. It represents the voltage margin between the data state and the noise threshold, ensuring reliable data retention during the hold phase. HSNM is measured by applying a small perturbation voltage to the bitlines and monitoring the stability of the stored data.

A higher HSNM value indicates better immunity to noise-induced disturbances, minimizing the risk of data corruption. HSNM is influenced by various factors, including transistor characteristics, circuit design, process variations, and noise sources. Designers strive to maximize the HSNM by optimizing transistor sizing, voltage levels, and noise

mitigation techniques to ensure robust and reliable operation of SRAM cells in the presence of noise sources.

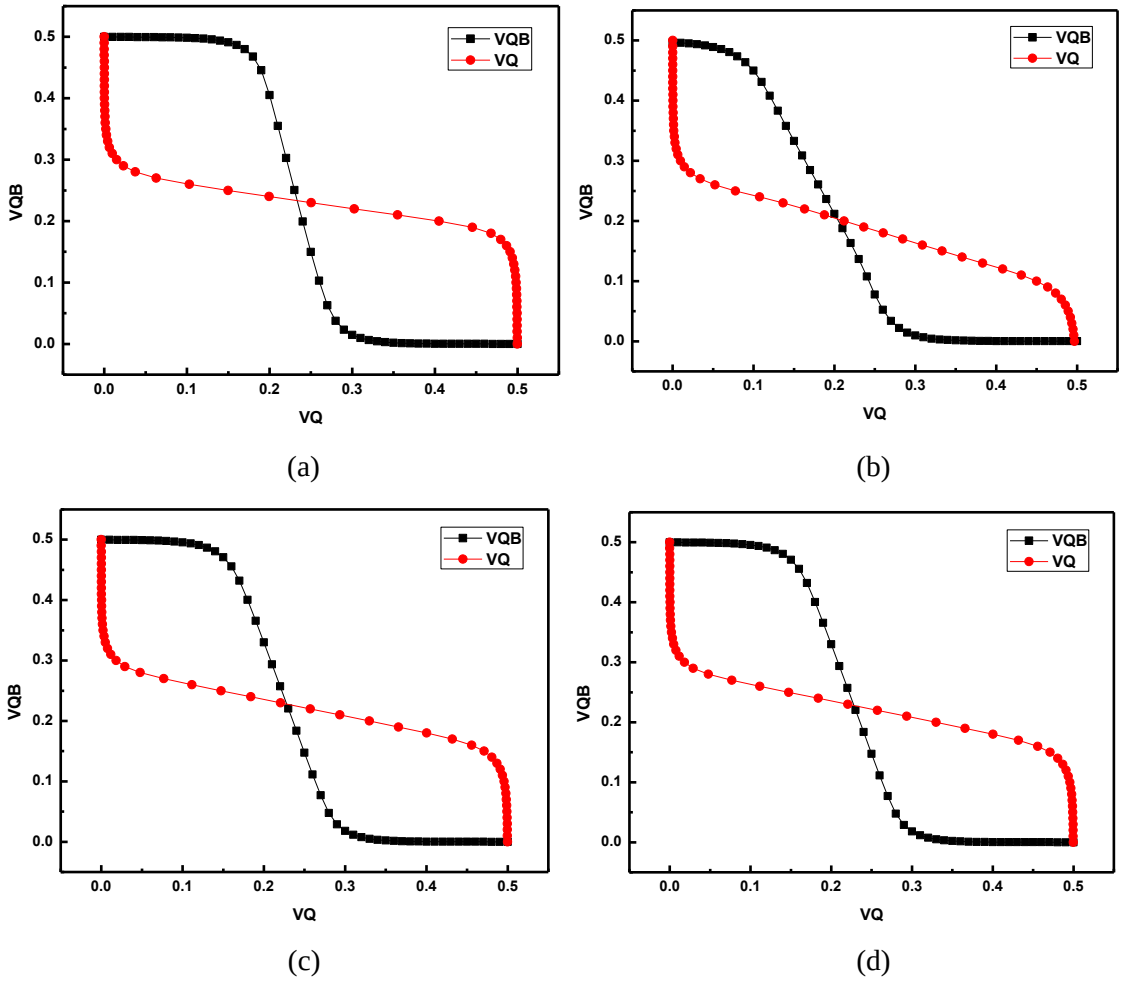

Fig. 3.6 Butterfly curves for HSNM (a) 10T SRAM, (b) TG10T SRAM, (c)11T SRAM, and (d) PPNN11T Cell

To measure the HSNM (Hold Static Noise Margin) value from butterfly curves, the following steps can be followed. First, plot the butterfly curve by varying the bitline voltage (VBL) and observing the corresponding wordline voltage (VWL) at which the stored data remains stable. The noise thresholds are determined by identifying the voltage levels where noise-induced disturbances can cause data flipping.

The voltage difference between the stable regions (where the curve intersects with stable data states) is measured and the noise thresholds is used obtain the HSNM value. It is important to repeat these measurements under various conditions to assess the robustness of the HSNM across different scenarios. The HSNM value obtained from butterfly curves

provides valuable insights into the noise immunity and reliability of the SRAM cell during the hold phase.

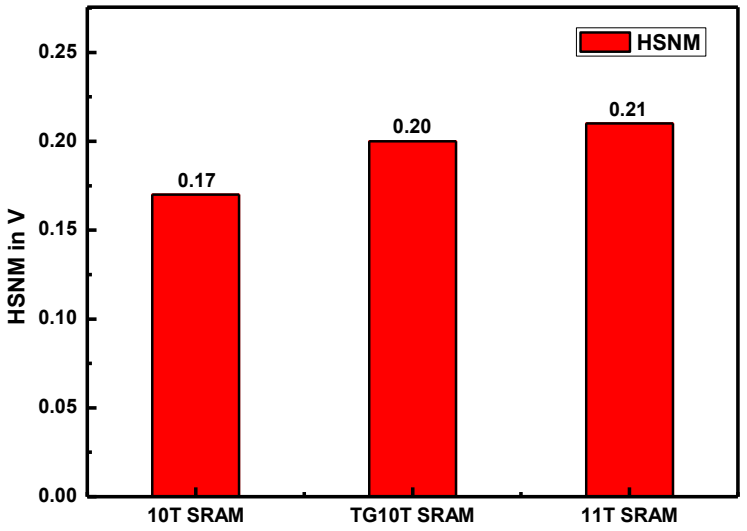

Fig. 3.7 Comparison of HSNM for various SRAM cells

The HSNM comparison between the different 10T and 11T cells as sown in figure 3.7 illustrates that the hold static noise margin for 11T SRAM is found to be maximum (i.e., 0.21 V) whereas it is found to be least in conventional 10T SRAM (i.e., 0.17 V).

3.4.2 Read static noise margin (RSNM)

It is a crucial metric for evaluating the robustness of an SRAM cell during the read operation. It represents the voltage margin between the logical high and low states of the stored data, ensuring accurate and reliable data sensing. RSNM is measured by applying a small perturbation voltage to the bit lines and observing the ability of the sense amplifiers to differentiate between the data states.

A higher RSNM value indicates better noise immunity and a larger voltage range over which the data can be accurately sensed. Achieving a high RSNM requires careful optimization of circuit design, transistor sizing, and sense amplifier characteristics to minimize the impact of noise sources and ensure accurate and reliable data retrieval from the SRAM cell.

Measuring the RSNM (Read Static Noise Margin) value from butterfly curves involves the following steps. First, plot the butterfly curve by varying the bitline voltage (VBL)

and observing the corresponding wordline voltage (VWL) at which the sense amplifiers accurately differentiate between the logical high and low states of the stored data.

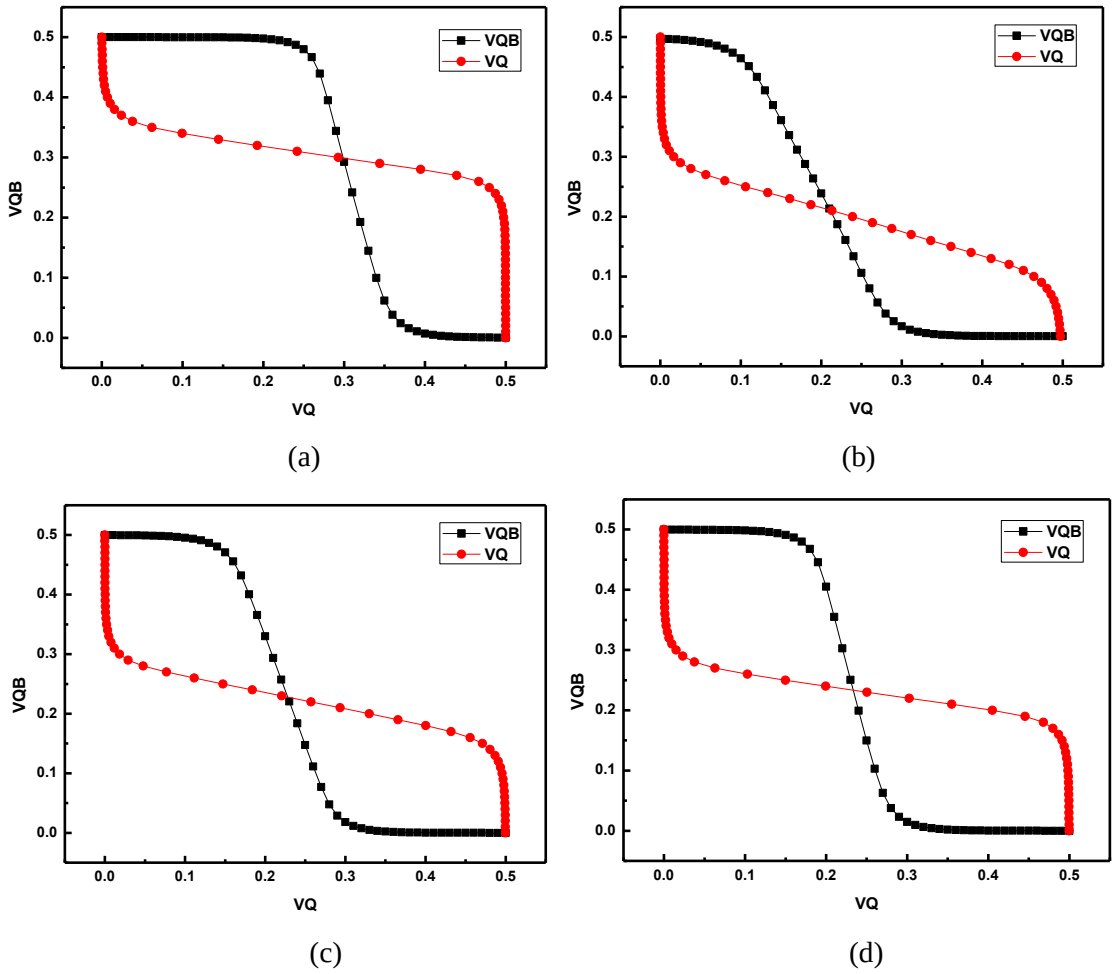

Fig. 3.8 Butterfly curves for RSNM (a) 10T SRAM, (b) TG10T SRAM, (c)11T SRAM, and (d) PPNN11T Cell

The voltage threshold is identified with separate the high and low states of the data. Measure the voltage margin between the stable regions (where the curve intersects with the accurate data states) and the voltage thresholds to obtain the RSNM value. It is important to repeat these measurements under different conditions to evaluate the robustness of the RSNM across various scenarios.

The RSNM value derived from butterfly curves provides crucial insights into the noise tolerance and reliability of the SRAM cell during the read operation.

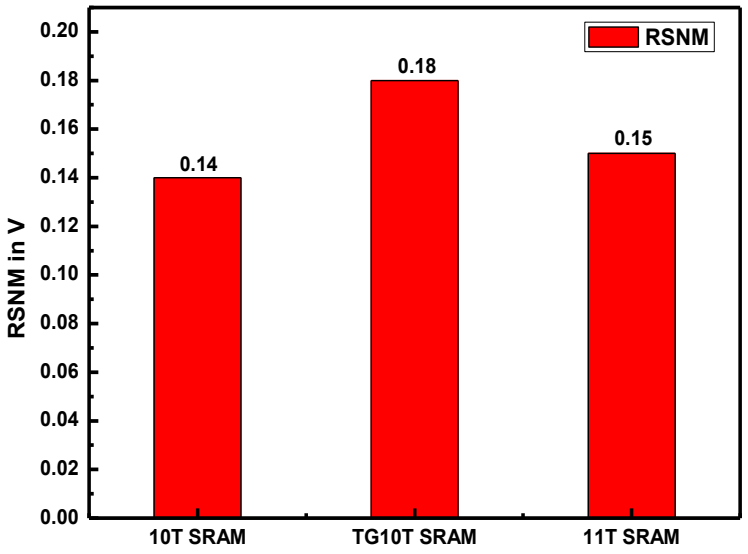

Fig. 3.9 Comparison of RSNM of various SRAM cells

The RSNM comparison between the different 10T and 11T cells illustrates that the read static noise margin for TG 10T cell is found to be maximum (i.e., 0.18 V) whereas it is found to be least in conventional 10T SRAM (i.e., 0.14 V).

3.4.3 Write static noise margin (WSNM)

It is an important parameter in the design and analysis of Static Random Access Memory (SRAM) cells, focusing on the stability of stored data during a write operation. It represents the voltage margin between the data state and the noise threshold that can cause unintentional data corruption during a write cycle. WSNM is determined by applying small perturbation voltages to the bitlines and assessing the ability of the cell to maintain the intended data state.

A higher WSNM value indicates better resilience against noise-induced disturbances, minimizing the risk of data flipping or unintended modifications during a write operation. Designers optimize the WSNM by carefully considering factors such as transistor characteristics, circuit design, process variations, and noise sources, ensuring robust and reliable write operations in SRAM cells, which are critical for accurate data storage and retrieval in memory applications.

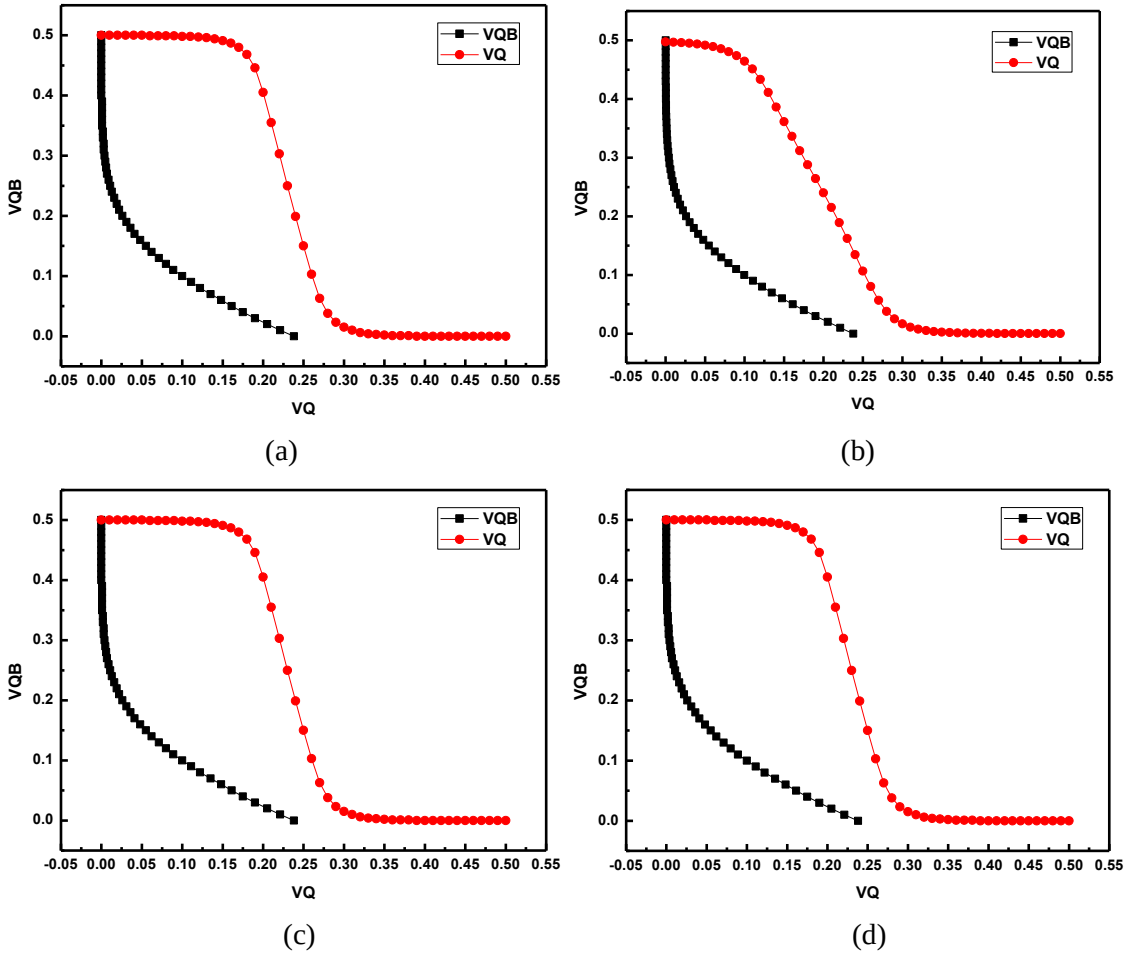

Fig. 3.10 Butterfly curves for WSNM (a) 10T SRAM, (b) TG10T SRAM, (c)11T SRAM

Measuring the WSNM (Write Static Noise Margin) value from butterfly curves involves the following steps. First, plot the butterfly curve by varying the wordline voltage (VWL) and observing the corresponding bitline voltage (VBL) at which the SRAM cell maintains the intended data state.

The voltage margin is measured between the stable regions (where the curve intersects with the intended data states) and the voltage thresholds to obtain the WSNM value. It is important to perform these measurements under different conditions to assess the robustness of the WSNM across various scenarios.

The WSNM value derived from butterfly curves provides valuable insights into the noise tolerance and reliability of the SRAM cell during the write operation, ensuring accurate and stable data storage.

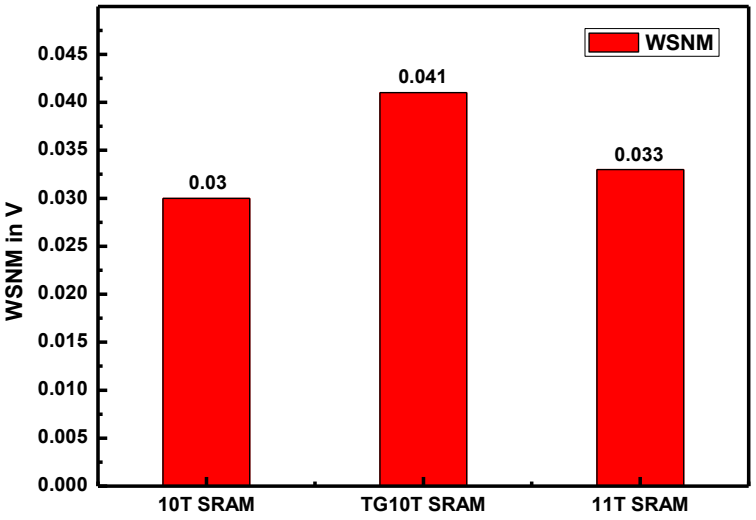

Fig. 3.11 Comparison of WSNM of various SRAM cells

The WSNM comparison between the different 10T and 11T cells illustrates that the write static noise margin for TG 10T cell is found to be maximum (i.e., 0.041 V) whereas it is found to be least in conventional 10T SRAM (i.e., 0.03 V).

3.5 POWER CONSUMPTION

Power consumption in SRAM cells is a critical consideration due to its impact on the overall energy efficiency of electronic devices. SRAM cells consume power in various aspects, including static power dissipation and dynamic power consumption.

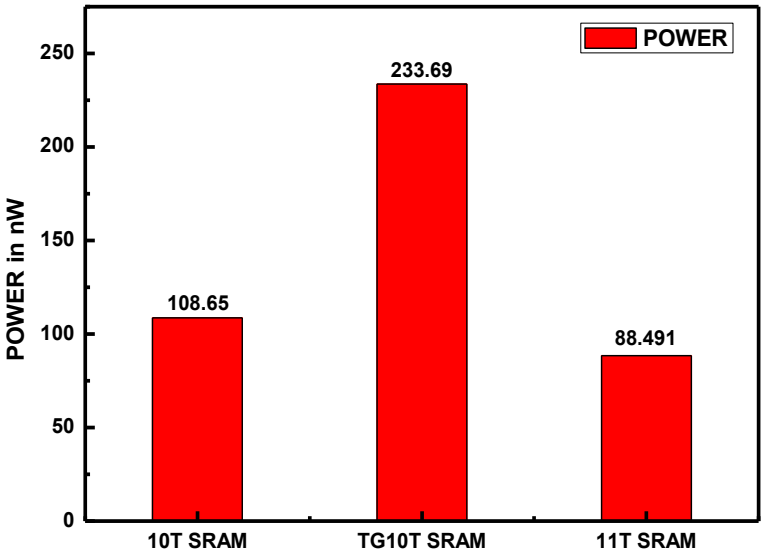

Fig. 3.12 Comparison of Power Consumption of various SRAM cells

Static power, also known as leakage power, arises from transistor leakage currents that flow even when the cell is in standby mode. It is influenced by factors such as transistor sizing, process variations, and temperature. **Dynamic power** consumption occurs during read and writes operations when charging and discharging the storage capacitors and during signal transitions. It is determined by factors like operating frequency, supply voltage, and access transistor characteristics.

Design techniques such as voltage scaling, transistor sizing optimization, and advanced low-power circuit architectures are employed to mitigate power consumption in SRAM cells, enabling energy-efficient operation and prolonging battery life in portable devices. The analysis confers power consumption for different variants of SRAM cells. The analysis associated depicts that the power consumed is maximum in TG10T SRAM cell whereas it is minimum in the case of 11T SRAM cell.

The power consumed by the TG10T cell (i.e., 233.69nW) is approximately two times as compared to the 10T SRAM cell (i.e., 108.65nW) and 11T SRAM cell (i.e., 88.491nW). As the technology node used in the analysis is 32nm, the power consumption is very low i.e., in nanowatts. Figure 3.12 depicts a graphical comparison of the three models in terms of power usage.

3.6 READ AND WRITE DELAY

The delay in a SRAM cell can be influenced by several factors, similar to other SRAM cell designs. The characteristics of the transistors used in the SRAM cell, such as channel length, width, and threshold voltage, can impact the delay. These parameters affect the transistor's switching speed and, consequently, the overall access time. The fabrication process used to manufacture the SRAM cell plays a significant role in its performance. Advanced process technologies with smaller feature sizes generally result in faster SRAM cells. However, the specific implementation details may vary depending on the process used.

The design choices and topology of the 10T SRAM cell can affect its delay. The specific arrangement of the transistors and the circuitry used to access and store data can impact the access time. Optimizations in the cell layout and peripheral circuitry can help mitigate

delays. The operating voltage and temperature can affect the delay in the 10T SRAM cell. Higher voltages can result in faster operation but may increase power consumption. Similarly, extreme temperatures can affect the overall performance and stability of the cell.

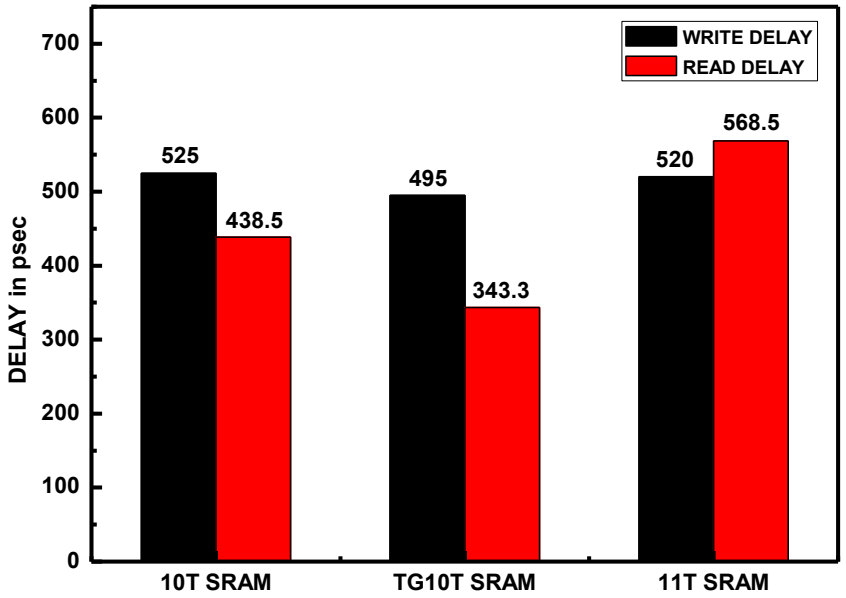

Fig. 3.13 Comparison of Delay of various SRAM cells

The TG10T model features a lower read and write access delay than the other two models, making it possible to read and write data to it more quickly. The read delay and write delay comparison for different variants of the SRAM cell is shown in Fig. 3.13. The analysis associated depicts that the read delay is maximum in 11T SRAM (i.e., 568.5 psec) due to a greater number of transistors in it whereas the write delay is maximum in case of 10T SRAM cell with source biased inverter (i.e., 525 psec). The analysis also shows that both read and write delay is minimal in TG10T SRAM cells. The read delay is 343.3 psec and the write delay is 495 psec respectively.

3.7 IMPORTANT RESULTS

From this chapter, after having studied in detail the important existing SRAM cell architecture that acted as the foundation for the design of the proposed 10T cell, following important outcomes can be drawn:

- The SRAM cell architectures developed previously by researchers were simulated individually in the LT Spice tool to analyze them extensively.

- The analysis included a proper understanding of their workings, quantifying their performance parameters by using the outputs obtained from the simulations. For instance, the butterfly curve is used for measuring Static Noise Margins (SNM), the transient analysis waveforms to understand read and write operations, and also to calculate the access delays. The read and write delay along with static noise margin was found to be the least in TG 10T cell but it has the highest power dissipation.
- Additionally, the complications and shortcomings in each architecture are discussed to understand what led to the development of other SRAM cell designs in order to improve the shortcomings.

CHAPTER 4

PROPOSED TRANSMISSION GATE BASED 10T SRAM CELL

The design and analysis of a low-power and high-performance transmission gate-based 10T SRAM cell involve optimizing the architecture and characteristics of the SRAM cell to achieve both low power consumption and high operational performance. The 10T SRAM cell architecture incorporates transmission gate-based access transistors, which offer improved speed and reduced leakage compared to traditional pass-gate or conventional CMOS-based SRAM cells.

The design focuses on minimizing power dissipation by carefully sizing the transistors and optimizing the voltage levels used for read and write operations. Additionally, advanced techniques like body biasing, power supply gating, and leakage reduction mechanisms are employed to further enhance power efficiency. Through detailed analysis, simulations, and performance evaluation, the low-power and high-performance 10T SRAM cell demonstrate improved speed, reduced power consumption, and adequate noise margin, making it suitable for energy-efficient and high-speed applications.

The chapter is divided into six sections. The first section (4.1) elaborates on the description of the proposed SRAM cell. The second section (4.2) mentions the dimension of the proposed cell, which highlights the technology node being used and the varying dimensions of pull-down, pull-up, and access transistors. The third section (4.3) deals with transient analysis to evaluate the behavior of SRAM cells during dynamic operations such as read and write operations. The fourth section (4.4) features data stability in which the butterfly curves HSNM, RSNM, and WSNM have been shown to evaluate robustness against noise and ensure reliable operation. The fifth section (4.5) shows the Monte Carlo analysis which plays a crucial role in assessing the performance and reliability of SRAM cells.

4.1 ARCHITECTURE AND WORKING OF PROPOSED 10T CELL

The proposed 10T SRAM cell is devised to reduce noise throughout read operations by incorporating an additional circuit that protects the cell from outside noise by switching off the access transistor despite the read operation being carried out. The read operations will be carried out by means of the transmission gate. In Figure 4.1, the input through PMOS of the transmission gate is the reverse of WL. While both the NMOS and PMOS assert, this takes the transmission gate to an active state which is connected to Q via an inverter. As a result, the value which Q holds can be read through an inverter.

With this design, any value retained at Q straight away flows via TG, eliminating the requirement for a precharge circuit as compared to other designs. Also, the power dissipated is negligible if the output read value is the same as the prior value of the read operation. So, this design diminishes the power when back-to-back 0 and 1 are to be read.

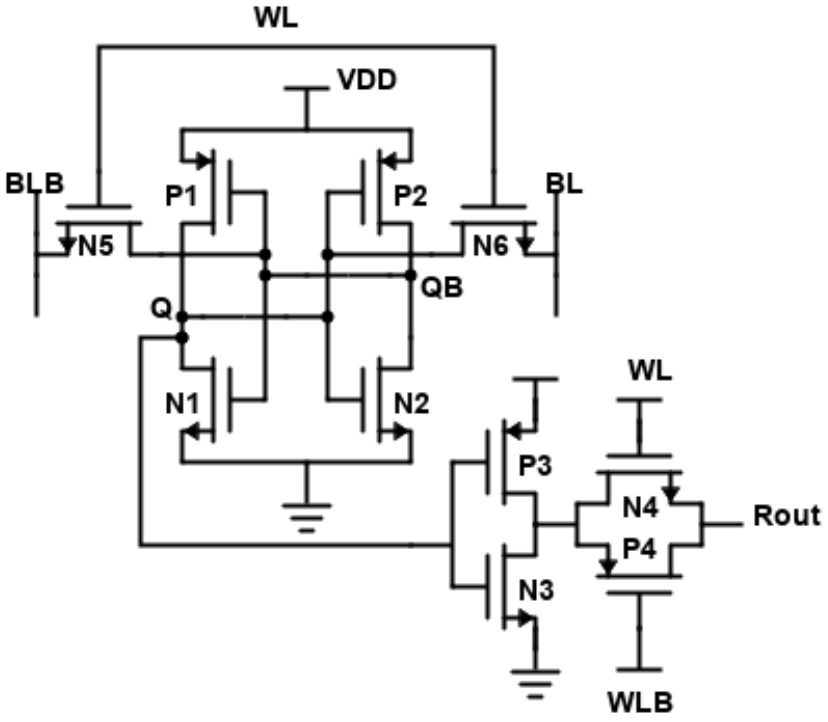

Fig 4.1 Schematic of Proposed TG based 10T SRAM cell

Here, the read operation along with the write operation is dependent on WL, BL, and BLB. When WL is 1, NMOS transistors N6 and N5 turn ON and so the value of QB and Q can be obtained. While performing the write operation, BL is 1 and BLB is 0. When WL switches on the transistors N5 and N6, the data is written on nodes QB and Q. On the

contrary, if the read operation is to be performed, BL=BLB=1 and WL=1. Here, as data can be read simultaneously, any of the bit lines begins to discharge. The output-connected sense amplifier reads the varying values.

4.2 DIMENSIONS IN THE PROPOSED CELL

The dimensions of an SRAM cell refer to the physical size and layout of the individual memory cell. Typically, an SRAM cell consists of several transistors, such as MOSFETs (Metal-Oxide-Semiconductor Field-Effect Transistors). The dimensions of these transistors, including their channel length, width, and other geometrical parameters, define the overall size of the SRAM cell. The dimensions of an SRAM cell are critical as they affect factors such as cell area, power consumption, access time, and noise margin. Shrinking the dimensions of an SRAM cell enables higher memory density, but it also presents challenges in terms of power consumption, stability, and manufacturing yield. Therefore, careful optimization of the dimensions is essential to achieve a balance between performance, area efficiency, and reliability in SRAM design.

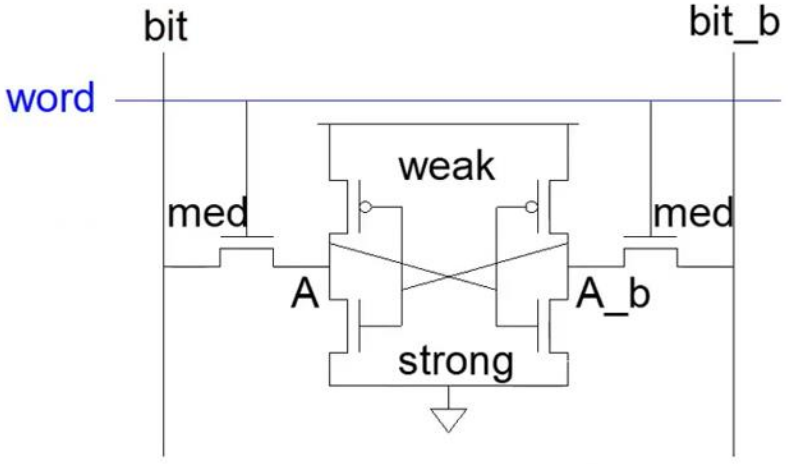

Fig. 4.2 A conventional 6T cell illustrating SRAM sizing

The LTSPICE tool was employed to execute simulations by constructing schematics of proposed SRAM cells for comparison. Table 4.1 shows the dimensions for the Proposed 10T cell.

TABLE 4.1 Dimensions for Proposed 10T cell

	Width (W)	Length (L)
P1, P2 (Pull-Up Transistors)	128n	32n
N1, N2 (Pull-Down Transistors)	256n	32n
N5, N6(Access Transistors)	192n	32n

The sizing of pull-up, pull-down, and access transistors in an SRAM cell plays a crucial role in determining its performance, power consumption, and stability. Here is a brief overview of the considerations for sizing these transistors:

a) Pull-up Transistors: The pull-up transistors are responsible for driving the stored data to a high voltage level (logic '1'). The sizing of pull-up transistors affects the read and write speeds of the SRAM cell. Larger pull-up transistors can provide a faster discharge of the bit-line during read operations and faster charging during write operations. However, larger transistors consume more area and power. The sizing of pull-up transistors is typically optimized to achieve a balance between speed, area efficiency, and power consumption.

b) Pull-down Transistors: The pull-down transistors are responsible for driving the stored data to a low voltage level (logic '0'). The sizing of pull-down transistors affects the stability and noise margin of the SRAM cell. Larger pull-down transistors enhance the stability of the '0' state and improve noise immunity. However, larger transistors may also lead to increased power consumption and larger cell area. The sizing of pull-down transistors is optimized to ensure a sufficient noise margin while considering the trade-offs with power and area.

c) Access Transistors: The access transistors enable the read and write operations in the SRAM cell by connecting the storage nodes to the bit lines. The sizing of access transistors impacts the cell's access time, power consumption, and noise margin. Smaller access transistors can reduce the cell's area and power consumption but may result in slower access times and reduced noise margins. Larger access transistors provide faster access times and improved noise margin but at the cost of increased area and power

consumption. The sizing of access transistors is optimized to meet the desired speed and noise margin requirements while considering the area and power constraints.

The sizing of the pull-up, pull-down, and access transistors in an SRAM cell involves a careful trade-off between performance, power consumption, stability, and area efficiency. It requires considering the specific requirements of the SRAM application and optimizing the transistor sizes to achieve the desired balance between these factors.

4.3 TRANSIENT ANALYSIS

Transient analysis of SRAM cells involves studying the dynamic behavior of the cell during various operations, such as read and write cycles. It focuses on analyzing the voltage and current responses over time, considering factors like access transistors, storage capacitors, and interconnects. During a read operation, transient analysis helps understand the stability and timing of data sensing, ensuring accurate retrieval of stored information. For write operations, the transient analysis examines the transient behavior during data storage, ensuring successful writing without corrupting adjacent cells. By simulating and analyzing the transients, designers can identify potential issues such as voltage droop, timing violations, and noise-induced disturbances. This analysis aids in optimizing the SRAM cell's performance, ensuring reliable and robust operation in terms of timing, voltage levels, noise immunity, and overall functionality.

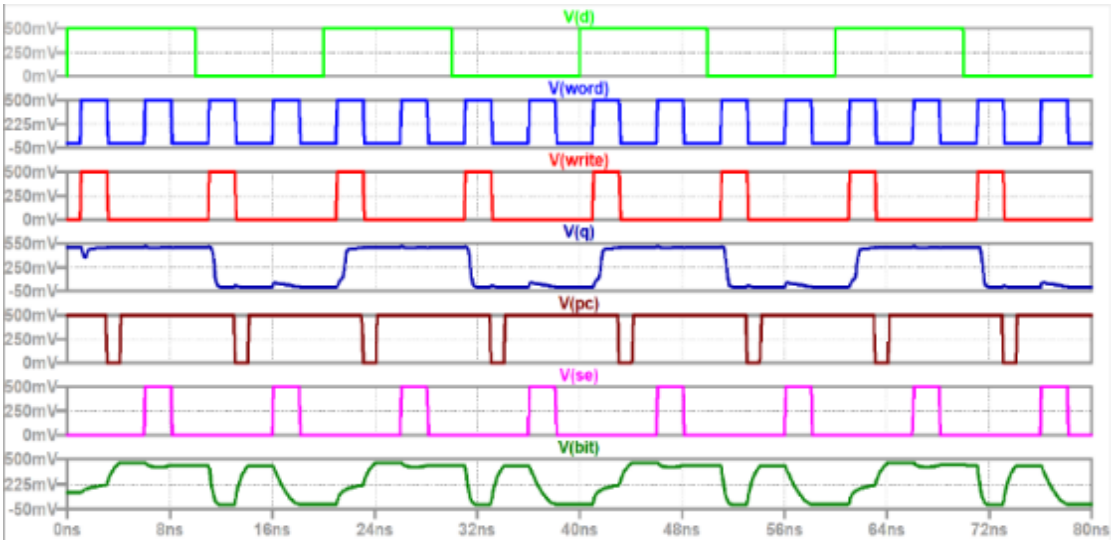

Fig. 4.3 Transient analysis of the Proposed 10T cell

To ensure that the hold, read and write operations worked correctly, transient analysis was performed for the proposed model. Similar read/write signals, identical input data signals, and precharge signals for read and write bit lines were employed to simulate the models. An identical sense amplifier, precharge circuit , and write driver were adopted to ensure the reliability of performance comparison. The results of the simulation are demonstrated in Figure 4.3.

According to the outcomes of the transient analysis, hold, read, and write operations are executed satisfactorily for the proposed models. Here, it is observed when both word and write are high, it writes onto the cell i.e., whatever data is there in D is transferred to Q. When both Word and SE are high, it reads from the cell. So, whatever data is there in Q is reflected in the bit line.

4.4 DATA STABILITY

The Static Noise Margin is calculated for all three operating modes. It is used to evaluate the data stability of cells during the operation of read, write, and hold. SNM, which is pertinent to all three operating modes, is defined as noise that applies to storage nodes before the stored state gets reversed. The specifics of measuring SNM using butterfly curves are described in this study.

The SRAM cell rests in a hold state for most of the operations in memory. So, the first analysis is to verify the stability of the hold operation, which is evaluated using the hold SNM. The values confer that as compared to other designs the Hold SNM for the proposed cell (i.e., 0.22V) is maximum.

The data saved in the memory of the SRAM cell could be viewed throughout a read operation by utilizing the access transistor. This makes it possible to sense the status of the cell using the bit lines.

4.4.1 Hold Static Noise Margin (HSNM)

It refers to the measure of noise immunity during the hold phase of the memory operation. SRAM cells are used to store digital information in memory chips and consist of multiple

transistors. Each SRAM cell typically consists of six transistors arranged in a cross-coupled configuration. During the hold phase, when the data is being stored, it is essential to ensure that the stored value remains stable and unaffected by external noise or disturbances. The HSNM parameter quantifies the minimum voltage or current difference required to maintain the stability of the stored data.

In an SRAM cell, the HSNM is determined by the critical node voltage margin. It represents the voltage difference between the input voltage at the hold node and the threshold voltage required to maintain the data state. A higher HSNM value indicates better noise immunity and a more robust SRAM cell.

The butterfly curve, often used for analyzing the hold static noise margin (HSNM) of an SRAM cell, represents the relationship between the bitline voltage and the wordline voltage during a hold operation. The curve illustrates the voltage levels at which the stored data in the SRAM cell can become vulnerable to flipping due to noise. The curve typically takes the form of a butterfly shape, with two lobes representing the stable regions where the stored data is secure. The curve's shape is influenced by factors such as transistor characteristics, circuit design, and noise sources. By plotting and analyzing the butterfly curve, designers can determine the hold voltage range that ensures reliable data retention and minimize the risk of data corruption or loss due to noise-induced disturbances.

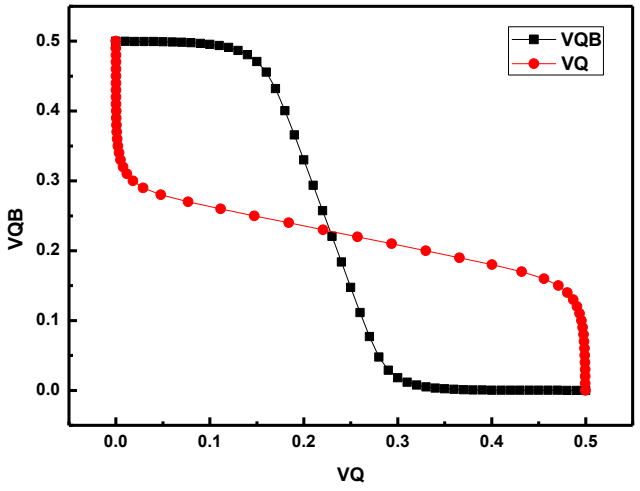

Fig. 4.4 Butterfly curve for HSNM of Proposed cell

Optimizing the butterfly curve and maximizing the hold static noise margin are crucial for achieving robust and reliable operation of SRAM cells in various memory

applications. Designers aim to maximize the HSNM value to enhance the reliability and performance of SRAM cells. Improving HSNM can be achieved through various design techniques, such as adjusting transistor sizes, optimizing supply voltages, or implementing circuit-level modifications. Overall, HSNM in an SRAM cell is a critical parameter that ensures the stored data remains intact and unaffected by noise or disturbances during the hold phase of memory operation.

4.4.2 Read Static Noise Margin (RSNM)

It is a measure of the noise margin or robustness of an SRAM (Static Random Access Memory) cell during the read operation. It quantifies the level of noise that the SRAM cell can tolerate while still providing a correct and reliable readout of stored data. When reading data from an SRAM cell, the cell's internal nodes are sensed to determine the stored value. RSNM is the measure of the voltage difference between the valid logic levels at the internal nodes, such as the bit-line or sense-amplifier inputs, necessary to ensure proper data readout.

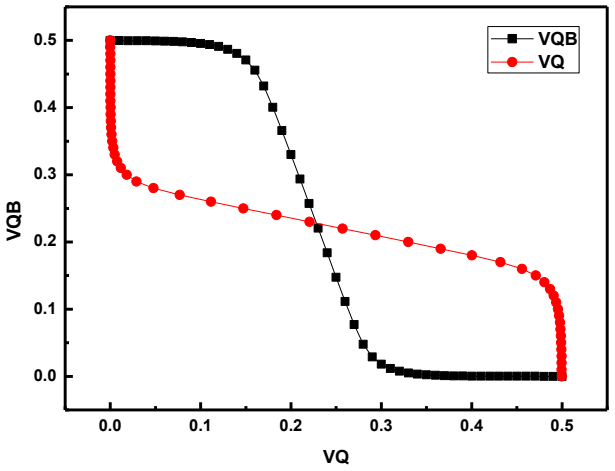

Fig. 4.5 Butterfly curve for SNM of Proposed cell

In an SRAM cell, RSNM is typically evaluated by applying a noise signal or perturbation to the internal nodes and measuring the amount of noise that can be tolerated without causing erroneous read results. The RSNM value is generally expressed as a voltage difference. A higher RSNM value indicates greater noise tolerance, implying that the SRAM cell is less susceptible to external disturbances and can provide more reliable readout. Improving RSNM is essential for maintaining data integrity in SRAM cells.

Designers employ various techniques to enhance RSNM, such as optimizing transistor sizes, adjusting voltage levels, and employing advanced circuit techniques like sense amplifiers, bit-line precharge, or noise-rejecting schemes. These techniques aim to increase the voltage difference between logic levels, reducing the likelihood of incorrect data readout due to noise-induced errors.

Read Static Noise Margin (RSNM) measures the noise tolerance of an SRAM cell during the read operation, indicating the level of noise that can be tolerated while still obtaining correct data. A higher RSNM value implies better noise immunity and improved reliability in data readout.

4.4.3 Write Static Noise Margin (WSNM)

It is a measure of the robustness of a static random access memory (SRAM) cell during the write operation. It indicates the minimum noise level that can be tolerated on the bitlines before the cell's state is affected. In an SRAM cell, data is stored using a pair of cross-coupled inverters. During a write operation, one of the inverters is driven to a high logic level (1) while the other is driven to a low logic level (0). The difference in voltage levels between the two bitlines (BL and $\overline{BL}$) determines the stability of the stored data.

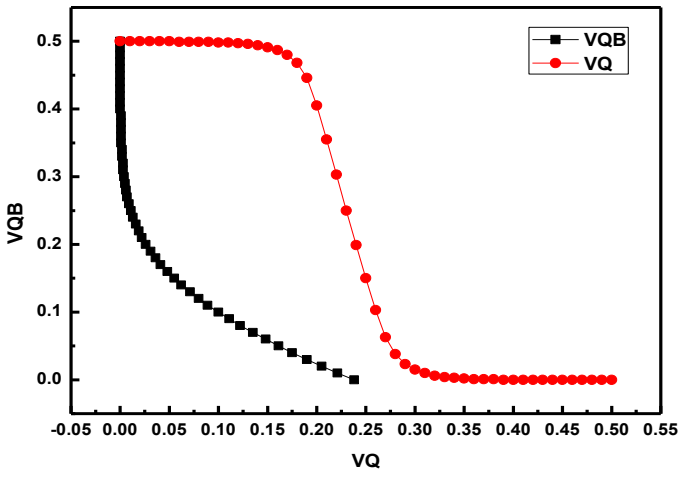

Fig. 4.6 Butterfly curve for WSNM of Proposed cell

The Write Static Noise Margin is typically defined as the minimum voltage difference required between the bitlines to reliably write data into the cell. It is measured by applying

noise or perturbations to the bitlines and determining the point at which the stored data starts to flip or become unreliable. A high WSNM indicates a more robust SRAM cell, capable of withstanding noise and maintaining the stored data integrity during a write operation. Conversely, a low WSNM implies that the cell is more susceptible to noise and may lead to data corruption or loss.

Designers aim to maximize the WSNM to ensure reliable operation of the SRAM cells under various operating conditions and noise sources. Achieving a high WSNM involves careful consideration of transistor sizing, power supply voltages, and circuit layout, among other factors, during the SRAM cell design process.

4.5 MONTE CARLO ANALYSIS

Monte Carlo analysis plays a crucial role in assessing the performance and reliability of SRAM cells. In SRAM design, various sources of variation, such as process variations, environmental conditions, and statistical fluctuations, can significantly impact the cell's functionality. By employing Monte Carlo analysis, designers can model these variations and evaluate their effects on key performance metrics, enabling them to make informed design decisions.

During Monte Carlo analysis, random input vectors are applied to the SRAM cell while considering the statistical distributions of the various sources. Simulations are then performed for each set of perturbed parameters, providing a comprehensive understanding of the cell's behavior under different operating conditions. This analysis enables designers to identify potential yield-limiting factors, assess the stability of read and write operations, evaluate noise margins, and optimize the SRAM cell's performance.

The Monte Carlo analysis aids in yield estimation and process control. By analyzing the statistical distribution of performance metrics across many simulations, designers can estimate the yield and determine the likelihood of meeting specified design specifications. It provides valuable insights into the statistical behavior of the circuit. It helps designers understand the impact of variations on the cell's performance, optimize the design for reliability and efficiency, estimate yield, and identify critical process steps for improvement. By leveraging Monte Carlo analysis techniques, designers can develop

robust and high-performance SRAM cells that meet the stringent requirements of modern semiconductor applications.

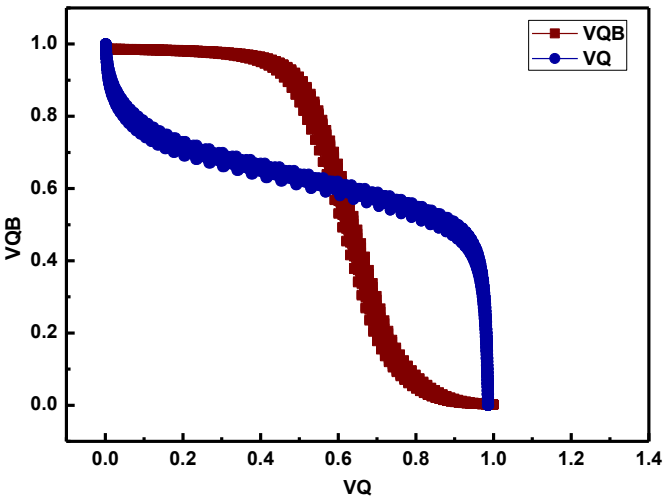

Fig. 4.7 Monte Carlo simulation of RSNM of proposed 10T cell

A Monte Carlo analysis was performed on a 10T SRAM cell, varying the threshold voltage (Vth), with a total of 1000 samples. This analysis aimed to evaluate the impact of Vth variations on the performance and stability of the SRAM cell. By considering a large number of samples, the analysis provided a comprehensive understanding of the statistical distribution and variability of key SRAM metrics, such as read and write margins, power consumption, and access time.

The Monte Carlo analysis allowed for a quantitative assessment of the cell's robustness against Vth variations, enabling designers to optimize circuit parameters and develop robust design methodologies to ensure the reliable operation of 10T SRAM cells in the presence of process variations.

4.6 IMPORTANT RESULTS

In this chapter, the proposed 10T SRAM cell is presented. The architecture is discussed in detail, and the measurement of values of parameters is shown using snapshots from the simulation. Major outcomes that can be drawn are:

- The proposed SRAM cell architecture is discussed in detail to acknowledge the changes in the cell architecture and understand how different it is from existing SRAM cell designs.

- Simulation findings revealed the measure of data stability in terms of static noise margins. The transient waveforms are analyzed to understand the different working natures of the proposed SRAM cell. The data stability analysis revealed the value of HSNM is 0.22V, RSNM is

CHAPTER 5

PERFORMANCE COMPARISON OF PROPOSED CELL WITH OTHER EXISTING CELLS

Performance comparisons of SRAM cells are conducted to assess and optimize their speed, power consumption, delay, and overall efficiency. SRAM cells are essential components in electronic devices, and their performance directly impacts the speed and power requirements of memory systems. Through such comparisons, engineers and researchers can identify the most efficient and high-performance SRAM cell designs for various applications. This enables them to make informed decisions about the selection and optimization of SRAM cells, ensuring optimal performance and power efficiency in modern digital systems.

The chapter is divided into two sections. The first section (5.1) elaborates on the performance comparison of the proposed cell with different 10T SRAM cells. The second section (5.2) features a performance comparison of the proposed cell with different 10T and 11T SRAM cells. The data stability is compared in which the butterfly curves HSNM, RSNM, and WSNM have been shown to evaluate robustness against noise and ensure reliable operation. The comparison of power consumption is done to explore if it can be mitigated through optimization techniques. The read and write delay of different 10T and 11T SRAM cells have also been compared to know the latency between initiating a read operation and obtaining the correct data output.

5.1 COMPARISON OF PROPOSED CELL WITH DIFFERENT 10T SRAM CELLS

The transmission gate-based 10T SRAM cell and the standard 10T SRAM cell are two variations of static random-access memory (SRAM) cells that differ in their circuitry. The transmission gate-based 10T SRAM cell replaces the access transistors of the standard 10T cell with transmission gates, which are composed of a pair of complementary metal-oxide-semiconductor (CMOS) transistors. This modification offers certain advantages over the standard 10T cell.

One key advantage of the transmission gate-based 10T SRAM cell is its improved write operation efficiency. The use of transmission gates allows for lower resistance paths during the write operation, resulting in reduced voltage drops and improved write stability. This can help mitigate issues like write failures and disturbances in the stored data. Additionally, the transmission gate-based 10T cell typically exhibits better write margins, enabling more reliable write operations and enhancing the overall performance of the SRAM cell. However, it is worth noting that the transmission gate-based 10T SRAM cell may introduce additional complexity in terms of area and power consumption due to the inclusion of the transmission gates.

Therefore, the choice between the transmission gate-based 10T SRAM cell and the standard 10T SRAM cell depends on the specific requirements of the application, considering factors such as power efficiency, write stability, and overall performance.

5.1.1 Data Stability

The Static Noise Margin is calculated for all three operating modes. It is used to evaluate the data stability of cells during the operation of read, write, and hold. SNM, which is pertinent to all three operating modes, is defined as noise that applies to storage nodes before the stored state gets reversed. The specifics of measuring SNM using butterfly curves are described in this study.

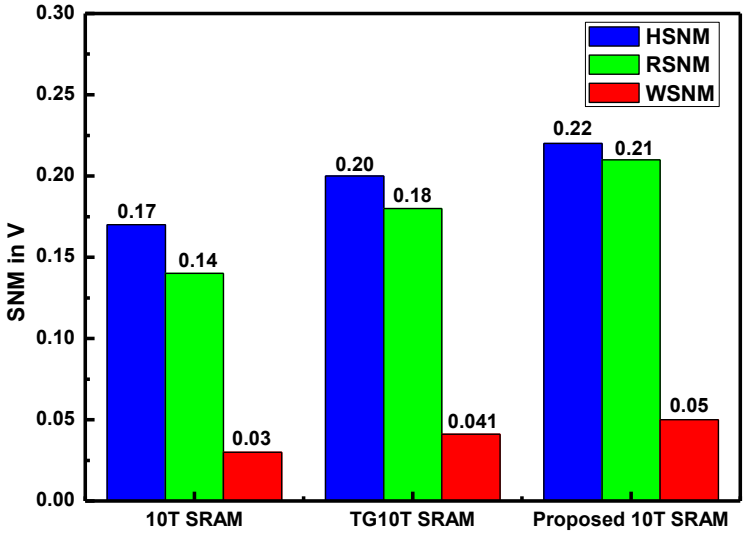

Fig. 5.1 Comparison of Static Noise Margin for various 10T cells

The results prove that as compared to other designs, the Read SNM (i.e., 0.21V) is greatest for the proposed cell. The writability of a bit cell is a computation of its capacity to upturn the data it has captured at the time of the write. It is often measured with write SNM. The writability for the cell proposed (i.e., 0.05V) is maximum.

5.1.2 Power Consumption

The power consumption of an SRAM cell is influenced by various factors, including the cell design, process technology, operating conditions, and data access patterns. Leakage power is the power consumed by a transistor when it is in an off-state but still exhibits some leakage current. In a 10T SRAM cell, the additional transistors compared to a 6T or 8T cell can contribute to increased leakage power. However, the leakage power can be mitigated through optimization techniques like transistor sizing and gate oxide thickness control.

When a read operation is performed on the SRAM cell, the stored data is accessed and read out. The power consumed during a read operation primarily depends on the bit-line capacitance and the voltage swings on the bit-lines. Higher bit-line capacitance and larger voltage swings generally result in increased power consumption during reads.

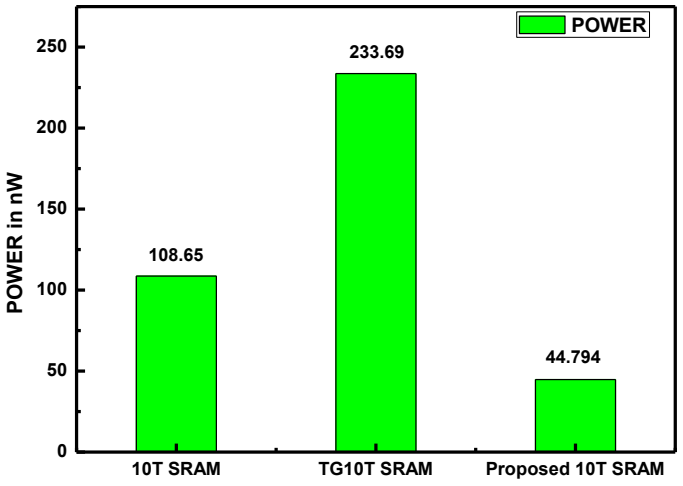

Fig. 5.2 Comparison of Power Consumption for various 10T cells

During a write operation, the SRAM cell is updated with new data. The power consumed during a write operation is influenced by factors such as the word-line capacitance and

the voltage swings on the word-lines. Higher word-line capacitance and larger voltage swings can result in increased power consumption during writes.

The power consumption in an SRAM cell can also be influenced by the access patterns of data. For example, if the data access patterns exhibit frequent read and write operations, the overall power consumption may increase compared to scenarios with less frequent access. The choice of process technology and operating voltage can impact the power consumption of an SRAM cell. Advanced process technologies with smaller feature sizes generally offer lower power consumption due to reduced parasitic capacitances and resistances. Additionally, operating an SRAM cell at lower voltages can help reduce power consumption, although it may affect performance.

The analysis confers power consumption for different variants of SRAM cells. The analysis associated depicts that the power consumed is maximum in the TG10T SRAM cell whereas it is minimum in the case of the TG based 10T SRAM proposed cell. The power dissipated by the TG10T cell (i.e., 233.69nW) is approximately two times in contrast to the 10T cell (i.e., 108.65nW) and five times when collated to the proposed 10T cell (i.e., 44.794nW). As the technology node used in the analysis is 32nm, the power consumption is very low i.e., in nanowatts. The power dissipated is negligible if the output read value is the same as the prior value of the read operation.

So, this design diminishes the power when back-to-back 0 and 1 are to be read. Figure depicts the power usage in a graphical observation of the three models. It's important to note that the power consumption of a 10T SRAM cell can vary based on the specific implementation, design optimizations, and operating conditions. Accurate power analysis is typically performed during the design phase, considering the target application's requirements and trade-offs between power consumption, performance, and area utilization.

5.1.3 Read And Write Access Delay

Read delay refers to the time required for data to be retrieved from a memory cell or storage element. It represents the latency between initiating a read operation and obtaining the correct data output. The read delay depends on various factors such as access time,

propagation delays, and the complexity of the read circuitry. During a read operation, the memory cell's stored data is sensed and amplified, typically using sense amplifiers or other detection mechanisms, before being outputted. The read delay is a critical parameter in memory systems, as it directly impacts the overall system performance and data access speed. Designers strive to minimize the read delay by optimizing circuit designs, reducing parasitic capacitances, and utilizing faster sensing techniques to ensure efficient and timely retrieval of data from memory elements.

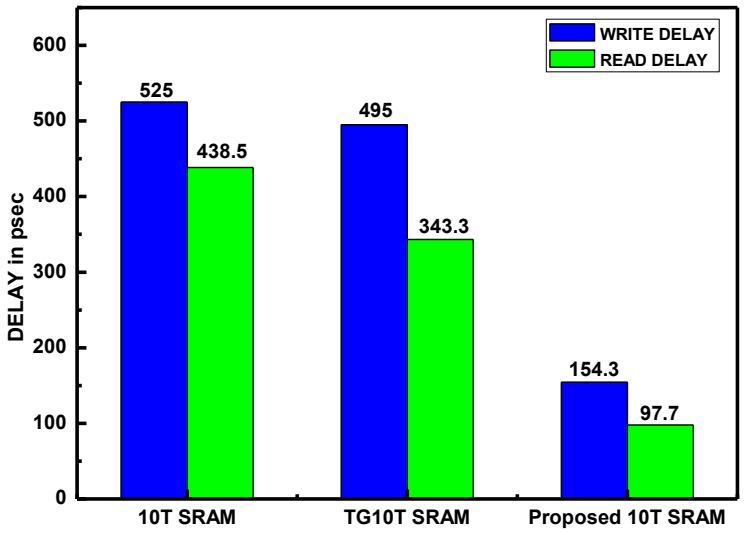

Fig. 5.3 Comparison of Delay for various 10T cells

The proposed TG based 10T model features a lower read delay than the other two models, making it possible to read data to it more quickly. The read delay along with the write delay comparison for different variants of the cell is demonstrated in Figure 4(b). The analysis associated depicts that the read delay (i.e., 97.7 psec) and write delay (i.e., 154.3 psec) is the least in the proposed 10T cell. For TG 10T cell, the read delay is 343.3 psec and the write delay is 495 psec respectively. For 10T cell, the read and write delay is maximum (i.e., 525 psec & 438.5 psec) respectively.

It's important to note that the delay in a 10T SRAM cell can vary depending on the specific implementation, process technology, and operating conditions. Detailed characterization and analysis are typically performed to determine the precise delay characteristics of the proposed cell.

5.2 COMPARISON OF PROPOSED CELL WITH DIFFERENT 10T AND 11T SRAM CELLS

The 10T SRAM cell and the 11T SRAM cell are two commonly used static random-access memory cell architectures with slight differences in their circuit designs. The 10T SRAM cell consists of 10 transistors, whereas the 11T SRAM cell has an additional transistor. The extra transistor in the 11T cell is typically used for stability and improved read operation.

One key advantage of the 10T SRAM cell is its lower power consumption compared to the 11T cell. The additional transistor in the 11T cell requires more power during read and write operations, resulting in increased power dissipation. On the other hand, the 10T cell offers a more power-efficient solution, making it preferable in low-power applications where energy efficiency is crucial.

However, the 11T SRAM cell has some notable advantages over the 10T cell as well. The additional transistor in the 11T cell improves the stability of the stored data, making it less susceptible to noise and process variations. This enhanced stability leads to improved read operation reliability and reduces the likelihood of data corruption. Additionally, the 11T cell may offer better performance in terms of access time and speed, as the additional transistor can help in reducing access delays and improving signal integrity.

The choice between the 10T and 11T SRAM cells depends on the specific requirements of the application. The 10T cell offers lower power consumption, making it suitable for energy-efficient designs, while the 11T cell provides better stability and potential performance advantages, which can be beneficial in applications that prioritize reliability and speed.

5.2.1 Data Stability

The data stability characteristics of 10T and 11T SRAM cells can vary due to their different circuit designs. Generally, the 11T SRAM cell offers improved data stability compared to the 10T SRAM cell. The additional access transistor in the 11T cell helps in isolating the bitline during read and write operations, reducing the potential for read disturbs and write failures. This additional transistor enhances the stability of the stored

data by providing a stronger read signal and better noise immunity, resulting in a more reliable SRAM cell.

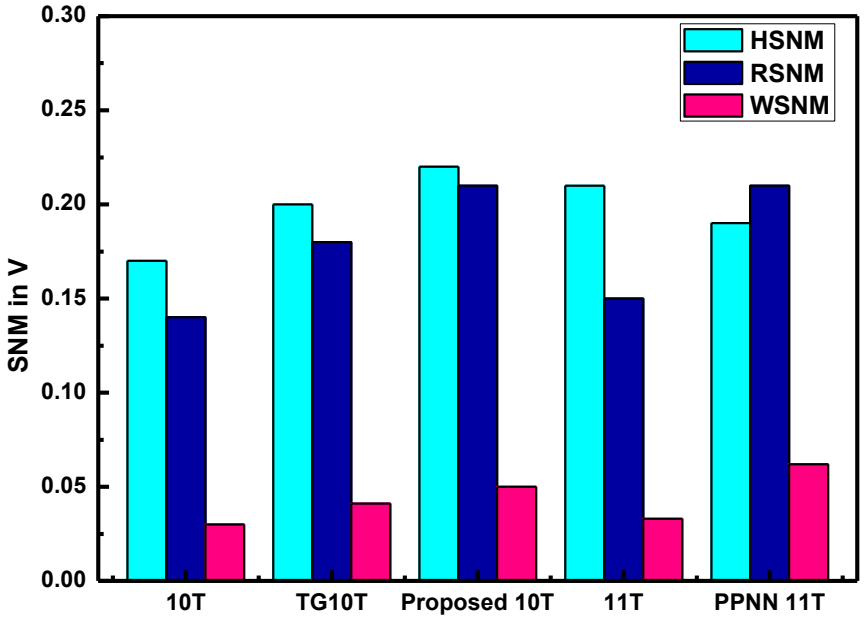

Fig. 5.4 Comparison of Static Noise Margin of proposed cell with various 10T and 11 cells

In contrast, the 10T SRAM cell may exhibit slightly lower data stability compared to the 11T cell. The absence of an access transistor in the 10T cell makes it more susceptible to read disturbances and write failures caused by noise or process variations. Without the isolation provided by the access transistor, noise coupling or variations in the bitline voltage can affect the stored data, potentially leading to errors or data corruption. However, it's worth noting that the data stability of both cell architectures can be further enhanced through techniques such as voltage scaling, improved sense amplifiers, and circuit optimization to mitigate the impact of noise and variations.

The results prove that as compared to other designs, the Read SNM (i.e., 0.21V) is greatest for the proposed cell. The writability of a bit cell is a computation of its capacity to upturn the data it has captured at the time of the write. It is often measured with write SNM. The writability for the cell proposed (i.e., 0.05V). The WSNM for PPNN11T cell is maximum (i.e., 0.06V)

The 11T SRAM cell generally provides better data stability compared to the 10T SRAM cell due to the presence of an additional access transistor. The extra transistor helps in isolating the bitline and improving the robustness of read and write operations. However, both cell architectures can be optimized to enhance data stability, and designers must carefully consider the trade-offs between stability, speed, and power consumption based on their specific application requirements.

5.2.2 Power Consumption

The power consumption characteristics of 10T and 11T SRAM cells can differ due to their distinct circuit designs. In general, the 10T SRAM cell tends to have lower power consumption compared to the 11T SRAM cell. This is primarily because the 10T cell has fewer transistors, resulting in reduced dynamic power dissipation during read and write operations. The simpler structure of the 10T cell leads to lower charging and discharging requirements, resulting in lower energy consumption per access.

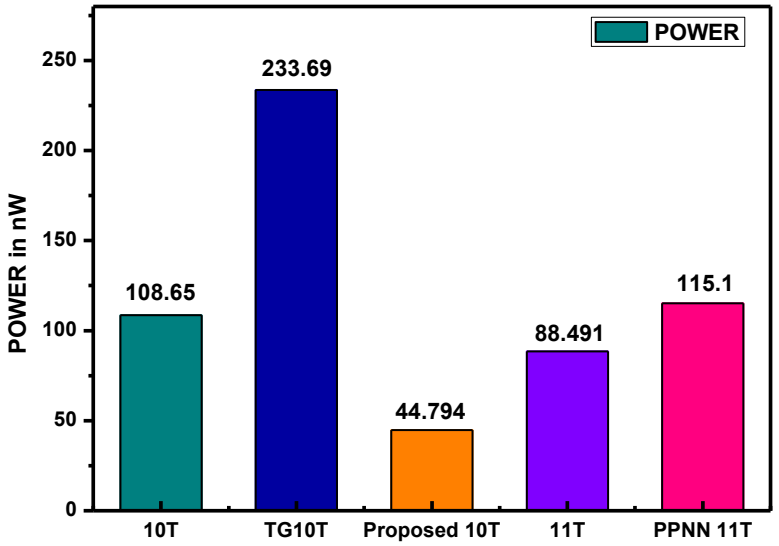

Fig. 5.5 Comparison of Power consumption of proposed cell with various 10T and 11 cells

On the other hand, the 11T SRAM cell typically consumes slightly higher power compared to the 10T cell. The presence of an additional access transistor in the 11T cell increases the overall transistor count and, consequently, the dynamic power dissipation. The additional transistor increases the capacitive load and switching activity, leading to slightly higher energy consumption during read and write operations. However, it's worth noting that the power difference between the two cell architectures is often relatively

small and can be mitigated through circuit optimization techniques and power management strategies.

The analysis confers power consumption for different variants of SRAM cells. The analysis associated depicts that the power consumed is maximum in the TG10T SRAM cell whereas it is minimum in the case of the TG based 10T SRAM proposed cell. The power dissipated by the TG10T cell (i.e., 233.69nW) is approximately two times in contrast to the 10T cell (i.e., 108.65nW) and PPNN 11T cell (i.e., 115.1 nW). It is five times when collated to the proposed 10T cell (i.e., 44.794nW). As the technology node used in the analysis is 32nm, the power consumption is very low i.e., in nanowatts. The power dissipated is negligible if the output read value is the same as the prior value of the read operation.

The 10T SRAM cell generally exhibits lower power consumption compared to the 11T SRAM cell due to its simpler circuit structure. However, the power difference between the two cell architectures is typically modest, and other factors such as process technology, operating frequency, and voltage scaling can influence the overall power consumption of the SRAM subsystem.

5.2.3 Read And Write Access Delay

The read and write delay characteristics of 10T and 11T SRAM cells can vary due to their different circuit architectures. The 10T SRAM cell is a popular choice in high-performance designs due to its reduced access delay. The absence of an access transistor in the 10T cell simplifies the signal path, resulting in faster read and write operations. However, the lack of an access transistor can make the 10T cell more susceptible to read disturbances and write failures caused by noise or process variations.

On the other hand, the 11T SRAM cell offers enhanced stability and improved read and write robustness compared to the 10T cell. The additional access transistor in the 11T cell provides a stronger read signal and helps isolate the bitline during write operations, reducing the likelihood of read disturbs and write failures. However, the presence of an extra transistor increases the overall circuit complexity, leading to slightly longer read and write delays compared to the 10T cell.

The 10T SRAM cell exhibits faster read and write delays but may be more vulnerable to noise and process variations. In contrast, the 11T SRAM cell provides improved stability and reliability at the cost of slightly longer access times. Designers must carefully consider the trade-offs between speed and robustness to select the appropriate SRAM cell architecture for their specific application requirements.

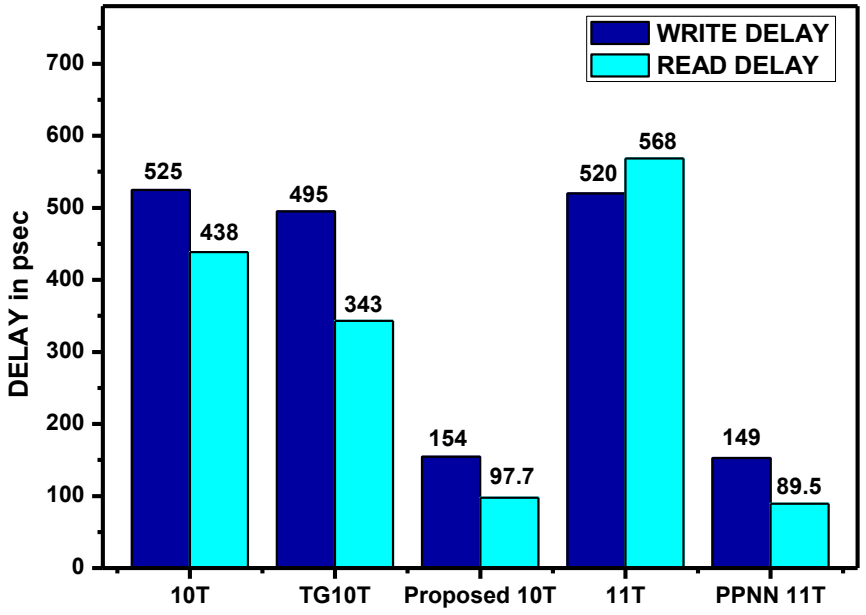

Fig. 5.6 Comparison of Delay of proposed cell with various 10T and 11 cells

The proposed TG based 10T cell and PPNN 11T cell features a lower read delay than the other two models, making it possible to read data to it more quickly. The read delay along with the write delay comparison for different variants of the cell is demonstrated in Figure 5.6. The analysis associated depicts that the read delay (i.e., 89.5 psec) and write delay (i.e., 149 psec) is the least in the proposed PPNN 11TT cell. It is almost comparable to the prposed cell. For TG 10T cell, the read delay is 343.3 psec and the write delay is 495 psec respectively. For 10T cell, the read and write delay is maximum (i.e., 525 psec & 438.5 psec) respectively.

5.3 IMPORTANT RESULTS

In this chapter, the proposed SRAM cell is compared against four other existing SRAM cell architectures, two of them are 10T SRAM cells and the other two are 11T SRAM cells. Thus, the comparison is divided into two sections for better understanding. They

were simulated them using the same technology node, supply voltage and under other conditions similar in all the topologies. Certain performance indicating parameters such as Static Noise Margins (SNMs), cell access delay, power consumption and Monte Carlo analysis are used as the basis for the comparative study. Important outcomes of the study include the following:

- Graphical interpretations are used to illustrate how the proposed SRAM cell fare against the existing models in terms of Static Noise Margins (SNM): Read SNM, Hold SNM and Write Margin. The results in both types of comparison indicate that the proposed SRAM cell has a very good margin in all three cases. The PPNN 11T SRAM is a little bit better in WSNM but this is compensated in the HSNM and RSNM.
- The PPNN 11T SRAM cell is found to have the least read and write access delays but it is almost comparable to that of the proposed SRAM cell.
- Power consumptions were also found to be least in the proposed cell.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

The research works on different SRAM cells have yielded valuable insights and advancements in the field of static random access memory. This study has focused on exploring the design, performance, and reliability aspects of 10T SRAM cells, aiming to uncover their potential as a viable alternative to other SRAM cells. Through a systematic investigation and analysis, several key findings have emerged, shedding light on various critical aspects. These findings have significant implications for the development of advanced integrated circuits. The chapter is divided into two sections. The first section (6.1) features the conclusion and the second section (5.2) draws a light on the future scope.

6.1 CONCLUSION

The research conducted on the proposed 10T SRAM cell has provided valuable insights into its performance compared to other SRAM cells. The proposed 10T SRAM cell offers several advantages over traditional 6T and 8T cells, including improved stability and reduced leakage power. One key finding of the research is that the 10T SRAM cell exhibits enhanced robustness against process variations and voltage fluctuations. This increased stability ensures reliable operation in various operating conditions, making it a promising choice for high-performance and low-power applications. Moreover, the proposed 10T SRAM cell demonstrates lower leakage power compared to other cells. This is attributed to the additional transistors that allow for better control of the power supply and leakage paths. The reduced leakage power contributes to improved energy efficiency and prolonged battery life in energy-constrained devices.

Another notable advantage of the proposed 10T SRAM cell is its higher static noise margin (SNM). The increased SNM enhances the cell's immunity to noise and improves the overall reliability of the memory design. This is particularly important in today's increasingly noisy and high-frequency environments. While the proposed 10T SRAM cell offers significant benefits, it is essential to consider its trade-offs. The additional

transistors in the 10T cell result in increased area overhead and slightly slower access times compared to other cells. However, these trade-offs can be acceptable in scenarios where stability, reduced leakage power, and improved noise immunity are critical requirements.

The TG10T SRAM cell is proven to be enhanced but it consumes more power. The TG10T SRAM cell considerably improves the stability of the data stored. This is primarily due to storage nodes being entirely cut from read bit-lines. On comparison with 10T SRAM, the latency is minimized for both TG10T SRAM and 11T SRAM. The read stability may have significantly increased as the TG10T SRAM cell has multiple bit-line discharging paths. It boosts writability by replacing NMOS access transistors with transmission gates. Moreover, the TG10T SRAM cell has increased read and write access speeds. It is plausible to conclude that the 11T models are much more compact than the 10T model despite using one more transistor due to the deployment of small-sized transistors, even though the comparison of the occupied area is not reproduced. The power consumed by the TG10T cell (i.e., 233.69nW) is approximately two times as compared to the 10T SRAM cell (i.e., 108.65nW) and 11T SRAM cell (i.e., 88.491nW). The analysis also shows that both read and write delay is minimal in TG10T SRAM cells. The read delay is 343.3 psec and the write delay is 494 psec respectively.

The comparison is also performed for three different 10T SRAM cells which consist of a 10T cell with source biased inverter, a TG10T cell, and a proposed TG based 10T SRAM cell. The data stability, power consumption, and read delay along with the write delay of all the SRAM cells are studied. The TG10T SRAM cell considerably improves the stability of the data stored. This is primarily due to storage nodes being entirely cut from read bit-lines. Secondly, as compared to the 10T cell, the latency is minimized for both TG based 10T cells. The analysis associated depicts that the read delay (i.e., 97.7 psec) and write delay (i.e., 154.3 psec) is the least in the proposed 10T cell. The proposed circuit absorbs five times less power as compared to the proposed 10T cell (i.e., 44.794nW). The proposed TG based 10T cell absorbs the lowest power and has better overall write and read stability as compared to the alternative designs. Additionally, the Monte Carlo analysis with 1000 samples has provided valuable insights into the statistical distribution and variability of key SRAM metrics, aiding in the optimization and robustness assessment of these cells. The PPNN 11T SRAM is a little bit better in WSNM but this

is compensated in the HSNM and RSNM. The PPNN 11T SRAM cell is found to have the least read and write access delays but it is almost comparable to that of the proposed SRAM cell.

The research on the proposed 10T SRAM cell highlights its potential as a viable alternative to traditional SRAM cells. Its enhanced stability, reduced leakage power, and improved noise immunity make it a promising option for future memory designs, especially in applications where reliability and energy efficiency are paramount considerations. Further optimization and integration efforts can unlock its full potential in driving advancements in memory technology.

6.2 FUTURE SCOPE

The 10T SRAM cell is a specific type of static random-access memory (SRAM) cell that consists of 10 transistors. It is commonly used in high-performance integrated circuits due to its advantages in terms of stability, read/write operations, and reduced leakage current. While predicting specific advancements in technology is challenging, there are several potential future scope areas for 10T SRAM cells:

- The continuous advancement of semiconductor manufacturing processes may lead to smaller feature sizes, enabling higher integration densities. This could result in packing more 10T SRAM cells in each chip area, thereby increasing memory capacity.
- Power efficiency is a critical concern in modern electronic devices. Future research may focus on optimizing the 10T SRAM cell's design to minimize leakage current and power consumption while maintaining or improving performance
- SRAM cells are susceptible to various forms of instability, such as read/write failures, retention failures, and process variations. Future research may aim to develop design techniques or circuit-level solutions to enhance stability and reliability, ensuring consistent operation even under challenging conditions
- Higher-performance computing systems often require faster memory access times. Future advancements may focus on reducing access latency, improving read and write speeds, and optimizing the cell design to enable faster operations
- With the increasing complexity of manufacturing processes, variations in transistor

characteristics are inevitable. Future research may focus on developing robust 10T SRAM cell designs that can tolerate process variations without significantly impacting performance, yield, or reliability

- Traditional SRAM cells are volatile, meaning they lose data when power is removed. Future research may explore the development of non-volatile 10T SRAM cells that retain their data even without power, combining the advantages of SRAM's high-speed access with non-volatility.
- Advancements in materials science and emerging technologies, such as nanoscale or alternative computing paradigms, could potentially influence the future of 10T SRAM cells. Exploring new materials or device architectures may lead to improved performance, reduced power consumption, or other desirable properties.
- As semiconductor fabrication technologies continue to evolve, new materials and device architectures may be introduced. Future scope for 10T SRAM cells may involve exploring these advancements and adapting the cell design to leverage the benefits offered by emerging technologies.

It's important to note that these potential future scopes are speculative and based on the current trends and challenges in the field of SRAM design. The actual directions of research and development may vary depending on technological breakthroughs, industry demands, and market requirements.

LIST OF PUBLICATIONS

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1. P. Yadav and P. Mittal, "A Comparative Performance Analysis of 10T and 11T SRAM Cells", 2nd International Conference Women Researchers in Electronics and Computing (WREC - 23), Jalandhar, India, April 2023 (**Scopus Indexed**)

   Status of Paper: Presented in the conference on 21st April 2023

2. P. Yadav and P. Mittal. "Design and Analysis of a Low-Power and High-Performance Transmission Gate Based 10T SRAM Cell", 7th International Joint Conference on Computing Sciences (ICCS-2023), May 2023 (**Scopus Indexed**)

   Status of Paper: Presented in the conference on 5th May 2023

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