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PERFORMANCE ANALYSIS OF AN IMPROVED 8T SRAM CELL FOR LOW POWER AND HIGH SPEED APPLICATIONS

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CERTIFICATE

I hereby certify that the Project Dissertation titled **"PERFORMANCE ANALYSIS OF AN IMPROVED 8T SRAM CELL FOR LOW POWER AND HIGH SPEED APPLICATIONS"** which is submitted by Deberjeet Usham, Roll No. 2K21/VLS/05, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the thesis work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

Memory is already known to be one of the most crucial parts of any electronic system. However, a class of memory called the cache memory is even more crucial amongst the type of memories since it is the one working closely in synchronization with the central processing unit (CPU). It is a faster and smaller memory and is also used to store data frequently used by the CPU. Its usage is inevitable in any system that performs computing digitally in any way. Cache memories consist of large arrays comprising millions of SRAM cells, which serve as the fundamental components of the cache memory system. As the ceiling of advancement of technology becomes higher, so does the demand of enhanced cache memories and hence the SRAM cells. Enhancement of these cells may be in the form of different parameters, but the crucial parameters that this paper will be focusing on are noise margins, access delay, power consumption, sturdiness to temperature and voltage drop variation, etc. Keeping the mentioned parameters as the guiding principle, a single ended, dual port SRAM cell architecture consisting of 8 transistors is proposed in this thesis work.

The memory cell under discussion incorporates several key design features to optimize its functionality. Firstly, it utilizes separate bitlines for read and write operations, ensuring independent and isolated functioning of these operations without any conflicts. Secondly, the storage node, formed by back-to-back inverters, remains undisturbed during read operations, resulting in enhanced data stability and reliability. Moreover, the cell employs dual VT (threshold voltage) transistors to minimize leakage power consumption, thereby improving energy efficiency. Lastly, the configuration of transistors within the cell is optimized to minimize the number of transistors in the read critical delay path, leading to reduced read delays and improved overall performance. These design considerations collectively contribute to the cell's efficiency, reliability, and speed, making it a valuable component for memory systems. However, upon closer inspection, this model suffers from a concerning shortcoming, that is, its write performance is very unsymmetrical, and lower than most of its counterparts. Thus, to make an improvement in this aspect and other aspects very crucial to SRAM functioning, another SRAM cell consisting of 8 transistors is proposed in this thesis work.

The performance indicating parameters of the suggested cell is also compared alongside five other models using the same technology node, supply voltage and identical simulation conditions. After conducting transient analysis on the proposed SRAM cell, the results indicate a read delay of 83 picoseconds (pS) and a write delay of 126 pS. Analysis of power consumption shows that the proposed SRAM cell consumes dynamic read and write power of 12.8 μW and 10.4 nW respectively and a static power consumption of 0.932 μW. It was also observed to have static read noise margin of 140.8 mV and hold noise margin of 143.5 mV each and a write margin of 400.6 mV. Supply voltage variation to emulate voltage drop variation reveals variation of hold, read and write margin as shown in the graphical representations below. Further, temperature variations were simulated which showed that hold margin varied at 0.77 mV/°C, read margin at 0.79 mV/°C and write noise margins at 0.58 mV/°C.

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LIST OF ABBREVIATIONS

S.No.	Abbreviation	Full Name
1.	SRAM	Static Random Access Memory
2.	BL	Bit Line
3.	BLB	Bit Line Bar
4.	WL	Word Line
5.	WLB	Word Line Bar
6.	TG	Transmission Gate
7.	SNM	Static Noise Margin
8.	RSNM	Read Static Noise Margin
9.	HSNM	Hold Static Noise Margin
10.	WM	Write Margin
11.	PVT	Process Voltage Temperature
12.	RBL	Read Bit Line
13.	RBLB	Read Bit Line Bar
14.	WBL	Write Bit Line
15.	WBLB	Write Bit Line Bar
16.	R	Read Signal
17.	W	Write Signal

18.	PC	Pre-Charge Signal
19.	RAM	Random Access Memory
20.	ROM	Read Only Memory
21.	DRAM	Dynamic Random Access Memory
22.	EPROM	Erasable Programmable Read Only Memory
23.	EEPROM	Electrically Erasable Read Only Memory
24.	PROM	Programmable Read Only Memory

CHAPTER 1

INTRODUCTION

Artificial intelligence (AI) is the recent buzz in today's technology world and the hype is rightly deserved, because AI is really the future. There aren't many things left that AI is not capable of doing. And with the advancement of AI, the amount of data to be stored and processed are going to become humungous. In the present technology market, the significance of memory has grown exponentially, with memory-intensive tasks being performed on various devices like mobile phones and computers. Cache memory, a critical component for memory-dependent systems, relies on the fundamental building unit known as the Static Random Access Memory (SRAM) cell [1]. From microcontrollers and System on Chips (SoCs) to personal computers and workstations, memory holds a paramount position in the functionality of diverse systems.

Amongst the different types of memory available, cache memory is one of the most crucial memories since it directly interacts with the Central Processing Unit (CPU) to temporarily store data that are often accessed by the CPU [2]. Thus, as the level of Artificial Intelligence and other technologies become more advanced, it is the cache memory and the memory in general that should be improved in order to facilitate the necessary advancements in technology. This would mean that the cache memories should become faster for the CPU to be able to store and retrieve data from at a much faster speed. Additionally, it should become more power efficient, more robust to noise to store data in a stable manner [2]. Also, the cache memory should be sturdy in response to temperature variance and also voltage variations caused by voltage drops in the power delivery network of chips are the need of the hour. Only when the cache memories perform to its full capacity, will AI live up to its full potential. Cache memories are fundamental components composed of arrays consisting of millions of Static Random Access Memory (SRAM) cells. These SRAM cells are responsible for storing data in a cache memory system, with each cell storing a single bit of data. The collective arrangement of these SRAM cells forms the structure of the cache

memory, allowing for efficient and high-speed data access and retrieval. [1]. So, each type of enhancement that would be demanded from the cache memories would only be achieved when the same enhancements are obtained from the SRAM cells.

This introductory chapter is distributed into six sections. Section 1.1 consists of the classification of different types of memory and where SRAM lies in it. Section 1.2 consists of the motivation, which highlights why the chosen field of research is important and relevant. Section 1.3 highlights the objectives of the research work. Section 1.4 gives a brief discussion about the methodology used to carry out this research work. Section 1.5 highlights the tool used to perform the research work. Lastly, section 1.6 presents the detailed organisation of the thesis.

1.1 MEMORY CLASSIFICATION

Memory can be classified into many different types. Fig. 1.1 graphically represents the classification of memory types.

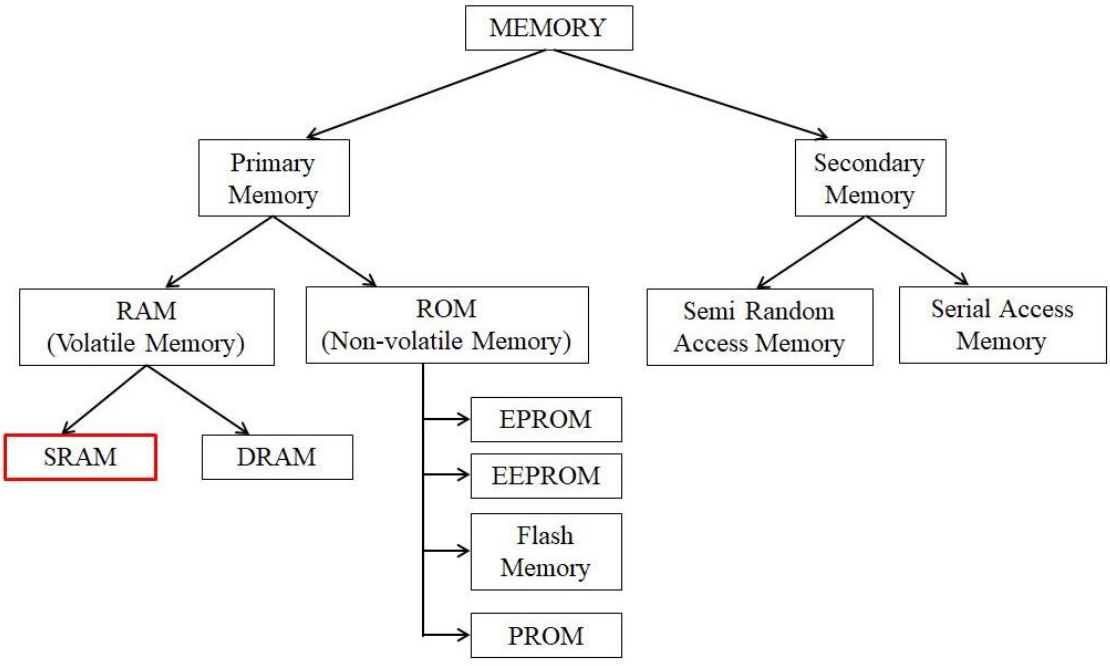


Fig. 1.1: Memory Classification

First of all, SRAM belongs to the class of memory called primary memory. Within the primary memory, there are two types divided based on whether it is volatile or not. Volatile

memory, specifically referred to as Random Access Memory (RAM), is a class of memory that retains data only till it receives a continuous power supply. However, as soon as the supply of power is interrupted or cut off, the data stored in RAM is degraded very fast [2]. On the other side, ROM (Read Only Memory) stores its data even when power supply is cut off. The name Read Only Memory is often misleading because many ROM memories can be written to as well as read from. It thus is a non-volatile memory. The types of memories belonging to this class are Flash Memory, , EEPROM (Electrically Erasable Programmable Read Only Memory), PROM (Programmable Read Only Memory), EPROM (Electrically Programmable Read Only Memory) [3]. So, the SRAM (Static Random Access Memory) is a type of Random Access Memory which is rapid and dense in nature. The DRAM on the other hand is slow and compact. The SRAM stores its data in a back-to-back inverter whereas the DRAM stores its data on a capacitor, so it needs to be refreshed periodically.

There is also another broad class of memory called the secondary memory. Secondary memory is external storage that everlastingly saves data. The CPU can access primary memory data directly, while secondary memory data cannot be accessed. [4].

1.2 MOTIVATION

There are certain features of an SRAM cell that has been the source of bad performances in the past existing SRAM architectures and hence improving these features would mean enhancing the SRAM cell. For instance, SRAM cells face challenges such as small noise margins and high power consumption. Their larger transistor count limits density, hindering the inclusion of more cells in a given area. While they offer fast access, achieving higher speeds can be difficult. Temperature and voltage variations contribute to higher noise parameter variations. These troubles are present in one or the other way in many existing SRAM cell architectures. Overcoming these troubles overall is the problem statement with regards to SRAM cell design. A common method researchers have taken up is to rigorously scale down the technology nodes.

However, along with the technology node scaling, supply voltages also must be scaled down so that field strength remains the same [1]. And with voltage scaling comes several adverse effects, such as the data held in the SRAM cell becoming more susceptible to noise

and variability with respect to temperature, process, etc increasing. In addition to this, with decrease in supply voltage, leakage power that happens in standby mode starts to increase so much beyond its normal levels that it becomes comparable to dynamic power consumption. Additionally, a decrease in supply voltage causes access delays to worsen, which means reduction of speeds and frequency in which the memory would operate. In an attempt to solve these complications, researchers have resorted to using a greater number of transistors and a configuration of transistors different to the famous 6T SRAM cell [10]. However, more transistors would also mean a more area occupation and hence less dense memory arrays. So, it all comes down to managing these trade-offs to find the perfect fit that would be robust to noise and variations, less power consuming, fast and at the same be fairly low on the transistor count.

1.3 OBJECTIVES

Having considered all the problems and concerns with regards to the design of an SRAM cell, it thus makes sense to dwell further into SRAM design and look for enhancements and modifications that can be made to the existing SRAM cell architectures and further make an effort to propose an improved SRAM cell that eases the complications stated in problem statements section. Thus the objectives of this thesis work are:

1. To review some important existing SRAM cell topologies, with an emphasis on how each architecture provides a unique form of improvement.

2. To propose a novel SRAM cell architecture that proves to be superior with regards to parameters such as Static Noise Margins (SNMs), power efficiency, access speed, sturdiness in response to temperature and supply voltage variations.

3. To compare the performances of the proposed SRAM cell architecture against that of some existing SRAM models that also acted as motivation towards the design of the architecture and are also similar in some aspects such as transistor configuration and count.

1.4 METHODOLOGY

The methodology of this research begins with the parametric extraction and comprehensive review of fundamental existing SRAM cell architectures that consists of varying number of transistors. The review is comprehensive because all the SRAM cell architectures have been simulated using the same tool, same technology node and other identical aspects to understand their working in detail, to measure the performance indicating parameters individually. Here, five previously reported SRAM cell architectures are studied and reviewed, out of which two models have the same number of transistors as the proposed SRAM cell and three models have varying number of transistors in their respective designs. The knowledge gained from this extensive review is used to help in the design of our proposed SRAM model. The proposed model incorporates a technique where the mutual feedback between a pair of inverters is interrupted during a write process. During the write operation, the outputs of the inverters in the SRAM cell are not directly connected to the inputs of the other inverter, resulting in an isolated configuration. By cutting this feedback loop, the model aims to optimize the write operation and improve the overall performance of the system. This is done so that the write performance improves. Then, the proposed SRAM model is realised schematically in the software and simulated using the same tool and technology node. The simulation results are used to authenticate the correct functionality of the circuit and also to extract the performance indicating parameters. Then lastly, the proposed SRAM cell is put into test by comparing the measures of its performance indicating parameters with that of the existing SRAM cells. The comparative analysis results are utilized to validate the advantage of the proposed cell compared to the existing SRAM cells.

1.5 TOOLS USED

The software used for carrying out the research is Cadence Virtuoso. The Cadence Virtuoso tool was used for constructing schematics of various SRAM cells and simulating them using the same technology node, identical supply voltage, same variation of temperature and supply voltage to observe their performance with regards to parameters such as Static Noise

Margins (SNMs), power consumption, access speed, sturdiness to variation of voltage and temperature.

1.6 THESIS ORGANIZATION

The complete dissertation is organized into 6 chapters. Chapter 1 gives introduction of the thesis work that includes in its subsections, the background behind the research work amongst other things. Then Chapter 2 that includes literature survey and research gap. Chapter 3 includes detailed review and analysis of some existing SRAM cell architectures that also served as motivation towards the architecture of the suggested SRAM cell. Chapter 4 gives a thorough explanation on the methodology and implementation of the proposed work. Chapter 5 gives a comparison of performance of some important parameters of the proposed SRAM model against some existing models. Chapter 6 consists of conclusion and future scope. Each chapter consists of subsections.

- **CHAPTER 1**: This chapter highlights the importance of memory in today's technologically advanced world. It includes the following: basic classification of memory types, the motivation behind choosing such a topic as an area of interest for research, the methodology followed during the research work, details of the tools used and the objectives of the thesis work in a detailed manner.
- **CHAPTER 2**: A literature review of previous reported works is discussed in this chapter. It consists of brief reviews of different types of SRAM cell architectures with varying transistor counts, varying number of bitlines and ports. It also includes the research gap that we will be looking to exploit in this thesis work.
- **CHAPTER 3:** This chapter presents the comprehensive review of some existing SRAM cell architectures. The extensive review of each of the considered SRAM cell architectures is concluded with the complications that were observed in each of the designs and how each model looks to improve on the shortcomings of previous design.
- **CHAPTER 4:** This chapter elucidates the proposed SRAM cell model, discussing its design and operation. It also includes the simulation results of each of the considered performance indicating parameters.

- **CHAPTER 5:** This chapter offers a detailed comparative analysis between the proposed 8T SRAM cell and five existing cell models that motivated its design in some or the other way. The comparison is done on five primary parameters such as static noise margins, access delays, power consumption, response to temperature variation and supply voltage variation. There are sub parameters within each parameter also.
- **CHAPTER 6:** The dissertation is concluded with the overall conclusions and data of results drawn from the research work. It also includes future scopes of improvement related to the topic of research.

The list of publications related to the research done for this thesis is also attached. After that, a comprehensive list of references is provided, which is utilized to cite earlier study to determine the routes our current work should take.

CHAPTER 2

LITERATURE REVIEW

Genuine research ideas mostly stem from previous works reported by other researchers in the same field. So in order to perform a research work, it is always vital to go through the work that has been reported. A literature review's purpose is to:

- Build an initial basis for understanding the topic of research.
- Identify past areas of research to reduce duplication and give deserved recognition to works done by other researchers.
- Acknowledge the discrepancies, research gaps, major research disputes, and unresolved problems in earlier studies.

This chapter is distributed into two sections. Previously reported work is the section 2.1. Section 2.2 gives a complete review in a tabular form. Research gap in this area of study is discussed in the section 2.3.

2.1 DIFFERENT REPORTED SRAM CELLS

- **"Implementation of Low-Power 6T SRAM Cell Using MTCMOS Technique", 2017**

T. Tripathi, D.S. Chauhan, S.K. Singh and S.V. Singh [17] reported a 6T SRAM cell based on MTCMOS technique. The major intention of the innovation was to reduce leakage power consumption during idle mode. It uses two types of transistors with, one with high threshold voltage (V_T) and the other with low V_T. The simulation results reported a significant reduction in leakage power consumption.

- **"A Modified SRAM Based Low Power Memory Design", 2016**

A. Pathak, D. Sachan, H. Peta, M. Goswami [18] reported another modified 6T SRAM cell that focused on reducing hold power consumption. The innovation in this architecture is the

usage of a tail transistor that enables reducing the short circuit power consumption by disconnecting the conductive trail from V_{DD} to V_{SS}. This extra transistor called the tail transistor additionally helps in reducing the off-state current (subthreshold current) because it basically helps in forming a stack configuration, thereby reducing subthreshold current. The findings from the simulation prove that the power consumption in hold mode is indeed reduced significantly. Statistical and corner analysis was also performed to determine the design's robustness.

- **"A Novel Approach to Design SRAM Cells for Low Leakage and Improved Stability", 2018**

T. Tripathi, D..S Chauhan, S.K. Singh [19] proposed a novel modified 6T SRAM with the intention to have high speed, low leakage current and high stability. They used a combination of multi threshold CMOS and two finger MOS transistors to achieve the enhancements. The research findings indicate that the reported design of the SRAM cell exhibits a remarkable improvement in read stability, nearly 2.7 times higher, and a notable reduction in leakage current, approximately 1.85 times lower, when contrasted with the 6T SRAM cell. As a penalty, an increase in area was observed in the new design.

- **"A robust and low power 7T SRAM cell design", 2015**

K. Mehrabi, B. Ebrahimi and A. Afzali-Kusha [20] reported an SRAM cell consisting of 7 transistors offering enhanced stability during reading and writing processes. The separation of the read and write access transistors in the research addressed the persistent issue of conflicting sizing requirements, enabling the satisfactory execution of both read and write process in the SRAM cell. This innovative approach resolved the long-standing problem of accessing transistors by optimizing their sizing individually for improved performance. The cell also features enhanced read stability through the segregation of the internal node away from the read path, ensuring improved data integrity and reliability. Write ability is also enhanced due to the weakening of positive feedback by usage of virtual ground at one of the inverters in the process of writing onto the cell. The virtual ground in the design also helped reduce the leakage current by providing a stacking effect. The simulation results recorded an improvement of read stability and write ability by 80% and 54.9% respectively.

- **“Single Bit Line Accessed High Performance Ultra Low Voltage Operating 7T SRAM Cell with Improved Read Stability”, 2021**

B. Rawat and P. Mittal [21] presented a static random-access memory (SRAM) bit cell design comprising of 7 transistors. Notably, their design employed only one bitline for the process of both reading and writing from and to the cell, addressing the need for efficient memory access. The utilization of one bitline in the proposed cell design resulted in reduced activity factor during read and write operations. Compared to other single-ended SRAM cells with varying transistor counts ranging from a transistor count of 5 to 10, the proposed cell exhibited an improved Static Noise Margin (SNM) in all 3 scenarios of read, write, and hold mode. Leakage power was also found to be minimal.

- **“A comprehensive analysis of different 7T SRAM topologies to design a 1R1 W bit interleaving enabled and half select free cell for 32 nm technology node”, 2022**

B. Rawat, P. Mittal [22] also reported a novel single ended, dual port, 1R1W SRAM cell consisting of 7 transistors. The proposed model uses an extra transistor that enables cutting of mutual feedback connection between the two inverters whose output terminal are coupled to the input terminal of the other inverter and converting it into a cascade of two inverters. The reported SRAM cell model was compared with other 7T SRAM cell models and was found to have the best Hold and Read Static Noise Margin (RSNM/HSNM). Its static power consumption was also observed to be one of the lowest amongst the other existing cells. Process, Voltage and Temperature (PVT) analysis was also performed to prove superior reliability of the cell.

- **“Leakage Power Attack-Resilient Symmetrical 8T SRAM Cell”, 2018**

R. Giterman , M. Vicentowski, I. Levi , Y. Weizman, O. Keren and A. Fish [23] proposed an 8T SRAM cell that is designed for low leakage power consumption. To alleviate the influence of leakage currents on stored data, the design of this cell increases two extra transistors to the design of the traditional 6T SRAM, thereby enhancing the stability and integrity of the data existing on the storage nodes. The findings of the simulation that

included Monte Carlo analysis indeed validated the reported SRAM cell's low leakage power.

- **"Design and analysis of a 32 nm PVT tolerant CMOS SRAM cell for low leakage and high stability", 2010**

S. Lin, K. Yong-Bin and F. Lombardi [5] proposed a 9T SRAM cell that is primarily aimed at providing a robust and process-voltage-temperature variation tolerant cell with minimum static power consumption. The cell is also designed so that the data stored on the cell is has high stability. The simulation findings validated that the tolerance and robustness. The results also revealed that the reported SRAM design consumes 33% lesser leakage power. It also showed that the delay being exhibited by the reported SRAM is on the lower side.

- **"Low leakage 10T SRAM cell with improved data stability in deep sub-micron technologies", 2021**

In their study, Krishna and Duraiswamy [28] introduced a novel SRAM cell consisting of 10 transistors. The design incorporates two additional transistors to form a source-biased inverter, effectively reducing static power dissipation. By increasing the potential of the source terminal and decreasing the drain-to-source potential, the leakage power is minimized. The design also employs various assist techniques to enhance cell stability. Simulation results confirm the successful achievement of the design objectives.

- **"Robust transmission gate-based 10T subthreshold SRAM for internet-of-things applications", 2022**

E. Abbasian and M. Gholipour [29], presented a complementary pass gate based 10T SRAM cell used in IoT applications. It is compared with other existing SRAM cell designs that are all subjected to the same extreme PVT variations. To enhance the sense margin, the proposed cell utilizes a differential scheme. It strengthens the write-ability by utilizing two complementary pass gates instead of two NMOS transistors used for accessing the nodes. In addition to the differential scheme, the proposed TG10T cell incorporates two additional buffer transistors to enhance read stability. Furthermore, the cell's design focuses on minimizing static power dissipation by utilizing more number of p-channel transistors. The

proposed cell renders better overall performance compared to other SRAMs which makes it appropriate for IoT applications.

- **“A reliable low standby power 10T SRAM cell with expanded static noise margins”, 2022**

E. Abbasian, F. Izadinasab, and M. Gholipour [30], proposed an SRAM cell that primarily focused on reducing power consumption during standby mode, or in other words the leakage power consumption. The proposed circuit consisted of 10 transistors. It also aimed to attain high read and write noise margins, emphasizing stability as a crucial aspect. The circuit's essential components are a Schmitt-trigger inverter with a pull-up transistor that is twice as long as other transistors and a cross-coupled inverter with stacked transistors. The design of the proposed SRAM cell includes an isolation mechanism that prevents disturbance to the stored data during a read operation by segregating the internal nodes away from the read path. The simulation results confirm the reduction in leakage power consumption achieved by the proposed design.

- **“A Novel Low-Power and Soft Error Recovery 10T SRAM Cell”, 2023**

C. Liu, H. Liu and J. Yang [31], proposed a 10T SRAM cell with the primary goal to decrease power consumption and increase resilience for soft error that may occur in the storage nodes. The innovation in the design is to add an extra PMOS transistor to facilitate full passage of logic ‘0’. Simulation results demonstrate that the power dissipation of the reported SRAM cell is significantly lower compared to other existing SRAM cell designs. Also, the resilience to soft-errors is proved. However, the shortcoming this proposed incurs is the increased area footprint because of the extra PMOS transistor used in the design.

- **“A reliable and temperature variation tolerant 7T SRAM cell with single bit line configuration for low voltage application”, 2022**

B. Rawat and P. Mittal [27], proposed a 7T cell which is of single-ended configuration. The reported cell demonstrates a satisfactory hold/read static noise margin, indicating its ability to maintain stable data storage and reliable read operations. The cell is architectured so that it is suited for low voltage applications. It uses just one bitline for each of the cell access

operations (read and write). The sturdiness of the suggested cell was validated using Monte Carlo analysis with respect to process and. The suggested cell was also contrasted with pre-existing SRAM cells in order to prove that it indeed is superior with regards to the performance indicating parameters. The simulation results validated that the power dissipation was found to be minimal in the proposed design. This is mainly accredited to the fact that performing read and write operation required a pulse width of a few nanoseconds. Thus, the proposed cell exhibited superiority when compared to its counterparts.

- **"A novel 8T SRAM cell with improved read-SNM", 2007**

A. Sil, S. Ghosh and M. Bayoumi [32] reported an SRAM cell that consisted of 8 transistors and primarily focused on enhancement of cell stability. It aims to eliminate the impact of noise during read operation. The simulation results indicated a very high Read Static Noise Margin (RSNM) value of 468 mV where the supply voltage was 1.2 V. It also achieved a low power consumption, which is achieved mainly because of the use of low voltage to pre-charge the bitlines, which is much lower than the supply voltages. But the major concern is that multi domain designs are always difficult to realise and involves many practical issues.

- **"A Single-Ended With Dynamic Feedback Control 8T Subthreshold SRAM Cell", 2015**

C. B. Kushwah and S. K. Vishvakarma [33] proposed an 8T SRAM cell that has improved data stability in subthreshold region. The cell designed by the researchers has a single ended architecture with dynamic feedback control. This innovative configuration allows an increase of write margin to almost 1.4 times compared to that of the traditional 6T SRAM architecture at 300 mV. The read and hold SNMs are fairly improved compared to other existing SRAM cell designs. Write access delay was also found to be better for this design. Additionally, write power is also minimized in comparison to other designs. Overall the design was proved to be more suitable for low power applications.

- **"Power-Gated 9T SRAM Cell for Low-Energy Operation", 2017**

T. W. Oh, H. Jeong, K. Kang, J. Park, Y. Yang and S. -O. Jung [34] proposed an SRAM cell consisting of 9 transistors that uses the power gating transistors to reduce power

consumptions. The proposed cell makes use of an access buffer that is decoupled from read path. The cell also focused on improving soft error immunity by using bit interleaving and a virtual ground for each column of SRAM array. The simulation results reveals an enhanced Read Static Noise Margin (RSNM).

- **"Single-Ended Subthreshold SRAM with Asymmetrical Write/Read-Assist", 2010**

M. -H. Tu, J. -Y. Lin, M. -C. Tsai, S. -J. Jou and C. -T. Chuang [37] proposed a novel 8T SRAM that makes use of a write assist scheme. It also uses a biasing technique that involves virtual ground. Additionally, it uses positive feedback sensing schemes. The main notion of the reported cell architecture is to improve the read and noise margins, and the access speeds. The architecture uses one bitline only for each of both read and write modes separately. The researchers assembled and array of 256x16 bits in order to test the cell's performances. The results proved that the read and write margins were improved significantly (up to 35% and 50% of supply voltage respectively).

- **"Single bit-line 11T SRAM cell for low power and improved stability", 2020**

R. Lorenzo and R. Pailly [38] reported an 11T SRAM cell. It aims to achieve a minimal leakage power and improved write performance by making use of the innovation of power gating transistors and transmission gates. It also looks to resolve the issue of half select disturbance by using a virtual ground signal for a common row. This eliminates the undesired discharge of bitline in an accessed row, which results in decrease energy consumption. The model is compared to other existing SRAM cells of varying transistor counts starting from 6T to 9T to validate its parameters' performances. The simulation findigns revealed a notable enhancement in read static noise margins and write margins and a significant improvement in read and write delays.

- **"An 8T low-voltage and low-leakage half-selection disturb-free SRAM using bulk-CMOS and FinFETs", 2014**

G. Pasandi and S. M. Fakhraie [39] proposed an 8T SRAM cell designed for low leakage power consumption. It is found to be functional at low supply voltages. It also focuses on making the SRAM cell array free from half- select disturbances during write operations by

using a novel internal write-back technique. The simulation results also revealed an improvement of 0.58 and 0.67 in read and write power. The researchers also design the SRAM cell on FinFET technology because of which the simulation results showed that the FinFET variant is less sensitive to variations and also recorded a significant improvement (about twice) in Read SNM.

2.2 REVIEW FOR PARAMETERS OF DIFFERENT SRAM CELLS

In the two tables given below, the existing SRAM cell architectures that have been reviewed in this section are presented in a tabular column that summarises the measure of parameters of the cells. The cells are grouped into two broad classes, one class with differential ended design and the other with single ended design.

Table 2.1: Parametric analysis of various differential ended SRAM cells

S. No.	Authors	Transistor count	Technology node	Supply Voltage	Access Delay	Leakage power	SNM (RSNM/HSNM/WM) (in mV)
1.	Tripathi *et al.* [17]	6	45nm	0.8 V	-	126.93 pW	41.25/32.67/130.33
2.	Pathak *et al.* [18]	6	45 nm	0.8 V	11.4 pS	5.68 pW	-/-/205
3.	Tripathi *et al.* [19]	8	55 nm	0.6 V	-	80 pW	59.94/45.32/176.98
4.	Giterman *et al.* [23]	8	65 nm	1.2 V	-	2.808 nW	205/460/445
5.	Lin *et al.* [5]	9	32 nm	0.6 V	82.04 pS	-	-
6.	Krishna *et al.* [28]	10	32 nm	1 V	916.7 pS	9.37 pW	201/-/463
7.	Abbasian *et al.* [29]	10	16 nm	0.36 V	340 pS	1.15 nW	29.8/87.3/-
8.	Abbasian *et al.* [30]	10	16 nm	0.7 V	299 pS	11.79 nW	225.5/225.5/356.6

9.	Liu *et al*. [31]	10	22 nm	0.8 V	17.9 pS	2.92 nW	340/510/270

Table 2.1 showcases all the differential ended SRAM cells with measurements of important performance indicating parameters. It also highlights the number of transistors used in the design, the technology node used and the supply voltage in which the circuit operates.

Table 2.2: Parametric analysis of various single ended SRAM cells

S. No.	Authors	Transistor count	Technology node	Supply Voltage	Access Delay	Leakage power	SNM (RSNM/HSNM/WM) (in mV)
1.	Mehrabi *et al.* [20]	7	90 nm	0.5 V	175.525 pS	11 nW	155/-/250
2.	Rawat *et al.* [21]	7	32 nm	0.3 V	-	8.4 pW	90/90/190
3.	Rawat *et al.* [22]	7	32 nm	0.8 V	72.5 pS	256 pW	324/324/428
4.	Rawat *et al.* [27]	7	32 nm	0.3 V	-	2 pW	94/94/150
5.	Sil et al. [32]	8	120 nm	1.2 V	562 pS	20.4 nW	468/468/-
6.	Kushwah *et al.* [33]	8	90 nm	0.5 V	650 pS	28.86 nW	85/151/400
7.	Oh *et al.* [34]	9	22 nm (FinFET)	0.32 V	256 nS	0.74 µW	164/-/-
8.	Tu *et al.* [37]	8	90 nm	0.5 V	-	-	198/-/170
9.	Lorenzo *et al*. [38]	11	65 nm	1.2	778.3 pS	46.42 nW	179/179/331
10.	Pasandi *et al.* [39]	8	90 nm	0.5 V	305 pS	18.77 nW	59/179/226.5

Table 2.2 showcases all the single ended SRAM cells in a tabular format. It consists of measurements of important performance indicating parameters and also highlights the number of transistors used in the design, the technology node used and the supply voltage in which the circuit operates.

2.2 RESEARCH GAP

After an extensive review of several previously reported works in the domain of SRAM design, some notable conclusions can be drawn.

- First, is the report of very few number of designs that excels in all parameters, majority of the designs perform excellently well in some parameter but fall behind in one or the other parameter. For instance, the Read Static Noise Margin may be very large in one model, but the Write Margin would be found to be very low for writing 0 or 1 or both.
- Instead of having only one of the noise margins at the excellent level and the other noise margins at a barely acceptable level, it would be better to have all the noise margin parameters at an optimal level. In some cases, even when all the noise margins are at optimal value, the power consumption would be very high.
- Now, some researchers may have found a way to get a good performance on all parameters but they have resorted to use more number of transistors, some reaching 11 or 12 transistors. This would mean more area overhead, and hence less dense SRAM arrays, which is non-desirable. So it is about managing the trade-off between a perfect all-round performance and a high transistor count SRAM cell.

So, in this thesis work, after having gathered knowledge and information from the extensive review to understand how a specific design affects the performance of a specific parameter, we look to find a way to design an SRAM cell architecture that has a robust, good and balanced all-round performance in every parameter but still maintain the transistor count to a fairly acceptable number. The design process stems from taking motivation from some existing SRAM cell designs that provides an enhanced performance in parameter or the other, and finding a way to club together the design innovations, at the same time putting our own innovation in the design.

CHAPTER 3

PARAMETRIC EXTRACTION AND PERFORMANCE ANALYSIS OF EXISTING SRAM CELLS

Several SRAM architectures have been proposed by researchers that concentrate on varying features. Some of them that focused on stability of data stored, power consumption, invariance to temperature and supply voltage and access speed is being discussed here. All of them were simulated using the same peripheral circuits to get fair and just results across all SRAM cell designs.

This chapter is organised into 3 main sections. Section 3.1 presents the architecture of different existing SRAM cells. Section 3.2 describes the process of parameter extraction of the considered SRAM cells. Section 3.3 gives an overall summary of the results obtained from the above two sections. The performance analysis process includes simulation of the SRAM cells to examine their working and actually see their performances with regards to some important parameters.

3.1 ARCHITECTURE OF DIFFERENT EXISTING SRAM CELLS

3.1.1 Conventional 6T SRAM cell

The main purpose of an SRAM Cell is to retain a bit of data, either 0 or 1, given that power supply is not cut off. At the same time, it should allow the data stored to be read and also be replaced by another bit written into the cell. The conventional 6T SRAM cell is the most prevalent SRAM cell architecture and has been widely used for a long time. As illustrated in Fig. 3.5, it comprises of a cross coupled inverter (P1, N1 & P2, N2) whose primary function is to retain the data. Then there are two bitlines called Bitline (BL) and Bitline_bar (BLB) that are used to get access to the data from the cell or to transfer data onto the cell via the access transistors (N3 and N4).

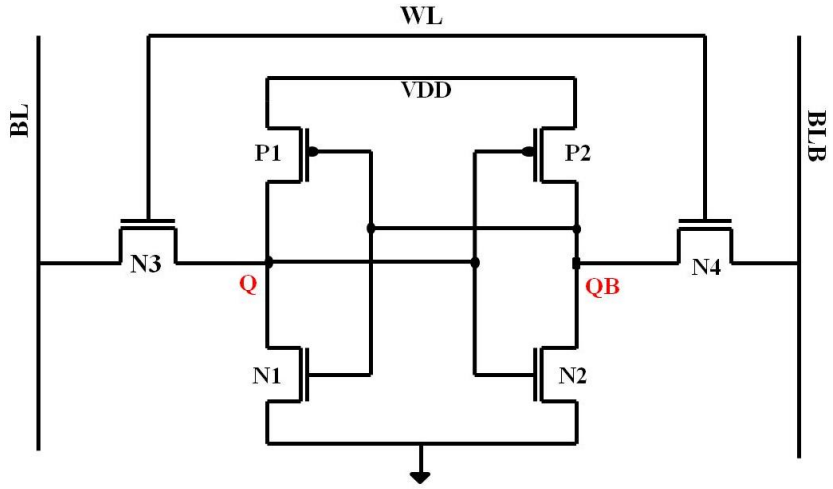


Fig. 3.1: Schematic of Conventional 6T cell (Reproduced from [1])

Write Operation:

To begin writing onto the cell, the bitline (BL) and bitline bar (BLB) are initially set to the data bit and its complement, respectively. Subsequently, the wordline (WL) is activated by setting it high, which activates the access transistors (N3 & N4). This enables forcing the data onto the two nodes of the weak cross-coupled inverter.

Read Operation:

To begin the process of accessing data from the cell, the bitline (BL) and the bitline bar (BLB) are charged up to V_{DD} with the help of a precharge circuit, then the wordline (WL) is set high to turn on the access transistors N3 and N4, so that one among the BL and BLB is discharged to ground according to the data present on the internal nodes.

Hold Operation:

To hold the stored data in the cell, the transistors N3 & N4 are kept in inactive mode by giving the wordline (WL) a low voltage.

Read Stability and Writability:

To ensure correct reading and writing of data onto the cell, two constraints need to be followed. The first constraint is the *read stability* constraint, which requires that the driver

transistors (N1 & N2) should have more strength than the access transistors (N3 & N4). This ensures that during the read operation, the current flowing through the access transistors does not raise the voltage of the node that should be low. The second constraint is the *writability* constraint, which states that the access transistors (N3 and N4) should be stronger than the pull-up transistors (P1 and P2). This allows for proper writing of data by ensuring that the weaker pull-up transistor allows the desired node to be forced to the desired voltage level. Table 3.1 provides the aspect ratios of the transistor sizes for the conventional 6T SRAM cell, satisfying these constraints.

Table 3.1 – Transistor sizing of conventional 6T SRAM cell

Transistors	**Width (W)**	**Length (L)**
P1, P2 (Pull-up transistors)	150 nm	100 nm
N1, N2 (Pull-down transistors)	400 nm	100 nm
N3, N4 (Access Transistors)	200 nm	100 nm

Complications in 6T SRAM cell

The conventional 6T cell, although simple and symmetric, has some limitations. One of the shortcomings is the lack of robustness, as the direct access of the storage nodes by the bitlines can lead to voltage division and potential disturbance of the stored data during a read operation, known as *destructive read*. Another concern is the leakage or static power consumption, which becomes more significant as SRAM cells are used in cache memories and as supply voltages are reduced due to technology scaling and power reduction goals. Addressing these issues becomes crucial for improving the performance and power efficiency of SRAM cells.

3.1.2 7T SRAM Cell

With the intention to solve these problems, an SRAM cell comprising of 7 transistors was reported by Tawfik & Kursun [2]. The circuit schematic of the 7T SRAM cell is represented in Fig. 3.2. It is a dual port and single ended SRAM cell. It makes use of one bitline to execute each of read or write processes (RBLB and WBL respectively), hence called single ended and dual port because it has separate ports for each of read and write operations [43].

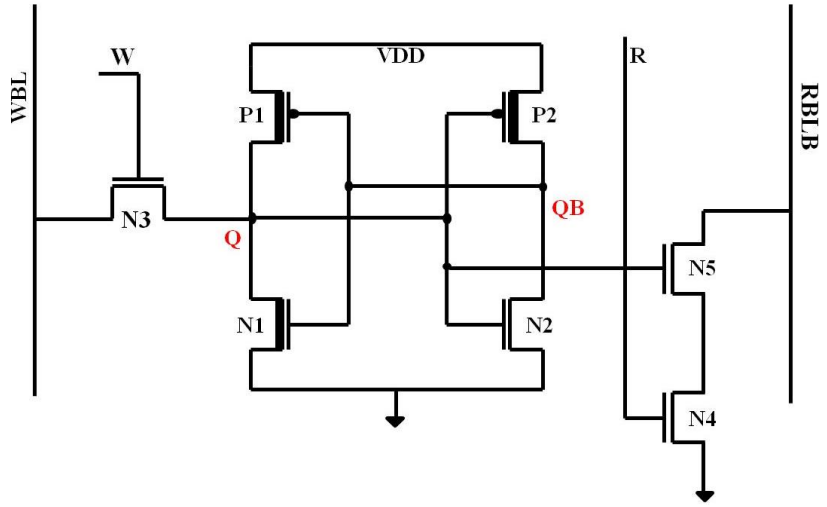


Fig. 3.2: Schematic of 7T SRAM cell (Reproduced from [2])

Table 3.2 gives the aspect ratios of the transistors sizes of the 7T SRAM cell as was followed by the researchers that proposed this model.

Table 3.2 – Transistor sizing of 7T SRAM cell

Transistors	**Width (W)**	**Length (L)**
P1, P2 (Pull-up transistors)	150 nm	100 nm
N1, N2 (Pull-down transistors)	150 nm	100 nm
N3 (Write access transistor)	150 nm	100 nm
N4, N5 (Stacked NMOS in read port)	300 nm	100 nm

The main innovation in this architecture is the separation of read and write bitlines denoted by RBLB and WBL respectively. It uses a normal access transistor (N3) to facilitate write operation, whereas, to perform read operation, an isolated read port is used that comprises of two stacked NMOS transistors (denoted by N1 & N2) [43]. As a result, the reported cell architecture minimizes disturbance during read process, causing a substantial enhancement in the Read Static Noise Margin (RSNM). Due to this read port configuration, the number of transistors in the critical read delay route is reduced leading to increase in access speed. It also uses dual threshold voltage transistors (indicated by thick MOSFET

symbols in schematic, PU1, PU2 and PD1) to control the leakage power consumption. This can be explained using the mathematical equation that governs the current in off state.

$$I_{OFF} = I_S . e^{\frac{q(V_{GS} - V_T - V_{offset})}{nKT}} (1 - e^{\frac{-qV_{DS}}{KT}}) \quad (3.1)$$

Where, V_T = Threshold Voltage, and

$$P_{static} = I_{OFF} . V_{DD} \quad (3.2)$$

As evident from equation (3.1), an increase in V_T results in a significant reduction in the off-state current, also known as subthreshold current. Consequently, this decrease in subthreshold current results in a substantial reduction in static power consumption, as indicated by equation (3.2).

Write Operation:

To write onto the cell, the Write Bitline (WBL) is first charged upto to V_{DD}, then the Write (W) signal is kept at logic '1', while Read (R) signal is set at logic '0'. Now if the input data to be written is a '1', the WBL remains charged to V_{DD} and thus the data logic '1' is forced to the node Q via the low V_T access transistor N3 (for easy write process). Alternatively, if the input data to be written is a '0', the WBL is discharged to GND and thus the bit '0' is force to node Q via N3 [43]. It should be noted here that WBL is required to be precharged to V_{DD} every time regardless of whether the input data is 0 or 1 because of the fact that the write driver that are used in every memory circuitry can only do the job of pulling down the WBL to GND via the control of Write (W) signal and input signal D.

Read Operation:

To begin the process of accessing data from the cell, first the read bitline bar (RBLB) is precharged to V_{DD}, then the read (R) signal is set high, while write (W) signal is set low so that N4 is ON. Now since N5 is directly connected to Q, if a '1' was stored on Q (which means the cell), N5 would become ON and the RBLB will be discharged to GND via the series stacked transistors N5 and N4. On the other hand, if a '0' was stored on Q, the RBLB will stay charged (high). So the RBLB reads a complement of the bit stored on the cell, and hence the name. Because of the architecture, the internal nodes Q and QB are segregated

away from the read bitline bar, since the internal nodes are not freely accessed by the bitline as was the case in conventional SRAM cell. This enhances the stability of the proposed SRAM cell during read mode. Also, the read bitline bar is provisionally discharged via the transistor stack with the data on storage node acting as one of the control signals. So, the pull up and the driver transistors of the back-to-back inverter does not take part in the critical read delay path and hence their sizing does not affect the read delay [43].

Hold Operation:

To hold the stored data in an undisturbed manner, both the read (R) and write signals (W) are kept low so that the read port and the write access transistor remains inactive. As a consequence, the data present at the internal nodes Q and QB remains intact and undistorted, preserving its state just prior to entering the hold mode.

3.1.3 Standard 8T SRAM Cell

To tackle the degradation in write performance, one of the solutions is to use two bitlines (bitline and bitline_bar) for write operation while keeping the isolated read port untouched. This led to introduction of an 8T SRAM cell by Calhoun & Chandrakasan [3] as illustrated in Fig. 3.18.

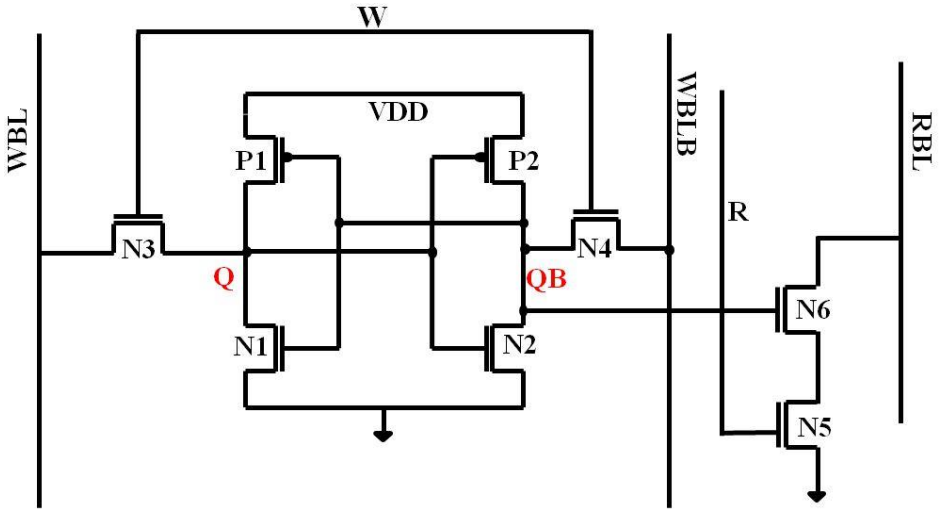


Fig. 3.3: Schematic of standard 8T SRAM (Reproduced from [3])

The architecture utilizes a single-ended configuration for read mode and a differential-ended configuration for write mode, meaning only one bitline is used for performing read operation whereas two complementary bitlines are used for performing write operations. Its write operation is similar to that in a conventional 6T SRAM cell. For read operation, it uses a read port that is isolated from the storage node. The read port comprises of two stacked NMOS transistors. By minimizing disturbance to the data present in the internal nodes during a read operation, the SRAM design ensures the maintenance of an enhanced Read Static Noise Margin (RSNM). Due to this read port configuration, the number of transistors in the critical read delay route is reduced leading to increase in access speed. The use of two bitlines to perform write operation leads to a more improved and a symmetric write performance. Table 3.3 gives the aspect ratios of the transistors sizes of the standard 8T SRAM cell as was followed by the researchers that proposed this model.

Table 3.3 – Transistor sizing of standard 8T SRAM cell

Transistors	**Width (W)**	**Length (L)**
P1, P2 (Pull-up transistors)	150 nm	100 nm
N1, N2 (Pull-down transistors)	150 nm	100 nm
N3, N4 (Write access transistor)	150 nm	100 nm
N5, N6 (Stacked NMOS in read port)	300 nm	100 nm

Write Operation:

Performing a write operation onto the cell would begin with setting the write bitline (WBL) and the write bitline bar (WBLB) equal to the data bit and its complement respectively. Then the write signal (W) is set to logic ‘1’ to turn on the access transistors (N3 and N4), so as to force the data on the two nodes of the weak cross coupled inverter.

Read Operation:

Performing a read operation would begin with precharging the read bitline bar (RBL) to V_{DD}. Then the read (R) signal is set high, while write (W) signal is set low so that N4 and N3 are turned OFF and N5 is turned ON. Now since N6 is directly connected to QB, if a ‘1’ was

stored on QB (meaning a ‘0’ stored in Q), N6 would become ON and the Read Bitline will be discharged to GND via the series stacked transistors N5 and N4. On the other hand, if a ‘0’ was stored on Q, the RBL will stay charged (high). So the RBL reads the value of the bit stored on node Q successfully. Because of the architecture, the storage nodes Q and QB are segregated away from the read bitline bar, since the nodes are not directly accessed by the bitline as was the case in conventional cell. This enhances the stability of the proposed SRAM cell during read mode. Also, the read bitline bar is conditionally discharged through the transistor stack with the data on storage node acting as one of the control signals. So, the pull-up and the driver transistors of the back-to-back inverter does not take part in the critical read delay path and hence their sizing does not affect the read delay.

Hold Operation:

To maintain the stored data without any disturbance, both the read (R) and write (W) signals are kept at logic ‘0’ so that the read port and the write access transistors remains inactive. As a consequence, the information bit present at the internal nodes Q and QB remains intact and undistorted, preserving its state just prior to entering the hold mode.

Complications in standard 8T SRAM cell:

The use of two bitlines during write mode increased the Write SNM upto the optimal value but led to huge reductions in read and hold stability of data in the cell. Increase in write delay and power consumption and area footprint was also observed. All these adverse effects were majorly due to the addition of an extra transistor and an extra bitline to enable differential write operation**.**

3.1.4 Transmission Gate Based 8T SRAM Cell

The SRAM cell architecture was proposed by Roy C and Islam A [4]. The schematic of the SRAM cell is shown in Fig. 3.4.

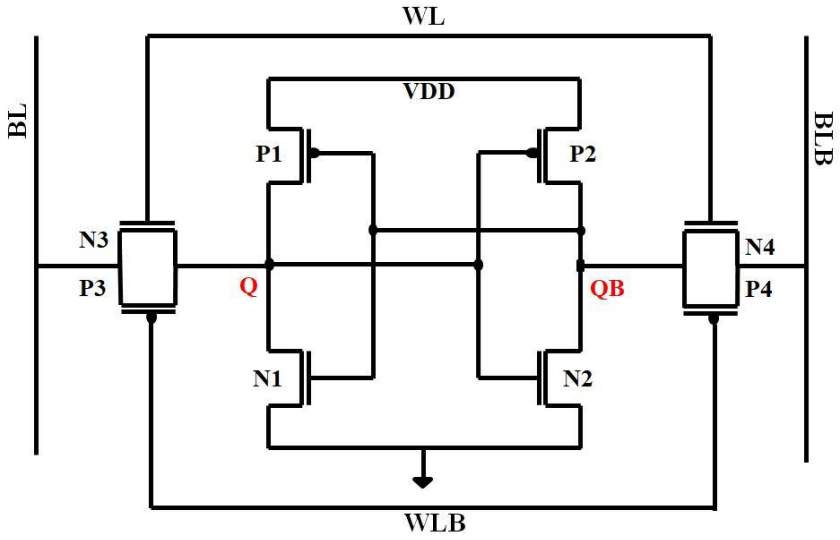


Fig. 3.4 Schematic of transmission gate based 8T SRAM cell (Reproduced from [4])

The architecture is very similar to that of the conventional 6T SRAM cell. The primary distinction here is the presence of transmission gates instead of the NMOS transistors as the device used to access the storage nodes. The transmission gate consists of parallel NMOS and PMOS transistors, serving as a bidirectional signal transmission device cell. So, it can allow transfer strong logic high and logic low, thus eliminating the problem of passing a weak 1 by the NMOS access transistors. Due to the usage of complementary pass gates, its write access time is hugely improved and the write stability is also enhanced. The cell is also design to consume low leakage power. Table 3.4 gives the aspect ratios of the transistors sizes of the standard 8T SRAM cell as was followed by researchers that proposed this model.

Table 3.4 – Transistor sizing of transmission gate based 8T SRAM cell

Transistors	**Width (W)**	**Length (L)**
P1, P2 (Pull-up transistors)	150 nm	100 nm
N1, N2 (Pull-down transistors)	300 nm	100 nm
N3, N4 (Transmission gate NMOS transistors)	225 nm	100 nm
P3, P4 (Transmission gate PMOS transistors)	225 nm	100 nm

Write Operation:

A write operation begins with setting the bitline (BL) and the bitline bar (BLB) equal to the data bit and its complement respectively. To activate the two transmission gates and control the data flow, the wordline (W) signal is set high, while the complementary wordline (W_bar) signal is set low, thereby forcing the data onto the two nodes of the weak cross-coupled inverter in the SRAM cell.

Read Operation:

A read operation begins with precharging the bitline (BL) and bitline bar (BLB) to V_{DD} to enable access to the internal nodes Q and QB, the wordline (W) signal is set high, while the complementary wordline (W_bar) signal is set low. One of bitline or bitline_bar is discharged to ground. Thus data at Q and QB are transferred onto the two complementary bitlines.

Hold Operation:

To hold the stored data in an undisturbed manner, wordline (W) and the wordline_bar (W) signals are set low and high respectively so that the storage nodes Q and QB are not accessible to the bitlines. Thus, data stored at the internal nodes Q and QB remains undistorted as it was just before the hold mode began.

3.1.5 9T SRAM cell

An SRAM cell comprising of 9 transistors was proposed by Sheng Lin, Yong-Bin Kim, and Fabrizio Lombardi. It uses two bitlines (bitline and bitline_bar) for write operation and a separate read port consisting of a stack of three transistors. The cell is particularly design to achieve low leakage power consumption. Fig. 3.5 illustrates the circuit diagram of the 9T SRAM cell.

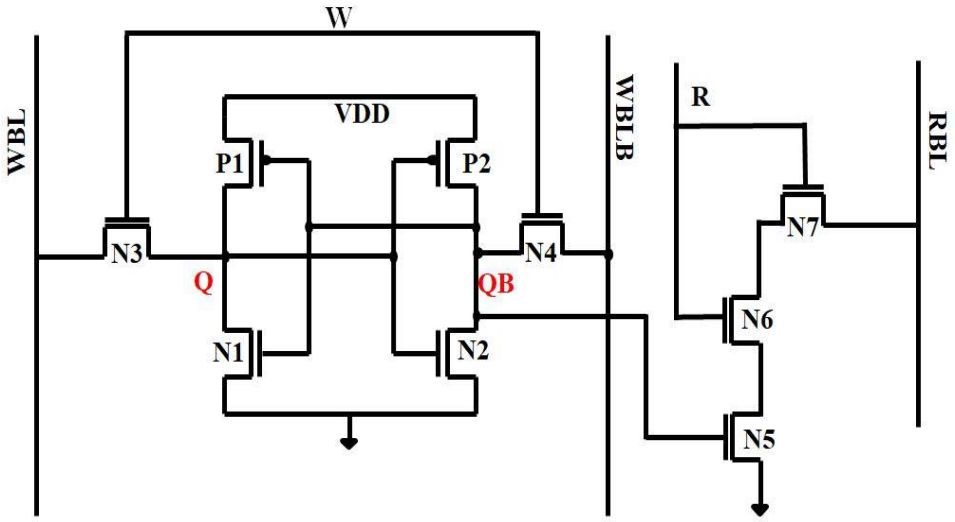


Fig. 3.5 Schematic of 9T SRAM cell (Reproduced from [5])

The architecture of the 9T SRAM cell is designed to use only one bitline for read operations and use two complementary bitlines for write operations. The stack of three transistros in the read port serves two main purposes. First, enhanced noise margin during read operations is achieved in the 9T SRAM cell through the isolation of read bitlines from the storage nodes. Second, the stacking effect enabled by the presence of three NMOS transistors is the main factor for the minimized leakage power consumption. Table 3.5 gives the aspect ratios of the transistors sizes of the standard 8T SRAM cell as was followed by authors that proposed this model.

Table 3.5 – Transistor sizing of 9T SRAM cell

Transistors	**Width (W)**	**Length (L)**
P1, P2 (Pull-up transistors)	150 nm	100 nm
N1, N2 (Pull-down transistors)	150 nm	100 nm
N3, N4 (Access transistors)	150 nm	100 nm
N5, N6, N7 (stacked NMOS in read port)	300 nm	100 nm

Write Operation:

Performing a write operation onto the cell would begin with setting the write bitline (WBL) and the write bitline bar (WBLB) equal to the data bit and its complement respectively. Then the write signal (W) is set at logic '1' to turn ON the access transistors (N3 and N4), so as to force the data on the two nodes of the weak cross coupled inverter.

Read Operation:

Performing a read operation would begin with precharging the read bitline (RBL) to V_{DD}. Then the read (R) signal is set high, while write (W) signal is set low so that N4 and N3 are turned OFF and N6 and N7 are turned ON. Now since N5 is directly connected to QB, if a '1' was stored on QB (meaning a '0' stored in Q), N5 would become ON and the RBL will be cleared to GND via the series stacked transistors N5, N6 and N7. On the other hand, if a '0' was stored on Q, the RBL will stay charged (high). So the RBL reads the value of the bit stored on node Q successfully. Because of the architecture, the internal nodes Q and QB are segregated away from the read bitline bar, since the nodes are not directly accessed by the bitline as was the case in conventional SRAM cell consisting of 6 transistors. This enhances the stability of the proposed SRAM cell during read mode. Also, the read bitline bar is provisionally discharged through the transistor stack with the data on storage node acting as one of the control signals. So, the pull-up and the driver transistors of the back-to-back inverter does not take part in the critical read delay path and hence their sizing does not affect the read delay.

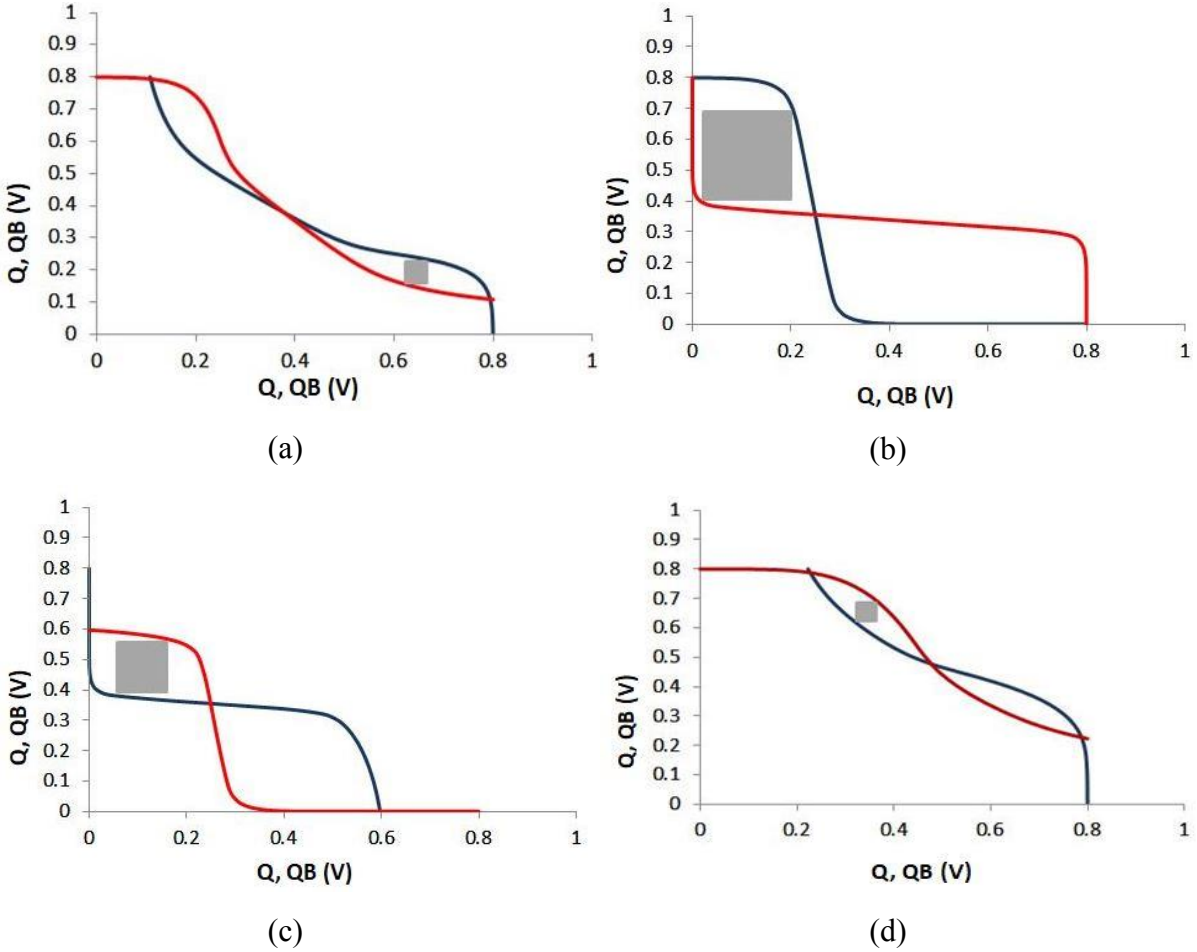
Hold Operation:

To hold the stored data in an undisturbed manner, both the read (R) and write signals (W) are kept low so that the read port and the write access transistors remains inactive. Thus, the data present at the internal nodes, Q and QB remains undistorted as it was just before the hold mode began.

3.2 PARAMETER EXTRACTION OF DIFFERENT EXISTING SRAM CELLS

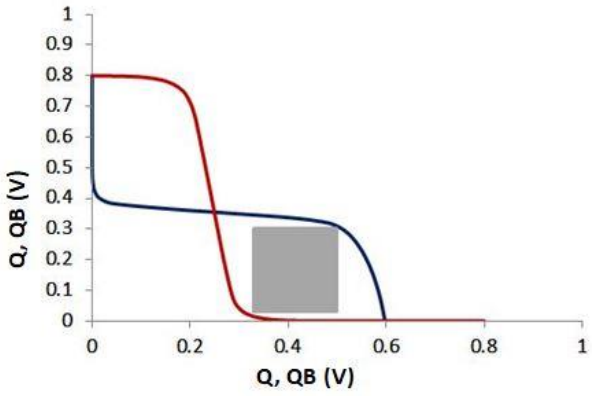
3.2.1 Read Static Noise Margin (RSNM):

RSNM is measured by using a graph called butterfly curves. While the reading process of the SRAM cell is in progress, the voltage transfer characteristics are formed by the combination of the voltage transfer characteristics curve of one inverter and the voltage transfer characteristics curve of the other inverter in the back-to-back configuration [36]. The RSNM, which represents the Read Static Noise Margin, is determined by the length of side of the largest square that can be present within the smaller hemisphere of the butterfly curve. Fig. 3.6 displays the butterfly curves utilized for RSNM measurement in different types of SRAM cells



(a) (b)

(c) (d)

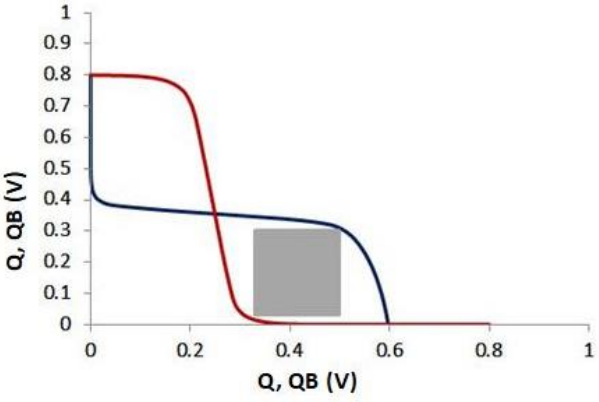


(e)

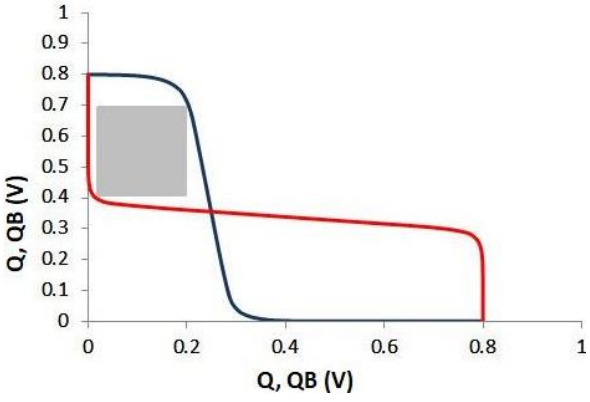
Fig. 3.6: Butterfly diagrams used to measure RSNM of (a) 6T SRAM, (b) 7T SRAM, (c) 8TS SRAM, (d) 8TTG SRAM, (e) 9T SRAM

3.2.2 Hold Static Noise Margin (HSNM):

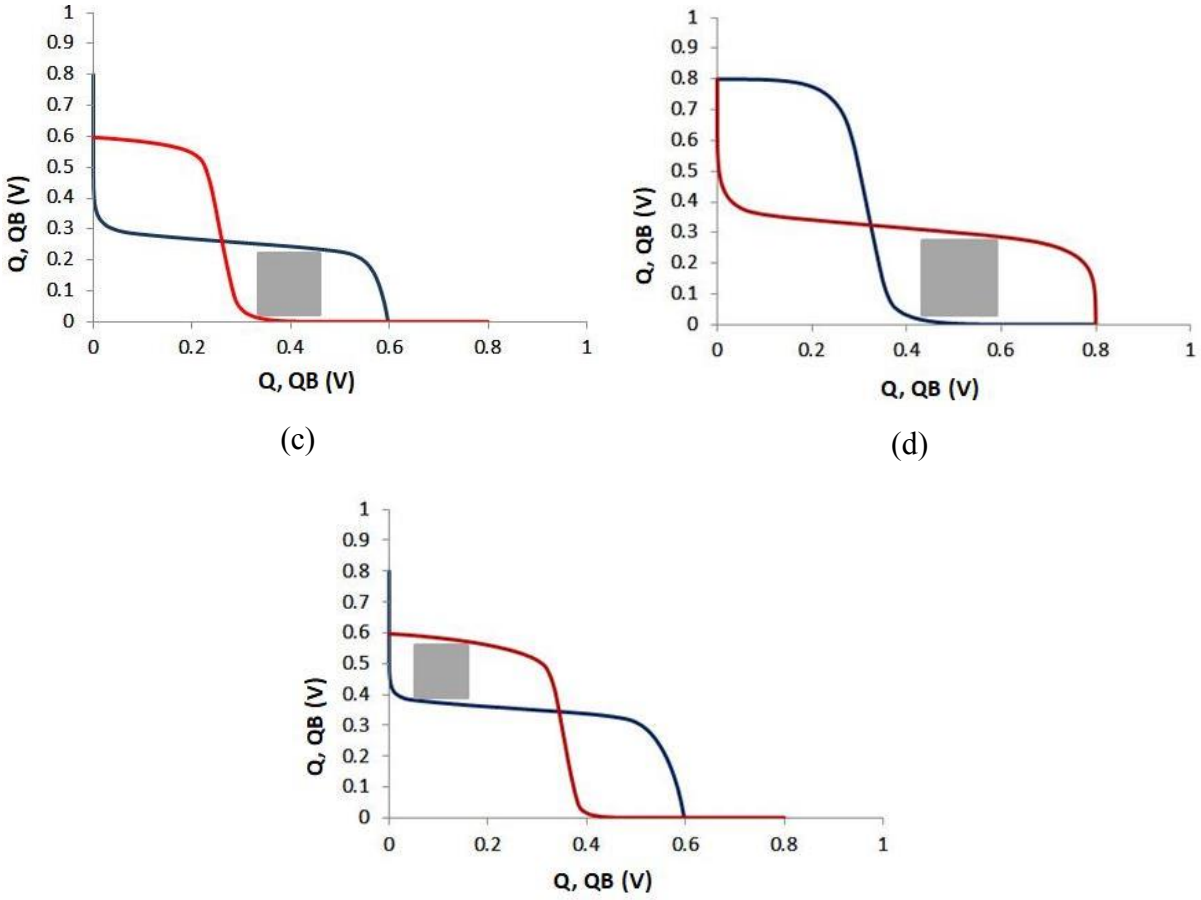
It is also calculated using the same butterfly curve approach as mentioned above. The only difference is that required write signal in each of the SRAM cells is kept at logic '0' so that the access transistors are inactive when the voltage at Q or QB is varied from 0 to V_{DD}. The supply voltage is kept at 0.8V for all the cells. The butterfly curves that give the HSNM value for all the considered SRAM designs is shown in Fig. 3.7.



(a)



(b)



(c) (d)

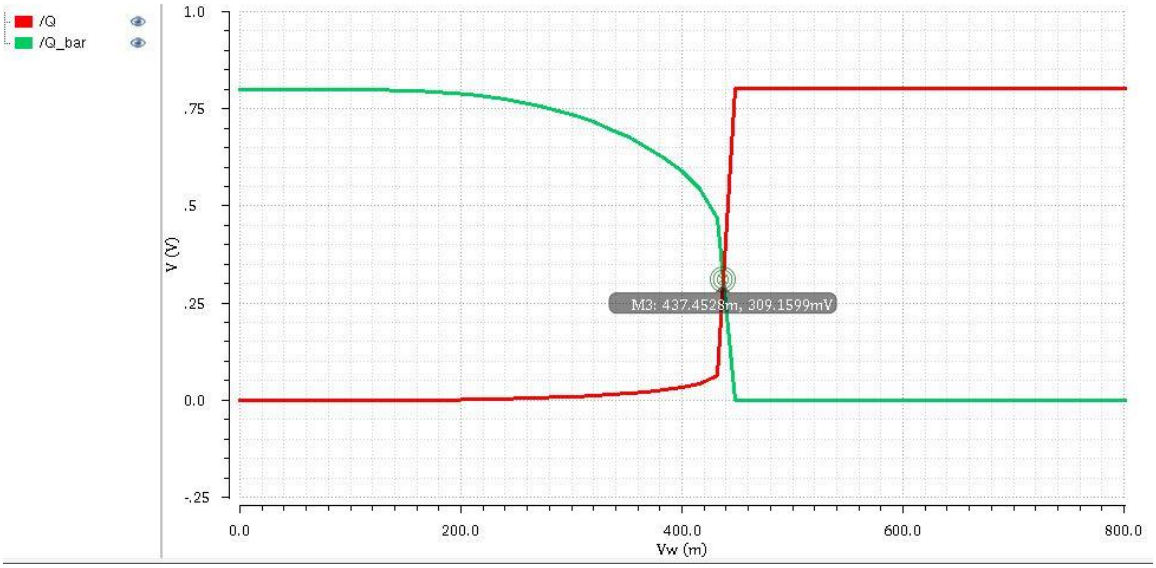
(e)

Fig. 3.7: Butterfly diagrams used to measure HSNM of (a) 6T SRAM, (b) 7T SRAM, (c) 8TS SRAM, (d) 8TTG SRAM, (e) 9T SRAM

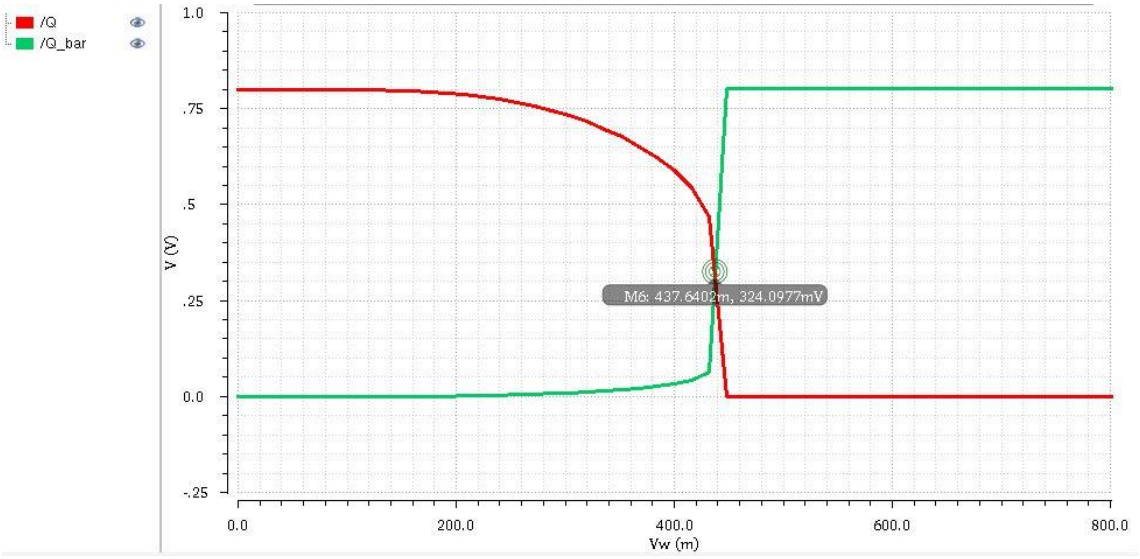
3.2.3 Write Margin (WM):

Write Margin is a little different from RSNM and HSNM. The meaning of writing into the cell is to overwrite the value at the storage nodes. So, the write performance is quantified by Write Margin (WM). Write Margins were calculated using the approach given by Aslam & Hassan [7]. It is calculated as the voltage difference between V_{DD} and the Word Signal (W) voltage at which the data at the storage node is flipped, assuming voltage at W increased from 0 till V_{DD} [7]. WM for an SRAM should be ideally $V_{DD}/2$. So, how good an SRAM cell with regards to write performance is determined by how close it is the $V_{DD}/2$. If it is too low, it means that it would be very difficult to write onto the cell. If it is very high, it means that it would be very easy to for noise to affect the write operation, and a small amount of noise can

invert the data present in the storage nodes. Write Margin is of two types: Write-1 Margin, Write-0 Margin. The V_{DD} used for calculating WM for all the cells is 0.8V.



(a)

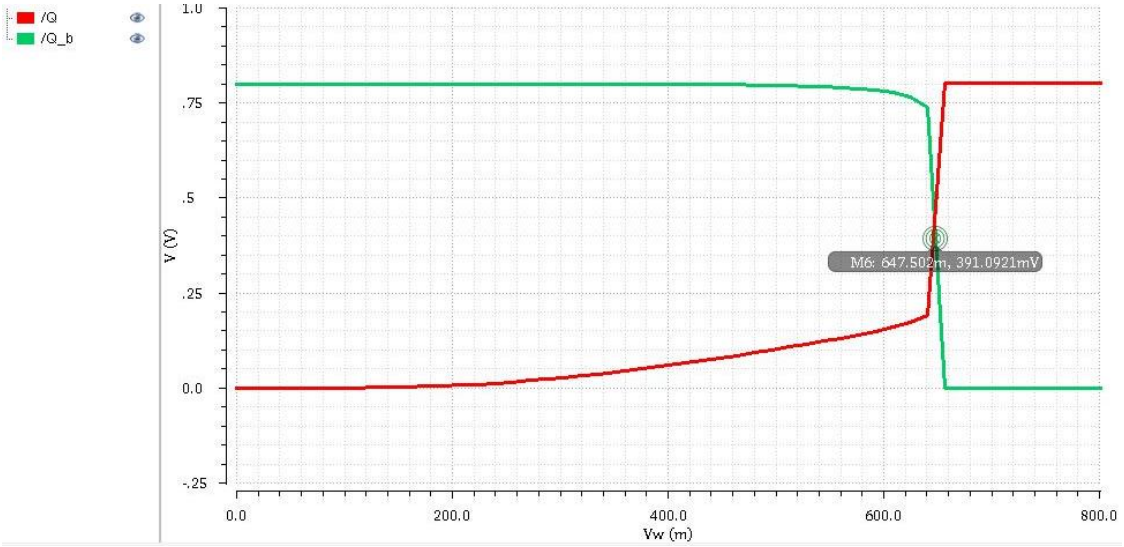


(b)

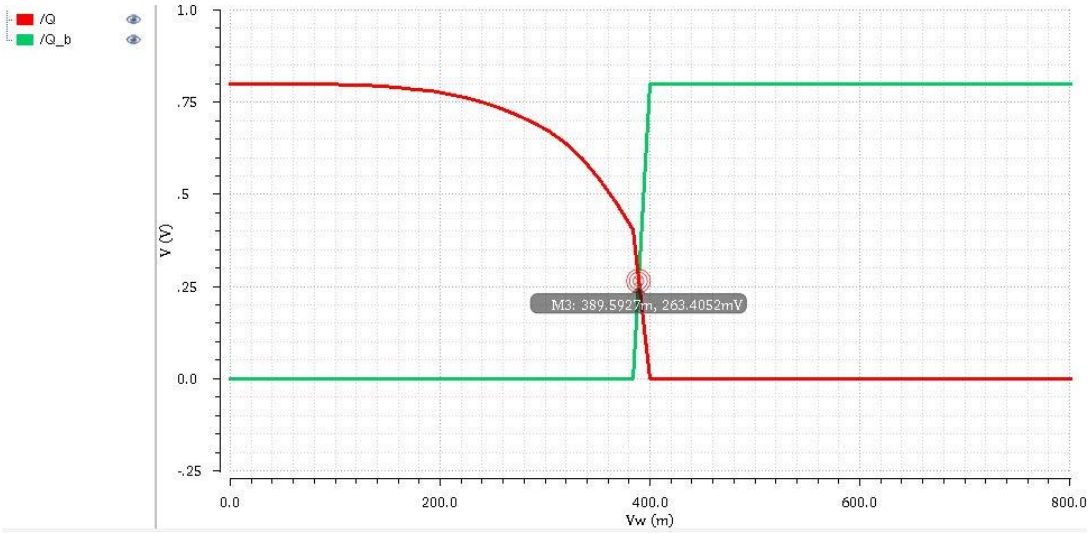
Fig. 3.8: (a) Write-1 Margin and (b) Write-0 Margin for 6T SRAM cell

The graphical curve used to find out write-1 margin and write-0 margin for conventional 6T SRAM cell is shown in Fig. 3.8. So, the write-1 margin and the write-0 margin are the same

because of the symmetrical architectural configuration in the 6T SRAM cell. Write and margins of the cell (both for writing '1' and '0') is (800 – 437.62) mV is 362.548 mV.



(a)

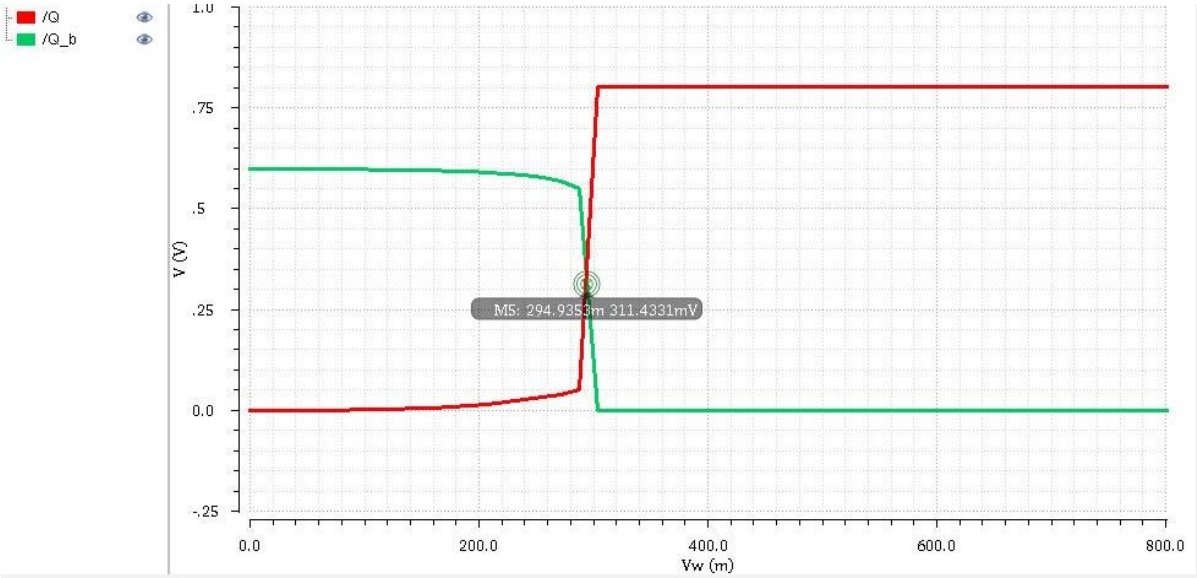


(b)

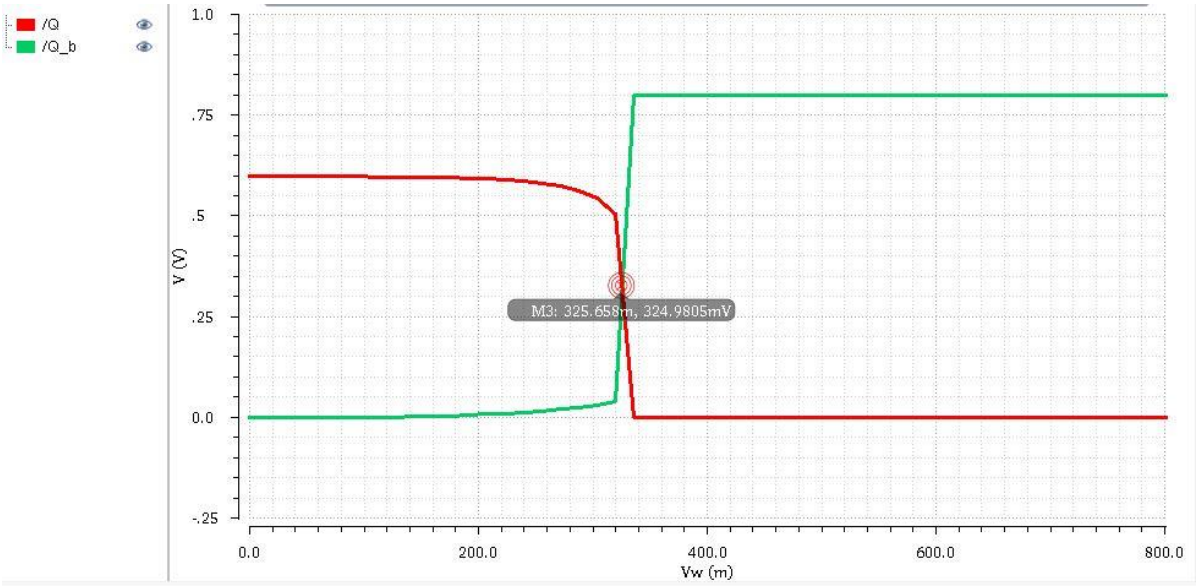
Fig. 3.9: (a) Write-1 Margin, (b) Write-0 Margin for 7T SRAM cell

The graphical curve used to find out write margins (both for writing 0 and 1) for the 7T cell is illustrated in Fig. 3.9. So, the write-1 margin and the write-0 margin are not the same because of the unsymmetrical configuration of transistors in the 7T SRAM cell. The value of

write-1 margin is (800-647.5) = 152.5 mV and that of write-0 margin is (800 – 389.592) = 410.48 mV.



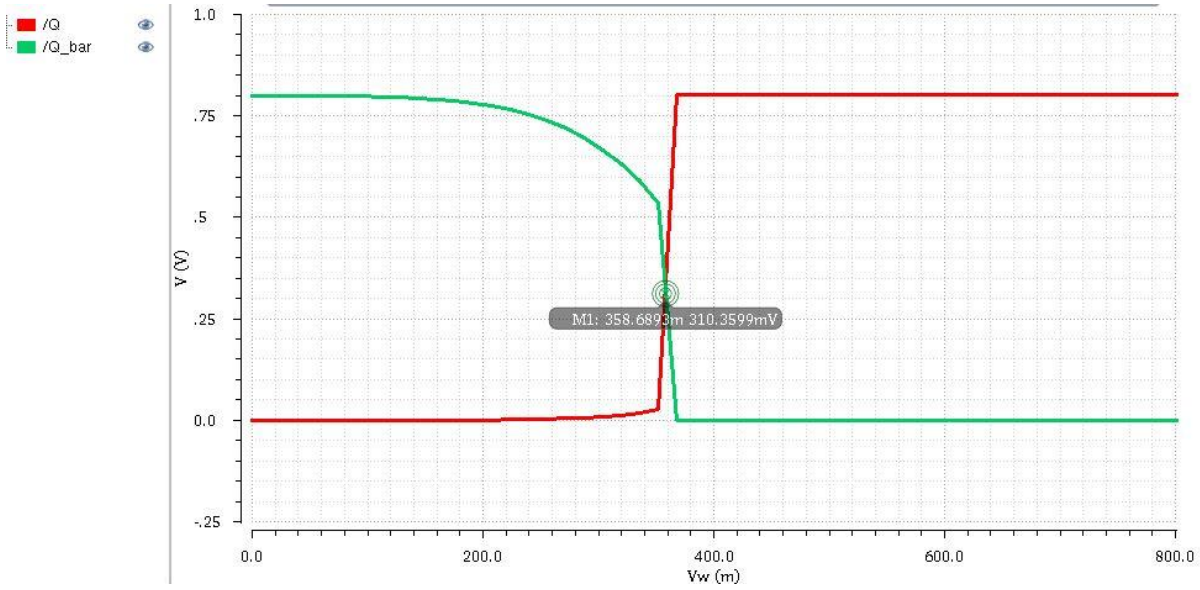
(a)



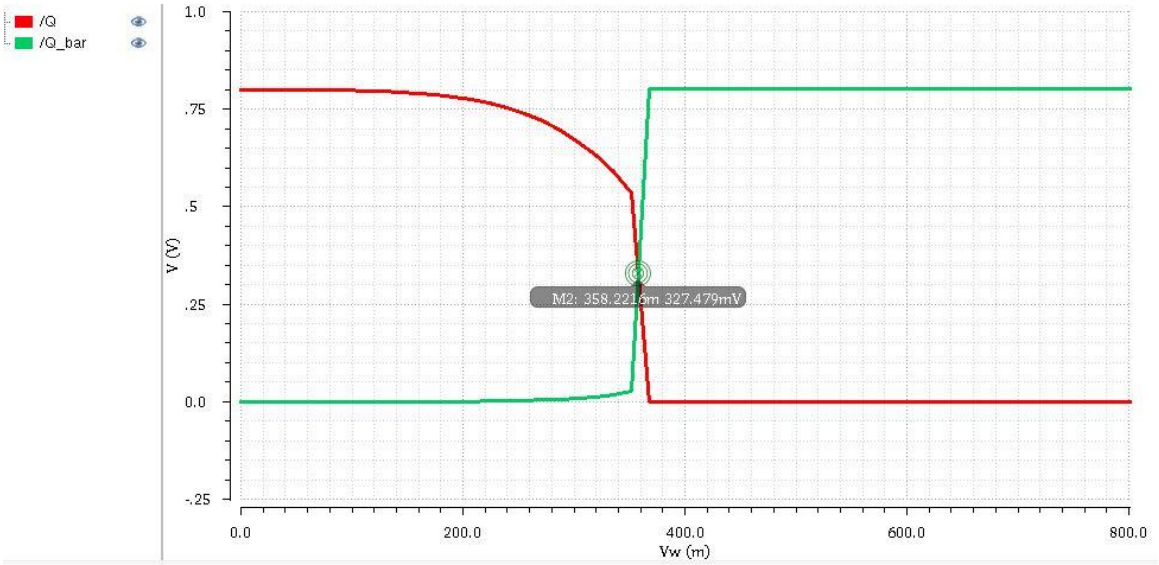
(b)

Fig. 3.10: (a) Write-1 Margin, (b) Write-0 Margin for standard 8T SRAM cell

The graphical curve used to find out write margins (both for writing 0 and 1) for the standard 8T SRAM cell is shown in Fig. 3.10. Write-1 margin of the cell is (800-294.9) = 505.1 mV and that of write-1 margin is (800 – 325.65) = 473.58 mV.



(a)

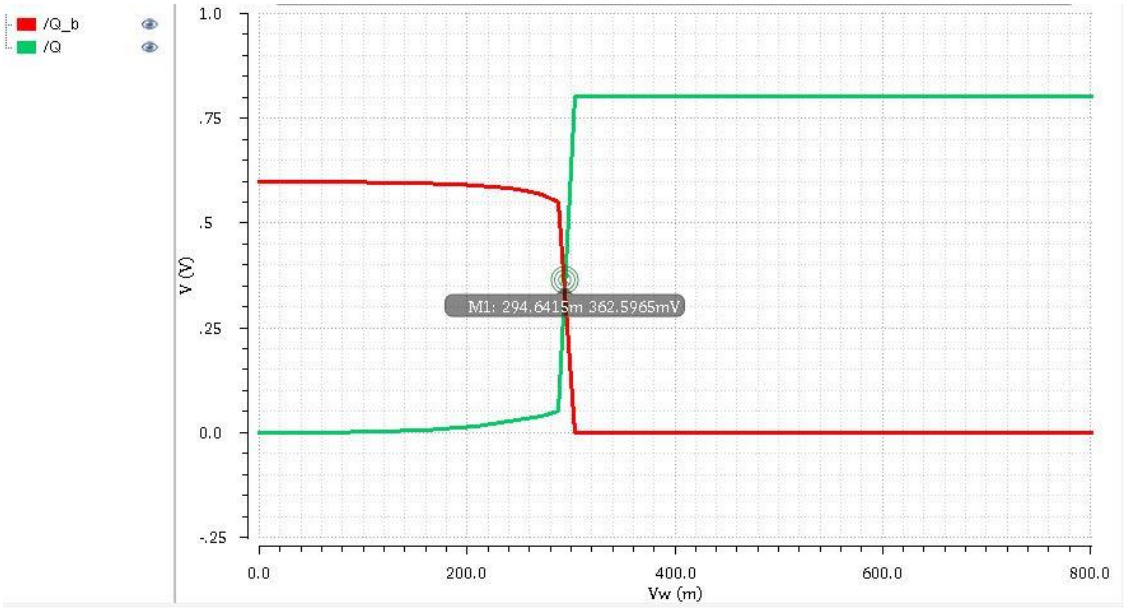


(b)

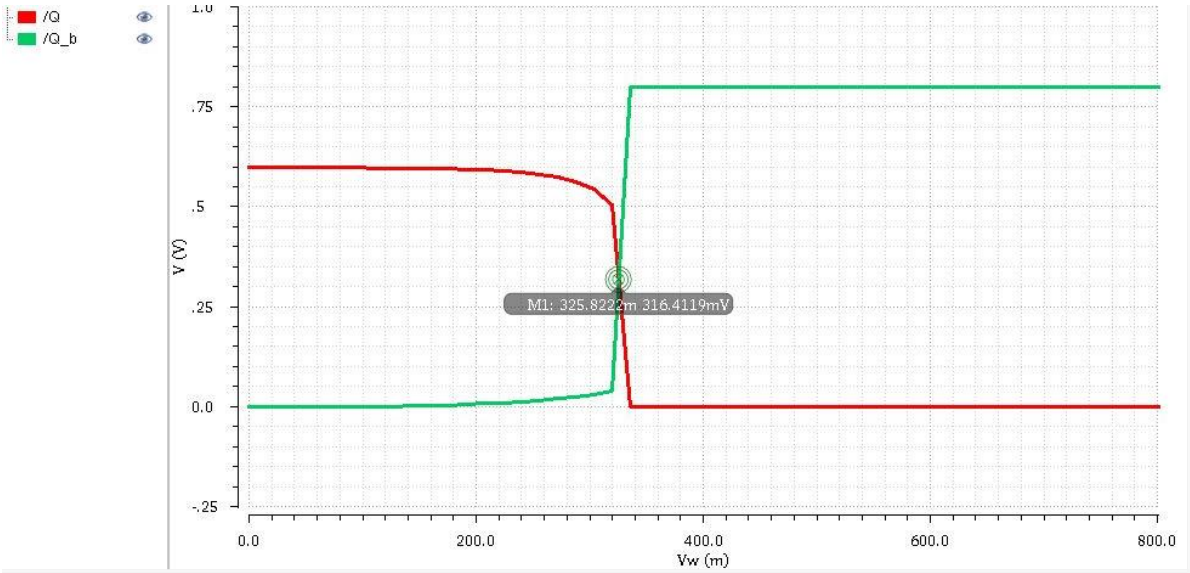
Fig. 3.11: (a) Write-1 Margin, (b) Write-0 Margin for 8TTG SRAM cell

The graphical curve used to find out write margins (both for writing 0 and 1) for the transmission gate based 8T SRAM cell is shown in Fig. 3.11. Here, write-1 margin and the

write-0 margin are the same because of the symmetrical configuration of transistors in the SRAM cell. The value of write-0 and write-1 margin is (800 – 358.2) mV is 441.8 mV.



(a)



(b)

Fig. 3.12: (a) Write-1 Margin, (b) Write-0 Margin for 9T SRAM cell

The graphical curve used to find out the write margins (both or writing 0 and 1) for 9T SRAM is illustrated in Fig. 3.12. The value of write-1 margin is (800-294.64) = 505.36 mV and that of write-1 margin is (800 – 325.82) = 474.2 mV.

3.2.4 Transient Analysis:

A transient analysis run on the considered SRAM cells reveals the how the read, write and hold operations actually happen by observing all the signals involved in the working of the cell.

Transient Analysis on conventional 6T cell

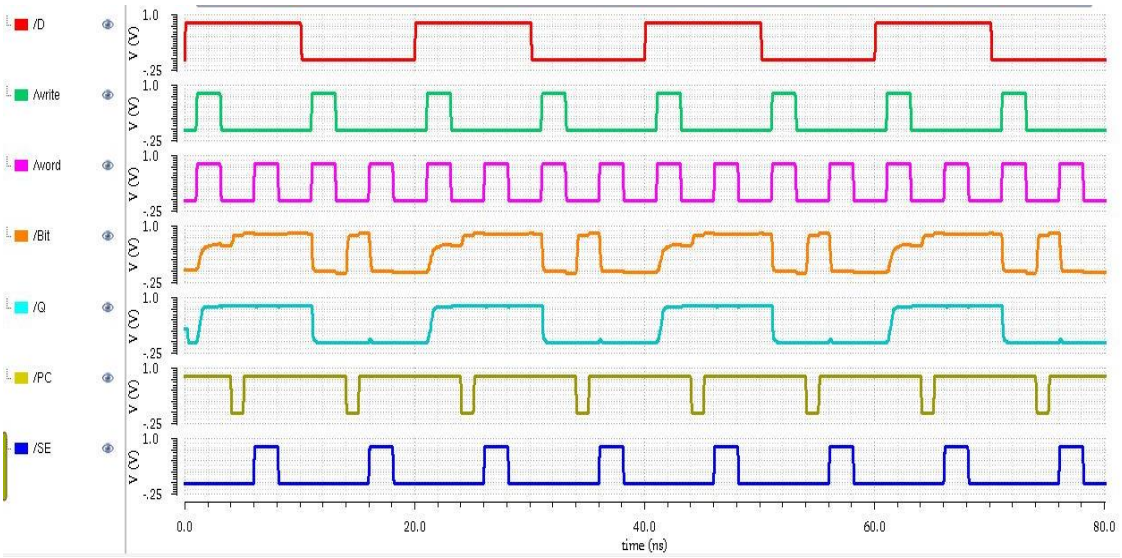


Fig. 3.13: Transient waveform of 6T SRAM cell.

As evident from Fig. 3.13, write operation in the conventional 6T SRAM cell is carried out when the write signal and the word signal are ON at the same period. Thus, whatever the data is in D signal is transferred onto Q node. Likewise, it can be seen that PreCharge (PC) signal is first pulled up high, and reading is done when word signal becomes high after the high PC signal event.

Transient Analysis on 7T SRAM cell

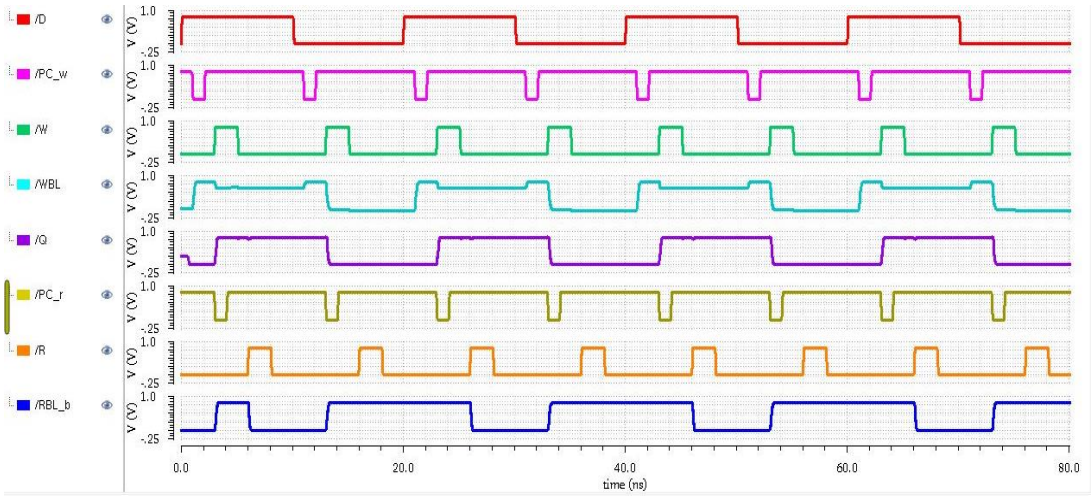


Fig. 3.14: Transient waveform of 7T SRAM cell

As evident from Fig. 3.14, before performing a write mode, the write bitline (WBL) is precharged to V_{DD}, and when W signal becomes high, WBL maintains the voltage or discharges to ground depending on D signal. Thus, whatever the data is in D signal is transferred onto Q node. Likewise, before performing a read process, read bitline_bar (RBL_b) is charged up to the maximum voltage. The RBL_b falls to low voltage or remains high when R become high, depending on what value is stored in node Q.

Transient Analysis on standard 8T SRAM cell

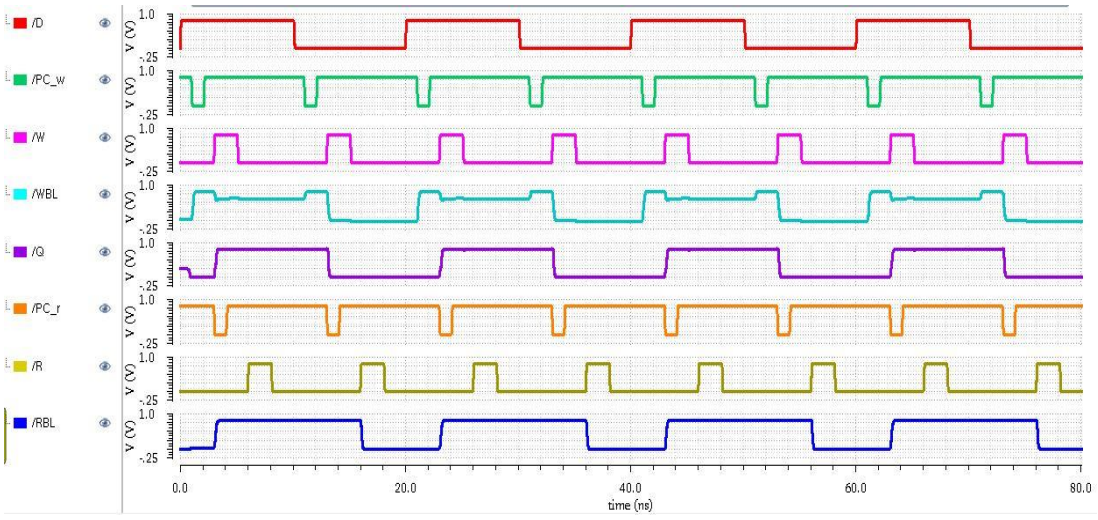


Fig. 3.15: Transient waveform of standard 8T SRAM cell

As evident from Fig. 3.15, before the process of writing onto the cell in standard 8T SRAM cell, the write bitline (WBL) and write bitline_bar (WBLB) are kept at the value of the desired bit and its complement using the write driver, and when W signal becomes high, whatever the data is in D signal is transferred onto Q node. Likewise, before writing onto the cell, read bitline (RBL) is charged up to maximum volatge. The RBL falls to low voltage or remains high when R become high, depending on what value is stored in node Q.

Transient Analysis on TG based 8T SRAM cell

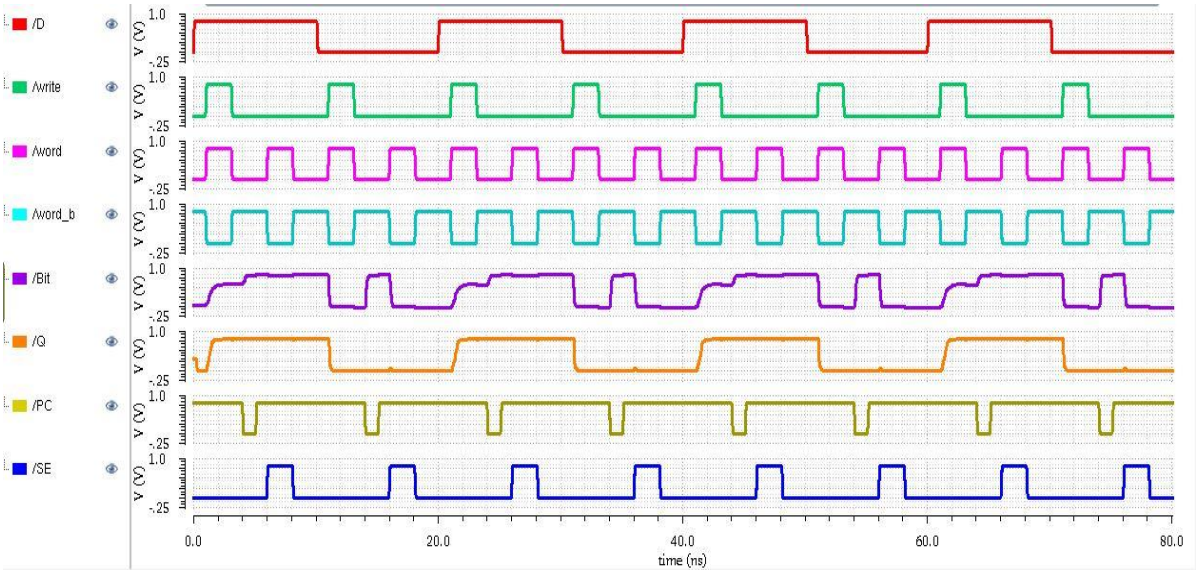


Fig. 3.15: Transient waveform of TG based 8T SRAM cell

As evident from Fig. 3.15, write process in the TG based cell is carried out when the write signal and the word signal are ON at the same period and the complement of word signal (word_b) is low. This turns the transmission gates ON. Thus, whatever the data is in D signal is transferred onto Q node. Likewise, it can be seen that PreCharge (PC) signal is first pulled up high, and reading is done when word signal becomes high after the high PC signal event.

Transient Analysis on 9T SRAM cell

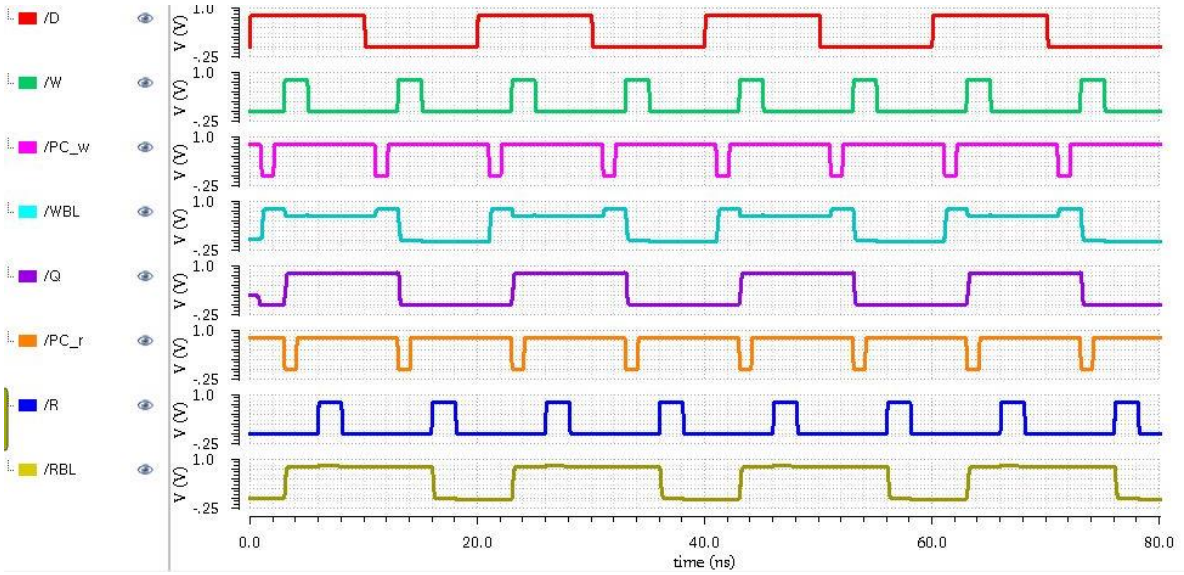


Fig. 3.16: Transient waveform of 9T SRAM cell

Fig. 3.16 shows the transient output waveform. It can be seen from here that write operation is carried out by first setting the write bitline (WBL) and write bitline_bar (WBLB) signals to the desired bit and its complement using the write driver. When W signal becomes high, whatever the data is in D signal is transferred onto Q node. Likewise, before accessing data from the cell, read bitline (RBL) is charged up to maximum voltage. The RBL falls to low voltage or remains high when R become high, depending on what value is stored in node Q.

3.3 SUMMARY OF RESULTS

From this chapter, after having studied in detail the important existing SRAM cell architecture that acted as foundation for the design of the proposed 8T cell, following important outcomes can be drawn:

- The RSNMs of the considered SRAM cells were measured using the butterfly curves, from which it was observed that the 7T SRAM cell proposed by Tawfik & Kursun [2] was the greatest with a value of 177 mV.

- Similarly, HSNMs of the considered SRAM cells measured using the butterfly curves revealed that the same 7T SRAM had the greatest HSNM amongst the considered cells with a value of 178.9 mV.
- The Write Margins were calculated using the approach given by Aslam & Hassan [7]. The simulation results revealed that the traditional 6T cell and the transmission gate based SRAM cell proposed by Roy and Islam [4] have values of write margins closest to $V_{DD}/2$. The values are 379 mV and 441 mV for write margins(writing 0 and 1 respectively) for the 6T SRAM cell and the TG based 8T cell respectively.
- Transient analyses were succesfully performed to verify their intended functionalities and also to have a good understanding of their working mechanisms.
- Additionally, the complications and shortcomings in each architecture are discussed to understand what led to the development of other cell designs in order to improve the shortcomings.

CHAPTER 4

DESIGN AND ANALYSIS OF PROPOSED 8T SRAM CELL

The proposed 8T SRAM cell is presented in this chapter. The chapter is further divided into six sections. Section 4.1 includes a detailed explanation of the architecture of the proposed cell that includes the different types of changes introduced in the proposed model. The Section 4.2 explains the working mechanism of the proposed cell including the read, write and hold operations. Section 4.3 discusses the simulation results obtained with regards to Static Noise Margins. Section 4.4 consists of the transient analysis of the proposed cell. Section 4.5 illustrates the measurement of access delays of the proposed cell. Then, section 4.6 concludes the chapter with a summary of results drawn from the chapter.

4.1 ARCHITECTURE OF PROPOSED SRAM CELL

The proposed SRAM cell design adopts the single ended, dual port, 1 Read 1 Write architecture. It uses only one bitline to perform the access operation (write and read), and has two ports, one meant for write operation and the other meant for read operation. Fig. 4.1 illustrates the architecture of the suggested cell.

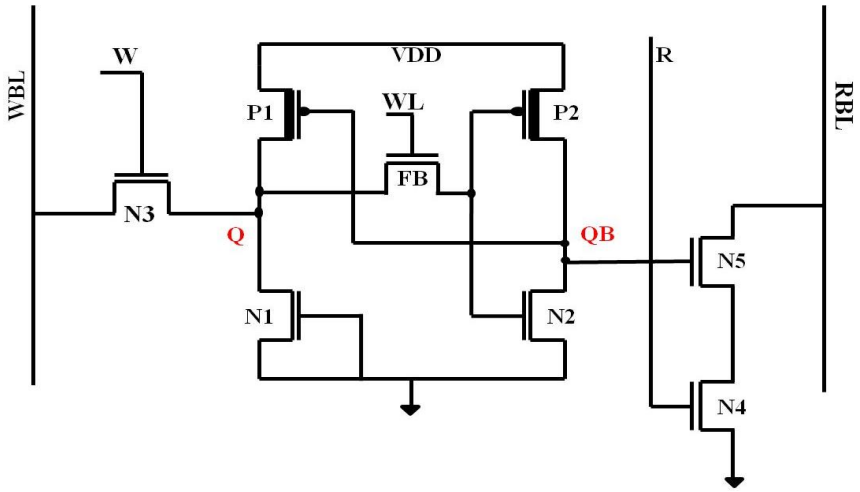


Fig. 4.1: Schematic of proposed 8T SRAM cell

It consists of 8 transistors. 5 MOS transistors make up the complementary storage nodes of the cell, where data is stored. The immediate noticeable change here compared to the prior architectures are: i) the use an extra transistor that cuts/ maintains the feedback between the two inverters, ii) pull down transistor of one inverter in cut off mode by shorting its gate terminal with ground. Then, the write bitline (WBL) is connected to the output of one inverter via a write access transistor, and the read port uses two stacked NMOS transistors to enable data to be read from the internal storage nodes to the read bitline (RBL). High threshold voltage PMOS transistors are used as pull-up device, P1 and P2 instead of normal transistors being used so that leakage power consumption is reduced.

First, the purpose using of an extra transistor between the back-to-back inverters is to eliminate the mutual feedback between the two inverters during a write operation. To understand this, assume the feedback cutting transistor was not there, then during write operation, the single write bitline would have to drive the inverter (made of P2 and N2) via the access transistor N3 to appropriate data values in the WBL. This is what caused the degradation in write performance in the 7T SRAM proposed by Tawfik & Kursun [2]. Thus to relieve the single write bitline of its duty to drive the inverter, the feedback transistor (FB) is turned off during write operations. This thus lead to improved write performance without using an extra write bitline.

Second, the purpose of grounding the gate terminal of transistor N1 is also related to improving write performance. During write mode, node Q would be forced with the data at WBL. Now, data is said to be transfered onto the cell since Q node is holding a new value. But after write mode, N3 would become OFF and the data at node Q would be essentially left floating, so this has to be reinforced by driving the inverter P1 & N1 by node QB. So when FB becomes ON immediately after write mode, data at node Q would drive inverter P2 & N2, pulling up/down QB to appropriate value. Now, QB has to reinforce Q. But since QB is driven by a floating value at Q, QB may not be strong enough so to facilitate easy driving of inverter P1 & N1, the pull down transistor N1 is cut off. This leads to a slight degradation in write-0 SNM but it is fairly compensated for by other enhancements and the write-0 performance degradation is not as bad the degradation in write-1 performance in the case of 7T SRAM [2].

The intention of using dual threshold voltage transistors is to decrease consumption of leakage power and also to enable usage of lowest sized transistors wherever possible. To understand the relation between using high threshold voltage transistors and decreasing leakage power can be understood better by considering the equation that defines the off-state current in a MOSFET [12].

$$I_{OFF} = I_S . e^{\frac{q(V_{GS} - V_T - V_{offset})}{nKT}} (1 - e^{\frac{-qV_{DS}}{KT}}) \quad (4.1)$$

Where, V_T = Threshold Voltage, and thus static power dissipation is minimized as the equation clearly shows, the off-state current exponentially declines as V_T increases. Thus, the use of static power is reduced as static power is given by equation (3.2) as indicated earlier in chapter 3.

However, question may arise here that the use high threshold voltage transistors are not used in place of all the other transistors too. This is accredited to the fact that, because of usage of two transistor types (one with high threshold voltage (V_T) and the other with low V_T), the size of both pull-up pull down transistors can be maintained at the minimum possible size. Even though the PMOS transistors have the same size as the NMOS transistors, they indeed are weaker compared to the NMOs because increased V_T results in reduced drive current. The aspect ratios of the transistor sizes of the proposed SRAM cell is given in Table 4.1.

Table 4.1 – Transistor sizing of proposed 8T SRAM cell

Transistors	**Width (W)**	**Length (L)**
P1, P2 (Pull-up transistors)	150 nm	100 nm
N1, N2 (Pull-down transistors)	150 nm	100 nm
N3 (Write access transistor)	400 nm	100 nm
N5, N6 (Stacked NMOS in read port)	300 nm	100 nm
FB (Feedback transistor)	150 nm	100 nm

4.2 WORKING MECHANISM OF PROPOSED SRAM CELL

This section explains the mechanism involved behind the working of this proposed SRAM cell. It begins with subsection 4.2.1 explaining the write operation. Likewise, hold operation and read operation are described in the subsections 4.2.2 and 4.2.3 respectively

4.2.1 Write Operation

To begin the process of writing onto the cell, WBL is precharged to V_{DD} voltage using the write driver circuit, Write signal (W) becomes high, Read signal (R) becomes low and FB transistor is turned OFF by giving WL a low signal. The write driver is a circuit peripheral to the SRAM cell as described in chapter 3. The WBL remains at V_{DD} after being precharged if a 1 is to be written onto the cell, whereas if a 0 is to be written onto the cell, WBL is discharged to ground via the write driver circuitry. Now, since FB transistor is OFF, whatever the data is at WBL is forced to node Q, but the crucial thing here is that it doesn't drive the P2 & N2 inverter during write operation. During write operation, the circuit schematic effectively reduces to the one illustrated in Fig. 4.2.

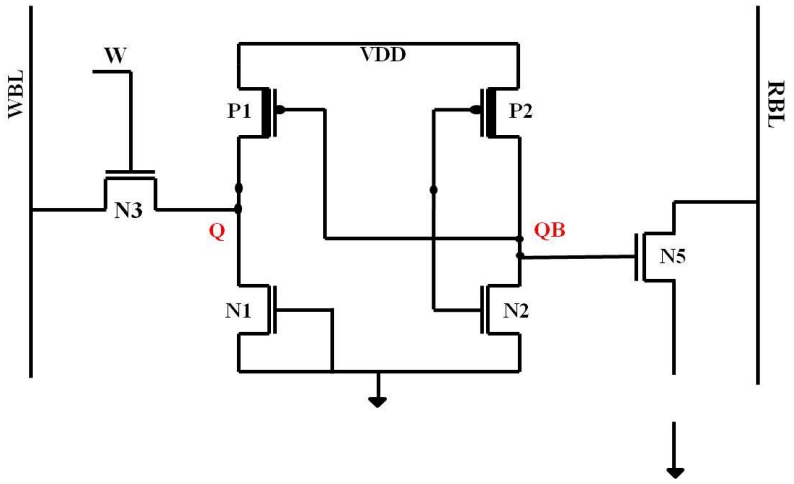


Fig. 4.2: Schematic of proposed 8T SRAM cell during write operation.

4.2.2 Hold Operation

After the write process is completed, Write signal (W) becomes low; WL becomes high, turning ON the FB transistor, while Read signal (R) remains low. Here, the role of FB transistor is crucial to retain the data in the storage nodes of the cell. This is because,

immediately after W becomes low, data at node Q is left floating and it can't be left floating for very long or else the data at Q will become degraded and true value might not be read during read mode. So, node Q has to be reinforced by node QB. FB transistor allows this, with FB transistor ON, node Q drives the inverter P2 & N2, drives QB to the value complement to that at node Q. then Node QB in turn drives inverter P1 & N1, reinforcing the data at Q. NMOS transistor N1 is made to be in cut-off mode, to allow easier driving of Q by QB. Fig. 4.3 shows the circuit that it has reduced to during hold mode.

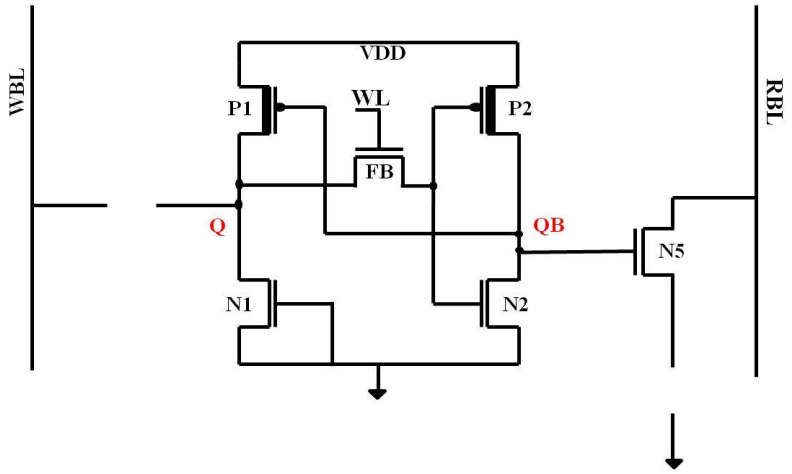


Fig. 4.3: Schematic of proposed 8T SRAM cell during hold operation.

4.2.3 Read Operation

To execute a read process, read bitline (RBL) is charged up to V_{DD} using the precharge circuit. WL signal is already ON, because they are made high as soon as write mode is over (i.e W become low). Then Read Signal (R) becomes high. The read port consists of a stack two NMOS transistors (N5 & N4) as shown in Fig. 4.1. Gate terminal of NMOS transistor N5 is shorted to node QB while the gate terminal of the other n-channel transistor in the stack, N4 is supplied by the read signal. Thus during the period when R is high, if the data at QB is a 1 (means Q holds a 0) it turns ON N5 and the RBL is pulled down to ground, whereas if the data at QB is a 0 (means Q holds a 1), it turns OFF N5, cutting off the path to ground via the stack, hence RBL remains at V_{DD}. This way, the data at the core of SRAM cell is essentially read. During read operation, the circuit schematic effectively reduces to the one illustrated in Fig. 4.4.

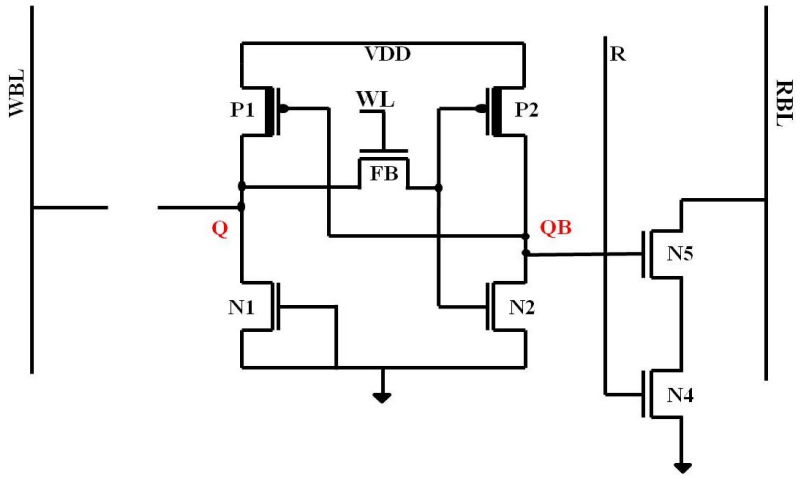


Fig. 4.4: Schematic of proposed 8T SRAM cell during read operation.

4.3 STATIC NOISE MARGINS

Static Noise Margins (SNM) are the measure of data stability in an SRAM Cell in each of the different operating modes. The upper limit of the DC noise that may be introduced to a storage node before the data stored there is inverted is known as the Static Noise Margin [35]. Thus, three types of SNM: Read, Hold and Write Static Noise margin (RSNM, HSNM and WM) are discussed below.

4.3.1 Read Static Noise Margin

RSNM is measured by using a graph called butterfly curves. It is basically a superposition of the Voltage Transfer Characteristics (VTC) of one inverter and the VTC of the other inverter of the two back-to-back inverters when the SRAM cell is in read mode [36]. Then the length of side of the largest square that can be fitted on the smaller of the two lobes of the butterfly curve gives the RSNM. The VTC of the two inverters are recorded by the following process: keep the signals of BL, RBLB, W and R at the level that is kept in an actual read operation, that is, RBLB at V_{DD} voltage, R also at V_{DD} voltage while W is kept low. Then, a voltage source is connected at Q node and swept from 0 to V_{DD}, then record the variation of potential at node QB to obtain the first VTC curve. To obtain the second VTC curve, the voltage source is connected at QB and swept from 0 to V_{DD} to obtain the second VTC curve, which is superposed on the first curve to obtain the correct butterfly curve. This butterfly curve is

used to calculate the RSNM value as shown in Fig. 4.5. The RSNM value obtained is 140.8 mV

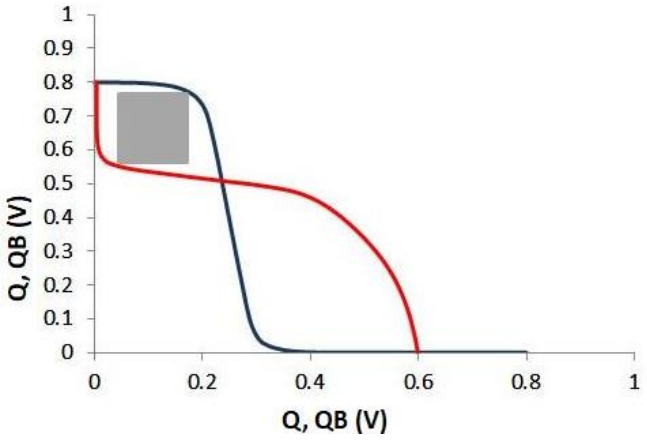


Fig. 4.5: Butterfly curve used to measure RSNM for proposed 8T SRAM cell

4.3.2 Hold Static Noise Margin

It is also calculated using the same butterfly curve approach as mentioned above. The only difference is that W and R signal are both kept low and the write access transistor and the read port are turned off when the potential at Q or QB is varied from 0 to maximum high voltage. The butterfly curve that gives the HSNM value, where the supply voltage is fixed at 0.8 V is illustrated in Fig. 4.6. HSNM for the 7T SRAM cell was found to be 143.8 mV.

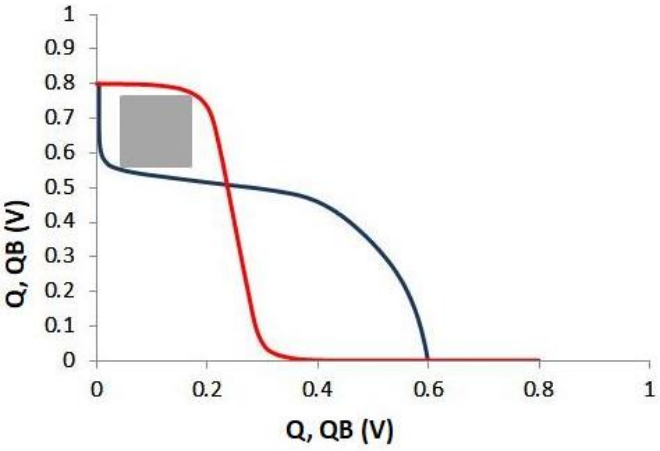


Fig. 4.6: Butterfly curve used to measure HSNM for proposed 8T SRAM cell

4.3.3 Write Margin

The Write Margin is determined by measuring the voltage gap between VDD and the Word Signal (W) voltage at which the data stored in the storage node is flipped, while progressively increasing the voltage at W from 0 to V_{DD}. [23]. WM for an SRAM should be ideally V_{DD}/2. So, how good an SRAM cell is in terms of write performance is determined by how close it is the V_{DD}/2. If it is too low, it means that it would be very difficult to write onto the cell. If it is very high, it means that it would be very easy to for noise to affect the write operation, and a small amount of noise can invert the data stored in the internal nodes. Write Margin is of two types: Write-1 Margin, Write-0 Margin. The V_{DD} used for calculating WM for all the cells is 0.8V. The graphical curve used to find out write-1 margin and write-0 margin is shown in Fig. 4.7 and Fig. 4.8. So, the write-1 margin and the write-0 margin are not the same because of the unsymmetrical configuration of NMOS and PMOS devices in the suggested SRAM cell. The value of write-1 margin is (800-294.67) = 505.3 mV and that of write-0 margin is (800 – 499.46) = 300.54 mV.

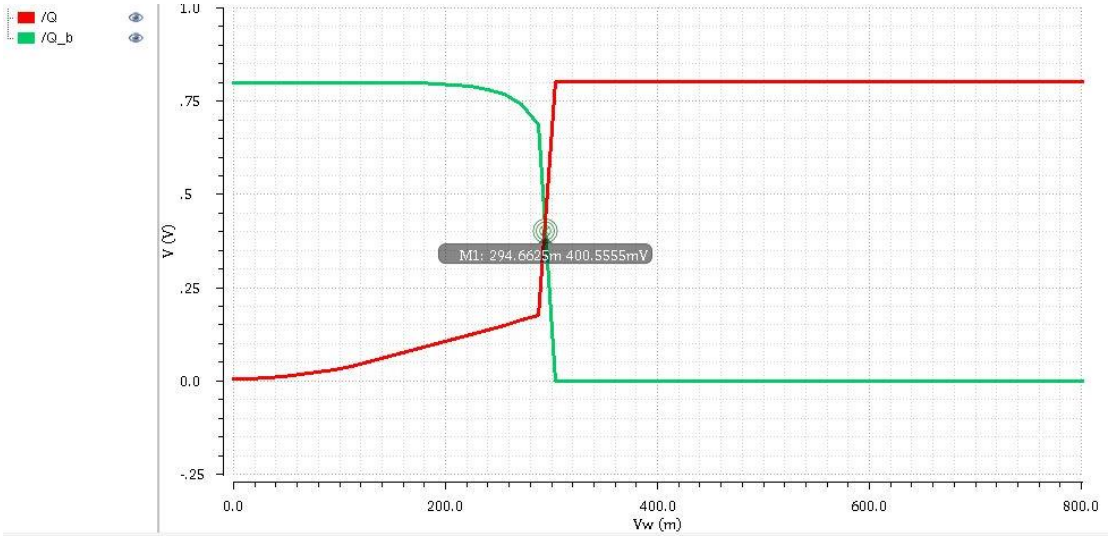


Fig. 4.7: Write-1 Margin for proposed 8T SRAM cell

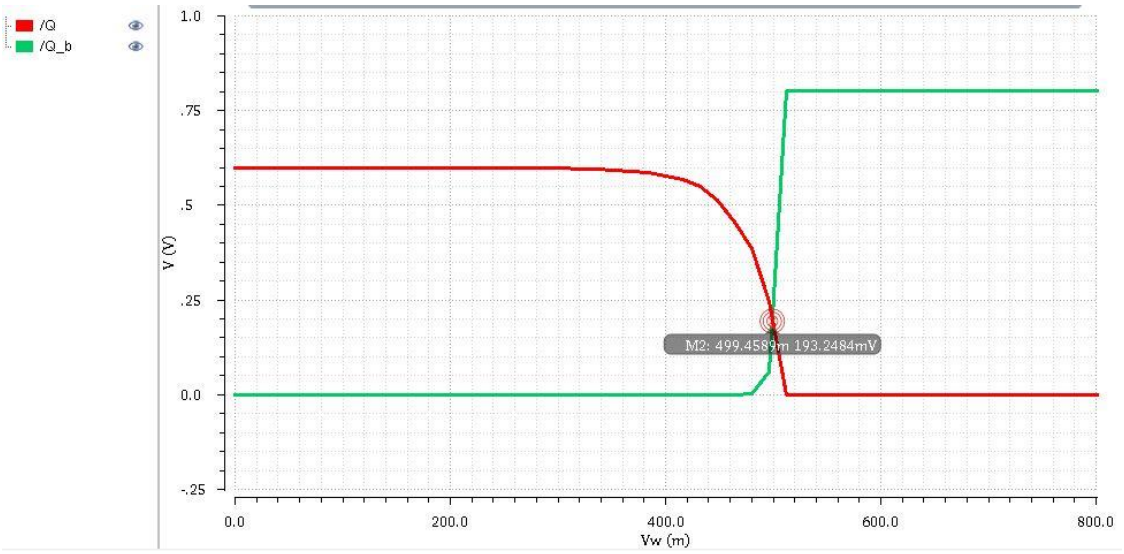


Fig. 4.8: Write-0 Margin for proposed 8T SRAM cell

4.4 TRANSIENT ANALYSIS

The output waveform of transient analysis on the proposed cell schematic helps us understand how the read, write and hold operations actually happen by observing all the signals involved in the working of the cell. As evident from Fig. 4.9, before performing a write process, the write bitline (WBL) is precharged by giving the signal PC_w a pulse just before the write signal (W) becomes high. Now, when W becomes high, using the write driver circuit, the WBL retains the charged V_{DD} voltage or gets discharged to ground depending on the D signal. As soon as write operation is over and W signal becomes low. WL signal becomes high so that the feedback between the pair of inverters can be restored and the data can be held on the storage nodes without being disturbed. If the feedback connection was not established, storage node Q would be left floating and the value will be lost after some time. Now, to perform read operation, read bitline (RBL) is precharged to V_{DD} by the PC_r signal. And read signal (R) becomes high while WL is still high. The RBL falls to low voltage or remains high, depending on what value is stored in node Q.

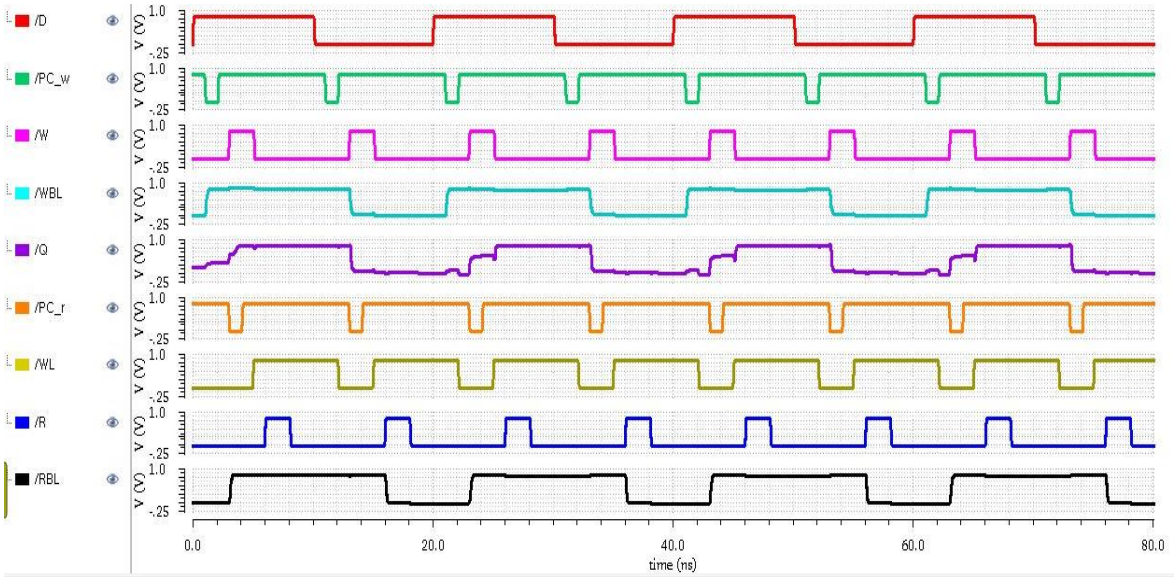


Fig. 4.9: Transient waveform of proposed 8T SRAM cell

4.5 ACCESS DELAY

The time taken to access the data present in the internal nodes during read or write process is known as access delay.

1) Read Access Delay: It is determined by measuring the time interval between the point at which the read signal (R) reaches 50% of its maximum value and the moment at which the potential on the read bitline (RBL) drops to the switching threshold voltage of the SRAM cell's inverter. [24].

2) Write Access Delay: It quantifies the time taken to transfer a data onto the storage nodes. It is calculated as the time interval between the moment at which write signal (W) attains 50% of final high value and the moment at which the data at the storage nodes is essentially flipped [25].

Access delays are calculated from the output waveforms of transient analysis as shown in Fig. 4.10. For the proposed cell, read delay is found to be 84 pS whereas the write delay is found to be 126 pS.

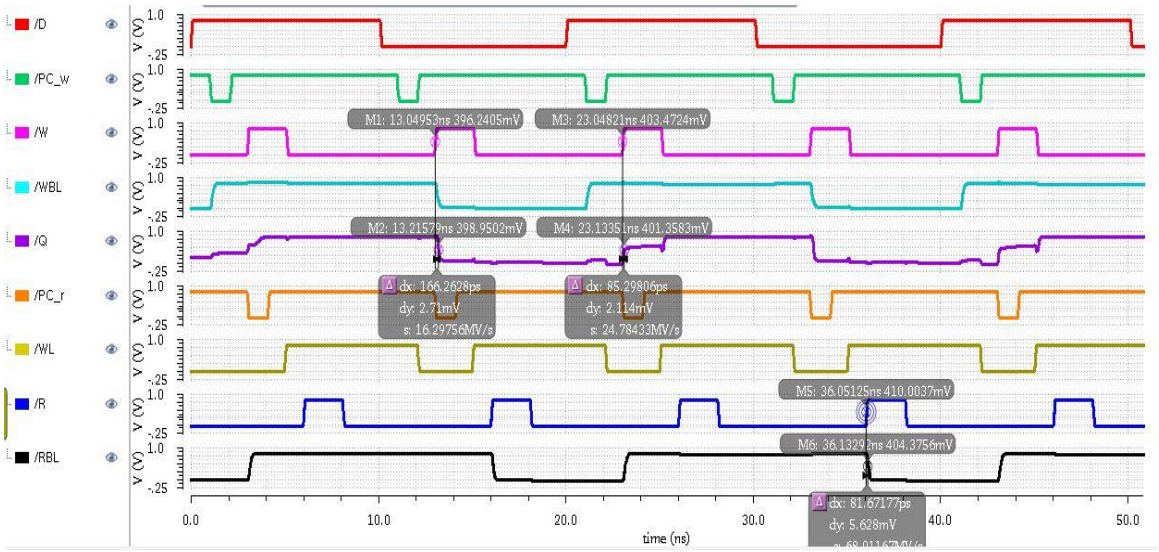


Fig. 4.10: Access delay calculation from transient waveform for proposed 8T SRAM cell

4.6 SUMMARY OF RESULTS

In this chapter, the proposed 8T SRAM cell is presented. The architecture is discussed in detail, the measurement of values of parameters are shown using snapshots from the simulation. Major outcomes that can be drawn are:

- The proposed SRAM cell architecture is analysed to acknowledge the changes in the cell architecture and understand how different it is from existing SRAM cell designs.
- Simulation findings revealed the measure of data stability with regards to static noise margins. The value of RSNM and HSNM obtained from the simulations are 130.8 mv and 133.8 mV respectively. The value of write-1 margin and write-0 margin are 505.3 and 300.54 mV respectively.
- The transient waveforms are analysed to understand the different working nature of the proposed SRAM cell.

The access delays for the proposed cell are also obtained using the transient waveforms which revealed. For the proposed cell, read delay is found to be 84 pS whereas the write delay is found to be 126 pS.

CHAPTER 5

STATIC AND DYANAMIC PERFORMANCE COMPARISON OF DESIGNED 8T CELL WITH EXISTING CELLS

The existing SRAM cells that were reviewed comprehensively in Chapter 3, that also formed a foundation for the design of the proposed SRAM cell will be used here for the purpose of comparison against the proposed 8T SRAM cell. A total of five existing SRAM cell models will be considered for comparison in this chapter.

The chapter consists of three main sections. The comparison is divided into two sections. Section 5.1 presents the comparative analysis of the proposed SRAM cell with other existing SRAM cells with varying transistor counts. Section 5.2 presents the comparative analysis of the proposed SRAM cell with existing SRAM cells of the same transistor count as that of the proposed cell. The comparison is illustrated in a detailed graphical manner for each performance indicating parameter with each parameter covered in the following individual subsections. Section 5.3 concludes the chapter with summary of the results obtained from the analysis done in this chapter.

5.1 COMPARISON OF PROPOSED 8T CELL WITH OTHER EXISTING CELLS OF DIFFERENT TRANSISTOR COUNTS

The Cadence Virtuoso tool was used to simulate all the models. All of them were designed using the same technology node of 90 nm and same supply voltage of 0.8V. They were put under the same temperature and supply voltage variations to produce a fair comparison result. The aspect ratios of the transistors in the SRAM cells are also maintained in accordance to their respective original papers. The W/L ratios of all the transistors of the models are indicated in the transistor sizing tables given in Chapter 3 and 4. In each of the graphical comparative figures, the traditional 6T SRAM cell is denoted by ‘6T’, the 7T

SRAM proposed by Tawfik & Kursun [2] as '7T', the 9T SRAM cell proposed by Sheng Lin, Yong-Bin Kim, and Fabrizio Lombardi [5] as '9T' and the proposed 8T SRAM cell is denoted by just '8T'.

5.1.1 Read Static Noise Margin

A graph is shown in Fig. 5.1 indicating the comparison of RSNM among the four models, one proposed cell and the other three existing SRAM cell models with different transistor counts. The RSNM of the proposed SRAM Cell (indicated by 8T in the graph) is more than the RSNM of 6T by 141%. The 7T SRAM Cell [2] and the 9T SRAM cell [5] is superior in terms of RSNM because of the architectures being solely designed to improve RSNM. But the RSNM of the suggested SRAM cell is also fairly decent enough for its working as a cell in a memory array. Also, the lesser RSNM compared to 7T and 9T SRAM is compensated hugely in other parameters as will be evident in further subsections.

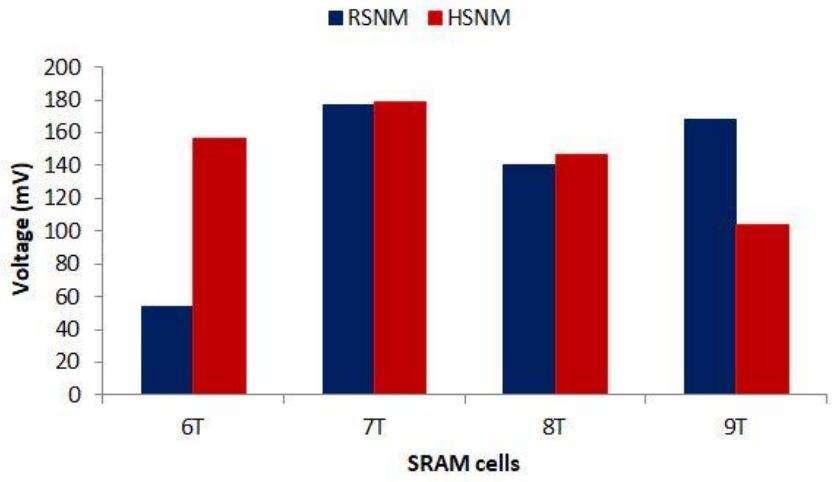


Fig. 5.1: Comparison of RSNM and HSNM of SRAM cells with varying transistor counts

5.1.2 Hold Static Noise Margin

Fig. 5.3 also shows the how the Hold Static Noise Margin (HSNM) of the proposed SRAM Cell compares to that of the other SRAM Cells. 9T SRAM cell has the highest HSNM. HSNM for the proposed cell is almost equal to that of that of 6T, but a little less than that of

7T and 9T SRAM Cells. However, it is still an acceptable value and will compensate this with other parameters.

5.1.3 Write Margin

The supply voltage, V_{DD} used for calculating Write Margin (WM) for all the considered SRAM cells is 0.8 V. Graph in Fig. 5.2 shows the comparison of WM of the other cells with the proposed cell (8T). As evident from the graphical comparison the SRAM cell whose WM is close to $V_{DD}/2$ for both write-1 and write-0 operation is the proposed SRAM cell (8T) followed by the 6T SRAM cell. The 7T has a highly unsymmetrical write performance where the write-1 margin is too low and not acceptable.

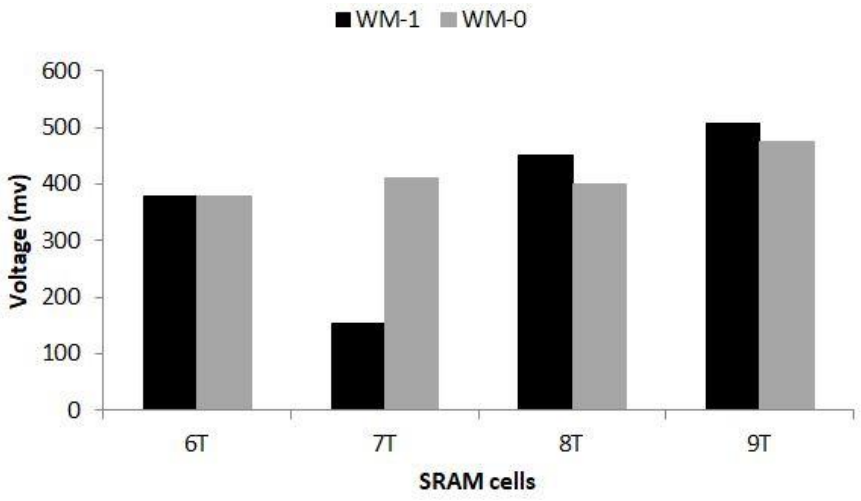


Fig. 5.2: Comparison of Write Margin of SRAM cells with varying transistor counts

5.1.4 Read Access Delay

As the graph in Fig. 5.3 indicates, the read access delay for the suggested SRAM cell (8T) is the minimum, and it is lesser than the read delay of 6T, 7T and 9T by 12.5%, 3.33% and 8.49% respectively.

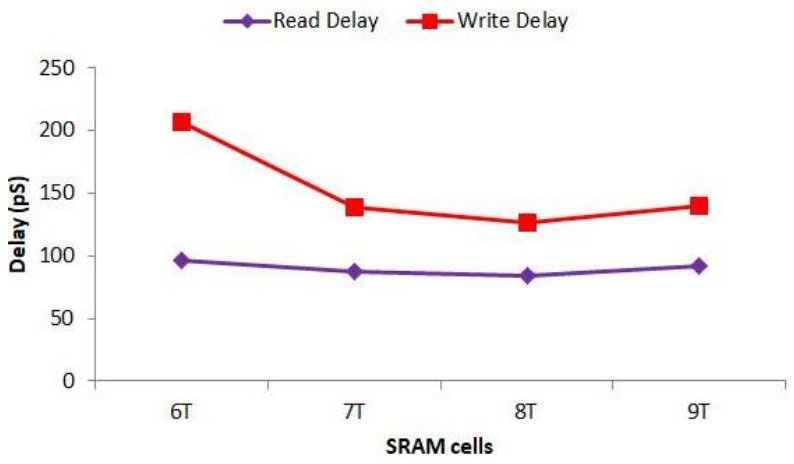


Fig. 5.3: Comparison of Read and Write delay of SRAM cells with varying transistor counts

5.1.5 Write Access Delay

From the graph in Fig. 5.3, the write delay is also the least for the proposed 8T SRAM cell. It is lesser than the write delays of 6T, 7T and 9T by 39.1%, 9.4% and 9.67% respectively. The conventional 6T SRAM has the largest amount of access delay (considering both read and write access delay) among the models.

5.1.6 Supply Voltage Variations

Like any instance in a System-on-Chip (SoC), memory arrays experience varying voltage drops at their supply voltage pins due to various regions during its usage in the real world. This means that the supply voltage of the SRAM cells can vary drastically. This would in turn have an impact on the noise margins. The SRAM cell whose noise margin varies the least in response to supply voltage variation would be the desirable one. Thus it is essential to study the variation of RSNM, HSNM and WM in response to varying supply voltage. Here, all the four SRAM cell architectures are put under the same supply voltage variation from 0.6 V to 1.2 V.

As evident from the graphical comparison in Fig. 5.4, the suggested 8T SRAM cell (8T) exhibits the least deviation of HSNM overall in response to supply voltage variation. The other SRAM cell architectures has great variation in their HSNMs and keeps on increasing as supply voltage is increased.

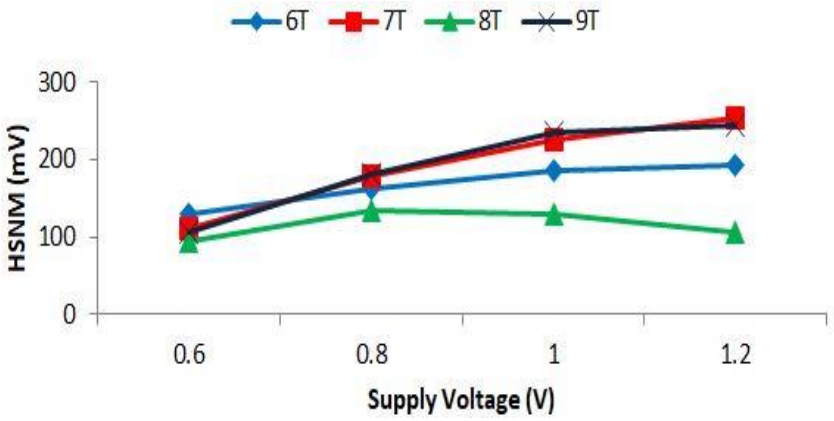


Fig. 5.4: Comparison of HSNM in response to supply voltage variations of SRAM cells with varying transistor counts.

Fig. 5.5 gives the graphical comparison of the variation of RSNM and the 9T SRAM cell is observed to have the least variation of RSNM in response to supply voltage variation but the proposed 8T SRAM (8T) comes close second to 9T SRAM cell. The 7T SRAM cell varies the most, followed by the standard 8T SRAM cell.

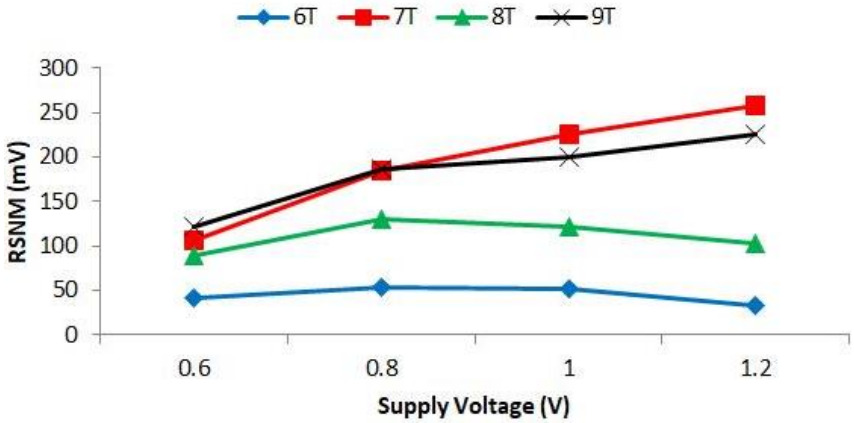
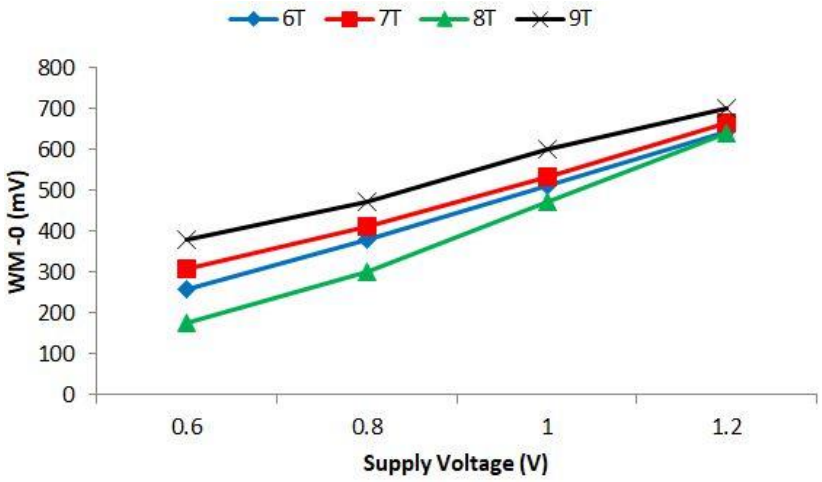
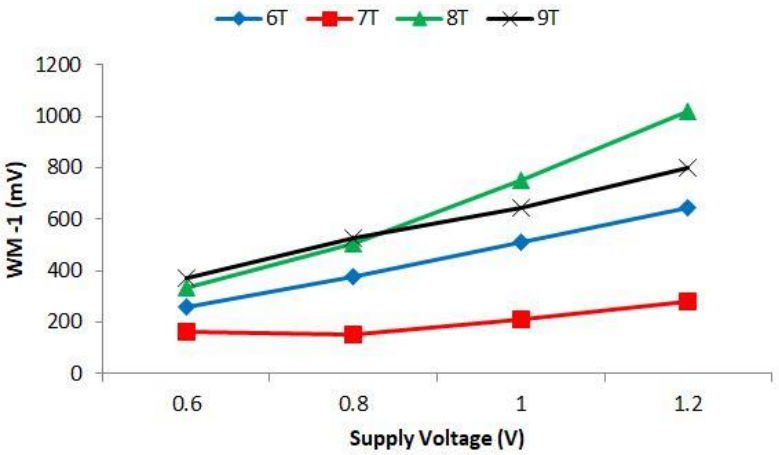


Fig. 5.5: Comparison of RSNM in response to supply voltage variations of SRAM cells with varying transistor counts.

Fig. 5.6 shows the variation of Write Margins (both for the case of writing '0' and '1') of various SRAM cells with varying transistor counts in response to variations in supply voltage. It indicates that almost all the models vary in a more or less similar way.



(a)



(b)

Fig.5.6: Comparison of (a) WM-0 and (b) WM-1, in response to supply voltage variations of SRAM cells with varying transistor counts

The Write-1 Margin of the porposed SRAM cell is observed to vary in the same trend as the others although slightly higher compared to others but it is compensation by its robustness of RSNM and HSNM in response to supply voltage scaling.

5.1.7 Temperature Variations

Just as supply voltage variations happen in a real world scenario, temperature variation is also an inevitable phenomenon in any System-on-Chip (SoC) that uses a memory array.

Therefore, it is essential to research how temperature fluctuations affect the performance parameters, notably the noise margin parameter. To examine the impact, all the SRAM cell models were put under a temperature variation from -10℃ to 110℃ and the variations of the noise margins were observed.

Hold Static Noise Margin

As indicated in the graphical comparison in Fig. 5.9, 6T and 9T SRAM cells are the architectures that experience the most variations of Hold Margin with respect to temperature. 6T and 9T SRAM cells have variation of 1.19 mV/℃ and 1.38 mV/℃ respectively. 7T SRAM cell and the suggested 8T SRAM cell have a low variation of 0.85 mV/℃ and 0.79 mV/℃ respectively.

Read Static Noise Margin

As the graphical comparison in Fig. 5.7 shows, the 9T SRAM cell has the largest variation at 1.35 mV/℃, proposed SRAM cell (8T) has a variation of 0.77 mV/℃.

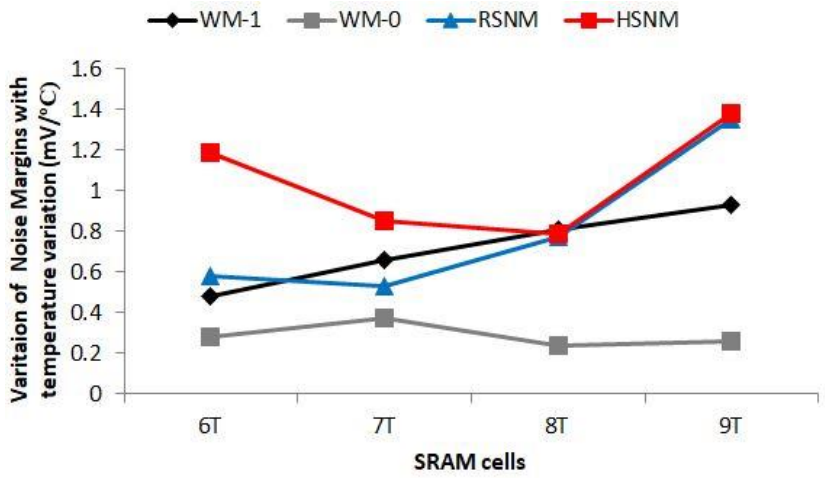


Fig. 5.7: Variation of Noise Margins with temperature of SRAM cells with varying transistor counts

The 7T and the 6T SRAM cell has the least variation of RSNM at 0.53 mV/ºC and 0.58 mV/ºC respectively.

Write Margin

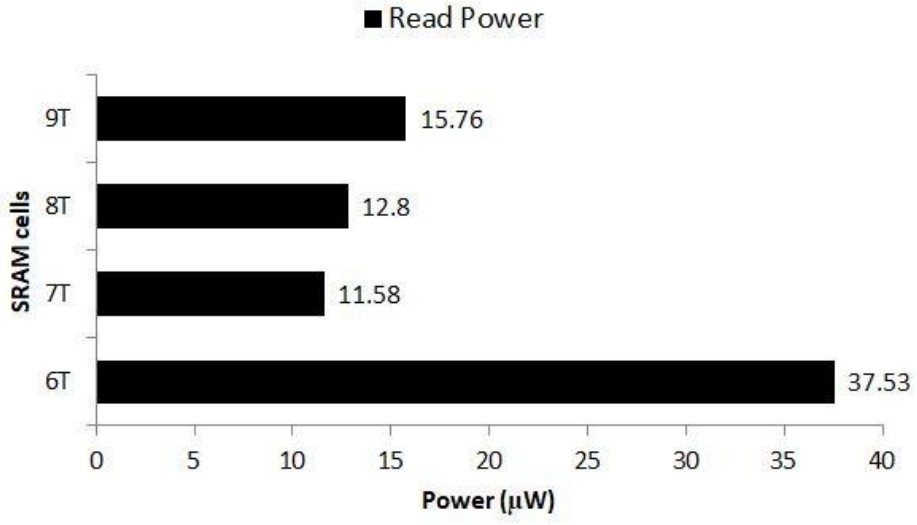
The proposed 8T SRAM cell is found to have the least variation of Write-0 margin at 0.24 mV/°C. However, variation of Write-1 margin is a bit of a problem with the proposed 8T cell slightly on the higher side compared to 6T and 7T cells, but much less than that of 9T SRAM cell.

5.1.8 Power Consumptions

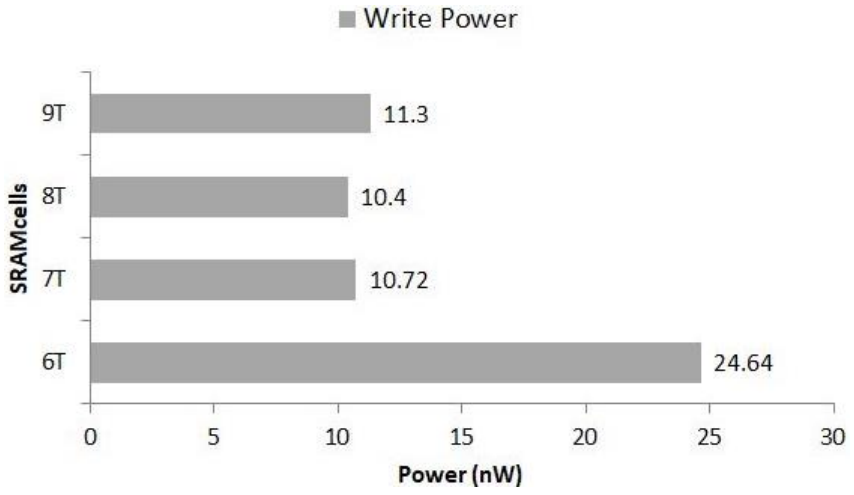
Power consumption is always a concern for any circuitry present in an integrated circuit. Any designer would strive towards having the lowest power consumption possible while designing any circuit. Power consumption for an SRAM cell is of two types: Dynamic Power Consumption and Static Power Consumption. Thus the analysis of power consumption would be better understood by discussing it in separate subsections.

Dynamic Power Consumption

It is the power consumed by the circuit when a read or a write operation is being carried out. Graphical comparison of dynamic powers for read and write mode is shown in Fig 5.8. The conventional 6T SRAM has the highest read power consumption at 37.53 μW. This is accredited to the use of two bitlines to read data from the cell.



(a)



(b)

Fig. 5.8: Comparison of dynamic (a) Read Power and (b) Write Power of SRAM cells with varying transistor counts

Proposed 8T SRAM and the 7T SRAM were observed to have least read power consumption at 12.8 µW and 11.58 µW respectively. Conventional 6T SRAM also has the highest write power consumption, while proposed 8T SRAM has the least read power consumption of 10.4 nW..

Static Power Consumption

It is the power consumed when the SRAM cell is in idle state. It is basically due to the accumulation of leakage currents in the MOS transistors hence also known as leakage power consumption. It is calculated as the leakage current during idle state multiplied by the supply voltage value. As evident form the graphical representation of the comparison shown in Fig. 5.9, the conventional 6T cell was observed to have the highest leakage power consumption. The leakage power consumptions of the 7T, 8T and the 9T SRAM cell do not have much of a difference.

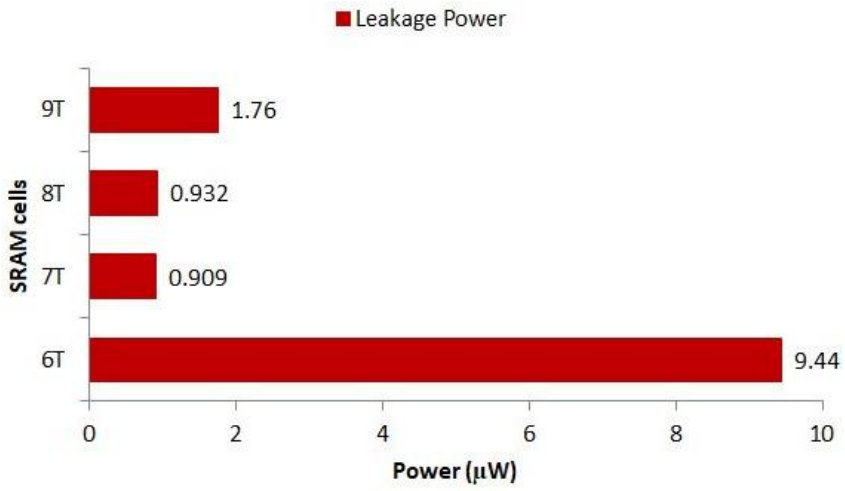


Fig. 5.9: Comparison of static power consumption of SRAM cells with varying transistor counts

The 7T SRAM cell was found to have the least standby static power followed by the suggested 8T SRAM design. The 9T SRAM design has slightly higher leakage power mostly due to absence of dual threshold voltage transistors in the design.

5.2 COMPARISON OF PROPOSED 8T CELL WITH OTHER CELLS OF SAME TRANSISTOR COUNT

In each of the graphical comparative figures, the 8T SRAM cell proposed by Calhoun & Chandrakasan [3] as '8TS', the transmission gate based 8T SRAM proposed by Roy C and Islam A [4] as '8TTG' and the proposed 8T SRAM cell is denoted by just '8T'.

5.2.1 Read Static Noise Margin

A graph is shown in Fig. 5.10 indicating the comparison of RSNM among the three models, one proposed cell and the other two existing SRAM cell models, all comprising of 8 transistor counts. The RSNM of the proposed SRAM Cell (indicated by 8T in the graph) is the highest. The transmission gate based 8T SRAM cell has the least RSNM because it doesn't use an isolated read port and has almost the same architecture as the conventional 6T SRAM cell.

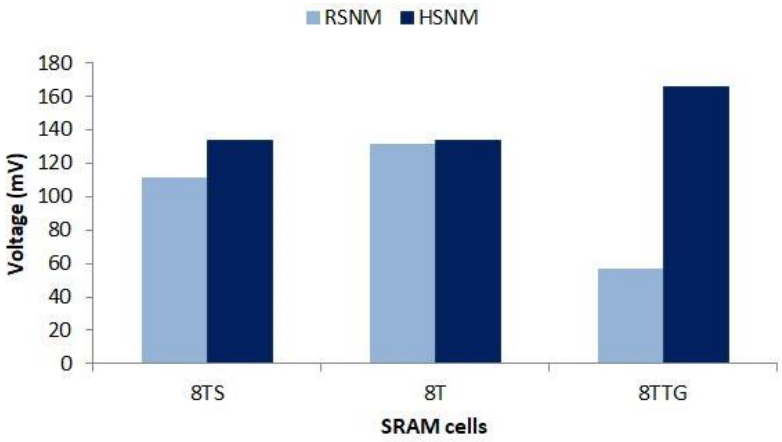


Fig. 5.10: Comparison of RSNM and HSNM of SRAM cells with same transistor count

5.2.2 Hold Static Noise Margin

Fig. 5.10 also shows how the Hold Static Noise Margin (HSNM) of the proposed SRAM Cell compares to that of the other SRAM Cells. Transmission gate based 8T SRAM cell (8TTG) has the highest HSNM. HSNM for the proposed cell is almost equal to that of that of the standard 8T SRAM cell (8T).

5.2.3 Write Margin

The V_{DD} used for calculating Write Margin for all the considered SRAM cells is 0.8 V. Graph in Fig. 5.11 shows the comparison of WM of the other 8T SRAM cells with the proposed cell (8T).

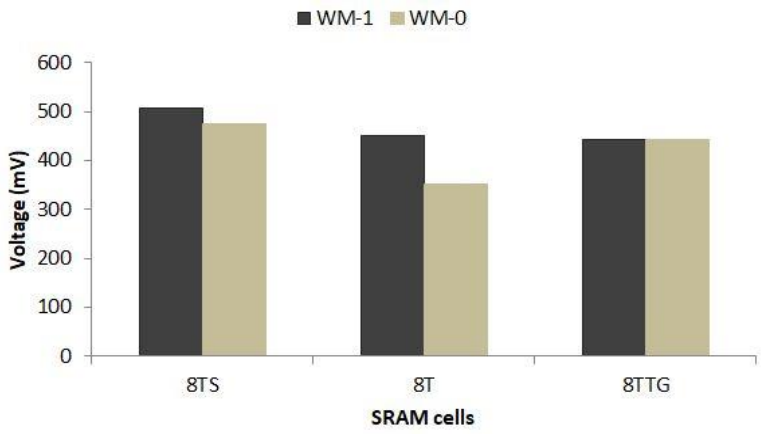


Fig. 5.11: Comparison of Write Margin of SRAM cells with same transistor count

As evident from the graphical comparison, the SRAM cell who's WM is close to $V_{DD}/2$ for both write-1 and write-0 operations is the suggested 8T SRAM cell (8T) and the transmission gate based 8T SRAM cell (8TTG). The write margin is too high for the 8TS cell.

5.2.4 Read Access Delay

The graphical representation of the comparison between the 8T SRAM cells is shown in Fig. 5.12. It indicates that the read access delay for the suggested SRAM cell (8T) is the minimum, and it is lesser than the read delay of 8TS and 8TTG by 1.18% and 12.13% respectively.

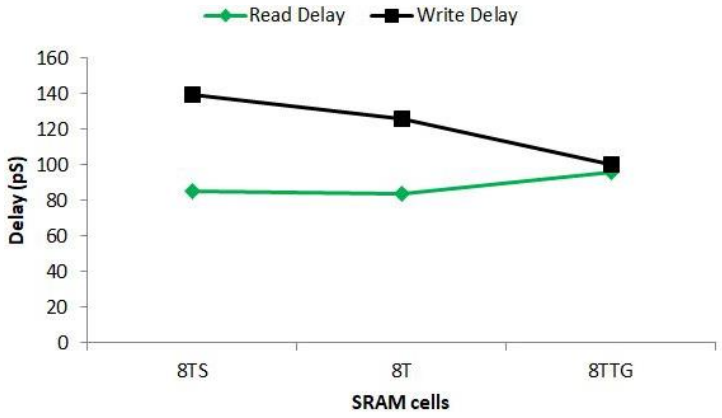


Fig. 5.12 Comparison of Read and Write delay of SRAM cells with same transistor count

5.2.5 Write Access Delay

From the graph in Fig. 5.14, the write delay is the least for 8TTG cell. The utilization of transmission gates instead of traditional pass gate transistors for accessing the storage nodes contributes to the observed improvement in read and write delays. The standard 8T SRAM cell has the largest amount of access delay (considering both read and write access delay) among the models.

5.2.6 Supply Voltage Variations

In practical usage of memory arrays, the operating supply voltage reaching the SRAM circuits can vary drastically. This would in turn have an impact on the noise margins. The

SRAM cell whose noise margin varies the least in response to supply voltage variation would be the desirable one. Thus it is essential to study the variation of RSNM, HSNM and WM in response to varying supply voltage. Here, all the four SRAM cell architectures are put under the same supply voltage variation from 0.6 V to 1.2 V. As evident from the graphical comparison in Fig. 5.13, the suggested 8T SRAM cell (8T) has the least deviation of HSNM overall in response to supply voltage variation.

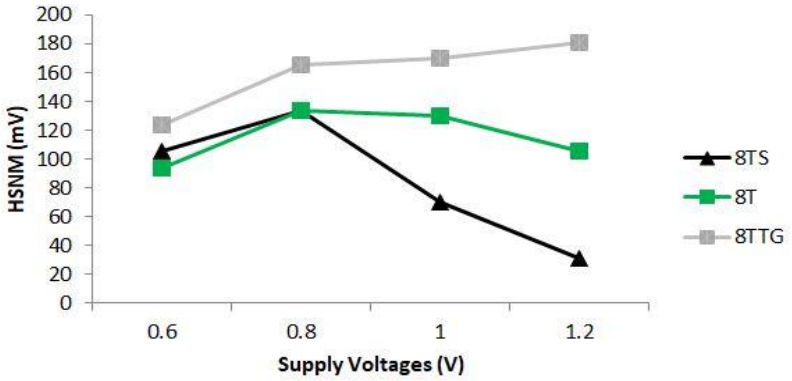


Fig. 5.13: Comparison of HSNM in response to supply voltage variations of various SRAM cells with same transistor count

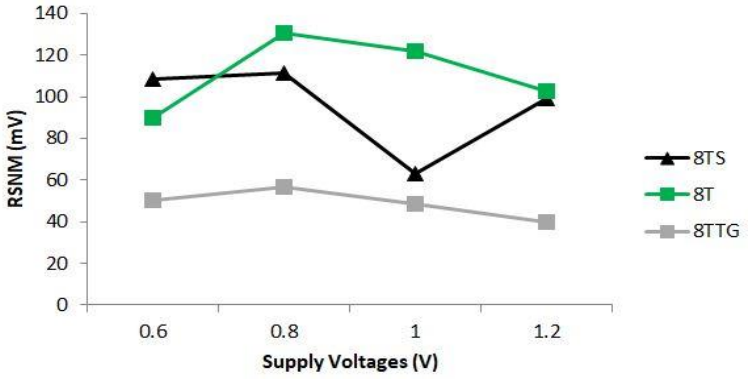
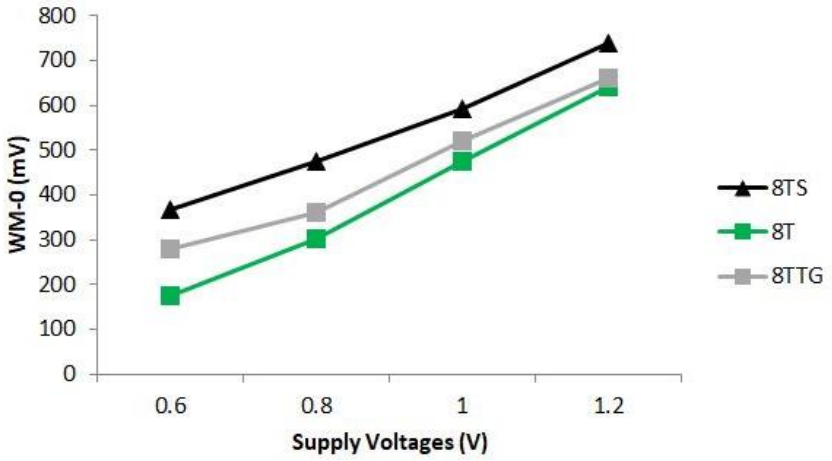


Fig. 5.14: Comparison of RSNM in response to supply voltage variations of various SRAM cells with same transistor count

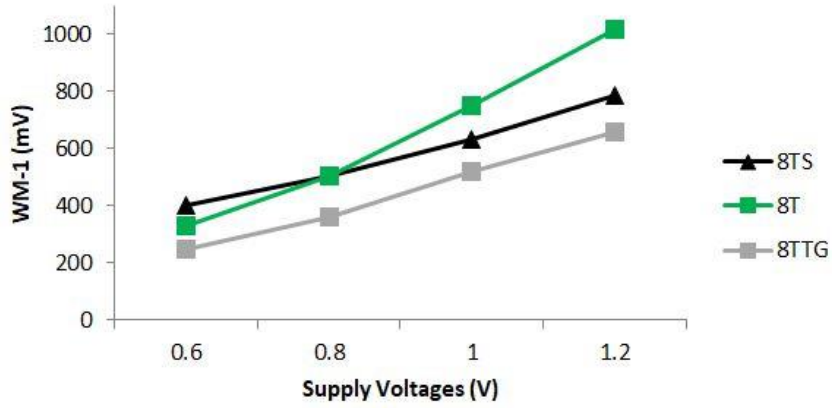
Fig. 5.14 gives the graphical comparison of the variation of RSNM in response to supply voltage variations of various SRAM cells with same transistor count. The proposed 8TTG SRAM cell is observed to have the least variation of RSNM, but the value is very minimal

and doesn't increase even when supply voltage increases. The standard 8T SRAM (8TS) cell varies the most, followed by the suggested 8T SRAM cell.

Fig. 5.15 shows the variation of Write Margins (both for writing '0' and '1') of the SRAM cells in response to variations in supply voltage. It indicates that almost all the models vary in a more or less similar way.



(a)



(b)

Fig.5.15: Comparison of (a) WM-0 and (b) WM-1, in response to supply voltage variations of SRAM cells with same transistor count

The Write-1 Margin of the suggested 8T SRAM cell is observed to vary in the same trend as the others although slightly higher compared to others but it is compensation by its robustness of RSNM and HSNM in response to supply voltage scaling.

5.2.7 Temperature Variations

Just as supply voltage variations happen in a real world scenario, temperature variation is also an inevitable phenomenon in any System-on-Chip (SoC) that uses a memory array. Therefore, it is essential to research how temperature fluctuations affect the performance parameters, notably the noise margin parameter. To examine the impact, all the SRAM cell models were put under a temperature variation from -10℃ to 110℃ and the variations of the noise margins were observed.

Hold Static Noise Margin

As indicated in the graphical comparison in Fig. 5.16, the suggested 8T SRAM cell experiences the least deviation of Hold Margin with respect to temperature at 0.79 mV/℃. 8TS and 8TTG SRAM cells have variation of 1.37 mV/℃ and 1.11 mV/℃ respectively.

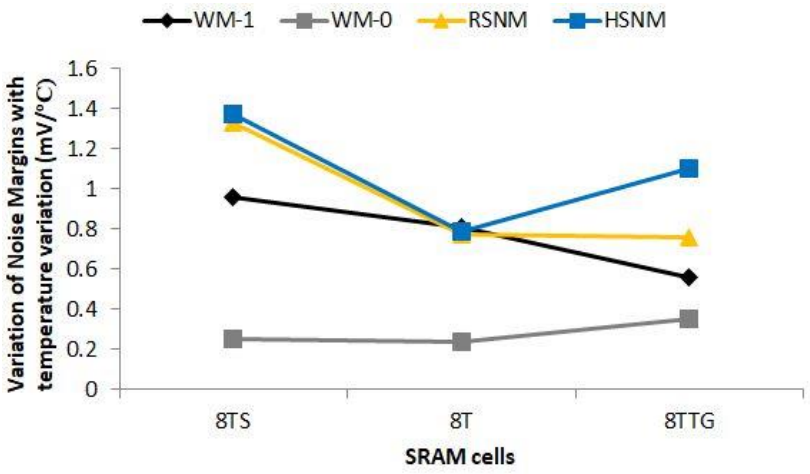


Fig. 5.16: Variation of Noise Margins with temperature of SRAM cells with same transistor count

Read Static Noise Margin

As the graphical comparison in Fig. 5.16 shows, 8TS SRAM cell has the highest variation at 1.33 mV/°C, proposed SRAM cell (8T) has a variation of 0.77 mV/°C. The 8TTG SRAM cell has the least variation of RSNM at 0.76 mV/°C.

Write Margin

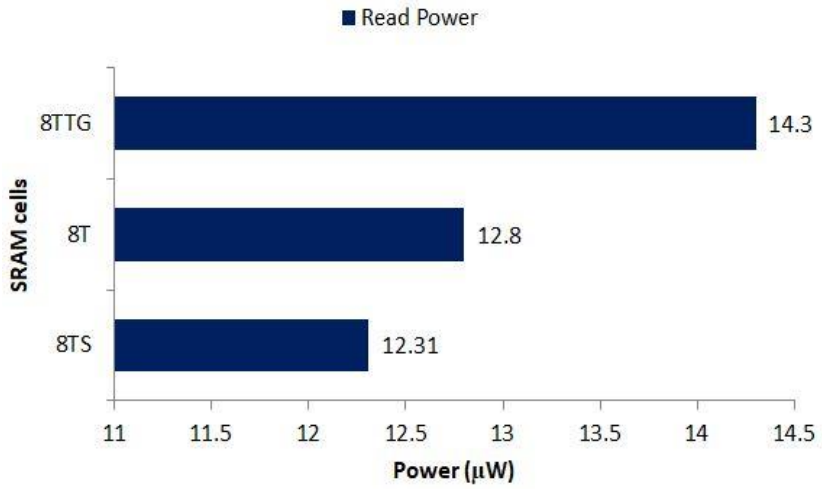
The proposed 8T SRAM cell is found to have the least variation of Write-0 margin at 0.24 mV/°C. However, variation of Write-1 margin is less than that of 8TS but larger than that 0f 8TTG.

5.2.8 Power Consumptions

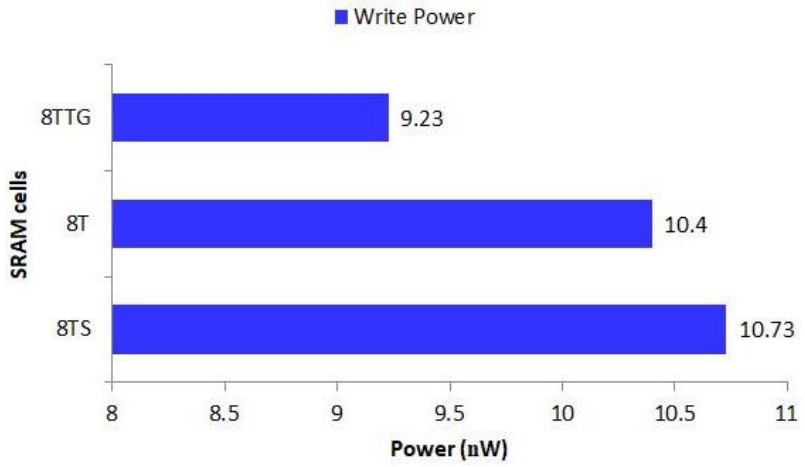
Power consumption is always a concern for any circuitry present in an integrated circuit. Any designer would strive towards having the lowest power consumption possible while designing any circuit. Power consumption for an SRAM cell is of two types: Dynamic Power Consumption and Static Power Consumption. Thus the analysis of power consumption would be better understood by discussing it in separate subsections.

Dynamic Power Consumption

It is the power consumed by the circuit when a read or a write operation is being carried out. Graphical comparison of dynamic powers for read and write mode is shown in Fig 5.17. The conventional 8TTG SRAM cell has the highest read power consumption at 14.3 μW. This is accredited to the use of two bitlines to read data from the cell. Proposed 8T SRAM and the 8TS SRAM were observed to have least read power consumption at 12.8 μW and 12.31 μW respectively.



(a)



(b)

Fig. 5.17: Comparison of dynamic (a) Read Power and (b) Write Power of SRAM cells with same transistor count.

The 8TTG cell however is observed to have the least write power consumption. The adoption of complementary pass transistors as the access device, in place of the conventional transistors, accounts for the observed improvement in read and writes delays. 8TS SRAM is observed to have the highest write power consumption, while proposed 8T SRAM has a decent power consumption of 10.4 nW.

Static Power Consumption

It is the power consumed when the SRAM cell is in idle state. It is basically due to the accumulation of leakage currents in the MOS transistors hence also known as leakage power consumption. It is calculated as the leakage current during idle state multiplied by the supply voltage value.

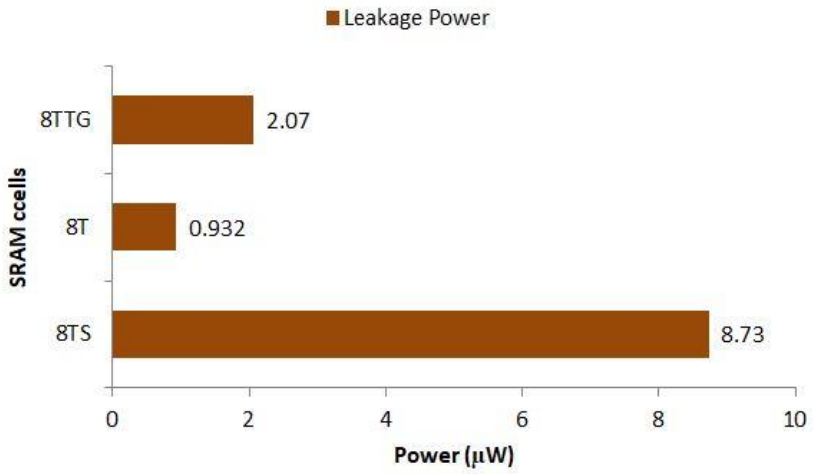


Fig. 5.18: Comparison of static power consumption of SRAM cells with same transistor count

As evident form the graphical representation of the comparison shown in Fig. 5.21, the conventional 8TS cell was observed to have the highest leakage power consumption at 8.73 µW. The proposed 8T SRAM cell was found to have the least leakage power of 0.932 µW followed by the proposed 8TTG SRAM cell. The 8TTG SRAM cell has slightly higher leakage power mostly due to absence of transistors with high threshold voltage in the design.

5.3 SUMMARY OF RESULTS

In this chapter, the proposed SRAM cell is compared against five other existing SRAM cell architectures, two of them with the same number of transistors and other three with varying number of transistors. Thus, the comparison is divided into two sections for better understanding. They were simulated them using the same technology node, supply voltage and under other conditions similar in all the topologies. Certain performance indicating parameters like access delay, Static Noise Margins (SNMs), power consumption, response

to temperature and supply voltage variations are used as the basis for the comparative study. Important results of the study include the following:

- Graphical interpretations are used to illustrate how the proposed SRAM cell fare against the existing models in terms of Static Noise Margins (SNM). The RSNM and HSNM for the proposed cell are 140.8 mV and 143.8 mv respectively. The SRAM cell with the highest RSNM and HSNM value is the 7T SRAM cell at 177mV and 178.9 mV respectively because of its design solely meant for good read and hold stability. The Write Margin (WM) for the proposed cell is 450 mV and 399 respectively which is very close to the ideal value.
- The proposed SRAM cell is found to have the least access delay during the read operation compared to the other existing SRAM cells. It is recorded to have a read acces delay value of 84 pS. The write access delay also comes second only to the transmission gate based 8T SRAM cell with a value of 124 pS.
- When all the SRAM cells were put under the same supply voltage variations and temperature variations, the proposed 8T SRAM cell is found to have a very sturdy and consistent noise margin performance overall, certainly better than that of other models.
- Power consumptions were also found to be very less in both cases, that is, dynamic and static power consumption. It was certainly found to be the least overall. Static power consumption for the proposed cell is recorded at a very least value of 0.932 μW. Read and write dynamic power consumptions are recorded at a value of 12.8 μW and 10.4 nW.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

The thesis work is concluded with this chapter that consists of two sections. Section 6.1 gives a conclusive detail of the main findings and the results obtained from this research work. Section 6.2 highlights the scope of expansion that can be done in the future with regards to this thesis title.

6.1 CONCLUSION

In this research work, various existing SRAM cell architecture are reviewed comprehensively to analyze their working and their performances. One of the purposes of reviewing them is to use them as a motivation in the designing of the suggested SRAM cell architecture. The suggested 8T SRAM cell is then simulated alongside the existing SRAM cells under the same conditions such as supply voltage, technology nodes, temperature variations, etc. The simulations were performed on various parameters to observe how the proposed 8T SRAM architecture fares against the existing SRAM architectures.

First, the comparison is made with regards to noise margins. In comparison to both classes of existing SRAM cells considered, one with different transistor counts and the other class with same transistor count, the proposed 8T SRAM is found to be the most consistent one maintaining a very good all round noise margin value for three types of noise margins. This is evident from graphical representations shown in prior chapters. The RSNM and HSNM for the proposed cell are 140.8 mV and 143.8 mv respectively. The other existing models would be better in RSNM/HSNM but would be very poor in WM or vice versa, hence consistency was the problem.

Second, the read and write delay of the proposed 8T SRAM cell is found to be the least in comparison to the other existing models with 84 pS and 126 pS respectively. The read access delay is lesser than that of 6T/ 7T/ 8TS/ 8TTG/ 9T SRAM cells by 12.5%/ 3.33%/ 1.18%/ 12.13%/ 8.49% correspondingly. The write access delay of the suggested 8T SRAM cell is

better than those of 6T/ 7T/ 8TS/ 9T SRAM designs by 39.1%/ 9.4%/ 9.67%/ 8.49% respectively.

Third, when the four models were put under supply voltage variations, the suggested 8T SRAM cell experienced the least variation of RSNM and HSNM as shown in graphical representations. However, the trend for Write Margin (WM) is the same as that of other existing SRAM cells. Fourth, with respect to temperature variations on the SRAM cells, the suggested 8T SRAM cell had the a very low variation of HSNM, RSNM at 0.77 mV/°C and 0.79 mV/°C and WM (average of variation of WM-1 and WM-0) at 0.58 mV/°C which is on par with the least variations possible among the existing SRAM cells.

Last but not the least, in terms of power consumption, the suggested 8T SRAM cell was observed to consume the least dynamic power read and write operation at 12.8 μW and 10.4 nW respectively. The static power consumption was also very less with a value of 0.932 μW almost equal to the least value obtained by 7T SRAM cell at 0.909 μW. Thus, considering the overall analysis of the results, the proposed 8T SRAM cell is the most consistent in terms of its performance and is the preferred SRAM architecture compared to the other existing SRAM cells.

6.2 FUTURE SCOPE

In this research work, The proposed SRAM cell outperforms the other three existing designs in terms of most of the considered performance indicators. But as future scopes of improvement always exist in any type of research, our research too has various scopes of improvement for the future. Some important future scopes worth highlighting are:

- Comparison of the proposed SRAM cell with more existing SRAM cells by considering various types of SRAM cell architecture types such as single ended, differential ended, dual port and single port. This is required to further get the assurance that the proposed cell is indeed a guaranteed superior model.
- More advanced performance indicating parameters in addition to the ones used currently can be used for comparison purposes to understand if the proposed model is superior in other aspects as well.

- More existing SRAM cell models can be comprehensively studied and simulated to understand their workings and their advantages in certain parameters as well as complications and shortcomings the cells have.
- The configuration of the transistors forming the SRAM cell can be changed and readjusted to see how the parameters are affected by each configuration. This also includes changing the number of bitlines used to perform read and write operations.

LIST OF PUBLICATIONS

SCOPUS INDEXED CONFERENCES

1. D. Usham and M. Bansal, "Low Power, Highly Stable and Enhanced Read Speed 7T SRAM," 2022 International Conference on Automation, Computing and Renewable Systems (ICACRS), Pudukkottai, India, 2022, pp. 162-167, doi: 10.1109/ICACRS55517.2022.10029285. (**Published in IEEE Xplore, Scopus Indexed**)
2. D. Usham and P. Mittal. "Low Power and Robust 8T SRAM with Enhanced Access Speed", 7th International Joint Conference on Computing Sciences (ICCS-2023), May 2023. (Accepted, Scopus Indexed)
   Status of Paper: Presented in the conference on 5th May, 2023
3. D. Usham and P. Mittal, "A Low Power Single Ended And Dual Port 8T SRAM With Robust Features", The international Conference on Advances in Management, Engineering and Renewable Energy (ADMIRE-2023), June 2023. (Submitted, Awaiting Acceptance)

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