DESIGN OF A NOVEL TERNARY D FLIP-FLOP BASED ON GNRFET

A DISSERTATION

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CANDIDATE'S DECLARATION

I, Shashank Pathak, Roll No. 2K19/VLS/16, student of M.Tech (VLSI Design & Embedded Systems), hereby declare that the project Dissertation titled "**Design of a novel Ternary D Flip-Flop based on GNRFET**" which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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Date: 30-08-2021

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CERTIFICATE

I hereby certify that the Project Dissertation titled "**Design of a novel Ternary D Flip-Flop based on GNRFET**" which is submitted by Shashank Pathak, 2K19/VLS/16, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date: 30-08-2021

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I take enormous delight in extending my acknowledgement to my family and friends who have helped me throughout this project work.

SHASHANK PATHAK
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ABSTRACT

For decades, computing logic uses Binary circuits based on Complementary metal-oxide semiconductor (CMOS) technology. However, as the trajectory of Moore's law is ascending, classical Binary logic and CMOS technology fail to cope with the VLSI industry's advancements. Multiple-Valued Logic (MVL), along with Graphene Nano Ribbon Field Effect Transistor (GNRFET) technology, have the potential to become the successor of classical CMOS technology. MVL, with its high information density and GNRFET's many characteristics, like its high Ion-Ioff ratio, low propagation delay, and adjustable threshold voltage, makes them an ideal combination to take over current technology.

Latches and Flip-Flops are the essential parts of any digital computational applications for real-time data processing systems. Hence designers try to make an efficient Flip-Flop design based on the trade-off between the design constraints like speed, power, and area. In this project, two new designs of Ternary D Flip-Flop (TDFF) are proposed and compared with their predecessors based on Power Consumption, Propagation Delay & Transistor Count. All the circuits are simulated & analysed in HSPICE using the GNRFET model present on the Nanohub website.

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LIST OF ABBREVIATIONS

VLSI:	Very Large Scale Integration
FET:	Field-Effect Transistor
GNRFET:	Graphene Nano-Ribbon Field-Effect Transistor
CMOS:	Complementary Metal Oxide Semiconductor
MVL:	Multiple-Valued Logic
Trit :	Ternary Digit
CNTFET:	Carbon Nano Tube Field Effect Transistor
TDFF:	Ternary D Flip-Flop
TDL:	Ternary D Latch
STI:	Standard Ternary Inverter
FF:	Flip-Flop
TG:	Transmission Gate
PDP:	Power Delay Product
STL:	Standard Ternary Logic
BTL:	Balanced Ternary Logic
NTI :	Negative Ternary Inverter
PTI :	Positive Ternary Inverter
NMOS:	N Channel Metal Oxide Semiconductor (FET)
PMOS:	P Channel Metal Oxide Semiconductor (FET)
N-GNRFET:	N Channel Graphene Nano-Ribbon Field-Effect Transistor
P-GNRFET:	P Channel Graphene Nano-Ribbon Field-Effect Transistor
PTDL:	Positive Ternary D Latch
NTDL:	Negative Ternary D Latch
RF:	Radio Frequency
GNR :	Graphene Nano-Ribbon
ZGNR:	Zig-Zag Graphene Nano Ribbon
AGNR:	Arm-Chair Graphene Nano Ribbon

CHAPTER 1
INTRODUCTION

1.1 BACKGROUND

In the present age, the VLSI industry is achieving new heights and keeping up with the ascending Moore's law trajectory is getting very hard. As the physical and electronic property of devices are shrinking new challenges keeps coming up. One of the most concerning challenge faced by VLSI circuit and system designers is to design innovative products while keeping the power consumption low with no compromises on area and delay constraints. The concern of power dissipation has been part of the design process since the 1970s but it was only towards the end of the century that it became the main design concern [1].

Binary logic is the backbone of all digital circuits since the dawn of the VLSI industry. As the transistor density in a chip is rising, it is struggling to maintain up with the progress. In an instance, it can process only 2 levels of information while MVL (Multiple-Valued Logic) can process multiple values in an instance, providing an edge over the former. The most efficient radix for the computation system is discovered to be 'e' (2.71828) for some specific circumstances. Since '3' is the closest integer to 'e' so it can be the most efficient integer radix for the system [2]. Interconnections comprise around 70% of the chip space in binary circuits. [1]. This inflicts some limitation on Fabrication and Logic implementation, MVL provides some relaxation in this as a Ternary digit (Trit) has $\log_2 3$ times more information than a Bit. Other than that, Ternary computation is $\log_2 3$ (1.585) times faster than Binary [3].

On the device level, many devices and techniques such as GNRFET, CNTFET, Spin-wave architecture, Single-electron devices, Quantum Computing etc. are developed in order to replace the CMOS technology. Among these new techniques

GNRFET operate satisfactorily and provide the best trade-off in terms of energy efficiency and circuit speed. Further, the property of GNRFET to manifest different threshold voltages at different Dimer Line configuration makes them the ideal candidate for implementing MVL technologies [4]. GNRFET also has an ambipolar nature due to its Quasi-ballistic electronic property and the same mobility of charge carriers in both n type channel and p type channel [5].

In this project two different TDFF designs have been proposed. These designs involve Ternary D Latch formed by STI gates, Pass gates and Transmission gates. Further these two designs are compared with their prevalent design in terms of speed area and power consumption.

All the simulations and analysis of the proposed Flip-Flops (FF) are done using HSPICE by considering the 3 ribbon GNRFET model present on Nanohub website [4].

1.2 OBJECTIVE

- To Design a Ternary D Flip-Flop (TDFF) based on GNRFET with low power consumption, less delay & least Transistor count.
- To investigate proposed designs in terms of following measurements:
  - Average Power Consumption
  - Delay
  - Power Delay Product (PDP)
  - Number of Transistors
- To do Comparative Analysis of proposed TDFFs with its CMOS, CNTFET & GNRFET predecessors.

1.3 ORGANIZATION OF THE REPORT

This thesis of Design of a novel Ternary D Flip-Flop is sorted out in five sections. chapter 1 gives you the outline of the proposed work.

In chapter 2, a brief introduction about Ternary Logic has been provided. It also describes the Ternary logic gates and their implementations.

In chapter 3, Graphene and GNRFET has been described. Further, it also describes the GNRFET implementations of Ternary Logic.

In chapter 4, proposed designs of TDFF are explained. The results are compared with the prevalent designs.

In chapter 5, the conclusion and future scope of presented designs are discussed.

CHAPTER 2
TERNARY LOGIC

Multiple-Valued Logic (MVL) and its' applications have been studied extensively over the last couple of decades due to the ability of the MVL logic devices to provide an exponentially higher information density compared to the binary logic. Multiple valued logic can be ternary (radix 3), quaternary (radix 4), quinary (radix 5), etc. However, ternary and quaternary logic systems have drawn much attention from the research community. The ternary logic system appears to be the most feasible MVL system that can be adopted in the near future because of its simplicity and ease in distinguishing different logic levels as in the binary system. Ternary Logic & its Logic gates are discussed in this chapter.

2.1 INTRODUCTION

In a Binary logic system, there exists two logic levels to decide the value of a variable. These levels are as follows: High (1) and Low (0). To keep up with the ascending trend in VLSI we have to think beyond Binary. The current Binary logic system has to be replaced by a much better MVL system, having "M" different logic levels. Here M > 2. These different logic levels present information about various signal variables. One such form of MVL system is the Ternary logic system, in which there are three logic levels (M = 3). On comparing with Binary logic, Ternary logic has shown better results in following fields: improved data processing ability per unit area, flexibility with design, less delay, less area, less power consumption, less interconnection complexity, and less active devices in a chip [6].

Ternary logic implementation in digital logic circuits can be classified in two different types:

1. Standard (Balanced) Ternary Logic
2. Balanced Ternary Logic

2.1.1 Standard Ternary Logic

Standard Ternary Logic (STL) is derived from Binary logic by extending a logic value to the value set in order to process more information. In a Binary logic 0 and 1 are used while in a STL the logic levels are denoted by 0, 1 and 2. STL symbols and associated information is shown in below table 2.1. STL is used in proposed design.

Logic Symbol	Information
0	FALSE
1	INTERMEDIATE
2	TRUE

TABLE 2.1: Standard Ternary Logic symbols and associated information

2.1.2 Balanced Ternary Logic

Balanced Ternary Logic (BTL) is a signed Ternary Logic in which we use -1, 0 and +1 for the logical expressions. It provides an advantage over the former by handling negative numbers better. Further it makes the calculations simpler. BTL symbols and associated information is shown in below table 2.2.

Logic Symbol	Information
-1	FALSE
0	INTERMEDIATE
+1	TRUE

TABLE 2.2: Balanced Ternary Logic symbols and associated information

2.2 TERNARY LOGIC GATES

Just like the Binary number system, Ternary logic system also has logic gates to perform desired operations on the provided information. In this project Standard Ternary Inverter (STI) along with Pass Transistors and Transmission gates is used.

2.2.1 Standard Ternary Inverter

Inverter is the most basic gate in a logic system. It inverts the data provided on the input node. In Ternary Logic system there exists three types of inverters:

1. Negative Ternary Inverter (NTI)
2. Positive Ternary Inverter (PTI)
3. Standard Ternary Inverter (STI)

Functionality of the inverters can be understood by following set of equations:

$$O_N = f_N(a) = \begin{cases} 2, & a = 0 \\ 0, & a \neq 0 \end{cases} \quad (2.1)$$

$$O_P = f_P(a) = \begin{cases} 2, & a \neq 2 \\ 0, & a = 2 \end{cases} \quad (2.2)$$

$$O_S = f_S(a) = \bar{a} = 2 - a \quad (2.3)$$

Here in these equations a is the input. O_N is the output of NTI, O_P is the output of PTI & O_S is the output of STI [7, 8]. The Truth table of the Inverters are shown in below Table 2.3.

Input (a)	**STI (O_S)**	**PTI (O_P)**	**NTI (O_N)**
0	2	2	2
1	1	2	0
2	0	0	0

TABLE 2.3: Ternary Inverters Truth Table

In proposed design, Standard Ternary Inverter is used. Symbol of STI gate is shown below in Fig. 2.1.

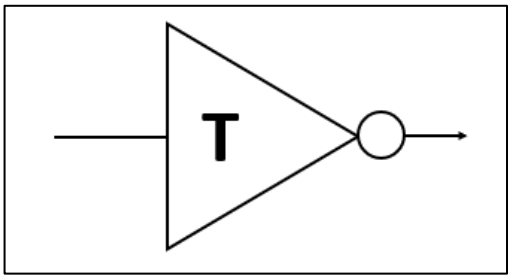

Fig. 2.1: Symbol of Standard Ternary Inverter

2.3 PASS TRANSISTOR

Transistors are called Pass Transistors when they are used as a switch to connect two nodes conditionally [9]. The control signal is provided at the gate of transistor, while the data is provided either at the drain or the source. The Body or Substrate terminal is connected to either low or High logic. Pass Transistors can be implemented by:

1. NMOS (N-GNRFET) as a Pass Transistor
2. PMOS (P-GNRFET) as a Pass Transistor

In CMOS based circuits NMOS is preferred due to its high speed but in GNRFET both can be used due to its ambipolar nature.

NMOS (N-GNRFET) transmits the data when gate signal is high and stays in Cut off if the gate signal is low. NMOS (N-GNRFET) has poor low-to-high characteristics that's why it passes a poor high signal (2). In terms of ternary logic system, if the input is 2 (V_{dd}), it passes a poor 2 or the output is $V_{dd} - V_t$. Body Terminal is connected to the lowest voltage node in the circuit for NMOS (N-GNRFET).

PMOS (P-GNRFET) transmits the data when gate signal is low and stays in Cut off if the gate signal is high. PMOS (P-GNRFET) has poor high-to-low characteristics that's why it passes a poor 0. In terms of ternary logic system, if the input is low (0), it passes a poor 0 or the output is V_t. Body Terminal is connected to the highest voltage node (V_{dd}) in the circuit.

Pass Transistors provides a high reduction in area and power over other designs. It also enhances the operating speed of the design. The only drawback of pass transistor is weak logic level transfer.

2.4 TRANSMISSION GATE

Transmission Gate (TG) or Analog switch is used in order to overcome the issue of weak logic level transfer in Pass Transistors. In TG an NMOS (N-GNRFET) and a PMOS (P-GNRFET) are connected in parallel. NMOS (N-GNRFET) & PMOS (P-GNRFET) restores the logic level when the other Transistor is passes a weak logic level. Schematic diagram of a Transmission gate is shown in Fig. 2.

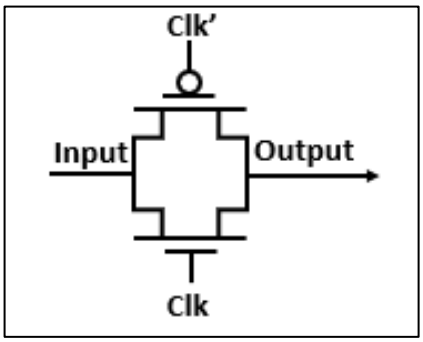

Fig. 2.2: Transmission Gate

The control signal is provided on the gate terminal of both the NMOS (N-GNRFET) & PMOS (P-GNRFET). For the proper functioning of TG, we need two separate non overlapping & inverted clocks. To overcome the Body effect, Body or Substrate of PMOS (P-GNRFET) is connected to Vdd and for NMOS (N-GNRFET) is connected to ground.

2.5 TERNARY D LATCH

In a Digital circuit, Latch is the most basic blocks used to store information. It has the ability to hold one bit (Trit in our case) data. Ternary D Latch (TDL) is a level sensitive device. A TDL works in two different modes:

1. Transparent Mode
2. Hold Mode

When the Enable signal is high, the TDL comes in Transparent Mode. A direct path is provided from input node to output node with the help of a switch. Since new data propagates from input to output node, this mode is called Transparent Mode.

When the Enable signal is low, the TDL comes in a Hold mode. The previous data is feed through a feedback loop which is controlled by another switch. Since the old data is stored at the output node, this mode is called Hold mode.

Just like the Binary latch, Ternary D Latch can also be classified into two types:

1. Positive Ternary D Latch (PTDL)
2. Negative Ternary D Latch (NTDL)

Since we are using a Binary Clock to control TDL. A Ternary D Latch is called Positive Ternary D Latch (PTDL) when it enables at high (V_{dd}) logic level. A Ternary D Latch is called Negative Ternary D Latch (NTDL) when it enables at low (0) logic level. The Truth table of TDL is shown below in Table 2.4.

ENABLE (PTDL/NTDL)	MODE	INPUT	OUTPUT	OUTPUT'
HIGH (2/0)	TRANSPARENT	0	0	2
		1	1	1
		2	2	0
LOW (0/2)	HOLD	X	Output (previous)	Output' (previous)

TABLE 2.4: Truth Table of Ternary D Latches (TDLs)

2.6 TERNARY D FLIP-FLOP

Just like Latches, Flip-Flops are also used to store information in Digital circuits. It can store one bit (Trit in our case) data. While a TDL is level sensitive, Ternary D Flip-Flop (TDFF) is an edge sensitive device. It comes in Transparent mode on a certain transition (edge) of clock. Otherwise, it stays in Hold mode and store the previous value of the output.

TDFFs are classified into two different types:

1. Positive-Edge Triggered TDFF
2. Negative-Edge Triggered TDFF

Positive-Edge Triggered TDFF comes into Transparent mode when there is low-to-high (0→2) transition in clock. Negative-Edge Triggered TDFF comes into Transparent mode when there is high-to-low (2→0) transition in clock.

A TDFF can be formed by cascading Two TDLs in Master-Slave configuration. In a Master-Slave configuration first Latch act as Master and the cascaded Latch act as a slave to the previous one. For a Positive-Edge Triggered TDFF a PTDL is cascaded after a NTDL. NTDL will act as a Master Latch and PTDL will act as Slave Latch.

For Clock = 0, NTDL will be Transparent and PTDL will be in Hold mode. Input data will be stored in an intermediate node. As PTDL is in Hold mode, data at output will be same as old one.

For Clock = 1, NTDL will be in Hold mode and PTDL will be Transparent. Input data stored in an intermediate node will propagate to the output node with the Transition. NTDL will store the previous value.
Consequently, both the latches act as a Positive edge-triggered TDFF.

Clock	MODE		OUTPUT	OUTPUT'
0 → 2	**TRANSPARENT**	0	0	2
		1	1	2
		2	2	0
2 → 0	**HOLD**	**X**	Output (previous)	Output' (previous)

TABLE 2.5: Truth Table of Positive Edge Triggered Ternary D Flip-Flop

The Truth table of Positive-Edge Triggered TDFF is shown above in Table 2.5. Two Positive-Edge Triggered TDFF designs are explored in this project.

CHAPTER 3
GNRFET TECHNOLOGY

Graphene Nano Ribbon Field Effect Transistor (GNRFET) is Graphene based Field Effect Transistor. The qualities of GNRFET which makes it better than its predecessors are its high speed, less power consumption and small area. Further its ability to manifest different threshold voltage by controlling width of Graphene Nano Ribbons (GNRs) and its ambipolar nature makes it an ideal candidate for Ternary logic. Properties of Graphene & GNRFET are discussed in this chapter.

3.1 GRAPHENE

Single layered Graphene, a shed composite of carbon, catches the limelight in 2004, considering the way that the primary dimensional surface with hanging advanced, magneto-electronic and optoelectronic properties. Due to extravagant transportability ballistic vehicle, speedy state trading by virtue of especially high administration adaptability and electrostatic decrease in perspective on the 2d structure, Graphene based gadget shave a promising future in supplanting standard CMOS nano hardware.

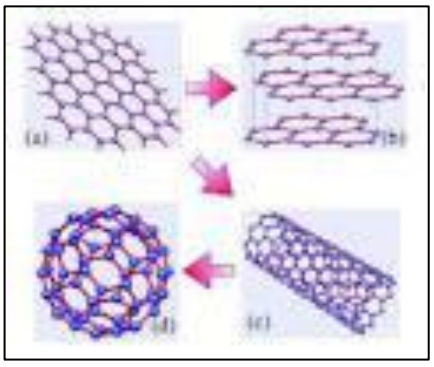

Fig. 3.1: Structure of Graphene

Graphene is a semi metal (zero opening semiconductors) with charge transporters carrying on as massless Dirac fermions. Underneath charge absence of predisposition conditions, the Fermi degree is at the square endeavor to the valance and conduction gatherings, yet may be moved with the utilization of a vertical electric controlled order to make a larger piece of openings or electrons. An advancement of the entryway coefficient from practical to horrendous characteristics is resolved. Graphene notable shows incredibly in ordinate provider motility at room temperature because of a vulnerable electron telephone on affiliation. The convenience of shed Graphene becomes recommended to be 100,000 cm 2V-1s-1 (On protected substrates) and 230,000 cm 2V-1s-1 for suspended structures. Graphene surely understood a warm conductivity of 5300Wm okay at room temperature.

The chance of band opening building in GNR pushes the material for good measured future use in nano-electronic circuits on account of its recognized qualities which fuse tremendous administration compactness and planar shape. Graphene a two-dimensional material is engineered in a honeycomb pearl grid. It has various specific homes. These particular home shave made this material a potential chance for different bundles, for instance electronic gadgets, nano-gadgets and dispatch. In any case not withstanding giving superb achievements in fantastic fields, a fundamental disadvantage of zero band holes limits its general execution. Graphene transistors ordinarily called as Graphene FETs display better by and large execution parameters in RF devices and correspondence structures due to its astoundingly high provider mobilities, am bipolarity, high warm conductivity and subsequently outperform the standard Si-based FETs. These transistor devices the use of graphene in like manner are totally used to as the arrangement silicon transistors. In any case, regardless of getting the incredibly extraordinary homes, it encounters its zero-band opening.

This zero-band gap makes the trading way hard and in like way the ON−OFF extents of those gadgets are nearly nothing. The low on off extent in such gadgets does never again permit turn off and fittingly power wastage happens and results in all things considered execution defilement. The decrease all in all execution defilement can be finished with the guide of building up appropriate band gap in graphene. The outlet of band opening in graphene is finished by methods for different methodologies.

Course of action of graphene nano ribbons is one among such method. This is practiced with the guide of encircling parts of graphene by method for decreasing the width of graphene sheet. Decrease in the width of graphene sheet presents band hole right now opening surface as GNRs along the side limits the development of venders and instigate equity hole that is alternately comparative with the width of the ribbon. As width of the ribbon diminishes, the band hole of graphene will increase with the lower. Graphene Nano ribbons are of two sorts. These can be either Zigzag (ZGNRs) or Armchair (AGNRs). The advanced homes of these graphene nano ribbons can be considered by using the width and the geometry of the GNR along their edges. These additionally have an element desert that is a basic parameter to mull over as the edge flaws prompts for the most part execution shakiness. ZGNRs are steel even as the AGNR are made semiconducting in nature. Graphene nano ribbons have fundamental bundles in electronic devices containing subject effect transistors. GNR based subject effect transistors is one of the normal Field Effect Transistor which depends upon graphene/graphene nano ribbons. Correspondingly a FET, it additionally has the 3 terminals alongside channel, source and the gate.

In an Armchair GNR, the number of Dimer lines (N) affects the ribbon's electrical properties. The GNR will behave like a metal if $N = 3p + 2$, where p is an integer. However, if $N = 3p$ or $3p + 1$, it will show semiconductor like behavior[10,11]. Fig. 3.2 shows the Dimer Line configuration in Armchair GNR.

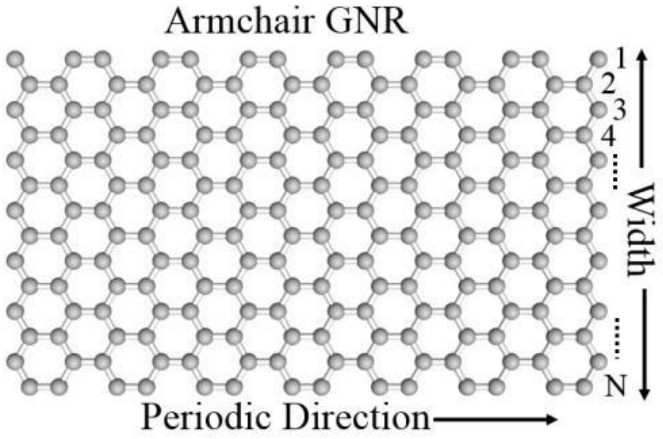

Fig. 3.2: Dimer Lines in Armchair GNR [12]

Graphene nano-ribbons have noteworthy applications in electronic gadgets including issue sway transistors. GNR based completely issue sway transistors is one of the not odd transistors dependent on graphene/graphene nano-ribbons. In like manner FET, it besides has the three terminals related to deplete.

3.1.1 Intrinsic & Extrinsic Graphene

It has one of kind limits, so it's basic to perceive among inward and outward Graphene. Gapless graphene (both mono layer MLG or bilayer BLG) has a charge fairness factor (CNP) i.e., the Dirac factor, where its character modifications from being electron need to being unfilled individually. see: Density of conditions of graphene is close to the Dirac point. Any such differentiation isn't important for a2D EG (or BLG with a colossal hole) considering the way that the regular gadget is actually an undoped gadget without an association (and accordingly is dull from the computerized dispatching living courses of action perspective).

In monolayer and bilayer graphene, the ability to gate (or dope) the machine through placing associations in to the conduction or valence band with the guide of tuning an outside gate voltage enables one to pass by methods for the CNP in which the invention limit (EF) is living precisely at the Dirac point. This structure with no loosened venders atT"0", and EF definitely at the Dirac point is all used to as trademark graphene with a completely packed (empty) valence (conduction) band.

3.2 GNRFET

3.2.1 Structure of GNRFET Device

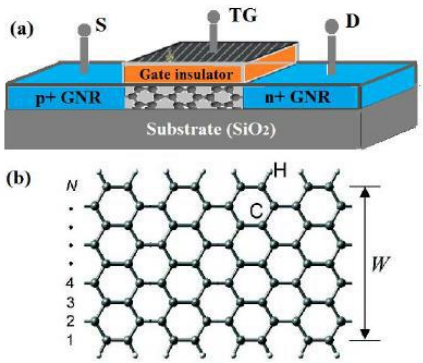

Fig. 3.3: GNRFET a) Transistor structure. b) GNR Lattice

The primary area of implementing Graphene based FET begin in 2007. The GNRFET gadget structure is fundamentally the same as MOSFET and is appeared in Figure 3.3. Regular Source design is portrayed in the Figure. The positive voltage at the back gate prompts the electron direct development in the GNR. The drain current is constrained by voltage at the top gate. The essential electron thickness is actuated by the back gate voltage. Numerous channels of GNR are designed on the substrate framing a multi-channel gadget [13].

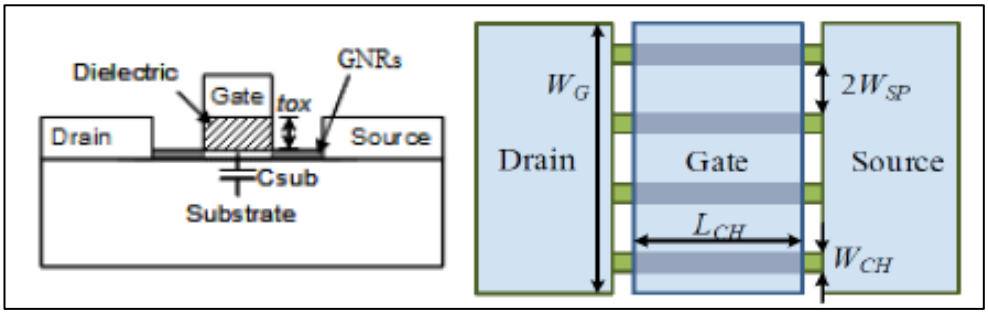

Fig 3.4: Structure of three ribbons GNRFET

A MOS type GNRFET with three armchair GNRs acting as the channel is presented in fig 3.4. The GNR channel, under the gate, is of intrinsic nature. The ribbon parts that connect the gate with the contact are called the Reservoirs and they are heavily doped. The voltage applied on the gate determines the state of the Transistor, whether it is on or off. The relation between Threshold voltage (V_{th}) of the transistor, Band Gap (b_g) and Electron charge (e) is given by equation (3.1).

$$V_t = b_g/3e \qquad (3.1)$$

Bandgap b_g can be expressed as equation (3.2):

$$b_g = 2\Delta E|\delta| \qquad (3.2)$$

The value of δ is 0.27, 0.4 and 0.66 for N equals to $3p$, $3p$ + 1 and $3p$ + 2, respectively. Here in eqn. (3.3), h is Plank's constant and v_f = 10^6 m/s [4].

$$\Delta E = \pi h v_f / W_{GNR} \qquad (3.3)$$

The drain current (I_D) in terms of Channel Potential (ψ_{CH}) , Drain Voltage (V_D) and Source voltage (V_S) in a GNRFET can be expressed by eqn. (3.4) [6].

$$I_D(\psi_{CH},\ V_D\ ,\ V_S\ ) = \frac{2qKT}{h}\sum_{\alpha}\left[ln\left(1+e^{\frac{q\,(\psi_{CH}-V_S)-\varepsilon_\alpha}{kT}}\right)-ln\left(1+e^{\frac{q\,(\psi_{CH}-V_D)-\varepsilon_\alpha}{kT}}\right)\right] \quad (3.4)$$

Here, ε_α=Sub-band edge, α = Sub-band index ($1 \le \alpha \le N$), k=Boltzmann's constant, and T=Temperature.

The threshold volage of GNRFET can be regulated by controlling the dimer lines which affects the ribbon width.

3.2.2 SPICE model of GNRFET

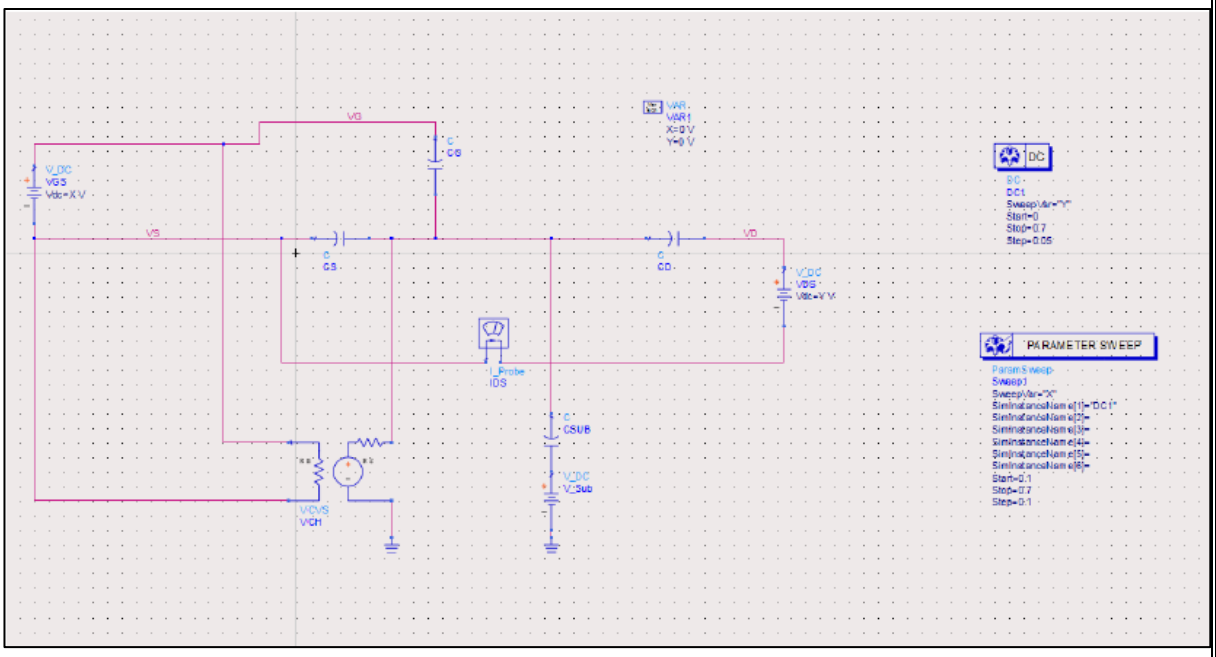

Fig 3.5: The SPICE GNRFET Model

The device SPICE model presented above was developed by the University of Illinois, Urbana, Champaign [4], where each device may have one or more Graphene Nano-Ribbons (GNRs). This SPICE model can be accessed at following link: https://nanohub.org/resources/17074 [4]. The minimum channel length is ~10 nm, as

various complex quantum mechanisms which describe the sub-10nm regime are not modeled here. Also, the model is based on the assumption of ballistic transport, which is only accurate in a short-channel GNRFET. As a result, we do not recommend setting channel length above 100nm. The device parameters that characterize its performance are:

1. V_{GS} is gate to source voltage.
2. V_{DS} is drain to source voltage.
3. I_{DS} is the current owing through the channel.
4. Capacitors C_G, C_D, C_S, C_{SUB} and V_{CH} are used to vary currents when the channel charges and discharges [4].

The channel width of the GNRFET is calculated based on the number of dimer lines in a graphene nano-ribbon [4] is given by the following equation:

$$W_{GNR} = (N-1) \times \left(\frac{\sqrt{3}}{2}\right) \times a_{c-c} \qquad (3.5)$$

Here (3.5), N = number of dimer lines & $\boldsymbol{a_{c-c}}$ is the lattice constant valued as 0.142nm.

. However, as the band gap of GNRs is inversely proportional to the width, a wide GNR would have a low $\mathbf{I_{on}/I_{off}}$ ratio and would no longer be suitable for digital circuits. Therefore, only recommended widths are up to N=50. The other parameters oxide thickness, line edge roughness, and doping fractions (for MOS-GNRFET only) were thoroughly tested in the ranges given in Table 3.1, and recommended settings of these parameters within these ranges [6,7].

Device Types	n-type/p-type GNRFET
Device Dimensions:	
Channel Length (Minimum)	~10nm
Channel Length (Maximum)	~100nm
Channel Width (Minimum) per GNR	~0.873nm (N=6)
Channel Width (Maximum) per GNR	~6.36nm (N=50)
Number of GNRs / device (Minimum)	1
Number of GNRs / device (Maximum)	Unlimited
Oxide Thickness (Minimum)	0.5nm
Oxide Thickness (Maximum)	2.5nm
Line Edge Roughness (Minimum)	0%
Line Edge Roughness (Maximum)	20%
Doping Fraction (Minimum)	0.001
Doping Fraction (Maximum)	0.015

Table 3.1: Summary of scope of GNRFET structure model [4]

3.3 GNRFET IMPLEMENTATION OF TERNARY LOGIC

The threshold value of a GNRFET varies depending on the width of the GNR. That means, controlling the number of dimer lines in the GNR which is acting as the channel in a GNRFET, the threshold voltage and I_{on} / I_{OFF} ratio can be manipulated [15]. The qualitative comparison of the electrical properties of GNRFET based on the number of dimer lines is given in Table below [14].

Dimer Lines (N)	**Band Gap**	**I_{on} /I_{off}**	**I_{on}**
8,11,14,17	Small	Low	Highest
6,9,12,15,18	Moderate	High	High
7,10,13,16	Highest	Highest	Low

TABLE 3.2: Characteristics variations of GNRFET with respect to Dimmer Lines

In this project, GNRFETs with three different threshold voltages has been used to gain the desired voltage levels [5].

N (Dimmer Lines)	V_{th} (N-GNRFET)	V_{th} (P-GNRFET)
7	0.59 V	- 0.59 V
9	0.24 V	- 0.24 V
10	0.4 V	- 0.4 V

TABLE 3.3: Characteristics of GNRFET used in this project

3.3.1: Standard Ternary Inverter Gate

In our project we have used STI gate. The schematic& symbol are on next page with the number of Dimer lines mentioned. Supply Voltage (V_{dd}) is 1 V.

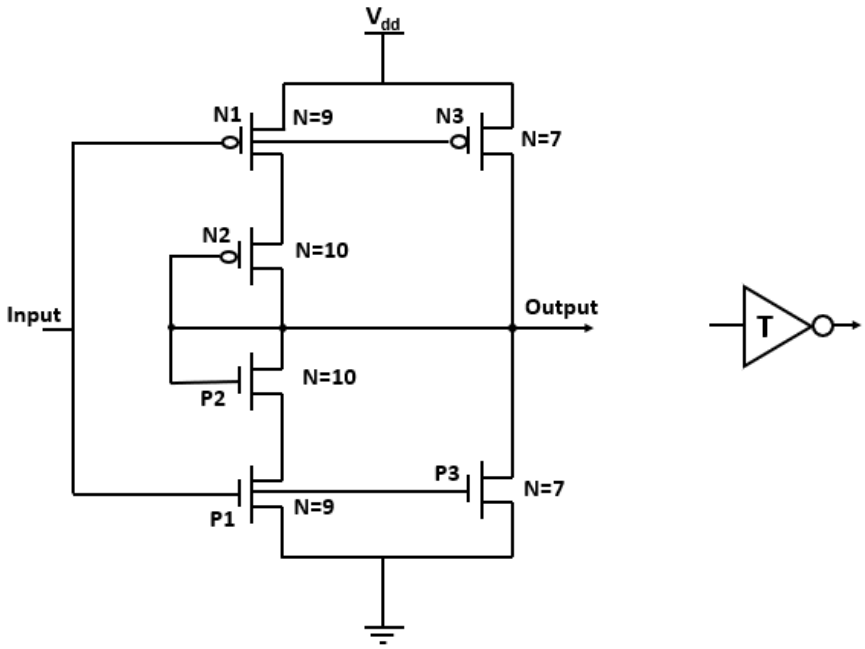

Fig 3.6: Schematic Diagram & Symbol of Standard Ternary Inverter using GNRFET [14]

Voltage Transfer Characteristics of implemented STI gate is shown below:

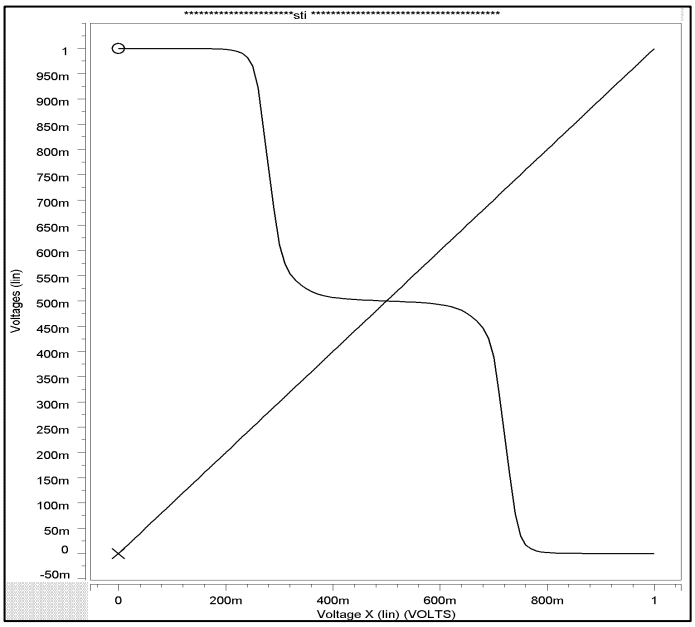

Fig 3.7: VTC of implemented GNRFET STI

From the figure we can infer that, for the input voltage variation from 0 to 1 V, the output voltage has three steps. Further this can also be verified by Transient response of implemented STI gate shown below:

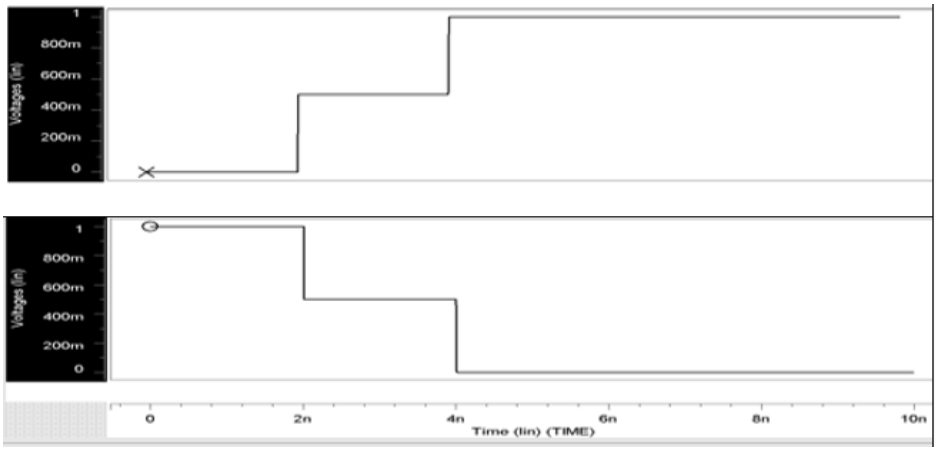

Fig 3.8: Transient Response of implemented GNRFET STI

In above figure, first plot is the input voltage & second plot is the output. For the steps 0V, 0.5 V & 1 V, we can see the output voltage is the inverse of the input signal. This

curve can be matched with the below Truth Table of STI gate so as to verify the functionality of implemented STI gate.

Input (Voltage)	Output (Voltage)
0 (0V)	2 (1V)
1 (0.5V)	1 (0.5V)
2 (1V)	0 (0V)

TABLE 3.4: Standard Ternary Inverter Truth Table & Voltage levels

CHAPTER 4
DESIGN AND IMPLEMENTATION

In a Digital circuit, Latches and Flip-Flops are the most fundamental elements used to store data. Both of them have the ability to hold one bit (Trit in our case) data. Since Latch is a level sensitive device, it acts in a transparent mode when it is enabled, and in a Hold mode when it's not enabled. On the other hand, Flip-Flop is edge triggered. In this chapter, two designs of Ternary D Flip-Flop (TDFF) are proposed and compared it with the other prevailing CMOS, CNTFET & GNRFET designs. First design is based on Transmission gate (TG) and other one is based on Pass Transistors. In the following section, TDFF based on TG & Pass transistors are proposed.

4.1 PROPOSED TDFF WITH TRANSMISSION GATES

This section proposes the design of Ternary D Latch (TDL) using Transmission gates & STI gates based on GNRFET. Further the TDLs are used to make Ternary D Flip-Flop (TDFF). The circuit is Node coded on HSPICE software using GNRFET SPICE model. A Piecewise Linear Ternary pulse is provided as the input and two binary Non-overlapping Pulses are given as Clock signal (0V- 1V) with the Period of 3 ns. After that, its Transient analysis is done to verify proper functionality of the circuit. Delay and Power calculations are done afterwards. For each transition, Delay is been calculated and then averaged. Power consumption is calculated as the total Power provided by the Voltage Source. Power Delay Product (PDP) is taken as the product of Average Delay and Power Consumption.

4.1.1 Ternary D Latch

Fig. 4.1 provides the schematic Diagram of the Positive Ternary D Latch (PTDL). From the fig it can observe that it consists of two STI gates and two Transmission Gates (TG1 & TG2). Number of GNRFETs used in this TDL design is 16. **TG1** is

provided with Clk signal on gate terminal of N-GNRFET & Clk' signal (Inverse of Clk) on gate terminal of P-GNRFET. **TG2** is provided with Clk' signal on gate terminal of N-GNRFET & Clk signal on gate terminal of P-GNRFET. Input signal is provided on **d** node output can be seen at **q** & **q'** node. At **q'** the inverse of output signal of **q** node is seen.

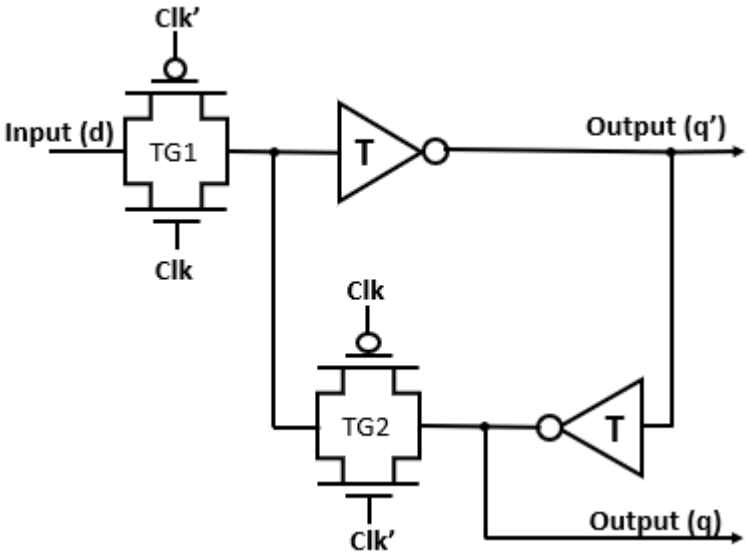

Fig. 4.1: Positive Ternary D Latch based on TG

Functionality of the proposed PTDL circuit is explained below:

At Clk = 1: (Transparent Mode)

(TG1 is ON & TG2 is OFF) Signal at Input node (**d**) will be inverted by STI and at **q'** the signal is inverted. It gets inverted again and at **q** we have the input signal. Since Input data is propagated to the Output nodes (**q & q'**), the latch is said to be in Transparent mode.

At Clk = 0: (Hold Mode)

(TG1 is OFF & TG2 is ON) No data propagate to the Output nodes (**q & q'**) from input node (**d**). Previously stored data propagates to Output nodes via TG2. Since previous data is sustained, the latch is said to be in Hold mode.

This TDL can be used Negative Ternary D Latch (NTDL) by inverting the Clk & Clk' at TG nodes (Gate terminals of N-GNRFET & P-GNRFET).
Functionality of the Ternary D Latch can be verified from the Transient response of the PTDL presented below:

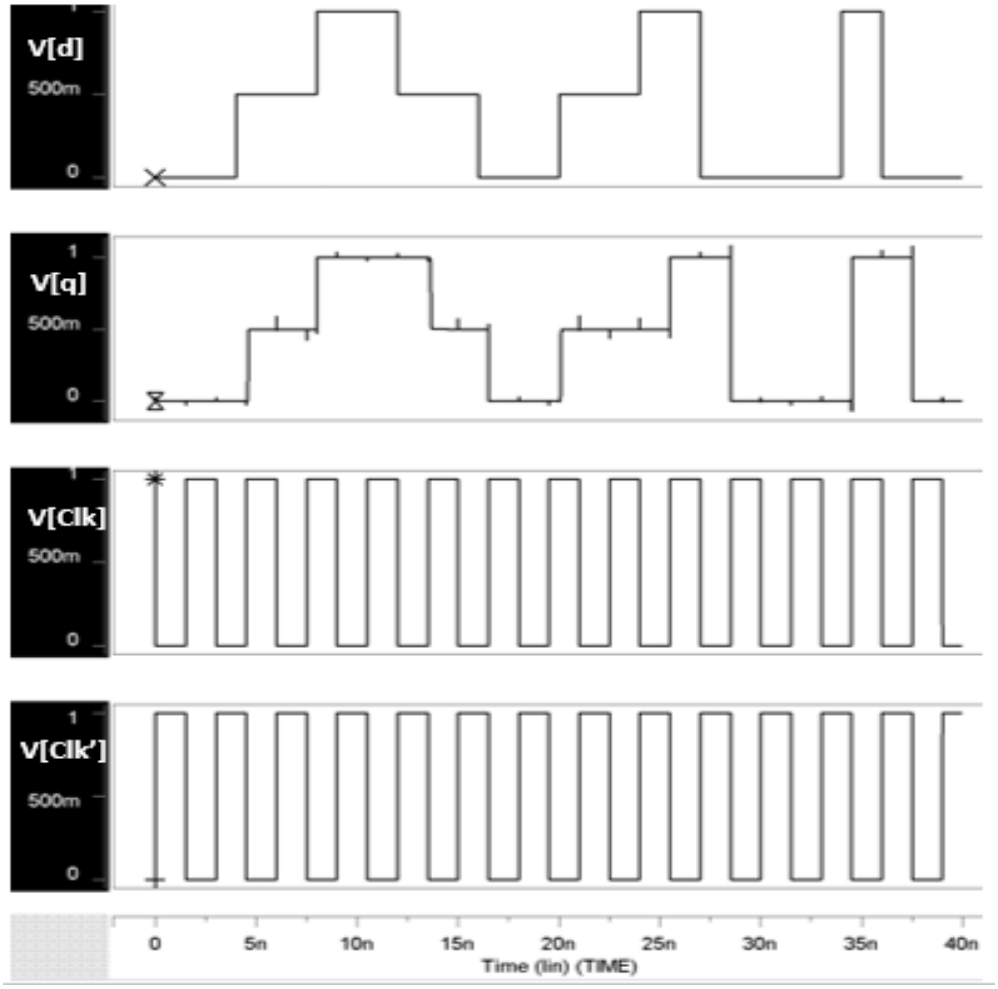

Fig. 4.2: Transient Response of Positive Ternary D Latch (PTDL) based on TG

In the above figure first plot is the input signal (Piecewise Linear with three voltage levels 0V, 0.5V & 1V) applied at node **d**. Second plot is the output at **q** node. Third plot is the Binary Clock (Period =3ns, Pulse Width = 1.5ns, Rise Time = 10 ps, Fall Time = 10ps) controlling the PTDL. We can observe that the output is changing in accordance with the input when the Clk signal is High & Clk' signal is Low. It is in Hold mode when the Clk signal is Low & CLk' signal is High. We can verify our Transient analysis by comparing the Plot with the Truth Table shown in next page.

Clk	MODE	d	q	q’
HIGH (2)	TRANSPARENT	0	0	2
		1	1	1
		2	2	0
LOW (0)	HOLD	X	**q**(prev)	**q’**(prev)

TABLE 4.1: Truth Table of proposed PTDL based on TG

4.1.2 Ternary D Flip-Flop

Fig. 4.2 provides the schematic diagram of the Positive Edge-Triggered Ternary D Flip-Flop (TDFF). From the fig we can observe that it consists of two TDLs connected in Master-Slave configuration. First TDL is a Negative Ternary D Latch (NTDL), it acts as Master Latch. Next TDL is a Positive Ternary D Latch (PTDL), acting as a slave latch. The design is made up of 4 STI gates & 4 Transmission gates. Input of Slave (PTDL) is taken from inverting node of Master (NTDL). Number of GNRFETs used in this TDFF design is 32.

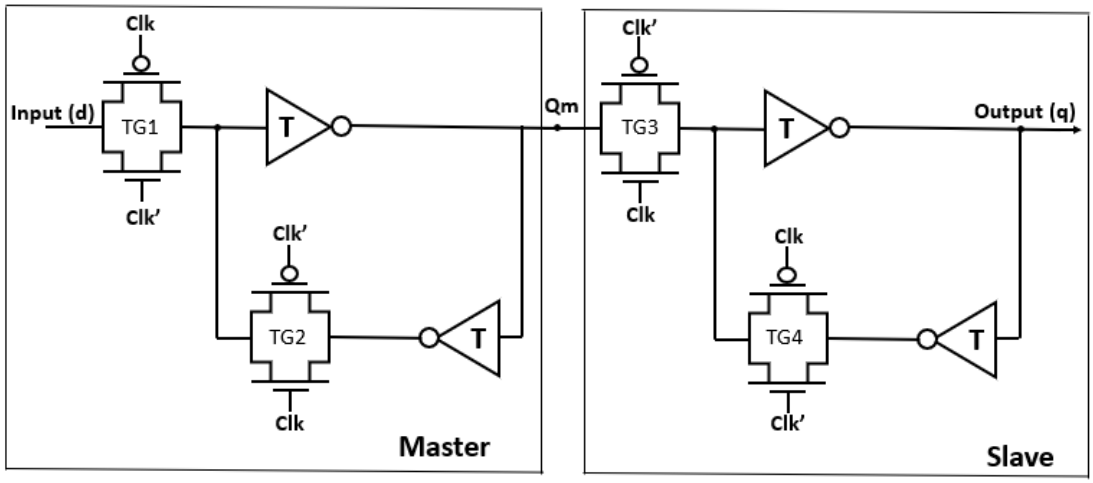

Fig. 4.3: Schematic Diagram of proposed TDFF based on TG

Functionality of the proposed TDFF circuit is explained below:

At Clk = 0: NTDL (Transparent Mode), PTDL (Hold Mode)

(TG1 & TG4 are ON, TG2 & TG3 are OFF) Signal at Input node (**d**) will be inverted by STI and we get inverted signal at Intermediate node (**Qm**). PTDL is in Hold mode so it will restore the previously stored value at Output node(**q**).

At Clk = 1: NTDL (Hold Mode), PTDL (Transparent Mode)

(TG1 & TG4 are OFF, TG2 & TG3 are ON). NTDL is in Hold mode so previously stored value at Intermediate node (**Qm**) will be restored. PTDL is in Transparent mode so the data at **Qm** will be inverted again to pass to the Output node. Thus, data at the input will be passed at Rising edge of the clock.

4.1.3 Simulation & Results

Fig. 4.4 presents the Transient Response of Proposed Ternary D Flip-Flop (TDFF).

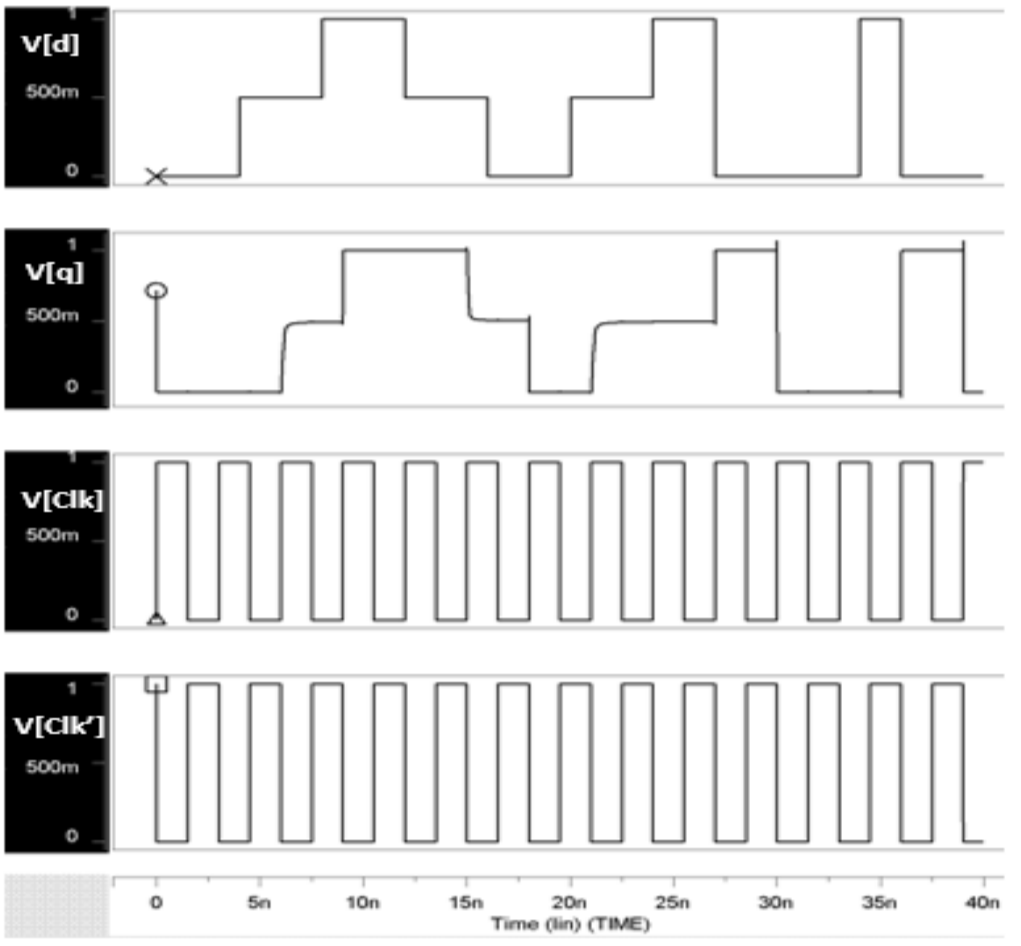

Fig. 4.4: Transient Response of proposed TDFF based on TG

In the Fig. 4.4, first plot is the input signal (Piecewise Linear) applied at node d. Second plot is the output at q node. Third plot is the Binary clock (Clk) controlling the PTDL. Fourth plot is the non-overlapping inversed clock of Clk named as Clk'. In the figure, we can observe that the output is changing in accordance with the input only when the Clk signal is changing from Low to High (Rising Edge) & Clk' signal is changing from High to Low (Falling Edge). TDFF is in Hold mode otherwise. We can verify our Transient analysis by comparing the Plot with the below Truth Table.

Clk	**MODE**	**D**	**q**	**q'**
0 → 2	**TRANSPARENT**	0	0	2
		1	1	2
		2	2	0
2 → 0	**HOLD**	**X**	q(prev)	q'(prev)

TABLE 4.2: Truth Table of proposed TDFF based on TG

The only problem in this design is the need of two non-overlapping clock signal, which is very hard to generate. To solve this issue, we have used Pass Transistors in our next proposed design.

Following are the Delay & Power calculations of proposed TDFF:

Transition Delay (ps)	**0 → 1**	102.6
	0 → 2	9.5
	1 → 0	5.8
	1 → 2	6.3
	2 → 0	7.5
	2 → 1	61.4
	Average	32.18
Average Power (μW)	0.479	
Power Delay Product (10^{-18} Joules)	15.41	
Number of GNRFETs	32	

TABLE 4.3: Power & Delay analysis of proposed TDFF based on TG

4.2 PROPOSED TDFF WITH PASS TRANSISTORS

This section proposes the design of Ternary D Latches (TDLs) using Pass Transistors & STI gates based on GNRFET. Further the TDLs are used to make Ternary D Flip-Flop (TDFF). This circuit is also Node coded on HSPICE software using GNRFET SPICE model. A Piecewise Linear Ternary pulse is provided as the input and a binary Pulse is fed to the circuit as Clock signal (Period = 3ns, Pulse Width = 1.5ns, Rise Time = 10 ps, Fall Time = 10ps). After that, its Transient analysis is done to verify proper functionality of the circuit. All Delay and Power calculations are done in the same way as in previous design. There is a reduction of 4 GNRFETs from the previously proposed design of TDFF.

4.2.1 Ternary D Latch

This section is divided into Two parts. In first section we will see the design of proposed Positive Ternary D Latch (PTDL) & in the second section we will see the design of proposed Negative Ternary D Latch (NTDL).

Positive Ternary D Latch (PTDL)

Fig. x presents the schematic diagram of the PTDL.

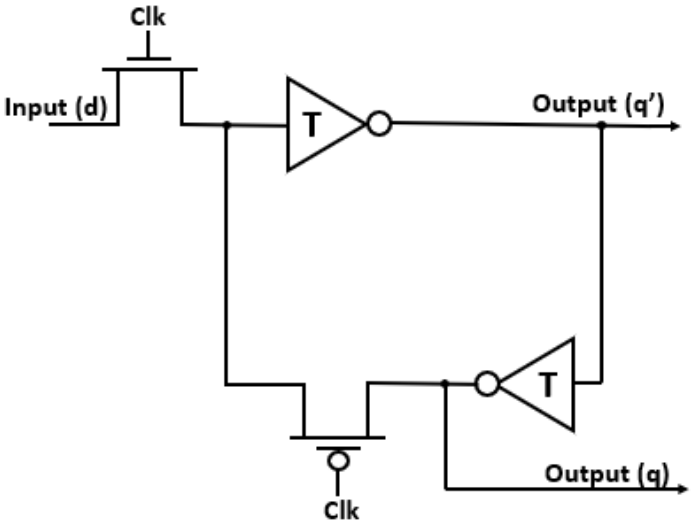

Fig. 4.5: Schematic Diagram of proposed PTDL based on Pass Transistors

From the fig we can observe that it consists of two STI gates and two Pass Transistors. One is N-GNRFET in the forward path and the other one is P-GNRFET in the feedback path. Clk signal is fed to the gate terminals of Pass Transistors. Input signal is provided on **d** node output can be seen at **q** & **q'** node. At **q'** we will see the inverse of output signal at **q** node. Functionality of the proposed PTDL circuit is explained below:

At Clk = 1: (Transparent Mode)

(N-GNRFET is ON & P-GNRFET is OFF) Signal at Input node (**d**) will be inverted by STI and at **q'** the signal is inverted. It gets inverted again and at **q** we have the input signal. Since Input data is propagated to the Output nodes (**q & q'**), the latch is said to be in Transparent mode.

At Clk = 0: (Hold Mode)

(N-GNRFET is OFF & P-GNRFET is ON) No data propagate to the Output nodes (**q & q'**) from input node (**d**). Previously stored data propagates to Output nodes via P-GNRFET. Since previous data is sustained, the latch is said to be in Hold mode. Functionality of the Ternary D Latch can be verified from the Transient response of the PTDL presented in Figure below:

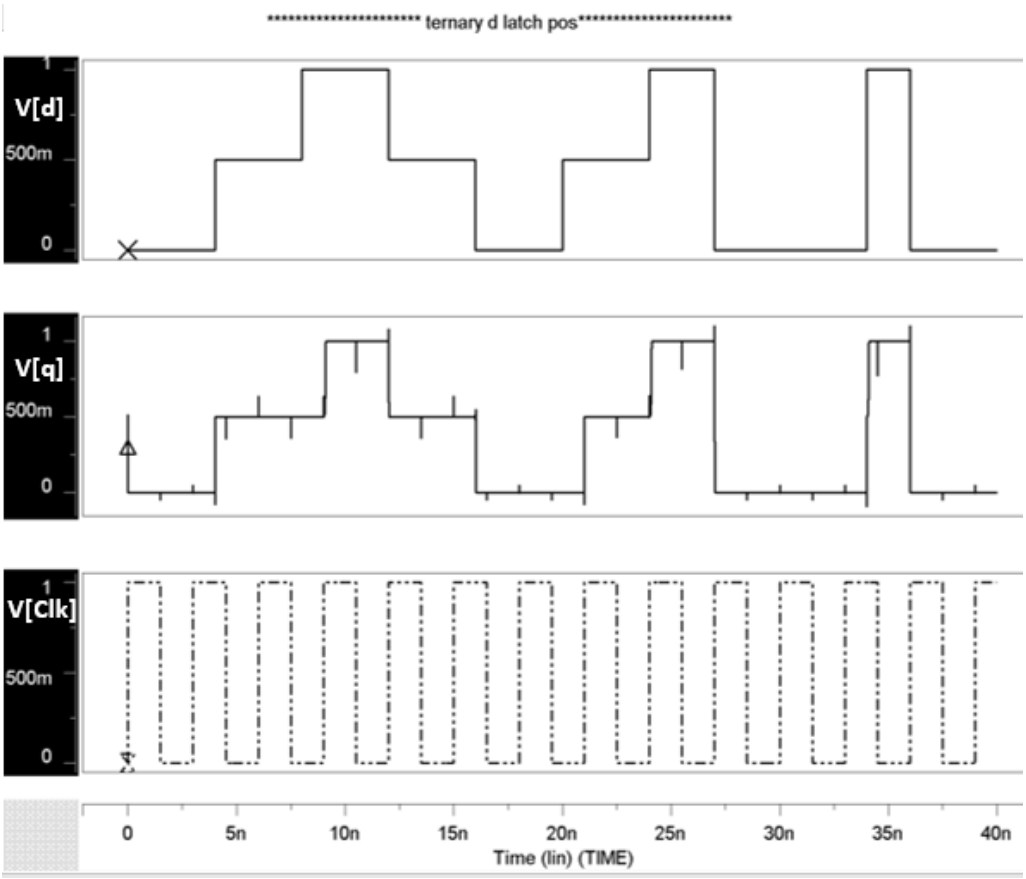

Fig. 4.6: Transient Response of proposed PTDL based on Pass Transistors

In the Fig. 4.6 first plot is the input signal (Piecewise Linear) applied at node **d**. Second plot is the output at **q** node. Third plot is the Binary clock controlling the PTDL. We can observe that the output is changing in accordance with the input when the Clk signal is High. It is in Hold mode when the Clk signal is low. We can verify our Transient analysis by comparing the Plot with the below Truth Table.

Clk	MODE	d	q	q'
HIGH (2)	TRANSPARENT	0	0	2
		1	1	1
		2	2	0
LOW (0)	HOLD	X	**q**(prev)	**q'**(prev)

TABLE 4.4: Truth Table of proposed PTDL based on Pass Transistor

Negative Ternary D Latch (NTDL)

Fig. x presents the schematic diagram of the PTDL.

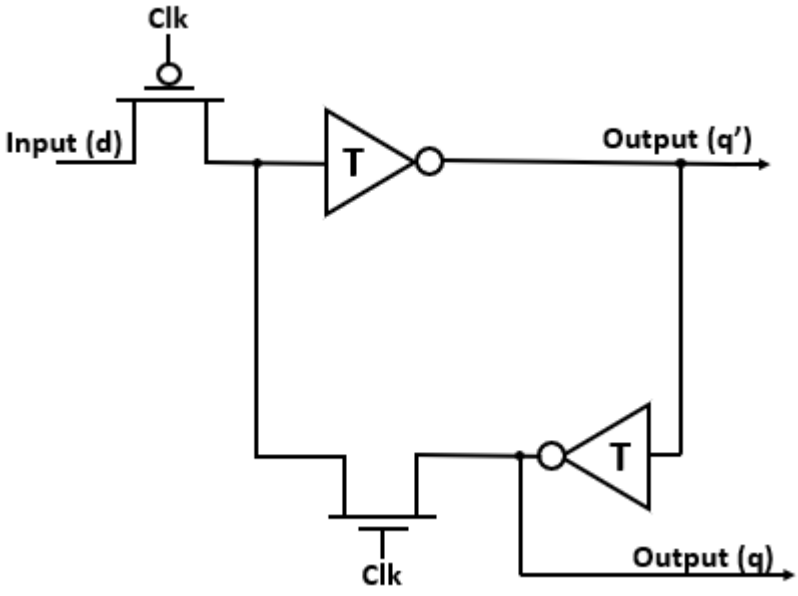

Fig. 4.7: Schematic Diagram of proposed NTDL based on Pass Transistors

From the Fig. 4.7 we can observe that it consists of two STI gates and two Pass Transistors. One is P-GNRFET in the forward path and the other one is N-GNRFET in the feedback path. Clk signal is fed to the gate terminals of Pass Transistors. Input signal is provided on **d** node output can be seen at **q** & **q'** node. At **q'** we will see the

inverse of output signal at **q** node. Functionality of the proposed PTDL circuit is explained below:

At Clk = 0: (Transparent Mode)

(P-GNRFET is ON & N-GNRFET is OFF) Signal at Input node (**d**) will be inverted by STI and at **q'** the signal is inverted. It gets inverted again and at **q** we have the input signal. Since Input data is propagated to the Output nodes (**q & q'**), the latch is said to be in Transparent mode.

At Clk = 1: (Hold Mode)

(P-GNRFET is OFF & N-GNRFET is ON) No data propagate to the Output nodes (**q & q'**) from input node (**d**). Previously stored data propagates to Output nodes via N-GNRFET. Since previous data is sustained, the latch is said to be in Hold mode.

Functionality of the Ternary D Latch can be verified from the Transient response of the NTDL presented in Figure below:

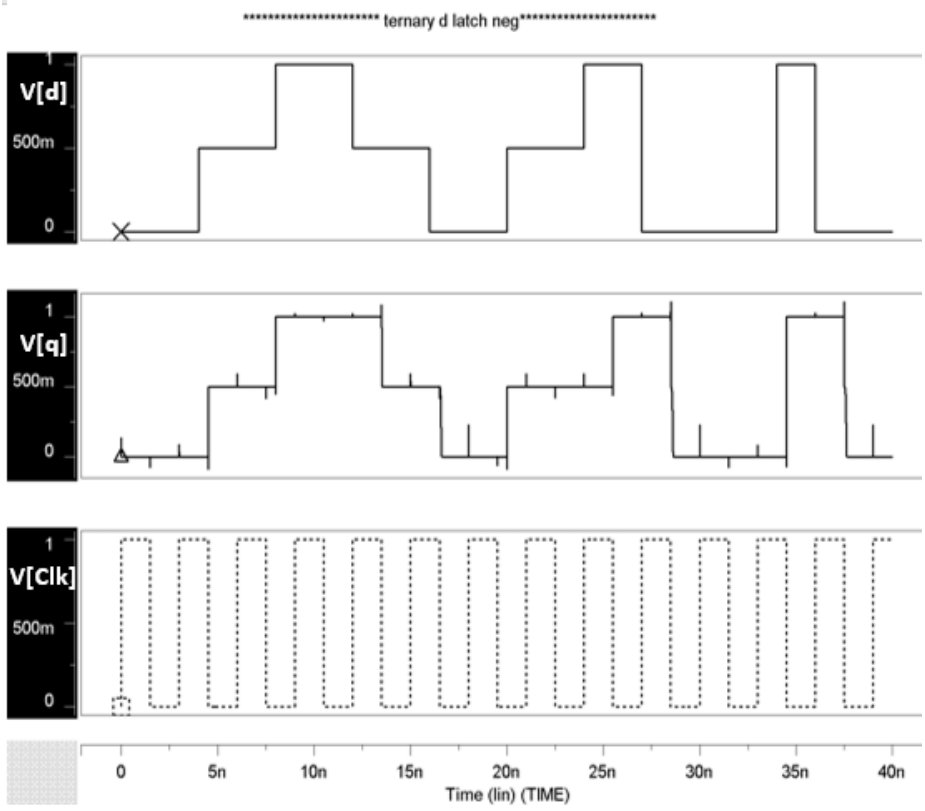

Fig. 4.8: Transient Response of proposed PTDL based on Pass Transistors

In the Fig. 4.8, first plot is the input signal (Piecewise Linear) applied at node **d**. Second plot is the output at **q** node. Third plot is the Binary clock controlling the NTDL. We can observe that the output is changing in accordance with the input when the Clk signal is Low. It is in Hold mode when the Clk signal is High. We can verify our Transient analysis by comparing the Plot with the below Truth Table.

Clk	MODE	d	q	q’
LOW (0)	TRANSPARENT	0	0	2
		1	1	1
		2	2	0
HIGH (2)	HOLD	X	**q**(prev)	**q’**(prev)

TABLE 4.5: Truth Table of proposed NTDL based on Pass Transistor

4.2.2 Ternary D Flip-Flop

Fig. 4.9 provides the schematic diagram of the proposed Positive Edge-Triggered Ternary D Flip-Flop (TDFF). From the fig we can observe that it consists of two TDLs connected in Master-Slave configuration. First TDL is a Negative Ternary D Latch (NTDL), it acts as Master Latch. Next TDL is a Positive Ternary D Latch (PTDL), acting as a slave latch. The design is made up of 4 STI gates & 4 Pass Transistors. P1 & P2 are P-GNRFETs while N1 & N2 are N-GNRFETs. Input of Slave (PTDL) is taken from inverting node of Master (NTDL). Number of GNRFETs used in this TDFF design is 28.

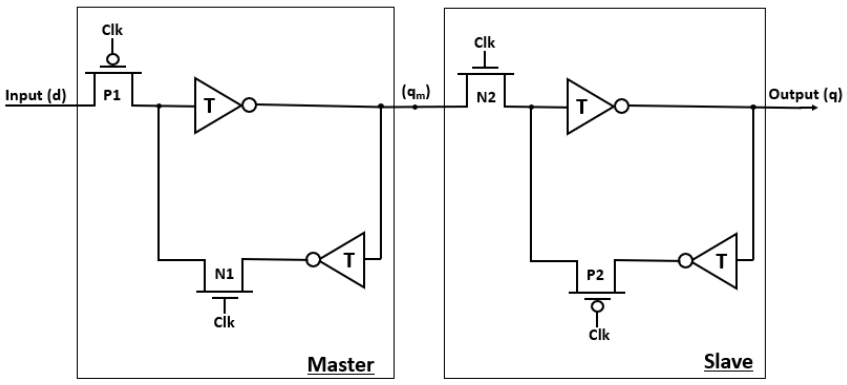

Fig. 4.9: Schematic Diagram of proposed TDFF based on Pass Transistors

Functionality of the proposed TDFF circuit is explained below:

At Clk = 0: NTDL (Transparent Mode), PTDL (Hold Mode)

(P1 & P2 are ON, N1 & N2 are OFF) Signal at Input node (**d**) will be inverted by STI and there is an inverted signal at Intermediate node (**Qm**). PTDL is in Hold mode so it will restore the previously stored value at Output node(**q**).

At Clk = 1: NTDL (Hold Mode), PTDL (Transparent Mode)

(P1 & P2 are OFF, N1 & N2 are ON). NTDL is in Hold mode so previously stored value at Intermediate node ($\mathbf{q_m}$) will be restored. PTDL is in Transparent mode so the data at $\mathbf{q_m}$ will be inverted again to pass to the Output node. Thus, data at the input will be passed at Rising edge of the clock.

4.2.3 Simulation & Results

Fig. 4.10 presents the Transient Response of Proposed Ternary D Flip-Flop (TDFF) based on Pass Transistors.

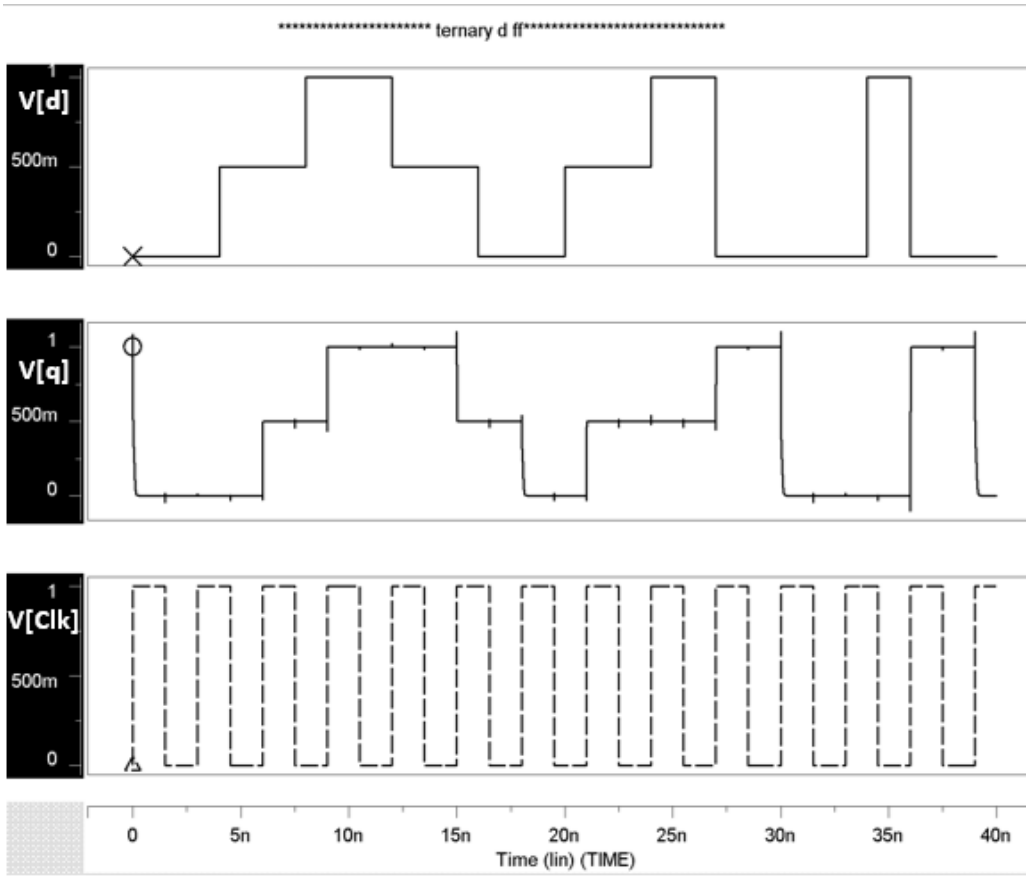

Fig. 4.10: Transient Response of proposed TDFF based on Pass Transistors

In the above figure first plot is the input signal (Piecewise Linear) applied at node d. Second plot is the output at q node. Third plot is the Binary clock (Clk)controlling the TDFF. In the figure, it can be observed that the output is changing in accordance with the input only when the Clk signal is changing from Low to High (Rising Edge). TDFF is in Hold mode otherwise. Verification of our Transient analysis can be done by comparing the Plot with the below Truth Table.

Clk	MODE	D	q	q'
0 → 2	**TRANSPARENT**	0	0	2
		1	1	2
		2	2	0
2 → 0	**HOLD**	**X**	q(prev)	q'(prev)

TABLE 4.6: Truth Table of proposed TDFF based on Pass Transistors

The need of two non-overlapping clock signal in the previous design has been resolved. Also, the GNRFET count is reduced by four.

Following are the Delay & Power calculations of proposed TDFF based on Pass Transistors:

Transition Delay (ps)	**0 → 1**	13.041
	0 → 2	8.4469
	1 → 0	45.597
	1 → 2	5.895
	2 → 0	9.1323
	2 → 1	6.0185
	Average	14.6884
Average Power (μW)	0.62252	
Power Delay Product (10^{-18} Joules)	9.14383	
Number of GNRFETs	28	

TABLE 4.7: Power & Delay analysis of proposed TDFF based on Pass Transistors

4.3 COMPARISION & ANALYSIS

There are many prevailing TDFF designs based on CMOS [3,14], CNTFET [15] and GNRFET [16]. Table 4.8 provides the details about power and delay analysis of proposed design and its comparison to former designs proposed in [3], [14], [15] and [16].

	Transition	CMOS [3]	CMOS [14]	CNTFET [15]	GNRFET [16]	TDFF (TG)	TDFF (Pass)
Delay (ps)	$0 \rightarrow 1$	69.196	90.504	99.416	24.8	102.6	13.041
	$0 \rightarrow 2$	116.66	326.88	284.92	61	9.5	8.4469
	$1 \rightarrow 0$	61.687	463.01	116.62	111	5.8	45.597
	$1 \rightarrow 2$	83.393	305.79	232.14	79.9	6.3	5.895
	$2 \rightarrow 0$	95.044	489.30	24.641	93	7.5	9.1323
	$2 \rightarrow 1$	38.405	220.88	60.475	51	61.4	6.0185
	Average	77.398	316.06	136.36	70.1	32.18	14.6884
Average Power (μW)		1.1835	2.5143	1.4918	0.523	0.479	0.62252
Power Delay Product (10^{-18} Joules)		91.6	794.66	204.28	36.66	15.41	9.14383
Transistor Count		72	92	32	92	32	28

TABLE 4.8: A Comparative analysis in terms of Delay & Power for TDFF.

For the better understanding of the above table each parameter of is discussed in the following segments:

Delay: This parameter measures the change in the Output with respect to the change in Input Signal for each transition. In a Ternary circuit there can be 6 types of transitions. Average of these delays can be taken as a parameter to compare the

devices. It gives us the idea about the speed of the circuit. Fig. 4.11 presents the comparison of Average Delay of the proposed designs with prevailing designs.

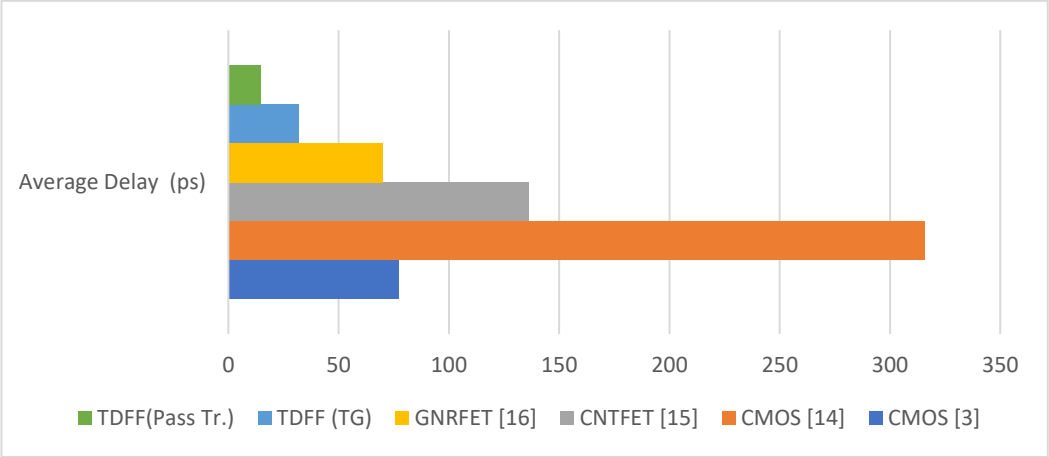

Fig. 4.11: Average Delay of proposed and prevailing Designs

From the figure, it can be observed that both the proposed designs have less delay than all the prevailing designs. Out of both TDFF based on Pass Transistor has the lowest delay.

Average Power: Average of the Power delivered by the Supply voltage over the time of 40 nano seconds is taken as the Average Power consumed by the circuit.

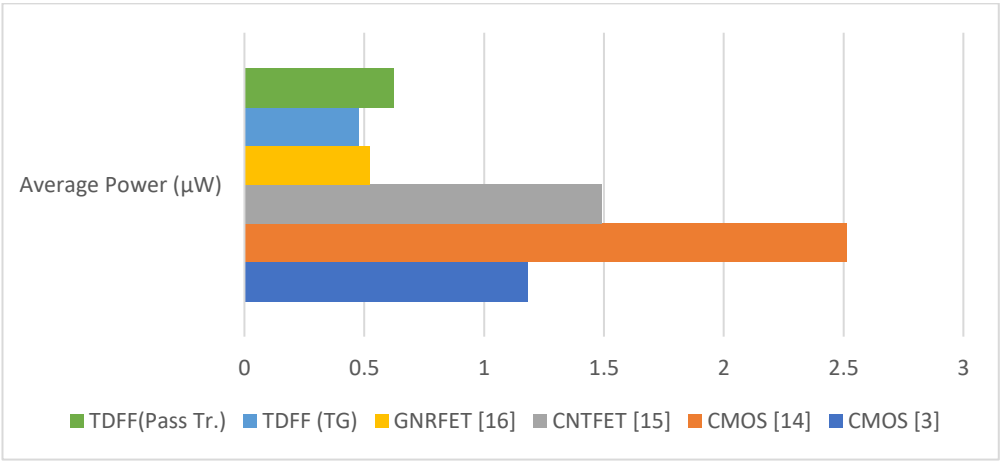

Fig. 4.12: Average Power of proposed and prevailing Designs

From the Fig. 4.12 it can be observed that the proposed TDFF with TG have least Average Power consumption than all the prevailing designs. TDFF based on Pass Transistor has slightly more power consumption than prevailing GNRFET design.

Power Delay Product (PDP): PDP is taken as the product of Average Delay and the Average Power. For a Digital signal it can be taken as the key parameter to measure the characteristics of the circuit.

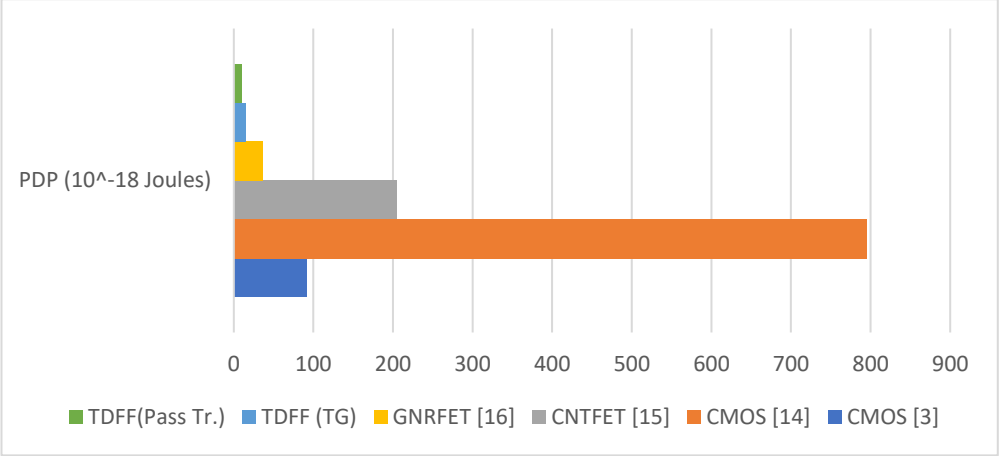

Fig. 4.13: PDP of proposed and prevailing Designs

From the Fig. 4.13, it can be observed that both the proposed designs have less PDP than all the prevailing designs. Out of both TDFF based on Pass Transistor has the lowest PDP.

Transistor Count: Number of Transistors in the circuit is provided by this parameter. This parameter gives us a rough idea of the Chip Area. Since number of Transistors is directly proportional to the Chip Area.

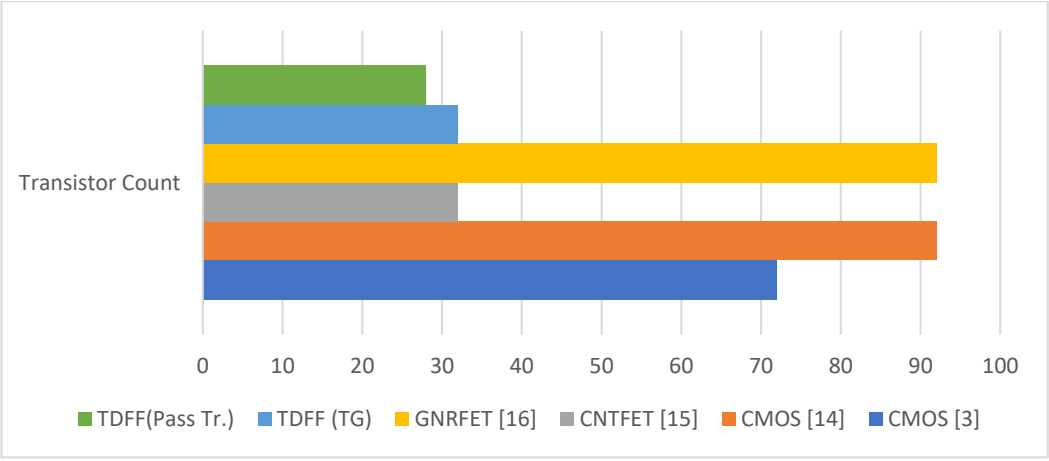

Fig. 4.14: Transistor Count of proposed and prevailing Designs

From the Fig. 4.14, it can be observed that both the proposed designs have least Transistor Count than all the prevailing designs. Out of both, TDFF based on Pass Transistor has the lowest Transistor Count (28). TDFF based on TG has a Transistor Count of 32.

CHAPTER 5
CONCLUSION & FUTURE SCOPE

5.1 CONCLUSION

In this project, the unique physical and electronic characteristics of GNRFET are utilized to propose two Ternary D Flip-Flop (TDFF) designs. In First design, a Ternary D latch is proposed using Standard Ternary Inverter, Transmission gates and non-overlapping clocks. Furthermore, two of these Ternary D Latches are cascaded as a Master-Slave configuration. In Second design, the need of two different non-overlapping clocks has been resolved by using Pass Transistors instead of Transmission Gates. A quantitative and comparative analysis based on the average Power Dissipation & Delay with prevailing design is done. All the computational values of prevailing designs are taken from [16].

In first design, delay has reduced about 58.42 %, 89.81 %, 76.4 % and 54.1 % from [3], [14], [15] and [16] respectively. In terms of Average Power, power has reduced about 59.52 %, 80.94 %, 67.89 % and 8.4 % in comparison with [3], [14], [15] and [16] respectively. Power Delay Product is reduced about 83.17 %, 98.06 %, 92.45 % and 57.96 % from [3], [14], [15] and [16] respectively. Transistor Count in circuit is also significantly less then [3], [14] and [16].

In Second design, delay has reduced about 81.02%, 95.35 %, 89.22% and 79.04 % from [3], [14], [15] and [16] respectively. In terms of Average Power, power has reduced about 47.4% , 75.24% and 58.27% in comparison with [3], [14] and [15] respectively. It's increased 19.02% when compared to GNRFET [16] design. Power Delay Product is reduced about 90.01%, 98.84 %, 95.52% and 75.05% from [3], [14],

[15] and [16] respectively. Transistor Count is reduced to 28 from 72, 92, 32 & 92 when compared to [3], [14], [15] and [16].

When compared with each other the TDFF based on Pass Transistor has 54.35 % less delay than the former. Power consumption is increased 29.96 % than the former. PDP is also reduced 40.66 % from the former. There is a reduction of 4 transistor in the design when compare to the formerly proposed design.

These new Ternary GNRFET designs have shown better results in every parameter. The number of Transistors is also reduced, so there is a huge reduction in area. The main shortcoming of TG based TDFF, the need of two non-overlapping clocks is resolved in the TDFF based on Pass Transistor. So, it is established that TDFF based on Pass transistors is superior to TDFF based on Transmission Gates.

5.2 FUTURE SCOPE

Innovation scaling has given us expanded circuit execution in the course of recent decades. The business has scaled the customary transistors for as far back as six years utilizing a few creative strategies, for example, high-k dielectrics and stressed silicon. In any case, scaling of ordinary transistors past the 22nm hub is extremely troublesome because of short-channel effects. GNRFET have risen as the most practical arrangement because of their simplicity of creation. The manufacture procedure of GNRFETs is very like the creation procedure of traditional transistors.

As the extension of proposed work, different other Ternary circuits can be designed. An ecosystem of Ternary design can be developed in order to keep up with the Moore’s Law trajectory. Other than that, higher order Multiple-Valued logic circuits can be also designed.

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