ANALYSIS, DESIGN AND IMPLEMENTATION OF DIGITAL CONTROL LOOP BASED ON TMS320F2812 DSP FOR BUCK AND SINGLE INPUT MULTI OUTPUT BOOST CONVERTER IN VOLTAGE CONTROL MODE

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CANDIDATE'S DECLARATION

I, VANSHIKA JINDAL, Roll No's – 2K20/PES/23 student of M.Tech (Power Electronics), hereby declare that the project Dissertation titled "Analysis, Design and Implementation of Digital control loop based on TMS320F2812 DSP for Buck and Single Input Multi Output Boost Converter in Voltage control mode" which is submitted by me to the Department of Electrical Enginering , Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "Analysis, Design and Implementation of Digital control loop based on TMS320F2812 DSP for Buck and Single Input Multi Output Boost Converter in Voltage control mode" which is submitted by Vanshika Jindal, Roll No's – 2K20/PES/23, Power Electronics, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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Abstract

DC-DC power converters play an important role in powering telecom and computing systems. With the speed improvement and cost reduction of digital control, digital controller is becoming a trend for DC-DC converters in addition to existed digital monitoring and management technology. Design and implementation of digital controllers for a buck and SIMO Boost converters using linear control methods are investigated in this thesis. The small signal analysis of an ideal and non ideal Buck and SIMO Boost is being obtained using standard state space averaging techniques. Analog PI controllers were designed for generic DC-DC converters using different PI tuning rules and compensator design using frequency response considering stability. The digital control loop is designed and implemented using Direct and Indirect design approaches using various discrete conversion methods such as Forward euler, Backward euler and Tustin approximations. The validity of the non-isolated DC-DC converter with ratings 45W, 15V, 3A for SIMO Boost converter at 50 kHz frequency and 18W,12V, 1.5A for Buck converter at 20 kHz switching frequency are verified by simulations and experimental results for closed loop operation under variation in input voltage and load. Control algorithms using PI and Fuzzy-Sugeno controller are implemented using Texas Digital Signal Processors - TMS320F2812 and MATLAB/Simulink (version 2021b) platform has been utilized for simulation purpose. Limitations of practical implementation of digital control on DC-DC converters which includes the digital PWM resolution (limit cycles), the ADC sampling delay and limited control bandwidth of digital compensator is also discussed in this thesis.

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Chapter 1

INTRODUCTION

Switched mode DC DC converters converts DC input voltage to regulated DC output voltage efficiently. SMPS As Compared to linear power supplies provide more efficiency and power density. Energy storage elements called as capacitor and inductors are generally used for energy transfer and work as a low pass filter (LPF). Also, It is been observed that the buck converter and boost converter are the most fundamental topologies. Previously, the control methods used for DC-DC converters has been analog control techniques. However due to recent advances in technology, digital signal processors are preferred as they are relatively more immune to environmental changes such as temperature and aging components. More advanced algorithms can be implemented on a DSP as high sampling rate because of its special architecture and high performance. Priorly in power electronics systems, output voltage regulation has been achieved using analog control. Analog signals of the output voltage or output current are controlled by the analog transfer function using OPAMP with compensation network. Through this the output signal is controlled and regulation is obtained.

The analog-opamp compensation network regulates the duty ratio with respect to switching frequency used for driving the power switching devices. analog control system possess real time operation and provides control over very high bandwidth. It carries infinite voltage resolution theoretically. However, Analog control restricts for hardware expansion and design changes and advanced control techniques are used to improve performance required more analog components[1]. Analog integrated circuits are the traditional pillers for controllers for SMPS. Whereas digital controllers are used in majority of applications ranging from high voltage and high switching frequency. The ease in generating number of control signals with less complexities forces us to use micro-controllers and digital signal processors. Commonly, Boost converters are used to 'increase' the input voltage to higher level. It carries an unique ability to transfer the energy stored by inductor to capacitor and inturn to load. During the first switching cycle , energy is transferred to inductor and and when the switch is opened the energy stored in inductor is being transferred to load via capacitor. It finds application to portable electronic devices, fuel cell and battery power systems.[2]

The digital control loop is designed and implemented using direct and indirect approaches using various discrete conversion methods. The validity of the non-isolated DC-DC SIMO Boost converters and their performances are verified by simulation and experimental results for closed loop operation under variation in load. PI and PID control algorithms are implemented using Digital Signal Processors and MATLAB/Simulink platform has been utilized for simulation purpose.

One of the major drawbacks of the Digital control is Limited bandwidth caused by time delay in ADC conversion, PWM generation, Quantization and computational time delays. Straight forward predictive schemes are used to compensate the delay and hence increasing control loop bandwidth[3].

1.1 Motivation

In Power Electronics , Digital Signal Processing is an important research area which resolves the concerns related to design and algorithms. DSPs are commonly used in different control applications because of low cost and good performance characteristics. These are prominently used in audio signal, sensing circuits for voltage , current and position, signal processing etc. Better resolution, control with inherent sampling, ease to implement sophisticated control algorithms, less effect of environment changes are the few advantages of digital control.

Therefore, Digital control loop design is the focus of this thesis. Single Input Multiple Output boost converter is being modelled, designed and controlled in this thesis.

1.2 Literature review

The applications for power electronics are entering into consumer electronics such as , switched mode power supplies, battery storage systems, electric drives and machines, charging infrastructures , electric vehicle, power factor correction etc. As digital control is gaining importance , many semiconductor companies such as Texas Instruments, Analog Devices and Motorola have launched high computational processors for control applications.

The Digital Signal Processor are a very high speed processor , prominently used to handle Power Electronics and Systems applications such as PWM generation of analog signals and quadrature encoder circuit for speed and position estimation[4]. To produces a constant voltage output aligned with the requirements of load, a converter is required. Single input single output boost converter can provide us high dc voltage but with more losses in inductor, capacitor and main switch or diode. With this efficiency of the converter gets degraded and EMI problem come into play. This thesis presents Single input multi output unidirectional boost converters for two controlled output applications. This circuit also propose component count reduction and the main advantages of the SIMO converter is to get two regulated voltage output with low cost and lesser power losses along switching devices[5].

This thesis proposes suitable topology for power converters, model of converter, analysis of the three switching states , control strategies and digital control loop design. The circuit simulation and hardware with linear and non-linear controllers are presented in this thesis. The major applications of DC-DC converters are in battery charging and discharging , battery energy storage systems and power factor correction, renewable energy systems etc. DC-DC converter provides the uninterrupted power transfer to other devices using appropriate switching techniques. Due to advancement in power devices and converters, efficiency, high voltage operation and high switching frequency devices. This results for the need of GaN ans SiC based devices with lesser switching and conduction losses[6].

Also, Cross voltage regulation is oftenly seen in multi output converters which makes the analysis and design more complex. The Analysis, design, modelling and implementation of closed loop Digital controlles for SIMO Boost converters using TMS320F2812 DSP controller is performed. Control Techniques such as PI, PD and PID and Non-linear- Fuzzy control are being discussed and implemented in this thesis using TI C2000 series DSP for SIMO boost converters[7]. Digital Control is a multi-disciplinary research which has its applications to Digital signal processing, speech analysis, audio processing and control of power converters, motor drives etc. Digital control Loop can be designed using tuning approaches, root locus method and bode plot methods using suitable gain, crossover frequency and phase margin. Digital control uses computer systems and microprocessors for processing analog signals. Digital controllers uses discrete-time models for processing and uses indirect control and direct control techniques for designing discrete controllers.

In the indirect design approach, analog controllers are initially designed using small signal models and then converted to digital controller using discretization methods such

as Tustin, Backward Euler, Forward Euler etc. Tustin seems to have better discretization then other methods. Vallittu and Suntio have studied the constraints and advantages of digital control in power circuits[8]. The analysis of Boost converters starts with small signal modelling , averaging and perturbations, linearization of the converter's average inductor and voltage equations. Linear controllers can be designed using various methods using frequency responses and step response in time domain. The output voltage to duty ratio transfer function is obtained for ideal and non- ideal converter parameters. Digital controller can also be designed using direct method. In this method, the transfer function of converter is converted to discrete using Matlab.

The inclusion of non-idealities in boost converter results into right half plane Zero. This right half plane zero results a gain of $20dB/decade$ and a phase delay of $90°$. Due to this Boost converter is termed as non-minimum phase function and it is difficult to control them relatively as compared to minimum phase function such as Buck converter. Due to addition of right half plane Zero, systems unstability increases and noise, disturbances enters the system. Therefore, Linear controllers are designed for operating point and controlling of Voltage is achieved[9] .

However, it is difficult to control Non- minimum phase function such as Boost converter, non-linear controller are used and implemented using digital controllers. Artificial intelligence and Optimization Techniques are majorly used for controlling any parameter. One of them is Fuzzy which is a nonlinear controller and can adapt to time varying operating points. Viswanathan and Srinivasan have researched on fuzzy controller and its performances. It is been observed that fuzzy controller improves the performance in terms of overshoot and rise time of output voltage.With appropriate scaling , design and analysis fuzzy controllers are implemented for SIMO converter and closed loop control is validated. Limit cycles are generated due to the quantization and are difficult to predict. All the digital controllers are implemented on TMS320F2812 DSP using various peripherals such as EVM and ADC.

1.3 Composition of the dissertation

The dissertation is organized in five parts. The first part consists of Chapter 1, which gives an outline about the literature review on the developments related to single input multi-output DC-DC converters. The motivation, aim and objectives for pursuing the research has been described here.

The second part of this dissertation, comprising of Chapter 2 and Chapter 3, outlining the topology, analysis and dynamic modelling of the converters. Chapter 2 presents an overview of DC-DC converters followed by analysis of different topologies of multiport converters. Chapter 3 gives a detailed mathematical modelling and dynamic state space analysis of SIMO converter. Small signal modelling technique is used to form a dynamic model of SIMO converter.

In Chapter 4, digital controllers (PID and fuzzy) are designed for DC-DC SIMO Boost converters using linear and non linear control methods. The controllers are designed using Frequency response techniques via bode plots. The transformation of analog controller to digital controller using descretization methods are discussed and implemented using and implementation of digital controllers are also discussed in Chapter 5.

In Chapter 6 of this dissertation, the experimental hardware circuitry and in chapter 5, DSP controller from Texas Instruments is described in detail. Converter design specifications are also introduced here. Control strategies used to generate gate pulses are hereby discussed and structure of microcontroller used to generate those control signals are hereby presented.

Laboratory results for the buck and the boost converters are presented and compared in Chapter 7. In Chapter 8, the research is summarized with conclusions, observations and suggestions for future work are made.

Chapter 2

NON-ISOLATED DC-DC CONVERTER TOPOLOGY

This chapter introduces various DC-DC converter topologies based on buck, boost and Single output converter. The converter structure, operating principle and different modes of operation are presented and analyzed in detail.

2.1 Overview

Switched mode DC-DC converters is used for stepping up and stepping down the voltage from the input supply to its load output. It is classified in switched-mode power supply (SMPS) consisting of atleast two semiconductor devices (a transistor and a diode) and atleast one energy storing element i.e. either a capacitor or an inductor or may be a combination of both. Voltage ripples can be reduced by using capacitor filter at both input and output[10].
Basic working of boost converter relies on the principle of storing of energy in inductor from the supply side (dc or rectified ac) and then transferring it to the capacitor (or load itself). Therefore, output voltage steps up, resulting it to be greater than the input supply voltage. The basic circuit topology can be enhanced to give other variants of the boost converter. Here we are discussing non-isolated DC-DC converters which can be classified into two parts:

i. Single Input Single Output (SISO)
ii. Single Input Multiple Output (SIMO)

Detailed analysis of these DC-DC converters will be done later in this chapter.

In single input single output (SISO) mode supply is from one input and here resistive load is taken as single output. This is a conventional form of DC-DC boost converter. Power transfer takes place between input supply (here a charged battery) and output load (resistive type) [2].

In single input multiple output (SIMO) mode single charged battery act as input supply and two or more resistive loads as output. This is a non-isolated SIMO converter topology and here power transfer occurs between one input supply and two resistive loads.

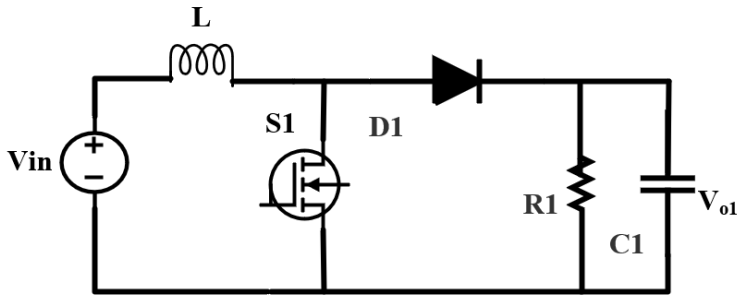


Figure 2.1: SISO Boost converter

2.2 Analysis of the Multiport Boost Converter

In a boost converter topology, conventional boost converters are merged for providing new topologies to get multiport converter. If we consider hybridizing alternate energy sources to be used as input sources for the converter which includes FC and ESS (here battery) then usage of each source accordingly can result in development of different topologies. Here we discuss detailed structure of each topology (i.e. conventional and proposed), its operating modes and useful mathematical equations. Classification of DC-DC Boost topology for non-isolated structure is as follows:

i. Single Input Single output Boost Converter (SISO)
ii. Single Input Multiple Output Boost converter (SIMO)

2.3 Single Input Single Output (SISO)

Single input single output converter topology is the conventional converter topology. The converter structure is shown in Fig. 2.1. It considers just one input supply and one resistive load at the output. In this structure inductor stores energy in one cycle from the input supply and in the next cycle it delivers the energy stored to the loads at the output. The cycle period is decided by the duty of the switch used in the converter.

2.4 Single Input Multiple Output (SIMO)

The multiport converter topology discussed above in Fig. 2.2 can be converted into SIMO converter structure. Considering just one input supply and two resistive loads as outputs we can simulate the structure of SIMO DC-DC converter.

In the fig.2.2, the SIMO converter has one-input two-output structure. In this figure, R_1 and R_2 are model equivalent resistances to denote either HEV system components or a multilevel inverter. Different types of multilevel inverters can be used in connection to this converter. HEVs have various DC-DC loads such as lightning or music system which can directly be feed from the converter output. But HEVs are difficult to operate with just one input supply as discussed earlier.

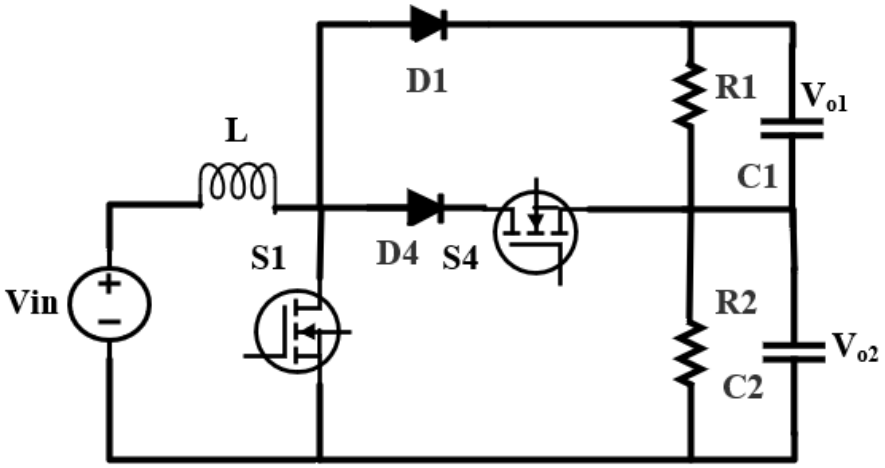


Figure 2.2: SIMO Boost converter

Table 2.1: Parameters of SIMO converter

Parameters	Values
Input voltage, Vin	$15V$
Load resistances, R_1, R_2	$18\Omega, 25\Omega$
Output voltage	$45V$
Inductance, L/r_L	$6mH/0.18\Omega$
Capacitance, C1, $C2/r_C$	$30/0.3\Omega$
Frequency, f	$50kHz$
Switch- on resistance, r_{sw}	0.044Ω
Diode forward resistance, r_d	0.024Ω
Diode forward Voltage drop, V_d	$0.7V$

2.4.1 Operating Modes

According to switching states of the switches, there are four different operating modes in one switching period as follows in figure 2.3.

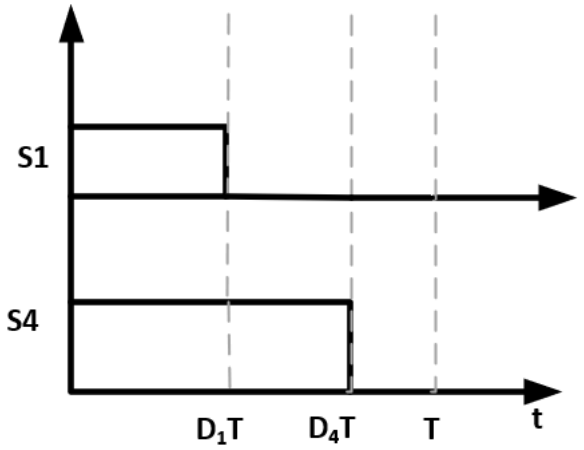


Figure 2.3: Gate pulses timing diagram

1) Switching State 1 ($0 < t < D_1T$):

In this state, switches S1 and S4 are made active by giving gate pulses. Since S1 is ON, diodes D1 and D2 are made reverse biased, so switch S4 is turned OFF. Equivalent circuit of the proposed converter in this state is shown in Fig. 2.4. In this switching state, Vin_2 charges inductor L, so inductor current increases. Simultaneously, in this state, capacitors C1 and C2 are discharged and deliver their stored energy to load resistances R1 and R2, respectively.

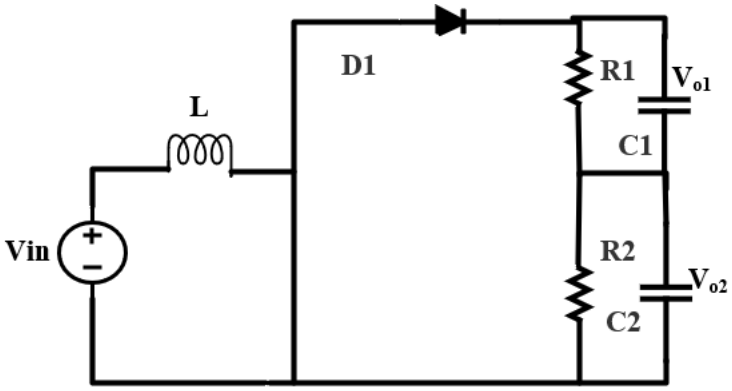


Figure 2.4: switching state 1

2) Switching State 2 ($D_1T < t < D_4T$):

In this switching state, switch S1 is turned OFF active and S4 is turned active. Since S1 is ON, diodes D1 and D2 are made reverse biased, so switch S4 is still inactive. Equivalent circuit diagram of proposed converter in this state is shown in Fig. 2.5. In this state, Vin1 charges inductor L, so inductor current furthermore increases. Simultaneously, capacitors C1 and C2 are discharged and delivers its stored energy to load resistances R1 and R2, respectively.

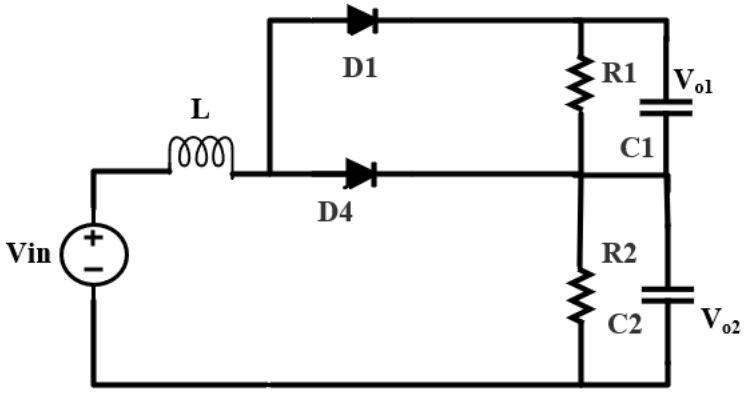


Figure 2.5: switching state 2

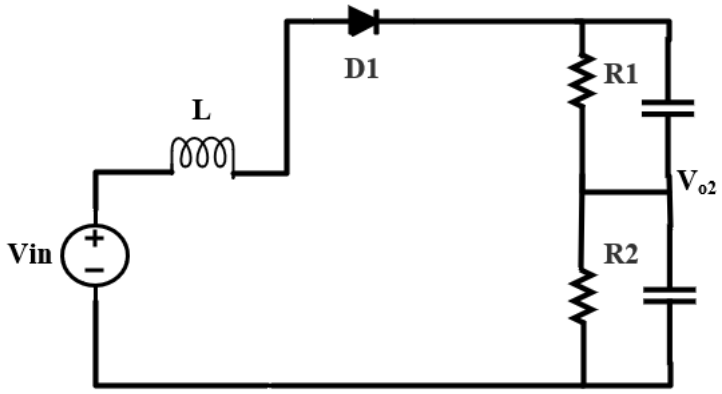


Figure 2.6: switching state 3

3) Switching State 3 $(D_4T < t < T)$**:**

In this state, switch S1 is turned inactive and switch S4 is turned OFF. Also, switch S4 is turned ON. Diode D4 is reversed biased. Equivalent circuit of proposed converter in this state is shown in Fig. 2.6. In this state, discharging on inductor L occurs and power is delivered to C1 and R1, so inductor current decreases. In this state, C1 is charged and C2 is discharged and delivers its stored energy to load resistance R2.

2.4.2 Buck converter Modelling

Based on the above procedure, mathematical modelling of buck converter can be done using state space averaging. The circuit diagram with non-idealities are shown in below figure 2.7.

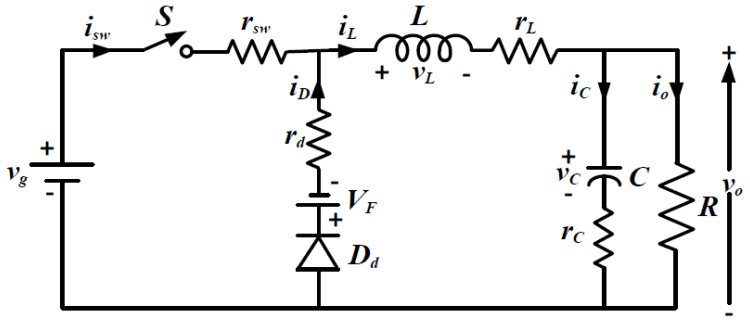


Figure 2.7: Circuit diagram of a non-ideal Buck converter

$$\frac{\tilde{v}_o(s)}{d(s)} = C_c(sI - A)^{-1}B_d \tag{2.1}$$

$$\frac{\tilde{v}_{out}(s)}{d(s)} = \frac{V_{in}}{LCs^2 + s\left[\frac{L}{R} + r_L C\right] + \left[1 + \frac{r_L}{R}\right]} \tag{2.2}$$

$$\frac{v_o(s)}{d(s)} = \frac{\frac{R(V_g+V_F-(r_{sw}-r_d)I_L}{LC(R+r_C)}(r_cCs+1)}{s^2+\left(\frac{1}{L}\left(r_x+r_L+\frac{r_cR}{R+r_C}\right)+\frac{1}{C}\left(\frac{R}{R+r_c}\right)\right)s+\left[\frac{r_L+r_x+R}{LC(R+r_c)}\right]} \tag{2.3}$$

The dynamic model for switched-on and off stage is obtained and averaged over switching cycle as per state space averaging technique. In the average model, small perturbations in the variables are introduced and then the model is linearized.

Chapter 3

DYNAMIC MODELLING OF NON-ISOLATED DC-DC CONVERTER

The objective of the control is to maintain tight regulation of output voltage in presence of input voltage or load current variations. Average small-signal modelling is based on averaging the converter's behaviour over switch on and off periods. The purpose of small-signal modelling is to convert time varying nature of the converter into time invariant system model.

In this chapter, small signal modelling is discussed and the parameters of the converter circuit are introduced. For designing the best optimal controller, small signal modelling plays a vital role.[11]

3.1 Dynamic Modelling and Analysis of SIMO converter

3.1.1 The Basic AC Modelling Approach

Mode I $(0 < t < D_1T)$

The key steps in small signal ac model of PWM converter are being derived in this section, these include:
(1) Development of equations relating the low frequency averages of the inductor and capacitor.
(2) Perturbation and linearization of the averaged equations
(3) Construction of ac equivalent model

The analysis begins by determining the voltage and current waveforms of the inductor and capacitor. When the switch is in position 1, the inductor voltage and capacitor current are:

$$L\frac{di_L(t)}{dt} = V_{in} - (r_L + r_{sw})i_L \tag{3.1}$$

$$C_1\frac{dv_{c1}(t)}{dt} = -\frac{V_{c1}}{(R_1 + r_{c1})} - \frac{I_{o1}R_1}{R_1 + r_{c1}} \tag{3.2}$$

$$C_2\frac{dv_{c2}(t)}{dt} = -\frac{V_{c2}}{(R_2 + r_{c2})} - \frac{I_{o2}R_2}{R_2 + r_{c2}} \tag{3.3}$$

Mode II $(D_1T < t < D_4T)$

$$L\frac{di_L(t)}{dt} = V_{in} - (r_L + r_{sw})i_L - V_d - i_{c2}r_{c2} - V_{c2} \tag{3.4}$$

$$C_1\frac{dv_{c1}(t)}{dt} = -\frac{V_{c1}}{(R_1 + rc1)} - \frac{I_{o1}R1}{R1 + rc1} \tag{3.5}$$

$$C_2\frac{dv_{c2}(t)}{dt} = \frac{i_L R_L}{R_L + r_{c2}} - \frac{V_{c2}}{(R_2 + r_{c2})} - \frac{I_{o2}R2}{R2 + r_{c2}} \tag{3.6}$$

Mode III $(D_4T < t < 1)$

$$L\frac{di_L(t)}{dt} = V_{in} - r_L i_L - V_d - i_{c1}r_{c1} - V_{c1} - i_{c2}r_2 - V_{c2} \tag{3.7}$$

$$C_1\frac{dv_{c1}(t)}{dt} = \frac{i_L R_1}{R_1 + r_{c1}} - \frac{V_{c1}}{(R_1 + r_{c1})} - \frac{I_{o1}R_1}{R_1 + r_{c1}} \tag{3.8}$$

$$C_2\frac{dv_{c2}(t)}{dt} = \frac{i_L R_2}{R_2 + r_{c2}} - \frac{V_{c2}}{(R_2 + r_{c2})} - \frac{I_{o2}R_2}{R_2 + r_{c2}} \tag{3.9}$$

3.1.2 Averaging the Inductor and Capacitor waveforms

Averaging perfomrs a low pass function to remove the switching ripple and harmonics. Then, applying small ripple approximation to the quantities having small ripple and are non pulsating like in inductor current and in capacitor voltages.

The equations below describes the low frequency component of the inductor current and capacitor voltage vary with time.

$$\begin{aligned}\langle v_L(t)\rangle_{T_s} = L\frac{d\langle i_L(t)\rangle_{T_s}}{dt} = V_{in} - (r_L + r_{sw}D_4)i_L - V_d(1 - D1) - i_{c1}r_{c1}(1 - D_4) \\ - i_{c2}r_{c2}(1 - D_1) - V_{c2}(1 - D1) - V_{c1}(1 - D4)\end{aligned}$$

$$\langle i_{c_1}(t)\rangle_{T_s} = C_1\frac{d\langle v_{c_1}(t)\rangle_{T_s}}{dt} = -\frac{V_{c1}}{R1 + r_{c1}} - I_{o1}\frac{R_1}{R_1 + r_{c1}} + i_L(1 - D4)\frac{R_1}{R1 + rc1} \tag{3.10}$$

$$\langle i_{c_2}(t)\rangle_{T_s} = C_2\frac{d\langle v_{c_2}(t)\rangle_{T_s}}{dt} = -\frac{V_{c2}}{R2 + r_{c2}} - I_{o2}\frac{R_2}{R_2 + r_{c2}} + i_L(1 - D1)\frac{R_2}{R2 + rc2} \tag{3.11}$$

$$\tag{3.12}$$

3.1.3 Perturbation and linearization

Equations above are nonlinear and time varying in nature i.e generated harmonics. Linearizing it by constructing a small signal model.
In small signal modelling method [30], the state variables, duty ratios, and input voltages contain two components, dc values (X, D, V) and perturbations $(\hat{x}, \hat{d}, \hat{v})$. So, the following equations for proposed converter are:

$$\langle i_L(t)\rangle_{T_s} = I_L + \hat{i}_L(t) \tag{3.13}$$
$$\langle v_{c1}(t)\rangle_{T_s} = V_{c1} + \hat{v}_{c1}(t) \tag{3.14}$$
$$\langle v_{c2}(t)\rangle_{T_s} = V_{c2} + \hat{v}_{c2}(t) \tag{3.15}$$
$$\langle i_{o1}(t)\rangle_{T_s} = I_{o1} + \hat{i}_{o1}(t) \tag{3.16}$$
$$\langle i_{o2}(t)\rangle_{T_s} = I_{o2} + \hat{i}_{o2}(t) \tag{3.17}$$
$$\langle d_1(t)\rangle = D_1 + \hat{d}_1(t) \tag{3.18}$$
$$\langle d_4(t)\rangle = D_4 + \hat{d}_4(t) \tag{3.19}$$

It is assumed that the perturbations are quite small and do not vary significantly during one switching period.

3.1.4 Construction of Small-Signal Equivalent Circuit Model

Applying the averaging to four state equations multiplied with corresponding duty cycle value, and subsequently neglecting second-order terms, we find small-signal model equations that are presented as follows:

$$\begin{aligned} L\frac{d\hat{i}_L(t)}{dt} = {} & \hat{i}_L(t)(-r_L - r_{sw}D_4) + (D4-1)\hat{v}_{c1}(t) + (D1-1)\hat{v}_{c2}(t) \\ & +(-r_{sw}I_L + i_{c1}r_{c1} - V_{c1})\hat{d}_4(t) + (V_d + i_{c2}r_{c2} - V_{c2})\hat{d}_1(t) \end{aligned} \tag{3.20}$$

$$C_1\frac{d\hat{v}_{c1}}{dt} = -\hat{v}_{c1}(t)\frac{1}{R_1 + r_{c1}} - \hat{i}_{o1}(t)\frac{R_1}{R_1 + r_{c1}} - \hat{d}_4(t)\frac{I_L R_1}{R_1 + r_{c1}} + \hat{i}_L(t)\frac{(1-D4)R_1}{R_1 + r_{c1}} \tag{3.21}$$

$$C_2\frac{d\hat{v}_{c2}}{dt} = -\hat{v}_{c2}(t)\frac{1}{R_2 + r_{c2}} - \hat{i}_{o2}(t)\frac{R_2}{R_2 + r_{c2}} - \hat{d}_1(t)\frac{I_L R_2}{R_2 + r_{c2}} + \hat{i}_L(t)\frac{(1-D2)R_2}{R_2 + r_{c2}} \tag{3.22}$$

3.1.5 The State Equation of a Network

The state space averaging approach is a canonical form of writing the different equation that describes a system. Thus, the system can be represented in a matrix form using a state-space model such taking $i_L(t)$, $v_{O1}(t)$, and $v_{O2}(t)$ as state variables. The state-space model is as follows [12]:

$$\frac{dX}{dt} = AX + BU \tag{3.23}$$
$$Y = CX + DU \tag{3.24}$$

where X represent state variable matrix, U represent control input matrix having $d_1(t)$, $d_3(t)$ and $d_4(t)$, and Y represents system output matrix having $v_{O1(t)}$, $v_T(t)$. Thus, matrices X, Y and U are as follows:

$$X = \begin{bmatrix} \hat{i}_L(t) \\ \hat{v}_{o1}(t) \\ \hat{v}_{o2}(t) \end{bmatrix}, Y = \begin{bmatrix} \hat{v}_{o1}(t) \\ \hat{v}_t(t) \end{bmatrix}, U = \begin{bmatrix} \hat{d}_4(t) \\ \hat{d}_1(t) \\ \hat{v}_{in}(t) \\ \hat{i}_{o1}(t) \\ \hat{i}_{o2}(t) \end{bmatrix} \tag{3.25}$$

Substituting the A, B, C, and D matrices using equations (3.20-3.22) and state equations (3.23-3.24), and following results is obtained:

$$A = \begin{bmatrix} -\frac{(r_L + r_{sw} D_4)}{L} & \frac{D_4 - 1}{L} & \frac{D_1 - 1}{L} \\ \frac{R_1(1-D_4)}{(R1+r_{c1})C1} & \frac{-1}{(R1+r_{c1})C1} & 0 \\ \frac{R_2(1-D_1)}{(R2+r_{c2})C2} & 0 & \frac{-1}{(R2+r_{c2})C2} \end{bmatrix} \tag{3.26}$$

$$B = \begin{bmatrix} -\frac{V_{c1} + i_{c1} r_{c_1} - I_L r_{sw}}{L} & \frac{i_{c2} r_{c2} + V_d + V_{c_2}}{L} & \frac{1}{L} & 0 & 0 \\ \frac{-R_1 I_L}{(R_1+r_{c_1})C_1} & 0 & 0 & \frac{-R_1}{(R_1+r_{c1})C1} & 0 \\ 0 & -\frac{R_2 I_L}{(R_2+r_{c2})C_2} & 0 & 0 & \frac{-R_2}{(R_2+r_{c2})C_2} \end{bmatrix} \tag{3.27}$$

$$C = \begin{bmatrix} -\frac{R_1 r_{c1}(1-D_4)}{R1+r_{c1}} & \frac{R_1}{R_1+r_{c1}} & 0 \\ \frac{R_1 r_{c1}(1-D_4)}{(R1+r_{c1})C1} + \frac{R_2 r_{c2}(1-D_1)}{(R2+r_{c2})C2} & \frac{R_1}{R_1+r_{c1}} & \frac{R_2}{(R_2+r_{c2})C2} \end{bmatrix} \tag{3.28}$$

$$D = \begin{bmatrix} -\frac{R_1 r_{c1} I_L}{R1+r_{c1}} & 0 & 0 & 0 & \frac{R_1 r_{c1}}{R_1+r_{c1}} \\ -\frac{R_1 r_{c1} I_L}{(R1+r_{c1})} & -\frac{R_2 r_{c2} I_L}{(R2+r_{c2})} & 0 & -\frac{R_1 r_{c1}}{(R_1+r_{c1})} & -\frac{R_2 r_{c2}}{(R_2+r_{c2})} \end{bmatrix} \tag{3.29}$$

So, now the unknown parameters of above mentioned matrices are D_1 and D_4. The values of duty applied to the switches is obtained by steady-state analysis which is shown in following equation:

$$\begin{bmatrix} -r_{sw} i_L + i_{c_1} r_{c_1} + V_{c_1} & V_d + i_{c_2} r_{c_2} + V_{c_2} \\ -i_L \frac{R_1}{R1+r_{c1}} & 0 \\ 0 & -i_L \frac{R_2}{R_2+r_{c2}} \end{bmatrix} \begin{bmatrix} D4 \\ D1 \end{bmatrix} = \begin{bmatrix} V_{in} - i_L r_L - V_d - i_{c_1} r_{c_1} \\ (V_{c_1} + I_{o_1} - i_L) \frac{R_1}{R_1+r_{c1}} \\ (V_{c_2} + I_{o_2} - i_L) \frac{R_2}{R_2+r_{c2}} \end{bmatrix} \tag{3.30}$$

The transfer function matrix of the converter is mentioned below which is obtained using state space averaging approach.
The small signal control to output transfer function by substituting the parameters as in table 3.1 is defined as :

$$G_{vd}(s) = \frac{\hat{v(s)}}{\hat{d(s)}} \tag{3.31}$$

This transfer function is found by setting the $\hat{v}_g(s)$ variations to zero, and solving for the dependence of $\hat{v}(s)$ on $\hat{d}(s)$.

$$G_{vdideal} = \frac{-78950s^2 - 4.866 \times 10^7 s + 6.831 \times 10^{10}}{s^3 + 2515s^2 + 2.484 \times 10^6 s + 1.128 \times 10^9} \tag{3.32}$$

$$G_{vdnonideal} = \frac{-0.3286s^3 - 78760s^2 - 3.663 \times 10^7 s + 8.332 \times 10^{10}}{s^3 + 2372s^2 + 2.135 \times 10^6 s + 9.134 \times 10^8} \tag{3.33}$$

The transfer function of buck converter is given below:

$$G_{vd}(s) = \frac{V_{out(s)}}{d(s)} = \frac{2417s + 1.714 \times 10^8}{s^2 + 9518s + 1.141 \times 10^7} \tag{3.34}$$

Chapter 4

VOLTAGE-MODE CONTROL OF SIMO BOOST DC-DC CONVERTER

The objective of the control loop is to obtain and maintain constant output voltage in spite of variations and disturbances in $V_g(t)$ and $i_{load}(t)$. Therefore, negative feedback is introduced to build a circuit that adjusts the duty cycle to obtain output voltage desired regardless of the disturbances.

Design goals and specifications are considered for compensator design in-order to obtain better transient response and stability. This chapter presents the standard frequency-domain based compensator design to attain adequate stability i.e phase margin and improvement in bandwidth. The small signal model of the system is presented in previous section[13].

In this chapter, Combined PID compensator, called as lead lag compensator is designed to obtain both wide bandwidth control and zero steady state error. The crossover frequency (f_c) is restricted to be less that 10% of the converter's switching frequency f_s.

The target crossover frequency is set as $f_c = 5kHz$ and a phase margin is set at $\phi_m = 55°$. At $f = f_C$, uncompensated loop gain exhibits a phase of about 92°, implying that a lead-lag (PID) type compensator is required in the neighborhood of f_c to boost the phase margin by $\theta = 85°$. Such compensation is obtained by forming a pole zero pair-

$$G_{PID}(s) = G_{PI\infty}\left(1 + \frac{\omega_{PI}}{s}\right) G_{PD0}\left(\frac{1 + \frac{s}{\omega_z}}{1 + \frac{s}{\omega_p}}\right) \tag{4.1}$$

the maximum phase boost generated by the PD pole-zero pair occurs at,

$$(\omega)_{max} = \sqrt{\omega_z \omega_p} \tag{4.2}$$

Substituting θ and target crossover frequency, the values for zero and pole, ω_z and ω_p shall be calculated.

$$(\omega)_z = \omega_c \sqrt{\frac{1 - \sin\theta}{1 + \sin\theta}} = 2\pi.(0.437)(kHz) \tag{4.3}$$

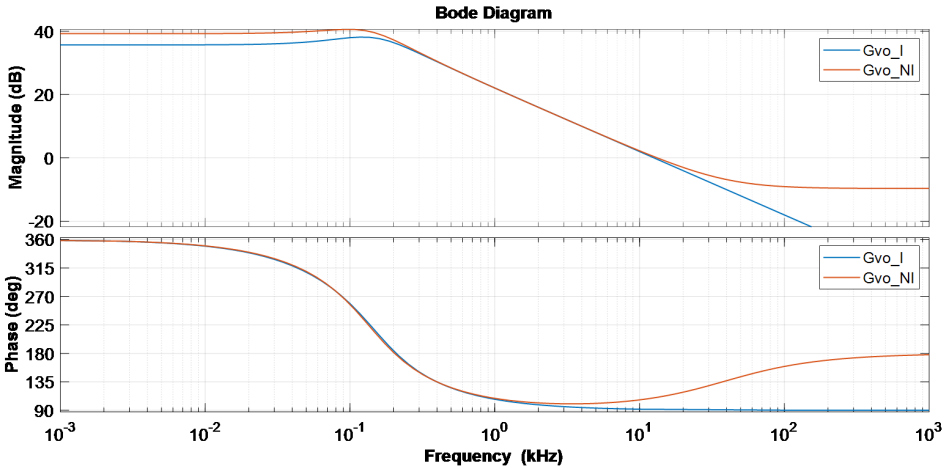


Figure 4.1: Bode plot of an uncompensated loop gain for ideal and non ideal SIMO converter

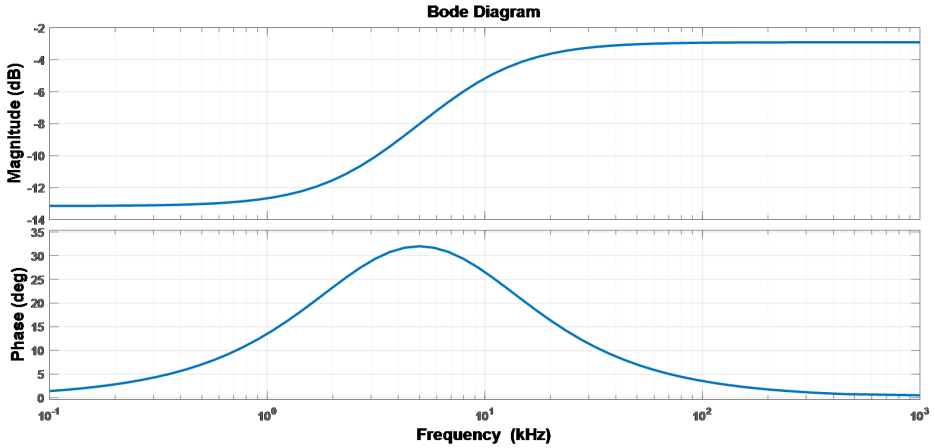


Figure 4.2: Bode plot of PID compensator for SIMO converter

$$(\omega)_p = \omega_c \sqrt{\frac{1+\sin\theta}{1-\sin\theta}} = 2\pi.(57.15)(kHz) \tag{4.4}$$

The DC gain G_{PD0} of the lead action is determined by imposing unity loop gain at the desired crossover frequency f_c,

$$G_{PD0} = \frac{1}{\mid T(j\omega_c) \mid} \sqrt{\frac{1+\left(\frac{\omega_c}{\omega_p}\right)^2}{1+\left(\frac{\omega_c}{\omega_z}\right)^2}} = 0.0349 \tag{4.5}$$

Bode plots of the lead compensation is:

Next, an integral action is introduced , the purpose of which is to null the steady state regulation error. ω_{PI} is chosen $1/10th$ of ω_c, that is $2\pi.(0.5)(kHz)$ and $G_{PI\infty} = 1$.

4.1 Digital Controller Design and Simulation

This Chapter highlights the direct digital compensator design approach. Digital controllers are more convenient to implement on microprocessors than are continuous time controllers. Continuous time controllers must be implemented either using analog circuitry (op amps) or using numerical integration routines. Discrete-time controllers, on the other hand, are easily implemented using difference equations, i.e. simple computer software[1].

Two methods are available for design of digital controller, these are discussed below:

4.1.1 Indirect design by Emulation

Designing the Analog controller in the continuous domain by ignoring the effects of Sampling effect and delays in digital control loop and then converting into discrete compensator using discretization methods.
The PID compensator designed in previous section is given as:

$$G_c(s) = \frac{4.5538(s+2749)(s+3142)}{s(s+3.591\times10^5)} \tag{4.6}$$

The bode plot for the compensator is shown in figure. This analog controller is the discretized by Bilinear (Tustin) , Forward Euler and backward Euler using MATLAB.
This generates the digital controller:

$$G_c(z) = \frac{2.6817(z-0.9891)(z-0.9875)}{(z-0.164)(z-1)} \tag{4.7}$$

$$G_c(z) = \frac{8.519\times10^{50}z^2 - 1.684\times10^{51} + 8.319\times10^{50}z}{1.871\times10^{50}z^2 - 1.054\times10^{50}z - 8.163\times10^{49}} \tag{4.8}$$

$$G_c(z) = \frac{8.721\times10^{50}z^2 - 1.724\times10^{51} + 8.519\times10^{50}z}{4.558\times10^{50}z^2 - 6.428\times10^{50}z + 1.87\times10^{50}} \tag{4.9}$$

The bilinear map, $z = e^{sT} = \left(\frac{1+\frac{sT}{2}}{1-\frac{sT}{2}}\right)$.
inversely, $s = \frac{1}{T}lnZ = \frac{2}{T_s}\frac{1-z^{-1}}{1+z^{-1}}$
Finally, the z domain PID gains are obtained from. Digital compensators z domain in additive form of PID transfer function is:

$$G_{PID}(Z) = K_p + \frac{K_i}{(1-z^{-1})} + k_d(1-z^{-1}) \tag{4.10}$$

Converting multiplicative form to parallel form for PID controller using PID gains K_p, K_i, and K_d.

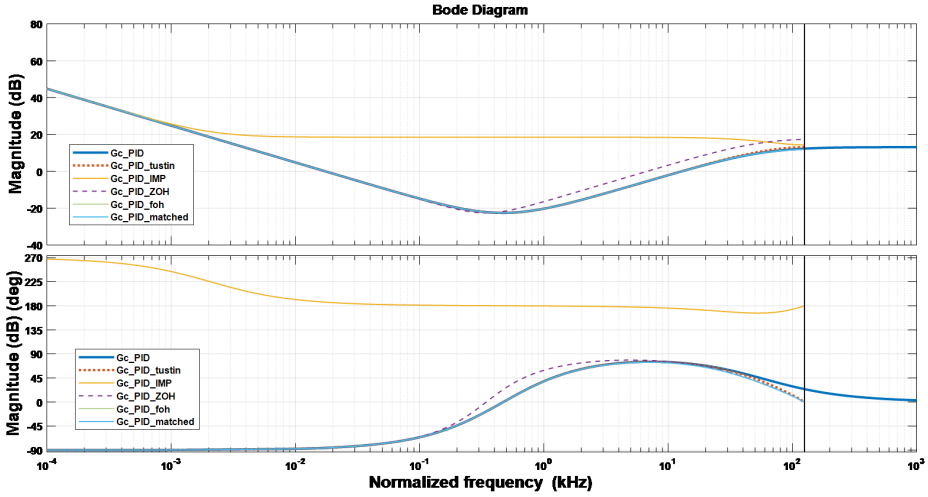


Figure 4.3: Controller discretization using various methods

$$K_p = G_{PI\infty}G_{PD0}(1 + \frac{\omega_{PI}}{\omega_{PD}} - \frac{2\omega_{PI}}{\omega_p}) \tag{4.11}$$

$$K_i = 2G_{PI\infty}G_{PD0}\frac{\omega_{PI}}{\omega_p} \tag{4.12}$$

$$K_d = \frac{G_{PI\infty}G_{PD0}}{2}(1 - \frac{\omega_{PI}}{\omega_p})(\frac{\omega_p}{\omega_{PD}} - 1) \tag{4.13}$$

The gain came out as $0.0741, 6.09 \times 10^{-4}$ and 2.23 using the above equation.

$$G_{PID}(Z) = 0.0741 + \frac{6.09 \times 10^{-4}}{(1 - z^{-1})} + 2.23(1 - z^{-1}) \tag{4.14}$$

4.1.2 Direct Digital Design

The continuous plant model is discretized with sampler and computational delays in control loop into account. Then, the discrete time controller is directly designed using frequency response like in continuous domain[14].

Converter plant model is Laplace form accounting time delay of 10μ sec of digital control loop is given as:

$$Gvd(z) = z^{-2}\frac{-0.01973z^3 + 0.01972z^2 + 0.01973z - 0.01972}{z^3 - 2.999z^2 + 2.997z - 0.9987} \tag{4.15}$$

Designing the PID controller for the above discrete converter model, we get:

$$G_c(z) = \frac{4.185z^2 - 8.357z + 4.173}{z^2 - 1.835z + 0.8352} \tag{4.16}$$

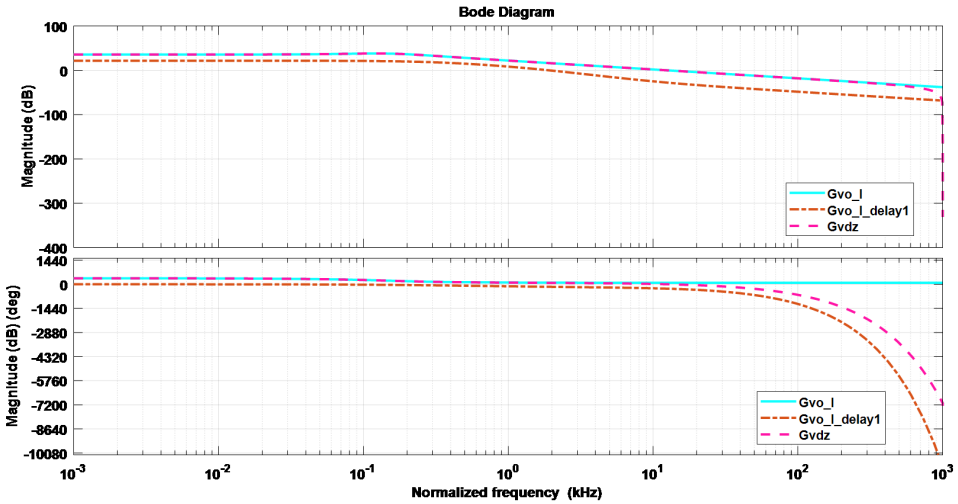


Figure 4.4: Bode plot of continuous transfer function with 20μ sec and without delay, discrete transfer function

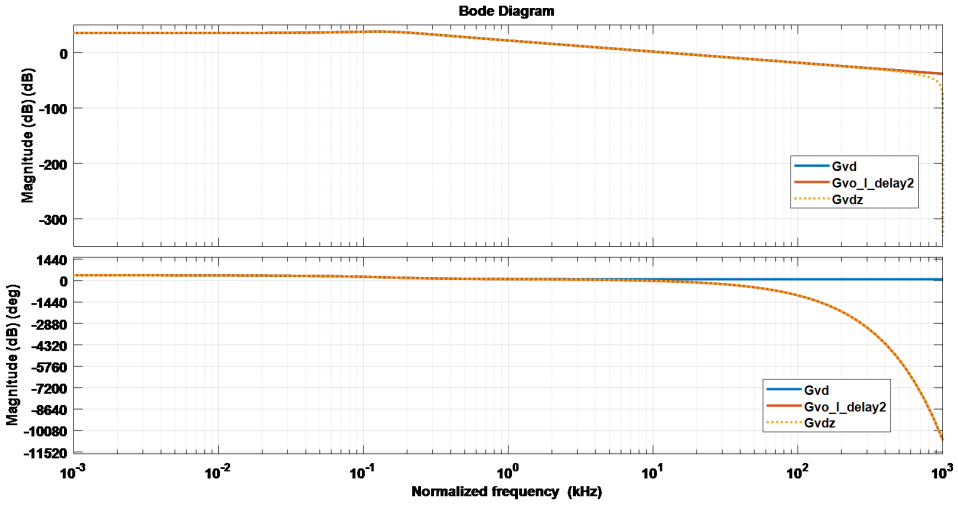


Figure 4.5: Bode plot of continuous transfer function with 30μ sec and without delay, discrete transfer function

Mapping of it into s domain can be performed. Converting multiplicative form to parallel form for PID controller using PID gains K_p, K_i, and K_d.

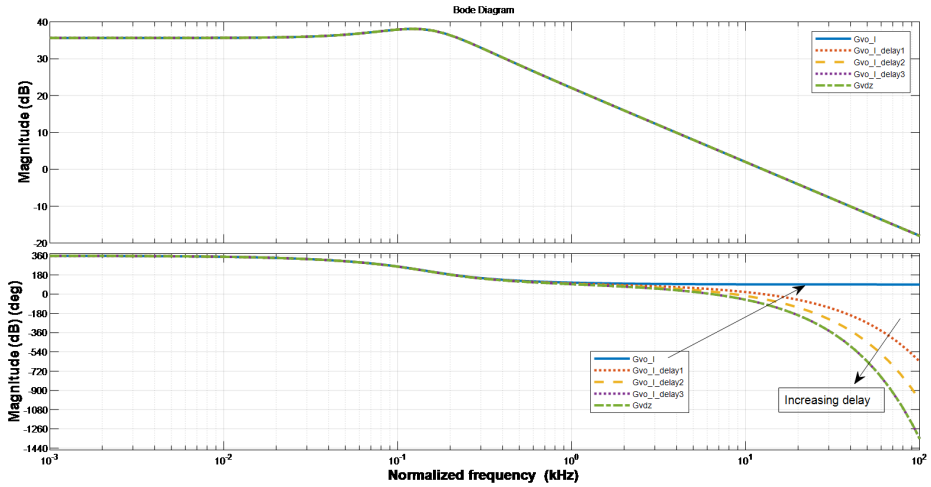


Figure 4.6: Transfer function of simo boost converter with time delay consideration

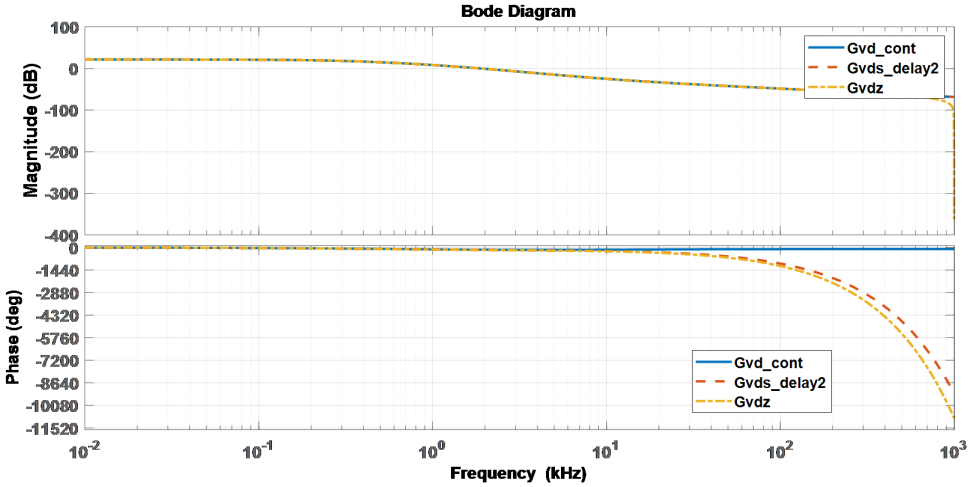


Figure 4.7: Synchronous buck converter comparsion between discrete-time model Gvdz and the effective s domain model with delay into consideration $Gvds_{delay2}$ and Gvd_{cont} (without delay)

4.1.3 Fuzzy Sugeno controller design

Fuzzy Logic controller are among the intelligent control techniques with applications ranging from DC-DC converter control to electric drives speed control. The methodology implemented in this thesis is using feedback output voltage to the controller. The error and change is error is respectively calculated and fed to controller.
Fuzzy set is widely being used in Power electronics application. It also serves a basis for Neural Network techniques which requires training of a model with input and output data.[15]

The fuzzy logic controller serves as intelligent controller for this propose. This methodology is applied in Buck, Boost and various other DC-DC converter. This controller is designed based on group of rules based on human knowledge and understanding. Therefore, the fuzzy controller provides the better steady state and transient performances than

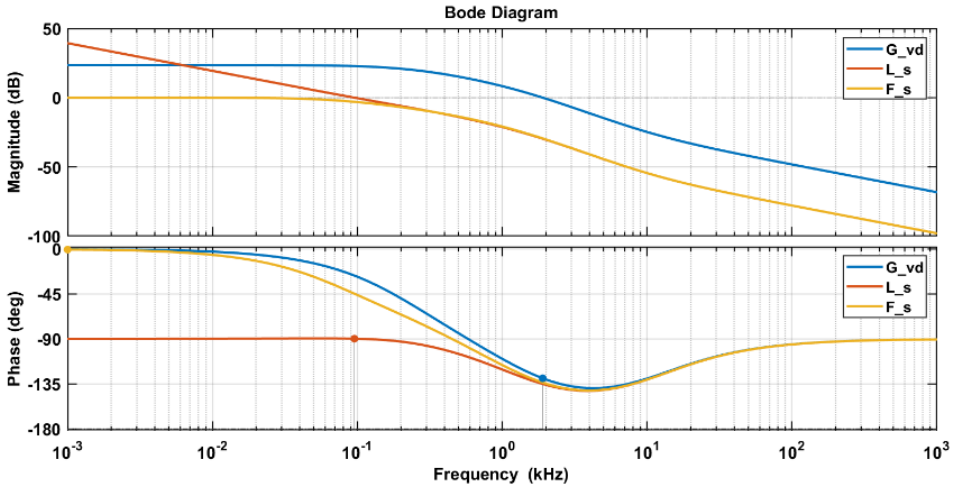


Figure 4.8: Bode plot of PI controller for uncompensated, open loop gain and compensated buck converter

linear PI control. Fuzzy controller also improves the robustness of the systems. It involves four principal steps such as :

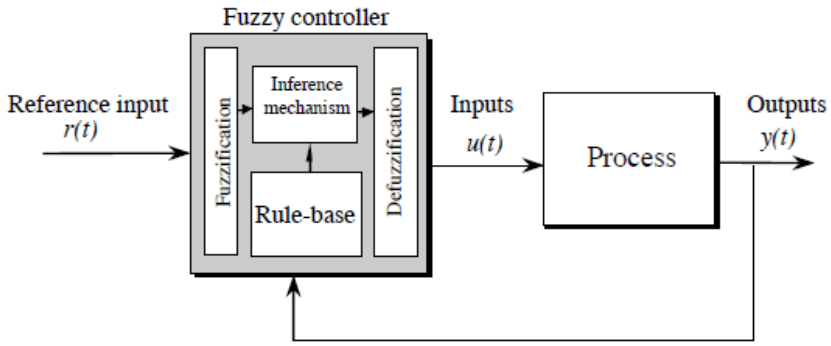


Figure 4.9: Block-diagram-of-fuzzy-logic-control-methodology

Fuzzification

This interface, which converts input data into suitable linguistic values; a knowledge base, which consists of a data base with the necessary linguistic definitions and the control rule set; a decision-making logic which, simulating a human decision process, infer the fuzzy control action from the knowledge of the control rules and linguistic variable definitions; a defuzzification interface which yields non fuzzy control action from an inferred fuzzy control action [15].

It also determines the degree of membership of the input values to defined fuzzy sets (linguistic variables). Absoulute error and differential error are defined as-

1. Absolute error

Error = SetSpeed – CurrentSpeed

2. Differential Vout error

This value is obtained by subtracting the previous error value from the current error value: dError = Error – LastError

The membership functions are triangular base and scaled to 0-1.

Fuzzy Logic Table Rules

		dError, X2[ ]				
		NM	**NS**	**ZE**	**PS**	**PM**
Error, X1[ ]	NM	PM	PM	PM	PS	ZE
	NS	PM	PM	PS	ZE	NS
	ZE	PM	PS	ZE	NS	NM
	PS	PS	ZE	NS	NM	NM
	PM	ZE	NS	NM	NM	NM

Figure 4.10: Fuzzy rules table

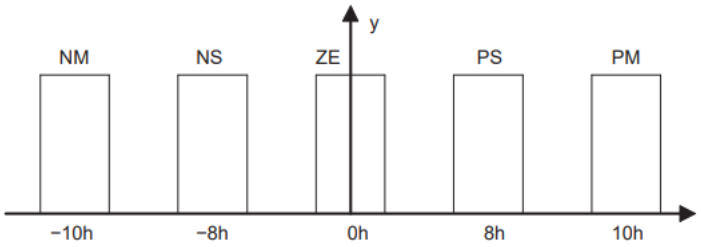


Figure 4.11: Output membership function

Centroid Calculation Defuzzification Method

The result of the defuzzification must be a numeric value that determines the duty factor of the PWM signal that drives the motor. This value is obtained by finding the centroid point of the function that is the result of the multiplication of the output membership function and the output vector Y[ ].

Chapter 5

DSP IMPLEMENTATION FOR DIGITAL CONTROLLERS

5.1 Introduction to Digital Signal Processor

The Discrete control system controls the Power electronics through an output interface (OI). The output interface of the converter has ADC, DAC and PWM etc. These are less susceptible to external disturbances, noise, parameter variation and reliability and cost. This DSP can used to obtain last number of computation with small sampling time such as 1 ms. Also, DSP has application to complex control algorithms and offers good performance[16].

5.2 Digital versus Analog Implementation

Digital controllers are used in various applications through traditionally analog controllers were used. Digital controller accepts digitized voltage which is sampled using smaple and hold circuit and processed by control algorithms. It provids pwm pulsed to drive switching devices.

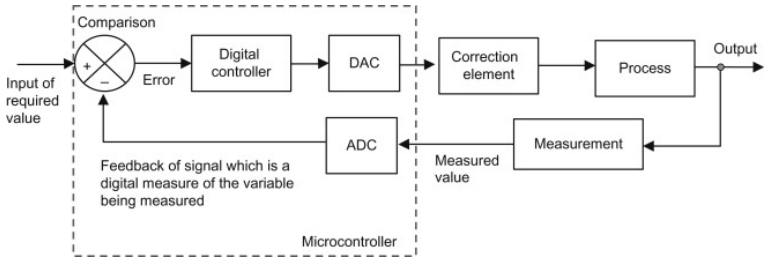


Figure 5.1: DSP based Digital Control System Diagram

Here, the few advantages and disadvantages of digital control are:-

1. Digital components are less prone to environmental variations and aging.
2. These are less sensitive to external harmonics and noise.
3. These is an ease to alter the hardware and alteration can be done easily.
4. Easy monitoring of systems and using IOT diagnostics can be done easily.
5. Some advanced control techniques, such as space vector modulation, adaptive control, fuzzy control, etc.

However, digital control systems are not without disadvantages when compared with analog control systems. Some of the disadvantages are as follows:
1. Finite Finite signal resolution due to the finite word length of the ADCs, and DACs or PWM outputs, which cause the output less accurate. Analog control gives infinite resolution of the measured signal.
2. Time delays in the control loop due to both the sampling of ADCs and computation of the control algorithm by the processors. Analog control can provide continuous processing of signal, thus allowing very high bandwidth.[17]

5.3 The TMS320F2812 DSP

A Digital Signal processor is a single chip which has both processor and the embedded systems. It uses real time control with complex calculations. 8 stages are there for each instruction for final completion. The pipeline is filled with instruction and each instruction is executed per clock cycle. DSP has 150MHz frequency with 6.67ns time taken by each instruction. It is a first 32-bit 150MIPS DSP with on-chip flash memory and on-chip high-precision analog peripherals[18].

5.3.1 Architecture of F2812

The TMS320F2812 Block Diagram can be divided into 4 functional blocks:
1) Internal and External Bus System
2) Central Processing Unit (CPU)
3) Memory
4) Peripherals

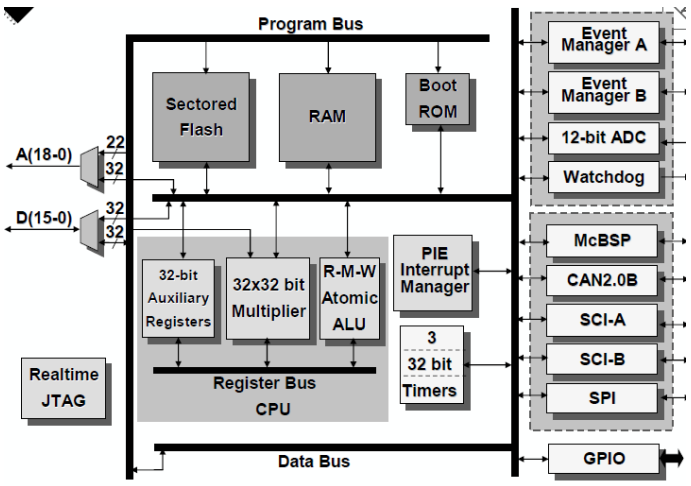


Figure 5.2: C281x Block Diagram

The F2812 CPU

CPU execute most of instructions with register to register operations

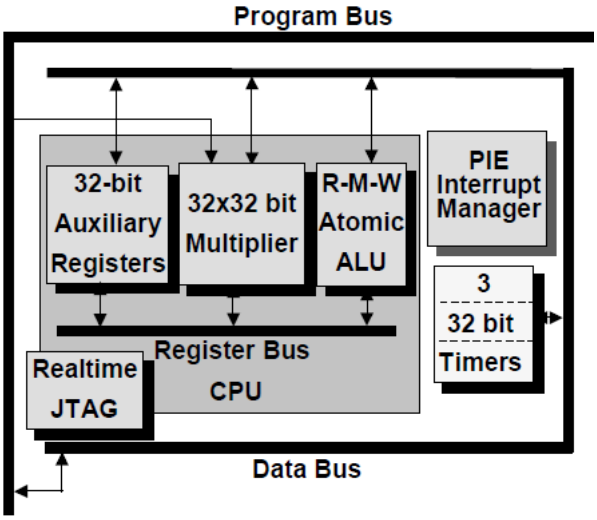


Figure 5.3: C28x CPU

The CPU is able to execute most of the instructions to perform register-to-register operations and a range of instructions that are commonly used by micro controllers, e.g. byte packing and unpacking and bit manipulation in a single cycle. The architecture is also supported by powerful addressing modes, which allow the compiler as well as the assembly programmer to generate compact code that almost corresponds one-to-one with the C code.

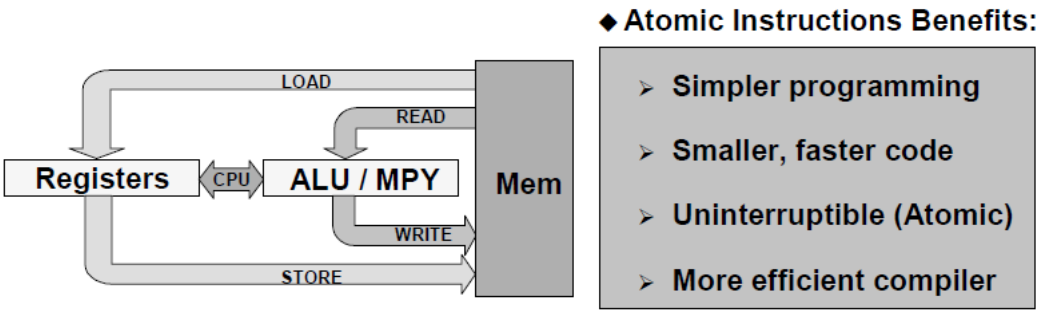


Figure 5.4: Atomic Arithmetic Logic Unit

Internal Bus Structure

The F2812 memory bus architecture contains:
1) A program read bus (22 bit address line and 32 bit data line)
2) A data read bus (32 bit address line and 32 bit data line)
3) A data write bus (32 bit address line and 32 bit data line)

The 32-bit-wide data busses enable single cycle 32-bit operations. This multiple bus architecture, known as a Harvard Bus Architecture enables the C28x to fetch an instruction, read a data value and write a data value in a single cycle. All peripherals and memories are attached to the memory bus and will prioritise memory accesses.

Memory Map

The memory space on the F2812 is divided into program and data space. There are several different types of memory available that can be used as both program or data space. They include flash memory, single access RAM (SARAM), expanded SARAM, and Boot ROM which is factory programmed with boot software routines or standard tables used in math related algorithms. Memory space width is always 16 bit.
The F2812 uses 32-bit data addresses and 22-bit program addresses. This allows for a total address reach of 4G words (1 word = 16 bits) in data space and 4M words in program space.

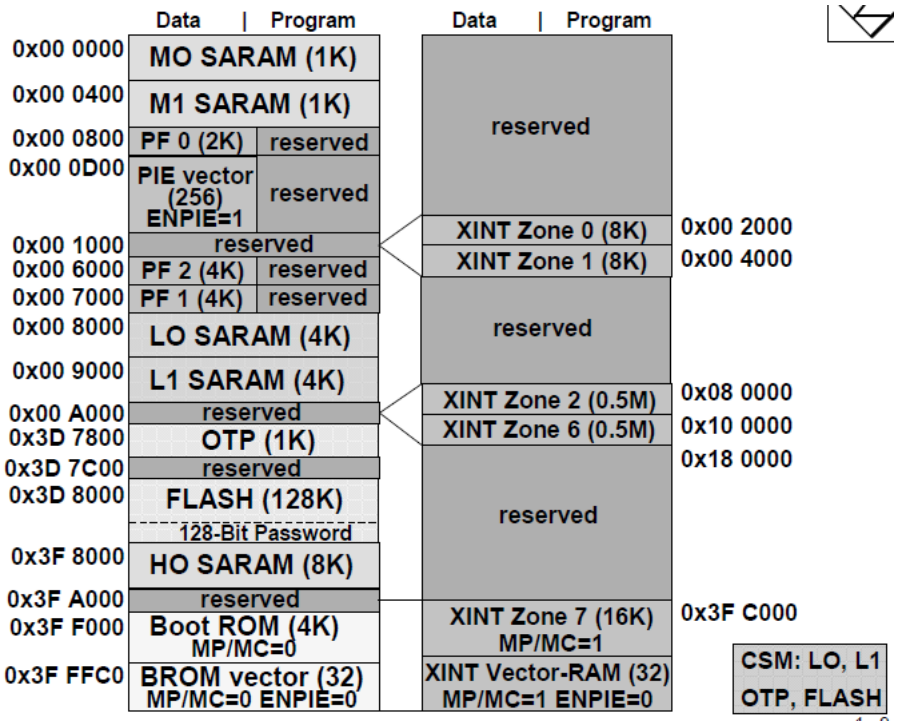


Figure 5.5: TMS320F2812 Memory Map

Interrupt Response

The fast interrupt response, with automatic "context" save of critical registers, resulting in a device that is capable of servicing many asynchronous events with minimal latency. Here "context" means all the registers you need to save so that you can go away and carry out some other process, then come back to exactly where you left. F2812 devices implement a zero cycle penalty to save and restore the 14 registers during an interrupt. This feature helps to reduce the interrupt service routine overheads.
The Peripheral Interrupt Expansion (PIE) – Unit allows the user to specify individual interrupt service routines for up to 96 internal and external interrupt events. All possible 96 interrupt sources share 14 maskable interrupt lines (INT1 to INT14), 12 of them are controlled by the PIE – module.

5.3.2 Peripherals of a DSP

Digital I/O Unit:

Integrated peripherals give the C28x an important advantage over other processors. All digital I/O's are grouped together into "Ports", called GPIO-A, B, D, E, F and G, means "general purpose input output".

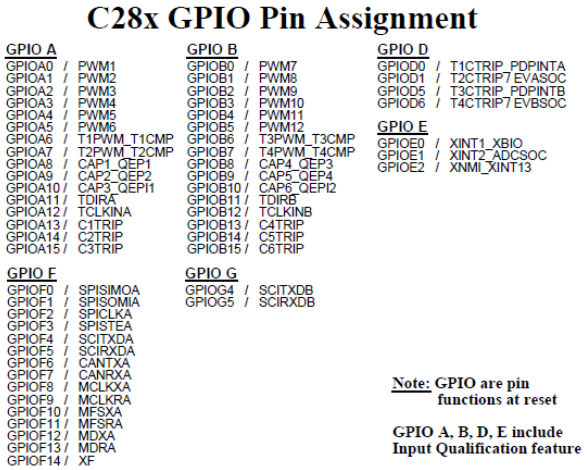


Figure 5.6: GPIO Pin Assignment

All six GPIO-Ports are controlled by their pwm multiplex register, called GPxMUX (where x stands for A to F). Clearing a bit position to zero means selecting its digital I/O function, setting a bit to 1 means selecting the special function. Most of the peripheral signals are multiplexed with general-purpose I/O (GPIO) signals. This enables to use a pin as GPIO if the peripheral signal or function is not used. On reset, all GPIO pins are configured as inputs. One can then individually program each pin for GPIO mode or Peripheral Signal mode.

5.3.3 PWM Generators and ADC of TMS320F2812

Event Manager

The F2812 has 2 Event Manager peripherals on-chip to provide a broad range of functions and features that are particularly useful in control applications. The event manager modules include general-purpose (GP) timers, full compare/ PWM units, capture units, and quadrature-encoder pulse (QEP) circuits. The 2 Event Manager modules are identical peripherals intended for multi-axis/digital control applications.
The event manager (EV) modules provide a broad range of functions and features that are particularly useful in motion control and motor control applications.

General-Purpose (GP) Timers

There are two GP timers. The GP timer x (x = 1 or 2 for EVA; x = 3 or 4 for EVB) includes:

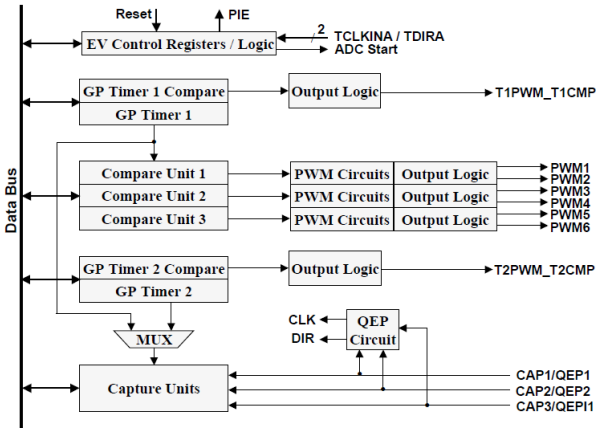


Figure 5.7: Event Manager block diagram

1) A 16-bit timer, up-/down-counter, TxCNT, for reads or writes.
2) A 16-bit timer-compare register, TxCMPR, for reads or writes.
3) A 16-bit timer-period register, TxPR, for reads or writes.
4) A 16-bit timer-control register, TxCON, for reads or writes.
5) A selectable direction input pin (TDIRx) (to count up or down when directional up-/down-count mode is selected).

The GP timers can be operated independently or synchronized with each other. The compare register associated with each GP timer can be used for compare function and PWM-waveform generation. There are three continuous modes of operations for each GP timer in up- or up/downcounting operations.
Internal or external input clocks with programmable prescaler are used for each GP timer. GP timers also provide the time base for the other event manager sub modules: GP timer 1 for all the compares and PWM circuits, GP timer 2/1 for the capture units and the quadrature pulse counting operations. Double-buffering of the period and compare registers allows programmable change of the timer (PWM) period and the compare/PWM pulse width as needed [21].
Full-Compare Units There are three full-compare units on each event manager. These compare units use GP timer1 as the time base and generate six outputs for compare and PWM-waveform generation using programmable deadband circuit. The state of each of the six outputs is configured independently. The compare registers of the compare units are double-buffered, allowing programmable change of the compare/PWM pulse widths as needed.

Timers

CPU-Timers 0, 1, and 2 are identical 32-bit timers with presettable periods and with 16-bit clock prescaling. The timers have a 32-bit count down register, which generates an interrupt when the counter reaches zero. The counter is decremented at the CPU clock speed divided by the prescale value setting. When the counter reaches zero, it is automatically reloaded with a 32-bit period value.

$$f_{PWM} = \frac{f_{CPU}}{T1PR.TPS_{T1}.HISCP} \tag{5.1}$$

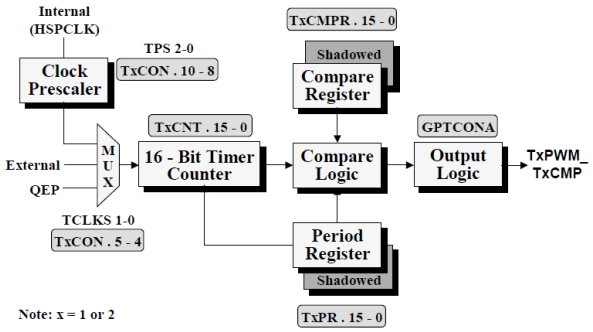


Figure 5.8: General purpose Timer Block diagram

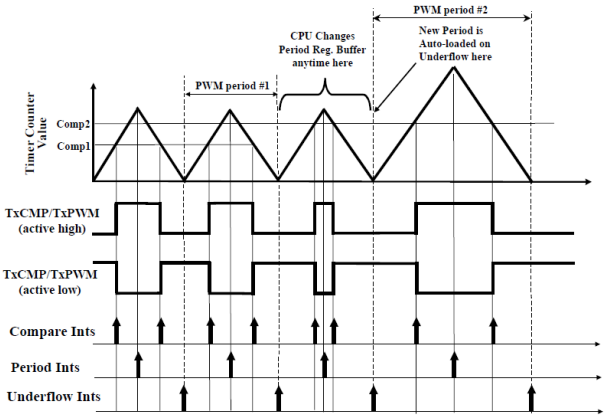


Figure 5.9: Generated Outputs and interrupts

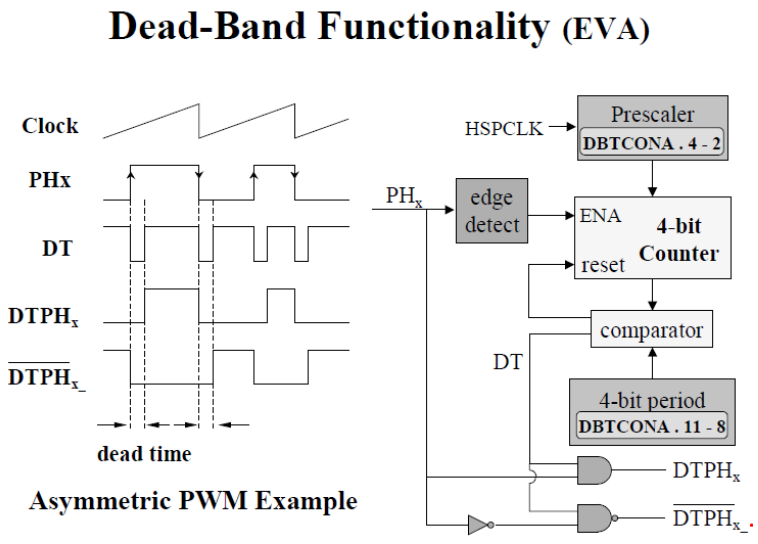


Figure 5.10: Dead-Band Functionality in EVA

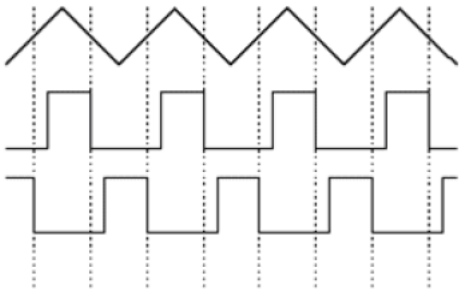


Figure 5.11: Deadband in PWM waves

with $TPST1 = 1$, $HISCP = 2$, $f_{CPU} = 150MHz$ and a desired $f_{PWM} = 50kHz$ we derive: $T1PR = 1500$

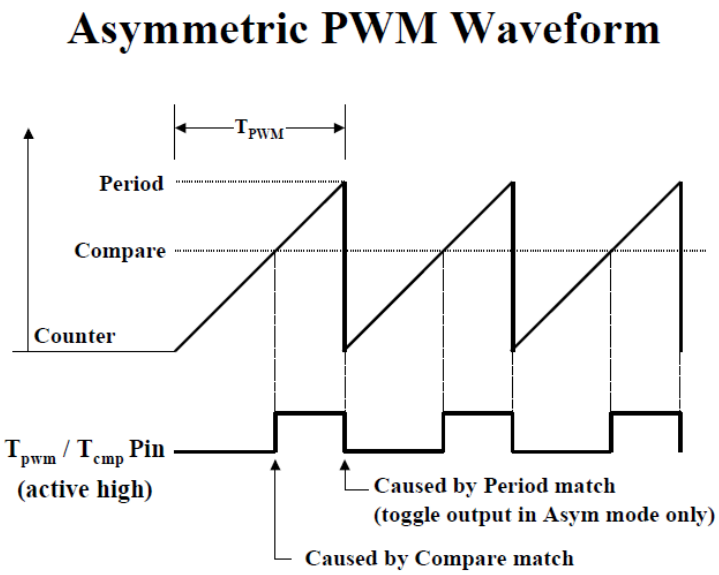


Figure 5.12: Asymmetric PWM waveform

T1CMPR defines the width of the PWM-pulse.

Analogue Digital Converter

an important interface between the controller and the real world. Most physical signals such as temperature, humidity, pressure, current, speed and acceleration are analogue signals. The purpose of the ADC is to convert this analogue voltage in a digital number.

The C28x internal ADC has a 12 Bit resolution (n =12) for the digital number D. This gives:

$$V_{in} = \frac{D \times 3.0V}{4085} = 0.73mV \tag{5.2}$$

It has two sh units, which can be used in parallel ("simultaneous sampling"). Each sample and hold is connected to 8 multiplexed input lines. The auto sequencer is a programmable state machine and is able to automatically convert up to 16 input signals. Each state of the auto sequencer puts a measurement into its own result register.The

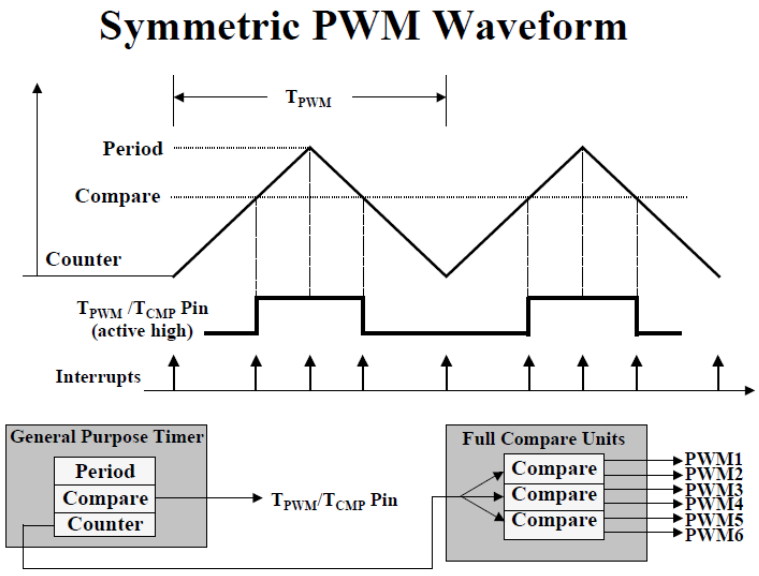


Figure 5.13: Symmetric PWM Waveform

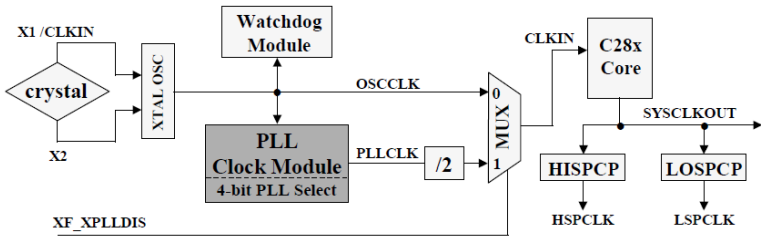


Figure 5.14: Clock

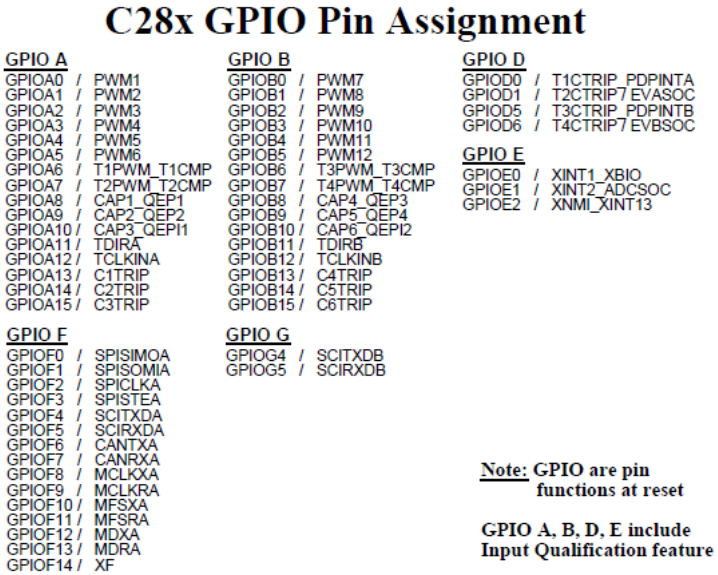


Figure 5.15: GPIO Pin assignment

fastest conversion time is 80ns per sample in a sequence and 160ns for the very first sample.
To obtain the specified accuracy of the ADC, proper board layout is very critical. To the best extent possible, traces leading to the ADCINxx pins should not run in close

15 - 3	2	1	0
reserved	HSPCLK2	HSPCLK1	HSPCLK0

15 - 3	2	1	0
reserved	LSPCLK2	LSPCLK1	LSPCLK0

H/LSPCLK2	H/LSPCLK1	H/LSPCLK0	Peripheral Clock Frequency
0	0	0	SYSCLKOUT / 1
0	0	1	SYSCLKOUT / 2 (default HISPCP)
0	1	0	SYSCLKOUT / 4 (default LOSPCP)
0	1	1	SYSCLKOUT / 6
1	0	0	SYSCLKOUT / 8
1	0	1	SYSCLKOUT / 10
1	1	0	SYSCLKOUT / 12
1	1	1	SYSCLKOUT / 14

Figure 5.16: Clock frequency Setting

proximity to the digital signal paths. This is to minimize switching noise on the digital lines from getting coupled to the ADC inputs. Furthermore, proper isolation techniques must be used to isolate the ADC module power pins from the digital supply.

Sampling Theorem

Let $x_a(t)$ be a band-limited signal with $X_a(j\omega) = 0$ for $|\omega| > \omega_m$. Then $x_a(t)$ is uniquely determined from its samples $x(k) = x_a(kT)$ if the sampling frequency $\omega_s > 2\omega_m$, i.e., the sampling frequency must be at-least twice the highest frequency present in the signal.

5.3.4 Practical Aspects of Digital Control- Choosing Sampling rate

In practical circuit design, word length and computational performance effects the digital control. The sampling period with high value tends to give better performance for a digital control system. Finite Wordlength is another problem when high sampling rate is chosen. Probably, sampling frequency is chosen to be higher than 20 to obtain a good behaviour. In majority cases sampling frequency is also chosen equal to switching frequency.

5.3.5 Filtering -anti aliasing Filter

To be sure that the frequency content of the input signal is limited, a low pass filter (a filter that passes low frequencies but attenuates the high frequencies) is added before the sampler and the ADC. This filter is an anti-alias filter because by attenuating the higher frequencies (greater than the Nyquist frequency) and prevents the aliasing components from being sampled. Because at this stage (before the sampler and the ADC) you are still in the analog world, the anti-aliasing filter is an analog filter.

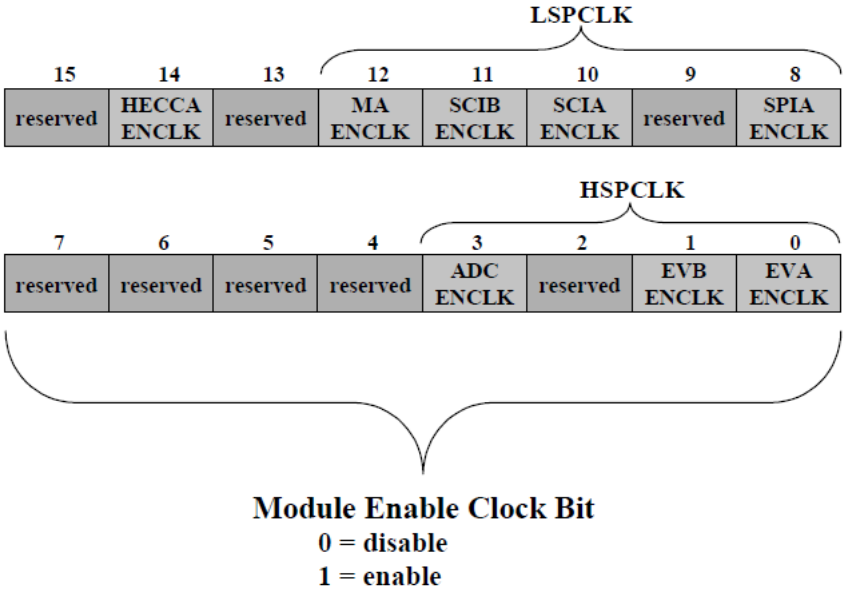


Figure 5.17: PCLKCR Register

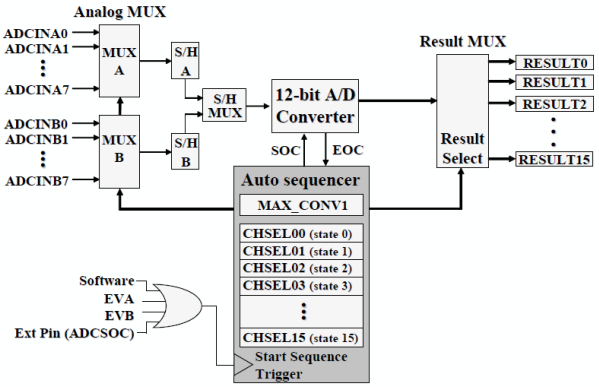


Figure 5.18: ADC block Diagram

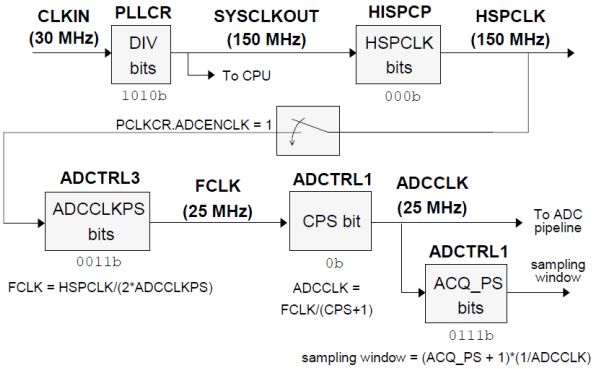


Figure 5.19: ADC Clock Setting

An ideal anti-alias filter passes all the appropriate input frequencies (below f1) and cuts off all the undesired frequencies (above f1).

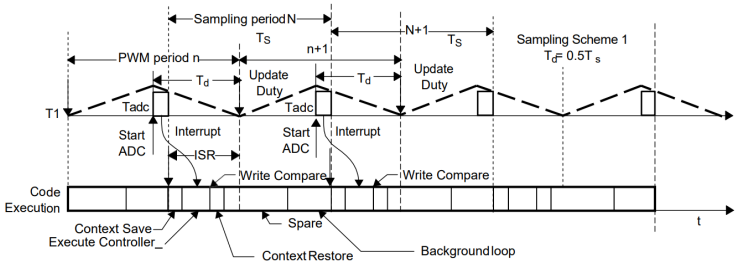


Figure 5.20: Digital control loop sampling

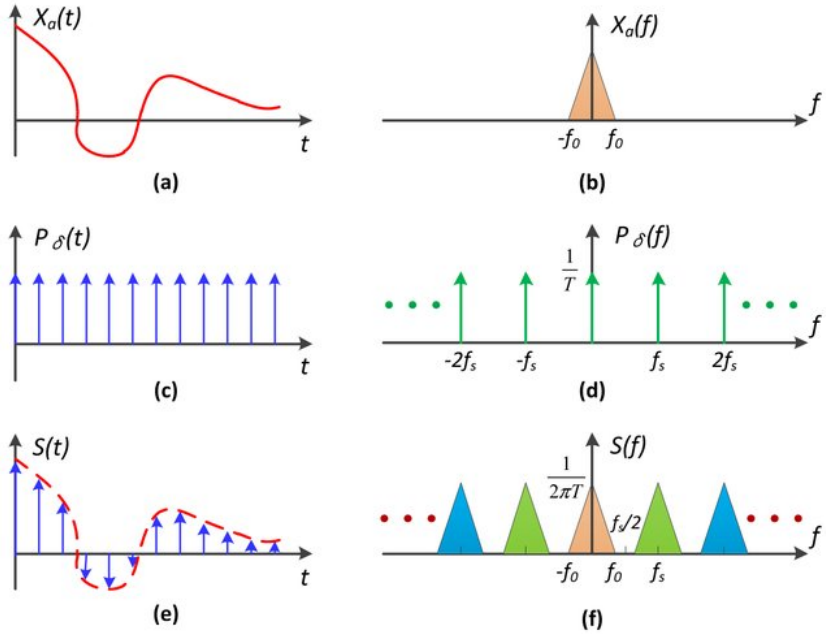


Figure 5.21: Nyquist Sampling theoram

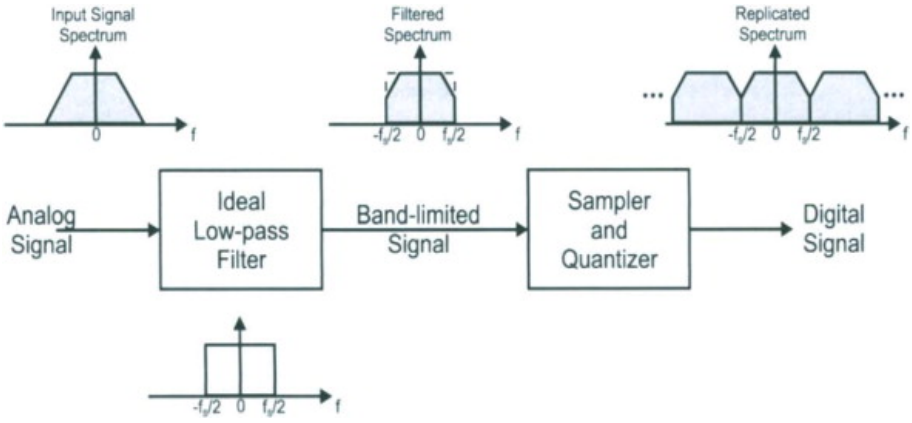


Figure 5.22: Function of ideal LPF

Although you want to pass only signals with frequencies ¡ fs/2, those signals in the transition band could still cause aliasing. Therefore in practice, the sampling frequency should be greater than two times the highest frequency in the transition band. This turns out to be more than two times the maximum input frequency (f1). That is one reason

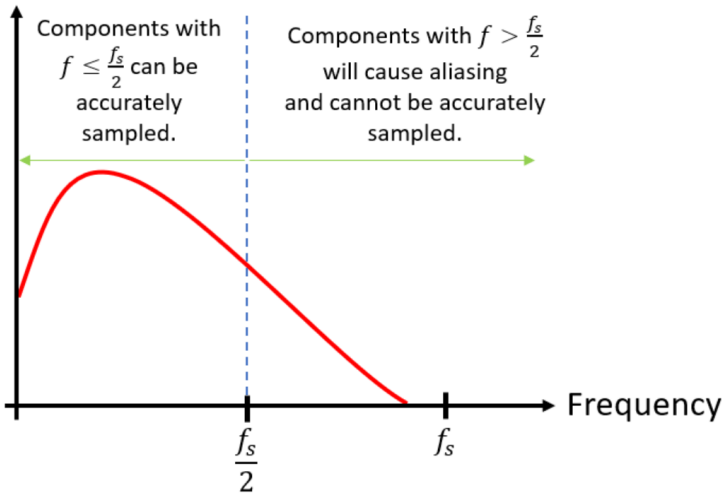


Figure 5.23: Choice of Sampling Frequency

why you may see that the sampling rate is more than twice the maximum input frequency.

Chapter 6

SYSTEM HARDWARE DEVELOPMENT

In this chapter, hardware development circuitry and implementation of Digital control loop for Single input multi output Boost converter and its various circuits such as Scaling, isolation circuit, voltage sensor etc. A DSP (Digital Signal Processor) is used to generate the firing Pulse width modulation pulses for the converter's power semiconductor switches S1 and for sensing the real time output voltage from voltage sensor. Initially the voltage is scaled from $0-40V$ to $0-8V$ (0.2 scaling factor). As this is boost circuit, the output voltage goes on increasing further and inorder to achieve more scaling relatively, a Subtractor circuit with voltage reference as 2.81V and V_{in} as scaled output of converter for higher range voltage control is being used using 741 opamp.

An isolation circuit is required to seperate the power circuit to digital circuit. Therefore Power ground and DSP ground are isolated from each other using an Optocoupler IC called as TLP350H with suitable calibration done via potentiometer to obtain 0-3V as scaled output. A LPF with R as 56Ω and $C = 0.1\mu F$ is set with a cut-off frequency as $1/RC$ to pass the frequency components below cut-off frequency. This analog signal is given to ADC input pin which is compared to the V_{ref} and an error is being generated. The controller performs its action and a control command called as duty ratio is generated. This is given to power circuit switches with appropriate isolation using optocoupler.

6.1 Power circuit Development

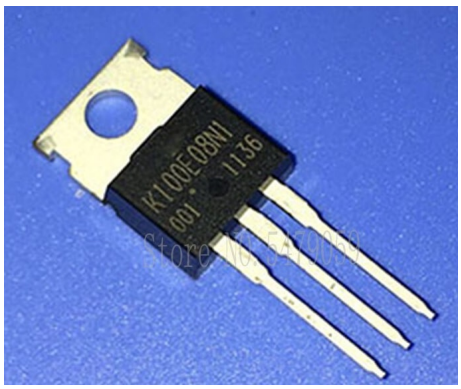


Figure 6.1: MOSFET-TK100E10N1

Here, the MOSFET used is TK100E10N1 at 50khz switching frequency. Each MOS-

FET switch carries an inbuilt anti-parallel freewheeling diode. MOSFETS's are self-commutated devices therefor no forced commutation is required to them.

6.2 Driver Circuit

The opto coupler TLP350H provides necessary isolation between the low voltage isolation circuit and high voltage power circuit. Optocoupler is used to drive a N channel MOSFET or IGBT for both high side and low side configurations.

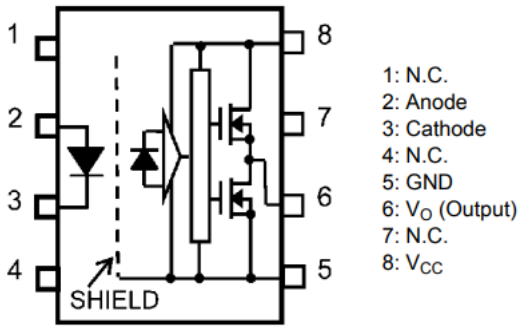


Figure 6.2: TLP350H optocoupler internal circuit

Figure 6.3: TLP350H optocoupler

The TLP250 has both input and output side and it is optically isolated driver means there is no direct connection. Isolation is provided using light sensitive LED called as photodetector.

The TLP350H is a photocoupler in a DIP8 package that consists of a GaA As infrared light-emitting diode (LED) optically coupled to an integrated high-gain, high-speed pho-

todetector IC chip. It provides guaranteed performance and specifications at temperatures up to 125 Celsius. The TLP350H has an internal Faraday shield that provides a guaranteed Common-mode transient immunity of ±20 kV/µs. It has a totem-pole output that can both sink and source current[19].
The TLP350H is ideal for IGBT of small capacity to middle capacity and power MOSFET gate drive

6.3 Voltage Sensor

Voltage sensor is based on potential divider using resistors. It is used to maintain the ratio as 5 : 1 and provides the scaling of 0.2. In this way it reduces the input voltage by 5 times.

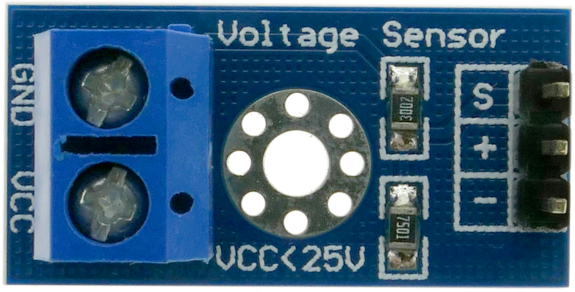


Figure 6.4: Voltage Sensor

Parameters
1. Voltage input range : $0 - 25V$
2. DC input interface: terminal positive terminal is connected to V_{CC}, negative terminal is connected to GND

The voltage at the output of the isolation amplifier is $v_{ov} = v1(R2/(R1 + R2))$. Thus the output voltage v_{ov} is properly scaled by a scalar circuit and the output voltage is given to the ADC of DSP kit.

6.3.1 Hardware Set-Up

Power electronics applications demands high-speed data acquisition and control. Therefore, Digital Signal processor (DSP) are used to meet the processing requirements in latest advances. TMS320 family has a fixed point and floating-point DSPs and targets wide variety of digital control application[17]. It also supports peripherals such as event manager

(EVM), timers for PWM, dual 12-bit, 16 channel ultrafast ADC used for embedded control and communication. The overall program control and step by step implementation of PI controlled boost converter flowchart structure is shown in Figure[20].

The block diagram of complete experimental setup and the Digital implementation flowchart is shown below in figure 6.5 and 6.7.

The output voltage for a particular instant is sensed by voltage sensor circuit and is given in-put to DSP via ADC channel. The digital value of voltage output result from DSP, obtained after ADC conversion is compared to reference voltage. An interrupt is generated after AD conversion and controller implementation is initiated. The updated duty ratio inside ISR is computed and given to appropriate PWM compare register. The Sampling frequency of the ADC is chosen as equal to switching frequency of the converter to reduce the sampling delay, $f_s = 2 \times f_{sw} = 50kHz$. The Sampling time of ADC is the total of acquisition time and conversion time. Acquisition time is Sample and hold (SOH) cycles (set as15) times the ADC clock time (1/3Mhz) and conversion time which is 0.5ms for the ADC. The Voltage reference was kept as 30V with scaling of 0.1. The resolution of 12bit ADC (1/4096×3 V) is 0.73mV. The range of ADC is 0-3V. In the feedback circuitry, output voltage is scaled by gain of 0.2 using opamp 741 and is given to ADC of DSP using optocoupler[10].

6.4 Design issues in Digital control

Latency or phase delays, sampling effects (adequate data acquisition), quantization errors and inclusion of Limit cycles are few of the major issues encountered in digital control.

6.4.1 Effect of Sampling frequency

Due to Digital component presence , there is latency in response to control effort. therefore main problem with digital control is effect of Sampling and Quantization.Sampling frequency is defined as number of samples recorded from continuous analog signal per second. It needs to be accurately selected for reconstruction of signal (without aliasing). According to Nyquist-Shannon sampling theorem, sampling frequency must be two times the frequency of analog signal to be sampled. Theoretically, the above criteria is followed but practically it should be $10 - 20$ times higher than switching frequency. Higher sampling rates results into wider Bandwidth and therefore more aggressive and faster control operations can be performed. The control with high sampling rates allows faster dynamics and better monitoring to responds rapidly to changes. It also smoothens the ripples in output voltage as observed in figure7.13.

Bandwidth described the analog's front end's ability to get the signal with minimum loss amplitude[14]. Practically, it defines the range of frequencies the oscilloscope can measure. Aliasing refers to appearance of false frequency components in the sample data. Therefore, to accurately reflect the input analog signal, following conditions needs to be ensured:
1) The sampling frequency is increased and maximum frequency is chosen for samples.
2) Using Anti-aliasing Filters to remove all the frequency content greater than then the

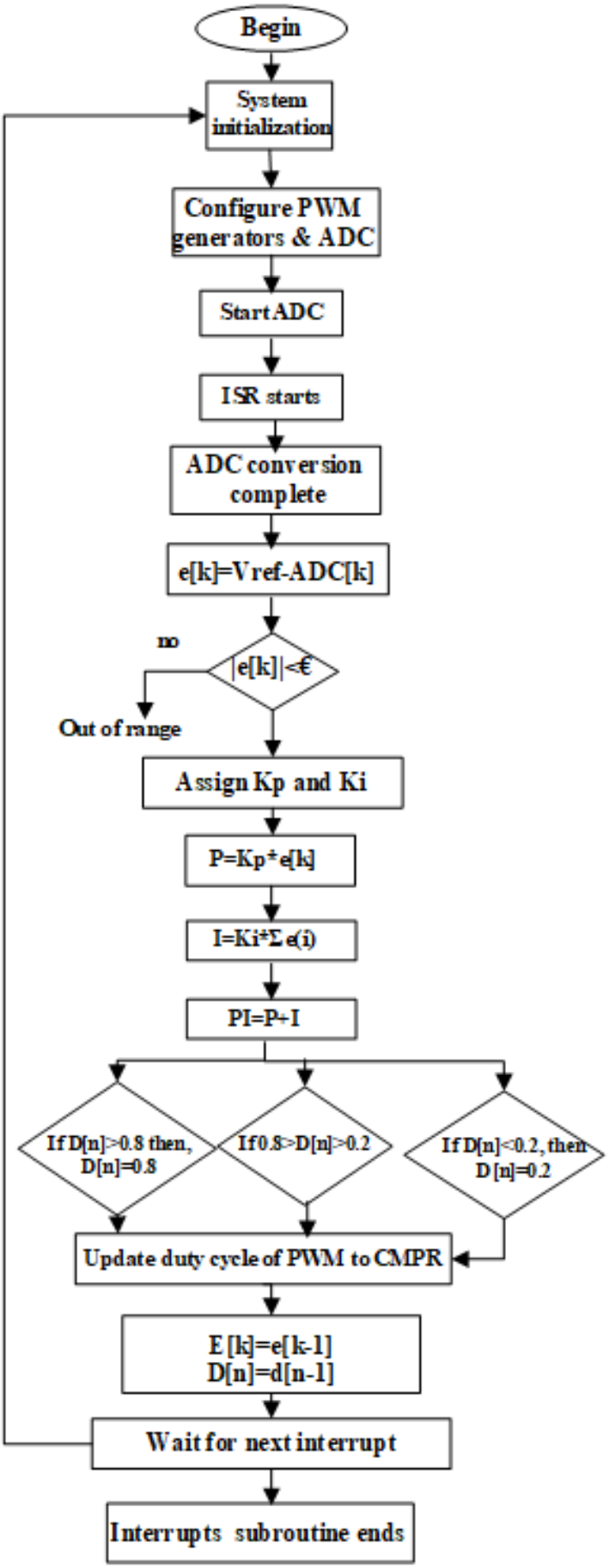


Figure 6.5: Flowchart of implementation of Digital control

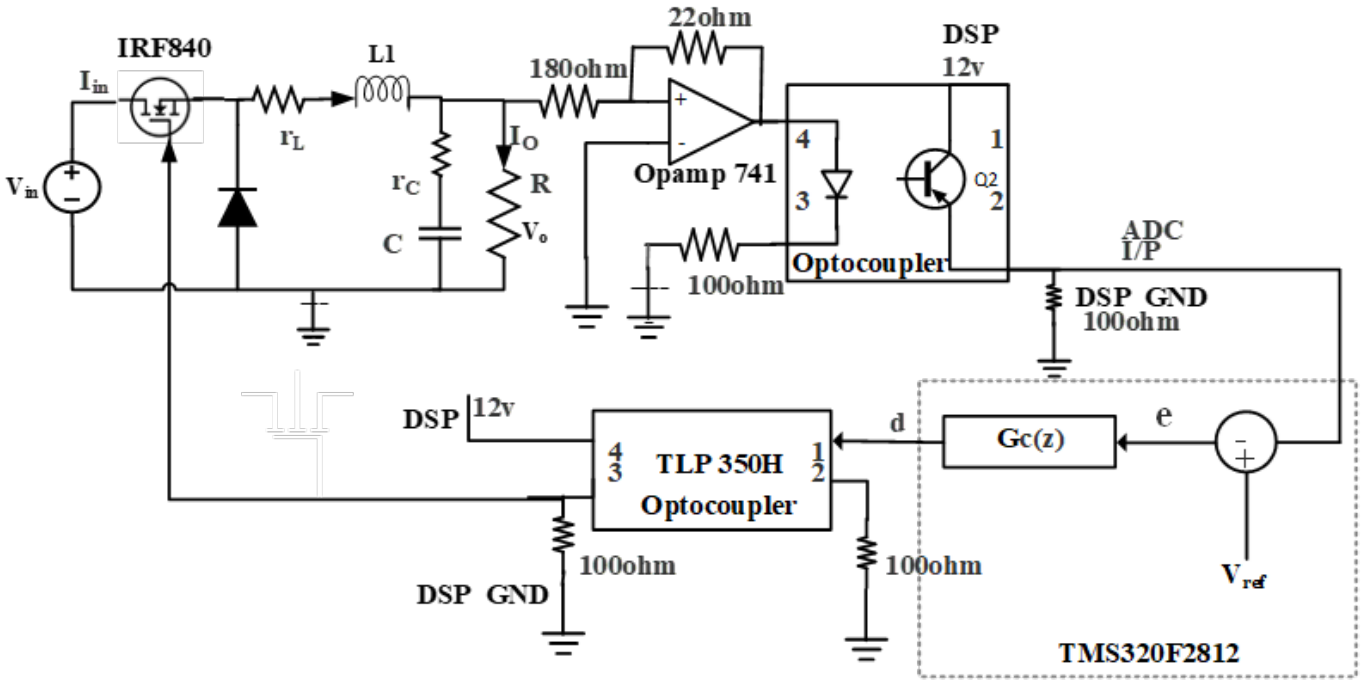


Figure 6.6: Buck complete control circuit block diagram

Nyquist frequency.
As long as the sampling rate is high, signal can be detected with high accuracy and quantization.

6.4.2 Limit cycles

Limit cycle is a condition when output voltage oscillates around steady state output. It can also be defined as steady state oscillations of lower frequency (less than switching frequency)[12]. Due to the presence of ADC and DPWM quantization (i.e amplitude and time quantization) in feedback control loop, there is an occurrence of zero bin error and limit cycle condition as shown in figure 7.14. This results in production of noise, persistant disturbances and EMI in output of converter. Let ADC resolution of N bits be ΔV_{adc} and DPWM resolution be q_{dpwm}. When DPWM resolution is less than ADC resolution, non linear effects affect the output and no steady state solution is achieved.

No limit cycle condition is the non-existence of steady state oscillations and existence of dc steady state solution. To eliminate Limit cycles, an equivalent DPWM resolution should be greater than the equivalent ADC resolution along with inclusion of integral action in feedback control loop.

$$q_{DPWM} > q_{ADC} \tag{6.1}$$

Provided $K_i \leq 0$ i.e. integral gain. With finer DPWM resolution, the mapping into zero bin error of DPWM levels is eliminated and equilibrium solution is obtained as shown in figure 7.15. The DPWM resolution is kept as 5760 which is greater than the resolution

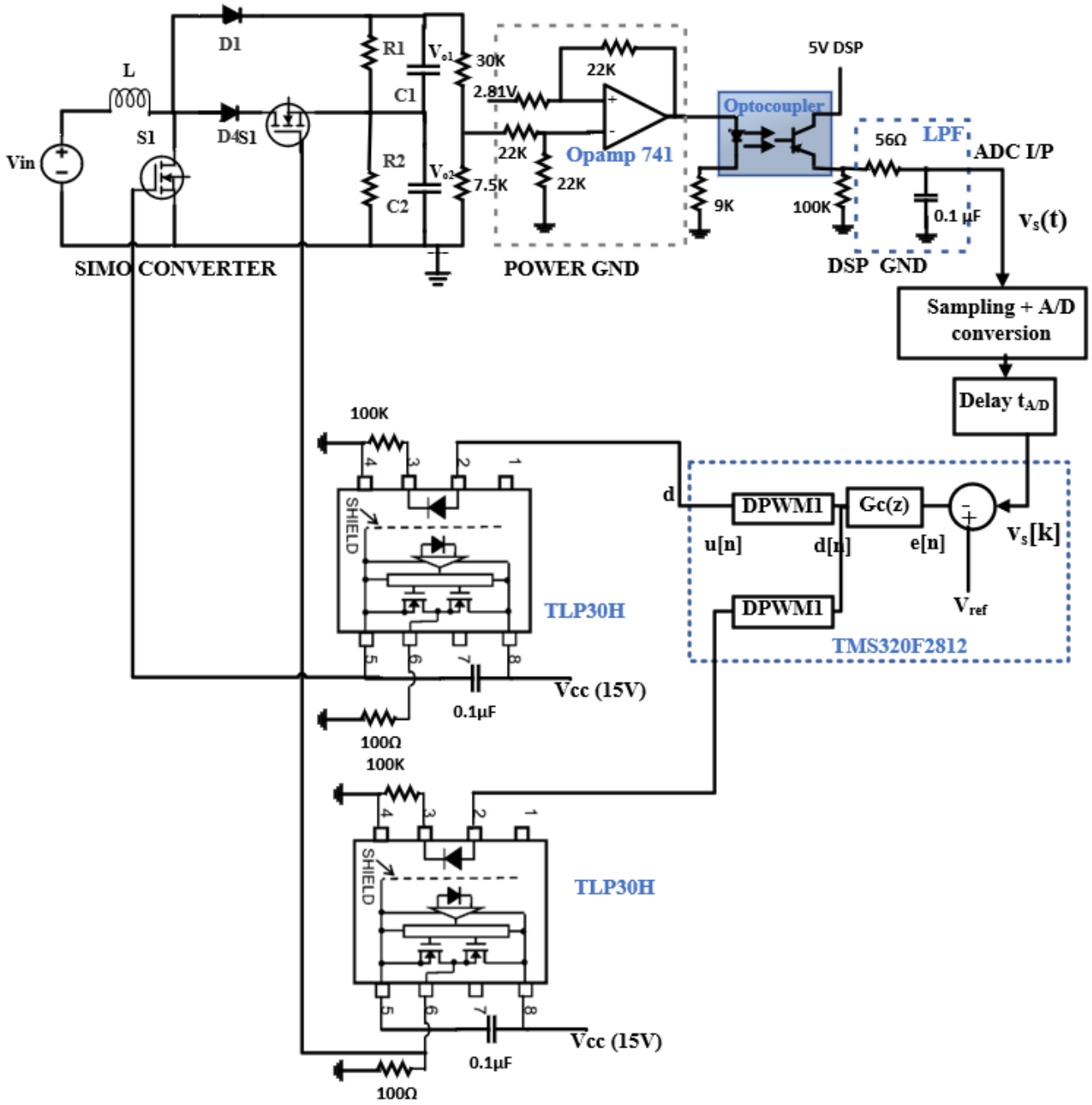


Figure 6.7: SIMO boost complete control circuit block diagram

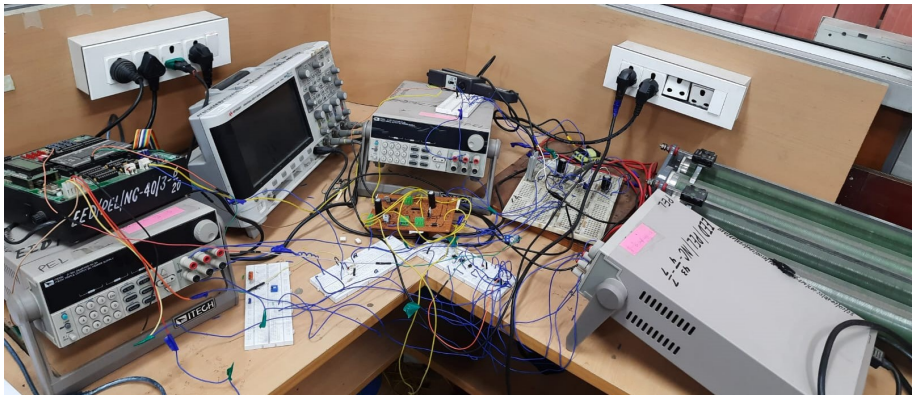


Figure 6.8: SIMO boost complete control circuit hardware setup

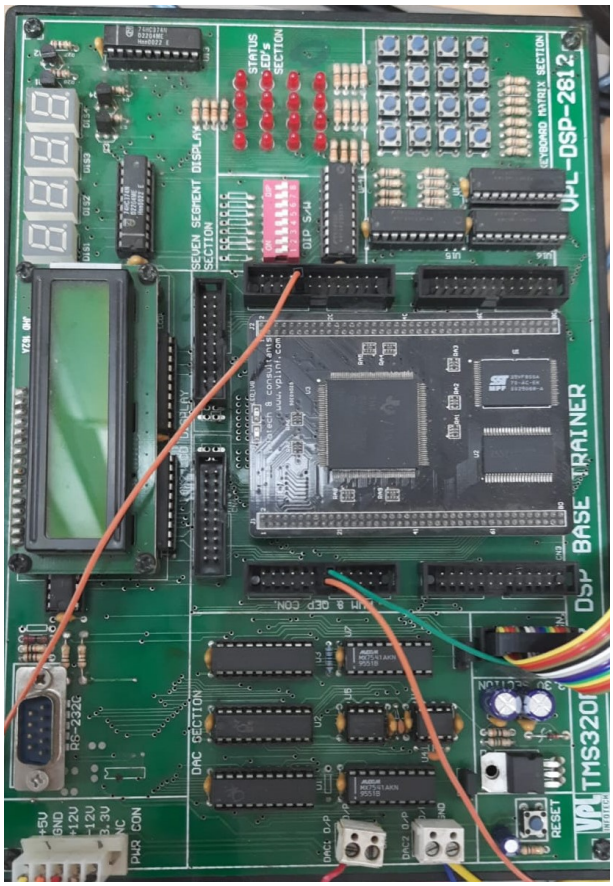
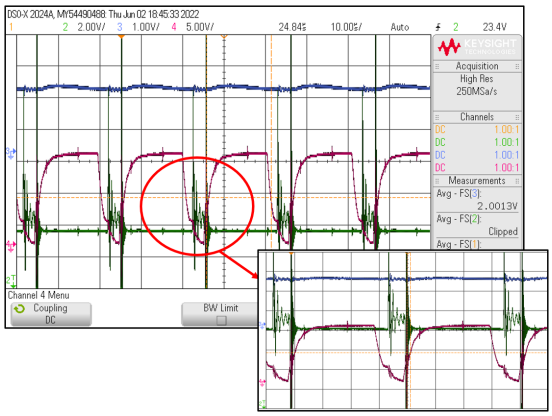
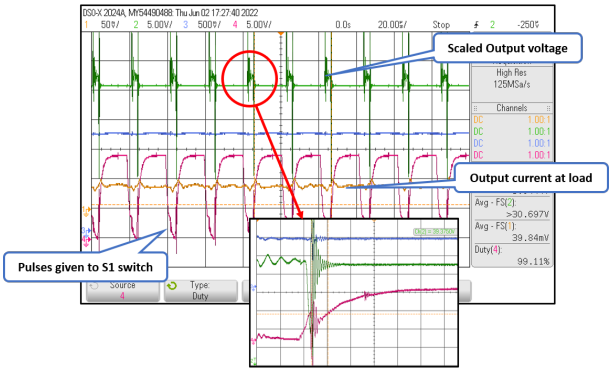


Figure 6.9: DSP TMS320F2812

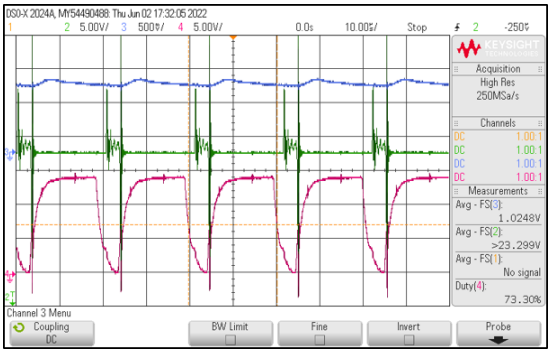


(a) Output dynamics of converter using sampling frequency lower than converter switching frequency-fs is 17.3kHz

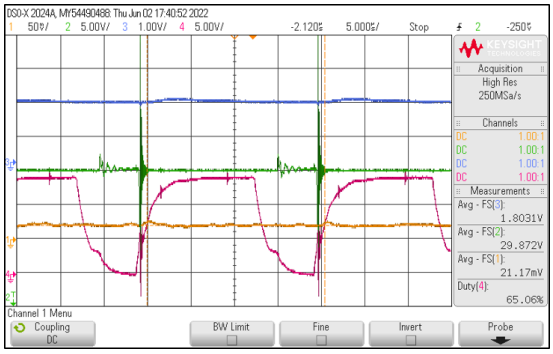


(b) Output dynamics of converter using sampling frequency lower than converter switching frequency-fs is 37.818kHz

(c) output waveforms when Sampling frequency is equal to switching frequency at fs = 50kHz



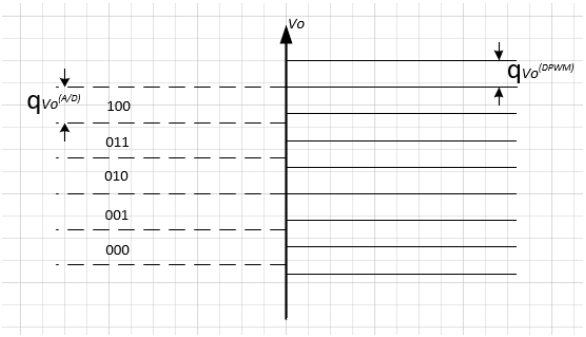
(d) output waveforms when Sampling frequency is more than switching frequency (195kHz)



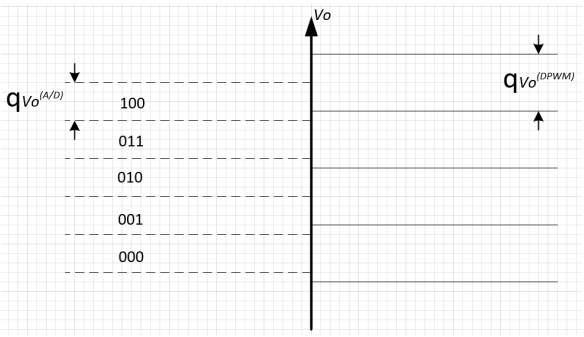
(e) output waveforms when Sampling frequency is much greater than switching frequency at 520 kHz

Figure 6.10: Effect of change in Sampling frequency

of ADC, 4095.

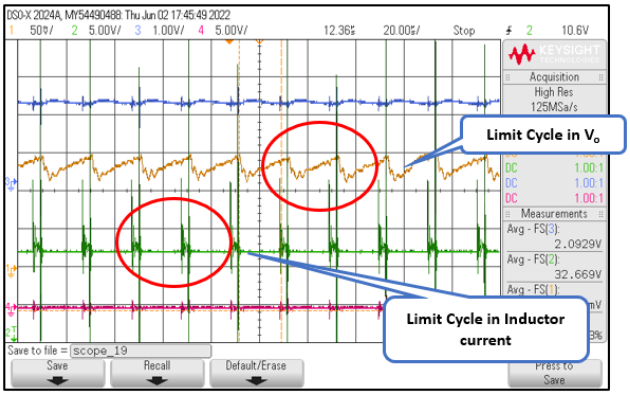


(a) DPWM resolution is finer than the A/D resolution in terms of output voltage quantization

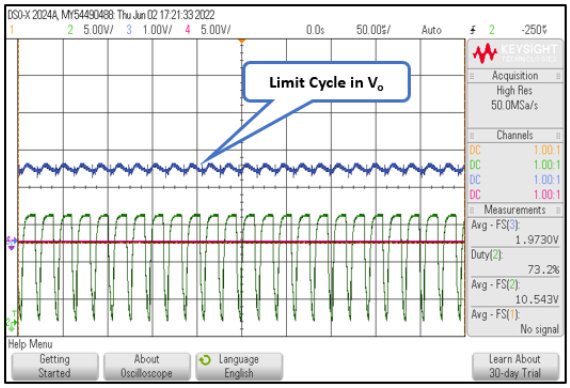


(b) DPWM resolution is coarser than the A/D resolution in terms of output voltage quantization.

Figure 6.11: Conditions for Limit cycle

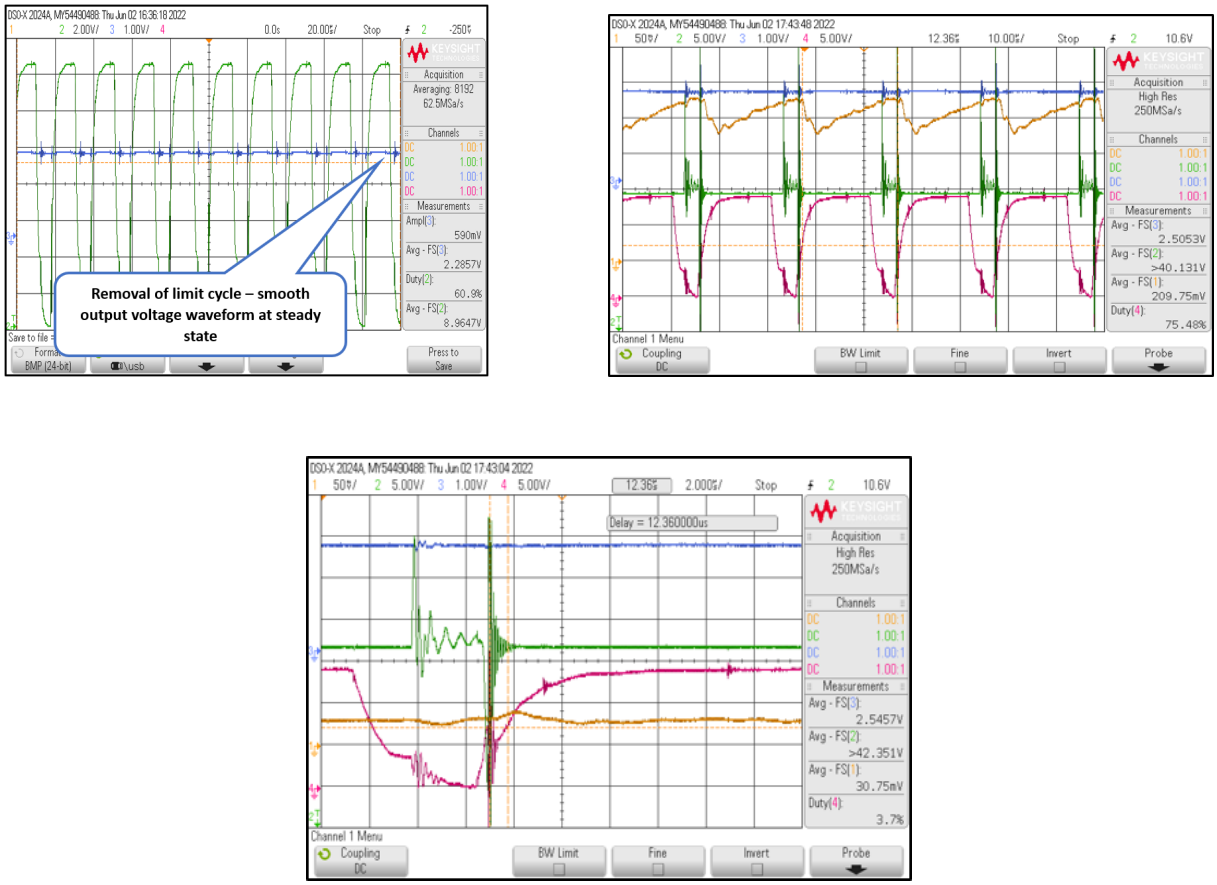


(a) Limit cycles occurrence in converter



(b) Limit cycles occurrence in converter

Figure 6.12: Limit cycle in converter



(a) Limit cycles occurrence in converter

Figure 6.13: No-limit cycles occurrence in converter

Chapter 7

RESULTS AND DISCUSSIONS

For this experimental work, the prototype of boost converter of 12-16V input and 45V output was being developed with nominal duty ratio as 0.6 and 0.7 for both switches. Resistive load was varied from 18Ω to 25Ω to observe the output voltage regulation. In Figure 7.3 and 7.4, steady state output voltages (V), inductor current (A) and switching pulses generated by controller for switching power semiconductor devices are shown. Output sensed by ADC, scaled output voltage by voltage sensor and non-inverting amplifier circuit, Low pass filter responses are also shown in below figures 7.5 to 7.9.

Figure 7.10, 7.11 and 7.12 shows the removal of ripples and noise using 138kHz cut-off frequency which is 1.3 times the Nyquist frequency. It acts as a anti-alias filter and used to filter the high frequency components from the output voltage and maintains the desired Bandwidth.

Table 7.1: Closed loop results for synchronous Buck converter

$Vref(mV)$	$V_o(V)$	D	$I_{in}(A)$
1000	2.96	0.23	1.50
1500	4.10	0.38	2.30
2000	5.70	0.48	2.90
2500	7.20	0.61	3.01

Table 7.2: Reading of Closed loop control of converter using PI controller

ADC reading (mV)	V_{ref} (mV)	**Total V_o of simulation(V)**	**V_o of converter(V)**	I_{in} **(A)**	D_1 **of CRO**	D_1 **of DSP**	V_o **(V) of LPF**
1372	1200	24	26	1.35	0.40	0.50	1.60
1468	1500	30	28	1.57	0.45	0.55	1.74
1589	1600	32	30	1.90	0.44	0.48	1.96
1850	1800	36	33	2.50	0.56	0.61	2.09
2154	2000	40	37	2.90	0.55	0.7	2.29

In Table 7.3, Output Voltage Readings of SIMO Boost converter with variation in

Duty Cycle of switch D1 is shown with V_{in} both at $15V$ and at $10V$and load resistances as 25Ω. Here, The duty cycles for D1 is varied from 0.3 to 0.7 , whereas D4 is kept constant at 0.6. With reference of the reading , figure 7.1 is being plotted and variation is depicted on graph.

Table 7.3: Readings of converter with respect to Duty cycle variation

V_{in} **(V)**	D_1	D_4	V_o **readings of converter (V)**	V_{o2} **(V)**
15	0.30	0.6	23.5	13.6
15	0.35	0.6	26.0	14.1
15	0.45	0.6	28.4	14.2
15	0.55	0.6	32.4	15.6
15	0.65	0.6	39.2	19.0
15	0.70	0.6	44.0	21.0
10	0.30	0.6	12.1	6.2
10	0.40	0.6	15.2	7.0
10	0.50	0.6	19.6	9.40
10	0.60	0.6	23.4	11.3
10	0.70	0.6	32.0	15.6

The settling time as nominal $15V$ input voltage is $10ms$. The results as shown in Table I verifies our digital controlled SIMO Boost converter at frequency $=50kHz$ and $V_{in} = 15V$ and load resistances as 25Ω. It depicts the ADC readings of scaled output measured by DSP result register following the V_{ref} respectively by regulating the duty ratio D1 and V_o of converter. V_o of converter is also being compared to simulation results in this table. Slight variation in Duty ratio D1 observed from CRO and command given from DSP is also highlighted in this table. However, the output voltage and inductor current ripple with ripple as 1% is verified successfully with figures 7.3.

In Table 7.4, the input Voltage is varied from $3.0V - 15.8V$ and average output voltage of subtractor, optocoupler and inductor current (A) is obtained a varying from $0.47A$ to $3V$. This variation can be seen in graph plot as Figure 7.2.

In figure 7.10, voltage output of Low pass filter is showing removal of high frequency components from the regular output voltage. The peak to peak ripple value of waveform in blue is shown as a output of LPF hvaing a valus of $0.8mV$ and average value as $2.85V$.

7.0.1 Simulation results of SIMO Boost with PI and Fuzzy controller

In figures 7.18- 7.20, ADC reading monitored from the Code composer window is shown with references varying from $1.5V - 1.9V$.

From Table 7.5 , it is observed that the simulation results and the hardware results of the V_o of converter are approximately same and also better transient responses are

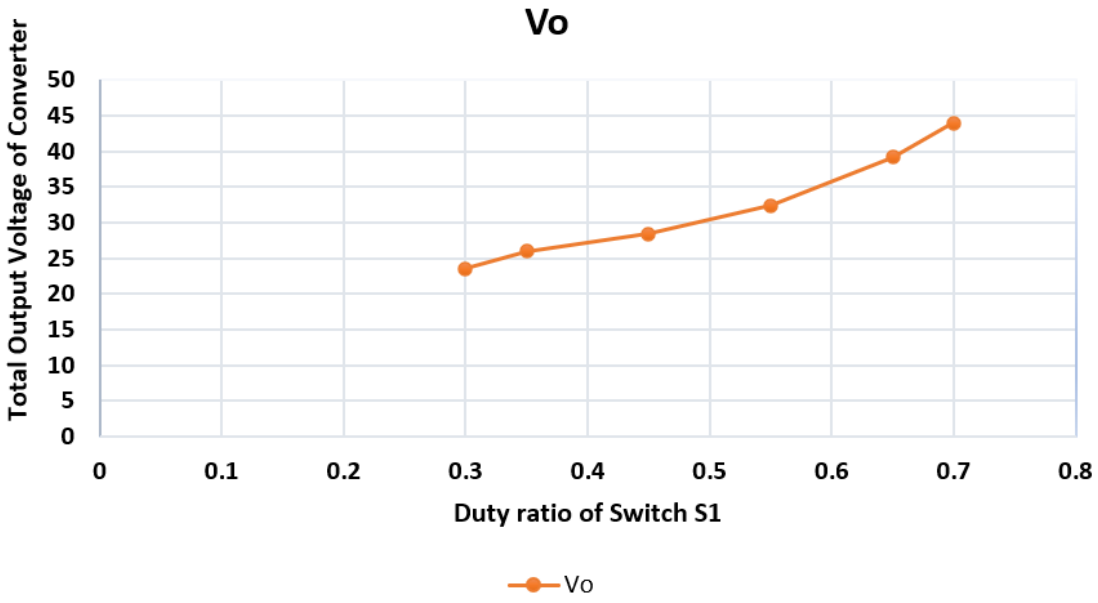


Figure 7.1: Output Voltage with duty cycle variation

Table 7.4: Readings of converter with respect to Input voltage variation

$I_L(A)$	V_{in} **(V) converter**	**Avg.** V_o **of Subtracter (V)**	**Avg.** V_{o2} **from Optocoupler (V)**	**Max.** V_{o2} **from Optocoupler(V)**	**Avg.** V_{o2} **from LPF(V)**
0.47	3	7.76	0	0.17	0
0.65	4	10.5	0.5	0	0
0.86	5	13.4	1.14	0.5	0.05
1.09	6	16.3	2.4	0.73	0.133
1.31	7	19.5	3.53	1.13	0.38
1.55	8	22.71	4.6	1.62	0.67
1.8	9	25.8	5.71	2.1	0.94
2.05	10	29	6.8	2.42	1.24
2.1	10.5	31	7.44	2.9	1.41
2.12	11.0	33.4	8.3	3.46	1.74
2.2	11.5	35	8.9	3.5	1.90
2.26	12	36.5	9.4	3.9	2.01
2.28	12.5	37.9	9.8	4.0	2.14
2.31	13	39.3	10.3	4	2.24
2.40	13.5	41.2	10.8	4.47	2.33
2.42	14.0	43.1	11.35	5.19	2.43
2.45	14.5	44.8	11.76	5.51	2.49
2.49	15.0	47.0	12.24	5.31	2.52
2.89	15.5	48.3	12.59	5.8	2.58
3.00	15.8	50	12.8	5.8	2.55

achieved with non-linear Sugeno-fuzzy controller. Output voltage and input current waveformes for transient and steady state condition are shown in figures 7.24 - 7.26.

In figure 7.24- 7.26, the last waveform shows the inductor current with 1% ripple

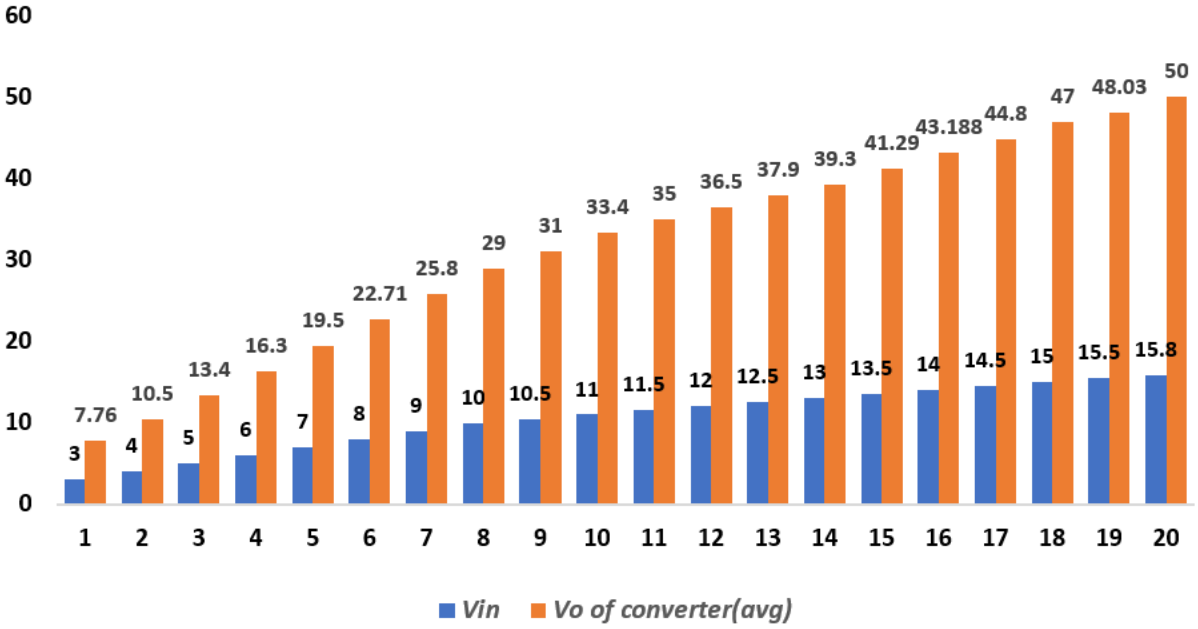


Figure 7.2: Output voltage variation w.r.t Input voltage variation

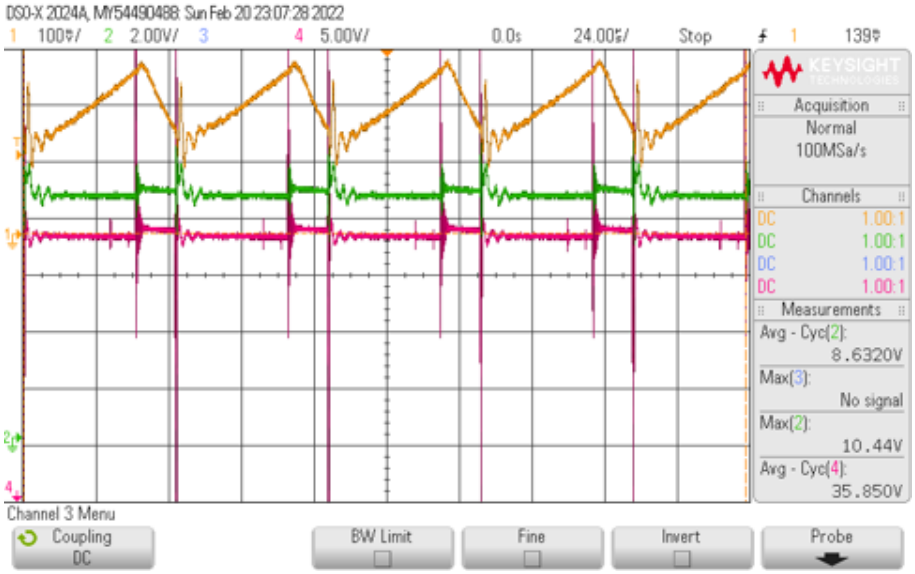


Figure 7.3: Total output voltage, V_{o1} and inductor current at 50 kHz

Table 7.5: Reading of Closed loop control of converter using Fuzzy controller

ADC reading (mV)	V_{ref} (mV)	**Total V_o of simulation(V)**	**V_o of converter(V)**	I_{in} **(A)**	D_1 **of CRO**
1452	1500	27	28	1.20	0.32
1501	1600	31	30	1.52	0.36
1790	1800	34	33	2.01	0.45
2005	2000	37	38	2.04	0.60

and output voltage with pulses in OFF stage of S1 switch , with ripple content of 1%

Figure 7.4: Output current, both output voltages of converter and pulses given to S1

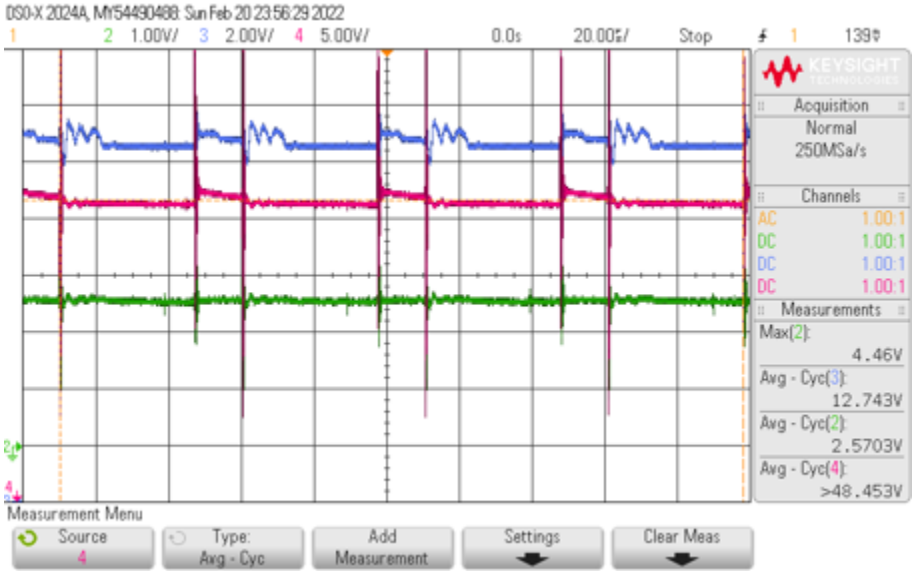


Figure 7.5: Total output, voltage sensor output and ADC sensed voltage (LPF output)

approximately is observed. The pulse generated by Fuzzy controller of duty ratio 0.6 is given to switches.

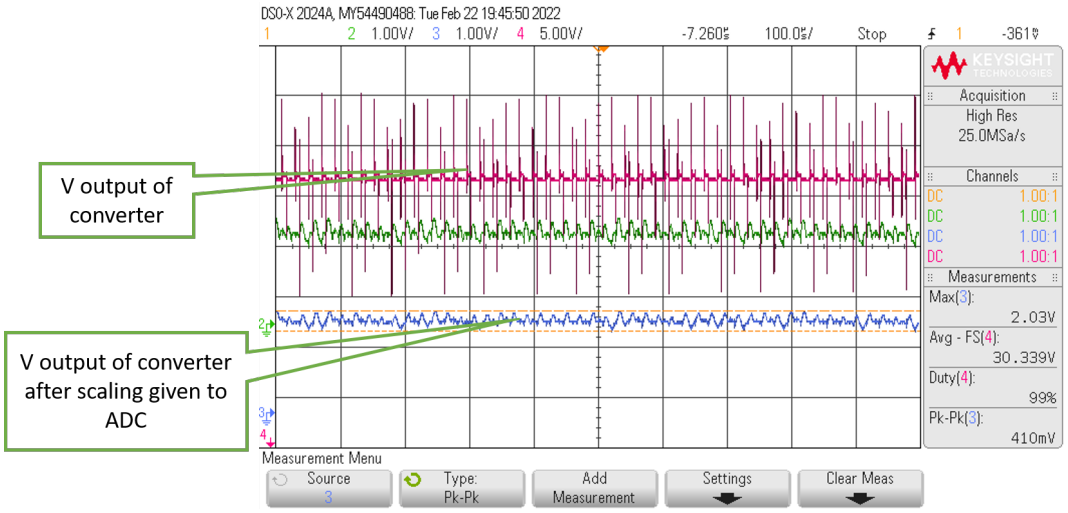


Figure 7.6: Total Voltage output of a converter and scaled Output voltage

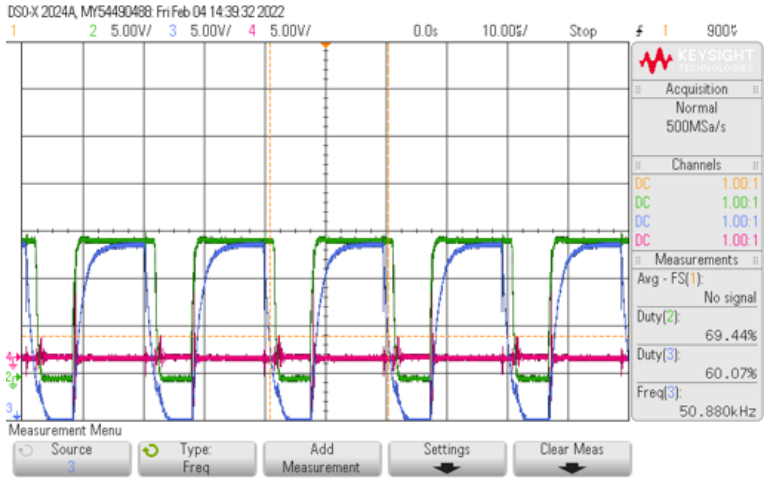


Figure 7.7: PWM pulse at DSP output, PWM pulse at Optocoupler output (includes delay at high frequency) at 50 kHz

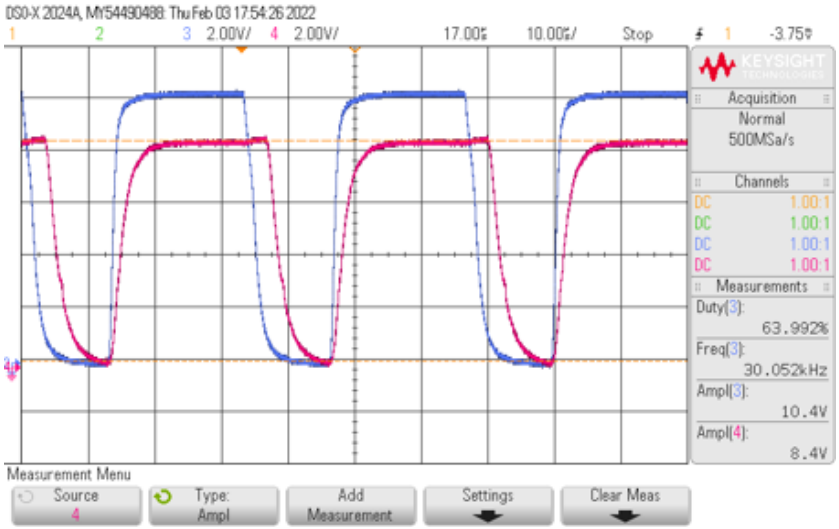


Figure 7.8: PWM Pulse of S1 and S4 at 30 kHz

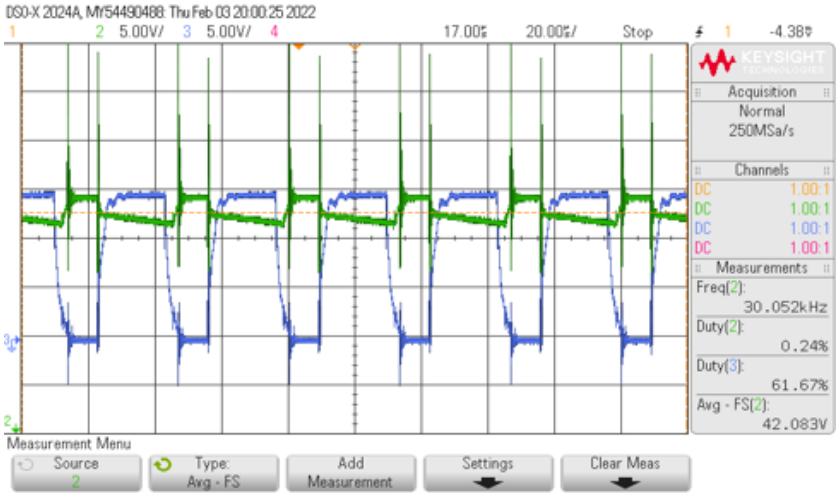


Figure 7.9: Output voltage at 30kHz frequency

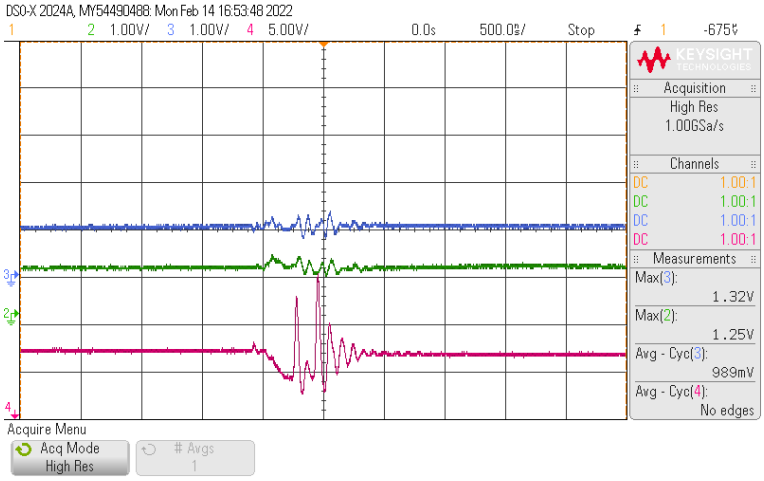


Figure 7.10: Removal of Ripples and noise using LPF

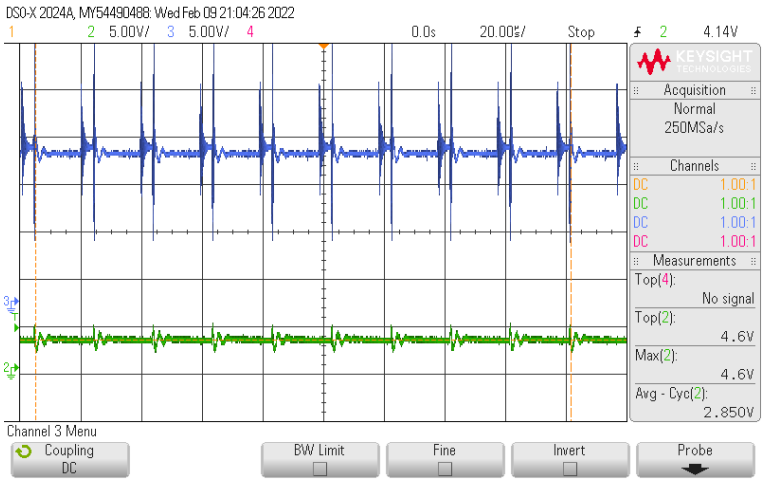


Figure 7.11: Total voltage output of converter and LPF output

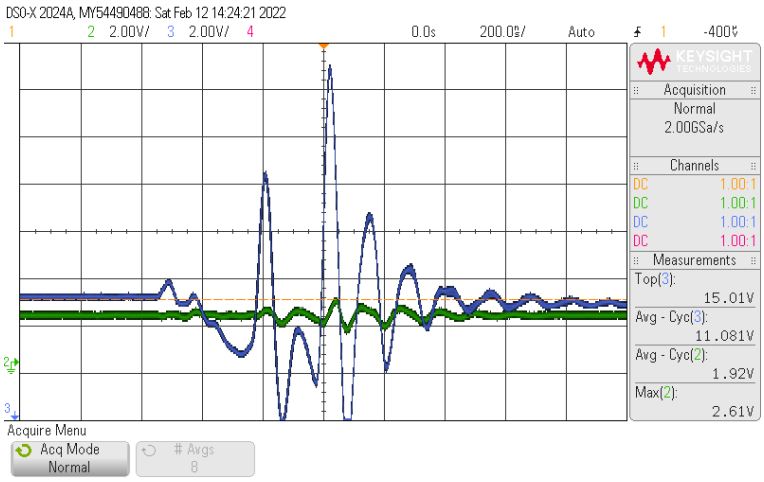


Figure 7.12: Scaled output using sensor circuit

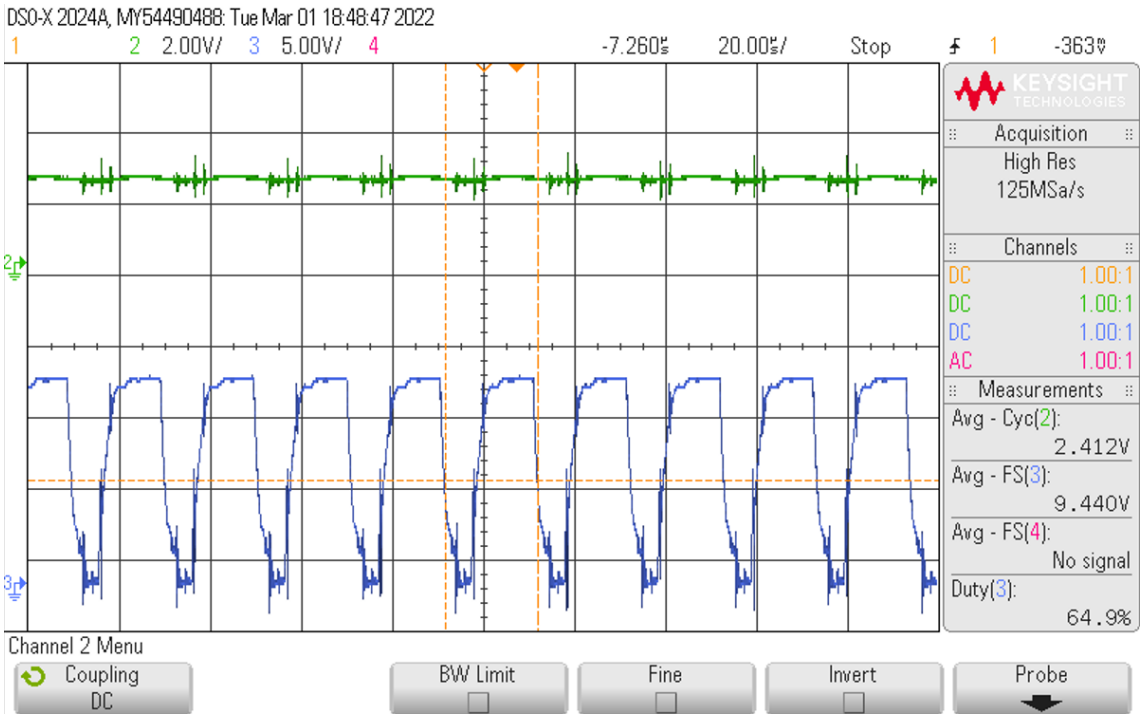


Figure 7.13: Output Voltage (Scaled) of Converter and Pulses given by controller in Closed loop control (V ref as 2V) for SIMO Boost converter

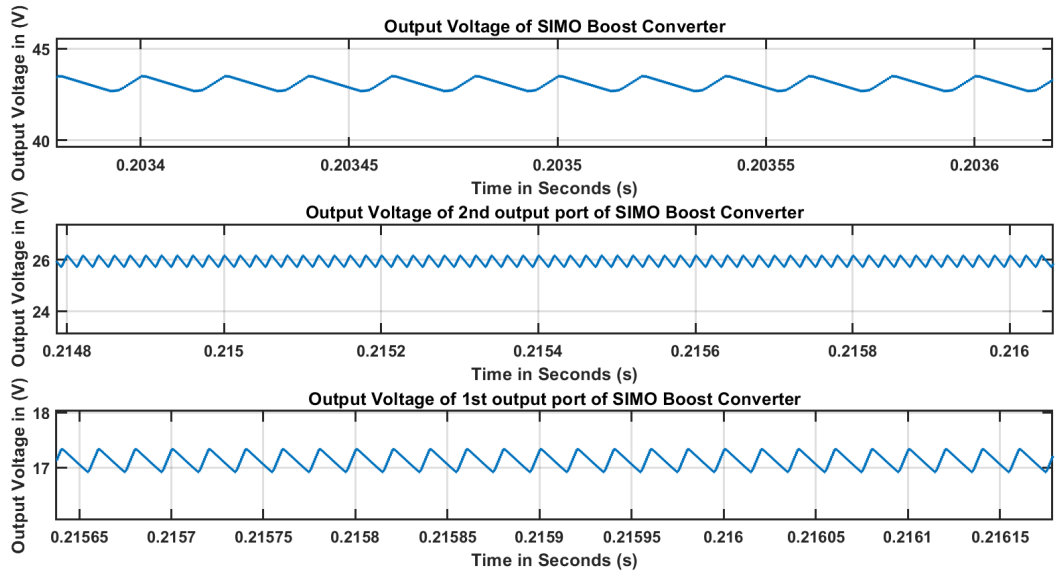


Figure 7.14: Output voltage (total), and output voltage at both the output ports for PI control for SIMO Boost converter

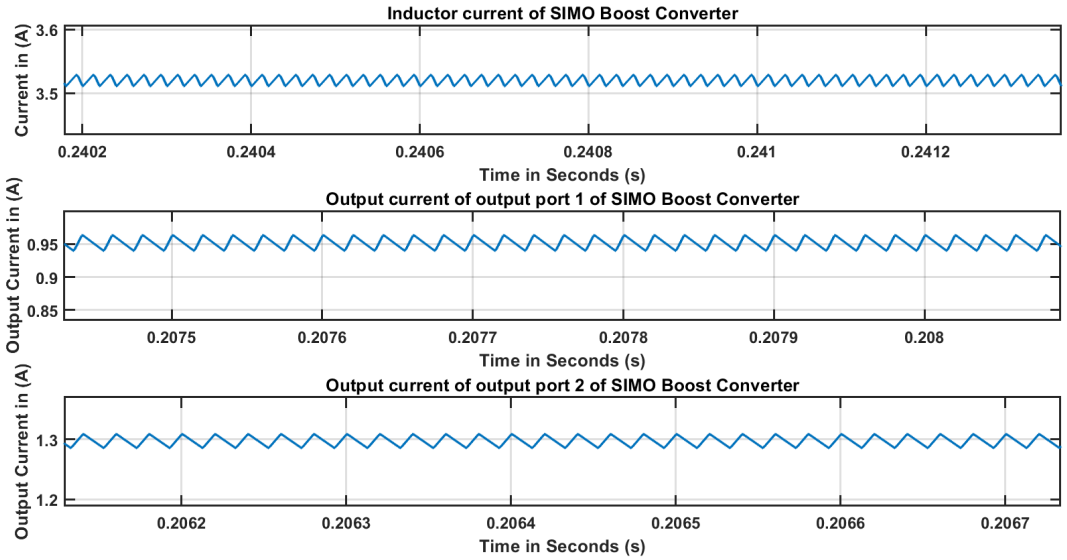


Figure 7.15: Inductor current, Output current for both the output ports for PI control for SIMO Boost converter

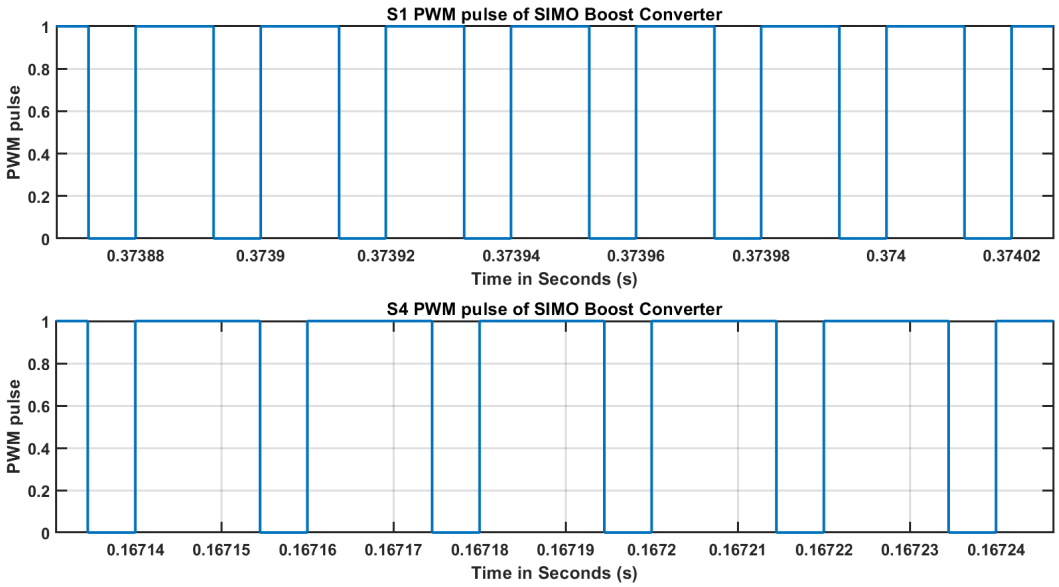


Figure 7.16: Pulses for both the switches S1 and S4 for PI control for SIMO Boost converter

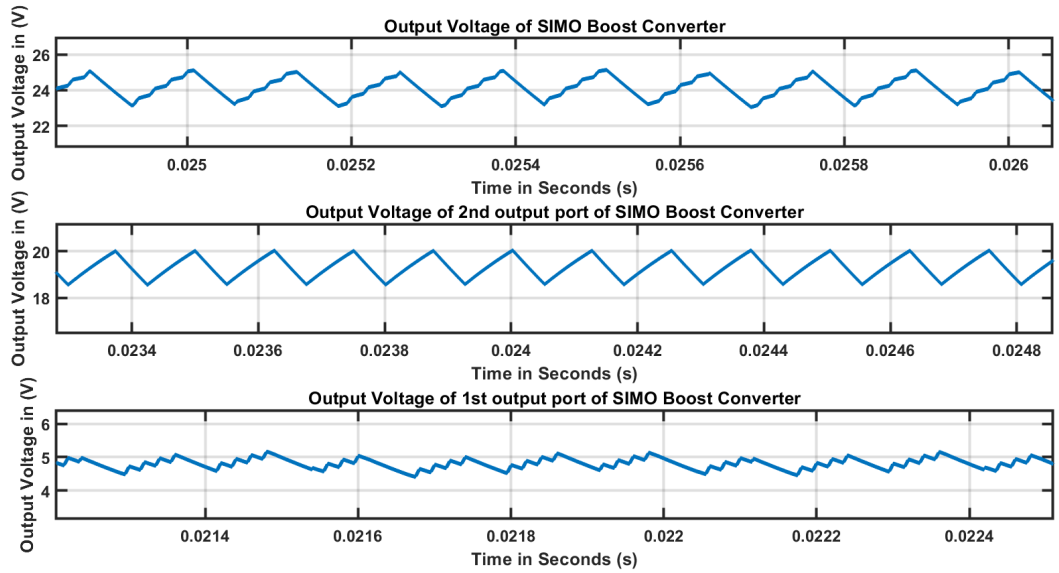


Figure 7.17: Total output voltage, Output voltages for both the output ports with fuzzy control for SIMO Boost converter

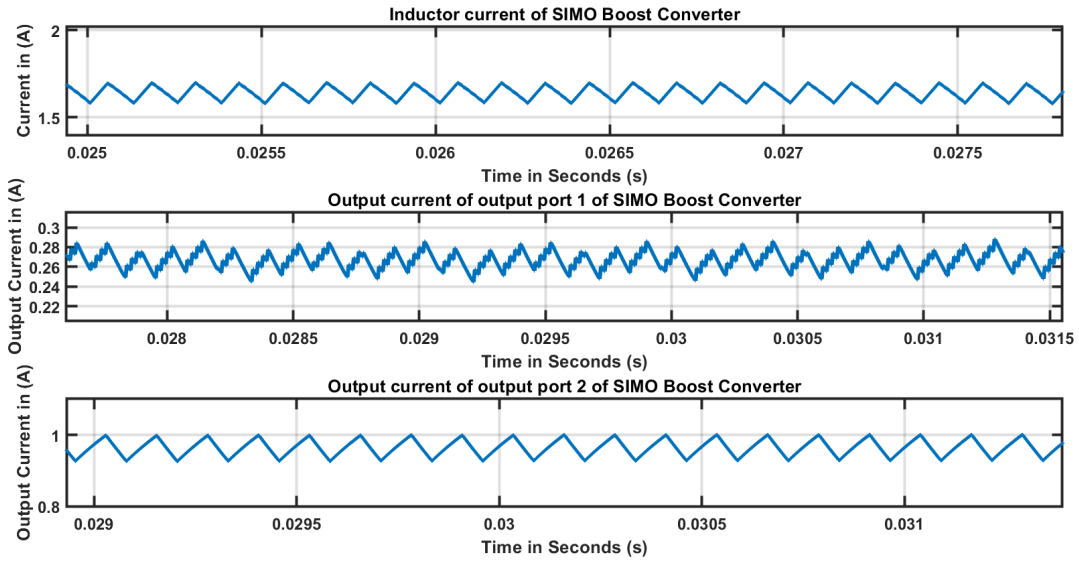


Figure 7.18: Inductor current, Output current for both the output ports with fuzzy control for SIMO Boost converter

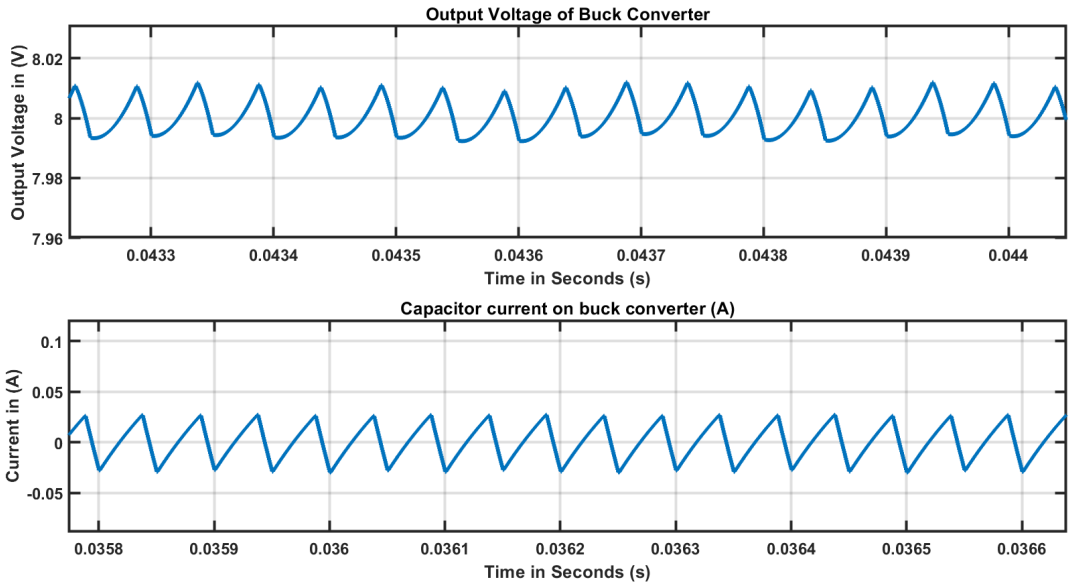


Figure 7.19: Output voltage and Capacitor current in Buck converter with PI control

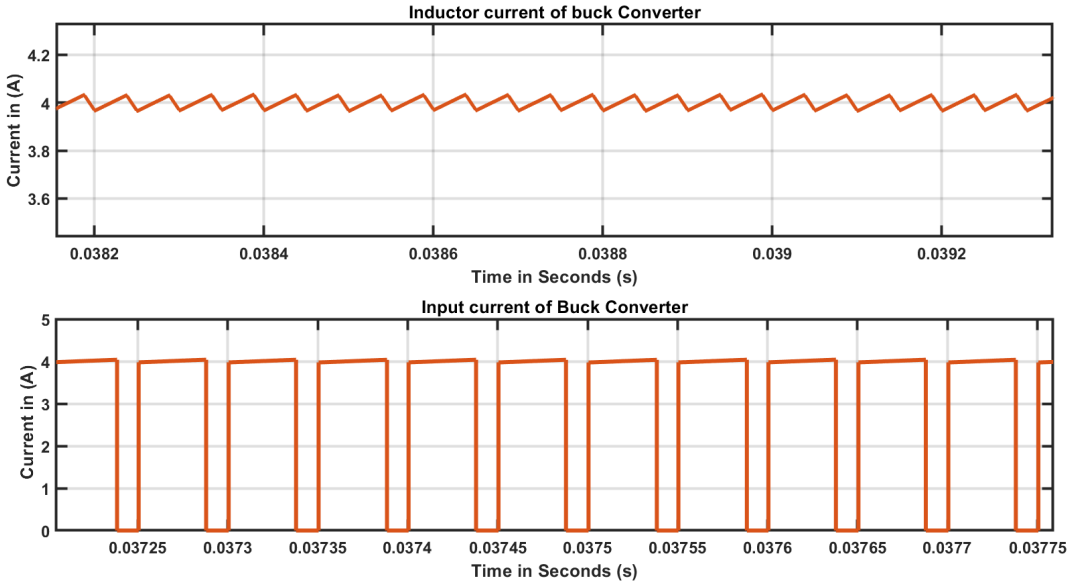


Figure 7.20: Inductor current and Input current of buck converter with PI control

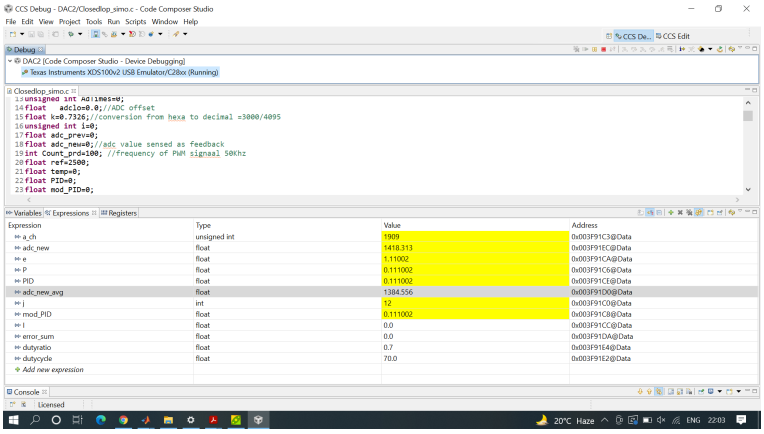


Figure 7.21: Closed loop control using output voltage reference as 1.9V

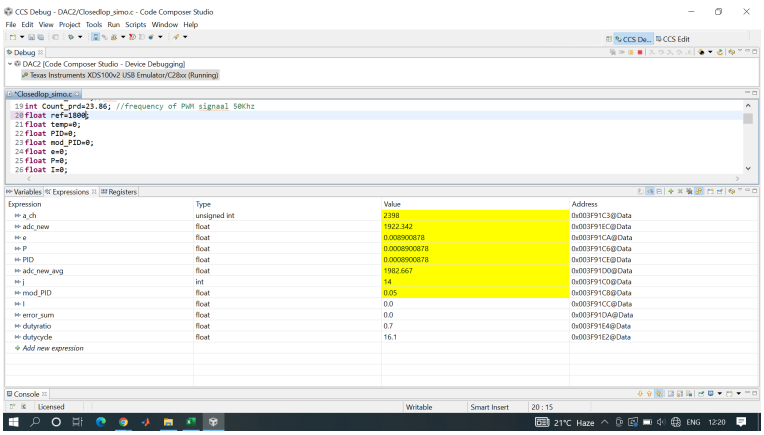


Figure 7.22: Closed loop control using output voltage reference as 1.8V

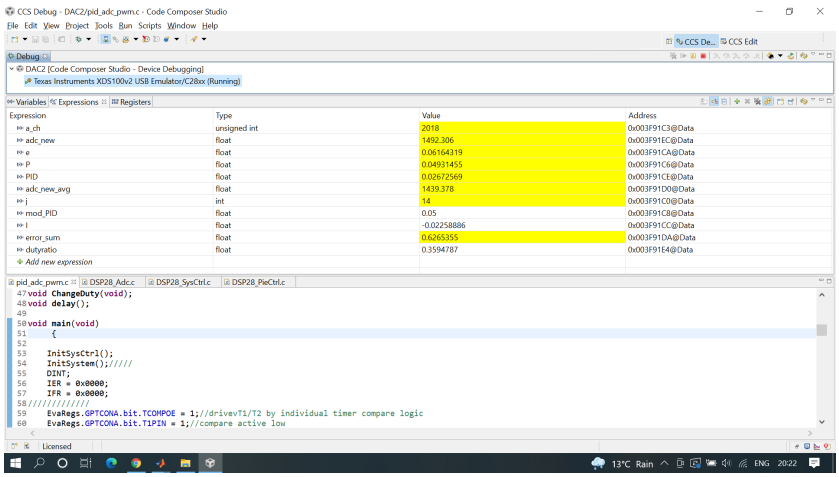


Figure 7.23: Closed loop control using output voltage reference as 1.5V

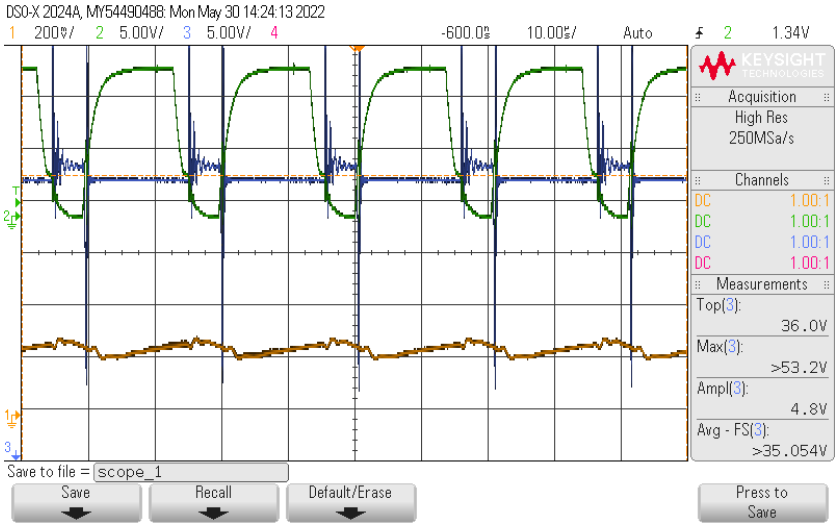


Figure 7.24: Closed loop control of SIMO boost using Fuzzy controller with Vref as 2 V

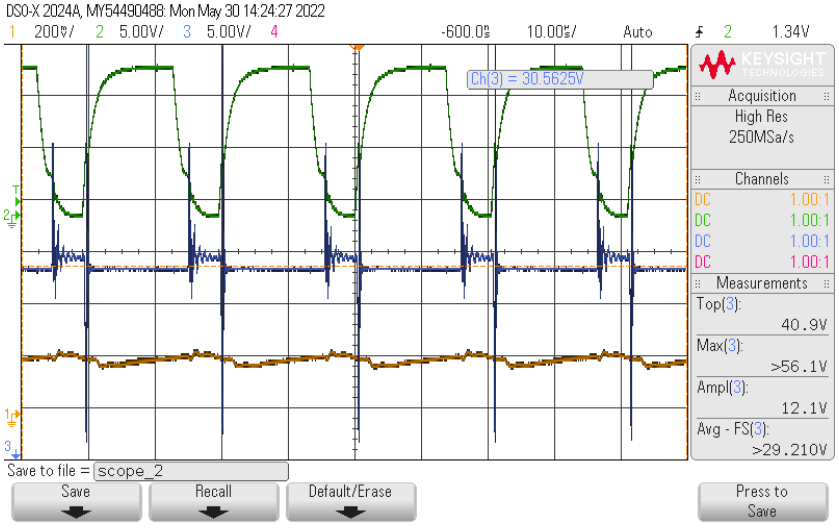


Figure 7.25: Closed loop control of SIMO boost using Fuzzy controller with Vref as 1.8 V

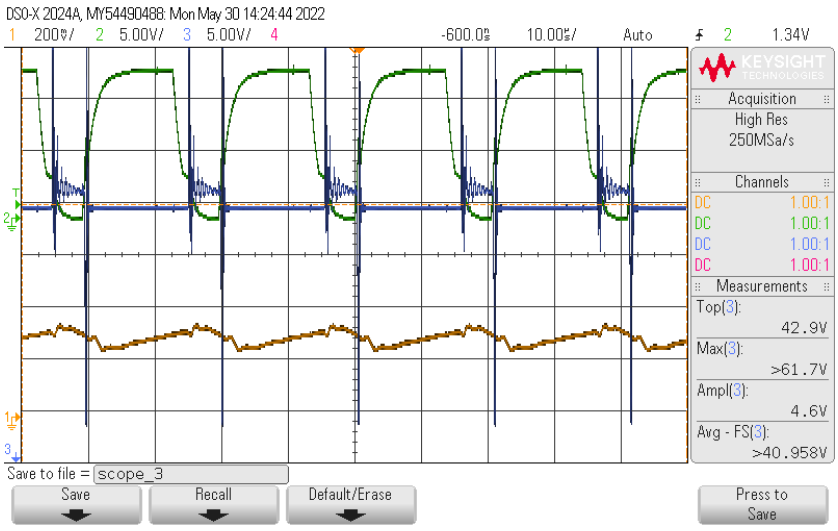


Figure 7.26: Closed loop control of SIMO boost using Fuzzy controller with Vref as 2.5 V

Chapter 8

CONCLUSION AND FUTURE SCOPE

This paper discusses Design, Analysis, Modelling and Implementation of digital control loop for DC-DC SIMO Boost converter based on Linear and Non-linear controllers on TMS320F2812 DSP. The boost converter tends to offer restrictions over voltage control mode operation because of Right-half-plane (RHP). While having major constraints on the design of loop compensation and crossover frequency , this Tuning of controller can be managed using appropriate hardware tuning methods such as Zeigner Nichol's, Cohen coon and Good gain Methods. However, using pole placement methods with several rules RHPZ can be stabilized and suitable control is achieved in this thesis.

In this chapter, the RHPZ frequency is understood and placed properly for better control of output voltage of converter. The converter was interfaced with a DSP controller of associated parameters for digital PI and Fuzzy (Sugeno method) controller design. The design by emulation method allows to convert designed controller design to discrete controller. For time variant boost converter topology, the exact discrete time model is also obtained via Tustin method with total loop delay taken into consideration for effective analysis. Indirect controller design is found to be better than direct controller design approach. Then, the detailed implementation of controller design is presented using TMS320F2812 DSP. Various issues in Digital control design such as Quantization, limit cycles and sampling effects are also analysed and discussed in this thesis. The MATLAB simulation results for digitally controlled converter are verified using hardware prototype of boost converter and satisfactory transient and steady state responses are received for 45W, 15V, 3A output boost converter and 18W, 12V, 1.5A for Buck converter.

This converter work shall be extended while using Wide band gap based devices such as SiC and GaN based devices for fast switching and low ON state resistances. Also, FPGA processors shall be used to avoid computational delays and fast processing speed. In future scope, non-linear controller called as Model Predictive control and other adaptive controllers are also proposed for controlling DC-DC controllers.

Chapter 9

PUBLICATIONS

1) V. Jindal and D. Joshi, "A Comparative analysis of classical Tuning methods of PI controllers on non-ideal Buck Converter," 2022 2nd International Conference on Power Electronics IoT Applications in Renewable Energy and its Control (PARC), 2022, pp. 1-5, doi: 10.1109/PARC52418.2022.9726251.

2) V. Jindal and D. Joshi, 2022, 'Analysis, Modelling and Design of DSP TMS320F2812 based Digital PI controller for DC-DC Buck converter', in Advanced Power Electronics Converters for Future Renewable Energy Systems, CRC Press, Taylor Francis.

Appendix A

APPENDIX A

Table A.1: BUCK CONVERTER DESIGN PARAMETERS

Parameters	**Values**
$Inputvoltage, V_{in}$	$12V - 16V$
$Loadresistance, R$	2Ω
$OutputVoltage, V_{out}$	$6V$
$Inductance, L/r_L$	$1.8mH/0.18\Omega$
$Capacitance, C/r_c$	$47\mu F/0.3\Omega$
$Frequency, f$	$20Khz$
$Switch - onresistance, r_{sw}$	0.044Ω
$Diodeforwardresistance, r_d$	0.024Ω
$Diodeforwardvoltagedrop, V_d$	$0.7V$

Table A.2: Parameters of SIMO converter

Parameters	Values
Input voltage, Vin	$15V$
Load resistances, R_1, R_2	$18\Omega, 25\Omega$
Output voltage	$45V$
Inductance, L/r_L	$6mH/0.18\Omega$
Capacitance, C1, C2/r_C	$30/0.3\Omega$
Frequency, f	$50kHz$
Switch- on resistance, r_{sw}	0.044Ω
Diode forward resistance, r_d	0.024Ω
Diode forward Voltage drop, V_d	$0.7V$

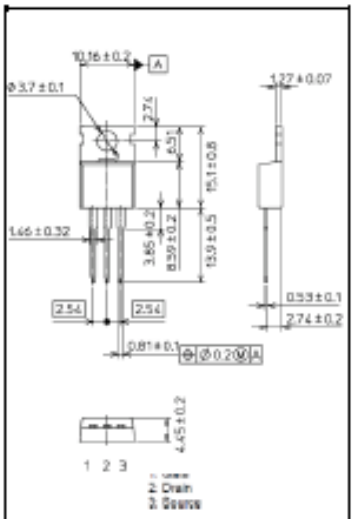
TOSHIBA Field Effect Transistor Silicon N-Channel MOS Type (U-MOSⅧ-H)

TK100E10N1

Switching Regulator Applications

- Low drain-source on-resistance:
  $R_{DS(ON)}$ = 2.8 mΩ (typ.) (V_{GS} = 10 V)
- Low leakage current: I_{DSS} = 10 μA (max) (V_{DS} = 100 V)
- Enhancement mode: V_{th} = 2.0 to 4.0 V (V_{DS} = 10 V, I_D = 1.0 mA)

Unit: mm



JEDEC	—
JEITA	—
TOSHIBA	2-10X1A

Weight: 1.93 g (typ.)

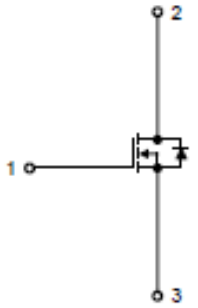
Absolute Maximum Ratings (Ta = 25°C)

Characteristic		Symbol	Rating	Unit
Drain-source voltage		V_{DSS}	100	V
Gate-source voltage		V_{GSS}	±20	V
Drain current	DC(Silicon limit)(Note 1,2)	I_D	207	A
	DC(Note 1,3)	I_D	100	
	Pulsed(t=1ms)(Note 1)	I_{DP}	434	
Drain power dissipation (T_c = 25°C)		P_D	255	W
Single-pulse avalanche energy (Note 4)		E_{AS}	222	mJ
Avalanche current		I_{AR}	100	A
Channel temperature		T_{ch}	150	°C
Storage temperature range		T_{stg}	−55 to 150	°C

Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings. Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Thermal Characteristics

Characteristic	Symbol	Max	Unit
Thermal resistance, channel to case	$R_{th(ch-c)}$	0.49	°C/W
Thermal resistance, channel to ambient	$R_{th(ch-a)}$	83.3	°C/W



Note 1: Ensure that the channel temperature does not exceed 150°C.

Note 2: Limited by silicon chip capability. Package limit is 100A.

Note 3: Device mounted with heatsink so that Rth(ch-a)=2.77°C/W.

Note 4: V_{DD} = 80 V, T_{ch} = 25°C (initial), L = 17.1 μH, R_G = 1.2 Ω, I_{AR} = 100 A

This transistor is an electrostatic-sensitive device.
Please handle with caution.

Figure A.1: Rating of MOSFET TK100E10N1

Electrical Characteristics (Ta = 25°C)

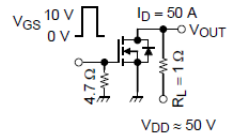
Characteristic		Symbol	Test Condition	Min	Typ.	Max	Unit
Gate leakage current		I_{GSS}	V_{GS} = ±20 V, V_{DS} = 0 V	—	—	±0.1	μA
Drain cutoff current		I_{DSS}	V_{DS} = 100 V, V_{GS} = 0 V	—	—	10	μA
Drain-source breakdown voltage		$V_{(BR)DSS}$	I_D = 10 mA, V_{GS} = 0 V	100	—	—	V
		$V_{(BR)DSX}$	I_D = 10 mA, V_{GS} = −20 V (Note 5)	65	—	—	
Gate threshold voltage		V_{th}	V_{DS} = 10 V, I_D = 1.0 mA	2.0	—	4.0	V
Drain-source on-resistance		$R_{DS(ON)}$	V_{GS} = 10 V, I_D = 50 A	—	2.8	3.4	mΩ
Input capacitance		C_{iss}	V_{DS} = 50 V, V_{GS} = 0 V, f = 1 MHz	—	8800	—	pF
Reverse transfer capacitance		C_{rss}		—	63	—	
Output capacitance		C_{oss}		—	1500	—	
Gate resistance		rg		—	2.6	—	Ω
Switching time	Rise time	t_r		—	32	—	ns
	Turn-on time	t_{on}		—	59	—	
	Fall time	t_f		—	45	—	
	Turn-off time	t_{off}		—	140	—	
Total gate charge (gate-source plus gate-drain)		Q_g	V_{DD} ≈ 80 V, V_{GS} = 10 V, I_D = 100 A	—	140	—	nC
Gate-source charge 1		Q_{gs1}		—	46	—	
Gate-drain (“Miller”) charge		Q_{gd}		—	34	—	
Gate switch charge		Q_{SW}		—	55	—	

Figure A.2: Electrical Characteristics of MOSFET-TK100E10N1

Source−Drain Ratings and Characteristics (Ta = 25°C)

Characteristics	Symbol	Test Condition	Min	Typ.	Max	Unit
Continuous drain reverse current (Note 1)	I_{DR}	—	—	—	100	A
Pulse drain reverse current (Note 1)	I_{DRP}	—	—	—	434	A
Forward voltage (diode)	V_{DSF}	I_{DR} = 100 A, V_{GS} = 0 V	—	—	−1.2	V
Reverse recovery time(Note 6)	t_{rr}	I_{DR} = 100 A, V_{GS} = 0 V, $-dI_{DR}/dt$ = 100 A / μs	—	93	—	ns
Reverse recovery charge(Note 6)	Q_{rr}		—	220	—	nC

Figure A.3: Source drain ratings of MOSFET

8. Absolute Maximum Ratings (Note) (Unless otherwise specified, T_a = 25 °C)

	Characteristics		Symbol	Note	Rating	Unit
LED	Input forward current		I_F		20	mA
	Input forward current derating	(T_a ≥ 116 °C)	$\Delta I_F/\Delta T_a$		-0.6	mA/°C
	Peak transient input forward current		I_{FPT}	(Note 1)	1	A
	Peak transient input forward current derating	(T_a ≥ 110 °C)	$\Delta I_{FPT}/\Delta T_a$		-25	mA/°C
	Input reverse voltage		V_R		5	V
	Input power dissipation		P_D		40	mW
	Input power dissipation derating	(T_a ≥ 110 °C)	$\Delta P_D/\Delta T_a$		-1.0	mW/°C
Detector	Peak high-level output current	(T_a = -40 to 125 °C)	I_{OPH}	(Note 2)	-2.5	A
	Peak low-level output current	(T_a = -40 to 125 °C)	I_{OPL}	(Note 2)	+2.5	
	Output voltage		V_O		35	V
	Supply voltage		V_{CC}		35	
	Output power dissipation		P_O		260	mW
	Output power dissipation derating	(T_a ≥ 110 °C)	$\Delta P_O/\Delta T_a$		-6.5	mW/°C
Common	Operating temperature		T_{opr}		-40 to 125	°C
	Storage temperature		T_{stg}		-55 to 150	
	Lead soldering temperature	(10 s)	T_{sol}	(Note 3)	260	
	Isolation voltage	AC, 60 s, R.H. ≤ 60 %	BV_S	(Note 4)	3750	Vrms

Figure A.4: Absolute maximum ratings of TLP350H

12. Switching Characteristics (Note)
(Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Propagation delay time (L/H)	t_{pLH}	(Note 1)	Fig. 13.1.7	I_F = 0 → 5 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	50	—	500	ns
Propagation delay time (H/L)	t_{pHL}	(Note 1)		I_F = 5 → 0 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	50	—	500	
Pulse width distortion	$\lvert t_{pHL}-t_{pLH}\rvert$	(Note 1)		I_F = 0 ⟷ 5 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	—	—	350	
Rise time	t_r	(Note 1)		I_F = 0 → 5 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	—	15	—	
Fall time	t_f	(Note 1)		I_F = 5 → 0 mA, V_{CC} = 30 V, R_g = 20 Ω, C_g = 10 nF	—	8	—	
Common-mode transient immunity at output high	CM_H	(Note 2)	Fig. 13.1.8	V_{CM} = 1000 V_{p-p}, I_F = 5 mA, V_{CC} = 30 V, T_a = 25 °C, $V_{O(min)}$ = 26 V	±20	±25	—	kV/μs
Common-mode transient immunity at output low	CM_L	(Note 3)		V_{CM} = 1000 V_{p-p}, I_F = 0 mA, V_{CC} = 30 V, T_a = 25 °C, $V_{O(max)}$ = 1 V	±20	±25	—	

Note: All typical values are at T_a = 25 °C.
Note 1: Input signal (f = 25 kHz, duty = 50 %, t_r = t_f = 5 ns or less).
C_L is approximately 15 pF which includes probe and stray wiring capacitance.
Note 2: CM_H is the maximum rate of rise of the common mode voltage that can be sustained with the output voltage in the logic high state (V_O > 26 V).
Note 3: CM_L is the maximum rate of fall of the common mode voltage that can be sustained with the output voltage in the logic low state (V_O < 1 V).

Figure A.5: Switching characteristics of TLP350H

10. Electrical Characteristics (Note)
(Unless otherwise specified, T_a = -40 to 125 °C)

Characteristics	Symbol	Note	Test Circuit	Test Condition	Min	Typ.	Max	Unit
Input forward voltage	V_F			I_F = 10 mA, T_a = 25 °C	1.4	1.55	1.7	V
Input forward voltage temperature coefficient	$\Delta V_F/\Delta T_a$			I_F = 10 mA	—	-2.0	—	mV/°C
Input reverse current	I_R			V_R = 5 V, T_a = 25 °C	—	—	10	μA
Input capacitance	C_t			V = 0 V, f = 1 MHz, T_a = 25 °C	—	95	—	pF
Peak high-level output current	I_{OPH}	(Note 1)	Fig. 13.1.1	I_F = 5 mA, V_{CC} = 30 V, V_{8-6} = -3.5 V	—	-1.6	-1.0	A
				I_F = 5 mA, V_{CC} = 15 V, V_{8-6} = -7.0 V	—	—	-2.0	
Peak low-level output current	I_{OPL}	(Note 1)	Fig. 13.1.2	I_F = 0 mA, V_{CC} = 30 V, V_{6-5} = 2.5 V	1.0	1.6	—	
				I_F = 0 mA, V_{CC} = 15 V, V_{6-5} = 7.0 V	2.0	—	—	
High-level output voltage	V_{OH}		Fig. 13.1.3	I_F = 5 mA, R_L = 200 Ω, V_{CC1} = +15 V, V_{EE1} = -15 V	11.0	13.7	—	V
Low-level output voltage	V_{OL}		Fig. 13.1.4	V_F = 0.8 V, R_L = 200 Ω, V_{CC1} = +15 V, V_{EE1} = -15 V	—	-14.9	-12.5	
High-level supply current	I_{CCH}		Fig. 13.1.5	I_F = 10 mA, V_{CC} = 30 V, V_O = Open	—	1.5	3.0	mA
Low-level supply current	I_{CCL}		Fig. 13.1.6	I_F = 0 mA, V_{CC} = 30 V, V_O = Open	—	1.5	3.0	
Threshold input current (L/H)	I_{FLH}			V_{CC} = 15 V, V_O > 1 V	—	1.0	5	
Threshold input voltage (H/L)	V_{FHL}			V_{CC} = 15 V, V_O < 1 V	0.8	—	—	V
Supply voltage	V_{CC}			—	15	—	30	
UVLO threshold voltage	V_{UVLO+}			I_F = 5 mA , V_O > 2.5 V	11.0	12.5	13.5	
	V_{UVLO-}			I_F = 5 mA, V_O < 2.5 V	9.5	11.0	12.0	
UVLO hysteresis	$UVLO_{HYS}$			—	—	1.5	—	

Figure A.6: Electrical Characteristics of TLP350H

Appendix B

APPENDIX B

B.1 Code of control of SIMO boost converter

```
include"DSP28_Device.h"
// Inititalization of parameters

    unsigned int a_ch=0;
float dutycycle=0;
float dutyratio=0.25;
unsigned int AdTimes=0;
float adclo=0.0;//ADC offset
float k=0.7326;
unsigned int i=0;
float adc_prev=0;
float adc_new=0;//adc value sensed as feedback
int Count_prd=23.3;//frequency of PWM signal 50kHz
float ref=1800;
float temp=0;
float PID=0;
float mod_PID=0;
float e=0;
float P=0;
float I=0;
float D=0;
float d=0;
float ek=0;
int j=0;
int ii=0;
float adc_new_sum=0;
float adc_new_avg=0;
float adc_val[10];
float error[10];
float error_sum=0;
float error_new_sum=0;

    // Prototype statements for functions found within this file.
```

```
    interrupt void ad(void);
void InitSystem(void);
void ChangeDuty(void);
void delay();

    void main(void)
{ // Initialize System Control registers, PLL, WatchDog, Clocks to default state

    InitSysCtrl();
InitSystem();

    // Disable and clear all CPU interrupts:
DINT;
IER = 0x0000;
IFR = 0x0000;

    //drive T1/T2 by individual timer compare logic (Compare Output Enable)

    EvaRegs.GPTCONA.bit.TCOMPOE = 1;

    //compare active low
EvaRegs.GPTCONA.bit.T1PIN = 1;
EvaRegs.GPTCONA.bit.T2PIN = 1;

    // For register "T1CON" set
// The "TMODE"-field to "counting up mode";
// Field "TPS" to "divide by 128";
// Bit "TENABLE" to "disable timer" (we will enable it later)
// Field "TCLKS" to "internal clock"
// Field "TCLD" to "reload on underflow" and
// Bit "TECMPR" to "enable compare operation"

    EvaRegs.T1CON.all = 0x1602; //0001 0110 0000 0010//
EvaRegs.T2CON.all = 0x1602;

    //0 Period register select
// 1 Timer compare enable
//3:2 Timer compare register reload
//5:4 Clock source select
//6 Timer enable
//7 Start GP timer 2 with GP timer 1's enable
//10:8 Input clock pre-scaler
//12:11 Count mode selection
// 13 reserved
//14 Free emulation control
//15 Soft emulation control

    //setup the timer for a sample period
```

```
EvaRegs.T1PR =Count_prd;
EvaRegs.T2PR =Count_prd;
EvaRegs.T1CMPR = EvaRegs.T1PR*.60;//S1
EvaRegs.T2CMPR = EvaRegs.T1PR*.71;//S4
EvaRegs.T2CON.bit.TENABLE = 1;

    // Initialize Pie Control Registers To Default State:
InitPieCtrl();

    // Initialize the PIE Vector Table To a Known State:
InitPieVectTable();

    //initialising General input output ports
InitGpio();
    EALLOW;// protected registers
PieVectTable.ADCINT=ad;

    // to change the GPIO multiplex status; we need T1PWM as signal at the pin. modifying the multiplex register setup

    GpioMuxRegs.GPAMUX.bit.T1PWM_GPIOA6 = 1;
GpioMuxRegs.GPAMUX.bit.T2PWM_GPIOA7 = 1;
GpioMuxRegs.GPADIR.bit.GPIOA6 =0;
GpioMuxRegs.GPADIR.bit.GPIOA7 =0;

    EDIS; // This is needed to disable write to EALLOW
//protected registers

    InitAdc(0,0);// basic ADC initialization:

    IER= M_INT1;
IER= M_INT14;

    EINT; // Enable Global interrupt INTM

    ERTM; // Enable Global real time interrupt

    EvaRegs.T1CON.bit.TENABLE = 1;

    for(;;)
{
KickDog();
e=(ref_ad_new_avg)/1000;//v error
d=e-temp;
//difference in error

    P=0.1×e;
```

```
    //I calc

    if (ii ≤ 10)
{
error[ii]= e;
ii=ii+1;
error_sum=error_sum+e;
I=(0.005*error_sum);
}

    else
{
error_sum=error_sum+error[ii-10]+e;
error[ii-10]=e;
ii++;
if (ii==20) ii=10;
}

    PID=P+I+D;
if (PID≤ 0)
//PuttingsaturationlimitstoPIDvalues

    {
mod_PID=PID* (-1);
}
else
{
mod_PID=PID;
}
if (mod_PID ≥ 0.7)
{
mod_PID = 0.7;
}
if(mod_PID ≤ 0.05)
{
mod_PID = 0.05;
}

    if (mod_PID ≤ 0.7mod_PID ≥ 0.05)
{
ChangeDuty(); }

    temp=e;
}

    }

    interrupt void ad(void)
```

```
{

    //clearing interrupts
IFR=0x0000;

    //Acknowledge PIE Interrupt:
PieCtrl.PIEACK.all=0xFFFF;

    delay();
a_ch=(AdcRegs.RESULT0<<= 4);
//AdcRegs.RESULT0sensedfromADCpin

    adc_new=a_ch*(k);

    // averaging of error:
if (j<= 10)
{
adc_val[j] = adc_new;
adc_new_sum = adc_new_sum + adc_new;
j + +;
adc_new_avg = adc_new_sum/j;
}
else
{
adc_new_sum = adc_new_sum_adc_val[j − 10] + adc_new;
adc_val[j − 10] = adc_new;
adc_new_avg = adc_new_sum/10;
j + +;
if(j == 20)
{j = 10; }
}

    //Clear Interrupt Flag ADC Sequencer 1 (Register ADCST)
AdcRegs.ADC_ST_FLAG.bit.INT_SEQ1_CLR=1
    EINT;
}

    void delay(void)
{
unsigned int abc;
for (abc=0;abc<= 6000; abc + +);
}

    void InitSystem(void)
{
EALLOW;

    //Watchdog - Timer -
```

```
SysCtrlRegs.WDCR= 0x0068;

    //System Control and Status Reg
SysCtrlRegs.SCSR.all = 0;

    //PLL Clock Register
SysCtrlRegs.PLLCR = 10;//A

    //high Speed Clock Prescaler
SysCtrlRegs.HISPCP.all = 0x1;

    //low Speed Clock Prescaler
SysCtrlRegs.LOSPCP.all = 0x2;

    SysCtrlRegs.PCLKCR.bit.EVAENCLK=1;
SysCtrlRegs.PCLKCR.bit.EVBENCLK=1;
SysCtrlRegs.PCLKCR.bit.SCIENCLKA=0;
SysCtrlRegs.PCLKCR.bit.SCIENCLKB=0;
SysCtrlRegs.PCLKCR.bit.MCBSPENCLK=0;
SysCtrlRegs.PCLKCR.bit.SPIENCLK=0;
SysCtrlRegs.PCLKCR.bit.ECANENCLK=0;
SysCtrlRegs.PCLKCR.bit.ADCENCLK=1;
EDIS; }

    void ChangeDuty(void)
{

    dutyratio= dutyratio + PID;
if (dutyratio ≥ 0.7)
{
dutyratio = 0.7;
//For buck converter Duty ratio is 0.1-0.8
}
if(dutyratio ≤ 0.05)
{

    dutyratio=0.05;
}

    dutycycle=EvaRegs.T1PR×(dutyratio);
EvaRegs.T1CMPR = dutycycle;
EvaRegs.T1CON.bit.TENABLE = 1;

    }
```

Bibliography

[1] R. W. Erickson and D. Maksimovic, *Fundamentals of Power Electronics*, 2nd ed. Springer, 2001.

[2] A. Boucher, C. Cox, and A. Doonan, "Sampling time selection and its effect on direct digital and adaptive control algorithm implementation," in *IEE Colloquium on Implementation Problems in Digital Control*, 1989, pp. 5/1–5/8.

[3] Tang and Salmon, "A dsp-based control system for current controlled 3-phase pwm boost rectifier," in *1994 Proceedings of Canadian Conference on Electrical and Computer Engineering*, 1994, pp. 781–784 vol.2.

[4] Y. Jin, J. Xu, G. Zhou, and C. Mi, "Small-signal modeling and analysis of improved digital peak current control of boost converter," in *2009 IEEE 6th International Power Electronics and Motion Control Conference*, 2009, pp. 326–330.

[5] L. Roggia, F. Beltrame, J. E. Baggio, and J. R. Pinheiro, "Digital control system applied to a pfc boost converter operating in mixed conduction mode," in *2009 Brazilian Power Electronics Conference*, 2009, pp. 698–704.

[6] M. F. N. b. Tajuddin, N. A. Rahim, and I. Daut, "Design and implementation of a dsp based digital controller for a dc-dc converter," in *2009 Second International Conference on Computer and Electrical Engineering*, vol. 1, 2009, pp. 209–213.

[7] O. Ellabban, O. Hegazy, J. Van Mierlo, and P. Lataire, "Dual loop digital control design and implementation of a dsp based high power boost converter in fuel cell electric vehicle," in *2010 12th International Conference on Optimization of Electrical and Electronic Equipment*, 2010, pp. 610–617.

[8] C. Zhou, Q. Zhang, D. Ezechias, Y. Gao, H. Deng, and S. Qu, "A general digital pid controller based on pwm for buck converter," in *Proceeding of the 11th World Congress on Intelligent Control and Automation*, 2014, pp. 4596–4599.

[9] K. Kajiwara, H. Tajima, and F. Kurokawa, "Integral gain switchover digital control boost converter to improve light load characteristics," in *2015 International Conference on Renewable Energy Research and Applications (ICRERA)*, 2015, pp. 1048–1051.

[10] M. M. Garg and M. Kumar Pathak, "Performance comparison of non-ideal and ideal models of dc-dc buck converter," in *2018 8th IEEE India International Conference on Power Electronics (IICPE)*, 2018, pp. 1–6.

[11] D. Ounnas, D. Guiza, Y. Soufi, R. Dhaouadi, and A. Bouden, "Design and implementation of a digital pid controller for dc–dc buck converter," in *2019 1st International*

Conference on Sustainable Renewable Energy Systems and Applications (ICSRESA), 2019, pp. 1–4.

[12] M. M. Garg, Y. V. Hote, and M. K. Pathak, "Design and performance analysis of a pwm dc–dc buck converter using pi–lead compensator," *Arabian Journal for Science and Engineering*, vol. 40, no. 12, pp. 3607–3626, Dec 2015. [Online]. Available: https://doi.org/10.1007/s13369-015-1838-z

[13] V. Jindal and D. Joshi, "A comparative analysis of classical tuning methods of pi controllers on non-ideal buck converter," in *2022 2nd International Conference on Power Electronics IoT Applications in Renewable Energy and its Control (PARC)*, 2022, pp. 1–5.

[14] T. Instruments, "Tms320f2812 analog-to-digital converter (adc) peripheral referance guide," 2002.

[15] L. Guo, "Implementation of digital pid controllers for dc-dc converters using digital signal processors," *2007 IEEE International Conference on Electro/Information Technology*, pp. 306–311, 2007.

[16] T. Instruments, "Texas implementation tutorial for tms320f2812," 2005.

[17] V. Viswanatha, R. V. S. Reddy, and Rajeswari, "Characterization of analog and digital control loops for bidirectional buck–boost converter using pid/pidn algorithms," *Journal of Electrical Systems and Information Technology*, vol. 7, no. 1, p. 6, Apr 2020. [Online]. Available: https://doi.org/10.1186/s43067-020-00015-6

[18] N. Mohan, T. M. Undeland, and W. P. Robbins, *Power Electronics. Converters, Applications and Design*, 3rd ed. John Wiley and Sons, Inc, 2003.

[19] T. Instruments, "Application report, spraab3," 2005.

[20] *The Digital Control Loop.* John Wiley Sons, Ltd, 2015, ch. 2, pp. 51–78. [Online]. Available: https://onlinelibrary.wiley.com/doi/abs/10.1002/9781119025498.ch2