COMPARISION OF POWER AND PERFORMANCE OF FULL-ADDER USING DYNAMIC CMOS LOGIC, NORA LOGIC, AND NORA LOGIC WITH MTCMOS OF SUB-45nm TECHNOLOGY NODE

A

THESIS

REPORT

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CANDIDATE'S DECLARATION

I **Abhishek**, Roll No. **2K18/VLS/01** student of **M.Tech** with specialization in **VLSI Design & Embedded System**, hereby declare that the project Dissertation titled **"Comparison of Power and Performance of Full-Adder using Dynamic CMOS Logic, NORA Logic and NORA Logic with MTCMOS of Sub-45nm Technology Node"** which is submitted by me to the Department of **Electronics and Communication Engineering**, **Delhi Technological University, Delhi** in partial fulfillment of the requirement for the award of the degree of **Master of Technology** is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any degree, Diploma Associateship, Fellowship, or other similar title or recognition.

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ABSTRACT

In digital systems, arithmetic operations play a major role and full adder is the center of focus of all arithmetic operations. By using static CMOS logic, transmission gates, dynamic logic, or pass transistor logic we can design a full adder. Here, the main focus is on Dynamic Logic because of its high performance and low power consumption. We have also proposed a hybrid of MTCMOS logic and NORA logic by introducing high-V_t transistors near the supply and ground to minimize leakage power because leakage is very high in Deep Submicron technology. We have also done a comparison of dissipated power and propagation delay of full-adder based on Basic Dynamic CMOS logic, NORA Dynamic Logic, and MTCMOS with NORA Dynamic Logic of 45nm, 32nm, 22nm high-k dielectric Predictive Technology Model (PTM) has been implemented for a constant supply.

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LIST OF SYMBOLS AND ABBREVIATIONS

CMOS	Complementary metal–oxide–semiconductor
MOSFET	Metal-oxide-semiconductor Field effect transistor
FET	Field effect transistor
PDN	Pull-Down network
PUP	Pull-Up network
PMOS	P-type metal-oxide-semiconductor
NMOS	N-type metal-oxide-semiconductor
CLK	Clock Signal
NORA	no-race
MTCMOS	Multi-threshold-voltage CMOS
V_t	Threshold Voltage
PTM	Predictive Technology Model
LP	low-power
HP	high-performance
P_{CLK}	average power dissipation by clock signal CLK
P_{CLK_B}	average power dissipation by clock signal CLK_B
P_{Vdd}	average power dissipation by DC voltage source Vdd.
P_A	average power dissipation by input signal A
P_B	average power dissipation by input signal B
P_{Cin}	average power dissipation by input signal Cin
DC	Direct current
PDP	Power-Delay Product
PTL	Pass-Transistor Logic
V	Volt
W	Watt
s	Second
μ	micro (10^{-6})
n	nano (10^{-9})

nm	nano-meter
p	pico (10^{-12})
max	maximum
$\oplus$	XOR

CHAPTER 1

INTRODUCTION

1.1 Motivation

Full-adder is widely used in processors, hence its power optimization with the least impact on performance is necessary for low-power VLSI technology. The most popular technique to decrease power dissipation in CMOS Logic circuit is to reduce supply voltage. As supply voltage reduces, both static and dynamic power dissipation decreases. But there would be a dramatic increment in the delay of a circuit and if we reduce supply voltage without reducing threshold voltage then the delay would increase drastically, which is not appreciable for high-frequency processors that we use nowadays. But if we reduce the threshold voltage then leakage would increase [8]. To reduce leakage power (mainly subthreshold leakage), which is dominant over dynamic power dissipation, many leakage reduction techniques are used i.e. transistor stacking, VTCMOS, MTCMOS, etc. MTCMOS [2] is used. In the case of transistor stacking if the number of inputs is high then it's a non-trivial approach to find out which combination gives the least leakage. For VTCMOS we need substrate biased control circuitry, which leads to the additional area and circuit complexity, hence we moved down to the MTCMOS approach. In MTCMOS [2] high-V_t transistors are connected to the power supply and ground which would decrease power dissipation during standby mode, the remaining logic would be implemented by low-V_t transistors to get less delay. For the processor, there are various algorithms to judicially combine low-V_t and high-V_t to get the optimized speed and leakage [7,9]. Gate leakage is reduced by using high-k dielectric [4] because for sub-45nm technology node, gate leakage is also considerable. But still, if we use static CMOS logic as the remaining low-V_t transistor logic, there would-be high-power dissipation with comparatively higher delay. Static CMOS logic with the number of inputs of N requires 2N devices. An assortment of methods was introduced to decrease the number of transistors needed to actualize a given logic function including pseudo-NMOS, pass transistor logic, and so on. The pseudo-NMOS logic needs just N + 1 semiconductors to execute an N input logic gate, however lamentably, it has static power dissipation. Another logic style called dynamic logic is introduced that acquires a comparable outcome while keeping away from static power dissipation. With the addition of a clock signal, it utilizes an order of pre-charge and evaluation phases. But there would be some disadvantages too, which is eliminated by DOMINO Logic and NORA Logic [5]. But DOMINO Logic has a comparatively higher transistor count (due to the attached inverter after 2 each stage). It also has the disadvantage of noninverting output, which is eliminated by NORA Logic implementation. Simulations are done in LTspice [17] XVII environment. Full-Adder of 1-bit has three inputs and two outputs.

Here we combine the concept of Dynamic circuit NORA logic and MTCMOS for full-adder design to decrease average power dissipation by DC voltage source (especially for lower technology node) with less compromise in performance.

1.2 Objective

The objective of this report is Comparison of Power and Performance of Full-Adder using Dynamic CMOS Logic, NORA Logic, and NORA Logic with MTCMOS of Sub-45nm Technology Node.

1.3 Organization of Report

This report has been organized into 8 chapters. Chapter 1 deals with the Introduction. It also includes motivation, objective, organization of the report, Dynamic CMOS, MTCMOS with NORA Logic, and Various Full-Adders. Chapter 2 is about Literature Survey. Chapter 3 deals with Setup and Simulation. Chapter 4 is about Results and analysis. Chapter 5 deals with the Conclusion and Future Scope.

1.4 Dynamic CMOS

Dynamic logic requires N+2 transistors for N number of inputs with a very high reduction in static power consumption. With the addition of a clock input, it uses an order of pre-charge and conditional evaluation phases.

1.4.1 Dynamic Logic: Basic Principles

The basic structure of an (n-type) dynamic logic gate is shown in Fig. 1.1. The PDN (pull-down network) is created exactly as in complementary CMOS.

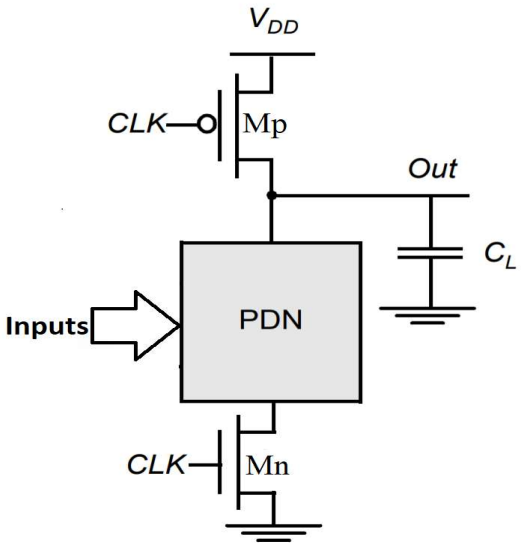

Fig. 1.1 Dynamic Logic

This circuit is operated in two modes: pre-charge and evaluation, and the operation mode is determined by the clock signal CLK.

1.4.2 Advantages of Dynamic Circuits:

1. No ratioed logic
2. Lower Static Power Consumption
3. High Speed due to much less load capacitance than static CMOS

4. For fan-in N, N+2 number of transistors instead of 2N. Hence less silicon area.
5. No glitching power dissipation, because it is synchronized by the clock.

1.4.3 Disadvantages of Dynamic Circuits:

1. Charge Leakage Problem
2. Charge Sharing Problem
3. Clock Skew Problem

We can overcome the Charge leakage and Charge Sharing problem by using a weak PMOS pull-up device and higher V_t transistors.

When we cascade dynamic gates, there will be a clock skew problem i.e., overlapping of pre-charge and evaluation. Depending on the clock tree network, the clock can reach different points of the circuit at a different time because of the different delay of the clock tree network. We may get incorrect output because of the overlapping of the pre-charge and evaluation phase of different stages of the dynamic circuit.

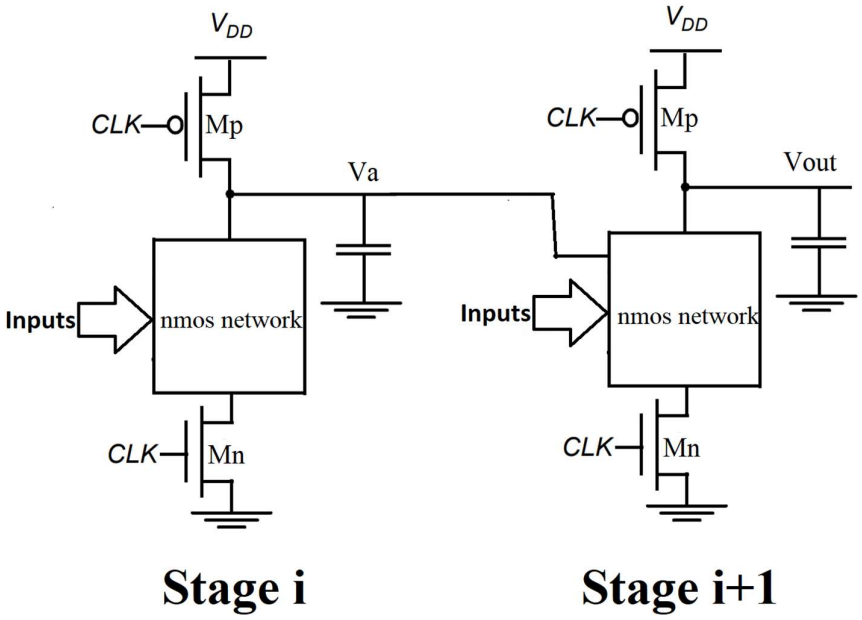

Fig. 1.2 Cascaded Dynamic Logic

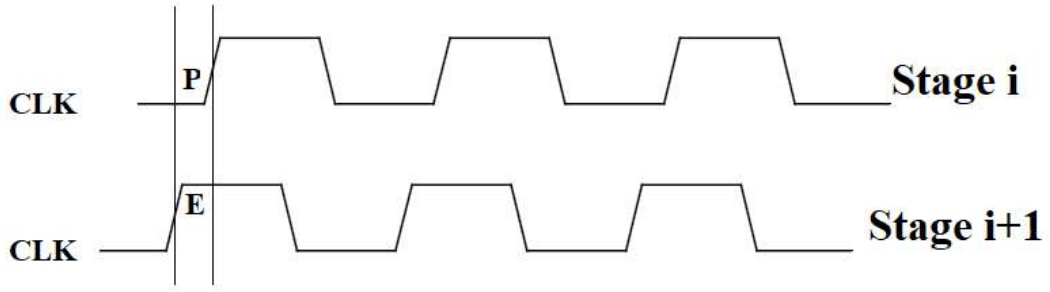

Fig. 1.3 Overlapping of pre-charge and evaluation phase due to clock skew

Suppose Stage i is in pre-charge mode but due to clock skew Stage i+1 comes under evaluation mode.

At that time Va will be at a logic high value, due to which there is a possibility that capacitance at Vout discharges at the pre-charge phase. Hence, we may get incorrect output. This problem can be overcome by DOMINO or NORA [5] styles:

1. If the output of Stage 'i' is low during the pre-charge phase by cascading an inverter with each stage. i.e. using Domino CMOS Circuit.
2. By alternatively cascading NMOS and PMOS logic (since the high value of the output of stage 'i' won't impact PMOS network). i.e. using NORA Logic.

But due to the higher switching activity and non-inverting nature of the Domino CMOS circuit, NORA Logic is used.

1.4.4 NORA Logic:

NORA means 'no-race,' demonstrating another technique to take out the 'racing' issue of the straightforwardly cascaded dynamic logic block. Fig. 1.4 portrays the basic structure of NORA logic which is characterized by alternating the MOSFETs in the logic block from PMOS to NMOS logic gates and so on.

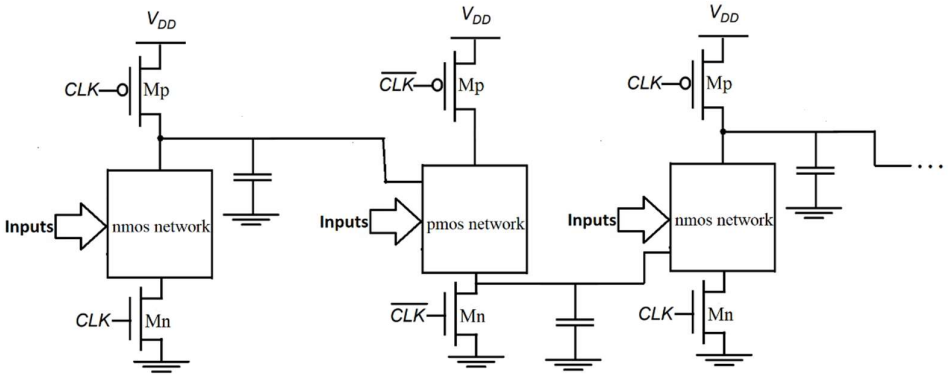

Fig. 1.4 Basic structure of NORA Logic

By alternatively putting the PMOS and NMOS network, the clock skew issue overcomes in the NORA logic circuit. It has a higher adaptability when contrasted with DOMINO.

Both inverted and non-inverted signals are accessible from the NORA logic.

In Full-adder realization, 20 transistors are used which is less than 28 transistors of Static CMOS Full-adder realization.

Also, each state is driving one transistor instead of two (i.e. no need to drive both NMOS and PMOS) causes a significant reduction in capacitance. Hence speed increases.

1.5 MTCMOS with NORA Logic

Leakage power increases as we go from one technology generation to the next technology generation due to the increment in subthreshold current and gate current because of short channel effects and less oxide thickness. Gate leakage is reduced by using high-k dielectric. To reduce leakage power (mainly subthreshold leakage), which is dominant over dynamic power dissipation, many leakage reduction techniques are used i.e transistor stacking, VTCMOS, MTCMOS, etc. MTCMOS [2] is used. In the case of transistor stacking if the number of inputs is high then it's a non-trivial approach to find out which combination gives the least leakage. For VTCMOS we need substrate biased control circuitry, which leads to the additional area and circuit complexity, hence we moved down to the MTCMOS approach. Here we use Multi-threshold-voltage CMOS (MTCMOS) to reduce Standby leakage, mainly subthreshold leakage.

The logic block contains low-V_t transistors that are used for faster switching speed at Active mode while high-V_t transistors to reduce leakage at Standby mode as shown in Fig. 1.5. When Mp and Mn transistors are ON, the circuit operates in Active mode. When OFF, the circuit is in Standby mode.

Earlier we discussed that NORA logic is used for lower Dynamic power and high speed. Here we combine the application of NORA and MTCMOS logic to get lower static as well as dynamic power and higher speed of 1-bit full adder. Low-V_t transistors are the PTM HP model of respective technology used in NORA logic for high performance and Lower Dynamic power. High-V_t transistors are the PTM LP model of respective technology to reduce leakage because at standby mode leakage current is minima of leakage of high-V_t and low-V_t transistors as shown in Fig. 1.6.

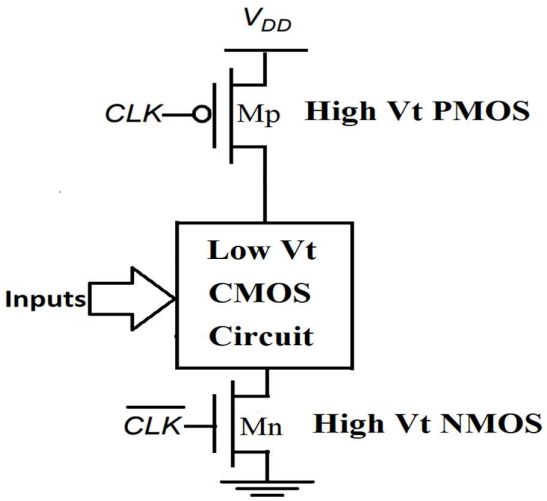

Fig. 1.5 MTCMOS Logic

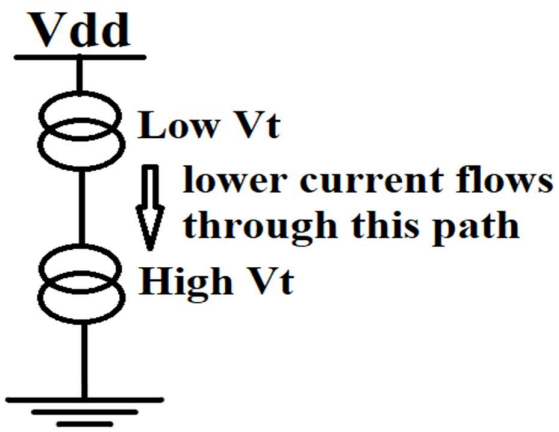

Fig. 1.6 Leakage current in Standby Mode

Here we don't add extra sleep transistors for MTCMOS, rather we make CLK and CLK_B operated transistors of high-V_t to reduce average power dissipation by DC voltage source without much impact on delay.

1.6 Various Full-Adders

1.6.1 Importance of Full-Adders in Digital Circuits:

The most well-known and broadly utilized arithmetic function is adding. The adder circuit is the essential building block of numerous digital frameworks like multipliers, processors to execute different calculations. The digital systems are desired to have high

speed and should be able to operate at high frequencies with low power consumption. Advanced gadgets like cell phones, workstations, and other convenient gadgets need more battery backup. Thus, the dissipated power of these circuits should be as less as could reasonably be expected. Thus, these parameters i.e. area, power, and speed need to be optimized while designing. All these parameters are very crucial and very difficult to attain in a single design. Consequently, contingent upon necessity and application area adjustments between these three parameters are being made.

1-digit Full-Adder has three sources of info and two yields. Let A, B, Cin be three sources of info and SUM, Cout is two outputs as appeared in Fig. 1.7.

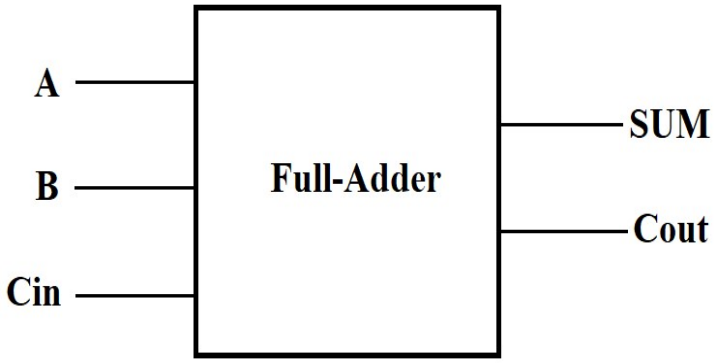

Fig. 1.7 Full-Adder Block Diagram

1.6.2 Full-Adder Truth Table and Boolean Equation:

For 3-input, there would be 8 combinations as shown in Table 1.1

A	B	Cin	SUM	Cout
0	0	0	**0**	**0**
0	0	1	**1**	**0**
0	1	0	**1**	**0**
0	1	1	**0**	**1**
1	0	0	**1**	**0**
1	0	1	**0**	**1**
1	1	0	**0**	**1**
1	1	1	**1**	**1**

Table 1.1 Full-Adder Truth Table

SUM= A ⊕B ⊕Cin = ABCin + $\overline{Cin}$ (A+B+Cin)

Cout= AB + Cin(A+B)

CHAPTER 2
Literature Survey

2.1 Summarization of various authors' work:

D. Radhakrishnan analyzed a full adder design using the new exclusive-OR and exclusive-NOR cell that does not experience threshold voltage drop using a fewer number of transistors, [1].

M.H. Anis, M.W. Allam, M.I. Elmasry analyzed dynamic logic using DOMINO and also added MTCMOS which substantially reduces the subthreshold leakage current, [2].

W. Zhao and Y. Cao conclude a new generation of predictive technology model developed for 130nm to 32nm technology nodes. This methodology has better scalability and physicality over a wide scope of design and process conditions. Amazing estimates checked for both nominal and variation characteristics, [3].

A. Venkateshan, R. Singh, K.F. Poole, J. Harriss, H. Senter, R. Teague, and J. Narayan gives detail about the results of a new process to deposit high-k dielectric materials. For EOT of 0.39 nm, the ultralow value of leakage current density has been achieved that can be used for less than 10nm technology nodes CMOS, [4].

D. Samanta, N. Sinha, and A. Pal give a new methodology for dynamic CMOS circuits using DOMINO and NORA style synthesis. That method gives better results regarding the area, delay, and consumption of power compared to the prevailing approaches, [5].

Keivan Navi, Omid Kavehei, Amir Sahafi, and Shima Mehrabi projected different full adder styles to find the most efficient in terms of area, delay, and power consumption with robustness, [6].

Pal, Ajit, proposed an algorithm to realize energy-optimized dual-V_t CMOS circuits for battery-operated portable systems, [7].

S. Roy and A. Pal proposed a new approach, which combines the judicious use of sizing and an optimal single-V_t to attain less leakage compared to that of dual-V_t, but also less sensitive to process parameter variations, [8].

Chen, Zhanping & Wei, Liqiong & Roy, and Kaushik present a new algorithm to balance different paths of a design converging to logic gates using multiple-threshold transistors such that both dissipation of power due to spurious transitions and leakage current is minimized. Leakage power is reduced due to the use of V_t transistors in the non-critical paths, [9].

Rumi Rastogi and Sujata Pandey proposed a new low power dynamic MTCMOS full-adder. Domino circuit of 8-bit and TSPC (True Single-phase clock) adder circuits at 45nm. Among the proposed adders, the TSPC adder is found to be the fastest with the least average power dissipation and the least transistors count as compared to other adders, [10].

Paro Bajpai, Priyanka Mittal, Amita Rana, and Bhupesh Aneja reviewed different CMOS logic families and estimation based on performance, power, and transistor count, [11].

Keerthana M and Ravichandran analyzed a hybrid Full Adder of 1-bit using a technology node of 22nm and also conclude that hybrid design logic circuits are primarily used for customizing design circuits with low power and delay with high efficiency, [12].

N. Weste, D. Harris, and A. Banerjee [16] J. M. Rabaey, A. Chandrakasan, and B. Nikolic [17] are reference book used to know about dynamic CMOS and MTCMOS in detail.

2.2 Conclusion of literature survey:

Based on the literature survey, it is concluded that lots of research work have been done to optimize full-adder in terms of dissipated power, speed, and area. But we observe that the quality of the signal is degraded in PTL. Static CMOS logic takes more transistor count and also has a clock skew problem. So, we moved to dynamic CMOS logic i.e. DOMINO logic to overcome with clock skew problem in conventional dynamic CMOS logic. But DOMINO increases transistor counts due to the inverter attached to each stage. It also has a problem to implement inverting logic.

So, here we will implement NORA logic to overcome the DOMINO Logic problem along with MTCMOS Configuration to decrease leakage power dissipation.

CHAPTER 3
Setup and Simulations

3.1 Tools Used:

In this report, we used the **LTspice** simulation tool version XVII.

LTspice is an elite SPICE software for simulation, schematic, and waveform viewer with improvements and models for facilitating the simulation of analog circuits, [17]. Included in the download of LTspice are macro models for a majority of Electronic Devices switching regulators, amplifiers, as well as a library of devices for general circuit simulation.

3.2 Benefits of LTspice Simulation Platform:

- It is an open-source tool.
- It is widely used for analog as well as digit circuit simulations.
- We can easily import the SPICE model to our schematic. Here we will import PTM.

3.3 Predictive Technology Model (PTM):

It gives precise, adjustable, and predictive model documentations for upcoming transistors and interconnects innovations, [16]. These documentations are viable with standard circuit simulators, for example, SPICE, and scalable with a wide range of process variations. With PTM, competitive circuit design and exploration begin even before the serious semiconductor innovation completely evolved.

PTM releases models for low-power applications (PTM LP), combining high-k/metal gate and stress effect.

- 22nm PTM LP model: V2.1
- 32nm PTM LP model: V2.1
- 45nm PTM LP model: V2.1

PTM releases models for high-performance applications (PTM HP), combining high-k/metal gate and stress effects.

- 22nm PTM HP model: V2.1
- 32nm PTM HP model: V2.1
- 45nm PTM HP model: V2.1

These models will be imported to our schematic. A high-k dielectric model is used because as we scaled down the technology node, gate leakage is increased and it even dominates subthreshold leakage.

Here A, B, Cin are input pulse signal with the different time period and same rise and fall time of 10ps.

SUM and Cout are output.

CLK, CLK_B clocks are pulse signal complement of each other with a rise and fall time of 10ps, time period of 12.5ns.

Vdd is a DC power supply of 1V.

W/L ratio of PMOS is 6 and W/L of NMOS is 2.

PMOS1 and NMOS1 are high-V_t transistors of a given technology node to decrease leakage power dissipation.

3.4 Different Full-Adders Schematic:

Here we will make Full-Adder by Dynamic CMOS logic, NORA logic, MTCMOS with NORA logic, MTCMOS with NORA logic, and high-V_t at carry output (as shown in Fig. 3.1, 3.2, 3.3, and 3.4) and compare their power dissipation and delay using 22nm, 32nm, 45nm high-k dielectric PTM.

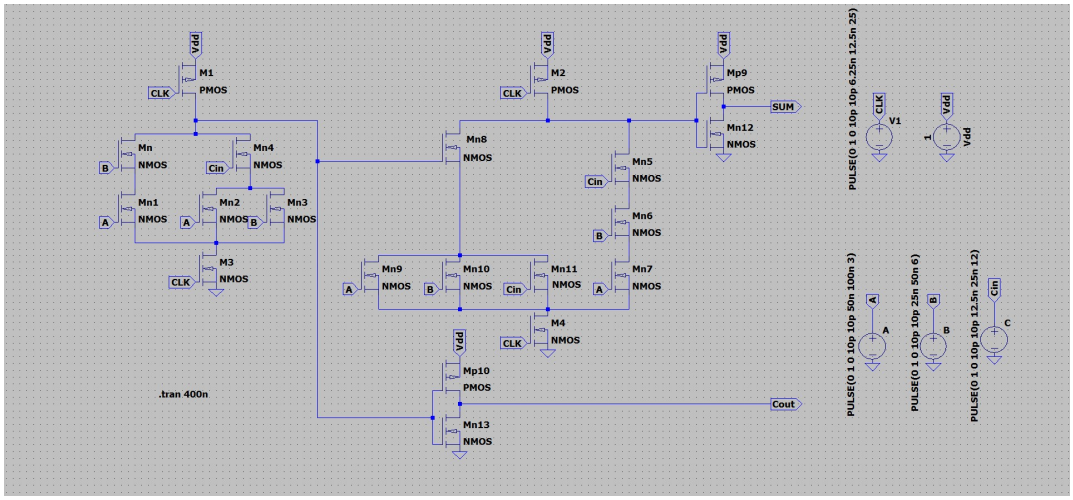

Fig. 3.1 Dynamic CMOS Full-Adder Schematic

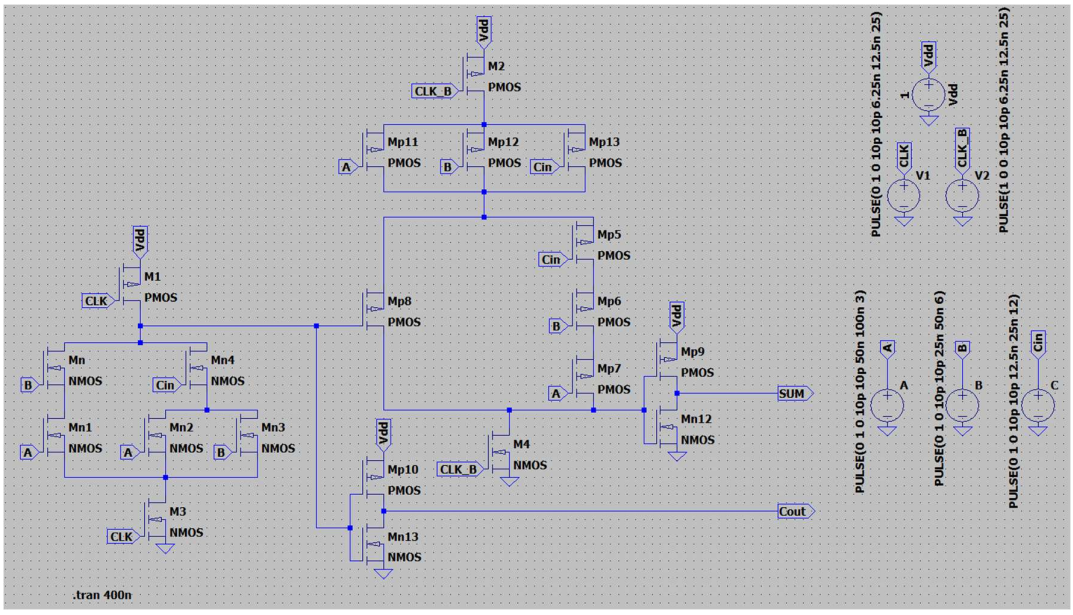

Fig. 3.2 Full-Adder using NORA Logic Schematic

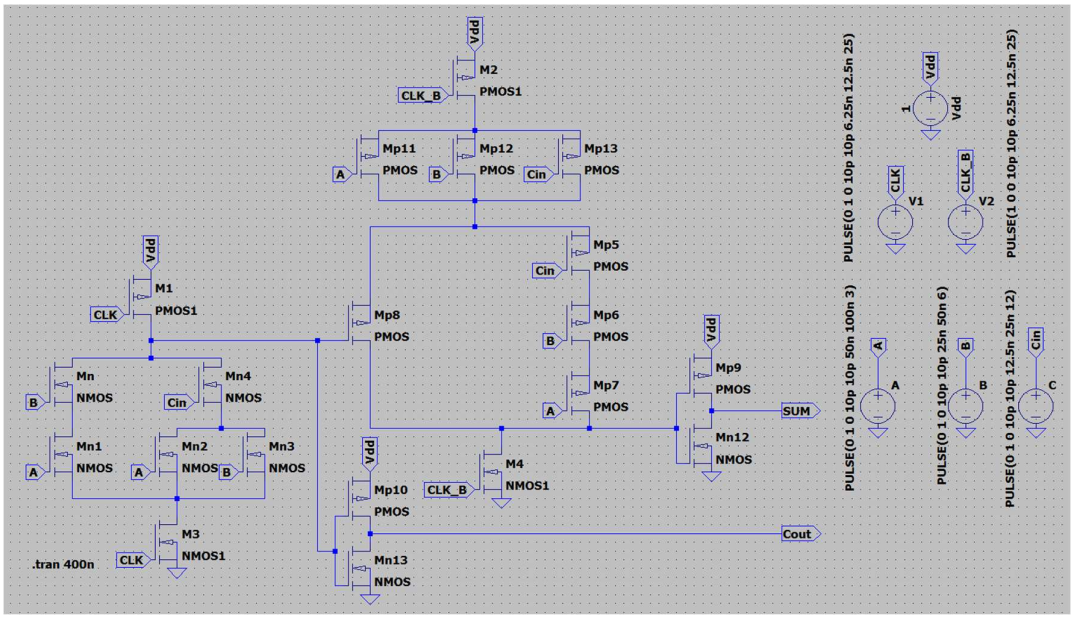

Fig. 3.3 Full-Adder using MTCMOS with NORA logic Schematic

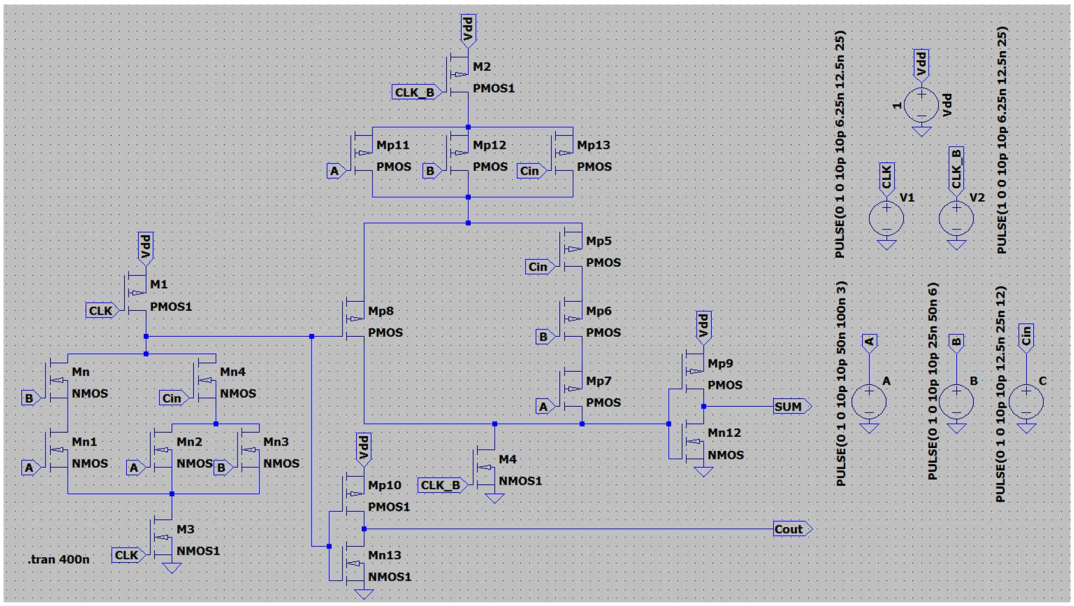

Fig. 3.4 Full-Adder using MTCMOS with NORA logic and high-V_t at Carry output Schematic

3.5 Various Full-Adder 45nm technology node Simulation:

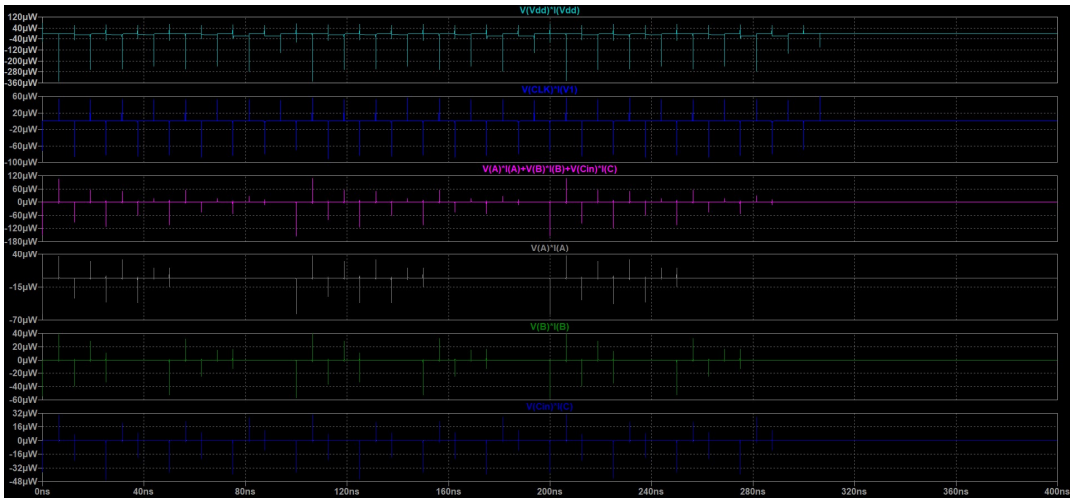

Fig. 3.5 Dynamic CMOS Full-Adder Power Dissipation (45nm)

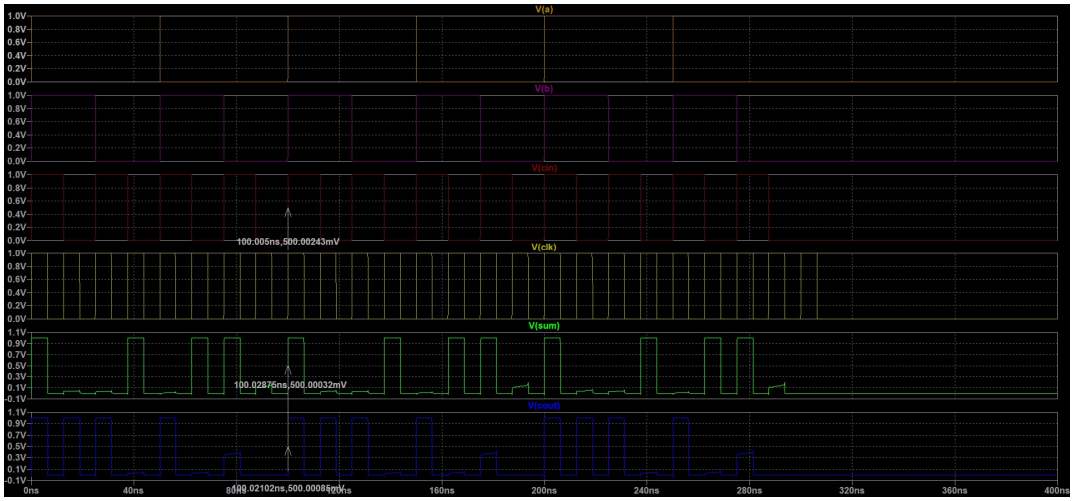

Fig. 3.6 Dynamic CMOS Full-Adder Propagation Delay (45nm)

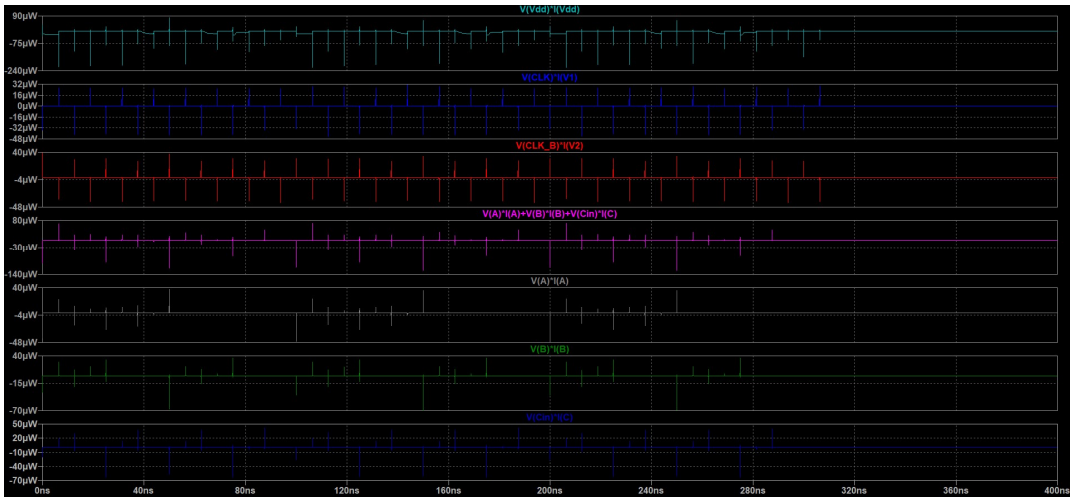

Fig. 3.7 Full-Adder using NORA Logic Power Dissipation (45nm)

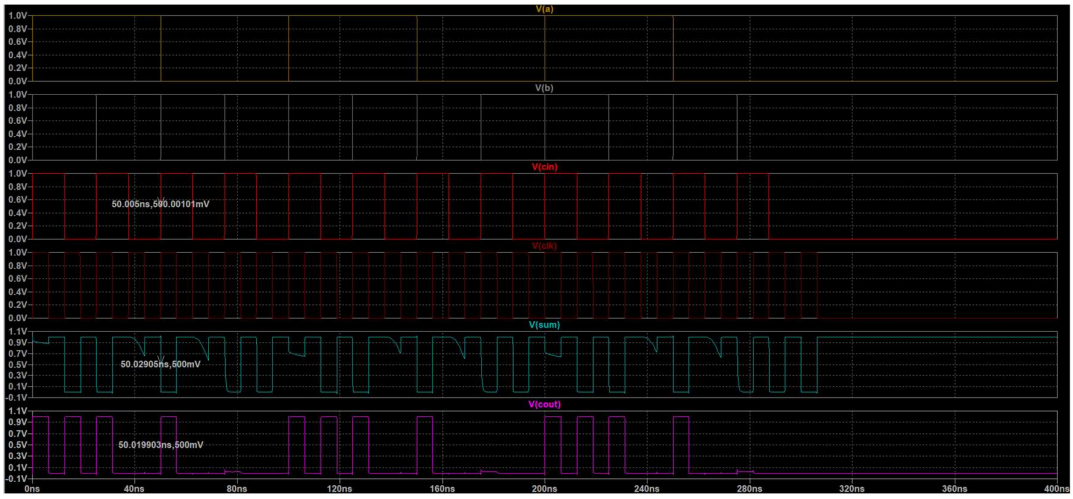

Fig. 3.8 Full-Adder using NORA Logic Propagation Delay (45nm)

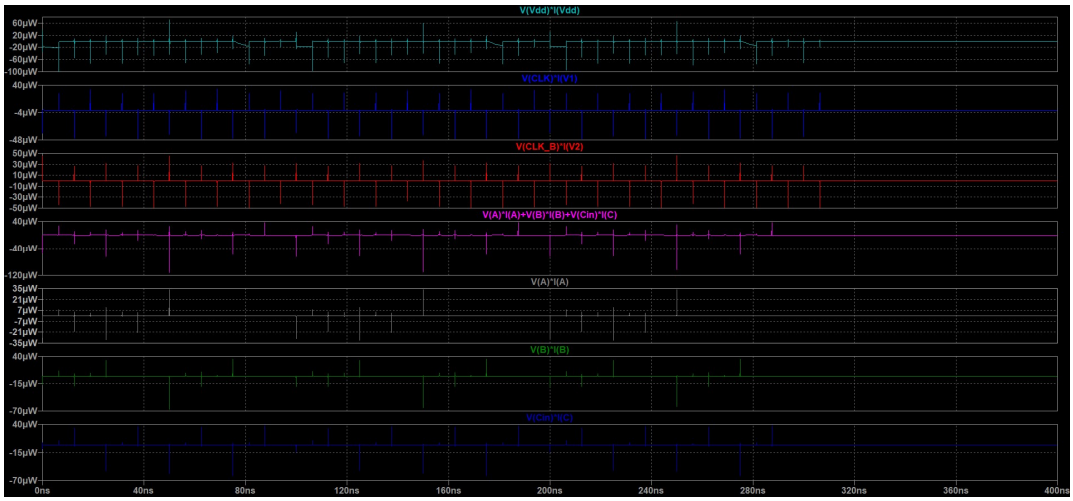

Fig. 3.9 Full-Adder using MTCMOS with NORA logic Power Dissipation (45nm)

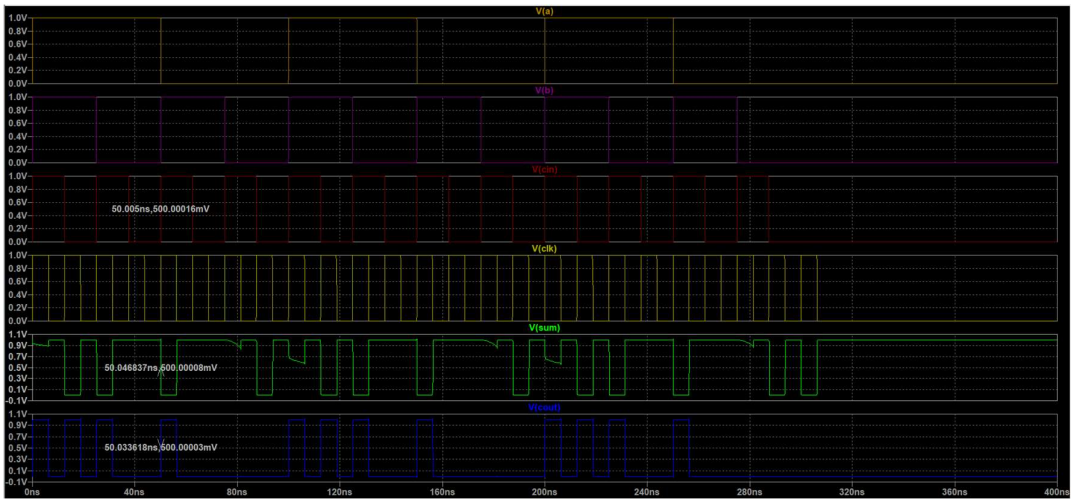

Fig. 3.10 Full-Adder using MTCMOS with NORA logic Propagation Delay (45nm)

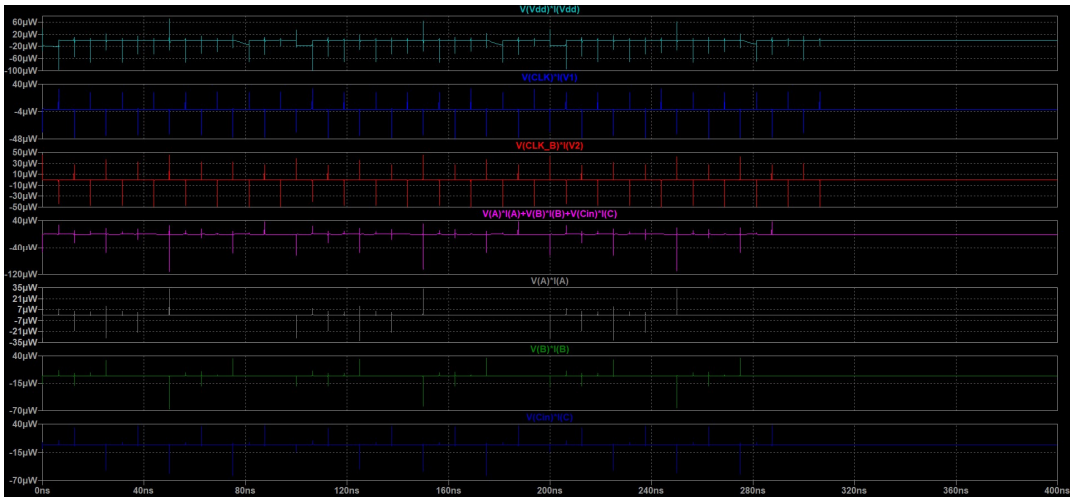

Fig. 3.11 Full-Adder using MTCMOS with NORA logic and high-V_t at Carry output Power Dissipation (45nm)

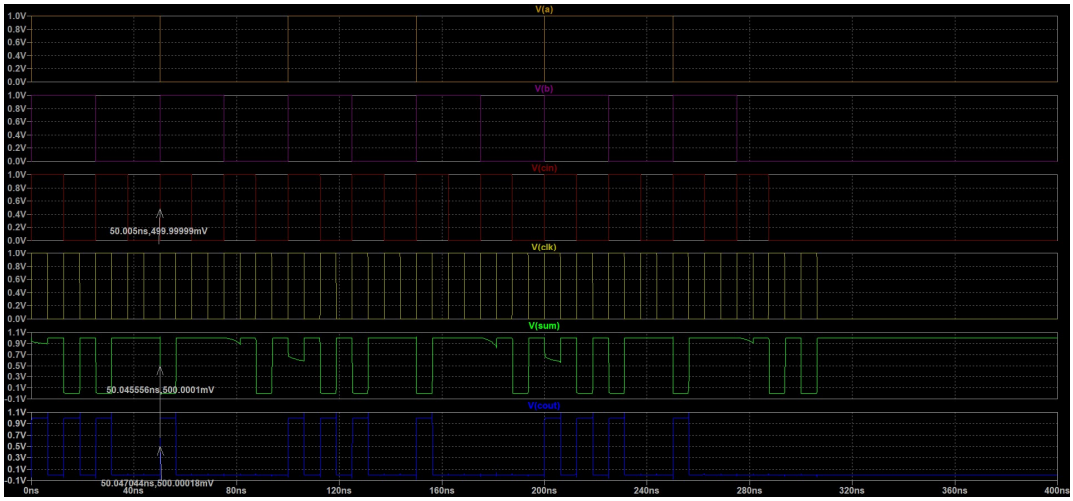

Fig. 3.12 Full-Adder using MTCMOS with NORA logic and high-V_t at Carry output Propagation Delay (45nm)

3.6 Various Full-Adder 32nm technology node Simulation:

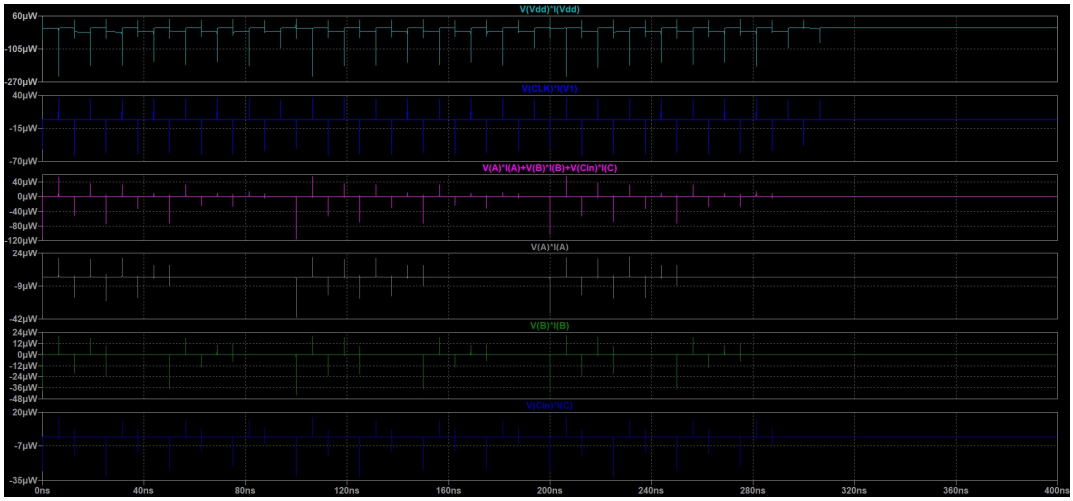

Fig. 3.13 Dynamic CMOS Full-Adder Power Dissipation (32nm)

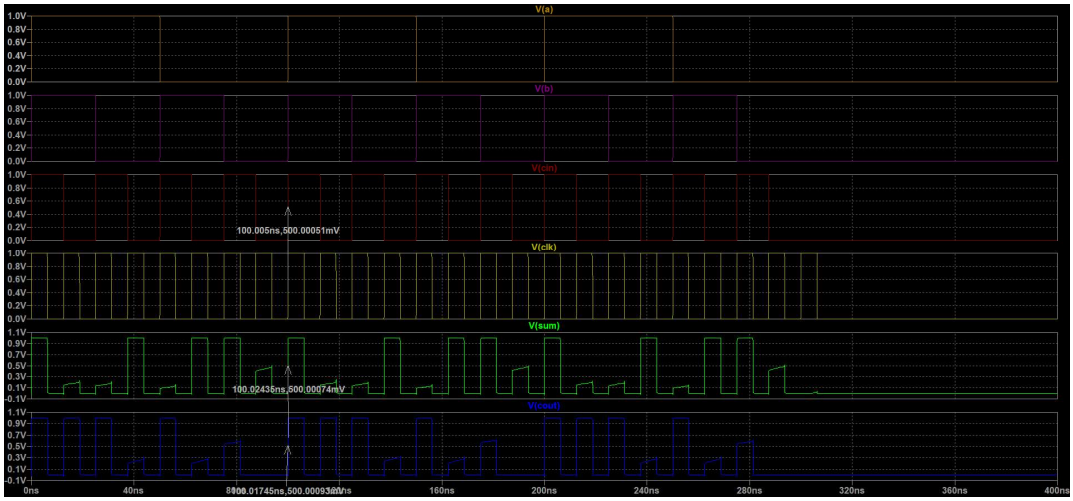

Fig. 3.14 Dynamic CMOS Full-Adder Propagation Delay (32nm)

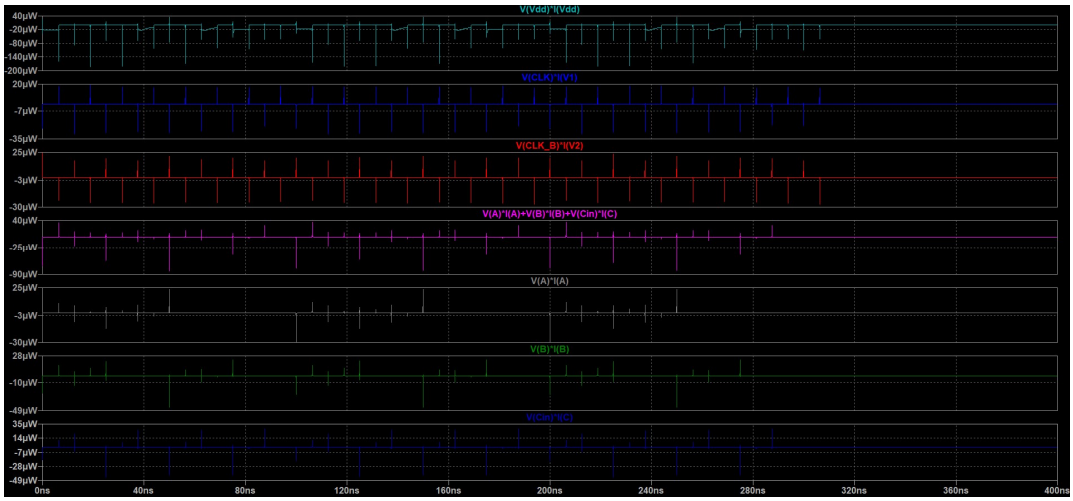

Fig. 3.15 Full-Adder using NORA Logic Power Dissipation (32nm)

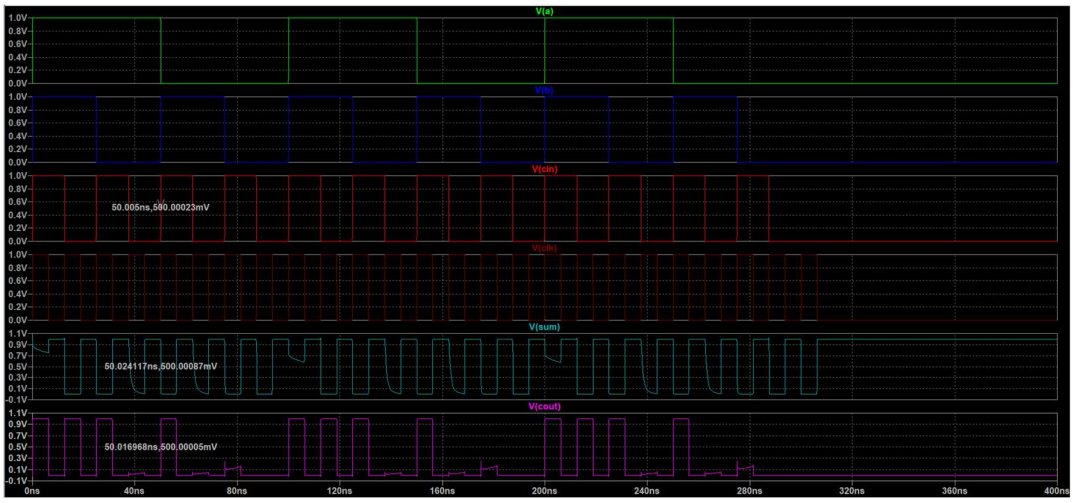

Fig. 3.16 Full-Adder using NORA Logic Propagation Delay (32nm)

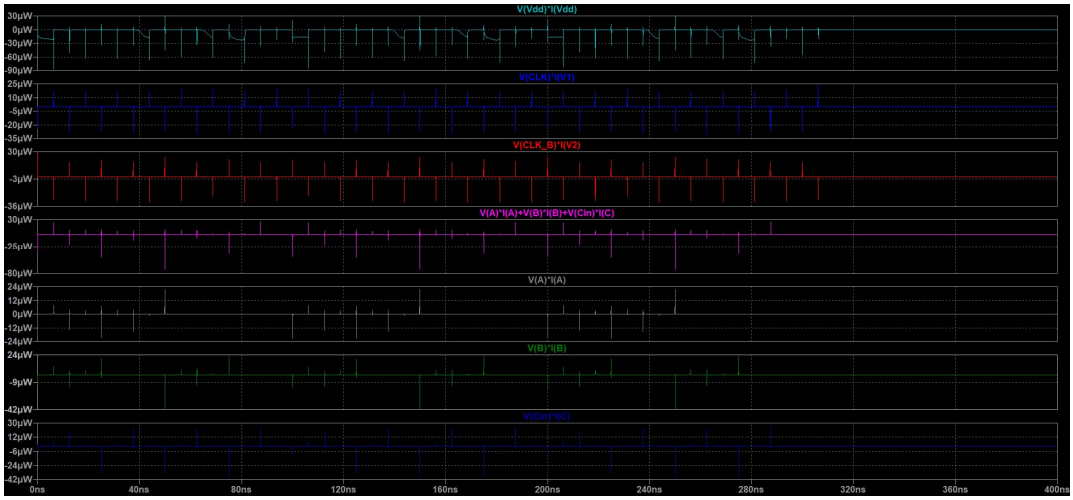

Fig. 3.17 Full-Adder using MTCMOS with NORA logic Power Dissipation (32nm)

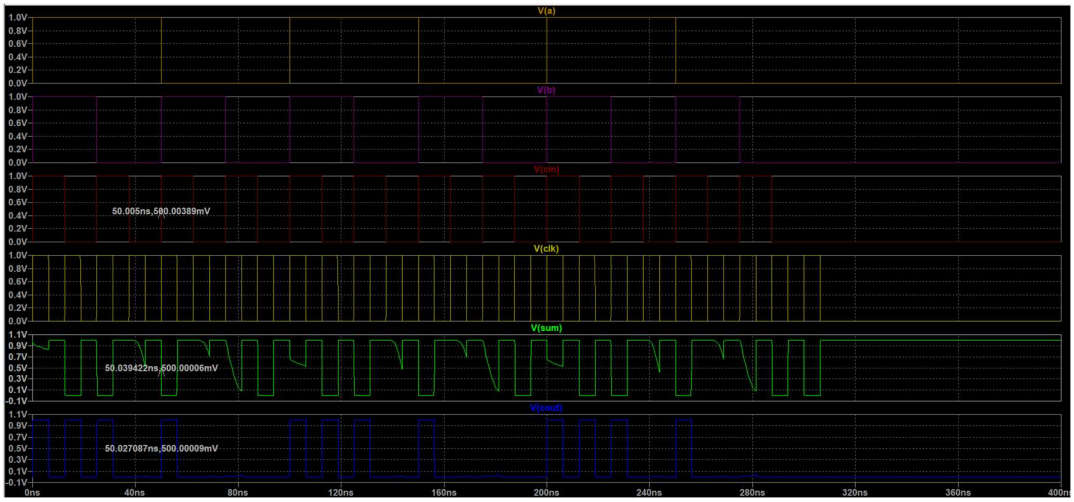

Fig. 3.18 Full-Adder using MTCMOS with NORA logic Propagation Delay (32nm)

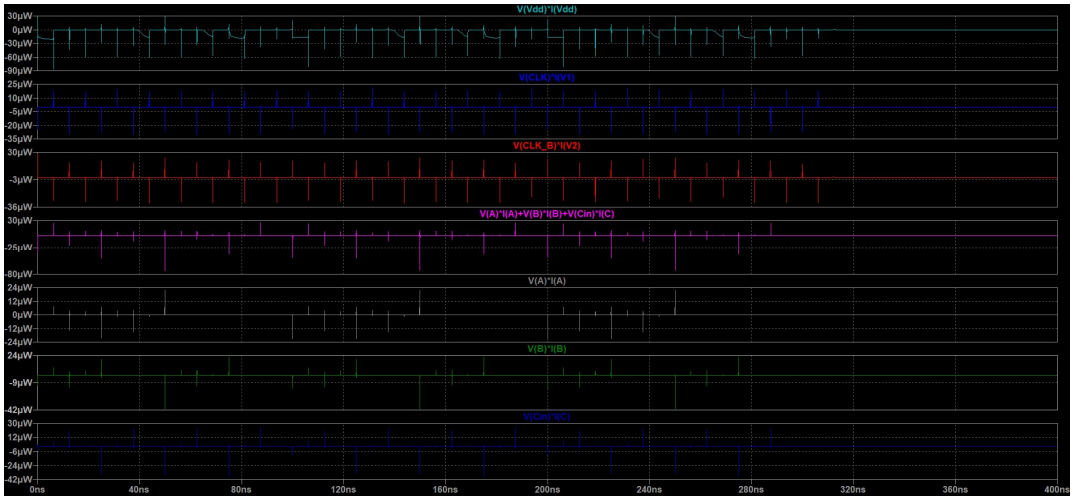

Fig. 3.19 Full-Adder using MTCMOS with NORA logic and high-V_t at Carry output Power Dissipation (32nm)

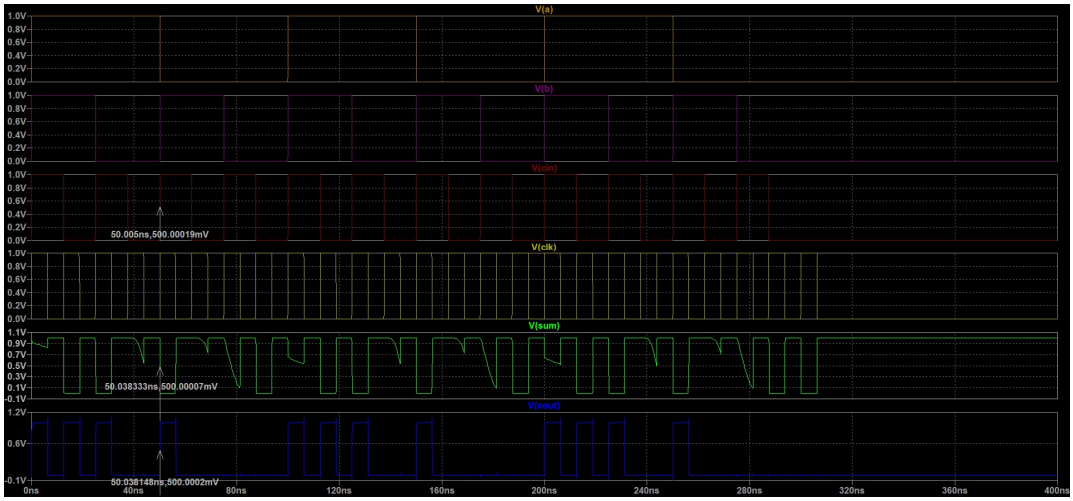

Fig. 3.20 Full-Adder using MTCMOS with NORA logic and high-V_t at Carry output Propagation Delay (32nm)

3.7 Various Full-Adder 22nm technology node Simulation:

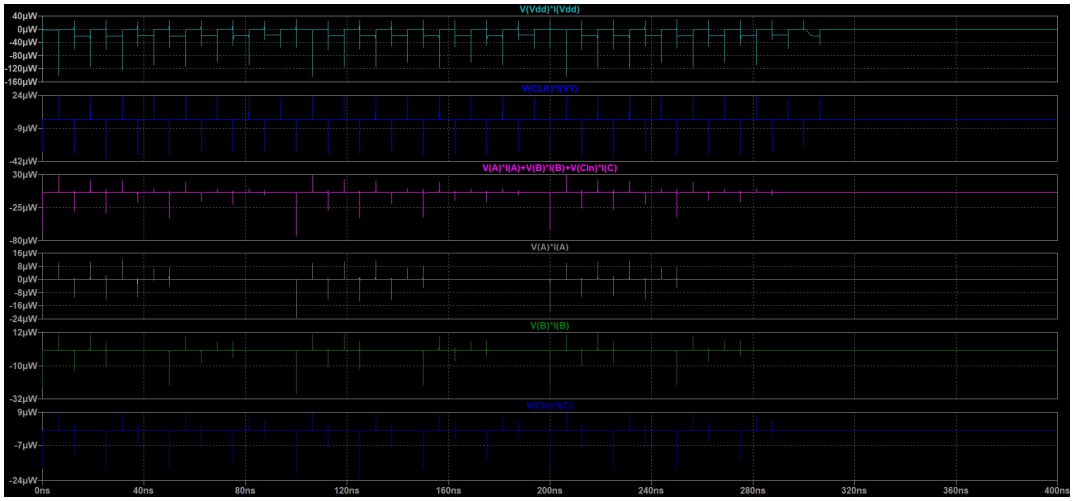

Fig. 3.21 Dynamic CMOS Full-Adder Power Dissipation (22nm)

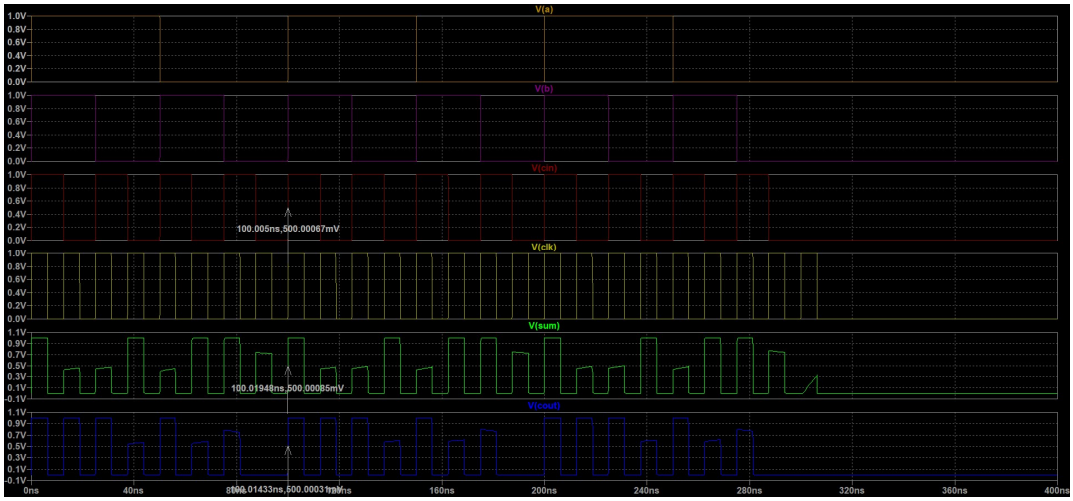

Fig. 3.22 Dynamic CMOS Full-Adder Propagation Delay (22nm)

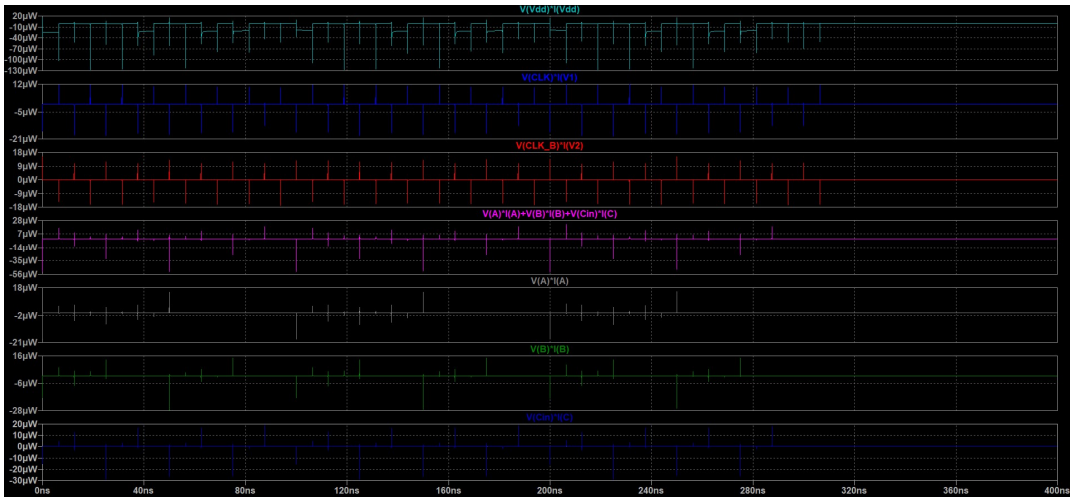

Fig. 3.23 Full-Adder using NORA Logic Power Dissipation (22nm)

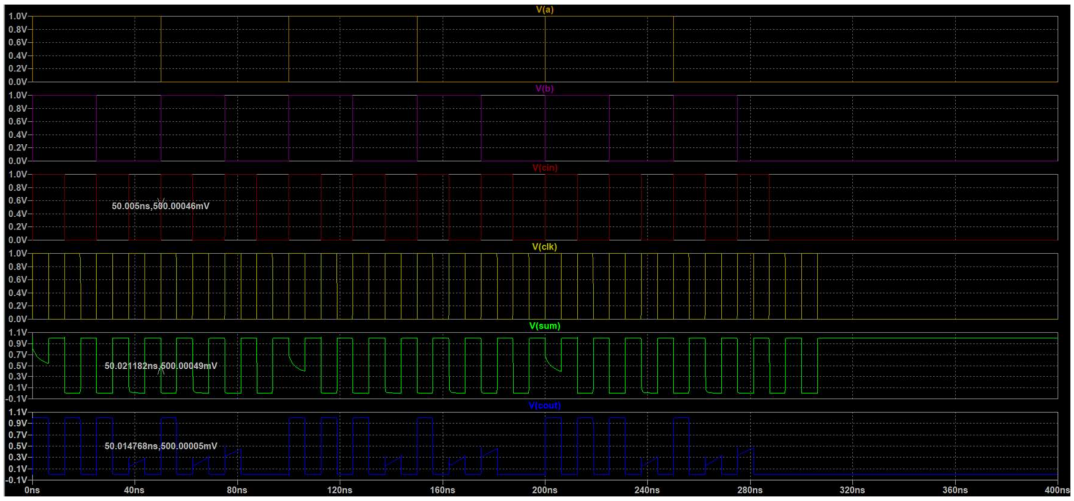

Fig. 3.24 Full-Adder using NORA Logic Propagation Delay (22nm)

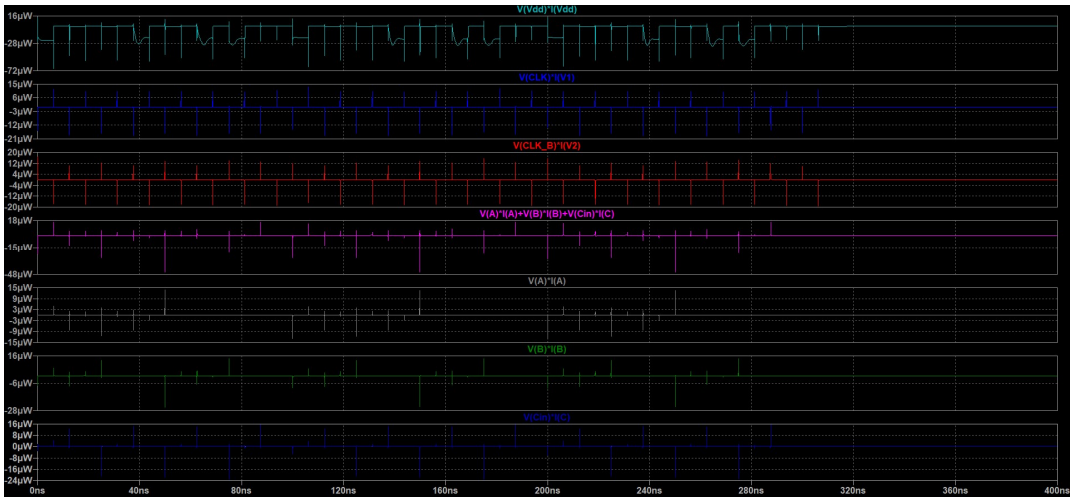

Fig. 3.25 Full-Adder using MTCMOS with NORA logic Power Dissipation (22nm)

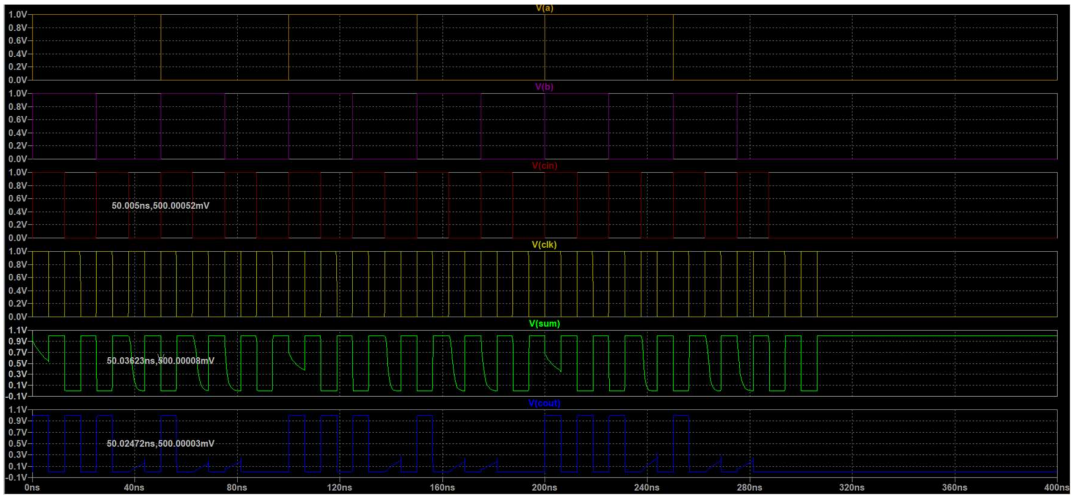

Fig. 3.26 Full-Adder using MTCMOS with NORA logic Propagation Delay (22nm)

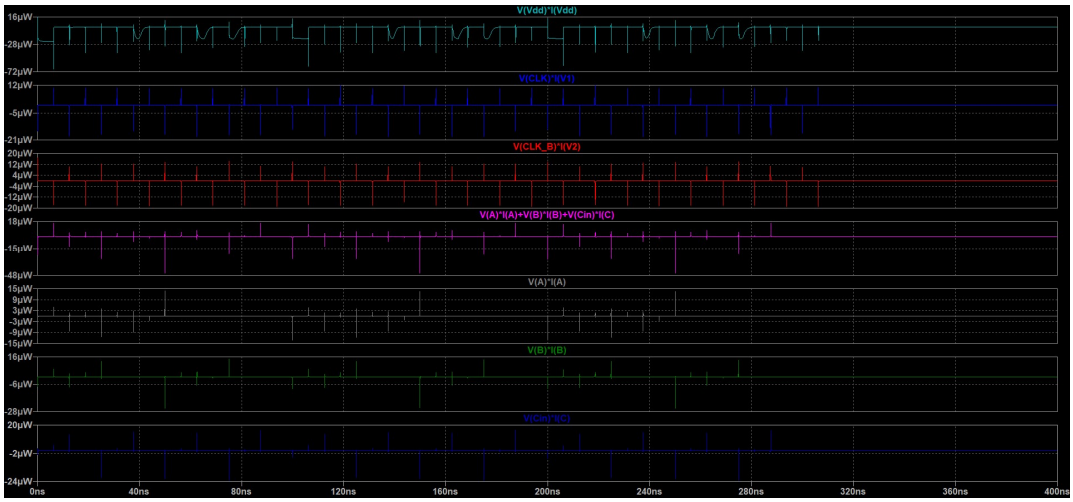

Fig. 3.27 Full-Adder using MTCMOS with NORA logic and high-V_t at Carry output Power Dissipation (22nm)

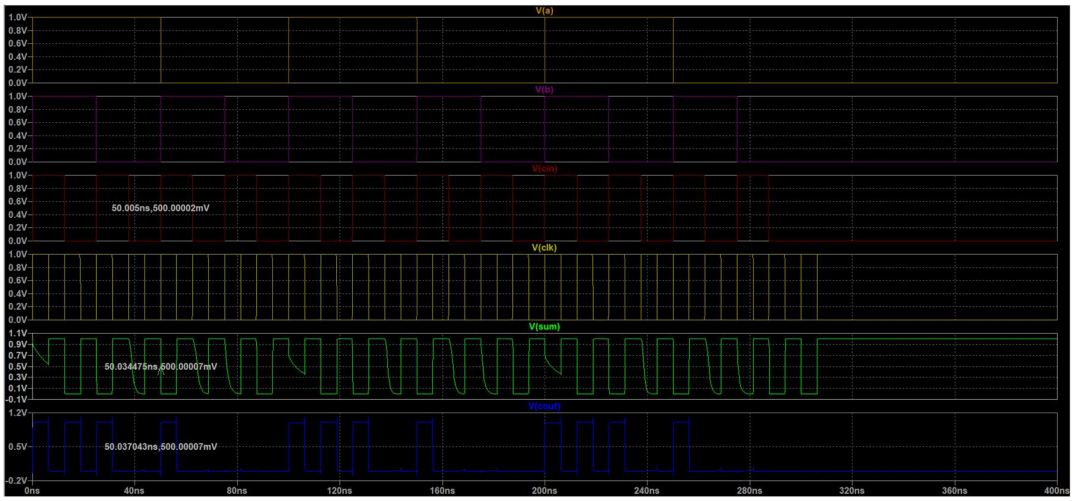

Fig. 3.28 Full-Adder using MTCMOS with NORA logic and high-V_t at Carry output Propagation Delay (22nm)

CHAPTER 4
Results and Analysis

4.1 Results:

Based on the simulation of various full-adders of 45nm, 32nm, and 22nm technology node we obtained various power dissipations and propagation delay which is shown in the following table.

In the following Tables-

- P_{CLK} and P_{CLK_B} are average power dissipation by the clock signal CLK and CLK_B respectively.
- P_{Vdd} is average power dissipation by DC voltage source Vdd.
- P_A, $P_{B,}$ and P_{Cin} are average power dissipation by input signals A, B, and Cin respectively.

Power Dissipation	45nm	32nm	22nm
P_{CLK}	-16.586 nW	-10.638 nW	-5.8953 nW
P_{Vdd}	-3.7838 µW	-6.2833 µW	-7.1433 µW
$P_A + P_B + P_{Cin}$	-5.4112 nW	-3.0199 nW	-1.5946 nW
P_A	-279.55 pW	108.56 pW	173.82 pW
P_B	-1.9137 nW	-1.0702 nW	-583.13 pW
P_{Cin}	-3.218 nW	-2.0583 nW	-1.1853 nW

Table 4.1 Dynamic CMOS Full-Adder Power Dissipation

Propagation Delay	45nm	32nm	22nm
SUM	23.75 ps	19.35 ps	14.48 ps
Cout	16.02 ps	12.45 ps	9.33 ps

Table 4.2 Dynamic CMOS Full-Adder Delay

Power Dissipation	45nm	32nm	22nm
$\mathbf{P_{CLK}}$	-7.4882 nW	-4.7461 nW	-2.8063 nW
$\mathbf{P_{CLK\_B}}$	-4.851 nW	-3.4873 nW	-2.1851 nW
$\mathbf{P_{Vdd}}$	-2.5573 µW	-3.5715 µW	-4.6511 µW
$\mathbf{P_A + P_B + P_{Cin}}$	-4.9002 nW	-2.9943 nW	-1.4944 nW
$\mathbf{P_A}$	1.2885 nW	915.07 pW	572.09 pW
$\mathbf{P_B}$	-1.1869 nW	-706.49 pW	-556.9 pW
$\mathbf{P_{Cin}}$	-5.0018 nW	-3.2029 nW	-1.5096 nW

Table 4.3 Full-Adder using NORA Logic Power Dissipation

Propagation Delay	45nm	32nm	22nm
SUM	24.05 ps	19.117 ps	16.182 ps
Cout	14.904 ps	11.968 ps	9.768 ps

Table 4.4 Full-Adder using NORA Logic Delay

Power Dissipation	45nm	32nm	22nm
$\mathbf{P_{CLK}}$	-9.526 nW	-6.106 nW	-3.9922 nW
$\mathbf{P_{CLK\_B}}$	-5.9278 nW	-4.2235 nW	-2.8594 nW
$\mathbf{P_{Vdd}}$	-1.4275 µW	-2.6701 µW	-4.736 µW
$\mathbf{P_A + P_B + P_{Cin}}$	-3.7632 nW	-2.5715 nW	-1.0095 nW
$\mathbf{P_A}$	1.9323 nW	773.92 pW	607.78 pW
$\mathbf{P_B}$	-256.11 pW	-208.92 pW	28.308 pW
$\mathbf{P_{Cin}}$	-5.4394 nW	-3.1365 nW	-1.6455 nW

Table 4.5 Full-Adder using MTCMOS with NORA logic Power Dissipation

Propagation Delay	45nm	32nm	22nm
SUM	41.837 ps	34.422 ps	31.23 ps
Cout	28.618 ps	22.087 ps	19.72 ps

Table 4.6 Full-Adder using MTCMOS with NORA logic Delay

Power Dissipation	45nm	32nm	22nm
$\mathbf{P_{CLK}}$	-9.4995 nW	-6.3081 nW	-4.2096 nW
$\mathbf{P_{CLK\_B}}$	-5.8735 nW	-4.2921 nW	-2.8996 nW
$\mathbf{P_{Vdd}}$	-1.365 µW	-2.3592 µW	-2.4015 µW
$\mathbf{P_A + P_B + P_{Cin}}$	-3.9692 nW	-3.3126 nW	-1.6563 nW
$\mathbf{P_A}$	1.8369 nW	704.33 pW	450.71 pW
$\mathbf{P_B}$	-196.8 pW	-437.33 pW	-226.68 pW
$\mathbf{P_{Cin}}$	-5.6093 nW	-3.5796 nW	-1.8803 nW

Table 4.7 Full-Adder using MTCMOS with NORA logic and high-V_t at Carry output Power Dissipation

Propagation Delay	45nm	32nm	22nm
SUM	40.556 ps	33.333 ps	29.475 ps
Cout	42.044 ps	33.148 ps	32.043 ps

Table 4.8 Full-Adder using MTCMOS with NORA logic and high-V_t at Carry output Delay

4.2 Analysis:

From Tables, we observe that:

- As we go from higher technology node to lower technology node-
  - $|P_{Vdd}|$ increases while $|P_{CLK}|$ and $|P_A + P_B + P_{Cin}|$ decreases.
  - Sum and Cout delay also decreases.

- For the same technology node but a different type of full adders:

  - $|P_{Vdd}|$
    - Dynamic CMOS logic > NORA logic > MTCMOS with NORA logic > MTCMOS with NORA logic and high-V_t at carry output

  - $|P_{CLK}|$
    - NORA logic < (MTCMOS with NORA logic, MTCMOS with NORA logic and high-V_t at carry output) < Dynamic CMOS logic

  - $|P_A + P_B + P_{Cin}|$
    - Dynamic CMOS logic > NORA logic > MTCMOS with NORA logic and high-V_t at carry output > MTCMOS with NORA logic

  - **SUM Delay**
    - MTCMOS with NORA logic > MTCMOS with NORA logic and high-V_t at carry output > NORA logic > Dynamic CMOS logic

  - **Cout Delay**
    - MTCMOS with NORA logic and high-V_t at carry output > MTCMOS with NORA logic > NORA logic > Dynamic CMOS logic

  - **Propagation Delay** = {max (SUM Delay, Cout Delay)}

(MTCMOS with NORA logic approximately equal to MTCMOS with NORA logic and high-V_t at carry output) > (Dynamic CMOS logic approximately equal to NORA logic)

CHAPTER 5
Conclusion and Future Scope

5.1 Conclusion:

Based on observations, we can conclude that:

a) $|\mathbf{P_{Vdd}}|$ i.e.; average power dissipation by DC voltage source Vdd is dominant (in order of μW) among all power dissipations (in order of nW or pW).
b) For smaller technology node $|P_{Vdd}|$ is high. And it is least for MTCMOS based circuits, for 22nm technology MTCMOS with NORA logic and high-V_t at carry output based full-adder reduces $|P_{Vdd}|$ to great extent (approximately 3 times than that of Basic Dynamic CMOS logic based full-adder).
c) $|\mathbf{P_{CLK}}|$ of Basic Dynamic CMOS logic is highest, while for NORA based logic it is lowest.
d) $|\mathbf{P_A + P_B + P_{Cin}}|$ for Basic Dynamic CMOS logic is highest, while for MTCMOS based circuits it is lowest.
e) Here we take the Clock with a 50% Duty Cycle. We can further reduce power dissipation by decreasing the duty cycle of Clock signals.
f) MTCMOS based circuits have the highest propagation delay. Since MTCMOS with NORA logic-based circuit has a great difference between SUM and Cout delay, hence MTCMOS with NORA logic and high-V_t at carry output is used such that delay difference reduces but propagation delay is unaffected and $|P_{Vdd}|$ decreases (by using high-V_t transistor at Cout for increasing Cout delay).
g) We also observe that SUM and Cout outputs are more degraded in the case of Basic Dynamic CMOS based full adder.

5.2 Future Scope:

As the technology node decreases, leakage increases due to SCE (Short-Channel effect). So, there is a scope to decrease leakage by using Carbon-nanotube FET, double gate FET, or different types of Fin-FET in place of high-k dielectric MOSFET for Full-adder implementation using NORA Logic with MTCMOS. But there might be a problem with reliability in that case.

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