Realization of Some Analog Signal Processing/Generation Circuits Employing OTRAs

A Thesis Submitted to the
Delhi Technological University
for the award of Doctor of Philosophy

in
Department of Electronics & Communication Engineering

by

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June 2022

Certificate

This is to certify that the thesis entitled **"Realization of Some Analog Signal Processing/Generation Circuits Employing OTRAs"** being submitted by **Ms. Garima (2K11/Ph.D/EC/09)** for the award of degree of **Doctor of Philosophy** in the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, is the record of students own work carried out by her under our supervision.The contents of this research work have not been submitted in part or fully to any other institute or university for the award of any degree.

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Acknowledgment

I take this opportunity to express my significant indebtedness, most profound sense of gratitude and heartiest thanks to my supervisors **Prof. Pragati Kumar** and **Prof. D. R. Bhaskar**, who kindly accepted to take me as Ph. D student and supported me with warm encouragement, patient guidance and fruitful discussions during the entire course of the research work. Their humane and warm personal approaches in all aspects, have given me the strength to carry out this research work on a steady and smooth course. I humbly acknowledge life time gratitude to them.

I would like to express my thanks to **Prof. N. S. Raghava**, HOD (ECE) and **Prof. Uma Nangia**, HOD (EE) for their kind support.

I would like to express my sincere thanks to **Prof. Raj Senani**, NSUT-Delhi and **Prof. Madhusudan Singh**, EED, DTU-Delhi, for their kind support, helpful advice and constructive suggestions.

More personally, I would like to express my sincere thanks to my colleagues **Dr. Ram Bhagat**, **Dr. Bhavnesh Jaint** EED, DTU-Delhi and **Dr. Alok Kumar Singh**, ECED, DTU-Delhi for their help and support throughout the present research work. I would also like to thank **Dr. Manoj Kumar** and **Dr. Ajishek Raj** for rendering their valuable help throughout the present work.

Also, I would like to extend my thanks to **Mr. Upendra Kumar, Mr. Jagvir**

Singh, Mr. Anil Butola, **Mr. Abhishek** and **Deepak** for providing and arranging all necessary help in Linear Integrated Circuits Lab for carrying out experimental work. I express my deep sense of gratitude to **Mr. Ashutosh Jha**, AGMATEL INDIA PVT. LTD. for arranging important measuring instruments for experimental works.

I am also grateful to all my family members who were always with me during my Ph.D. course and tolerated me.

Last, but not the least, I thank **Mother Nature** and **God Almighty** for providing me the opportunity for pursuing doctoral studies.

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List of Symbols

g_m	Transconductance
R	Resistor
C	Capacitor
I_{Bias}	Bias Current
ω	Pole Frequency
Q	Quality Factor
BW	Bandwidth
H	Voltage Gain
S	Sensitivity
Ω	Ohm
$\mho$	Mho
g_p	Parasitic Transconductance
R_p	Parasitic Resistance
C_p	Parasitic Capacitance
r_o	Output Resistance
C_o	Output Capacitance
ϕ	Phase
S^F	Stability Factor

I_D	Drain Current
V_{DS}	Drain to Source Voltage
V_{GS}	Gate to Source Voltage
V_{TH}	Threshold Voltage
μ_n	Surface Mobility
C_{ox}	Gate Oxide Capacitance per Unit Area
W	Width
L	Length

List of Abbreviations

ABB	Active Building Block
IC	Integrated Circuit
Op-Amp	Operational Amplifier
OTA	Operational Transconductance Amplifier
CC	Current Conveyor
CCII	Second Generation Current Conveyor
MOCCCII	Multiple Outputs Current Controlled Conveyor
DO-CCCII	Dual Output Current Controlled Current Conveyor
DDCC	Differential Difference Current Conveyor
FDCCII	Fully Differential Current Conveyor
DVCC	Differential Voltage Current Conveyor
CFOA	Current Feedback Operational Amplifier
FTFN	Four Terminal Floating Nullors
VDTA	Voltage Differencing Transconductance Amplifier
CDTA	Current Differencing Transconductance Amplifier
CCCCTA	Current Controlled Current Conveyor Transconductance Amplifier
DVCCTA	Differential Voltage Current Conveyor Transconductance Amplifier
CFTA	Current Follower Transconductance Amplifier

CDCTA	Current Differencing Cascaded Transconductance Amplifier
MCCTA	Modified Current Conveyor Transconductance Amplifier
MISO	Multiple-Input Single-Output
A/D	Analog to Digital Converter
D/A	Digital to Analog Converter
VM	Voltage Mode
CM	Current Mode
TRM	Transresistance Mode
TCM	Transconductance Mode
TOQSO	Third Order Quadrature Sinusoidal Oscillator
BJT	Bipolar Junction Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
CMOS	Complementary Metal Oxide Semiconductor
GC	Grounded Capacitor
LPF	Low Pass Filter
HPF	High Pass Filter
BPF	Band Pass Filter
BRF	Band Reject Filter
APF	All Pass Filter
TOSO	Third Order Sinusoidal Oscillator
CO	Condition of Oscillation
FO	Frequency of Oscillation

Chapter 1

Introduction

This thesis deals with "Realization of some analog signal processing/generation circuits employing operational transresistance amplifiers". Novel signal processing/generation circuits in voltage mode (VM) employing operational transresistance amplifiers (OTRAs) having several advantageous features not available simultaneously in circuit structures known earlier have been proposed.

Analog signal is basically a continuous time signal. Most of the signals encountered in real world are analog in nature. That is, the signals are function of a continuous variable, such as time or space, and usually take on values in a continuous range. Such signals may be processed directly by appropriate analog systems (such as filters or frequency analyzers) or frequency multipliers for the purpose of changing their characteristics or extracting some desired information.

The integrated circuit (IC) op-amp, though quite versatile, has few major limitations such as, constant and finite gain bandwidth product, slewing at high frequency (because of finite slew rate). Also, in many applications, the op-amp based designs require passive component matching constraints and, also, the number of components required is not canonic. To overcome the limitations of conventional op-amp circuits, several alternative new analog active building blocks (ABBs) have been proposed from time to time during the past four decades by researchers and circuit designers. Basically, Op-amp is a voltage controlled voltage source i.e., it has

voltage output which depends on the differential voltage available at its input terminals. Almost all the active devices implement one of the following controlled sources namely, voltage controlled voltage source (VCVS), voltage controlled current source (VCCS), current controlled voltage source (CCVS) and current controlled current source (CCCS). Based on the classification of these controlled sources, there can be four modes of operation of the circuit namely, voltage mode, current mode, transimpedance mode and transconductance mode. A very comprehensive review of numerous active building blocks, along with a unified framework for development of new active building blocks with different features, has been presented by **Biolek**, **Senani**, **Biolkova** and **Kolka** in [1].

The input source of any amplifier is never ideal, having ideally zero (for voltage source) or infinite (for current source) output resistance. Similarly, the load on any amplifier can range from very low to very high. The circuit designer must have the option of choosing from any one of the following amplifiers (controlled sources):

1. **Voltage-controlled voltage source**

   If the input source has a very low output impedance and the load impedance is very high, the amplifier must have very high input impedance (ideally infinite) and very low output impedance (ideally zero). This requirement is met by a voltage amplifier/ voltage controlled voltage source (VCVS).The active devices that come under this category have voltage as input and provide voltage output. Hence, they have a high input impedance and ideally zero output impedance. For example traditional operational amplifier, differential difference amplifier (DDA), voltage differencing buffered amplifier (VDBA), voltage differencing inverted buffered amplifier (VDIBA), etc. comes under this category.

2. **Voltage-controlled current source**

If the input source has a very low output impedance and the load impedance is very low, the amplifier must have very high input impedance as well as very high output impedance. This requirement is met by a transconductance amplifier/ voltage controlled current source (VCCS).These devices operate at an input voltage and provide current output. They have a high input resistance and high output resistance.The operational transconductance amplifier (OTA), voltage differencing transconductance amplifier (VDTA), voltage differencing current conveyor (VDCC), etc is an example of this type of active device.

3. **Current-controlled current source**

   If the input source has a very high output impedance and the load impedance is very low, the amplifier must have very low input impedance (ideally zero) and very high output impedance (ideally infinite). This requirement is met by a current amplifier/ current controlled current source (CCCS). These devices are controlled by input current and have current outputs. Hence they exhibit ideally zero input impedance and very high output impedance. The most commonly used active devices under this category is the current-conveyor (CC), current differencing transconductance amplifier (CDTA), current differencing current conveyor (CDCC), dual X current conveyor transconductance amplifier (DXCCTA), current differencing cascaded transconductance amplifier (CDCTA), current controlled transconductance amplifier (CCTA), etc.

4. **Current-controlled voltage source**

   If the input source has a very high output impedance and the load impedance is very high, the amplifier must have very low input impedance as well as a low output impedance. This requirement is meant by a transresistance amplifier/ current controlled voltage source (CCVS).Here the input is a current source while at output voltage is produced. They have ideally zero input as well as output impedance. Current differencing buffered amplifier (CDBA), current differencing differential input buffered amplifier (CDDIBA), current differencing differential output buffered amplifier (CDDOBA), current differencing op-

erational amplifier (CDOA), etc. are an example of this type of source. Operational transresistance amplifier (OTRA) is an active device that falls under this category, which has an ideally zero input and output impedances.

Over the past few years, numerous analog signal processing and generation circuits have been developed using an ABB called Operational transresistance amplifier (OTRA). OTRA is a differential current controlled voltage source characterised by ideally zero input impedance and zero output impedance. Because of the presence of virtual ground at the input terminals, the effect of parasitics is removed at the input terminals of OTRA due to which OTRA has received prominent attention in the design of filters, oscillators and non-linear analog applications. Also, its low output impedance facilitates easy cascadability. The symbolic representation of OTRA has been depicted in Fig. 1.1.

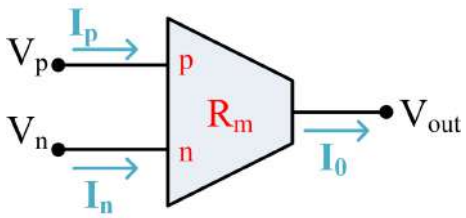


Figure 1.1: Symbolic notation of OTRA

OTRA is a three terminal active device having ideally zero input and zero output impedance. The characterizing terminal equations of an OTRA can be expressed in the matrix form as:

$$\begin{bmatrix} V_p \\ V_n \\ V_{out} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 0 & 0 & 0 \\ R_m & -R_m & 0 \end{bmatrix} \begin{bmatrix} I_p \\ I_n \\ I_{out} \end{bmatrix} \tag{1.1}$$

Thus, from equation (1.1), the output voltage (V_{out}) of the OTRA can be written

as:

$$V_{out} = R_m(I_p – I_n) \tag{1.2}$$

where R_m is transresistance gain of OTRA whose ideal value is infinite. Whenever an appropriate negative feedback is present between output and the input terminals, thus forcing the device to operate in linear region, the very high value of R_m (ideally infinite) forces the differential input currents to zero. In any real implementation, however, R_m is a function of frequency, usually represented by a single pole model, as given in equation (1.3):

$$R_m(s) = \frac{R_0}{1 + \frac{s}{\omega_0}} \tag{1.3}$$

where R_0 is dc transresistance gain and ω_0 is the angular pole frequency of first pole of OTRA.

Various Realizations of OTRA

In 1992, **Chen, Tsao** and **Chen** proposed Operational Transresistance Amplifier (OTRA) as a versatile active building block and gave its first CMOS realization [2]. The structure was based on implementing the current-differencing operation by current mirrors as shown in Fig. 1.2.

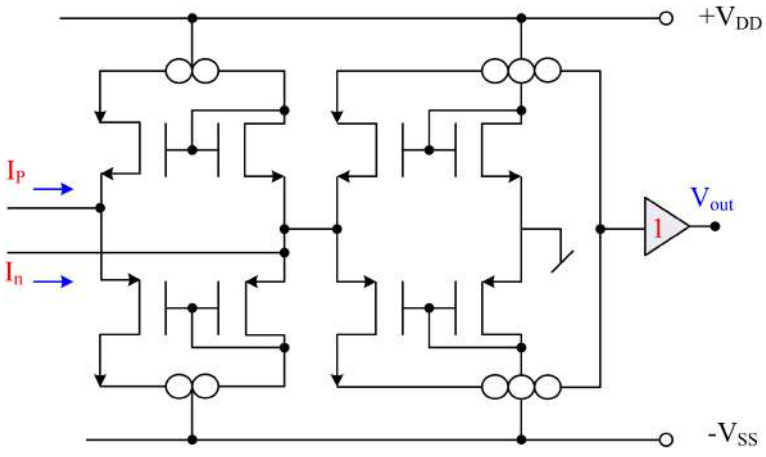


Figure 1.2: CMOS representation of OTRA proposed by Chen, Tsao and Chen [2]

On the other hand, in 1999 **Salama** and **Soliman** in [3] presented a different CMOS realization of OTRA that is based on the cascaded connection of a modified differ-

ential current conveyor architecture to provide current-differencing operation where a common source amplifier has been used to provide high gain.

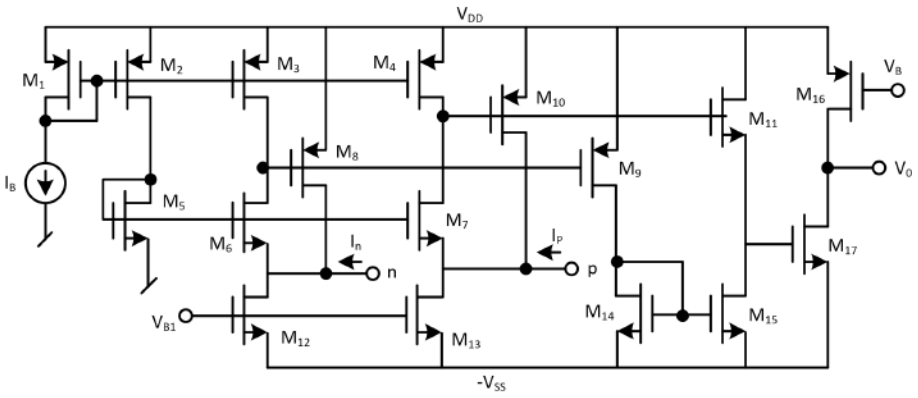


Figure 1.3: CMOS representation of OTRA presented by Salama and Soliman [3]

A bipolar representation of the OTRA has been presented by **Barthelemy, Koudobine** and **Van Landegehem** in [4]. The proposed circuit has a positive first generation current conveyor as the input stage followed by a translinear voltage follower.

Ravindran, Savla, Younus and **Ismail** in [5] have presented a low-voltage CMOS OTRA that employs low-voltage regulated cascode current mirror with a low-voltage regulated cascode load.

Duruk and **Kuntman** in [6] proposed a differential OTRA topology that can operate at very low power supply voltages where the basic input cell consists of class AB current mirror connection.

Another low voltage CMOS differential OTRA suitable for operation in sub-micron technologies has been presented by **Duruk, Gunes** and **Kuntman** in [7]. Its basic cell consists of six transistors, which form a low-voltage current mirror topology (M_1–M_6).

A structure that is most commonly used by others in realizing their OTRA based applications is the one presented by **Mostafa** and **Soliman** in 2006 [8], as shown in

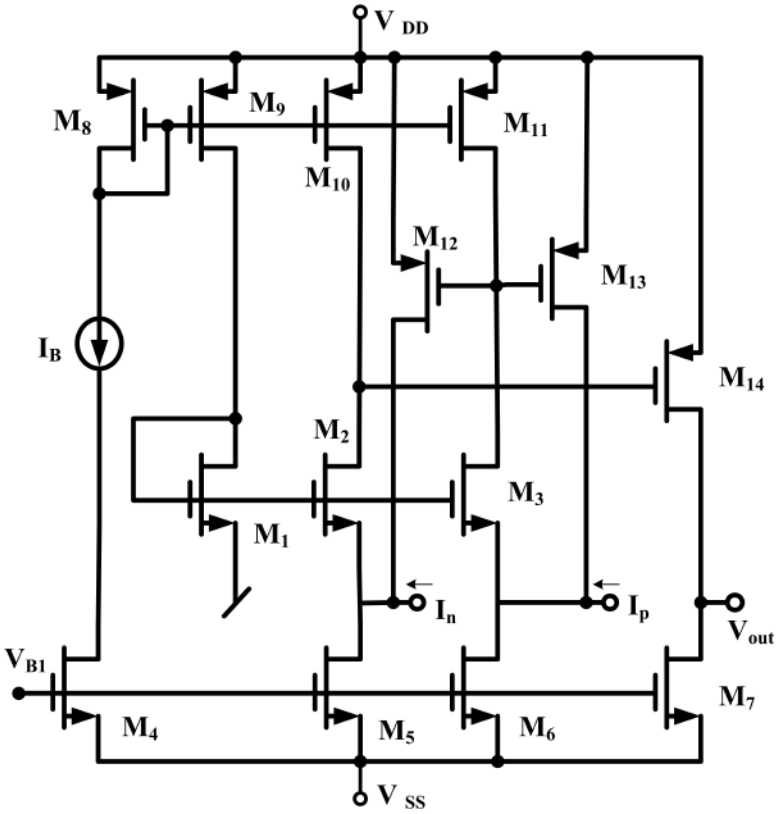


Figure 1.4: CMOS representation of OTRA [8]

Fig.1.4. It is based on the cascaded connection of the modified differential current conveyor and a common source amplifier, but comparatively, has smaller number of current mirrors than the OTRA presented in [3]. Assuming that each group of transistors (M1-M3), (M5 and M6), (M8-M11) and (M12 and M13) are matched and all the transistors operate in the saturation region, the circuit operation can be explained as follows. The current mirrors formed by (M8-M11) forces equal currents (I_B) in the transistors M1, M2 and M3 and thereby making their gate to source voltages equal and thus virtually grounding the input terminals. The current mirrors formed by the transistor pairs (M10 and M11) and (M12 and M13) provide the current differencing operation, while the common source amplifier (M14) achieves the high gain stage. The aspect ratios of the MOSFETs used in Fig. 1.4 are given in Table 1.1.

Table 1.1: Aspect ratios of MOSFETs shown in Fig. 2.8

MOSFETs	Aspect Ratio (W/L) in μm
$M_1 - M_3$, $M_{12} - M_{13}$	36/0.9
M_4, M_7	3.6/0.9
M_5, M_6	10.8/0.9
$M_8 - M_{11}$	18/0.9
M_{14}	18/0.18

The DC transfer characteristic of Fig. 1.4 is shown in Fig. 1.5. The frequency responses of magnitude and phase of the OTRA have been displayed in Fig. 1.6.

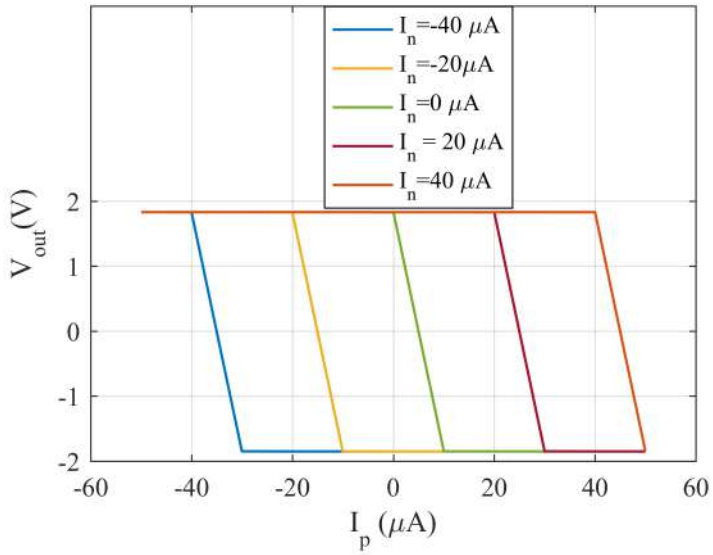
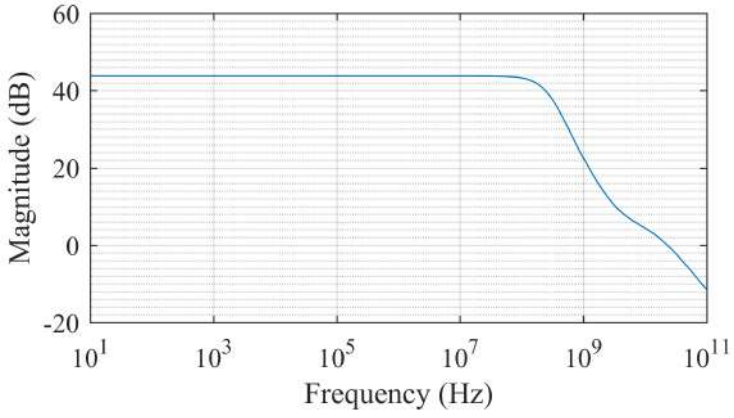
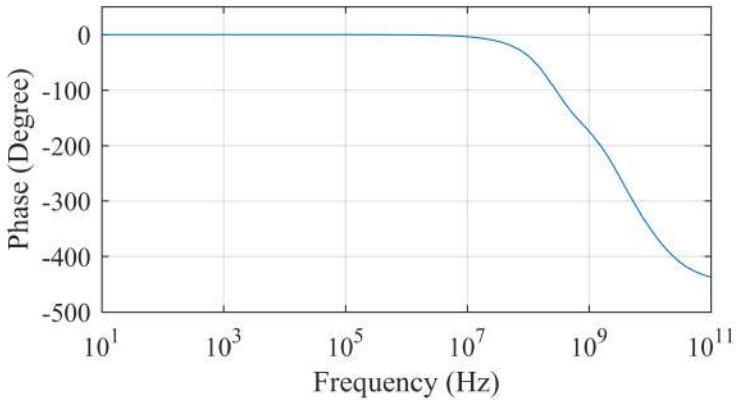


Figure 1.5: DC characteristic of the OTRA



(a)



(b)

Figure 1.6: Frequency responses of magnitude and phase of an OTRA

A high open-loop transresistance gain OTRA has been reported by **Kafrawy** and **Soliman** in [9] that is based on the same input stage as in [8] while a differential gain stage is used instead of a common source amplifier and a compensation circuit is used to compensate the difference between the two drain voltages of the transistors M_2 and M_3.

Obaid, Tayyab and **Chaudhary** in [10] have proposed a CMOS differential OTRA, that is a high open-loop gain differential OTRA employing a differential gain stage. This low-power wide-band OTRA is based upon a common source amplifier and a cascaded connection of the modified differential current conveyor (MDCC).

A modified representation of CMOS OTRA, has been presented by **Kafraway** and **Soliman** in [11], that is capable of providing two complimentary voltage outputs by employing a differential gain stage instead of the common source amplifier as the output stage as given in [8].

A new approach to design a field-programmable CMOS OTRA has been presented by **Mittal, Kapur, Markan** and **Pyara** in [12], where all the MOSFETs have been replaced by floating gate MOSFETs to make the OTRA design programmable.

Another CMOS architechture of OTRA using the sub-micron technology has been presented by **Pawade** and **Ghongade** in [13]

A gain tunable and low-power OTRA circuit based on FGMOS has been proposed by **Prasad, Gautam** and **Aggarwal** in [14] by replacing some of the MOSFETs in the conventional OTRA circuit of Mostafa and Soliman by two-input floating gate MOSFETs.

A CMOS implementation of OTRA, used in the present work apart from the CMOS implementation presented in [8] employing a current differencing unit and a translinear buffer [15] is shown in Fig. 1.7.
In Fig. 1.7, the current-differencing unit consists of two translinear voltage buffers formed by (M1-M4) and (M1,M3,M17,M18). The input terminals of both the buffers has been grounded resulting in a virtual ground at the p and n terminals. Furthermore, the cascode current mirrors formed by transistors $(M_5 - M_8)$, $(M_9 - M_{12})$, $(M_{13} - M_{16})$ and $(M_{19} - M_{23})$ provide high output impedance. The aspect ratios of MOSFETs used in Fig. 1.7 are given in Table 1.2.

Table 1.2: Aspect ratios of MOSFETs shown in Fig. 1.7

MOSFETs	Aspect Ratio (W/L) in μm
$M_1, M_2, M_{17}, M_{23}, M_{25}$	50/0.5
$M_3, M_4, M_{18}, M_{24}, M_{26}$	100/0.5
$M_5 - M_{16}$,$M_{19} - M_{22}$	3.33/0.5

The DC characteristic and frequency responses of gain and phase of the OTRA shown in Fig. 1.7 are shown in Figs. 1.8 and 1.9 respectively.

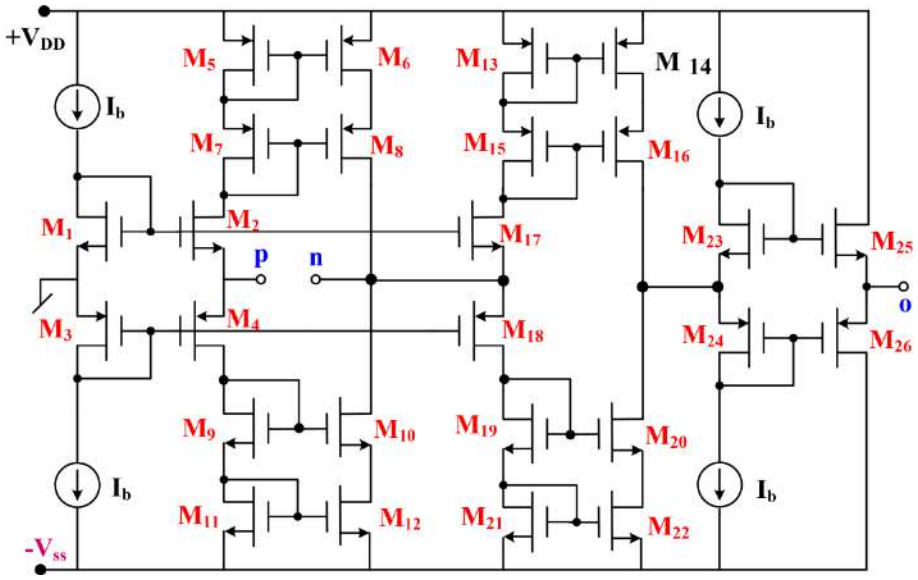


Figure 1.7: CMOS representation of OTRA derived from [15]

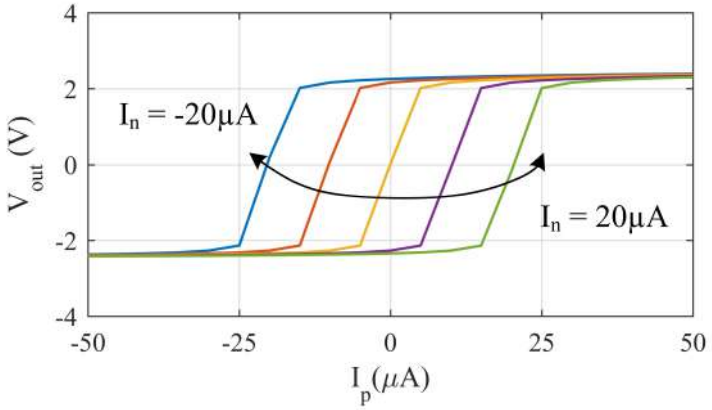
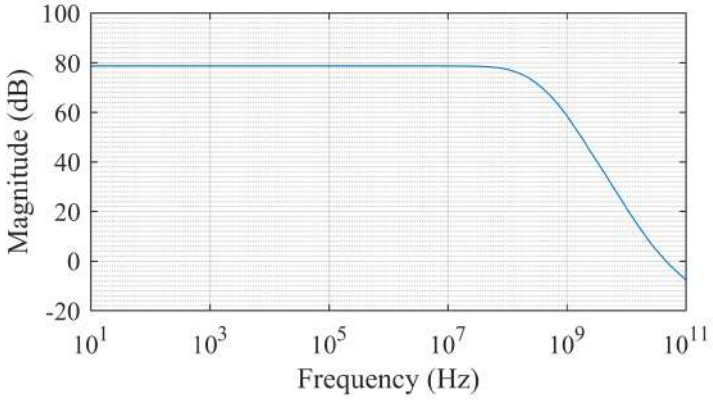
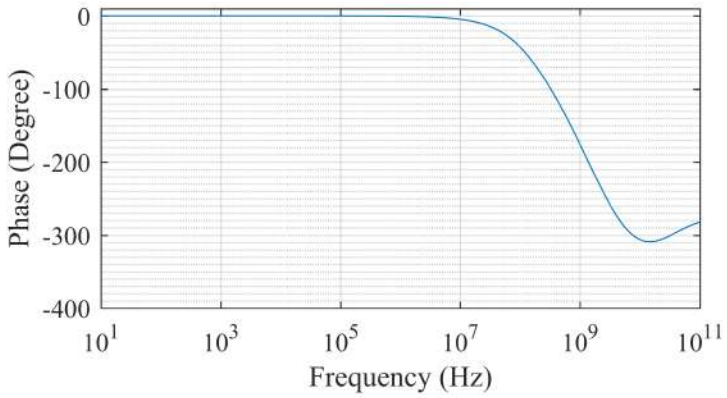


Figure 1.8: DC characteristic of the OTRA presented in [15]



(a)



(b)

Figure 1.9: Frequency responses of magnitude and phase of an OTRA of [15]

As of now, no integrated OTRA circuit has been made commercially available as an off-the-shelf IC. However, in practice, an alternate realization of OTRA is using the commercially available ICs (AD844) [16] the implementation of which has been displayed in Fig. 1.10.

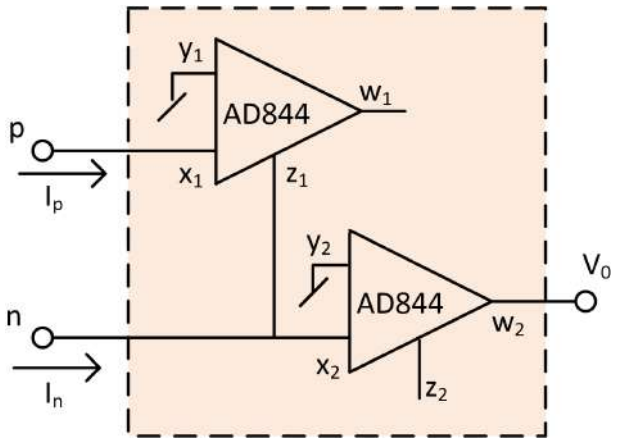


Figure 1.10: OTRA realized using commercially available CFOA ICs [16]

Various Applications of OTRA

Numerous applications of OTRA and its various derivatives in analog signal processing and generation viz filters, oscillators/quadrature oscillators, simulated impedances and various non-linear functions have been reported in [17–129]. In the area of simulated impedance realization, the OTRA based circuits known so far can be broadly

classified as grounded lossy inductance simulators [17–21], lossless grounded inductor simulators [22–27] and generalized impedance simulators [28–30, 32]. On the other hand, only one capacitance multiplier circuit using OTRA is available in the open literature [32].

OTRA has been extensively used in the realization of continuous time filters. These filters can be broadly categorised depending on the order of the filter like first order filters [31, 33–37, 130], second-order filters [19, 38–58], third and higher order filters [59–71]. Recently, some fractional order and shadow filters have also been reported using OTRA [72–76]. The available second-order filters can further be classified as single-input-single-output (SISO) [38–42], single-input-multiple-output (SIMO) [19, 44–52], multiple-input-single-output (MISO) [53–57] and multiple-input-multiple-output (MIMO)[58] type filters.

Sinusoidal oscillators using OTRA have also been a topic of extensive research as is evident from the available literature [16, 19, 77–103]. These oscillators can be classified as second order [19, 77–87, 89, 90, 93], third order [16, 88, 90–92, 94–98] and fractional order [99–101]. Multiphase sinusoidal oscillators using OTRA are also available in the literature [102, 103].

Interesting applications of the OTRA have been demonstrated in [104–113], in realizing a variety of relaxation oscillators and non-sinusoidal waveform generators.

Numerous other applications of OTRA like design of PD and PID controllers, precision rectifiers, analog multipliers, etc. have been given in [111, 114–129].

From a detailed perusal of the OTRA-based analog signal processing and generation circuits available in the open literature, it has been found that:

(i) No lossy series immittance simulator using OTRA is available in the literature.

(ii) No single OTRA-based grounded lossy inductor circuit has been reported so far which can provide independent tunability of inductance with a single resistor without affecting its equivalent resistance and also utilizing the intrinsic property of the OTRA.

(iii) No single OTRA-based capacitance multiplier circuit is available that is capable of realizing both positive as well as negative multiplication factors by changing the value of resistance used.

(iv) No single OTRA-based second order filter configuration is present that employs canonic number of passive components while fully utilising the intrinsic property of the OTRA and without imposing any component matching constraints.

(v) No third order quadrature sinusoidal oscillators based on OTRAs have been reported in the open literature so far, which can provide independent tunability of CO and FO utilizing intrinsic property of OTRA.

(vi) No single OTRA-based third order sinusoidal oscillator employing canonic number of components have been presented that can provide independent tunability of CO and FO utilizing intrinsic property of OTRA.

Thus, the main objective of this work is to add new circuits with above mentioned features to the existing repertoire of the OTRA-based analog signal processing and generation circuits while fully utilising the intrinsic property of the OTRA.

The work presented in the thesis has been organized as follows:

In **Chapter 2**, we present two new grounded lossy inductor circuits employing OTRA along with some passive components.The first configuration is a new grounded series RL simulator configuration employing single OTRA, one voltage buffer, two

capacitors and two resistors. The designed inductance can be independently tuned without affecting the equivalent resistance. The second configuration is a new single OTRA-based grounded parallel immittance simulator (GIS) which has independent control on the value of the realized inductance while fully utilising the input terminals of the OTRA.

In **Chapter 3**, a new topology of a lossless grounded capacitance multiplier circuit using an OTRA, a voltage follower (VF), one capacitor and three (virtually grounded) resistors is presented. The proposed circuit is capable of realizing both positive as well as negative capacitance multiplication factors by changing the value of resistances used.

In **Chapter 4**, new biquad filter configurations employing OTRAs have been presented. The first circuit presents a single OTRA-based second order filter configuration employing canonic number of capacitors and relatively lower number of resistors as compared to previously reported filters utilising the intrinsic property of the OTRA without imposing any component matching constraints. In addition, two new structures of SIMO type biquad filter employing OTRAs have also been presented which realize a low pass filter (LPF), high pass filter (HPF) and band pass filter (BPF). Furthermore, the realized filters can easily be modified into quadrature sinusoidal oscillators capable of generating low frequency sinusoids with fully uncoupled condition and frequency of oscillation.

Chapter 5 presents third order oscillators employing OTRAs. Two new TOQSOs employing OTRAs that can provide independent tunability of CO and FO utilizing intrinsic property of OTRA have been presented first. Afterwards, a single OTRA-based third order sinusoidal oscillator configuration with canonic number of passive components is also presented, that has independent tunability of CO and FO, under the equality of capacitance constraints.

Chapter 6 of the thesis presents a summary of the work presented and some suggestions for the further work.

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Chapter 2

Realization of Simulated Inductors

2.1 Introduction

After presenting a survey of impedance simulating circuits presented by different researchers, in this chapter, two new lossy grounded inductor simulator configurations using the intrinsic property of OTRA, are proposed.

Passive inductors, for low-intermediate frequency applications, require a large chip area for IC implementation and are characterized by low quality factor values, hence, the implementation of simulated inductors using different active building blocks (ABBs) has received much attention in open literature [1]. Also, realization of simulated lossy inductors requires lower count of active and passive components and requires less stringent component matching constraints compared to simulated lossless inductors, find numerous applications in the design of analog signal processing and signal generation circuits [2].

Since the work presented in this chapter describes the OTRA-based inductance simulator configurations, therefore, a detailed account of various OTRA based impedance simulator circuits presented earlier [3–17], is now detailed out below so that the proposed new grounded inductance simulator circuits can be put in proper perspective.

2.1.0.1 Grounded lossy inductance simulators using OTRAs

Kacar, Cam, Cicekoglu, Kuntman and **Kuntman** in [3], have reported OTRA-based four lossy inductor simulator circuits (shown in Fig. 2.1) wherein, one OTRA, two/three resistors and one capacitor have been employed. Two of these circuits (Fig. 2.1a and Fig. 2.1d) do not utilize the intrinsic property of OTRA (equality of the two input currents under the condition of negative feedback because of very large value of the transresistance gain of the OTRA) as one of the input terminals of OTRA in both of these circuits is left unutilized. Also, the realized inductance values are not independently tunable. The proposed simulators were used to realize a current-mode multifunction filter to establish the workability of the simulated inductors. PSPICE simulations using a CMOS implementation of the OTRA realized with 1.2μm MOS transistor parameters supplied by MIETEC were presented to substantiate the theoretical propositions.

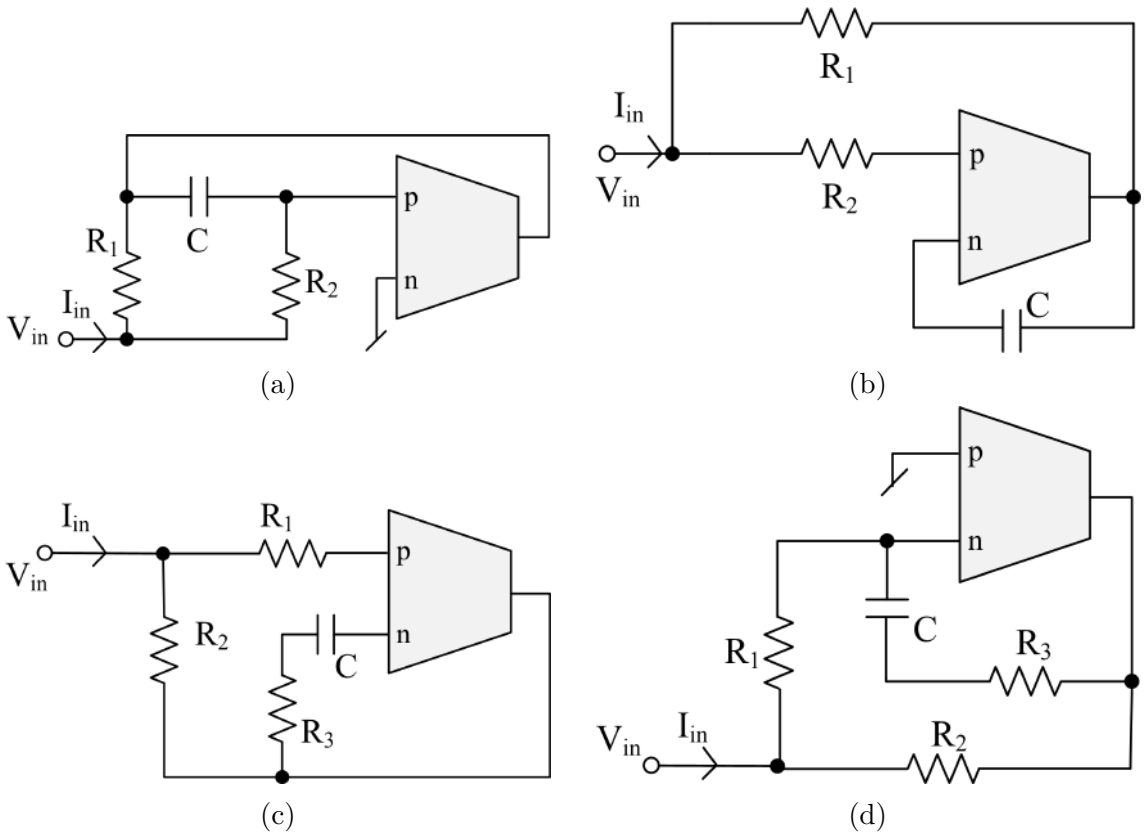


Figure 2.1: Grounded lossy immitance simulator topologies presented in [3]

In [4], **Cam, Kacar, Cicekoglu, Kuntman** and **Kuntman** have presented six lossy inductance simulator circuits. Four of these topologies have been presented in [3] also. One of the new topologies employs a single OTRA, three resistors and one capacitor while the other uses one OTRA, two resistors and two capacitors. The values of the realized inductance in these topologies do not have independent tunability feature despite employing more than the canonic number of components. As an application of the presented topologies a current-mode multifunction filter was designed and simulated in PSPICE using a CMOS OTRA.

A single OTRA-based lossy grounded inductor has been presented by **Senani, Singh, Gupta** and **Bhaskar** in [5] utilizing the pole of the transresistance gain of the OTRA along with two resistors. In this reported circuit, one of the input terminals of OTRA has been left open and the realized inductor lacks independent tunability feature. The performance of the presented circuit was verified using PSPICE simulations, wherein a CMOS OTRA implemented in 0.5μm CMOS technology parameters was used.

In [6], **Cam, Kacar, Cicekoglu, Kuntman** and **Kuntman** reported three, parallel grounded lossy inductor configurations using two OTRAs, four/five resistors and a capacitor. With appropriate selection of resistances, the third reported circuit can simulate a lossless inductance also. In two of these circuits, one of the input terminal of one of the OTRAs has been left open. The simulated inductors have independent tunability feature. Current-mode band-pass and high-pass filters were realized using these inductors. PSPICE simulation results using OTRAs realized with CFOA ICs AD844 were also presented to establish the workability of the current-mode filters and thus the simulated inductors.

Nagar and **Ghosh** reported an OTRA-based lossy inductor circuit in [7] which

employs one OTRA, two resistors and one capacitor as shown in Fig. 2.2. The proposed circuit does not utilize the intrinsic property of the OTRA as one of the input terminals of the OTRA has been directly connected to ground. Moreover,no independent tunability feature is available for the realized inductor. As an application of the presented grounded lossy inductor, a current-mode multifunction filter employing the lossy inductor was designed.

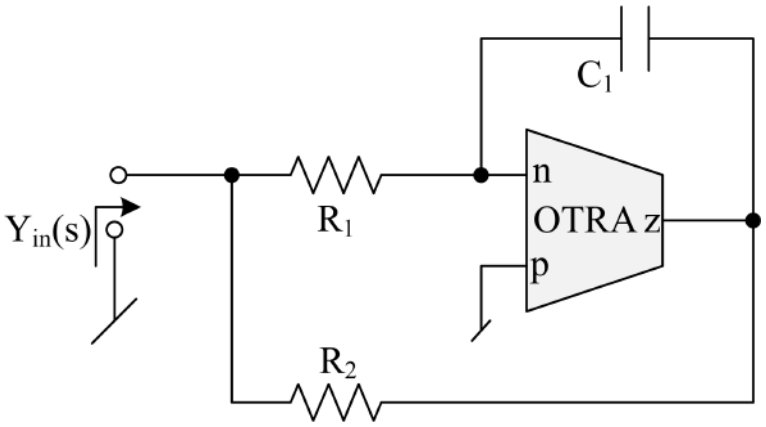


Figure 2.2: Positive lossy inductor (parallel R-L) simulator presented in [7]

2.1.0.2 Lossless grounded inductor simulators using OTRA

Kilinc, Salama and **Cam** in [8] have presented a generalized grounded negative inductance emulator employing a single OTRA, one capacitor and five resistors. Different passive component matching constraints were prescribed to realize four different lossless grounded inductor simulators from the same configuration. Of these, two circuits have full control on the condition for realization of lossless negative inductance, one circuit has independent controllability of the realized inductance, while the fourth has independent control on both, the condition of realization, as well as the value of realized inductance. The reported circuits were simulated in PSPICE using the macro-model of IC AD844 for the implementation of OTRA. The reported circuits were also experimentally tested using the two CFOA-based implementation of OTRA.

Two topologies of lossless grounded inductor employing two OTRAs, five resistors and a capacitor have been presented by **Pandey, Pandey, Paul, Singh, Sriram** and **Trivedi** in [9]. In the reported configurations, independent control of the value of realized inductance is possible. One of the reported structures does not utilize the intrinsic property of the OTRA (as one of the input terminals of the OTRA is directly connected to ground). As application examples of the presented circuits, a second order high-pass filter, a second-order band-pass filter and an LC oscillator have been realized and simulated in PSPICE. The proposed topologies were also tested experimentally using OTRAs implemented with off-the-shelf available ICs AD844.

Ghosh and **Paul** in [10] have presented a single OTRA-based negative grounded inductance simulator circuit using a single capacitor and three/four resistors as shown in Fig. 2.3. The lossless negative inductance is realized from the reported circuit if proper matching conditions on the resistances are fulfilled. The reported negative inductance was simulated in PSPICE using CMOS as well as the CFOA based implementation of OTRA. As an application of the presented negative inductance, an inductance cancellation circuit was demonstrated. For experimental verification a triangular voltage is provided as input and a square wave output current was obtained.

Pandey, Pandey, Paul, Singh, Sriram and **Trivedi**, in [11], have reported a grounded inductance simulator circuit employing a single OTRA, three equal valued resistors and two capacitors. Two application examples have been provided to justify the feasibility of the reported grounded inductance simulator circuit. A CMOS implementation of the OTRA was used in PSPICE simulations, while the two

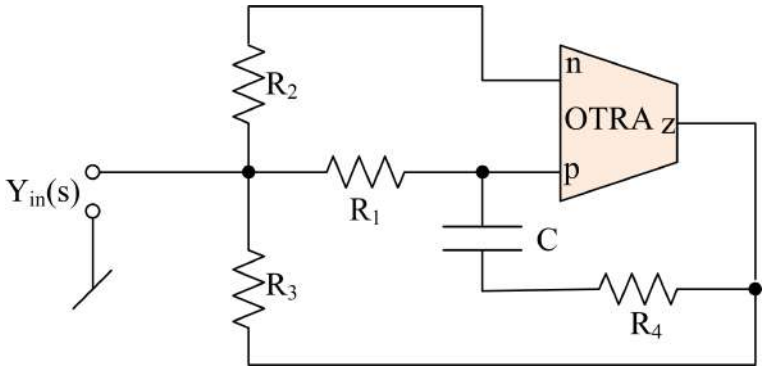


Figure 2.3: Negative grounded inductance simulator using an OTRA reported in [10]

CFOA based implementation of OTRA has been used for experimental verification.

Pramanik in [12] has presented an active inductor circuit employing two OTRAs, five resistors and one capacitor. The reported circuit requires component(s) matching constraints for the realization of a lossless inductor, and also, one of the OTRA is not fully utilized as one of its input terminal is grounded .

A negative inductance simulator circuit using a single OTRA, three resistors and one floating capacitor was reported by **Nagar** and **Paul** in [13]. For the realization of lossless negative inductor, matching constraint on resistors is prescribed. Moreover, no independent tunability feature is available to control the value of inductance using a single resistor.

From the above detailed description, it may be noted that in all the presented grounded lossless (positive/negative) inductance simulators, either the intrinsic property of OTRA has not been utilized or passive component matching constraint have been used.

2.1.0.3 Generalised impedance simulators using OTRAs

Gupta, Senani, Bhaskar and **Singh** in [14] have presented a grounded frequency dependent negative resistance (FDNR) and grounded inductance simulation circuits

employing a single OTRA, one voltage follower, two resistors and two capacitors. Two equal valued resistors are required to simulate a grounded FDNR while for the simulation of grounded inductor two equal valued capacitors are needed. The presented circuits were experimentally tested using an OTRA implemented from commercially available CFOAs (IC AD844).

A lossless grounded FDNR simulator employing a single OTRA, two resistors and three capacitors has been reported by **Nagar** and **Paul** in [15]. The presented FDNR has been used to design a single resistance controlled oscillator (SRCO) and an elliptic filter. The functionality of the reported circuit was validated through simulations using the CMOS implementation of OTRA. Post layout simulation results have also been provided. The workability of the reported FDNR circuit was tested experimentally, using an OTRA implemented with IC AD844 CFOAs.

In [16], **Gupta, Senani, Bhaskar** and **Singh** presented a generalised impedance convertor (GIC) circuit employing two OTRAs, one voltage buffer and six impedances (two equal valued impedances) which is reproduced here in Fig. 2.4. The reported circuit yields an input impedance (assuming ideal OTRA) $Z_{in} = \frac{Z_1 Z_3 Z_5}{Z_2 Z_4}$, like the traditional operational amplifier based GIC. By suitable selection of impedances Z_1 to Z_5 to be either resistive or capacitive or a combination of both, the circuit can simulate various impedances like grounded inductor, grounded FDNR, resistively variable capacitor and grounded frequency dependent negative capacitor (FDNC). An interesting feature of this circuit is that it can also simulate a generalised negative impedance convertor (GNIC) by interchanging the input terminals of the first OTRA and leaving the p-terminal open with Z_4 used in the feedback path with Z_5 connected to the n-terminal. As an application of the presented grounded inductor, a second order band-pass filter was realized and simulated in PSPICE using the two CFOAs based implementation of OTRA.

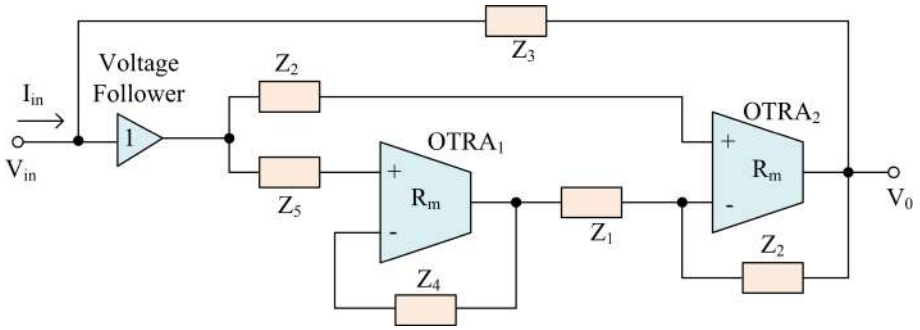


Figure 2.4: Positive generalized impedance simulator presented in [16]

A generalised lossless grounded admittance simulator using two OTRAs, one voltage follower two resistors and one capacitor has been presented by **Nagar** and **Paul** in [17]. An input admittance $Y_{in} = \frac{Y_1 Y_2}{Y_3}$ has been realized (assuming ideal OTRAs) which was used to design a lossless grounded positive inductor, lossless grounded positive FDNR and lossless grounded positive capacitance simulator/ multiplier. The workability of the reported circuits was validated using PSPICE with a CMOS implementation of OTRA.

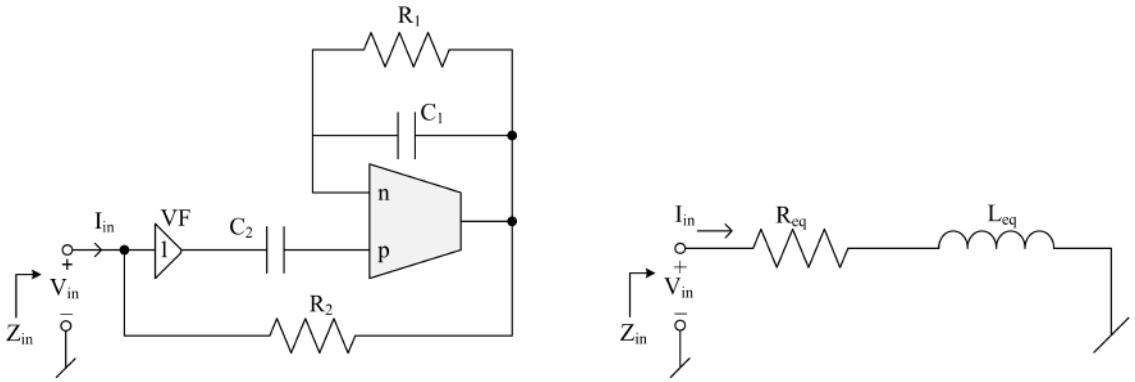
From the above description, it thus, emerges that no single OTRA-based series/parallel lossy grounded inductor circuit has been reported in the open literature so far that can provide independent tunability of inductance with a single resistor without affecting its equivalent resistance and utilizing the intrinsic property of the OTRA.

Thus, in this chapter, we propose two new grounded lossy inductor simulator circuits employing a single OTRA along with some passive components. The first configuration uses a single OTRA, one voltage buffer, two resistors and two capacitors to simulate a grounded series lossy inductor. Although, a matching constraint is needed for the realization of grounded lossy inductor, the values of the realized inductance in the proposed circuit can be varied independently without changing the values of the equivalent simulated resistance. An application example has also been presented, using the proposed circuit to validate the theoretical propositions.

The second configuration of this chapter presents a grounded parallel RL simulator configuration employing a single OTRA, five resistors and only one capacitor. In this circuit also, the designed value of inductance can be independently tuned without affecting the equivalent simulated resistance value.

2.2 Grounded Series RL Simulator Using OTRA[1]

In this section, a series grounded lossy inductor configuration is presented. The proposed circuit employs only a single OTRA, one voltage buffer, two resistors and two capacitors which is displayed in Fig. 2.5a and its passive equivalent circuit has been demonstrated in Fig. 2.5b.



(a) (b)

Figure 2.5: (a) Proposed grounded series RL-Simulator (b) Its passive equivalent

Assuming ideal OTRA and VF, circuit analysis of Fig. 2.5a yields the following input impedance:

$$Z_{in} = \frac{V_{in}}{I_{in}} = \frac{sC_1R_1R_2 + R_2}{1 + sR_1\left(C_1 - C_2\right)} \tag{2.1}$$

Now, if we consider $C_1 = C_2$, equation (2.1) reduces to:

$$Z_{in} = \frac{V_{in}}{I_{in}} = sC_1R_1R_2 + R_2 \tag{2.2}$$

[1]The material presented in this section has been published in: Garima, Pragati Kumar and D. R. Bhaskar, "Single OTRA-Based Grounded Series Lossy Simulator Configuration" In 2021 3rd International Conference on Advances in Computing, Communication Control and Networking (ICACCCN), pp.1159-1163, IEEE, 2021.

From equation (2.2), it is clear that the circuit of Fig. 2.5a simulates a grounded series lossy inductor. The equivalent values of realized inductance and resistance are given as:

$$\begin{aligned} L_{eq} &= C_1 R_1 R_2 \\ R_{eq} &= R_2 \end{aligned} \tag{2.3}$$

From equations (2.3), it may be observed that for constant value of R_{eq}, the realized value of L_{eq} can be controlled independently through virtually grounded resistor R_1.

2.2.0.1 Realization of MOS Voltage Follower

The implementation of the voltage follower structure [18] has been shown in Fig. 2.6 which employs two NMOS transistors operating in saturation region.

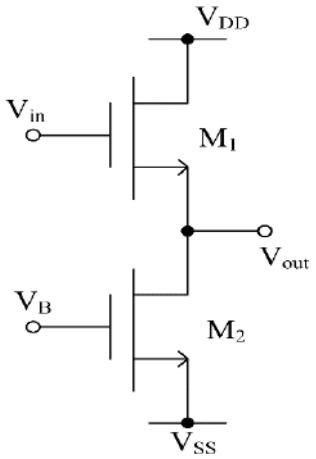


Figure 2.6: MOS implementation of VF [18]

2.2.0.2 Non-Ideal Analysis

Because of non-idealities inherent in a real OTRA, the behaviour of the simulated lossy series grounded inductor may be affected under non-ideal conditions. Therefore, we have examined the proposed circuit by using a non-ideal model of the OTRA

proposed in [19], given as under:

$$R_m(s) = \frac{R_0}{1 + \frac{s}{\omega_0}} \tag{2.4}$$

For frequencies much larger than ω_0, $R_m(s)$ reduces to:

$$R_m(s) = \frac{1}{sC_p}, \quad where \quad C_p = \frac{1}{R_0\omega_0} \tag{2.5}$$

Using the non-ideal model of OTRA as given in equation (2.5), the non-ideal input impedance for the circuit of Fig. 2.5a, may be written as:

$$Z_{in}^{/} = R_2 + \frac{sC_1R_1R_2}{1 + sC_pR_1} \tag{2.6}$$

As observed from equation (2.6), the ideal input impedance has been affected because of the presence of OTRA parasitics. The passive equivalent of the non-ideal series RL circuit is given in Fig. 2.7.

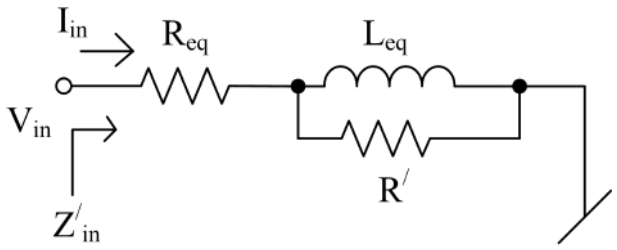


Figure 2.7: Non-ideal equivalent circuit of the proposed grounded series RL

From Fig. 2.7, it may be observed that due to parasitic pole of an OTRA, an additional resistance has been introduced in parallel with the equivalent inductor. The values of the equivalent impedances as shown in Fig. 2.7 (R_{eq}, L_{eq} and $R^{/}$) have been given in equation (2.7).

$$\begin{aligned} R_{eq} &= R_2 \\ L_{eq} &= C_1R_1R_2 \\ R^{/} &= \tfrac{R_2C_1}{C_p} \end{aligned} \tag{2.7}$$

From equation (2.7), it may be noted that, the non-ideal equivalent circuit as shown in Fig. 2.7, reduces to the ideal equivalent circuit as shown in Fig. 2.5b as the value of C_p for an OTRA is very small, and also the value of R_0 is very high (ideally infinite) which alleviate the parasitic effect.

2.2.0.3 Simulation Results

To validate the functionality of the proposed lossy series inductance simulator circuit, the circuit shown in Fig. 2.5a has been tested through PSPICE using OTRA [20] implemented in CMOS using 0.18μm technology parameters. The CMOS implementation of OTRA used in the simulations has been reproduced in Fig. 2.8 and the aspect ratios of various MOSFETs used have been provided in Table 2.1.

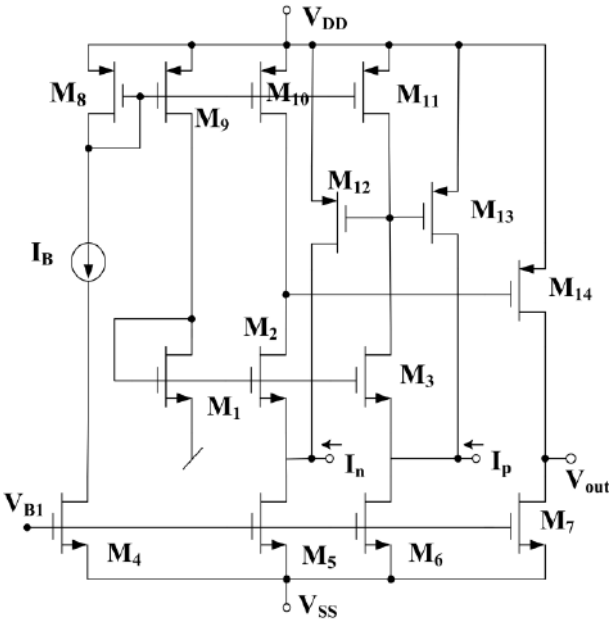


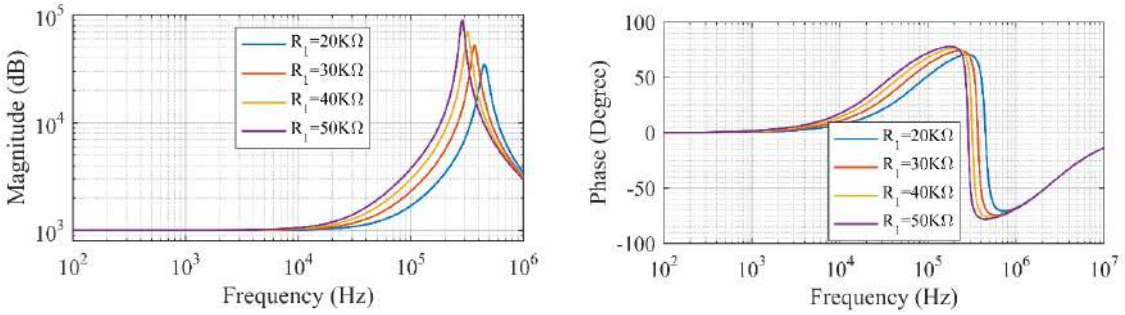
Figure 2.8: CMOS Realization of OTRA [20]

Table 2.1: Aspect ratios of MOSFETs shown in Fig. 2.8

MOSFETs	Aspect Ratio (W/L) in μm
$M_1 - M_3,\ M_{12} - M_{13}$	36/0.9
M_4, M_7	3.6/0.9
M_5, M_6	10.8/0.9
$M_8 - M_{11}$	18/0.9
M_{14}	18/0.18

The power supply voltages (V_{DD} and V_{SS}) for the Fig. 2.8 were taken as ±1.85V. The bias current (I_B) and bias voltage (V_{B1}) of CMOS OTRA were taken as 18μA and 0.36V respectively.

The circuit of Fig. 2.5a has been validated by performing the frequency and time response simulations. The passive components values were chosen as $R_1 = 50\text{k}\Omega$, $R_2 = 1\text{k}\Omega$ and $C_1 = C_2 = 100\text{pF}$ resulting in $R_{eq} = 1\text{k}\Omega$ and $L_{eq} = 5\text{mH}$. The frequency responses of magnitude and phase of input impedance, for different values of resistor R_1 (20kΩ – 50kΩ) have been displayed in Fig. 2.9a and Fig. 2.9b respectively.



(a) (b)

Figure 2.9: (a) Magnitude response of simulated impedance (b) Phase response of simulated impedance

From Fig. 2.9a , it can be observed that the lossy inductor is behaving as a resistor in the lower frequency range, while in the higher frequency range it acts as an inductor. The time responses of input current and voltage of lossy inductor have also been demonstrated in Fig. 2.10 when the input voltage was set at 100mV at 100 kHz.

2.2.0.4 Application Example

We now present an application example of the proposed series lossy grounded inductor simulator circuit of Fig. 2.5a, in the realization of a voltage mode second-order

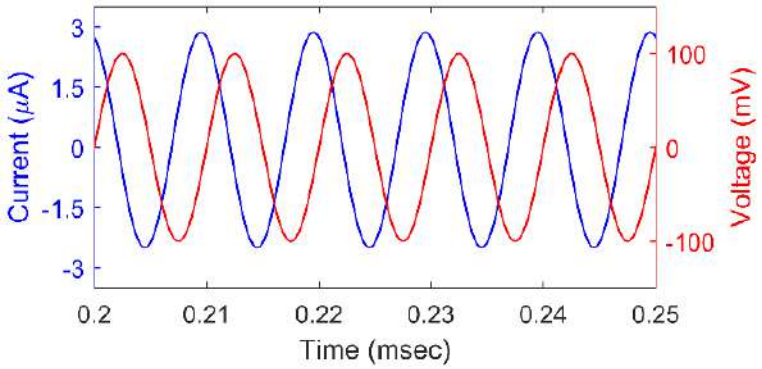


Figure 2.10: Transient voltage and current responses of simulated impedance

low pass filter which is shown in Fig. 2.11.

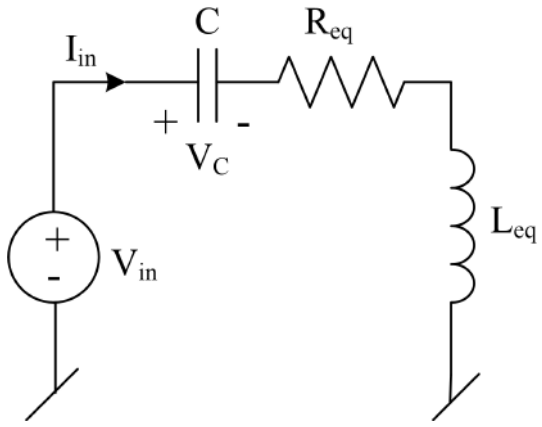


Figure 2.11: Voltage-mode LPF circuit as an application of the proposed grounded series RL simulator

Assuming ideal OTRA, the transfer function of the LPF is found as:

$$\frac{V_C(s)}{V_{in}(s)} = \frac{\frac{1}{L_{eq}C}}{s^2 + s\left(\frac{R_{eq}}{L_{eq}}\right) + \frac{1}{L_{eq}C}} \tag{2.8}$$

The expressions for L_{eq} and R_{eq} are given in equation (2.3).

Based on the model circuit of LPF shown in Fig. 2.11, the workability of the proposed grounded lossy inductor is verified. The LPF is designed using the proposed lossy inductor as shown in Fig. 2.12.

It may be noted that the output voltage V_C, shown in Fig. 2.11, has been taken at

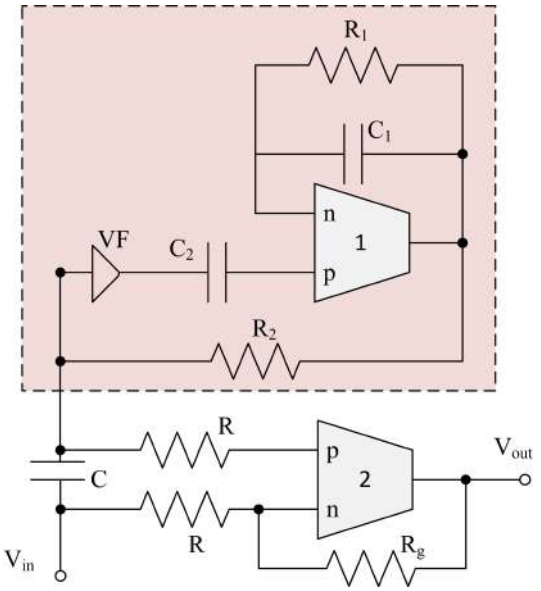


Figure 2.12: Simulated inductor based LPF circuit

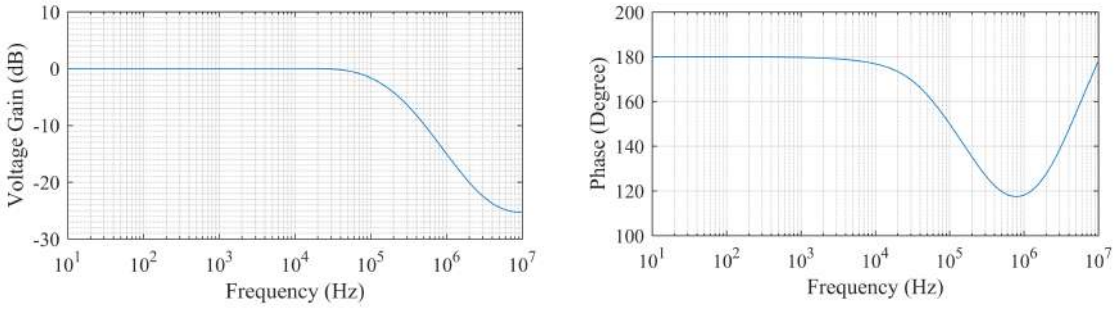
the output terminal of the second OTRA, which has been used to convert the floating voltage V_C to a grounded referred voltage available at a low impedance node. The circuit of Fig. 2.12 can provide a voltage gain also. From a straight forward analysis (assuming ideal OTRAs), the transfer function of the circuit of Fig. 2.12 is obtained as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{R_g}{CC_1R_1R_2R}}{s^2 + \frac{s}{C_1R_1} + \frac{1}{CC_1R_1R_2}} \tag{2.9}$$

which represents a second-order LPF. The filter parameters, namely, pole frequency (ω_0) and pole quality factor (Q_0) of the LPF can be given by:

$$\omega_0 = \frac{1}{\sqrt{CC_1R_1R_2}} \; and \; Q_0 = \frac{1}{R_2}\sqrt{\frac{C_1R_1R_2}{C}} \tag{2.10}$$

The LPF circuit was simulated in PSPICE using the proposed series RL simulator of Fig. 2.12, for a nominal pole frequency of 159 kHz, for which passive components were selected as: C = 1nF, R_1 = 1kΩ, R_2 = 1kΩ and $C_1 = C_2$ = 1nF. The magnitude and phase response of LPF have been demonstrated in Fig. 2.13. The simulated value of pole frequency is found to be 151kHz.



(a) (b)

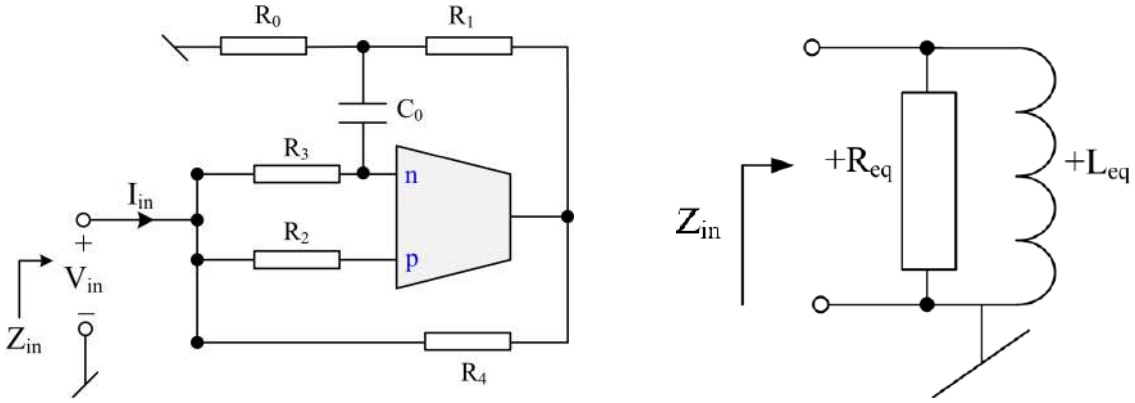
Figure 2.13: (a) Magnitude response of LPF (b) Phase response of LPF

The above simulation results, thus, validate the functionality of the proposed series grounded lossy inductor simulator circuit of Fig. 2.5a.

2.3 Grounded Parallel Lossy Inductor Simulator Using OTRA[2]

In the preceding section, a series RL simulator circuit has been presented. In this section, we present another grounded immittance simulator (parallel lossy inductor) circuit which employs only a single OTRA, five resistors and a virtually grounded capacitor. The proposed circuit and its passive equivalent circuit are shown in Fig. 2.14.

Using the terminal relationships of an OTRA ($V_0 = R_m\ (I_p – I_n)$), and assuming



(a) (b)

Figure 2.14: (a) Proposed grounded lossy inductor circuit (b) Passive Equivalent of the proposed circuit.

$R_m = \infty$, a routine circuit analysis of Fig. 2.14a yields the input impedance as:

$$\frac{V_{in}}{I_{in}} = Z_{in} = \frac{sL_{eq}R_{eq}}{sL_{eq} + R_{eq}} \tag{2.11}$$

$$where\ L_{eq} = \left(\frac{C_0R_2R_3R_4}{R_2 - R_3}\right)\frac{1}{\left(1 + \frac{R_1}{R_0}\right)}\ \ and\ \ R_{eq} = \frac{R_4}{\left(\frac{R_2+R_4-R_1}{R_2} + \frac{R_1+R_4}{R_3}\right)} \tag{2.12}$$

From equation (2.12), it can be seen that the value of inductance of the proposed circuit can be independently varied through a grounded resistor R_0 without disturbing the equivalent resistance. Inductance value can also be controlled independently

[2]The material presented in this section has been published in: D. R. Bhaskar, Garima and Pragati Kumar "Single operational transresistance amplifier-based grounded resistance-controlled synthetic inductor configuration" International Journal of Circuit Theory and Applications, 2022.

by adjusting the value of virtually grounded capacitor.

The proposed lossy inductor circuit can also be configured as a lossless negative inductor with the following conditions:

$$R_2 = R_4 = R = \frac{R_3}{2} = \frac{R_1}{5} \tag{2.13}$$

Substituting the above conditions in equation (2.11), then the equation (2.11) reduces to:

$$\frac{V_{in}}{I_{in}} = Z_{in} = s\left(\frac{-2C_0R^2}{1+\frac{5R}{R_0}}\right) = sL_{lossless} \tag{2.14}$$

where $L_{lossless} = \frac{-2C_0R^2}{1+\frac{5R}{R_0}}$

From equation (2.14), it can be observed that in this case also, the lossless negative inductor can be independently controlled by the grounded resistor R_0.

2.3.1 Non-Ideal Analysis

In practice, nonidealities of OTRA affect the ideal characteristics. The nonideal behavior of the proposed simulated grounded lossy inductor has been examined by using a nonideal model of the OTRA implemented with CFOAs (IC AD844) as shown in Figure 2.15.

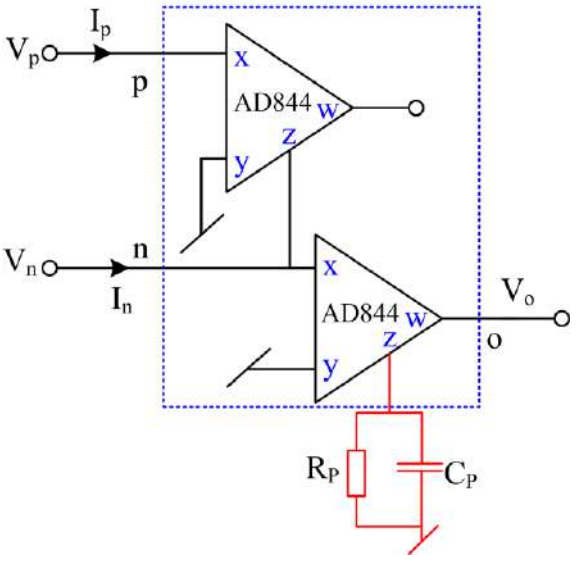


Figure 2.15: Non-ideal model of OTRA [19]

In deriving the nonideal model, we have neglected the parasitic resistances associated with X-terminals of both the CFOAs. Simple circuit analysis of the circuit shown in Figure 2.15 shows that:

$$V_0 = (I_p - I_n)\left(\frac{R_p}{sC_pR_p + 1}\right) \tag{2.15}$$

Using equation (2.15), the nonideal input admittance of the proposed lossy grounded inductor can be written as:

$$Y_{in} = \frac{1}{Z_{in}} = \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_4}\left(\frac{1}{R_3} - \frac{1}{R_2}\right)\left(\frac{R_0 + R_1 + sC_0R_0R_1}{\frac{1}{R_m}(R_0 + R_1 + sC_0R_0R_1) + sC_0R_0}\right) \tag{2.16}$$

where $R_m(s) = \left(\frac{R_p}{sC_pR_p+1}\right)$

For the frequencies much larger than $\left(\frac{1}{C_pR_p}\right)$, $R_m(s)$ reduces to:

$$R_m(s) \approx \frac{1}{sC_p} \tag{2.17}$$

Therefore, the nonideal input admittance can be written as:

$$Y_{in} = \frac{1}{Z_{in}} = \frac{1}{R_2} + \frac{1}{R_3} + \frac{1}{R_4} + \frac{1}{R_4}\left(\frac{1}{R_3} - \frac{1}{R_2}\right)\left(\frac{R_0 + R_1 + sC_0R_0R_1}{sC_p(R_0 + R_1 + sC_0R_0R_1) + sC_0R_0}\right) \tag{2.18}$$

From Equation (2.18), it is clear that the input admittance of the proposed circuit has been affected due to the presence of nonidealities of the OTRA. The nonideal input admittance approaches to its ideal expression given in equation (2.12) as the value of C_p tends to zero.

2.3.1.1 Application Examples of the proposed parallel lossy inductor

To show the usability of the lossy inductor structure, a voltage mode second order high pass filter (HPF) and band pass filter (BPF) have been designed using the proposed circuit of Fig. 2.14a. The realized HPF and BPF using grounded lossy

inductor circuit have been shown in Fig. 2.16.

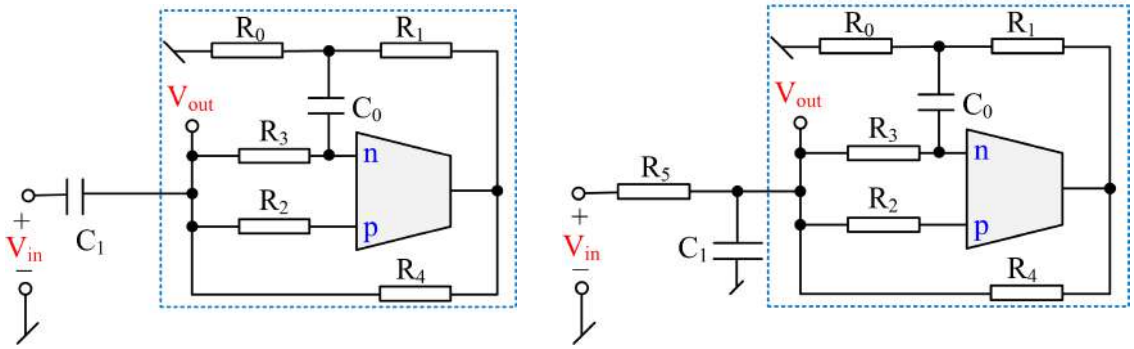


Figure 2.16: Realization of (a) HPF and (b) BPF utilizing the proposed grounded lossy inductor

Assuming ideal OTRA, the transfer function of HPF can be expressed as:

$$\frac{V_{out(s)}}{V_{in(s)}} = \frac{s^2 R_{eq} L_{eq} C_1}{s^2 R_{eq} L_{eq} C_1 + s L_{eq} + R_{eq}} \tag{2.19}$$

where L_{eq} and R_{eq} have been taken from equation (2.12).

The filter parameters, namely, pole frequency (ω_0) and pole quality factor (Q_0) of the HPF can be given by:

$$\omega_0 = \frac{1}{\sqrt{L_{eq} C_1}} \; and \; Q_0 = R_{eq} \sqrt{\frac{C_1}{L_{eq}}} \tag{2.20}$$

The transfer function of BPF shown in Fig. 2.16b has also been evaluated assuming ideal OTRA and can be expressed as:

$$\frac{V_{out(s)}}{V_{in(s)}} = \frac{\frac{s}{C_1 R_5}}{s^2 + s\left(\frac{R_4 R_5 (R_2+R_3) + R_2 R_3 (R_4+R_5) + R_1 R_5 (R_2-R_3)}{C_1 R_2 R_3 R_4 R_5}\right) + \frac{(R_2-R_3)(R_0+R_1)}{C_0 C_1 R_0 R_2 R_3 R_4}} \tag{2.21}$$

The expressions of the pole frequency and bandwidth (BW) of the BPF can be

written as:

$$\omega_0 = \sqrt{\frac{(R_2-R_3)(1+\frac{R_1}{R_0})}{C_0C_1R_0R_2R_3R_4}}$$
$$BW = \frac{R_4R_5(R_2+R_3)+R_2R_3(R_4+R_5)+R_1R_5(R_2-R_3)}{C_1R_2R_3R_4R_5} \quad (2.22)$$

From equation (2.22), it is observed that both pole frequency and BW of BPF can be controlled independently i.e., ω_0 can be varied through R_0 and/or C_0 and BW can be adjusted through resistor R_5.

2.3.2 Simulation and Experimental Results

2.3.2.1 Simulation Results

For the validation of the proposed lossy parallel RL circuit displayed in Fig. 2.14a, CMOS OTRA as shown in Fig. 2.17 has been used. The CMOS OTRA has been implemented in 0.18μm with TSMC technology parameters. The power supply voltages used were $\pm$ 2.5V. The bias current (I_B) of OTRA was taken as 40μA. The aspect ratios of the MOSFETs used in Fig. 2.17 have been given in Table 2.2.

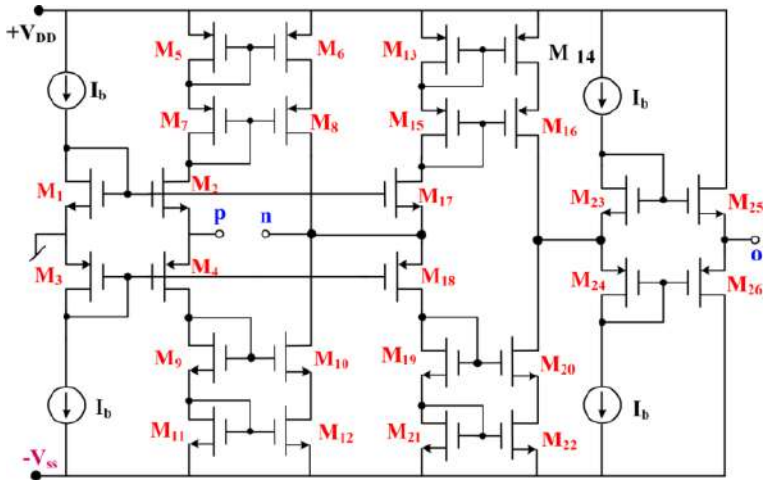


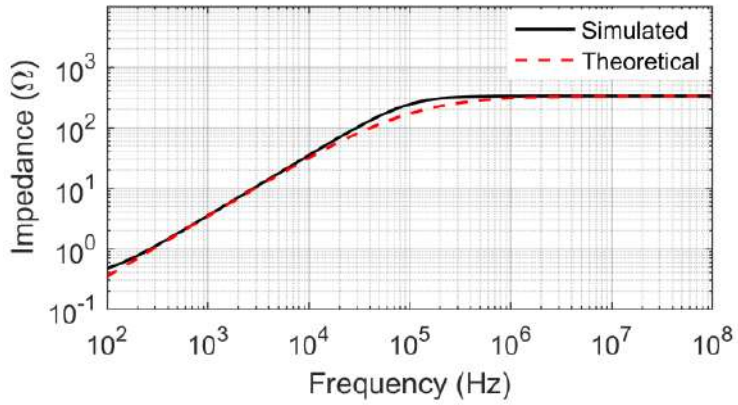
Figure 2.17: CMOS Realization of OTRA [21]

The passive components values for the simulation of lossy inductor were used as: $R_1 = R_3 = R_4 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, $R_0 = 10\text{k}\Omega$ and $C_0 = 100\text{pF}$, resulting in L_{eq} and

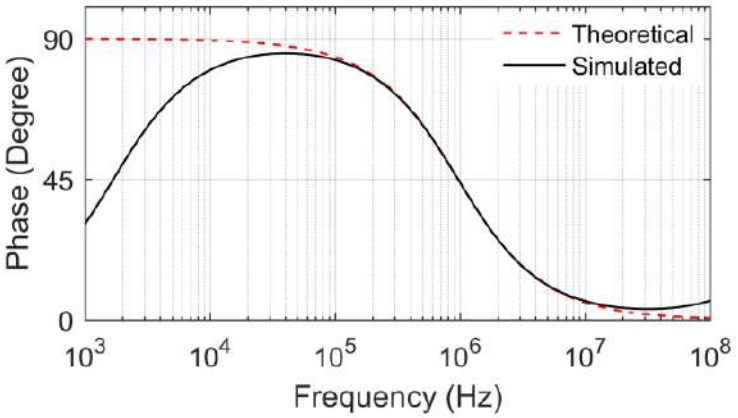
Table 2.2: Aspect ratios of MOSFETs shown in Fig. 2.17

MOSFETs	Aspect Ratio (W/L) in μm
$M_1, M_2, M_{17}, M_{23}, M_{25}$	50/0.5
$M_3, M_4, M_{18}, M_{24}, M_{26}$	100/0.5
$M_5 - M_{16}$,$M_{19} - M_{22}$	3.33/0.5

R_{eq} as 101μH and 333Ω respectively. The simulated and theoretical magnitude and phase responses of the proposed lossy inductor have been displayed in Fig. 2.18.



(a)

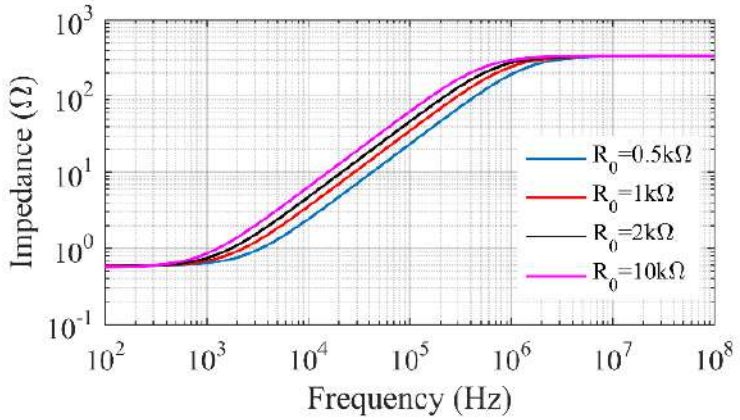


(b)

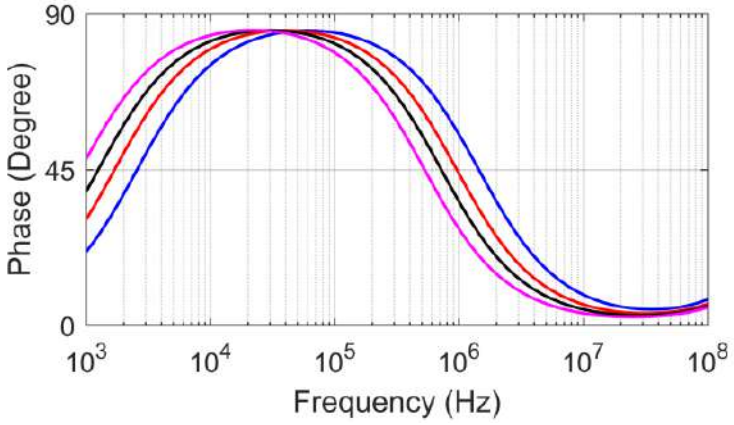
Figure 2.18: (a) Simulated Magnitude Response of the proposed grounded lossy inductor (b) Simulated Phase Response of the proposed grounded lossy inductor

The variations in magnitude and phase of the proposed lossy inductor have been demonstrated by varying resistor R_0 from 0.5kΩ - 10kΩ and the results have been displayed in Fig. 2.19.

The equivalent inductance of the proposed lossy inductor was also varied during



(a)

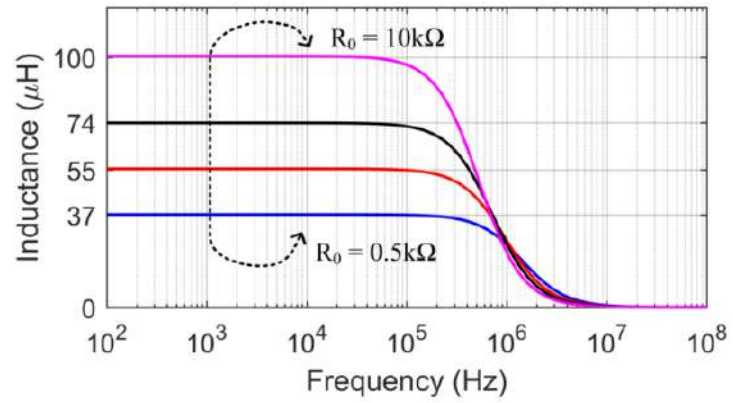


(b)

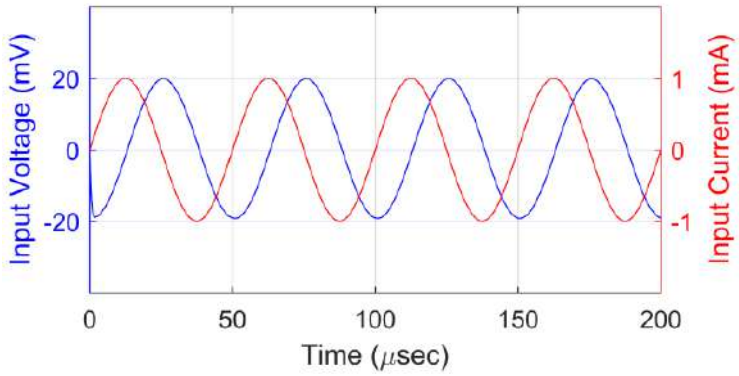
Figure 2.19: (a) Variation in magnitude of the proposed grounded lossy inductor (b) Variation in phase of the proposed grounded lossy inductor

the simulations for which, resistor R_0 was varied with the values 0.5kΩ, 1kΩ, 2kΩ and 10kΩ and correspondingly, the equivalent inductance values were obtained as 37.145μH, 55.503μH, 73.865μH and 100.581μH and the results have been shown in Fig. 2.20a. The input voltage and current transient responses of proposed lossy inductor have also been demonstrated for which the input current was set to 2mA peak to peak at 20kHz with $R_0 = 20$kΩ. The transient responses of input current and voltage have been demonstrated in Fig. 2.20b.

From Fig. 2.18, it can be seen that the simulated responses are in good agreement with the theoretical responses. From Fig. 2.19, it can be observed that by



(a)

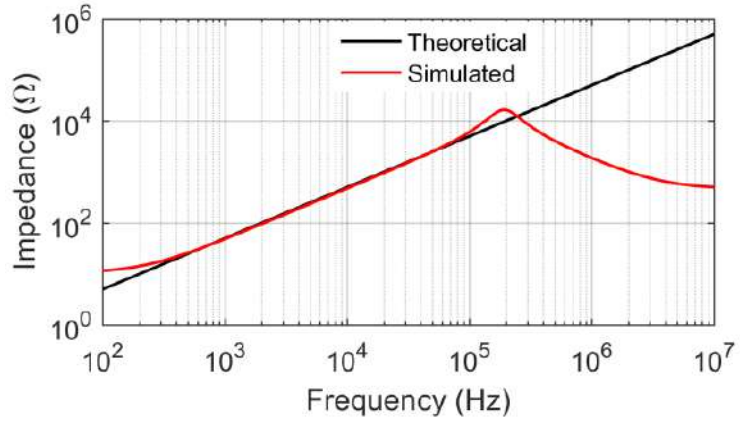


(b)

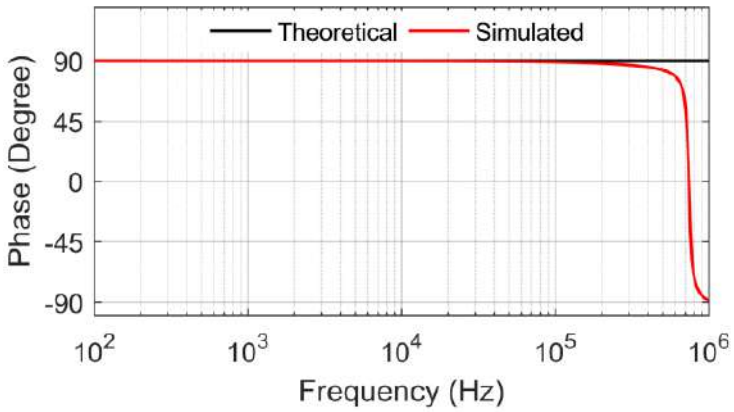
Figure 2.20: (a) Variation in equivalent inductance of the proposed grounded lossy inductor (b) Input transient current and voltage of the proposed grounded lossy inductor

varying the value of resistance R_0, only the value of equivalent inductance is changing while, the value of equivalent resistance remains constant. Fig. 2.20a shows that the equivalent inductance varies with the variation in the value of R_0. From the transient responses of the input current and voltage shown in Fig. 2.20b, it can be noticed that there is a phase difference between the current and voltage at the input terminal as should exist for a lossy inductor.

For the realization of lossless inductor, passive components of the circuit of Fig. 2.14a were chosen as: R_1=50kΩ,R_3 = 20kΩ, $R_2 = R_4$ = 10kΩ, R_0 = 2kΩ and C_0 = 100pF which results L_{eq} = -0.8mH. The simulated and theoretical magnitude and phase responses of the grounded negative lossless inductor have been displayed in Fig. 2.21.



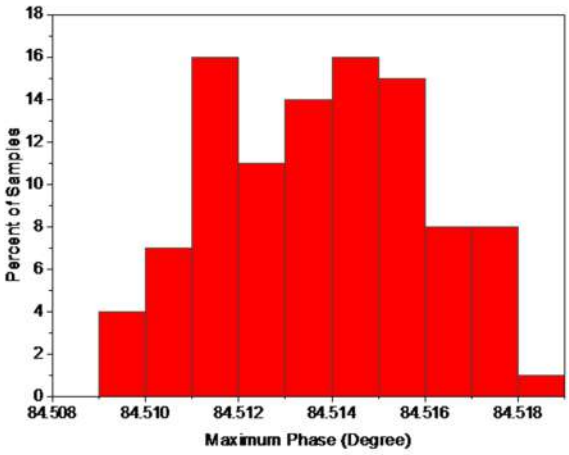
(a)



(b)

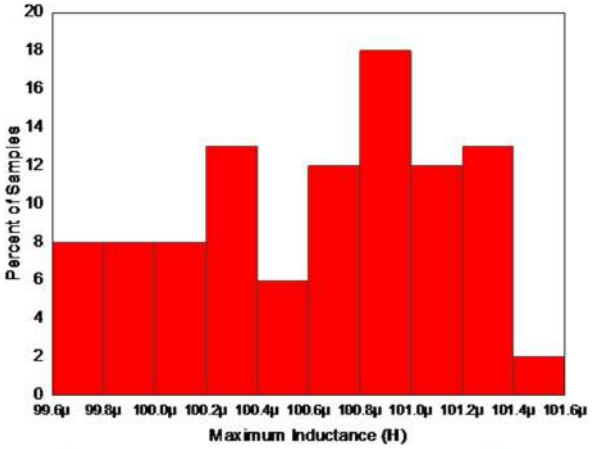
Figure 2.21: (a) Simulated and theoretical magnitude responses of the proposed negative lossless inductor (b) Simulated and theoretical phase responses of the proposed negative lossless inductor

Monte-Carlo and temperature analyses have also been carried out to justify the robustness of the simulated lossy inductor. To measure the maximum variation in impedance and phase of the lossy inductor circuit, the Monte-Carlo analysis has been performed for 100 times by varying the resistor R_0 with 10% tolerance. The histograms of the respective simulations have been shown in Fig. 2.22.



n samples	= 100	10th %file	= 84.5107
n divisions	= 10	Median	= 84.5136
Mean	= 84.5137	90th %file	= 84.5167
Sigma	= 0.002222584	Maximum	= 84.5167
minimum	= 84.5091	3*sigma	= 0.00667753

(a)



n samples	= 100	10th %file	= 9.98228e-005
n divisions	= 10	Median	= 0.000100738
Mean	= 0.000100635	90th %file	= 0.000101269
Sigma	= 5.26457e-007	Maximum	= 0.000101417
minimum	= 9.96289e-005	3*sigma	= 1.57969e-006

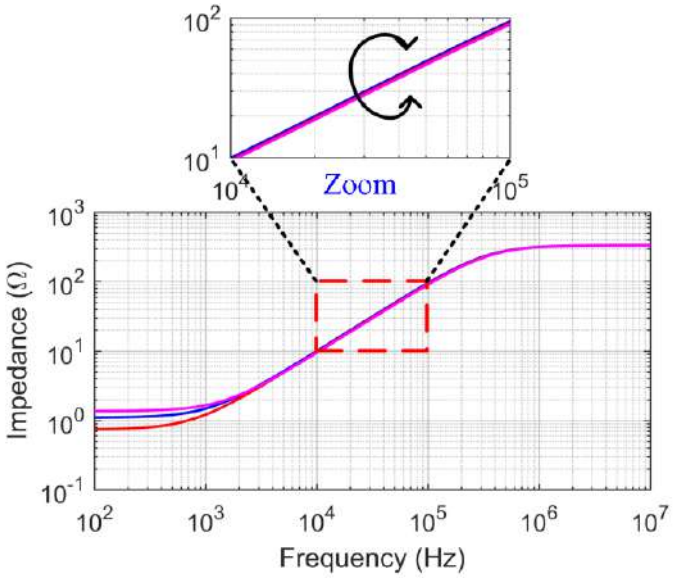
(b)

Figure 2.22: (a) Histogram of maximum phase of the proposed grounded lossy inductor (b) Histogram of maximum inductance of the proposed grounded lossy inductor

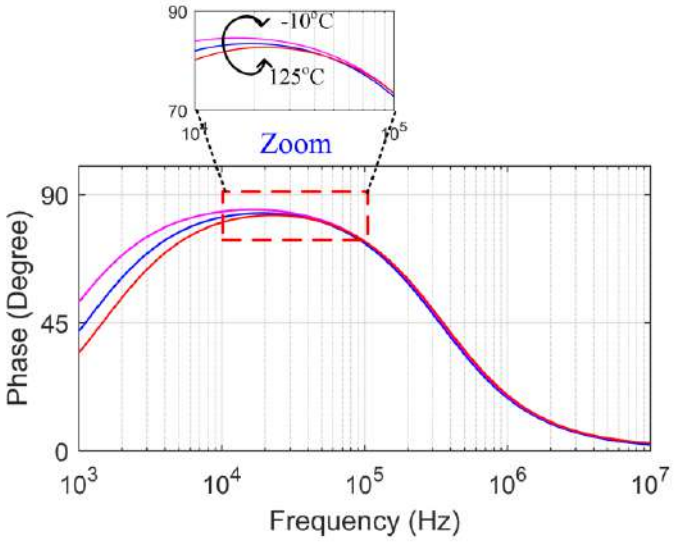
From these histograms of the phase and inductance, it can be inferred that the phase of the lossy inductor varies from 84.5091° to 84.4167° with a mean value of 84.5137° while, the inductance varies from 99.62μH to 101.41μH for the ideal value

of 101μH.

For temperature analysis, the proposed circuit has been operated at different temperatures of values $-10°$C, 70°C and 125°C and the magnitude and phase responses of impedance of Fig. 2.14a have been shown in Fig. 2.23.



(a)



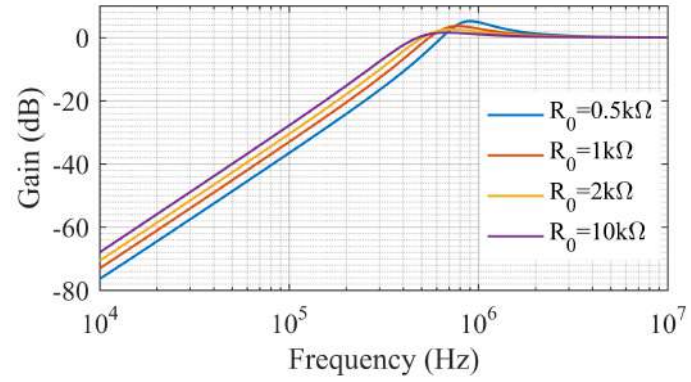
(b)

Figure 2.23: (a) Magnitude response of the proposed grounded lossy inductor with different temperature (b) Phase response of the proposed grounded lossy inductor with different temperature

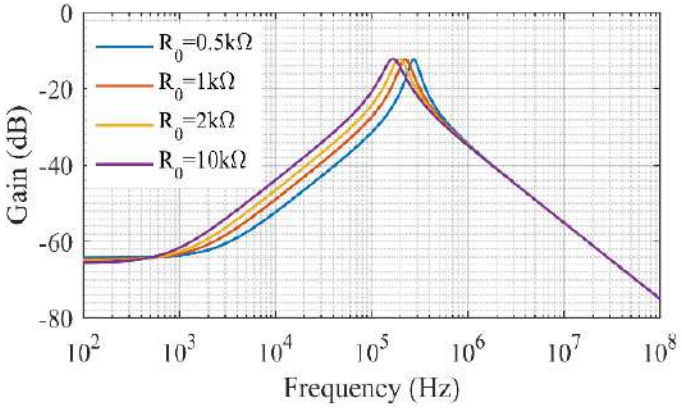
From the results shown in Fig. 2.23, it can be concluded that the variation in

temperature have insignificant effect on the characteristics of the proposed lossy inductor structure of Fig. 2.14a.

To demonstrate the usability of the proposed configuration, the applications of the grounded lossy inductor in the realizations of second-order HPF and BPF have been validated through simulations. The passive components used for HPF were taken as: $R_1 = R_3 = R_4 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, $C_0 = 100\text{pF}$, $C_1 = 1\text{nF}$ and R_0 was varied between $0.5\text{k}\Omega$ – $10\text{k}\Omega$ while, for BPF the values of passive components were selected as: $R_1 = R_3 = R_4 = 1\text{k}\Omega$, $R_2 = 10\text{k}\Omega$, $C_0 = 100\text{pF}$, $C_1 = 9\text{nF}$, $R_1 = 1\text{k}\Omega$ and R_0 was varied between $0.5\text{k}\Omega$ – $10\text{k}\Omega$. The simulated frequency responses of HPF and BPF have been displayed in Fig. 2.24.



(a)



(b)

Figure 2.24: (a) Simulated frequency responses of HPF (b) Simulated frequency responses of BPF

From Fig. 2.24, the simulated pole frequencies of the HPF were obtained as 701.91kHz,

569.03 kHz, 493.05l kHz and 426.75 kHz against the theoretical pole frequencies of 826kHz, 674.16 kHz, 583.53 kHz and 499.26 kHz respectively while, the simulated center frequencies of BPF were obtained as 275.423kHz, 224.151kHz, 195.55kHz and 167.225kHz against the theoretical center frequencies of 275.396kHz, 224.859kHz, 194.734kHz and 166.76kHz respectively. Thus, the simulated values of frequencies are found to be very close to the theoretical values. The power dissipation has also been carried out through simulations and found to be 3.59mW.

2.3.2.2 Experimental Results

Functionally, the IC chips, namely, LM3900 and AN-278 popularly known as $Norton\ amplifiers$, can implement the input–output relationship of an OTRA; these ICs have the following limitations:

(i) absence of virtual ground at their input terminals,

(ii) nonzero voltage reference (as both of these ICs operate on single power supply), and

(iii) acceptability of only unipolar currents.

Therefore, to examine the time response of the proposed grounded lossy inductor, an experimental verification employing OTRA implemented with off-the-shelf available ICs AD844 (shown in Fig. 2.25) has been carried out and its implementation has been displayed in Fig. 2.26. Passive components for Fig. 2.26 were selected as: $R_1 = R_3 = R_4 = 1k\Omega, R_2 = 10k\Omega, R_0 = 10k\Omega$, $R_c = 10k\Omega$ and $C_0 = 10$nF resulting $L_{eq} = 10.1$mH (Z = 68.96Ω at 1kHz).

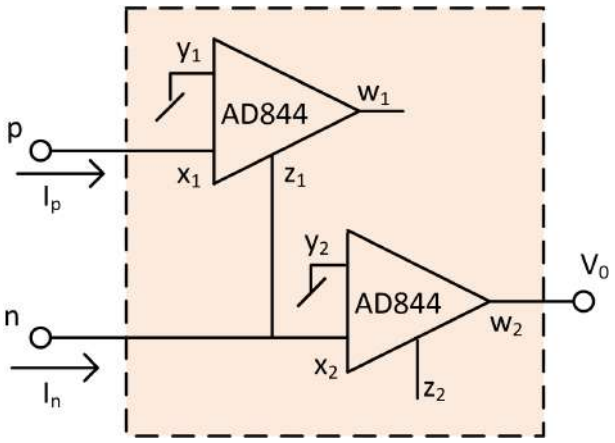


Figure 2.25: OTRA implementation using off-the-shelf ICs AD844 [22]

For experimental verification of the transient response of the lossy grounded inductor, a sinusoidal input voltage of $1V_{pp}$ at 1 kHz was applied and corresponding output voltage was measured. As input current was required for the grounded lossy inductor, hence a voltage to current convertor using AD844 IC was used with the proposed circuit. Both these input and output voltages have been displayed in Fig. 2.27.

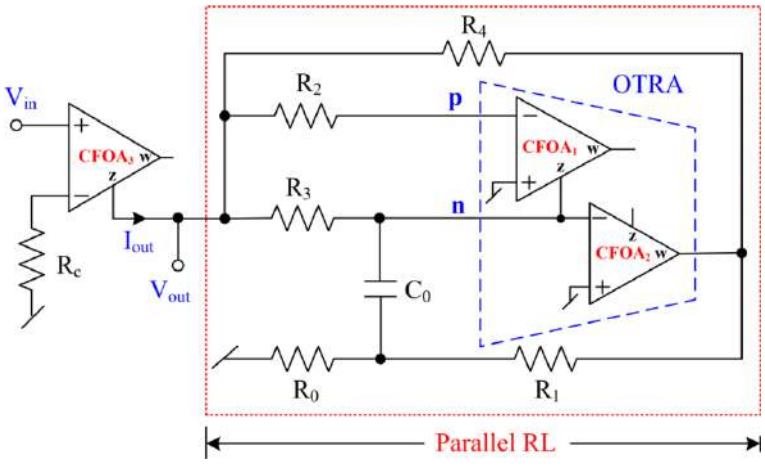


Figure 2.26: Complete current excited OTRA realization using CFOAs

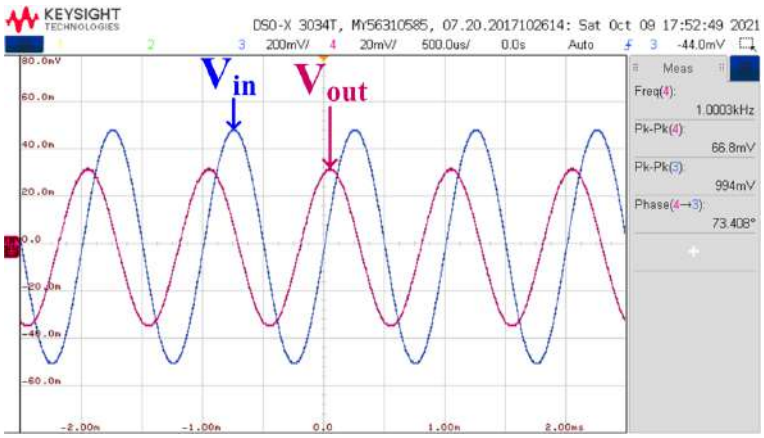


Figure 2.27: Experimental input and output voltages of the proposed grounded lossy inductor

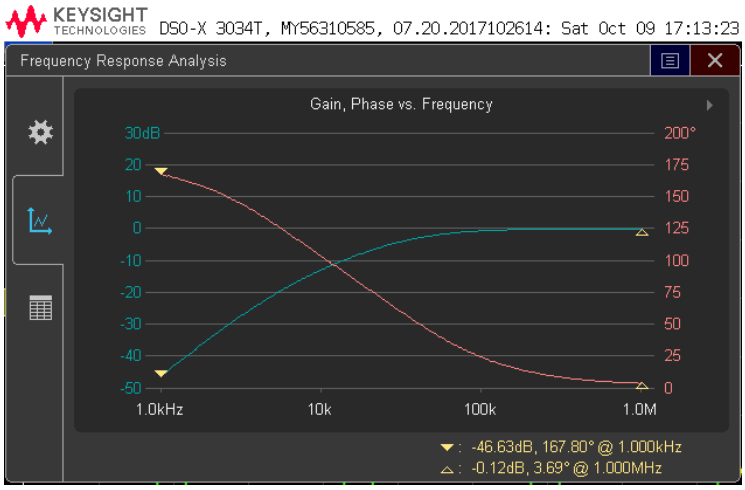
From Fig. 2.27, it is observed that the input and output voltages for the proposed lossy inductor of Fig. 2.14a has a phase difference of 73.408°.

To validate the theoretical propositions of the presented lossy inductor circuit, second-order HPF and BPF circuits shown in Fig. 2.16 were bread-boarded using OTRA of Fig. 2.26, with 5% tolerance in resistors and capacitors. The power supply voltages were set at ± 8V D.C. The experimental snapshot of the configuration has been displayed in Fig. 2.28.

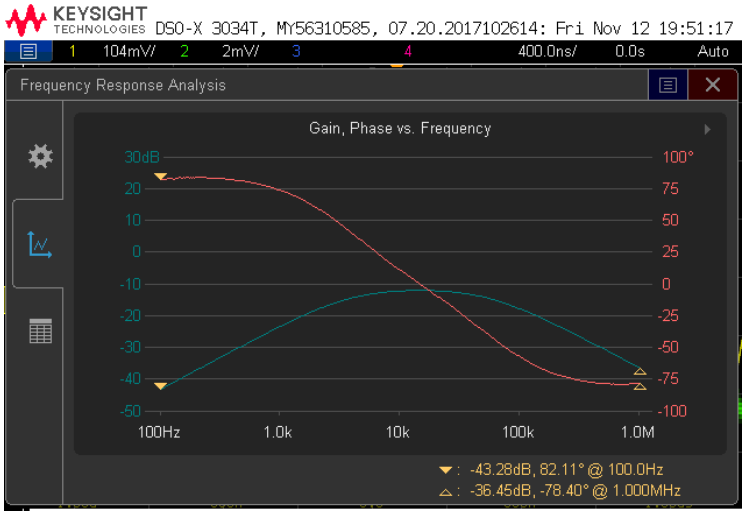
Figure 2.28: Snapshot of the experimental setup for HPF

The experimentally obtained frequency and phase responses of HPF and BPF have been demonstrated in Fig. 2.29a and Fig. 2.29b respectively. Fig. 2.30a and Fig.

2.30b display the input and output transient responses of HPF and BPF respectively.

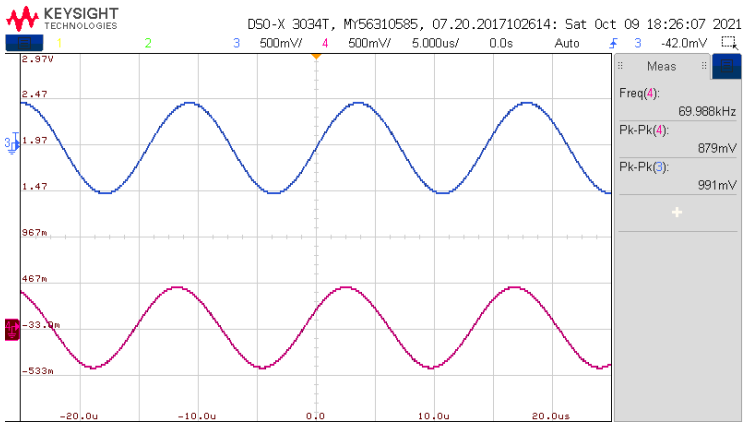


(a)

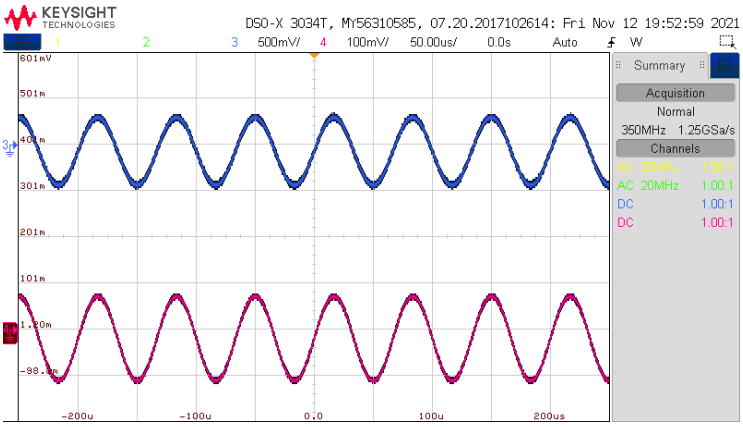


(b)

Figure 2.29: (a) Experimental magnitude and phase response of HPF (b) Experimental magnitude and phase response of BPF



(a)



(b)

Figure 2.30: (a) Experimental time response of input and output for HPF (b) Experimental time response of input and output for BPF

The above simulation and experimental results, thus, validate the functionality of proposed grounded lossy inductor circuit of Fig. 2.14a.

2.4 Concluding Remarks

In this chapter, we have presented two new configurations of grounded series/parallel lossy inductor simulator circuits employing a single OTRA. The first proposed circuit provides a grounded series lossy inductor simulator employing a single OTRA, one buffer, two resistors and two capacitors. A capacitor matching constraint is also required for the realization. The simulated value of inductance can be independently

controlled without changing the series equivalent resistance value. Non-ideal analysis with a one pole model of OTRA has also been carried out and compared with the ideal propositions. Functionality of the proposed circuit has been validated using CMOS OTRA implemented in 0.18 μm TSMC technology parameters. Application example has also been demonstrated using the proposed configuration.

A grounded parallel lossy inductor simulator has also been presented in this chapter employing a single OTRA, five resistors and one virtually grounded capacitor. The proposed circuit can also be configured as lossless negative inductor subject to matching constraints. The value of both lossy as well as lossless inductance can be controlled independently by a grounded resistor. Application examples of the proposed lossy inductor have also been demonstrated as a second order HPF and second order BPF. To validate the workability of the proposed lossy parallel inductor circuit, CMOS OTRA implemented in 0.18 μm TSMC technology parameters has been used. To check the robustness of the proposed parallel lossy inductor circuit, Monte Carlo simulations and temperature analysis have also been carried out. Experimental results have also been appended using OTRA implemented with AD844 type CFOAs.

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Chapter 3

New Design of Capacitance Multiplier Circuit Using Single OTRA

3.1 Introduction

In the previous chapter we have proposed new impedance simulator circuits realized with single OTRA. In this chapter, a new capacitance multiplier configuration employing a single OTRA is proposed. The proposed structure is capable of providing both positive and negative multiplication factors depending on the value of resistances used.

Circuits used in low frequency applications require large value capacitances, which in turn require large silicon area in integrated circuit implementation, and hence, are impractical or not feasible for full integration. Capacitance multiplier (CM) circuit which multiplies a small capacitance embedded on chip to realize a large capacitance value is an optimal solution for this problem.

In the available literature, there are numerous CM circuits using various active

devices like operational amplifier (op-amp) [1], operational transconductance amplifier (OTA) [2–4], operational transresistance amplifier (OTRA) [5], second generation voltage conveyor (VCII) [6], current feedback transconductance amplifier (CFTA) [7–9], voltage differencing buffered amplifier (VDBA) [10], current differencing transconductance amplifier (CDTA) [11], current feedback operational amplifier (CFOA) [12–17], current controlled current conveyor transconductance amplifier (CCCCTA) [18], differential input buffered transconductance amplifier (DBTA) [19], voltage differencing inverting buffered amplifier (VDIBA) [20], differential voltage current conveyor transconductance amplifier (DV-CCTA) [21], differential voltage current conveyor (DVCC) [22], current conveyor and its different variants [23, 24], differential voltage second generation current conveyor (DVCCII) [25], current backward transconductance amplifier (CBTA) [26] and modified current feedback operational amplifier (MCFOA) [27].

The CM circuits may also be classified depending on the type of capacitance realized viz. grounded CM [1–20] and floating CM [8, 9, 13, 21–27]. Also, depending on the value of capacitance realized, it can be further classified as positive CM [1–12, 15–28] and negative CM [4, 6, 7, 13–15, 17, 22]. Yet another classification may be done on the basis of number of active devices used like the CM circuits using a single active device [11–13, 16, 19–21, 27] or two active devices [1, 2, 5–7, 10, 14, 15, 17, 18, 22, 23, 25] or three active devices [3, 4, 24]. Some authors have also used four [8, 24] and five [9] active devices to design CM circuits. Since this chapter deals with the realization of lossless grounded CM circuit, in the following, we present a brief overview of the important lossless, grounded CM circuits reported so far in the open literarure.

Tang, Ismail and **Bibyk** in [1], presented a Miller CM circuit using a single op-amp and a voltage follower (VF). The circuit uses three passive components, of which one resistor is grounded while the other resistor and a capacitor are floating. To validate the workability of the presented Miller CM circuit, a third-order charge pump phase

locked loop (PLL) synthesiser is implemented and its performance was verified with PSPICE simulations.

A temperature independent CM circuit has been presented by **Khan** and **Ahmed** in [2] using one OTA and a VF alongwith a resistor and a capacitor. The circuit had the features of electronic tunability of the multiplication factor(k). The performance of the circuit was verified experimentally using dual, buffered OTAs, LM13600N IC.

Tunable grounded and floating CM circuits using OTAs were reported by **Ahmed, Khan** and **Minhaj** in [3]. The grounded CM circuit employs two OTAs and an op-amp while the floating CM circuit uses three OTAs and an op-amp. The presented circuits were experimentally verified using the OTA IC LM3080E and the operational amplifier IC LM741.

To obtain both positive and negative multiplication factors, a new CM circuit has been presented by **Al-Absi** and **Al-Khulaifi** in [4] using two OTAs and a MOS translinear loop. The reported capacitance multiplier circuit has been used in the design of a tunable low-pass filter. The filter was simulated using TANNER TSPICE simulator employing 0.18μm CMOS technology parameters.

In [5], **Nagar** and **Paul**, employed two OTRAs, a voltage follower, two resistors and a capacitor to implement two positive grounded CM circuits. PSPICE simulations using 180nm CMOS technology parameters have been presented to validate the functionality of the circuit. A first-order low-pass filter has also been implemented as an application of the reported CM circuit.

In [6], CM circuits using two VCIIs, two resistors and a capacitor have been presented by **Stornelli, Safari, Barlie** and **Ferri** as shown in Fig. 3.1, wherein, two different circuits have been presented to realize positive and negative multiplication

factors. CMOS implementation of VCII has been used for simulations. Experimental results have also been provided wherein the AD844 implementation of VCII was used. An exemplary first-order low-pass filter was also implemented as an application of the presented CM.

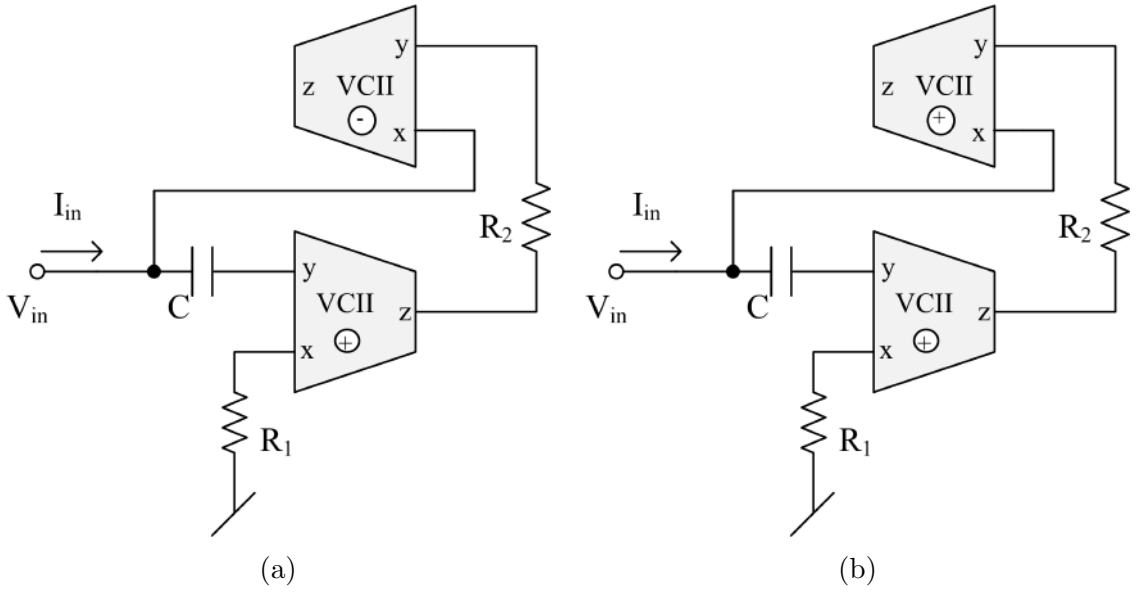


Figure 3.1: Capacitance multiplier presented in [6]

Four new grounded CM circuits employing CFTAs have been reported by **Ozer** in [7]. Of these, two have positive multiplication factors while the other two have negative multiplication factors. All the presented circuits employ two CFTAs, two grounded resistors and a floating capacitor. No component matching constraint was necessary for the realization of the circuits. To demonstrate the workability of the presented CM circuits two application examples, the first, a capacitance cancellation scheme and the second, a current-mode universal biquad filter were also provided.

Li in [8], presented a four CFTA-based grounded/floating CM circuit. The multiplication factor (k) could be tuned electronically by changing the bias currents of different CFTAs.

Another realization of a grounded CM using CFTAs was presented by **Koton, Herencsar** and **Venclovsky** in [9]. Here, three CFTAs have been used alongwith two resistors and a capacitor.

In [10], an active only grounded CM is presented using VDBAs. The circuit employs two VDBAs. The circuit does not employ any passive component, has low sensitivity of multiplication factor (k) and does not have any component matching constraints (in terms of equality of transconductances, etc.)

Two new grounded CM circuits using a single CDTA, one/two resistors and a capacitor have been reported by **Biolek, Vavra** and **Keskin** in [11]. Using an additional CDTA, these circuits can be converted into a floating CM also. The CM circuits were experimentally verified using an on-chip CDTA manufactured in 0.7μm CMOS technology parameters.

Two modified CFOA-based grounded CM circuits were presented by **Yuce** and **Minaei** in [12]. The circuits employed a single modified CFOA, two grounded resistors and a grounded capacitor. No component matching constraints were prescribed for the realization.

A negative grounded capacitance multiplier using a single CFOA has been reported by **Dogan** and **Yuce** in [13] using a grounded capacitor, two grounded resistors and a floating resistor as shown in Fig. 3.2. However, the reported circuit realizes the CM only if a component matching constraint is satisfied.

Four new circuits employing CFOAs to realize CM have been presented by **Lahiri**

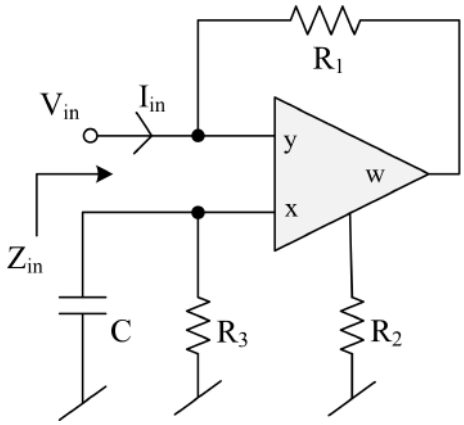


Figure 3.2: Negative capacitance multiplier reported in [13]

and **Gupta** in [14]. The first two circuits employ two CFOAs, two grounded resistors and a grounded capacitor while the other two circuits employ a single CFOA, two resistors and a capacitor to realize a grounded negative CM. The use of all grounded passive components especially the capacitor, in the first two and in the fourth circuit, make them suitable for monolithic integration.

Another CM using two CFOAs, two resistors and a capacitor has been presented by **Verma, Pandey** and **Pandey** in [15] which can provide a high multiplication factor even if the component values are not widely spread. The drawback of this CM circuit is that the sensitivity of the multiplication factor with respect to the passive components is high. The presented circuit has been employed in the design of a parallel RLC resonator, to demonstrate the workability of the CM circuit.

In [16], another positive grounded CM circuit has been reported by **Arslanalp** and **Yucehan** using a single CFOA, a grounded capacitor and two floating resistors. The reported circuit has low sensitivity to temperature variation.

Another positive/negative CM circuit employing a CFOA, an OTA, a grounded capacitor and a grounded resistor that is capable of providing high multiplication factor has been presented by **Al-Absi** and **Abuelmaatti** in [17]. As an application example, the proposed CM circuit is used in the design of a first-order low-pass

filter.

In [18], **Silapan, Tanaphatsiri** and **Siripruchyanun** presented a CM circuit using two CCCCTAs and a capacitor as shown in Fig. 3.3. In the reported circuit multiplication factor is electronically tunable as well as temperature insensitive. PSPICE simulations were used to validate the performance of the circuit. A fifth-order Chebyshev low-pass filter has been implemented as an application of the presented CM circuit.

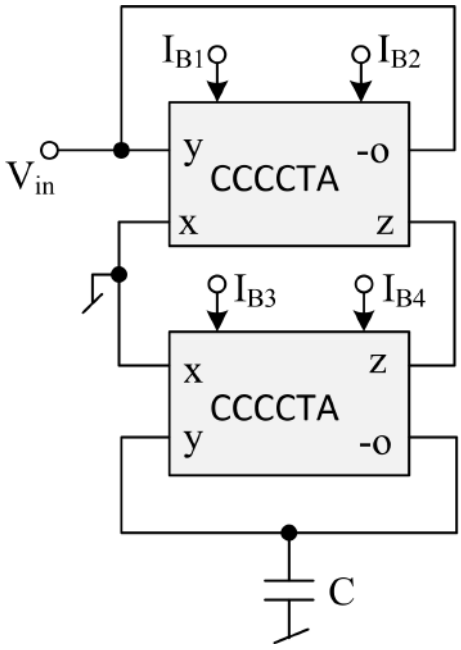


Figure 3.3: Grounded capacitance simulator presented in [18]

A CM circuit using a single DBTA, a grounded capacitor and a grounded resistor has been reported by **Vavra** in [19]. The DBTA was realized by means of three AD844 ICs. A first-order low-pass filter has been presented as an application of the reported CM circuit.

A resistorless grounded CM circuit has been presented by **Tangsrirat** in [20] using a single VDIBA, a floating capacitor and a NMOS transistor (acting as a voltage controlled resistor) which is displayed in Fig. 3.4. To validate the functionality

of the reported CM circuit , a first-order low-pass filter has been implemented and simulated in PSPICE using TSMC 0.25μm CMOS process parameters.

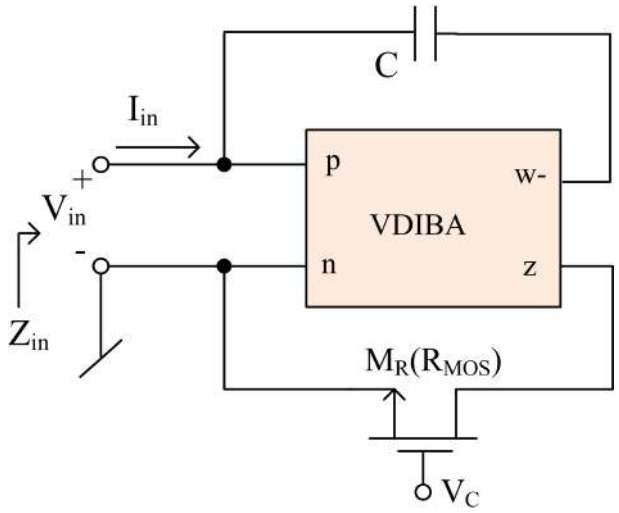


Figure 3.4: Single VDIBA based capacitance multiplier presented in [20]

From the above description, it thus, emerges that a good circuit of capacitance multiplier should (i) employ a minimum number of active elements, (ii) not use large number of passive elements, (iii) have a provision of electronic tuning of the multiplication factor and (iv) have minimum low frequency restrictions.

After a careful perusal of the available literature and the major factors for realization of a CM circuit, in this chapter, we have proposed a new topology of a lossless grounded capacitance multiplier circuit using an OTRA, a voltage follower (VF), one capacitor and three (virtually grounded) resistors. The proposed circuit is capable of realizing both positive as well as negative capacitance multiplication factors by changing the value of resistances used. Implementation of CM using OTRA has the advantage of having less parasitic effects, as the presence of virtual ground at the input terminals of the OTRA removes the effect of input parasitic immittances, as a result, the low frequency limitations which arise due to the presence of parasitics are thus eliminated. Also, the use of MOS resistors with OTRA are preferable for monolithic IC implementation and also allow electronic tunability. Therefore, the proposed circuit is made electronically tunable by replacing the passive resistors

with MOSFETs (operating in ohmic region).

3.2 OTRA-Based Positive/ Negative Grounded Capacitance Multiplier[1]

The proposed capacitance multipler circuit has been shown in Fig. 3.5

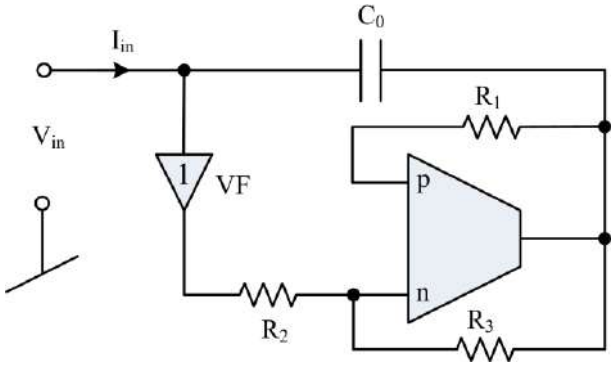


Figure 3.5: Proposed capacitance multiplier circuit

Assuming ideal OTRA, routine circuit analysis leads to the input impedance as given by:

$$Z_{in}(s) = \frac{V_{in}(s)}{I_{in}(s)} = \frac{1}{sC_{eq}} \tag{3.1}$$

where C_{eq} is given by equation (3.2):

$$C_{eq} = C_0 \left(1 + \frac{R_1 R_3}{R_2(R_1 - R_3)}\right) \tag{3.2}$$

From equation (3.2), it may be observed that the proposed CM circuit can perform in both positive as well as negative mode of operation with the following condition(s):

Case 1: If we take $R_3 = \infty$, then the equivalent capacitance becomes:

$$C_{eq} = C_0 \left(1 - \frac{R_1}{R_2}\right) \tag{3.3}$$

The capacitance multiplication factor obtained from equation (3.3) may be positive when $R_2 > R_1$ and the same would be negative if $R_1 > R_2$.

[1]The material presented in this section has been published in: D. R. Bhaskar, Garima and Pragati Kumar, "OTRA-Based Positive/ Negative Grounded Capacitance Multiplier" Analog Integrated Circuits and Signal Processing, 2022.

Case 2: If the resistor R_3 is selected as $\frac{R_1}{2}$, the equivalent capacitance reduces to:

$$C_{eq} = C_0 \left(1 + \frac{R_1}{R_2}\right) \tag{3.4}$$

From equation (3.4), it may be noticed that the multiplication factor of proposed CM circuit may be of higher value with appropriate selection of resistors R_1 and R_2.

3.2.0.1 MOS-C implementation of CM

The passive resistors consume large area in IC implementation compared to the linear resistors implemented using MOS transistors operating in the triode region. The current differencing property of an OTRA allows resistors connected to the input of the OTRA to be implemented using MOS transistors with complete non-linearity cancellation [29] as shown in Fig.3.6.

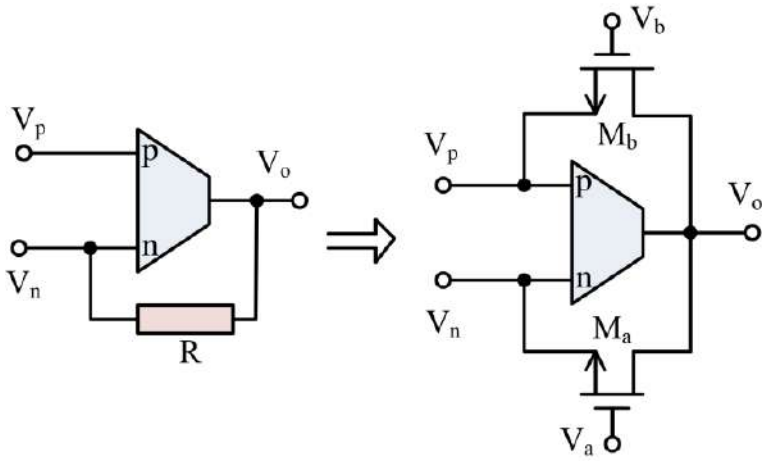


Figure 3.6: MOS implementation of linear resistance connected between inverting input and output terminal of OTRA [29]

The resistance value can be adjusted by appropriate choice of gate voltages, thereby making the multiplication factor of the CM electronically tunable. The resistance value thus obtained can be expressed [29] as:

$$R = \frac{1}{\mu_n C_{ox} \left(\frac{W}{L}\right) (V_a - V_b)} \tag{3.5}$$

where μ_n, C_{ox}, W and L are channel mobility, oxide capacitance per unit gate area, effective channel width and effective channel length of MOS respectively. V_a and V_b are the gate voltages applied to the MOSFETs.

The CM structure shown in Fig. 3.5, thus, can be converted into MOS-C configuration replacing passive resistors by identical MOS transistors operating in the triode (ohmic) region (Fig. 3.6), which is now demonstrated in Fig. 3.7.

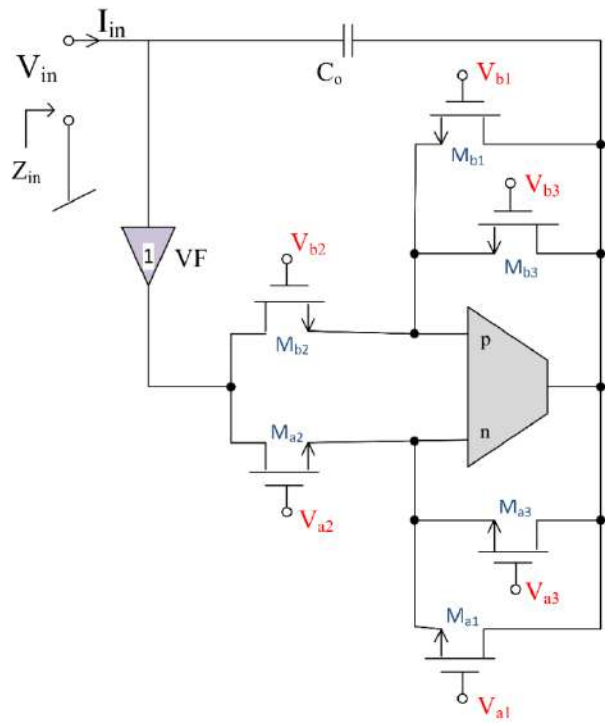


Figure 3.7: MOS-C implementation of proposed capacitance multiplier circuit

Substituting the value of R from equation (3.5) in equation (3.2), we get the equivalent capacitance as a function of bias voltages (assuming all the MOSFETs of Fig. 3.7 to be completely matched) as:

$$C_{eq} = C_0 \left(1 + \frac{(V_{a2} - V_{b2})}{(V_{a1} + V_{a3}) - (V_{b1} + V_{b3})}\right) \tag{3.6}$$

3.2.0.2 Non-Ideal Analysis

In this section, the effects of major non-idealities inherent in the OTRA on the proposed CM circuit are considered, using a single pole model for the trans-resistance

gain R_m [30], given below as:

$$R_m(s) = \frac{R_0}{1 + \frac{s}{\omega_0}} \tag{3.7}$$

For applications intended for high frequencies, R_m(s) reduces to:

$$R_m(s) = \frac{1}{sC_p} \; where \; C_p = \frac{1}{R_0\omega_0} \tag{3.8}$$

Using the non-ideal model of the OTRA (given by equation (3.8)), the non-ideal equivalent capacitance has been determined as:

$$C_{eq}(s) = C_0\left(1 + \frac{R_1R_3}{sC_pR_1R_2R_3 + R_2(R_1 - R_3)}\right) \tag{3.9}$$

Putting the value of C_p from equation (3.8) in equation (3.9), we get:

$$C_{eq}(s) = C_0\left(1 + \frac{R_1R_3}{\frac{sR_1R_2R_3}{R_0\omega_0} + R_2(R_1 - R_3)}\right) \tag{3.10}$$

It is noted from equation (3.10) that for large values of R_0 (ideally infinite), we may neglect the coefficient of s in the expression of C_{eq}(s). Thus, the ideal and non-ideal equivalent capacitance of the proposed circuit becomes equal.

3.2.0.3 Application Examples

To demonstrate the effectiveness of the proposed CM, two application examples have been presented. The first is a capacitive cancellation circuit where the parasitic

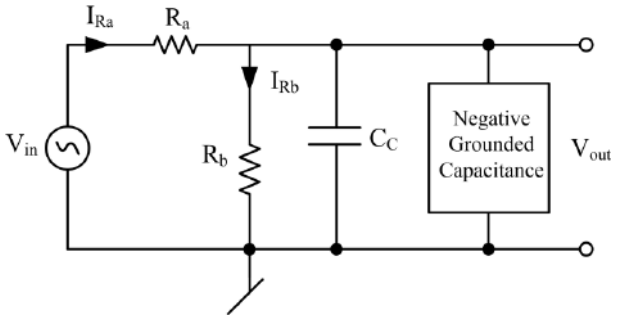


Figure 3.8: Capacitance cancellation circuit [14]

capacitors present in the output of the active circuit can be eliminated with the help of the negative capacitance. The capacitive cancellation circuit scheme is shown in Fig. 3.8.

The transfer function for the circuit of Fig. 3.8 is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{R_b}{sC_{eq}R_aR_b + R_a + R_b} \tag{3.11}$$

where $C_{eq} = C_C$ + negative grounded capacitance (NGC)

If the values of both the capacitances C_C and NGC are equal, then NGC will cancel out the effect of C_C and therefore, the circuit in Fig. 3.8 will become purely resistive and hence, the currents I_{Ra} and I_{Rb} will be in phase.

The second application of CM structure is in the realization of a first order low pass filter(LPF) using a resistor and a capacitor, which requires a large value capacitor for realization of a given pole frequency. This large capacitor may, in turn is realized by a CM circuit using a small value capacitor as given in equation (3.4). The circuit is shown in Fig. 3.9.

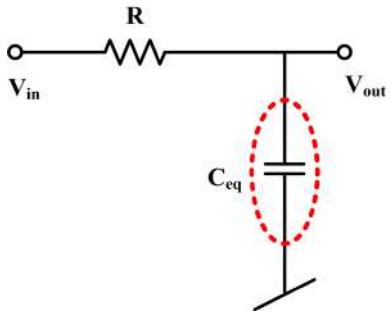


Figure 3.9: First-order LPF

The transfer function for the filter of Fig. 3.9 is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{1}{RC_{eq}}}{s + \frac{1}{RC_{eq}}} \tag{3.12}$$

and the pole frequency is given by:

$$f_0 = \frac{1}{2\pi RC_{eq}} \tag{3.13}$$

3.2.0.4 Simulation Results and Matlab Evaluations

To establish the workability of the proposed grounded capacitance multiplier circuit, CMOS OTRA implemented with 0.18μm TSMC technology parameters has been used. The schematic CMOS implementation of OTRA [31] used in the simulations has been shown in Fig. 3.10. The power supply voltages for the biasing of CMOS OTRA were taken as $\pm$ 1.85V. The bias current (I_B) and bias voltage (V_{B1}) used in Fig. 3.10 were taken as 18μA and 0.36V respectively. The aspect ratios for various MOSFETs used in Fig. 3.10 have been tabulated in Table 3.1.

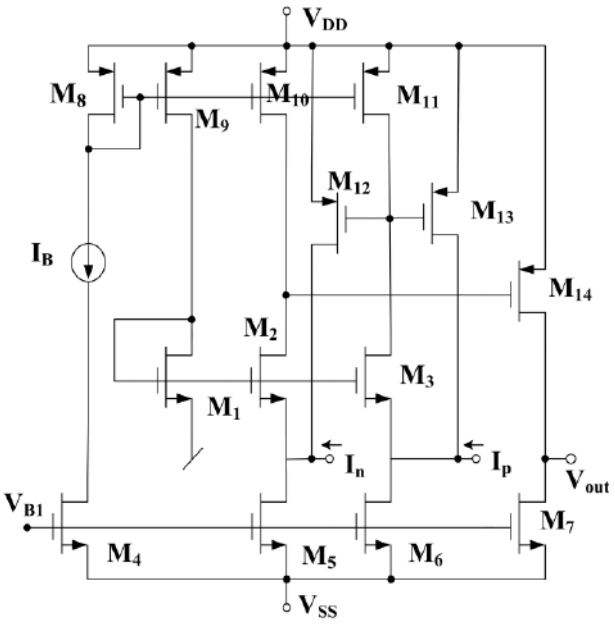


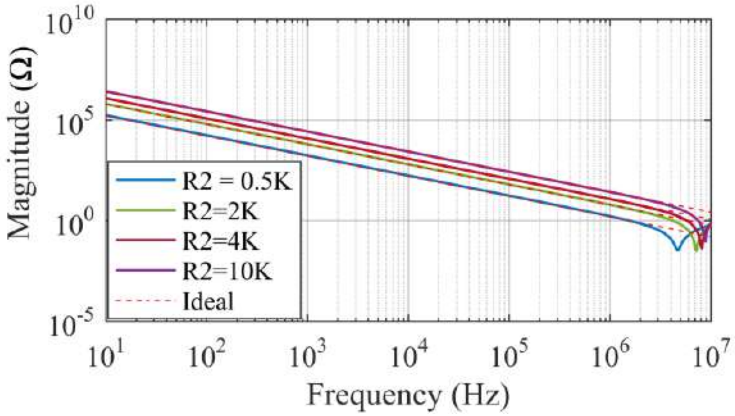
Figure 3.10: CMOS Implementation of OTRA [31]

Table 3.1: Aspect ratios of MOSFETs shown in Fig. 3.10

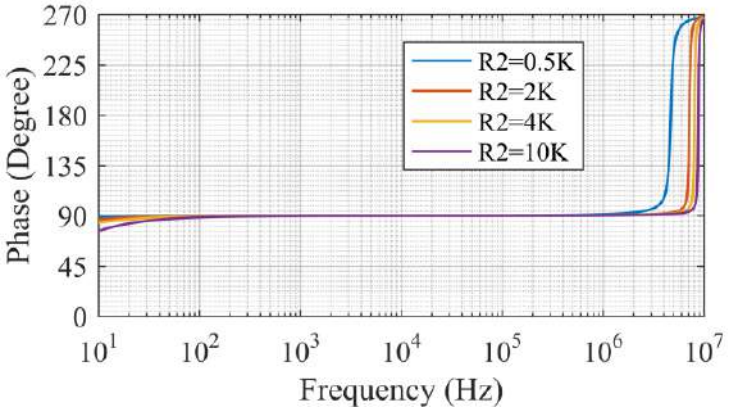
MOSFETs	Aspect Ratio (W/L) in μm
$M_1 - M_3$, $M_{12} - M_{13}$	36/0.9
M_4, M_7	3.6/0.9
M_5, M_6	10.8/0.9
$M_8 - M_{11}$	18/0.9
M_{14}	18/0.18

The CM circuit presented in Fig. 3.5 has been simulated in PSPICE for which the

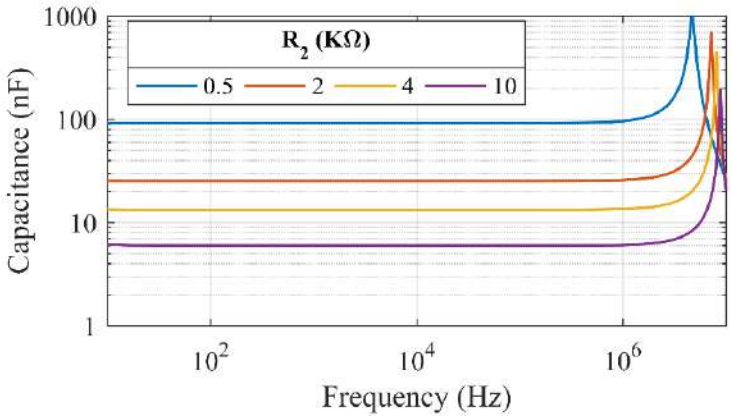
values of various passive components were taken as: $R_1 = 50\text{k}\Omega$, $R_3 = 25\text{k}\Omega$ and $C_0 = 1\text{nF}$. The magnitude and phase responses of the positive grounded CM for various multiplication factors have been shown in Fig. 3.11a and Fig. 3.11b respectively. The variation of realized capacitance with frequency has been shown in Fig. 3.11c. From Fig. 3.11c, it is observed that the realized capacitance remains constant upto a frequency of 1 MHz. In order to adjust the multiplication factor, R_2 was varied as per the details given in Table 3.2 that also contains the simulated and theoretical values of the realized capacitance.



(a)



(b)



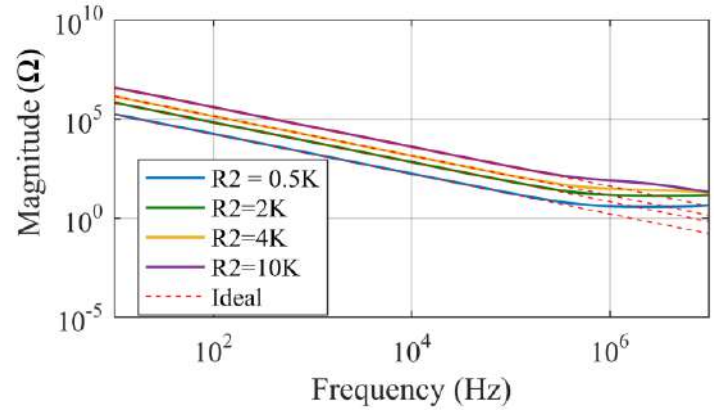
(c)

Figure 3.11: Variation of (a) magnitude (b) phase (c) capacitance with R_2 for the proposed positive CM

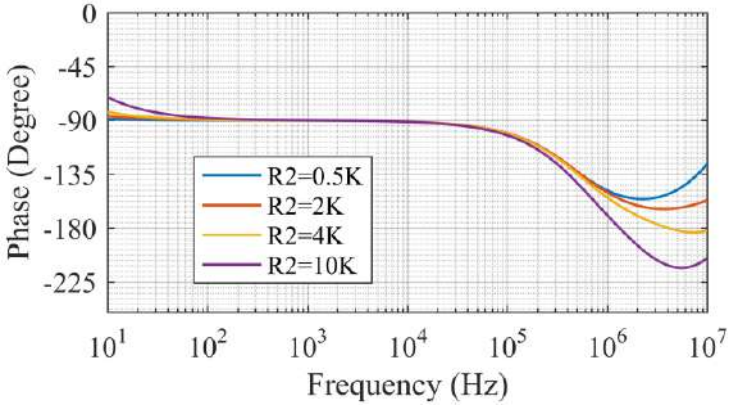
Table 3.2: Variation in capacitance with R_2

R_2 **(kΩ)**	C_{eq}**(simulated) (nF)**	C_{eq}**(theoretical) (nF)**
0.5	99.953	101
2	25.422	26
4	13.429	13.5
10	6.147	6

The negative CM circuit has also been simulated and the magnitude and phase responses have been shown in Fig. 3.12a and Fig. 3.12b respectively along with MATLAB evaluations. For the realization of a negative CM, the component values were taken as $R_1 = 50\text{k}\Omega$, $C_0 = 1\text{nF}$ with R_3 open circuited. R_2 was varied (0.5kΩ, 2kΩ, 4kΩ and 10kΩ) and correspondingly the magnitude of multiplication factors obtained for the negative CM for the various values of R_2 were found 99, 24, 11.5 and 4 respectively.



(a)



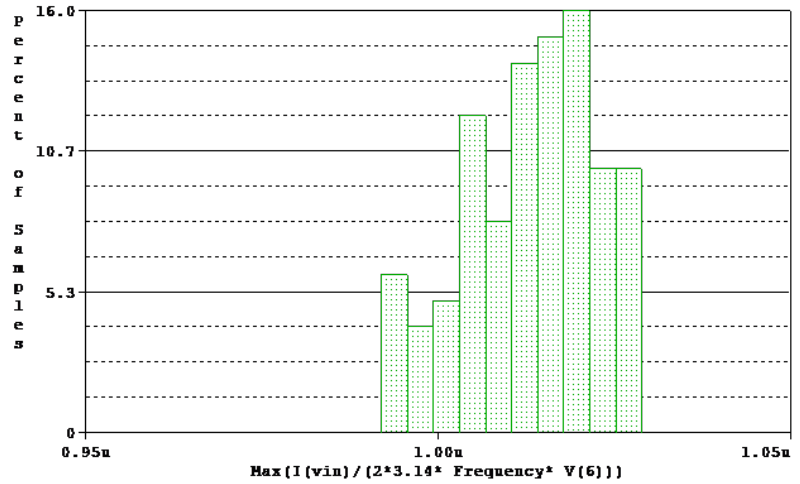
(b)

Figure 3.12: Variation of (a) magnitude (b) phase with R_2 for the proposed negative CM

From Fig. 3.11 and Fig. 3.12, it is observed that the proposed positive CM circuit can work properly in the frequency range of 100 Hz to 1 MHz while, the proposed negative CM circuit can work properly in the frequency range of 100 Hz to 100 kHz.

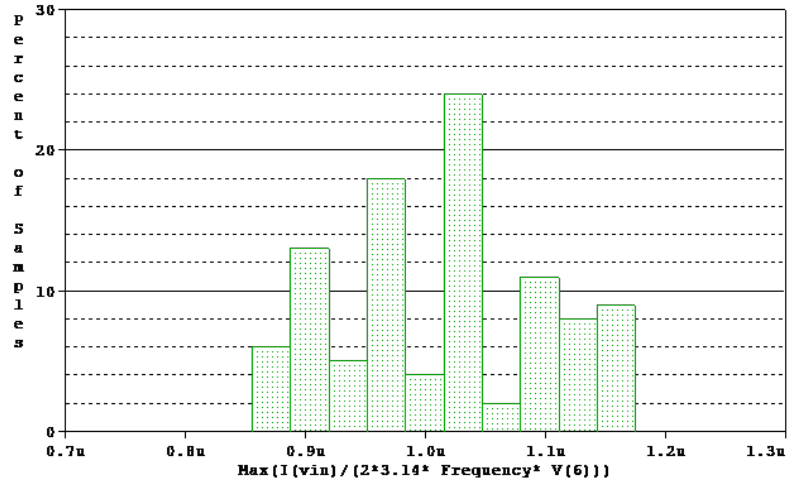
3.2.0.5 Monte Carlo Simulation

Monte Carlo analysis has also been carried out to check the robustness of the proposed CM circuit and for these 100 samples with 10% tolerance in parameter values have been taken. The histograms for tolerances in R_2 and C_0 for the positive and negative CM circuits have been shown in Fig. 3.13 and Fig. 3.14 respectively.



n samples	= 100	10th %ile	= 9.98712e-007
n divisions	= 10	median	= 1.01425e-006
mean	= 1.01317e-006	90th %ile	= 1.02513e-006
sigma	= 9.65167e-009	maximum	= 1.02891e-006
minimum	= 9.91936e-007	3*sigma	= 2.8955e-008

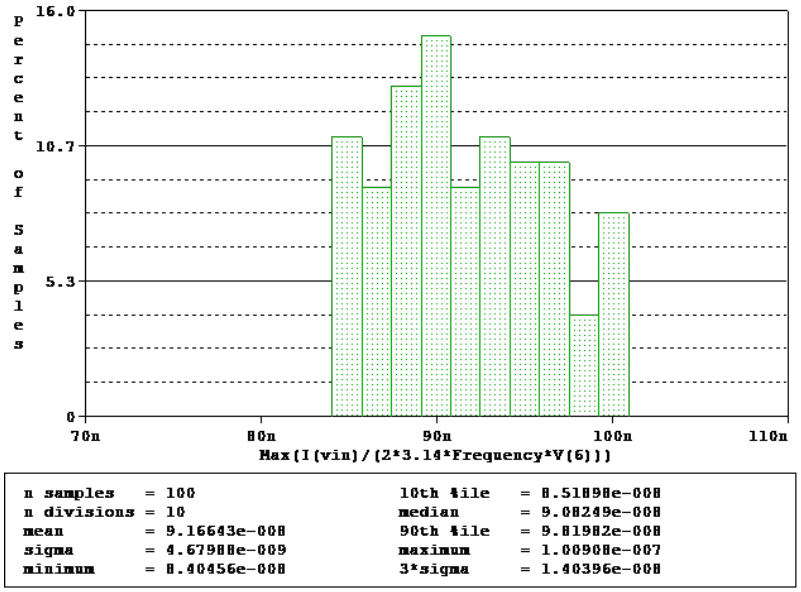
(a)



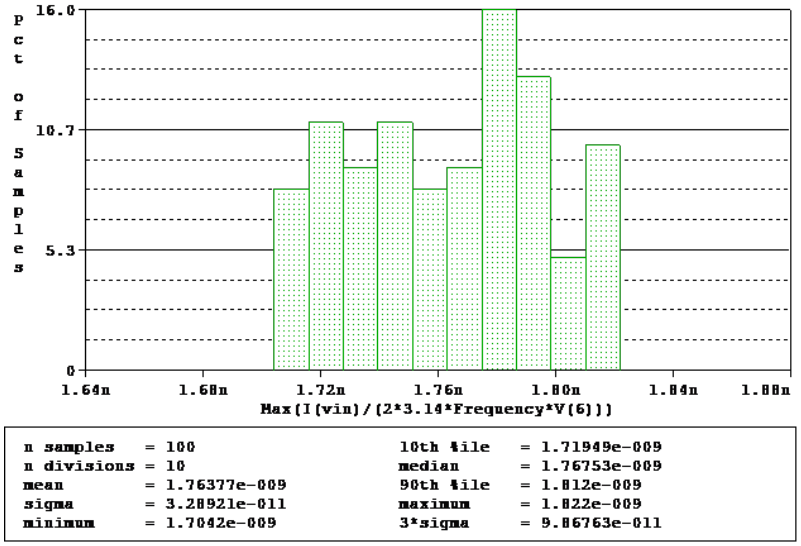
n samples	= 100	10th %ile	= 9.88029e-007
n divisions	= 10	median	= 1.03861e-006
mean	= 1.01783e-006	90th %ile	= 1.12953e-006
sigma	= 8.54033e-008	maximum	= 1.17503e-006
minimum	= 8.55723e-007	3*sigma	= 2.5621e-007

(b)

Figure 3.13: Histogram of equivalent capacitance realized by positive CM with 10% tolerance in(a) R_2 (b) C_0



(a)



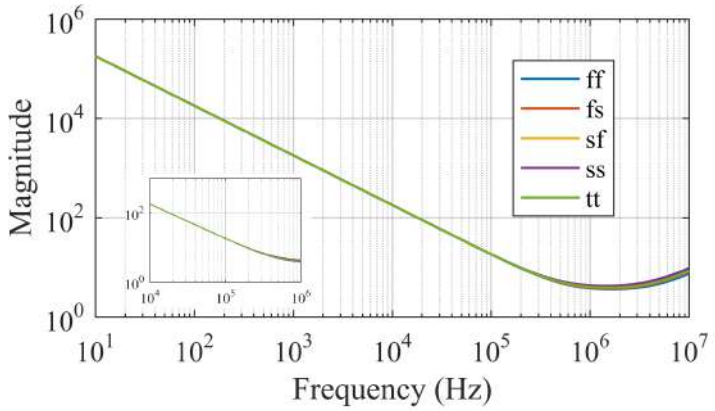
(b)

Figure 3.14: Histogram of equivalent capacitance realized by negative CM with 10% tolerance in(a) R_2 (b) C_0

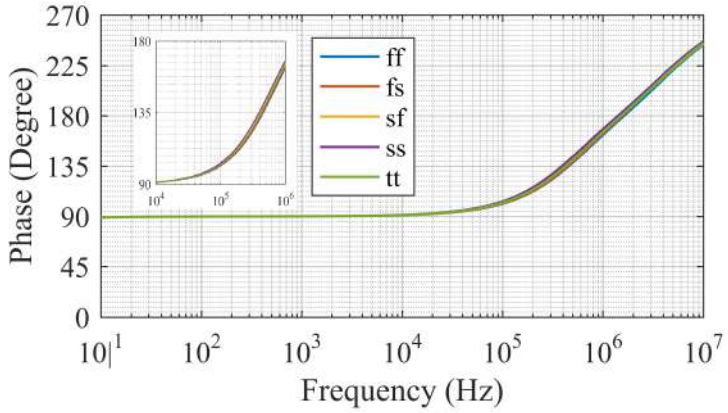
From the statistical data obtained from Monte Carlo analysis, the deviation in the value of capacitance realized using positive CM circuit by (i) varying R_2 is around 9nF and (ii) by varying C_0 is around 0.8nF for the designed value of 101nF. In case of negative CM configuration, the deviation is 4.67nF for the variation in R_2 while it is 5.06nF for the variation in C_0 for the designed value of 99nF.

3.2.0.6 Process Corner and Temperature Analysis

To evaluate the prefabrication performances of MOS CM circuit, process corner and temperature analyses have also been carried out. The effects of different process corners i.e., slow-slow (ss), slow fast (sf), fast-slow (fs), fast-fast (ff), and typical-typical (tt) on the magnitude and phase of impedance of CM circuit have been shown in Fig. 3.15a and Fig. 3.15b respectively. The effects of temperature variation on the magnitude and phase of input impedance of the proposed positive and negative CM circuit have been shown in Fig. 3.16 and Fig. 3.17 respectively.

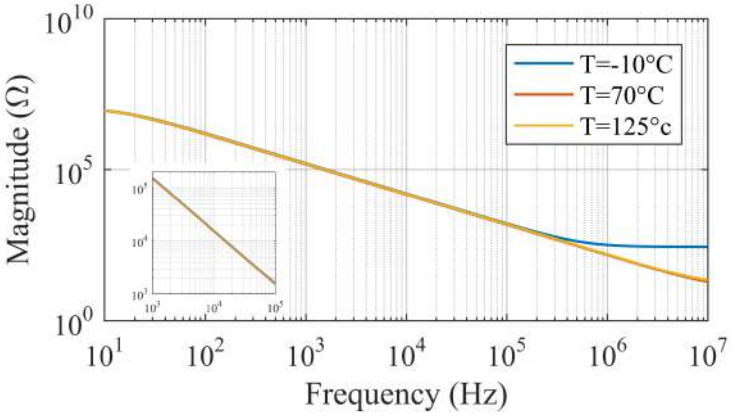


(a)

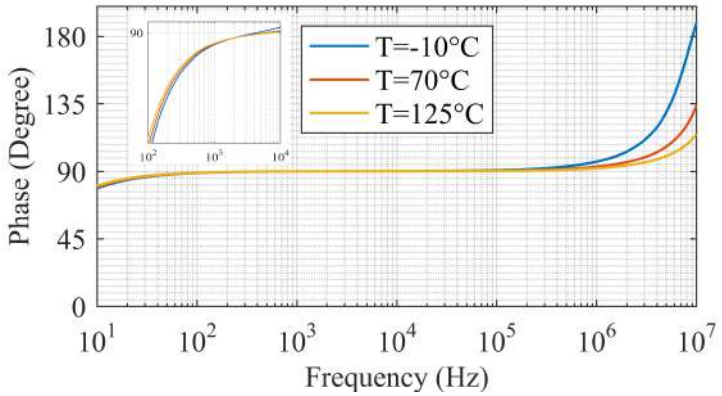


(b)

Figure 3.15: Process corner analysis on (a) magnitude and (b) phase of positive CM

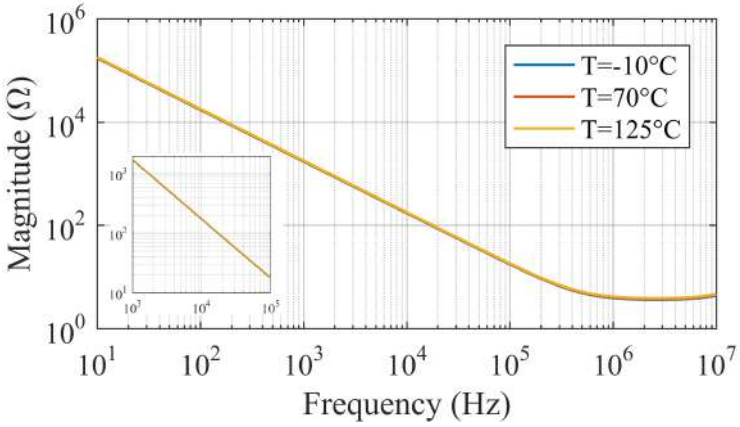


(a)

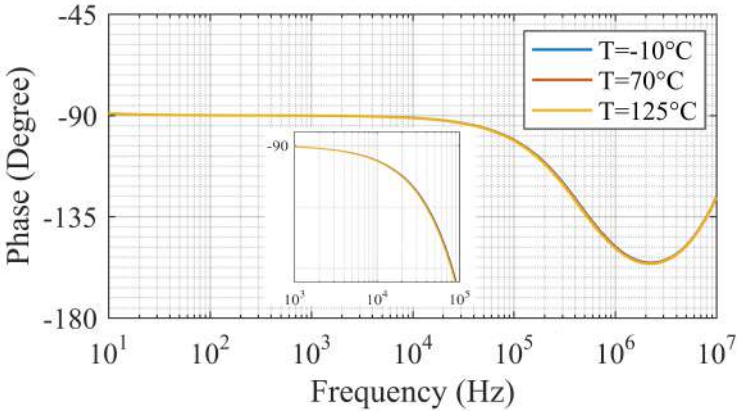


(b)

Figure 3.16: Variation of (a) magnitude and (b) phase with temperature for positive CM



(a)



(b)

Figure 3.17: Variation of (a) magnitude and (b) phase with temperature for negative CM

From Fig. 3.15, Fig. 3.16 and Fig. 3.17, it is observed that the proposed CM circuit works satisfactorily at different process corners and different temperatures.

3.2.0.7 Magnitude and Phase Responses of MOS-C CM Circuit

The MOS-C CM circuit as shown in Fig. 3.7 has also been simulated in PSPICE. The MOS implementation of the voltage follower structure [32] has been shown in Fig. 3.18.

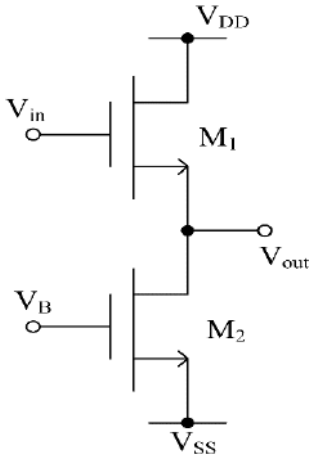


Figure 3.18: MOS implementation of VF [32]

The various biasing voltages for the simulation of the circuit shown in Fig. 3.7 used

were $V_{a1} = V_{a3} = 0.8$V, $V_{a2} = 1.5$V and $V_{b1} = V_{b3} = 0.76$V. Value of the capacitance was varied by varying the bias voltage V_{b2}. The magnitude and phase responses of the circuit of Fig. 3.7 for various values of V_{b2} have been shown in Fig. 3.19a and Fig. 3.19b respectively, while capacitance has been shown in Fig. 3.19c.

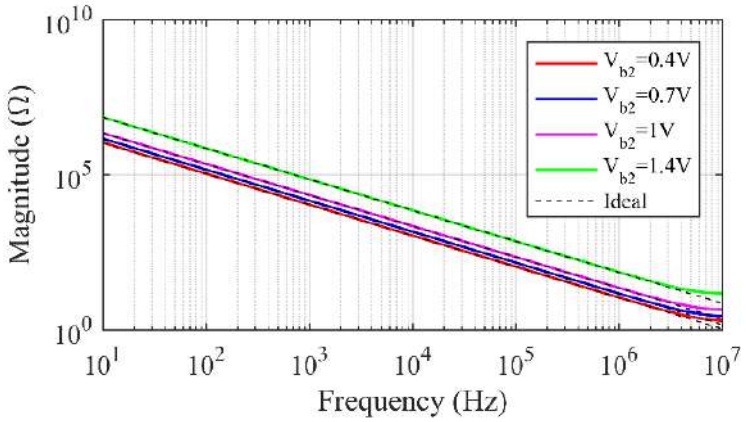
The value of capacitance obtained, through simulation of the circuit of Fig. 3.7, for various values of V_{b2} have been provided in Table 3.3.

Table 3.3: Variation in capacitance with V_{b2}

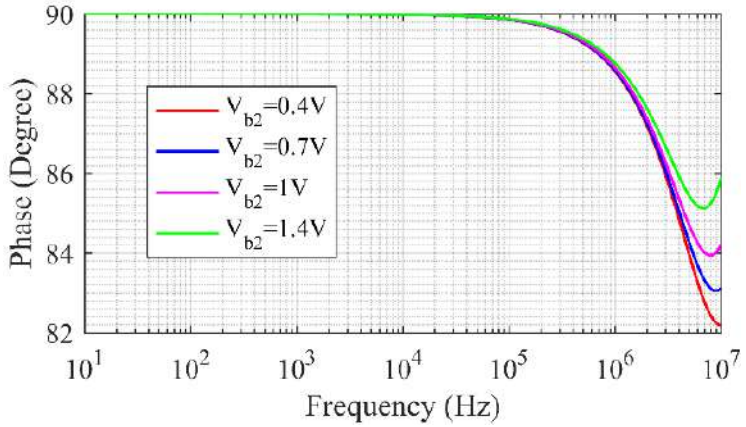
V_{b2}**(V)**	C_{eq}**(simulated) (nF)**	C_{eq}**(theoretical) (nF)**
0.4	14.617	14.75
0.7	10.888	11
1	7.171	7.25
1.4	2.232	2.25

The variation of magnitude and phase of MOS-C CM with temperature has been depicted in Fig. 3.20a and 3.20b respectively.
The histogram of equivalent capacitance realized by using MOS-C equivalent of positive CM circuit with 10% tolerance in C_0 is depicted in Fig.3.21.

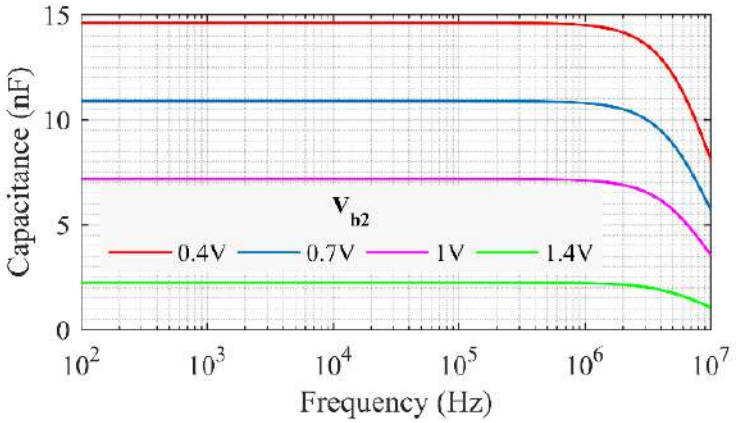
From Fig. 3.19, it is noted that the performance of CM circuit of Fig. 3.7 is found to be satisfactory up to a frequency of 1MHz. In this range of operation, the CM circuit of Fig. 3.7 is insensitive to temperature variations also, as can be observed from Fig. 3.20a and 3.20b. The results of Monte Carlo analysis (Fig. 3.21 of the CM circuit of Fig. 3.7 reveals that the deviation in the value of capacitance realized by varying C_0 is 0.8pF around the designed value.



(a)



(b)

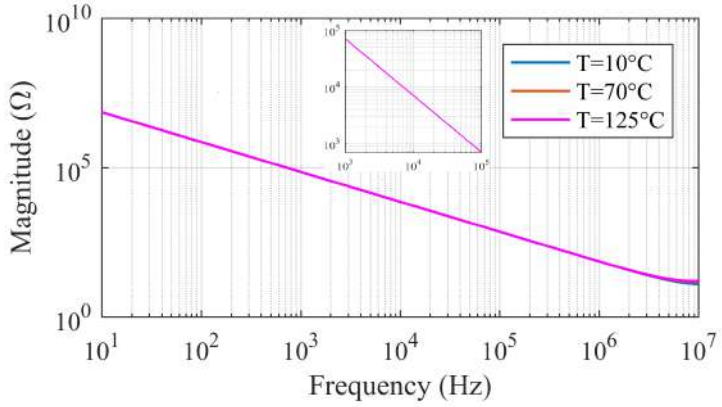


(c)

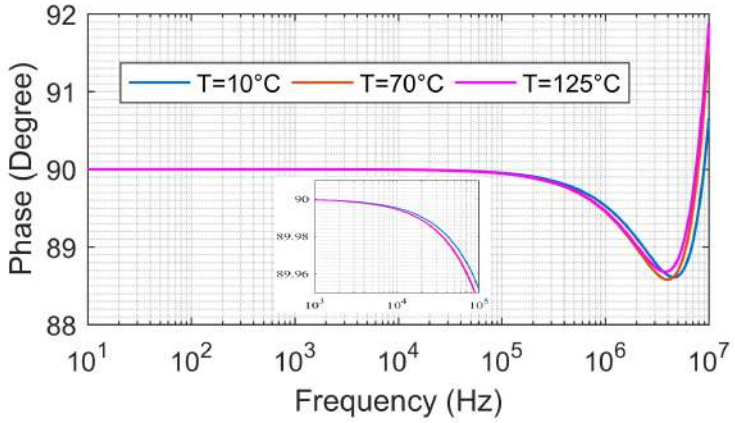
Figure 3.19: (a) Magnitude and (b) phase of impedance and (c) capacitance for MOS-C CM circuit

3.2.0.8 Time and Frequency Responses of Capacitance Cancellation Scheme and First-Order LPF

The performance of the proposed negative grounded CM has been tested with the capacitance cancellation circuit shown in Fig. 3.8. The negative capacitance was



(a)



(b)

Figure 3.20: Variation of (a) Magnitude and (b) phase of impedance with temperature for MOS-C CM circuit

realized with the circuit given in Fig. 3.5 by removing the resistance R_3 (thus realizing a negative capacitance). A sinusoidal input voltage with peak to peak amplitude of 100mV and a frequency of 100 kHz is applied with $R_a = R_b = 10\Omega$, and $C_C = 9$nF. The component values for the realization of negative grounded capacitance were taken as $R_1 = 10\text{k}\Omega$, $R_2 = 1\text{k}\Omega$ and $C_0 = 1$nF. The current waveforms through R_a and R_b are shown in Fig. 3.22. The fact that the waveforms are in phase proves that the parasitic capacitance has been cancelled by the proposed grounded negative CM circuit.

The performance of the first order low pass filter shown in Fig. 3.9 was tested by choosing resistance R = 1 kΩ while the value of capacitance was varied using the proposed positive grounded CM. Values of $C_{eq} = 101$nF, 26nF, 13.5nF and 6nF

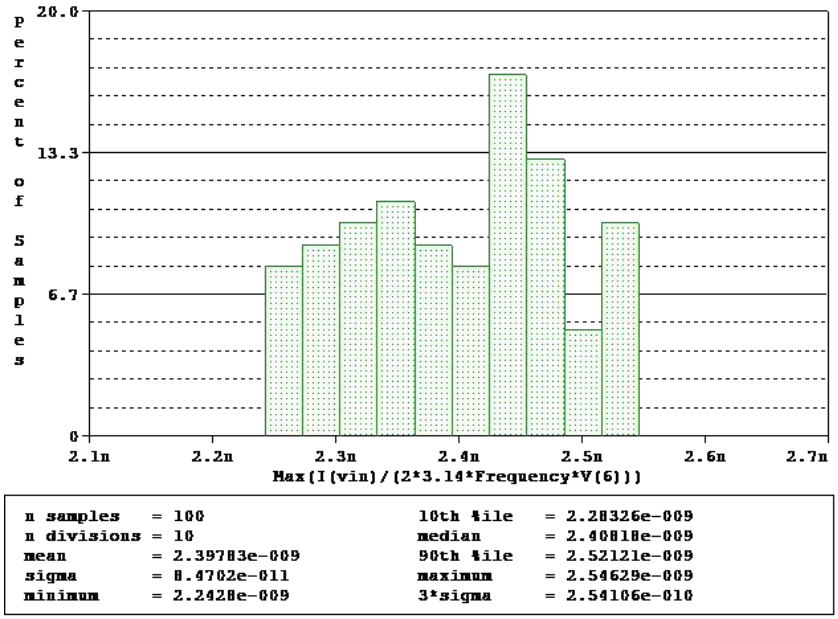


Figure 3.21: Histogram of equivalent capacitance realized by using MOS-C equivalent of positive CM with 10% tolerance in C_0

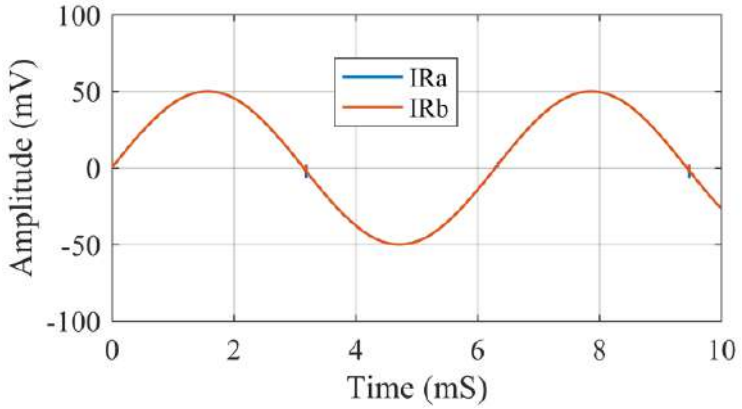


Figure 3.22: Transient responses for current through R_a and R_b

were obtained by changing the value of resistance R_2 as 0.5kΩ, 2kΩ, 4kΩ and 10kΩ respectively, as shown in Fig. 3.5. The values of other passive components in Fig.3.5 were taken as $R_1 = 50\text{k}\Omega$, $R_3 = 25\text{k}\Omega$ and $C_0 = 1\text{nF}$. The frequency responses of the filter depicting the tunability of capacitance and hence, pole frequency with variation in R_2 are shown in Fig. 3.23.

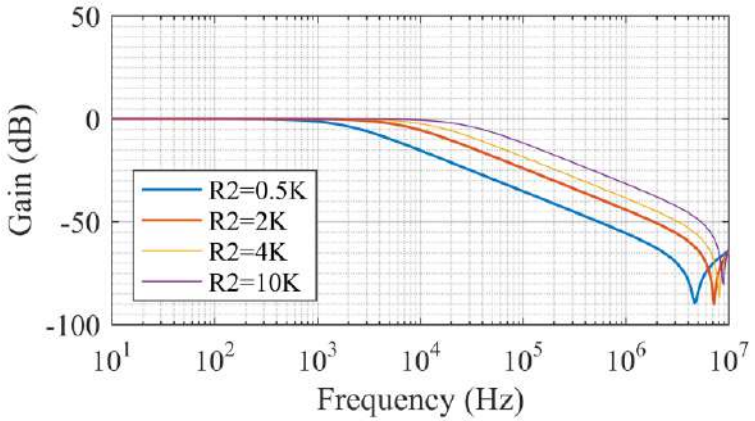


Figure 3.23: Simulated frequency responses of LPF for different multiplication factors

3.2.0.9 Experimental Results

In order to verify the performance of the proposed CM circuit experimentally, the LPF circuit was breadboard using two analog ICs AD844 to implement the OTRA as shown in Fig. 3.24. The DC power supply voltages of value ± 5V were used to bias the AD844. A pole frequency of 15.9kHz has been realized by employing R = 100Ω and C_{eq} = 101nF in the filter configuration depicted in Fig. 3.9. This value of C_{eq} has been obtained using the values of passive components as R_1 = 100kΩ, R_2 = 1kΩ, R_3 = 50kΩ and C_0 = 1nF in the circuit of Fig. 3.5. The experimental frequency response of the filter is shown in Fig. 3.25 and the transient response of input (yellow color) and output (green color) voltages at 100Hz are displayed in Fig. 3.26. The experimentally obtained pole frequency is around 15.14kHz which is very close to the designed pole frequency of 15.9kHz.

The simulation and experimental results from Fig. 3.10 – Fig. 3.26, thus, validate the functionality of the proposed grounded capacitance multiplier circuit.

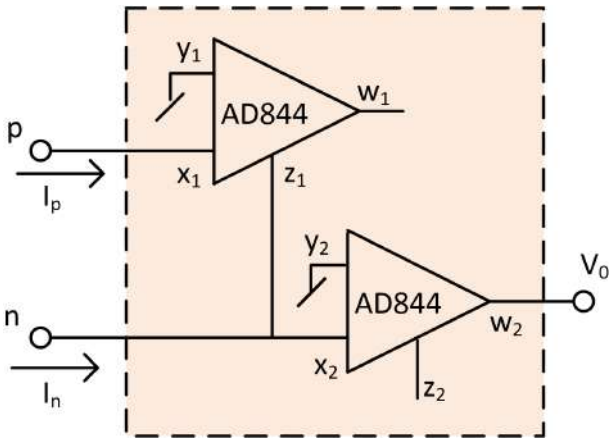


Figure 3.24: CFOA implementation of OTRA [33]

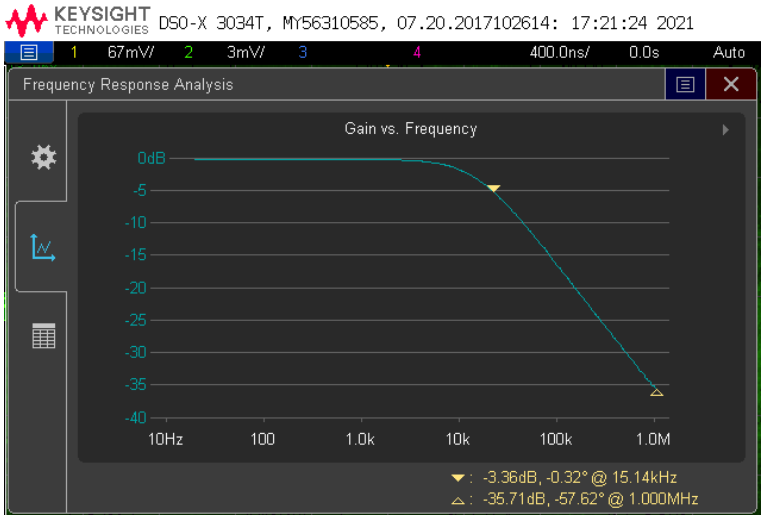


Figure 3.25: Experimental frequency response of first-order low-pass filter

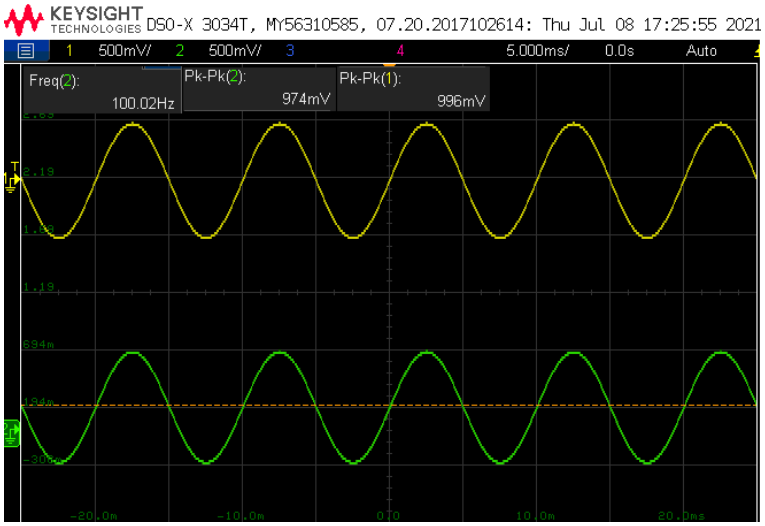


Figure 3.26: Transient responses of first order low-pass filter

3.3 Concluding Remarks

The main contribution in this chapter can be summarized as follows:

This chapter deals with a new realization of analog capacitance multiplier using single OTRA. The proposed circuit employs one OTRA, one voltage buffer, three virtually grounded resistors and a capacitor. The presented circuit provides both positive as well as negative multiplication factors of a grounded capacitor with the proper selection of resistances. Furthermore, the proposed circuit has also been converted into MOS-C configuration replacing passive resistors by identical MOS transistors operating in linear region. Non-ideal analysis incorporating the parasitic of the OTRA has also been carried out and compared those with the obtained ideal values. The application examples of proposed capacitance multiplier in capacitance cancellation and first order low pass filter have also been provided. Simulation results using CMOS OTRA implemented with 0.18 μm TSMC technology parameters have been presented to validate the workability of the proposed capacitance multiplier circuit. Various advanced analyses i.e., Monte-Carlo simulations, process corner and temperature analysis have been carried out for the justification of robustness of the proposed circuit. Experimental results demonstrating the application of a first-order low-pass filter, in which an OTRA implementation employing IC AD844 has been used, have also been presented.

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Chapter 4

New Realizations of Voltage Mode Second Order Biquadratic Filter Configurations

4.1 Introduction

In the previous chapters, we have proposed two circuits of grounded lossy active inductor simulators and a grounded capacitance multiplier circuit employing OTRA. In this chapter, a literature survey of OTRA-based biquadratic filters has been presented and three new realizations of second-order biquadratic filter configurations employing OTRAs are proposed.

Over the years, analog active filters have played a vital role in the implementation of continuous time signal processing circuits. Consequently, researchers have reported numerous configurations of active filters employing classical operational amplifiers, current conveyor and its variants, current feedback operational amplifiers (CFOA) and various other modern active building blocks (ABBs) viz. , current differencing buffered amplifiers (CDBA), operational transconductance amplifiers (OTA), current differencing transconductance amplifiers (CDTA), and many more ABBs.

Because of the presence of virtual ground at the input terminals of the OTRA, the effect of parasitic impedances of these terminals can be eliminated. As a consequence, OTRA has received prominent attention in the design of active filters, oscillators and other non-linear analog applications. Also, its low output impedance facilitates easy cascadability for the voltage mode operations.

Analog active filters can be categorised on the basis of (i) the order of the filters (first order, second order and higher order) and (ii) the number of inputs and outputs (single-input single-output (SISO), multiple-inputs single output (MISO), single-input multiple-outputs (SIMO), and multiple-inputs multiple-outputs (MIMO)).

Since, the work presented in this chapter deals with active analog filter circuits realised with OTRAs, therefore, it is worthwhile to present a comprehensive account of the various reported active analog filters realized with OTRAs to put the work of this chapter in the proper perspective.

4.1.1 First Order Filters using OTRAs

In [1], **Cam, Cakir** and **Cicekoglu** presented an OTRA-based first-order transimpedance mode all-pass filter configuration using a single OTRA and four admittances as shown in Fig. 4.1. In this reported circuit, the intrinsic property of OTRA

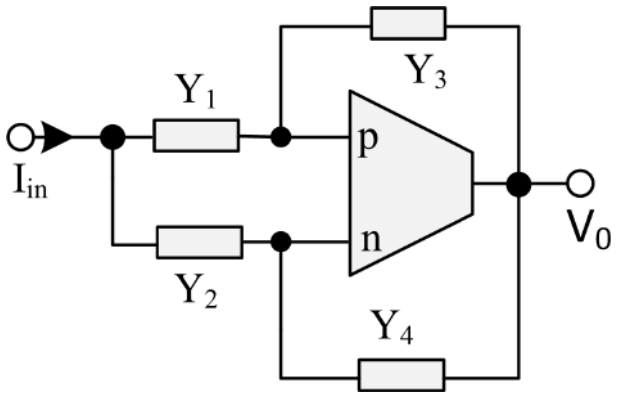


Figure 4.1: Single OTRA-based generalized topology to realize first-order filters [1]

has been fully utilised. With the appropriate choices of the four admittances, two different filter realizations have been presented. The reported filters do not require

any component matching constraints and also provide independent gain tunability feature. PSPICE simulation results have been presented to validate the functionality of these filters using CMOS OTRA implemented with 1.2μm MIETEC MOS parameters.

In [2], **Cakir, Cam** and **Cicekoglu** reported a generalized filter structure employing a single OTRA and four admittances. With the appropriate (resistive/capacitive) choice(s) of four admittances inverting/ non-inverting first order all pass filters (APF), a second order APF and a band reject filter have been presented. An application example of the these filters, wherein a quadrature sinusoidal oscillator has been constructed by cascading two APFs alongwith two unity gain voltage buffers, has also been presented. Workability of these filters has been verified in PSPICE using CMOS OTRA implemented using 0.5μm MIETEC CMOS technology parameters.

Another single OTRA-based all-pass filter configuration has been reported by **Kilinc** and **Cam** in [3], employing three admittances. This configuration provides inverting as well as non-inverting type first-order all-pass filters with appropriate(resistive/capacitive) selection(s) of three admittances. PSPICE simulations were carried out employing CMOS OTRA to validate the feasibility of these filters. Experimental results were also appended in the application of quadrature oscillator wherein OTRA was implemented with two AD844 ICs.

In [4], three new current mode first order all pass filter configurations using single OTRA, one/two resistors and one capacitor have been reported by **Kacar**. The first configuration uses equal valued resistances to realize a first-order all-pass filter. In only one of the reported filter structures, the author has fully utilised the intrinsic property of OTRA, whereas in the remaining two configurations, the intrinsic property of the OTRA has not been utilized, as one of the input terminals of OTRA

is left open. All the filter circuits were tested using PSPICE simulations wherein a CMOS OTRA implemented with 0.35μm CMOS TSMC parameters was used.

A voltage mode first order multifunctional filter configuration was presented by **Banerjee, Ranjan** and **Paul** in [5]. The reported configuration employs three OTRAs, two equal valued capacitors and six equal valued resistors. The reported circuit is non-canonic due to employment of three capacitors for the realization of first-order filter functions. PSPICE simulation results, using a CMOS OTRA implemented with 0.5μm CMOS (MOSIS) parameters, were presented to validate the theoretical propositions.

Another first-order universal active filter has been reported by **Gahalawat, Kumar, Kamnani, Dagar** and **Pandey** in [6]. The presented structure utilises single OTRA, three resistors and two capacitors. This circuit is also non-canonic (because of the use of two capacitors for the realization of a first-order filter). The authors also presented MOS-C implementation of this first-order universal active filter by replacing passive resistors with MOS transistors operating in the triode region. PSPICE simulations using a CMOS OTRA implemented with 0.5μm MOSIS technology parameters, were also presented to test the workability of the presented circuits.

4.1.2 Second Order Filters using OTRAs

4.1.2.1 Single-Input-Single-Output Biquads

Gocken and **Cam** in [7] presented a single OTRA-based generalized structure employing three admittances for the realization of second-order filter(s) as shown in Fig.4.2 . With appropriate choice(s) of admittances (resistances/ capacitances or combination of these), the reported configuration provides all the five filter functions. The filter parameters of the presented circuits are not independently controllable. Furthermore, the MOS-C implementation of the reported circuits has also been presented, making the filter parameters electronically tunable. PSPICE simulations

using CMOS OTRAs were also presented to validate the presented filter functions.

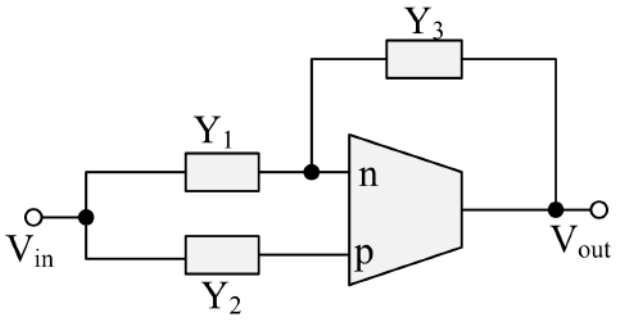


Figure 4.2: Single OTRA filter topology presented by Gocken and Cam [7]

A Fleischer-Tow type biquad has been presented by **Gokcen, Kilinc** and **Cam** in [8] employing three OTRAs, seven resistors and two capacitors. The intrinsic property of the OTRA was not utilized in the realization. Passive component matching conditions were needed for implementing all the five generic filter functions. The presented circuits contained provision of independent tuning of resonant frequency and the pole quality factor. MOS-C version of the presented circuit was also provided. All the filter functions were verified by simulations in PSPICE using a CMOS OTRA.

A voltage mode biquadratic filter configuration has been reported in [9] by **Pandey, Pandey, Singh, Jain** and **Paul**. The reported circuit employs a single OTRA and five admittances as shown in Fig. 4.3. It may be noted from the figure that one of the input terminals(p) of the OTRA has been connected to ground, thus remains unutilized. The presented circuit can provide only three filter functions namely LP, HP and BP filter responses by appropriate choices of admittances. Two of the filter functions (LP and BP) represent canonic realization while the HPF employs three capacitors, thus, is not canonic. PSPICE simulations employing CMOS OTRA implemented with 0.5μm has been used to validate the functionality of the presented filter functions.

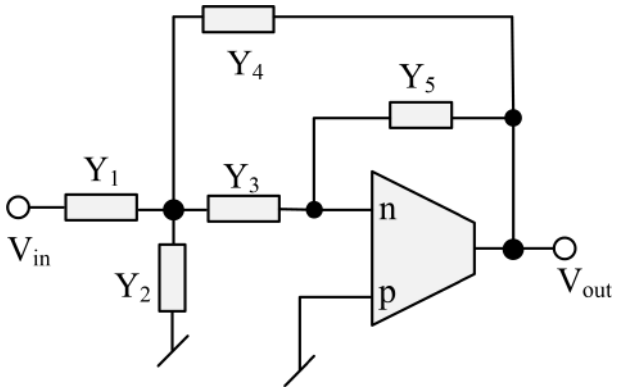


Figure 4.3: Voltage-mode biquadratic filter configuration presented in [9]

In [10], **Pandey, Pandey, Paul, Singh** and **Jain** came up with another configuration of voltage mode biquadratic filter using a single OTRA and six admittances as shown in Fig. 4.4. This circuit also, provides only three filter functions as presented in [9], but utilises the intrinsic property of OTRA. As compared to [9], all three filter functions are canonic in terms of the number of capacitors used. The quality factor (LP and HP)/ bandwidth (BP) of the presented filter can be controlled independently. PSPICE simulations employing CMOS OTRA have been carried out to verify the workability of the presented filters.

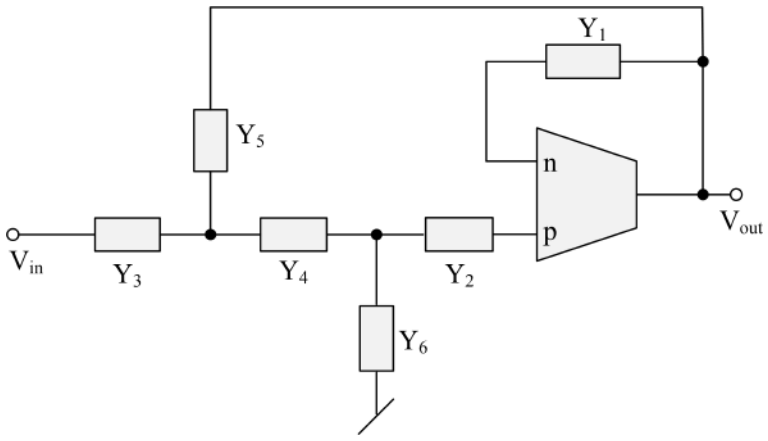


Figure 4.4: OTRA based Sallen Key biquadratic filter configuration reported in [10]

In [11], **Bhatt** and **Shekhar** presented a realization of second order all pass filter employing a single OTRA, four capacitors and four resistors. By appropriately selecting the passive component values a (i)Butterworth, (ii)Chebychev and (iii)Bessel

type APF can be realized. The performance of these filter responses has been validated using PSPICE simulations employing CMOS OTRA.

4.1.2.2 Single-Input-Multiple-Output Biquads

In [12], **Soliman** and **Madian** presented an active-RC version of classical KHN biquad using three OTRAs, six resistors and two capacitors as shown in Fig. 4.5. The reported circuit provides three filter responses namely, high pass (HP), low pass (LP) and inverting band pass (BP) at three low output impedance nodes of the OTRAs. The authors have also provided a MOS-C implementation of the proposed circuit where the resistors were simulated by MOSFETs operating in linear region and having complete non-linear cancellation. The realized filters were tested in PSPICE using CMOS OTRA.

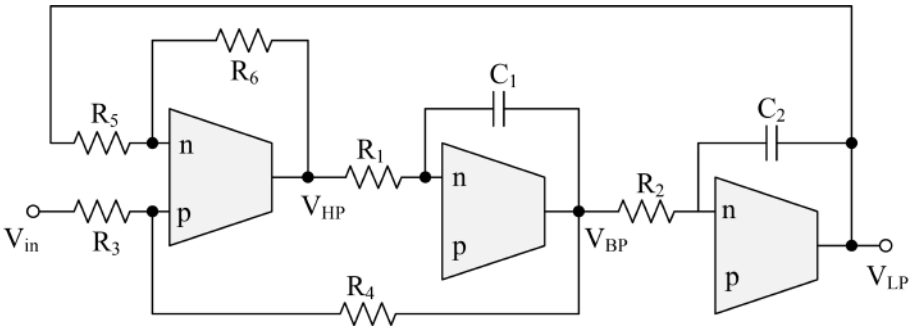


Figure 4.5: KHN biquad using OTRAs presented by Soliman and Madian [12]

Two transresistance mode universal filter circuits employing OTRAs have been reported by **Chada** and **Arora** in [13]. One of these circuits is based on SIMO-type topology, while the other is based on MISO-type topology. All the five second order filter responses, namely, LP, HP, BP, band elimination(BE) and AP, are available in transresistance mode in both the circuits. Orthogonal tunability of the pole frequency (ω) and the quality factor (Q) is possible while gain is fixed in both the configurations.

In [14], **Soliman** and **Madian** presented the MOS-C implementation of the classical Tow-Thomas biquad circuit using two OTRAs, two capacitors and eight MOSFETs.

The validation of the proposed circuit was carried out using PSPICE simulations wherein the OTRA was implemented with two AD844 ICs.

In [15], **Senani, Singh, Gupta** and **Bhaskar** have presented two OTRAs and four resistors based active-R realization of inverting LP and BP filter as shown in Fig. 4.6. The realization utilizes the poles of OTRAs to replace the capacitors. All the three filter parameters namely, pole frequency, quality factor and gain of the proposed band pass filter can be controlled independently through different resistors. The reported filter circuit has been derived from an oscillator circuit simply by changing the polarities of the OTRA. It may be mentioned that one terminal of one of the OTRAs is left open, thus the circuit does not fully utilize the intrinsic property of the OTRA. The workability of both the circuits was verified using PSPICE simulations employing CMOS OTRAs.

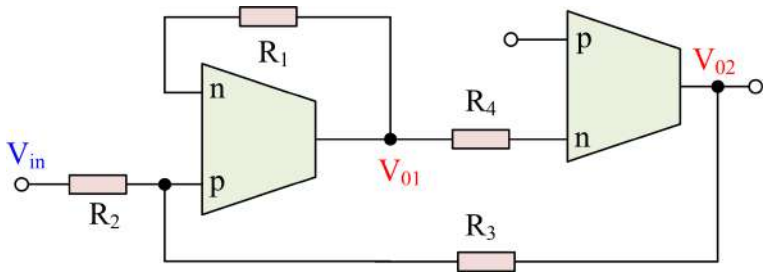


Figure 4.6: LP/BP filter employing two OTRAs [15]

In [16], **Pandey, Pandey, Anurag** and **Vijay** presented a signal flow graph (SFG) based approach for the realization of SIMO type filters employing differentiators. The circuits were realized with OTRAs, resistors and capacitors. The presented circuits have been classified into two categories: one topology realizes the LP, inverting BP and the inverting HP functions in voltage mode, while the other structure realizes inverting LP, BP and the HP responses in voltage mode. A total of sixteen variants have been derived from the proposed differentiator based SFG. All these structures employ three OTRAs, six resistors and two capacitors and provide independent ad-

justment of the filter performance parameters. But in all these realizations, one of the input terminals of the OTRA has been left open.

In [17], **Chang, Lin, Hsu, Hou** and **Horng** presented an analytical synthesis method, which is based on the state variable approach of active network synthesis, to realize a multifunction biquad filter using three OTRAs, two capacitors and six resistors. Three filter functions, namely, the HP, inverting BP and the LP are available at the output of the three OTRAs. As the capacitors are not placed in the feedback around the OTRAs, these capacitors do not introduce additional parasitic poles in conjunction with the finite transresistance of the OTRAs. A MOS-C version of the circuit where all the resistors have been replaced by MOS resistors has also been presented.

A voltage mode biquad filter employing three OTRAs, six resistors and two capacitors realizing LP, BP and HP responses has been presented by **Kumngern, Junnapiya** and **Chanwutitum** in [18] as shown in Fig. 4.7. No component matching constraint is required for the realization of filter functions and the filter parameters are independently tunable.

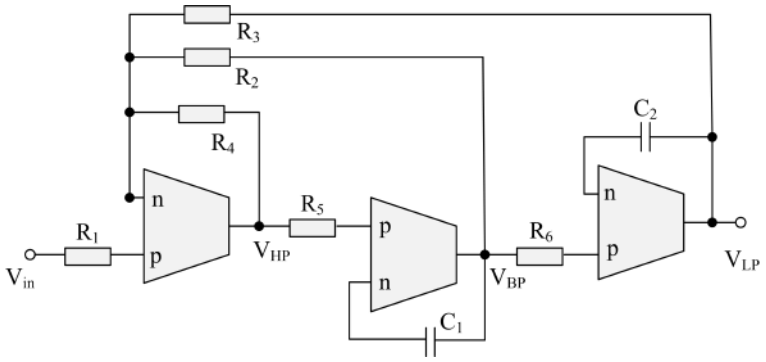


Figure 4.7: OTRA based universal filter presented in [18]

Pandey, Pandey, Paul, Singh, Sriram and **Trivedi** in [19], reported a universal filter topology employing five OTRAs, twelve resistors and two capacitors. The

pole frequency and the pole quality factors of the realized filters are orthogonally tunable while the gain can be tuned independently. Passive components matching constraints have been prescribed for the realization of band reject and all pass filter responses. MOS-C implementation of the universal filter has also been provided.

4.1.2.3 Multiple-Input-Single-Output Biquads

A voltage mode single OTRA-based second order multifunction filter was presented by **Kilinc, Keskin** and **Cam** in [20]. The presented configuration has been shown in Fig. 4.8. With the appropriate choice(s) of the input signals, all the five filter functions can be obtained. A CMOS OTRA implemented with 1.2μm CMOS technology parameters has been used in PSPICE simulations to demonstrate the workability of the presented circuit.

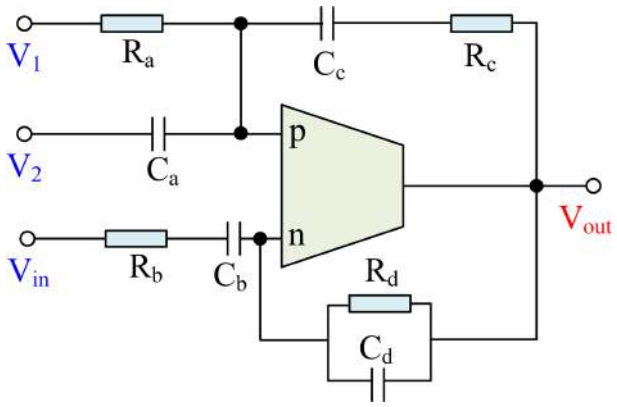


Figure 4.8: Voltage mode MISO type universal filter configuration employing single OTRA [20]

A MISO-type biquad filter was presented by **Mullick, Pandey** and **Pandey** in [21] which can realize all the second order filter functions by appropriate selection(s) of input voltages. The pole quality factor of the realized filters is independently controllable without affecting their pole frequency. The presented circuit was simulated in PSPICE using CMOS OTRA implemented with 0.5μm CMOS process parameters.

Another MISO type second order universal filter employing single OTRA and eight

admittances was presented by **Bhatt, Benjwal** and **Joshi** in [22]. The generalized structure can be used to design various types of filters based on Butterworth, Chebyshev and Bessel approximations. PSPICE simulation results using a CMOS OTRA implemented in 0.5μm CMOS technology have been provided which substantiate the reported circuits.

An OTRA based transimpedance type biquadratic filter configuration capable of realizing all five filter functions has been proposed by **Kilinc** and **Cam** in [23] and [24]. The reported circuits have been developed using the basic blocks like integrators and summers working in the transimpedance mode employing OTRAs. A general signal flow graph is provided for the synthesis of transimpedance type second-order biquadratic transfer funtion. This block diagram is then used for the MOS-C implementation of OTRA based transimpedance type biquadratic filter. Simulations were performed in PSPICE using OTRA implemented with AMI 1.2μm CMOS technology parameters.

4.1.2.4 Multiple-Input-Multiple-Output Biquads

A MIMO type second order LP, BP, HP and BR filter configuration, using two OTRAs, three capacitors and four resistors has been presented by **Chang, Ko, Guo, Hou** and **Horng** in [25] which is shown in Fig. 4.9. The reported circuit has been realized through a new analytical synthesis method. MOS-C implementation of the proposed circuit has also been presented.

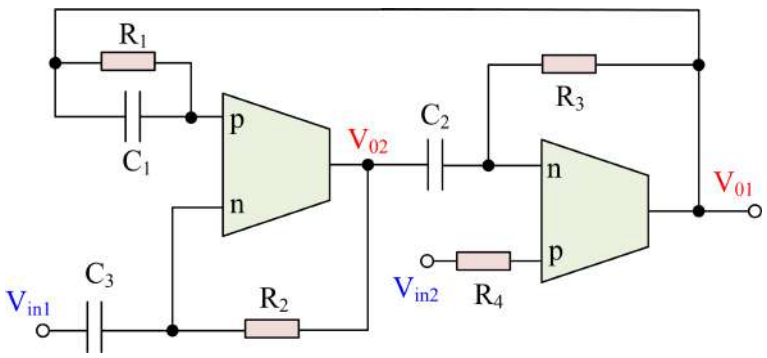


Figure 4.9: OTRA based biquadratic filter presented in [25]

4.1.3 Third and Higher order filters using OTRAs

Chen, Tsao, Liu and **Chiu** in [26] presented a parasitic capacitance insensitive, MOSFET-C integrator and differentiator using OTRA. A universal current-mode biquad using this integrator and another universal current-mode biquad using the proposed differentiator have been presented. Furthermore, a third-order low-pass Chebychev filter has also been presented using the leapfrog synthesis method. The workability of the presented circuits has been tested experimentally using OTRA implemented with three commercially available AD844 ICs.

Kilinc and **Cam** in [27] have presented a new configuration for designing a n-th order voltage transfer function employing a single OTRA and four admittances. The RC-RC decomposition technique has been used for synthesizing the transfer function. As an example of the reported methodology, a third-order all-pass and a third-order low-pass filter have been designed and simulated in PSPICE using the MIETEC 0.5μm CMOS process parameters.

Khachab and **Naeim** in [28] presented a design of fourth order filters using OTRAs. Fourth-order band pass and notch filters have been designed by cascading second order low pass and high pass filters using OTRAs. The performance of the presented circuits were tested using PSPICE simulations employing CMOS OTRA.

OTRA-based MOSFET-C filters based on high order linear transformation have been presented by **Hwang, Chang** and **Lee** in [29]. An exemplary third order Chebyshev low pass filter using the proposed method has also been presented. Experimental results have been provided to validate the theoretical propositions.

A structure similar to [29] has been presented by **Hwang, Wu, Chen, Shih** and **Chou** in [30] as shown in Fig. 4.10. MOSFETs based resistors are used for the design of presented circuits.

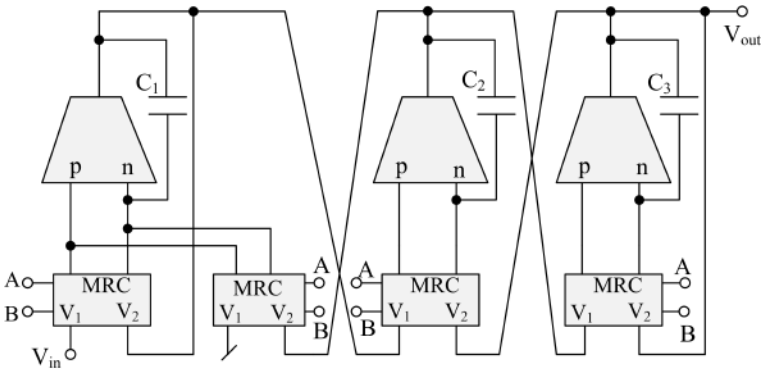


Figure 4.10: OTRA based third-order Chebychev lowpass filter configuration presented in [30]

Electronically tunable, doubly terminated LC ladder-based HPF using a systematic approach was reported by **Pandey, Kumar, Goel** and **Gupta** in [31]. The presented OTRA-based filter is made electronically tunable by replacing the resistors with completely matched MOS transistors operating in the triode region.

Hwang, Wu, Chen, Shih and **Chou** in [32] presented a systematic method and design procedure which can efficiently synthesize third order active filters using MOSFET resistors and all virtually grounded capacitors. Third order current mode Chebychev LPF and HPF have been realized. Commercially available CFOA IC AD844 and CMOS transistor array CA3600 have been used to realize the proposed low-pass filter for experimental verification.

Chang and **Swamy**, [33] presented an analytical synthesis based n-th order approximate elliptical structure using OTRAs which follows an exact mathematical process. Three new analytical synthesis methods have been presented for the realization of n-th order (both odd as well as even) Cauer (elliptic) filters.

Ranjan, Ghosh and **Paul** in [34] have reported two new VM third order asymmetric band pass filter structures using single OTRA, four resistors and four capacitors.

A general third-order asymmetric band-pass filter structure using OTRA as shown in Fig. 4.11 was presented. The same topology has been used to derive the two types of asymmetric transfer functions, simply by the appropriate selection of the passive component values.

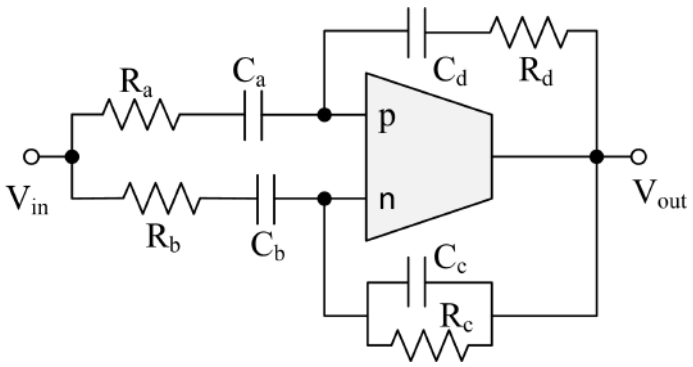


Figure 4.11: OTRA based third-order bandpass filter configuration presented in [34]

Ghosh, Paul and **Ranjan** in [35] have reported a MISO type third order voltage-mode universal filter employing a single OTRA, five resistors and six capacitors. The presented circuit was obtained from a generalized n-th order filter structure using single OTRA and four admittances. The proposed filter is simulated in PSPICE using the CMOS implementation of OTRA.

Ghosh, Paul, Ranjan and **Ranjan** in [36] have presented a MISO-type third order universal filter structure similar to the one presented in [35].

An OTRA based LC–ladder filter implementation using the leapfrog method employing all grounded passive elements has been presented by **Kumari, Gupta, Pandey, Pandey** and **Anurag** in [37]. To verify the theoretical proposition, a sixth-order Chebychev low-pass filter has been simulated using the CFOA-based realization of OTRA.

Two new analytical synthesis methods were presented by **Chang** in [38] for the

design of n-th order high pass filter using OTRAs.

A fifth order video band elliptic filter topology has been reported by **Gocken** and **Cam** in [39]. The presented elliptic filter consists of two lowpass notch filters connected in cascade and a lowpass filter obtained using OTRA based Fleischer-Tow biquad. The MOS-C realization of the filter has also been presented.

From the above description it has emerged that a variety of second order filters employing OTRAs are available in the literature. A careful perusal of the different single OTRA-based filters presented above reveals that:
(i)the number of passive components required for the realization of a particular filter function are non-canonic,
(ii)presence of component matching constraints for the realization of different filter functions and
(iii)incomplete utilization of the input terminals of OTRA, as one of the input terminals is either left open or grounded.
Thus, the main aim of this chapter is to propose:

- new single OTRA-based second order filter configurations employing canonic number of capacitors and relatively lower number of resistors as compared to previously known filters utilising the intrinsic property of the OTRA without imposing any component matching constraints.

- new structures of SIMO type biquad filters using OTRAs which realize LPF, BPF and HPF utilizing the intrinsic (current differencing) property of OTRA. The proposed filters have orthogonal control of the pole frequency (ω_0) and the pole quality factor (Q_0), while the gain of the filters can also be controlled independently.

4.2 Single OTRA based multifunctional filter configuration[1]

Fig. 4.12 shows the proposed single input single output (SISO) type biquad filter configuration.

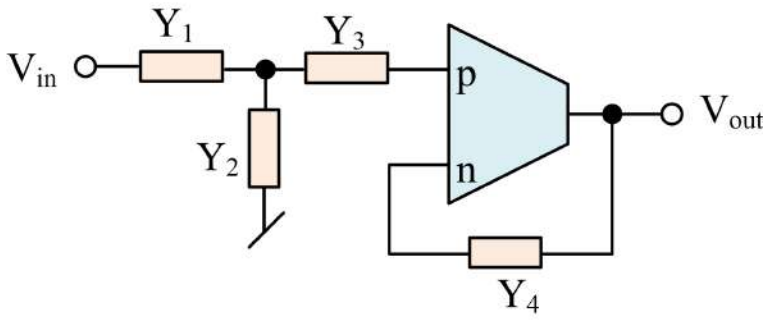


Figure 4.12: Proposed filter configuration

A routine circuit analysis of the circuit shown in Fig. 4.12 (using the ideal terminal relationships of an OTRA), yields the following expression for the voltage transfer function:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{Y_1 Y_3}{Y_4(Y_1 + Y_2 + Y_3)} \tag{4.1}$$

From equation (4.1), various second-order filter responses can be obtained by appropriate selection(s) of branch admittances as given below:

Case I: If we select $Y_1 = G_1, Y_2 = sC_2, Y_3 = G_3$ and $Y_4 = sC_4 + G_4$, a second-order LPF can be obtained whose transfer function is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{\frac{G_1 G_3}{C_2 C_4}}{s^2 + s\left(\frac{G_1+G_3}{C_2} + \frac{G_4}{C_4}\right) + \left(\frac{G_4}{C_2 C_4}\right)(G_1 + G_3)} \tag{4.2}$$

Different filter parameters namely, pole frequency (ω_0), DC gain and quality factor (Q_0)/bandwidth (BW) of the proposed LPF can be derived from equation (4.4)

[1]The material presented in this section has been published in: Garima, Pragati Kumar and D. R. Bhaskar, "Single OTRA based multifunctional filter configuration" 7th IEEE International Conference on Signal Processing and Communications (ICSC), pp. 245-249, 2021, Noida, India.

which are given by:

$$\begin{aligned} \omega_0 &= \sqrt{\frac{G_4(G_1+G_3)}{C_2C_4}} \\ Q_0 &= \frac{\sqrt{C_2C_4G_4(G_1+G_3)}}{C_4(G_1+G_3)+G_4C_2} \\ H_0 &= \frac{G_1G_3}{G_4(G_1+G_3)} \end{aligned} \tag{4.3}$$

Case II: If we select $Y_1 = G_1, Y_2 = G_2, Y_3 = sC_3$ and $Y_4 = sC_4 + G_4$, a second-order BPF can be obtained whose transfer function is given by:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s\left(\frac{G_1}{C_4}\right)}{s^2 + s\left(\frac{G_1+G_3}{C_3} + \frac{G_4}{C_4}\right) + \left(\frac{G_4}{C_3C_4}\right)(G_1+G_2)} \tag{4.4}$$

Hence, for these values of admittances, a BPF can be realized for which ω, BW and H_0 may be expressed as:

$$\begin{aligned} \omega_0 &= \sqrt{\frac{G_4(G_1+G_2)}{C_3C_4}} \\ BW &= \frac{G_1+G_2}{C_3} + \frac{G_4}{C_4} \\ H_0 &= \frac{G_1C_3}{C_4(G_1+G_2)+C_3G_4} \end{aligned} \tag{4.5}$$

Case III: For HPF function realization, the admittances were selected as: $Y_1 = \frac{sC_1G_1}{G_1+sC_1}, Y_2 = G_2, Y_3 = sC_3$ and $Y_4 = G_4$, and the transfer function can be expressed as:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{s^2\left(\frac{G_1}{G_4}\right)}{s^2 + s\left(\frac{G_1+G_3}{C_3} + \frac{G_1}{C_1}\right) + \left(\frac{G_1G_2}{C_1C_3}\right)} \tag{4.6}$$

The filter parameters of HPF can be obtained from equation (4.6) and may be expressed as:

$$\begin{aligned} \omega_0 &= \sqrt{\frac{G_1G_2}{C_1C_3}} \\ Q_0 &= \frac{\sqrt{C_1C_3G_1G_2}}{G_1(C_1+C_3)+G_2C_1} \\ H_0 &= \frac{G_1}{G_4} \end{aligned} \tag{4.7}$$

in all the cases $G_i = \frac{1}{R_i}$

4.2.0.1 Non-Ideal Analysis

The consequences of major non-idealities present in the OTRA on the realized filter are considered in this section. We have used the single pole model of trans-resistance

gain R_m [40] as given in equation (4.8) to evaluate the non-ideal filter parameters:

$$R_m(s) = \frac{R_0}{1 + \frac{s}{\omega_0}} \tag{4.8}$$

For high frequency applications, R_m(s) reduces to:

$$R_m(s) = \frac{1}{sC_p} \; where \; C_p = \frac{1}{R_0\omega_0} \tag{4.9}$$

Using the above non-ideal model of the OTRA, the transfer function of the proposed structure of Fig. 4.12 may be expressed as:

$$\frac{V_{out}^{/}}{V_{in}^{/}} = \frac{Y_1Y_3}{Y_4(Y_1+Y_2+Y_3) + sC_P(Y_1+Y_2+Y_3)} \tag{4.10}$$

From equation (4.10), the non-ideal transfer functions and parameters of each filter functions can be derived. The non-ideal transfer function of LPF is given by:

$$\frac{V_{out}^{/}(s)}{V_{in}^{/}(s)} = \frac{\frac{G_1G_3}{C_2(C_4+C_p)}}{s^2 + s\left(\frac{G_1+G_3}{C_2} + \frac{G_4}{C_4+C_p}\right) + \left(\frac{G_4(G_1+G_3)}{C_2(C_4+C_p)}\right)} \tag{4.11}$$

The non-ideal filter parameters of the LPF may be evaluated from equation (4.11) and are given by:

$$\begin{gathered} \omega_0^{/} = \omega_0\sqrt{\frac{C_4}{C_4+C_p}} \\ Q_0^{/} = \frac{\sqrt{C_2(C_4+C_p)G_4(G_1+G_3)}}{(C_4+C_p)(G_1+G_3)+G_4C_2} \\ H_0^{/} = H_0 \end{gathered} \tag{4.12}$$

Similarly, the non-ideal transfer function for BPF can be expressed as:

$$\frac{V_{out}^{/}(s)}{V_{in}^{/}(s)} = \frac{s\frac{G_1}{(C_3+C_p)}}{s^2 + s\left(\frac{G_1+G_2}{C_3} + \frac{G_4}{C_4+C_p}\right) + \left(\frac{G_4(G_1+G_2)}{C_3(C_4+C_p)}\right)} \tag{4.13}$$

From equation (4.13), the non-ideal filter parameters of the BPF may be evaluated and are given in equation (4.14):

$$\begin{aligned} \omega_0^{/} &= \omega_0 \sqrt{\frac{C_4}{C_4+C_p}} \\ BW^{/} &= \frac{G_1+G_2}{C_3} + \frac{G_4}{C_4+C_p} \\ H_0^{/} &= \frac{G_1 C_3}{(G_1+G_2)(C_4+C_p)+C_3 G_4} \end{aligned} \tag{4.14}$$

The non-ideal transfer function of HPF can also be derived from equation (4.10) and can be expressed as:

$$\frac{V_{out}^{/}(s)}{V_{in}^{/}(s)} = \frac{s^2\left(\frac{G_1}{G_4}\right)}{s^3\left(\frac{C_p}{G_4}\right) + s^2 + s\left(\frac{G_1+G_2}{C_3} + \frac{G_1}{C_1}\right)\left(1+\frac{sC_p}{G_4}\right) + \left(\frac{G_1+G_2}{C_1C_3}\right)\left(1+\frac{sC_p}{G_4}\right)} \tag{4.15}$$

Since in general $\frac{sC_p}{G_4} << 1$, so we can approximate the non-ideal term as:

$$D^{/}(s) = s^2 + s\left(\frac{G_1+G_2}{C_3} + \frac{G_1}{C_1}\right) + \left(\frac{G_1 G_2}{C_1 C_3}\right) \tag{4.16}$$

Thus, the non-ideal HPF parameters are given by:

$$\omega_0^{/} = \omega_0, \quad Q_{NI} = Q_0 \quad and \quad H_{NI} = H_0 \tag{4.17}$$

It can be seen that the parasitic affects the filter parameters of the proposed filter functions and it may be minimized by selecting the value of passive components such that $C_i >> C_p$.

4.2.0.2 Simulation Results

Using CMOS OTRA implemented in 0.18μm CMOS technology [41] as shown in Fig. 4.13, the functionality of the presented filter structures has been validated through MATLAB evaluations along with PSPICE results. The power supply voltages used were $\pm$1.85V. The bias current (I_B) and bias voltage (V_{B1}) of CMOS OTRA were taken as 18μA and 0.36V respectively. The aspect ratios of the MOSFETs shown

in Fig. 4.13 have been provided in Table 4.1.

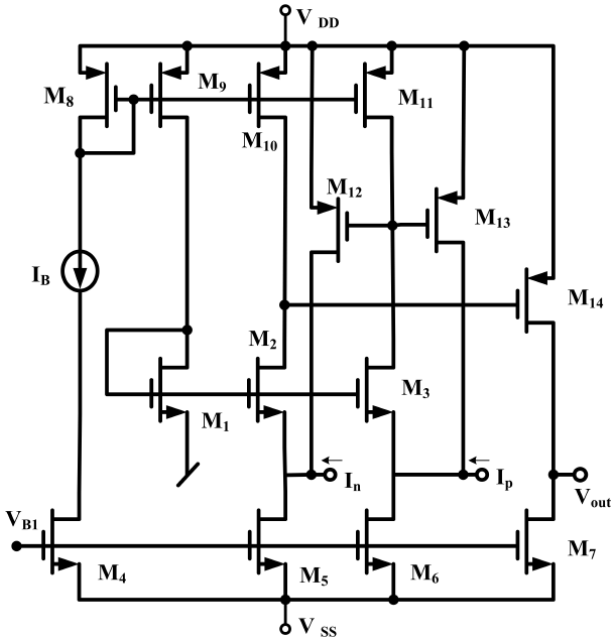


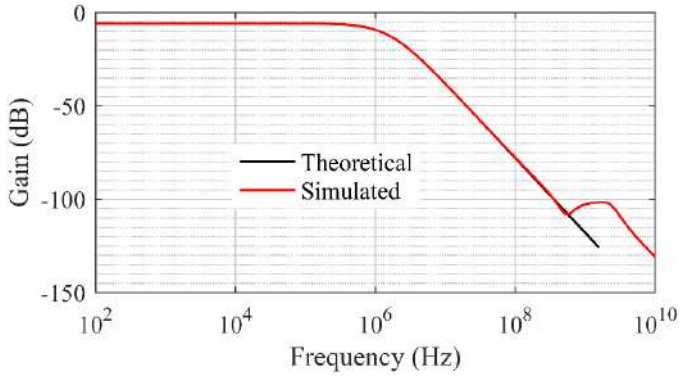
Figure 4.13: CMOS realization of OTRA [41]

Table 4.1: Aspect ratio of MOSFETs shown in Fig. 4.13

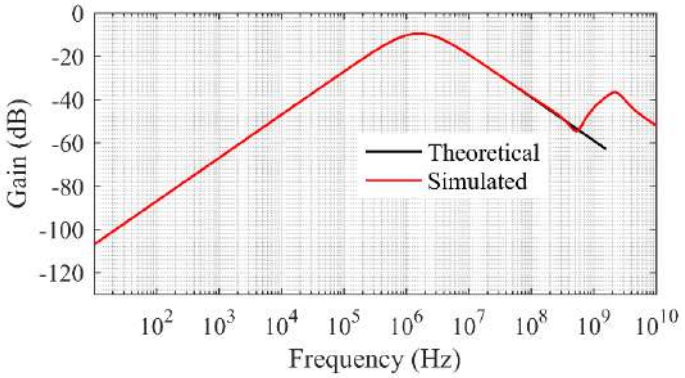
MOSFETs	Aspect Ratio (W/L)
M1-M3, M12, M13	36/0.9
M4, M7	3.6/0.9
M5-M6	10.8/0.9
M8-M11	18/0.9
M14	18/.18

The proposed filter was designed for a nominal value of the pole frequency/centre frequency of 1.59MHz for LPF, HPF and BPF. The passive component values were taken as: $R_1 = R_3 = R_4 = 14.1$ kΩ and $C_2 = C_4 = 10$ pF (for LPF), $R_1 = R_2 = R_4 = 10$ kΩ and $C_1 = C_3 = 10$ pF (for HPF) and $R_1 = R_2 = R_4 = 14.1$ kΩ and $C_3 = C_4 = 10$ pF (for BPF). For these values of passive components, the DC gain and the Q of LPF, HPF and BPF were obtained as (-6dB and 0.4713), (0dB and 0.33) and (-9dB and 0.4713) respectively. The corresponding values of the -3dB frequency of LPF and HPF are 937.46 kHz and 4.25 MHz respectively while the corresponding value for the bandwidth for the BPF is 3.36 MHz. The simulated values of the 3-dB frequencies for LPF, HPF and BPF were found to be 950KHz, 4.008MHz and

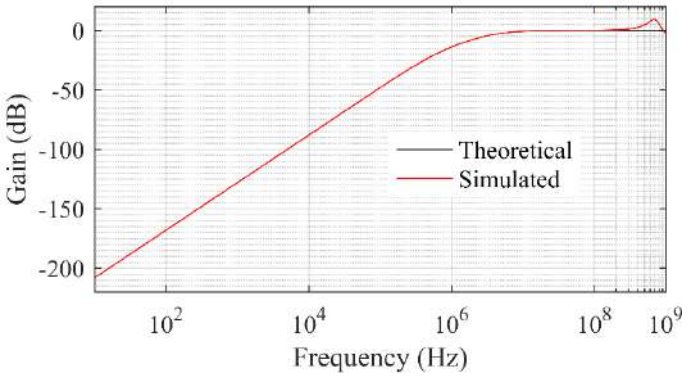
3.24MHz respectively. It may be noted that the 3-dB frequencies of the realized filter are different from the pole frequencies, as the design values of the pole quality factor 'Q' is less than 0.5 (real poles). The simulated PSPICE magnitude responses of different filter functions have been shown in Fig. 4.14 alongwith MATLAB evaluations.



(a)



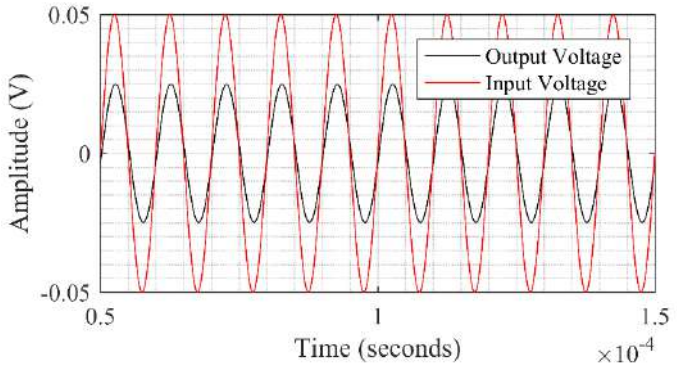
(b)



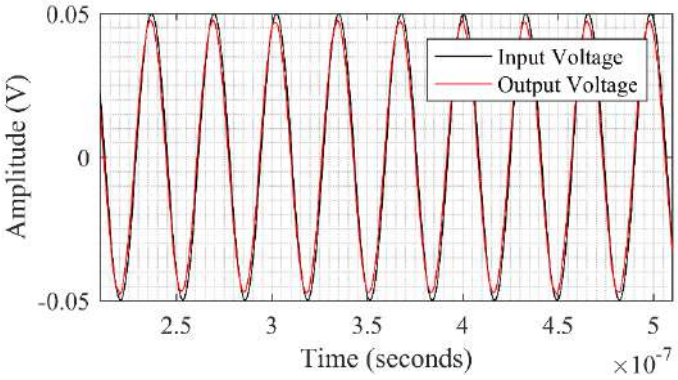
(c)

Figure 4.14: (a) Gain Vs Frequency plot for LPF (b) Gain Vs Frequency plot for BPF (c) Gain Vs Frequency plot for HPF

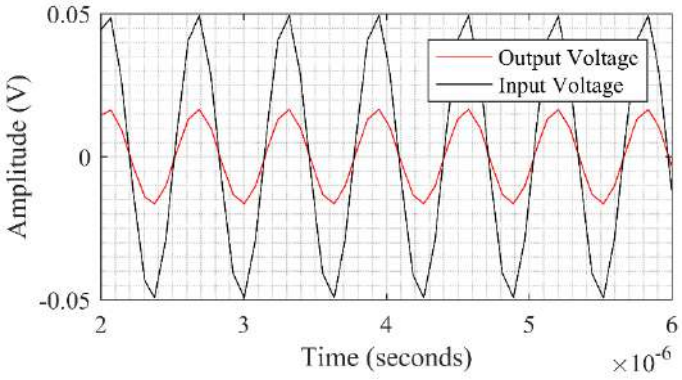
Fig. 4.15 displays the transient responses of the proposed filter functions for the input signal of 50 mV at different frequencies (100 kHz for LPF, 30.59 MHz for HPF and 1.59 MHz for BPF).



(a)



(b)



(c)

Figure 4.15: (a) Time response of LPF (b) Time response of BPF (c) Time response of HPF

The evaluate the quality of the filters, total harmonic distortions (THD) simulations

have been carried out by varying the applied peak input voltage and the respective graphs have been displayed in Fig. 4.16. The simulation results, thus, validate the

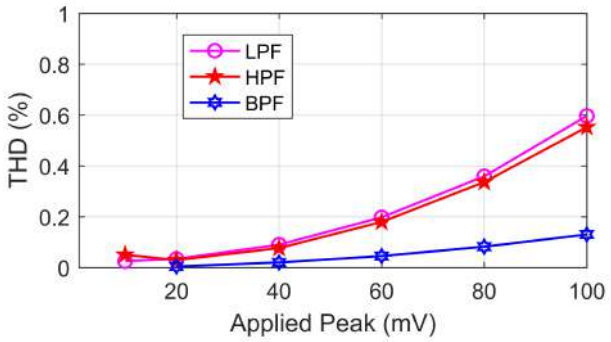
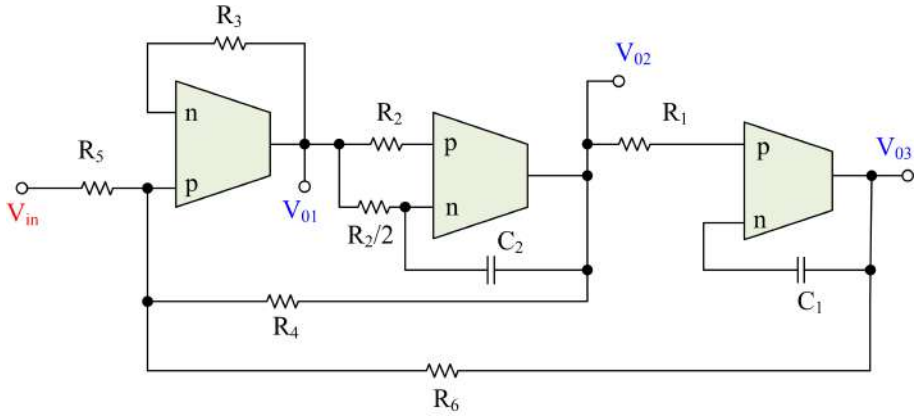


Figure 4.16: Variations in THD with applied peak to peak input voltage

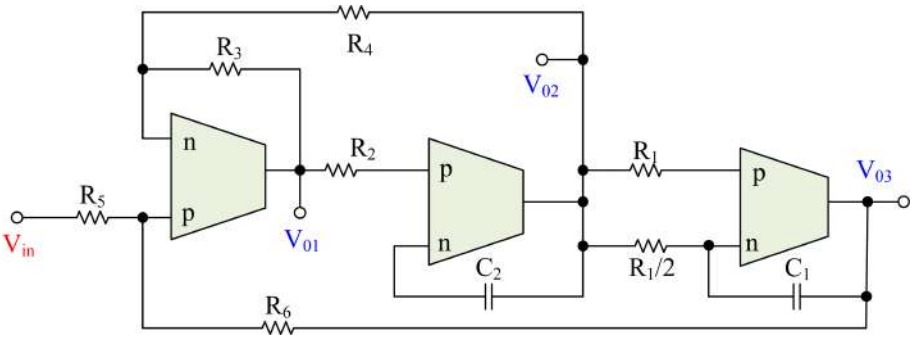
workability of the proposed single-OTRA based biquad filter.

4.3 Realization of SIMO biquad filters and quadrature sinusoidal oscillators using OTRAs[2]

The proposed SIMO type biquad filter configurations have been shown in Fig. 4.17a and 4.17b



(a)



(b)

Figure 4.17: Proposed single input multiple output filter configurations

Analysis of the circuits shown in Fig. 4.17a and Fig. 4.17b, using the port relations of the ideal OTRA, gives the different transfer function of the filters namely high pass filter (HPF), band pass filter (BPF) and low pass filter (LPF) as given by equations (4.18) - (4.20) for Fig. 4.17a while in equations (4.21) - (4.23), the transfer functions

[2]The material presented in this section has been published in: Garima, Pragati Kumar and D. R. Bhaskar, "Realization of SIMO biquad filters and quadrature sinusoidal oscillators using OTRAs" Journal of Engg. Research ICARI Special Issue, pp.161-172, 2021.

of filters shown in for Fig. 4.17b have been provided.

$$\frac{V_{01}(s)}{V_{in}(s)} = \left(\frac{R_3}{R_5}\right)\left(\frac{s^2}{D(s)}\right) \tag{4.18}$$

$$\frac{V_{02}(s)}{V_{in}(s)} = \left(\frac{R_4}{R_5}\right)\left(\frac{s\frac{R_3}{C_2R_2R_4}}{D(s)}\right) \tag{4.19}$$

$$\frac{V_{03}(s)}{V_{in}(s)} = \left(\frac{-R_6}{R_5}\right)\left(\frac{\frac{R_3}{C_1C_2R_1R_2R_6}}{D(s)}\right) \tag{4.20}$$

$$\frac{V_{01}(s)}{V_{in}(s)} = \left(\frac{-R_3}{R_5}\right)\left(\frac{s^2}{D(s)}\right) \tag{4.21}$$

$$\frac{V_{02}(s)}{V_{in}(s)} = \left(\frac{R_4}{R_5}\right)\left(\frac{s\frac{R_3}{C_2R_2R_4}}{D(s)}\right) \tag{4.22}$$

$$\frac{V_{03}(s)}{V_{in}(s)} = \left(\frac{R_6}{R_5}\right)\left(\frac{\frac{R_3}{C_1C_2R_1R_2R_6}}{D(s)}\right) \tag{4.23}$$

where

$$D(s) = s^2 + s\left(\frac{R_3}{C_2R_2R_4}\right) + \left(\frac{\frac{R_3}{R_6}}{C_1C_2R_1R_2R_6}\right) \tag{4.24}$$

The filter parameters, namely, ω_0, Q_0 and bandwidth (BW) can be obtained from equation (4.24), which are given below:

$$\begin{aligned} \omega_0 &= \sqrt{\frac{\left(\frac{R_3}{R_6}\right)}{C_1C_2R_1R_2}} \\ Q_0 &= R_4\sqrt{\frac{C_2R_2}{C_1R_1R_3R_6}} \\ BW &= \frac{R_3}{C_2R_2R_4} \end{aligned} \tag{4.25}$$

From equation (4.25), it may be seen that the Q_0 can be varied by varying R_4 without changing ω_0. On the other hand, the BW can be tuned by changing the value of R_4 without changing the value of ω_0 , which in turn, can be tuned without disturbing the BW by varying either R_1 or R_6.

The gain (H_0) of HPF, BPF and LPF are derived from equations (4.18) - (4.20) and

(4.21) - (4.23) which are given below:

$$\begin{aligned} Fig.4.17a: \quad & H_{0HPF} = \tfrac{R_3}{R_5}, H_{0BPF} = \tfrac{R_4}{R_5}, H_{0LPF} = \tfrac{-R_6}{R_5} \\ Fig.4.17b: \quad & H_{0HPF} = \tfrac{-R_3}{R_5}, H_{0BPF} = \tfrac{R_4}{R_5}, H_{0LPF} = \tfrac{R_6}{R_5} \end{aligned} \tag{4.26}$$

It is clearly seen from equation (4.26) that the gain of HPF, BPF and LPF can be independently controlled simply by varying R_5, without affecting ω_0, Q_0 and BW.

4.3.0.1 Non-ideal Analysis

The consequence of major non-idealities immanent in the OTRA on the realized filters are considered in this section. Taking into account the single pole model for the trans-resistance gain R_m [40], given below as:

$$R_m(s) = \frac{R_0}{1 + \frac{s}{\omega_0}} \tag{4.27}$$

For high frequency applications, $R_m(s)$ reduces to

$$R_m(s) \approx \tfrac{1}{sC_p} \quad where \quad C_p = \tfrac{1}{R_0\omega_0} \tag{4.28}$$

Using this non-ideal model of the OTRA, the non-ideal transfer functions of the filters have been determined as:

$$\frac{V_{03}^{/}(s)}{V_{in}(s)} = \frac{-R_6}{R_5}\left(\frac{R_3R_4}{D^{/}(s)}\right) \tag{4.29}$$

$$\frac{V_{02}^{/}(s)}{V_{in}(s)} = \frac{R_4}{R_5}\left(\frac{R_1R_3R_6(C_1 + C_p)}{D^{/}(s)}\right) \tag{4.30}$$

$$\frac{V_{01}^{/}(s)}{V_{in}(s)} = \frac{R_3}{R_5}\left(\frac{s^2R_1R_2R_4R_6(C_1 + C_P)(C_2 + C_P)}{D^{/}(s)}\right) \tag{4.31}$$

$$\begin{aligned} D^{/}(s) = s^3C_PR_1R_2R_4R_6(C_1 + C_P)(C_2 + C_p) + s^2R_1R_2R_4R_6(C_1 + C_p)(C_2 + C_p) + \\ sR_1R_3R_6(C_1 + C_P) + R_3R_4 \end{aligned} \tag{4.32}$$

It is noted from equation (4.28) that for large values of R_0 (ideally, infinite), the value of C_p will be very small, we may neglect the cubic term in the expression of $D^{/}(s)$. Thus, equation (4.32) now reduces to:

$$D^{/}(s) = s^2 R_1 R_2 R_4 R_6 (C_1 + C_p)(C_2 + C_p) + s R_1 R_3 R_6 (C_1 + C_P) + R_3 R_4 \quad (4.33)$$

From equation (4.33), we can derive expressions for non-ideal pole frequency, quality factor and bandwidth. These expressions are given by equations (4.34), (4.35) and (4.36) respectively.

$$\omega_0^{/} = \frac{\omega_0}{1 + \frac{C_p}{C_1 C_2}(C_1 + C_2 + C_P)} \quad (4.34)$$

$$Q_0^{/} = Q_0 \sqrt{1 + \frac{C_p}{C_1 C_2}(C_1 + C_2 + C_P)} \quad (4.35)$$

$$BW^{/} = BW \frac{1 + \frac{C_p}{C_1}}{\sqrt{1 + \frac{C_p}{C_1 C_2}(C_1 + C_2 + C_P)}} \quad (4.36)$$

It is thus observed that the non-ideal values of the filter parameters deviate little from their ideal values as C_P is very small.

4.3.0.2 Sensitivity Analysis

The tolerances in component values cause deviation in the response of actual filter from the ideal response. Therefore, we have evaluated the sensitivity of filter parameters ω_0, Q_0 and BW with R and C. These sensitivities can be calculated using the classical formula:

$$S_X^{F(x)} = \left(\frac{X}{F(x)}\right) \frac{\partial F(x)}{\partial X} \quad (4.37)$$

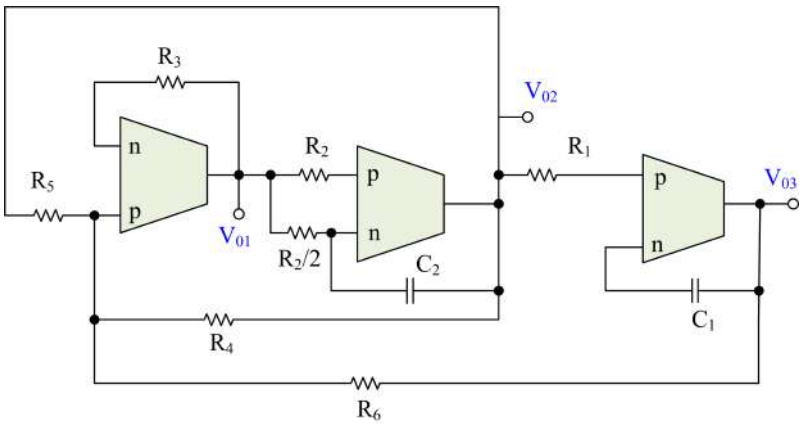
where F(x) denotes a circuit parameter and x denotes parameter of interest.
The sensitivities of ω_0, Q_0 and BW with respect to parameter of interest have been evaluated and tabulated in Table 4.2.

Table 4.2: Sensitivities of filter parameters with respect to various passive components

Parameter	R_1	R_2	R_3	R_4	R_5	R_6	C_1	C_2
$S_x^{\omega_0}$	-0.5	-0.5	0.5	0	0	-0.5	-0.5	-0.5
$S_x^{Q_0}$	-0.5	0.5	-0.5	1	0	-0.5	-0.5	0.5
S_x^{BW}	0	-1	1	-1	0	0	0	-1

4.3.1 Proposed VM Fully Uncoupled Quadrature Sinusoidal Oscillator

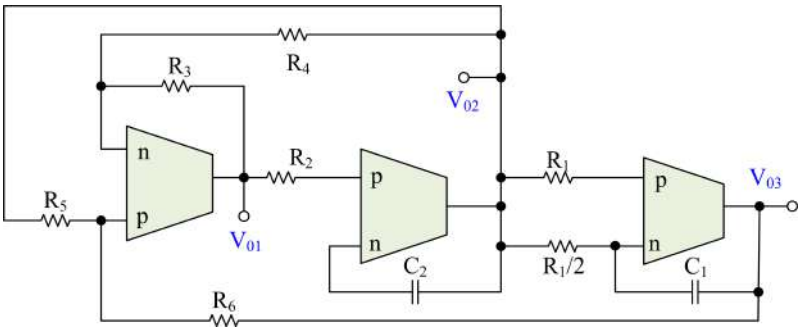
A careful look at the transfer functions given by equations (4.19) and (4.22) reveal that the bandpass filter outputs (V_{02}) available in both the circuits shown in Fig. 4.17 are non-inverting. Thus, these filters can be modified into second order sinusoidal oscillators by simply closing the loop between the input terminals (by removing the external input) and the terminal at which the voltage V_{02} is available. The circuit diagrams of derived sinusoidal oscillators are shown below in Fig. 4.18.



(a)

Assuming ideal OTRAs, routine circuit analysis of Fig. 4.18a and Fig. 4.18b gives the characteristic equation as:

$$s^2 + \left(\frac{R_3}{C_2 R_2}\right)\left(\frac{1}{R_4} - \frac{1}{R_5}\right)s + \frac{R_3}{(C_1 C_2 R_1 R_2 R_6} = 0 \tag{4.38}$$



(b)

Figure 4.18: Proposed quadrature sinusoidal oscillators

The CO and FO of the proposed oscillators can be calulated from equation (4.38) and are given by:

$$\begin{aligned} CO: &\quad R_5 - R_4 \leq 0 \\ FO: &\quad \omega_0 = \sqrt{\frac{\frac{R_3}{R_6}}{C_1 C_2 R_1 R_2}} \end{aligned} \tag{4.39}$$

From equation (4.39), it may be noted out that the proposed oscillator circuits have fully uncoupled control of CO and FO, i.e., CO can be independently set through two resistors R_4 and R_5 without affecting FO which has four degree of freedom to tune independently (using resistors R_1, R_2, R_3 and R_6) and also it can be tuned through capacitors C_1 and C_2.

From the equation of FO, it may be noted that the proposed oscillator has a feature to generate low frequency oscillations which may be done if the ratio of the resistors R_3 and R_6 is selected to be very small by choosing R_6 much larger than R_3. For the circuits of oscillator presented in Fig. 4.18, two quadrature voltages are available, first is between V_{01} and V_{02} and the second, between V_{02} and V_{03}, as can be seen from equations (4.40) and (4.41).

$$\frac{V_{02}(s)}{V_{01}(s)} = \frac{1}{sC_2R_2} \quad \frac{V_{02}(j\omega)}{V_{01}(j\omega)} = \frac{1}{\omega C_2 R_2} e^{-90^\circ} \tag{4.40}$$

$$\frac{V_{03}(s)}{V_{02}(s)} = \frac{1}{sC_1R_1} \quad \frac{V_{03}(j\omega)}{V_{02}(j\omega)} = \frac{1}{\omega C_1 R_1} e^{-90^\circ} \tag{4.41}$$

4.3.1.1 Frequency Stability of the Quadrature Oscillators

For an oscillator, frequency stability is an essential figure of merit. It measures the capability of an oscillator to maintain its fundamental frequency constant for a long period. The frequency stability S^F is defined as:

$$S^F = \frac{\partial \phi(u)}{\partial u} \tag{4.42}$$

where $u = \frac{\omega}{\omega_0}$ and ϕ is the phase of the open loop transfer function of an oscillator. We have used the open loop transfer function of BPF given in equation (4.19) to calculate the frequency stability factor and found it to be -2n, when $R_1 = R_2 = R_3 = R_6 = \frac{R}{n}, R_4 = R_5 = R$, and $C_1 = C_2 = C$. The calculated S^F shows that the FO has a very high frequency stability, when the value of n is made very large.

4.3.1.2 Simulation and Experimental Results

Validation of the proposed filters and oscillator circuits has been done through simulation using PSPICE and the same have been verified through experimental results also. A discrete implementation of the OTRA using two current feedback operational amplifiers (CFOAs) ICs, AD844 [42] as shown in Fig. 4.19, was used in SPICE simulations as well as experimental verification of the results. The power supplies used were ± 5V.

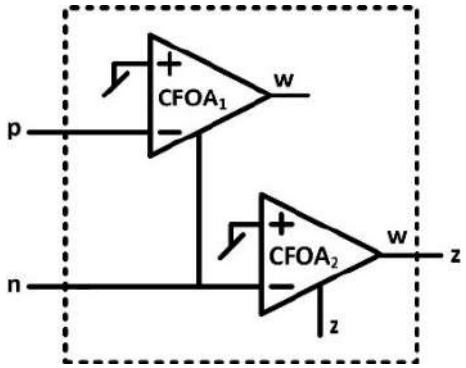


Figure 4.19: CFOA implementation of OTRA

In the following, we present the simulation and experimental results for the filter cir-

cuit shown in Fig. 4.17 and the sinusoidal oscillator circuit shown in Fig. 4.18. The filters were designed for a nominal ω_0 of 15.9kHz, Q_0 of 1, BW (for BPF) =15.9kHz and gain 1. The passive components used were: R_i = 10kΩ (where i = 1 to 6) and $C_1 = C_2$ = 1nF. The experimental frequency responses of filters obtained on Keysight DSOX3034T superimposed on the simulated frequency response obtained using PSPICE, have been shown in Fig. 4.20.

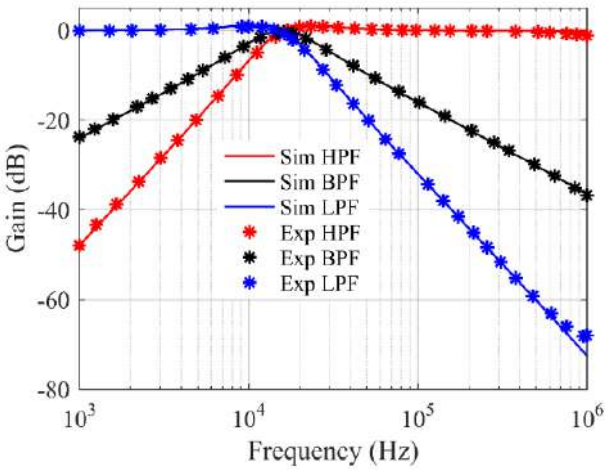
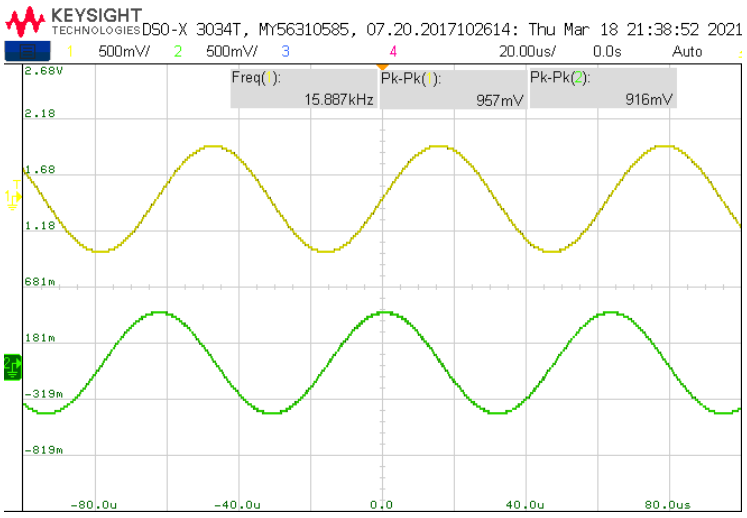
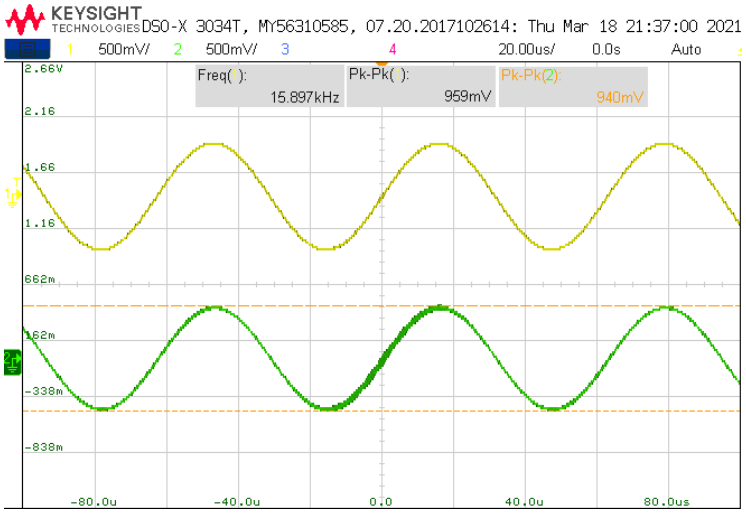


Figure 4.20: Simulated and Experimental frequency responses of proposed filters

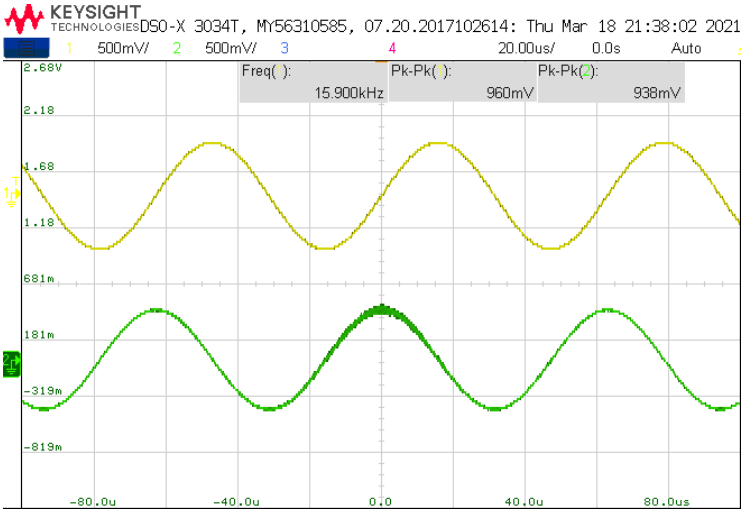
The time response of these filters have also been depicted in Fig.4.21 where input voltages of $1V_{pp}$ at 15.9 kHz were applied.



(a)



(b)



(c)

Figure 4.21: (a) Transient input and output voltages of (a) HPF (b) BPF (c) LPF

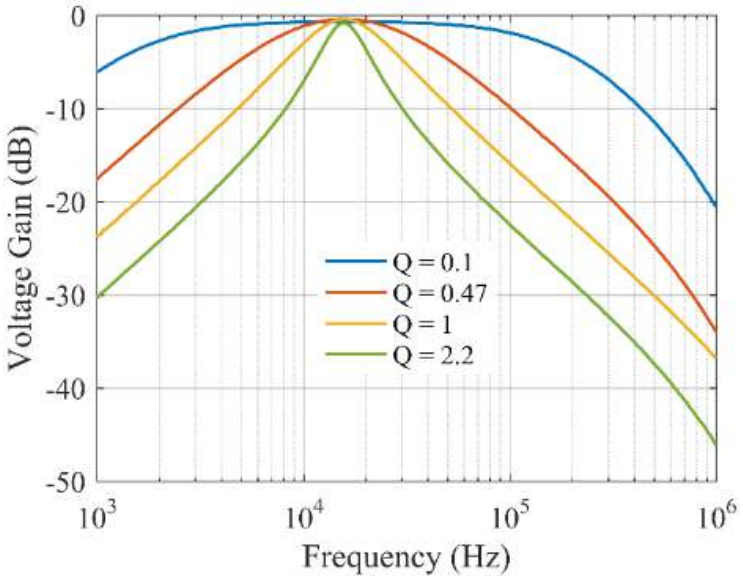
Tunability of Q_0:

We have also demonstrated the tunability of Q_0 without changing the value of ω_0, and the gain by varying R_4 and R_5 simultaneously. We have taken $R_4 = R_5 = 1\text{k}\Omega$, 4.7k$\Omega$, 10k$\Omega$ and 22kΩ for $Q_0 = 0.1$, 0.47, 1 and 2.2 respectively. For these values $\omega_0 = 15.9$ kHz and gain = 1. The respective graphs have been shown in Fig. 4.22a.

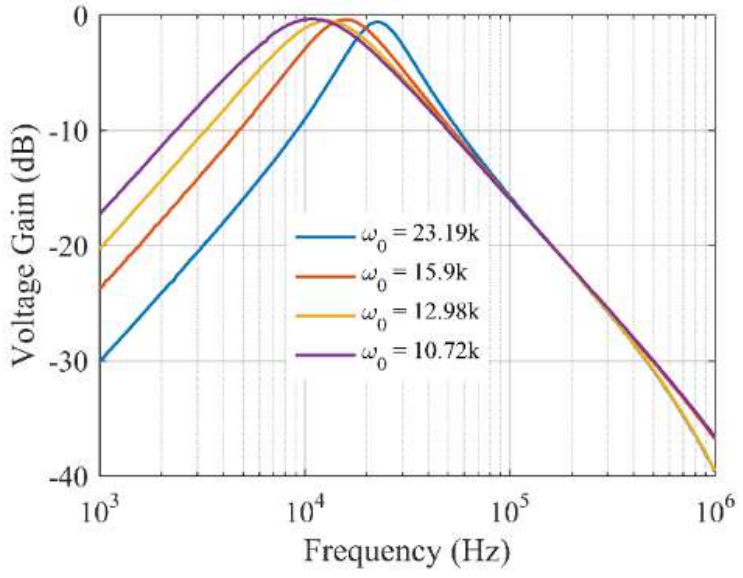
Tunability of ω_0:

From the expression of the pole frequency, it may be noted that the pole frequency

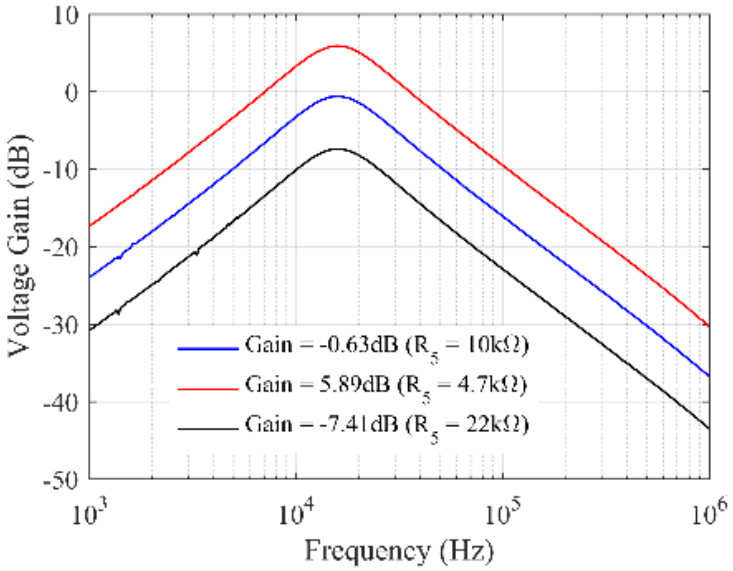
can be varied without changing the values of the BW and the gain by varying the value of R_6. In Fig. 4.22b, we have presented the variation of ω_0 for a given value of BW and gain by varying R_6 (4.7kΩ, 10kΩ, 15kΩ and 22kΩ) for value of pole frequency as 23.19 kHz, 15.9 kHz, 12.98 kHz, and 10.72 kHz respectively. In Fig. 4.22c we have depicted the variation of gain for a given value of pole frequency and bandwidth.



(a)



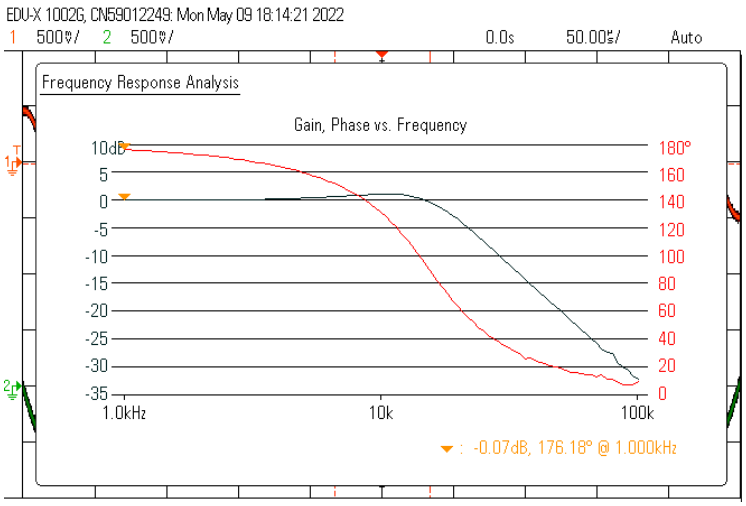
(b)



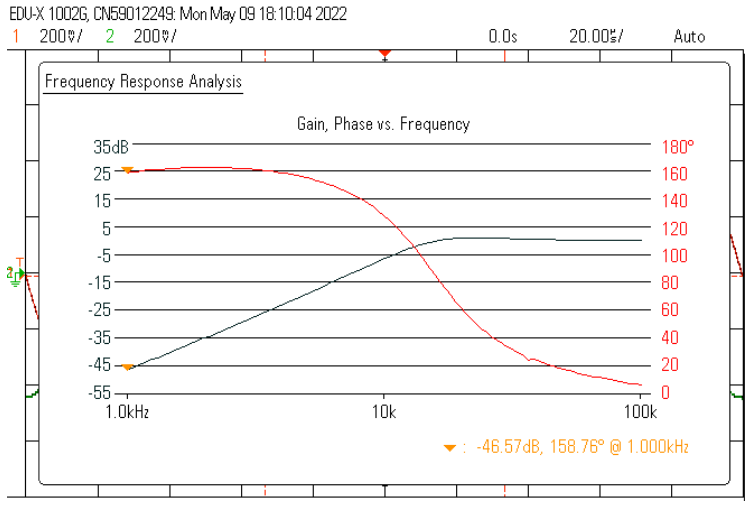
(c)

Figure 4.22: (a) Tunability of Q with ω_0 (b) Tunability of ω_0 (c) Tunability of Gain

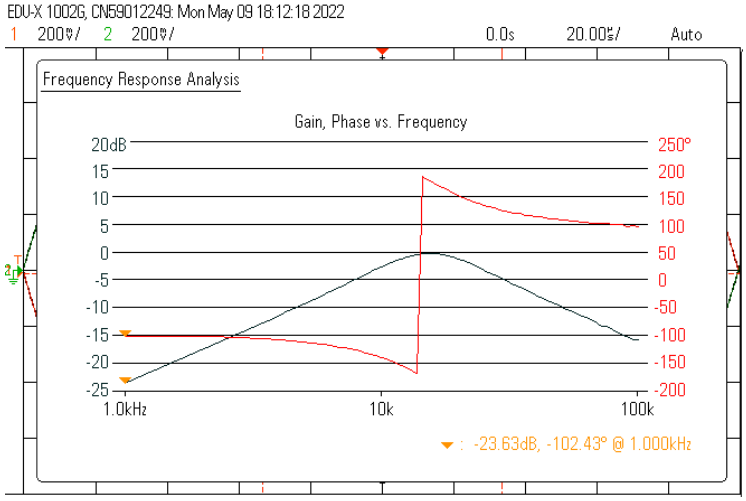
Similarly, the frequency and time domain responses of the proposed filter shown in Fig. 4.18b have been demonstrated in Fig. 4.23 and Fig. 4.24 respectively.



(a)

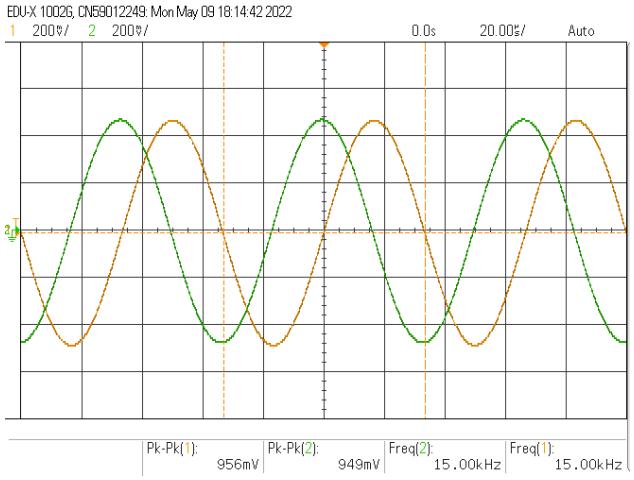


(b)

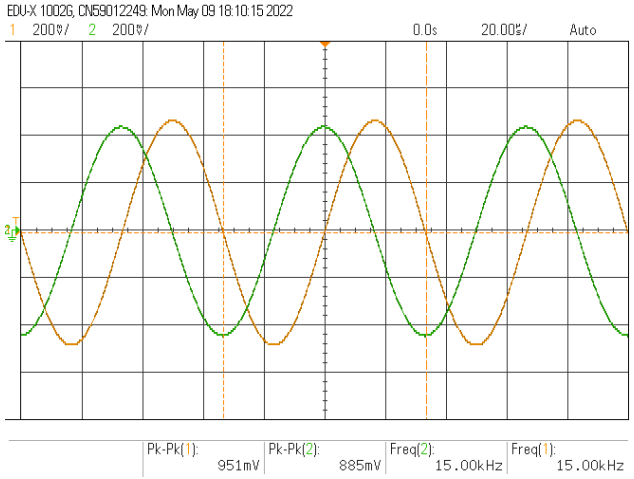


(c)

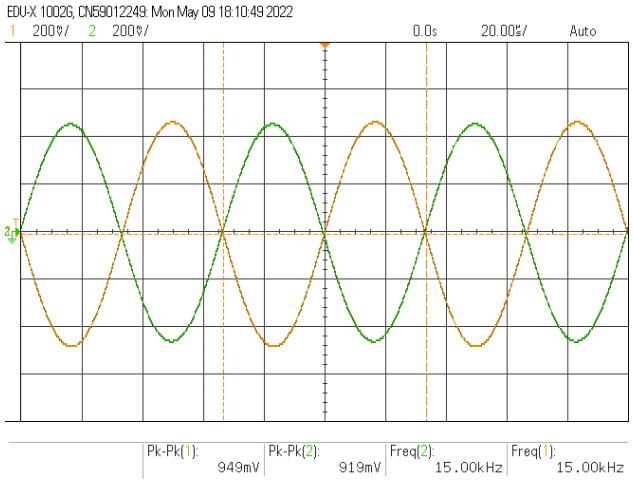
Figure 4.23: Frequency responses of the proposed filter shown in Fig. 4.18b (a) LPF (b) HPF (c) BPF



(a)



(b)

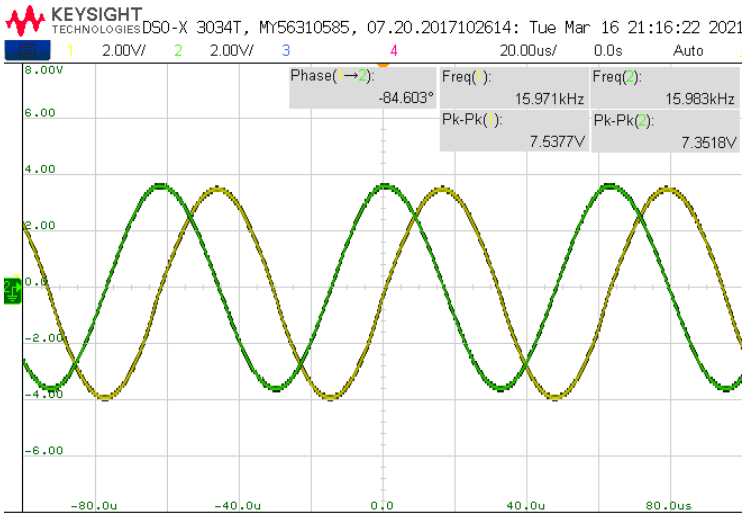


(c)

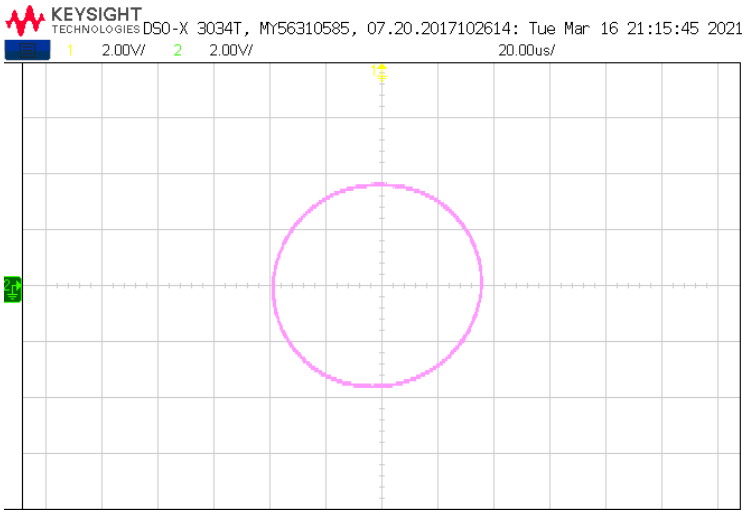
Figure 4.24: Time domain responses of the proposed filter shown in Fig. 4.18b (a) LPF (b) HPF (c) BPF

4.3.2 Quadrature Sinusoidal Oscillator

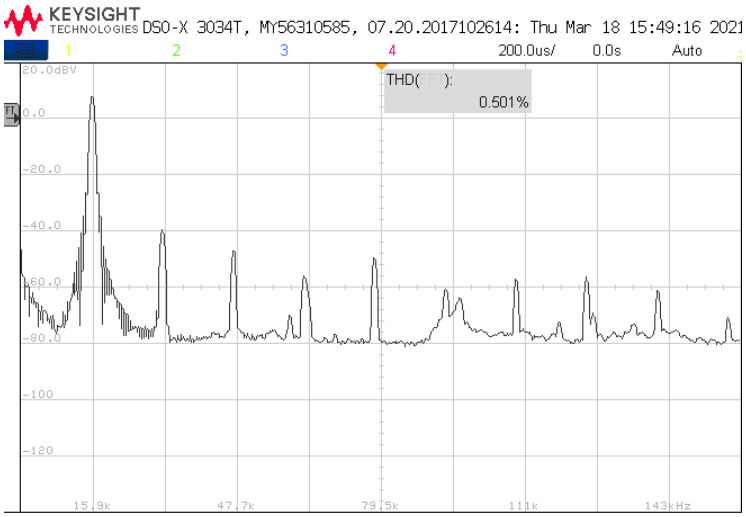
The quadrature sinusoidal oscillator circuits presented in Fig. 4.18a was breadboarded with the same values of passive components which were used for filter design. Two quadrature output voltage responses (V_{01}, V_{02}) and (V_{02} and V_{03}), Lissajous patterns and frequency spectrums have been displayed in Fig. 4.25 and Fig. 4.26 respectively.



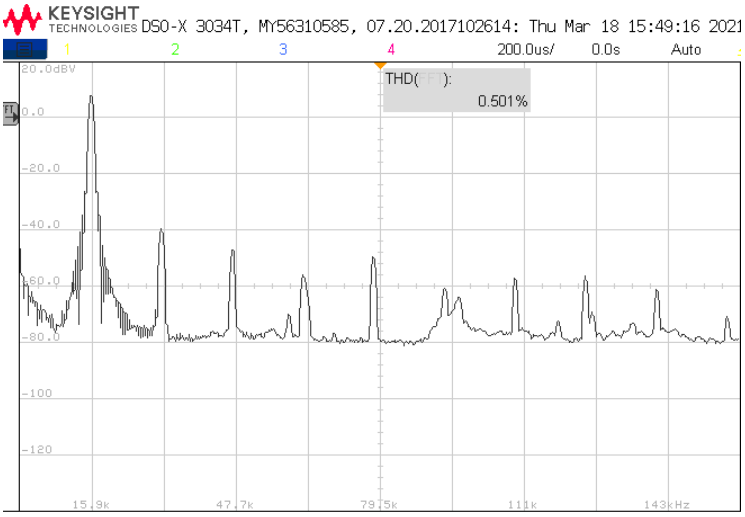
(a)



(b)

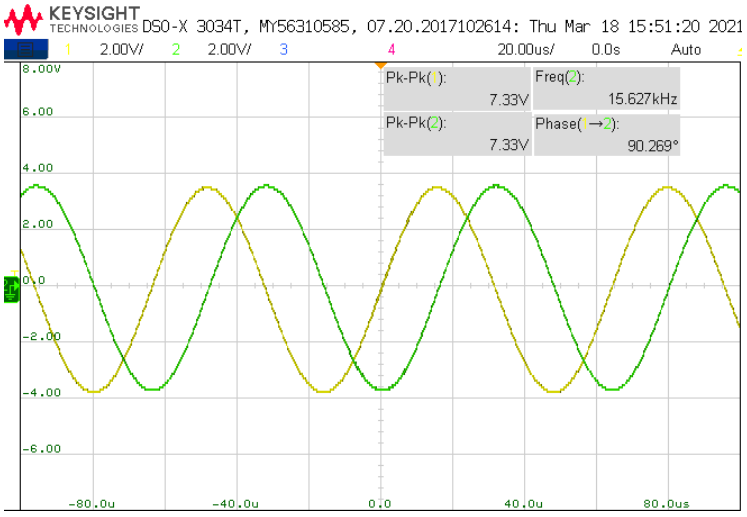


(c)

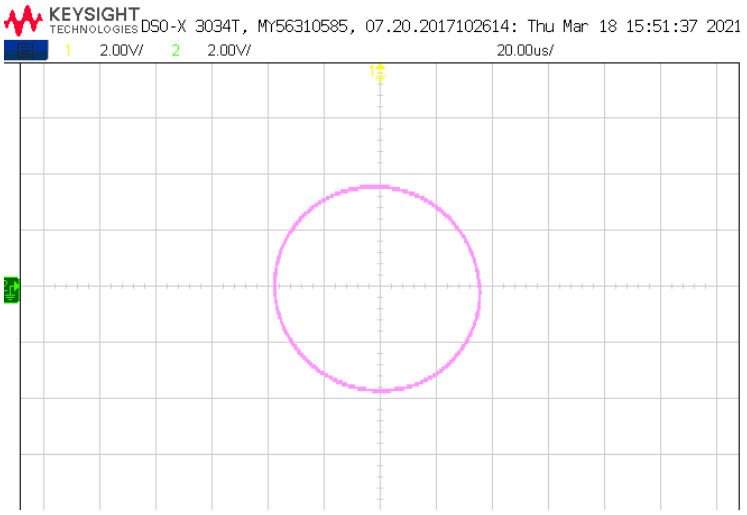


(d)

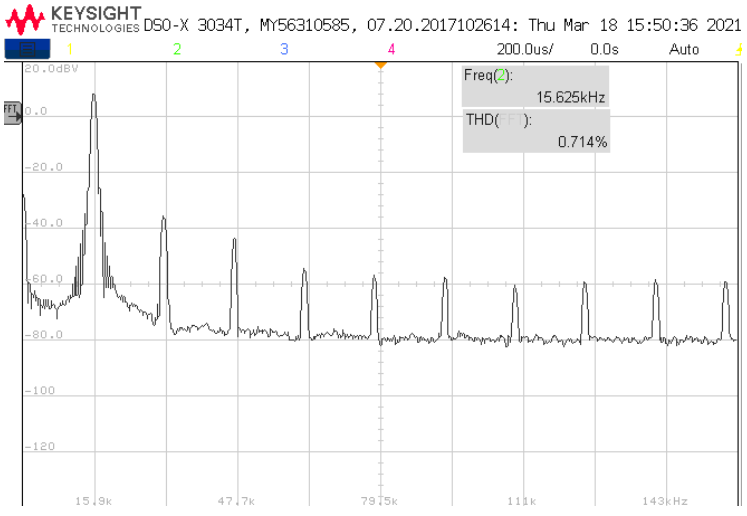
Figure 4.25: (a) Experimental transient responses between quadrature voltage V_{01} and V_{02} (b) Lissajous pattern (c) frequency spectrum of voltage V_{01} (d) Frequency spectrum of voltage V_{02}


KEYSIGHT TECHNOLOGIES DSO-X 3034T, MY56310585, 07.20.2017102614: Thu Mar 18 15:51:20 2021
1 2.00V/ 2 2.00V/ 3 4 20.00us/ 0.0s Auto
Pk-Pk(1): 7.33V
Freq(2): 15.627kHz
Pk-Pk(2): 7.33V
Phase(1→2): 90.269°
8.00V
6.00
4.00
2.00
0.0
-2.00
-4.00
-6.00
-80.0u
-40.0u
0.0
40.0u
80.0us

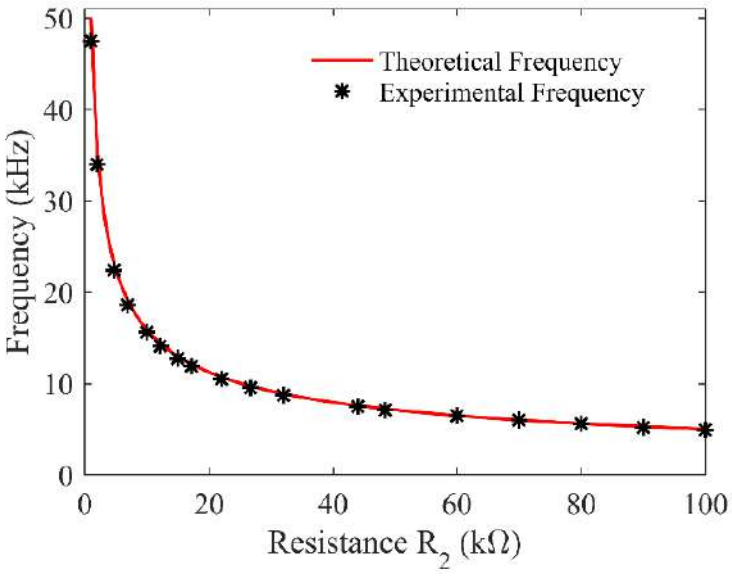
(a)


KEYSIGHT TECHNOLOGIES DSO-X 3034T, MY56310585, 07.20.2017102614: Thu Mar 18 15:51:37 2021
1 2.00V/ 2 2.00V/ 20.00us/

(b)


KEYSIGHT TECHNOLOGIES DSO-X 3034T, MY56310585, 07.20.2017102614: Thu Mar 18 15:50:36 2021
1 2 3 4 200.0us/ 0.0s Auto
Freq(2): 15.625kHz
THD(FFT): 0.714%
20.0dBV
0.0
-20.0
-40.0
-60.0
-80.0
-100
-120
15.9k
47.7k
79.5k
111k
143kHz

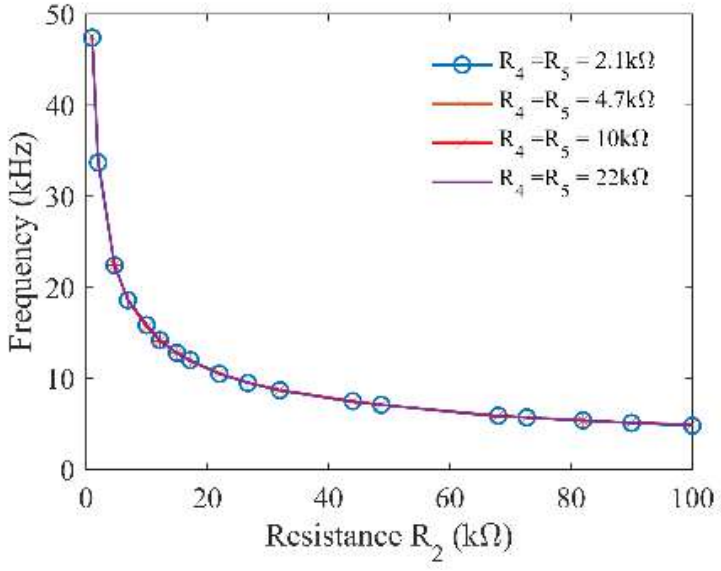
(c)



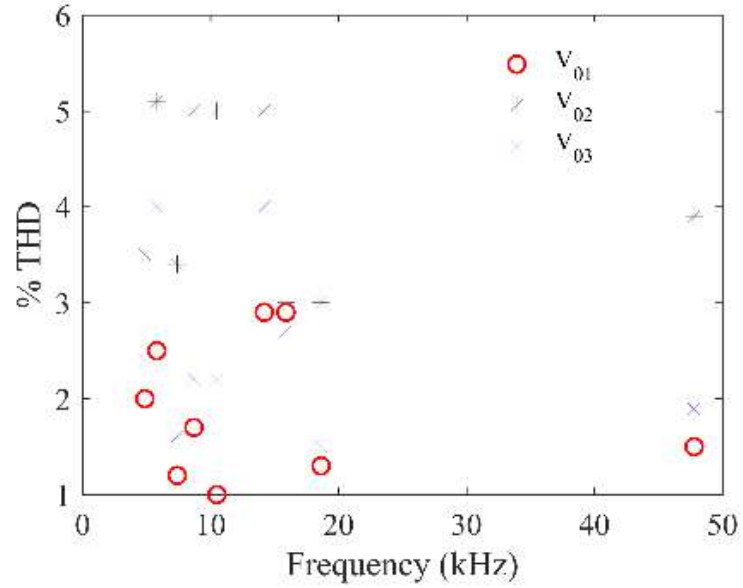
(d)

Figure 4.26: (a) Experimental transient responses between quadrature voltage V_{02} and V_{03} (b) Lissajous pattern (c) frequency spectrum of voltage V_{03} (d) Variation in frequency with resistor R_2

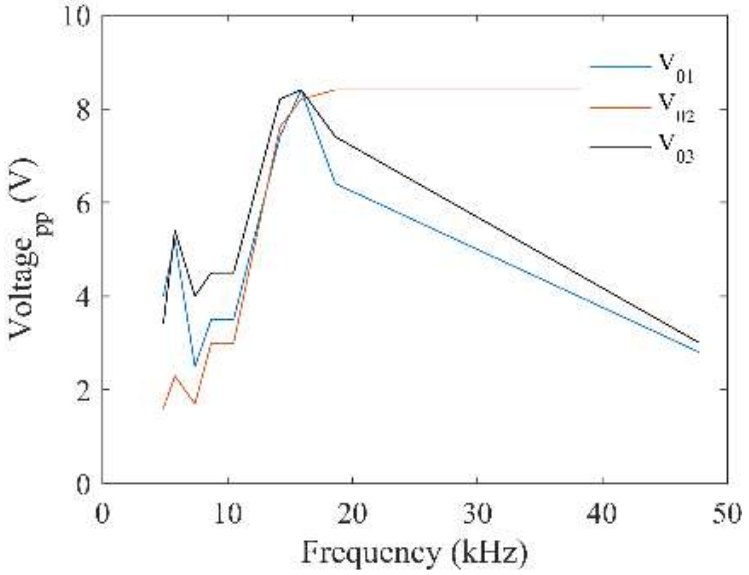
The effect of varying resistor R_2 on frequency is shown in Fig. 4.26d. Fig. 4.27a shows that for different values of R_4 and R_5 the variation in frequency with resistor R_2 remains the same, thus, confirming the decoupled nature of tuning of FO and CO. Variation of %THD and peak to peak voltage outputs V_{01}, V_{02} and V_{03} with frequency has been shown in Fig. 4.27b and Fig. 4.27c respectively.



(a)



(b)



(c)

Figure 4.27: (a) CO decoupled tuning of FO (b)Variation in THD with frequency (c)Variation in peak to peak voltage with frequency

The simulation and experimental results thus, validate the functionality of the bi-quadratic filter configurations presented in this chapter.

4.4 Concluding Remarks

In continuation of the preceeding chapters, in this chapter we have presented biquadratic filter configurations. The first proposed filter circuit employs a single OTRA and four admittances and proper selection(s) of each admittance yields three different filter responses namely low pass filter, high pass filter and band pass filter. The topology of the filter is based on single-input single output type. The filter parameters namely, cut-off frequency, pole quality factor/bandwidth and gain of each filter is orthogonally controllable. Non-ideal analysis using a single pole model of OTRA has been described and non-ideal expressions of transfer functions, cut-off frequency, quality factor and gain have been mathematically evaluated. The functionality of the proposed filter functions has been validated using CMOS OTRA implemented with 0.18 μm TSMC technology parameters.The numerous simulation results alongwith MATLAB evaluations, thus, verify the validity of the proposed filters.

Two different configurations of biquad filters have been presented using three OTRAs, seven resistors and two virtually grounded capacitors. The single-input multiple-output topology has been employed for both the structures to realize various filter functions namely LPF, HPF and BPF. The quality factor of the proposed filters can be independently controlled without changing the cut-off frequency. On the other hand, bandwidth can also be tuned independently for a constant cut-off frequency. The gain of each filter can be varied independently. Sensitivity and non-ideal analyses have also been carried out. The proposed filter circuits may further be converted into second order quadrature sinusoidal oscillators with simple artifices. Frequency stability factors of the derived oscillators has also been studied. The workability of both the filters as well as of oscillator circuits have been verified using simulation and experimental results. For simulation and experimental results, an OTRA was implemented with commercially available analog ICs AD844.

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Chapter 5

Third Order Sinusoidal Oscillators Using OTRAs

5.1 Introduction

In the previous chapter we proposed biquad filters employing OTRAs. The present chapter deals with the realization of OTRA-based third order sinusoidal oscillators.

Harmonic oscillators belong to a class of autonomous, closed loop, analog circuits in which the output signal is a sinusoidal signal whose frequency and amplitude can be set by the designer. Since these circuits are autonomous, no input signal at signal frequency is applied to the circuits. For low and medium frequency applications, these oscillators are usually realized with an amplifier, which is built with one or more ABBs, resistors and capacitors. These harmonic oscillators may be classified in several ways viz.,

(i) Voltage mode and current mode: Depending on the type of signal available at the output, the oscillators can be categorised as voltage mode, or current mode.

(ii) Single phase, multiphase/quadrature: Oscillators can be classified as single

phase or multiphase depending upon the phase difference between different output voltages/currents. If different output voltages/currents exhibit a quadrature relation, then the oscillator is known as quadrature oscillator.

(iii) Second order, third order or higher order oscillators: The order of the oscillator depends on the order 'n' of the characteristic equation. If the characteristic equation is of order '2', then the oscillator is called as second order oscillator. Usually, the canonic realization of such RC oscillators employ two capacitors. However, it has been reported in literarture, that higher order oscillators (where the number of capacitors employed is '3' or more) have better accuracy, low harmonic distortion and high quality factor.

(iv) Fixed frequency oscillators (FFO), single resistance controlled oscillators (SRCO) and single capacitor controlled oscillators (SCCO): In an RC oscillator, if the frequency of oscillation (FO) cannot be changed without changing the condition of oscillation (CO), then such oscillator is known as FFO. On the other hand, if the FO can be changed without changing the CO, by varying either a resistor or a capacitor, then the oscillator is called as SRCO/SCCO. If in an oscillator, the FO and CO can be controlled by different set(s) of passive elements, then such type of oscillators are preferred from the point of view of amplitude stabilization and control.

(v) Voltage/current controlled oscillators (VCOs/CCOs): If the FO in harmonic oscillators can be tuned by varying some external voltage/current, then, such oscillators are also known as voltage/current controlled oscillators. These oscillator circuits (VCOs/CCOs) are very useful for frequency modulation or phase modulation by applying a modulating signal to the control input.

From a detailed perusal of the research work carried out on harmonic oscillators

available in an open literature, it has been observed that compared to second order oscillators with different properties, relatively less work has been done on the realization of third order oscillators [1–40].

Since this chapter deals with the realization of third order sinusoidal oscillators(TOSOs), in the following, we present a detailed account of the work reported earlier on the realization of TOSOs using different active building blocks, so that the work presented in this chapter can be put in proper perspective.

In [1], two different configurations of third order quadrature sinusoidal oscillators(TOQSOs) using three operational amplifiers (op-amp) have been presented by **Horng**. The first circuit employs five resistors and three capacitors whereas the second circuit requires five capacitors and three resistors. The CO and FO of both the circuits are orthogonally controllable. The reported circuits were experimentally tested using off-the-shelf available IC LM351 type op-amps.

In [2], **Prommee** and **Dehjan** reported two TOQSO structures which are based on two different topologies. The first topology is based upon a cascade connection of two lossy integrators and a lossless integrator with a unity feedback while in another topology, three lossy integrators with a unity feedback have been used. The first TOQSO configuration has employed three OTAs and three capacitors, while the other configuration used four OTAs, three capacitors and an electronic resistor. Both the derived TOQSO circuits have electronic control of CO and FO but do not possess independent control of CO and FO. One of the reported circuits is displayed in Fig. 5.1.

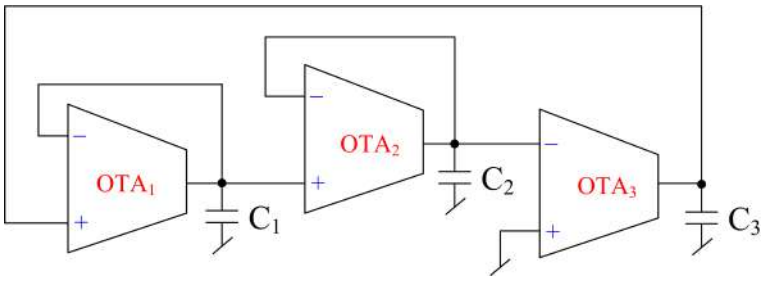


Figure 5.1: TOQSO using OTAs reported by Prommee and Dehjan [2].

Three OTAs and three grounded capacitors based TOQSO has been reported in [3] by **Komal, Pushkar** and **Kumar**. The scheme used in this circuit is a cascade connection of second order LPF and an inverting lossless integrator with a unity feedback loop. This oscillator circuit provides independent electronic control of CO and FO both through seprate transconductors.

Two different structures of TOQSOs have been presented in [4] by **Raj, Bhaskar** and **Kumar** which are based on the combination of second order low pass filter and a lossless integrator. For the implementation of reported approach, four OTAs and three grounded capacitors have been employed. The CO and FO of both the structures possess fully independent electronic control and also one of the TOQSOs also provides voltage and current quadrature outputs. The workability of these oscillator circuits has been verified in PSPICE using CMOS OTAs. The operation of these TOQSOs has also been verified experimentally using LM13700 type OTAs.

Four TOQSOs have been presented in [5] by **Bhaskar, Raj** and **Kumar** whose circuit configurations have been shown in Fig. 5.2. All the four circuits employ three OTAs and three capacitors out of which, two of the capacitors are grounded while the third capacitor is floating. The reported TOQSOs provide independent electronic control of CO and FO and also possess voltage as well as current quadrature outputs. The workability of all the four TOQSOs has been verified in PSPICE using CMOS OTA and also tested experimentally using LM13700 type OTAs.

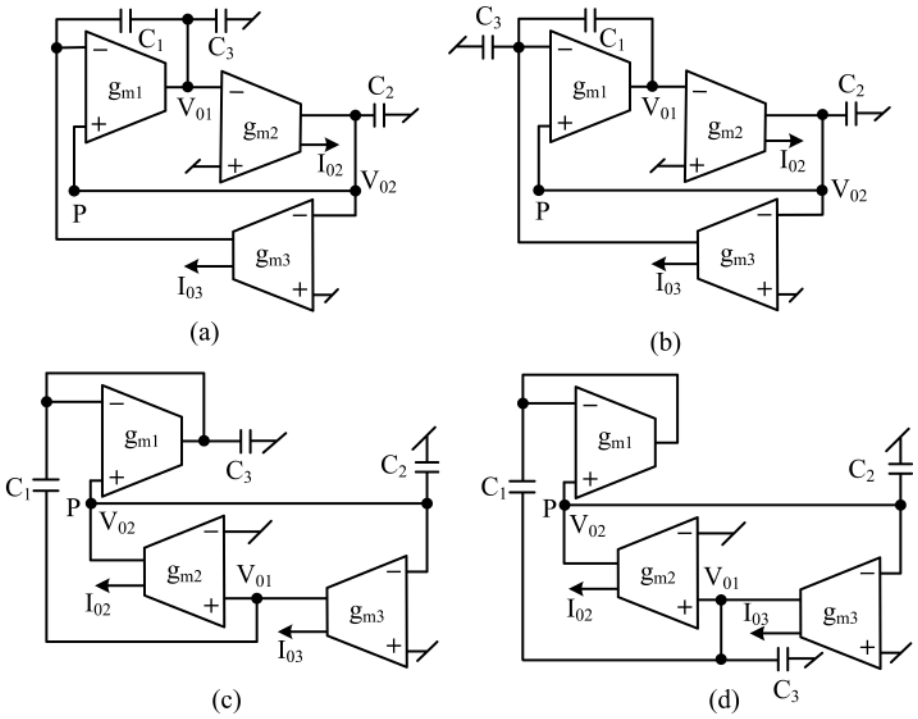


Figure 5.2: OTA-based TOQSOs reported by Bhaskar, Raj and Kumar [5].

Joshi, Kirti and **Thakur** [6] presented a third order sinusoidal oscillator employing four CFOAs and two OTAs. This circuit requires five passive elements and provides both voltage and current outputs. Although the circuit does not provide independent control of CO and FO but has electronic tuning of both CO and FO.

Soliman [7] described a systematic synthesis procedure for realizing TOQSOs, employing grounded components only, which is based on nodal admittance matrix (NAM) expansion. Based on the presented approach, four new circuits employing current conveyors (CCII) and also four different circuits using inverting current conveyors (ICCII) have been reported. However, these reported circuits do not offer independent control of CO and FO.

In [8], **Raj, Kumar** and **Bhaskar** presented short circuit admittance based twelve matrices, which are capable of realizing third order sinusoidal oscillators. Four distinct low frequency third order sinusoidal oscillator with minimum active

and passive components have been reported whose circuit realizations have been displayed in Fig. 5.3. All the four oscillator circuits employ three CFOAs, four resistors and three grounded capacitors. These oscillators provide independent control of both CO and FO. Two of the presented circuits have quadrature outputs also.

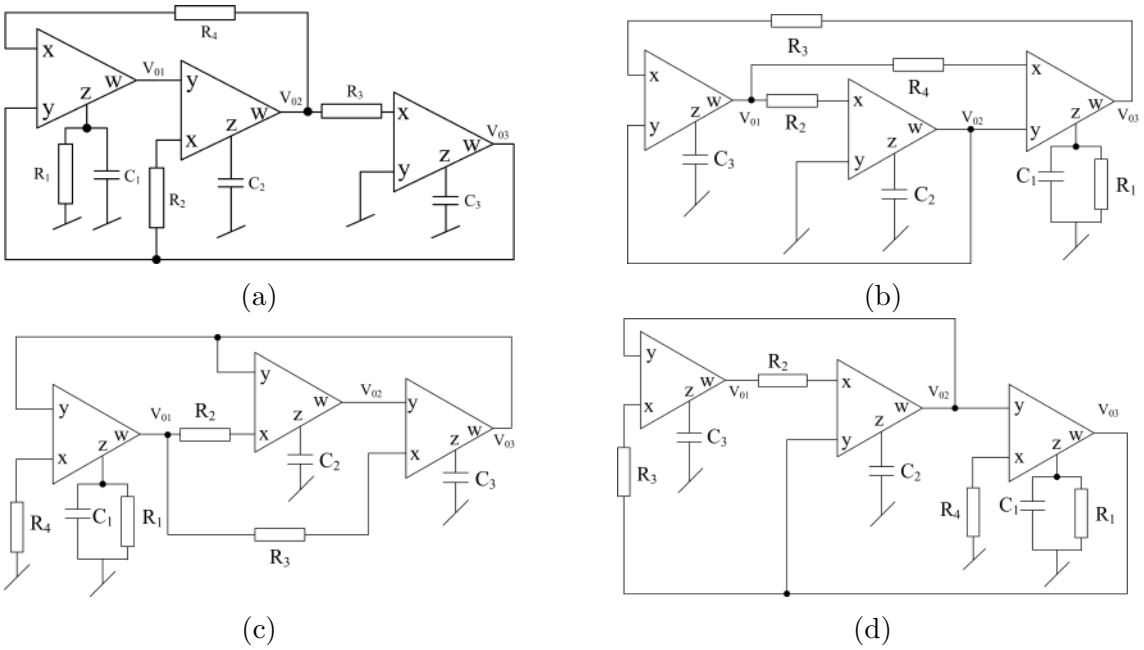


Figure 5.3: Four different configurations of TOQSOs employing CFOAs [8]

Three TOQSO configurations using three CCIIs have been reported in [9] by **Horng, Hou, Chang, Chung, Tang** and **Wen**. All the three structures of TOQSOs employ two CCIIs+ and one CCII-. Two of these reported circuits require five resistors and three grounded capacitors while the third circuit requires, three resistors and five capacitors. The CO and FO of the reported circuits do offer independent control. Two of the circuits have the novel feature of having all the five/three resistors being grounded. This is an attractive feature for IC implementation as well as converting the circuits into voltage-controlled circuits by replacing the grounded resistors by FET/MOSFET-based linear voltage-controlled resistances.

In [10], **Raj, Bhaskar** and **Kumar** presented two new configurations of TOQ-

SOs that employ four CFOAs, four/five resistors and three grounded capacitors. Out of these two configurations, the first TOQSO offers independent control of CO and FO while the second TOQSO enjoys fully decoupled control of CO and FO. Both the presented circuits generate low frequency oscillations which are beneficial from the view point of biomedial applications.

A CCII and universal voltage conveyor based TOQSO was presented by **Koton, Herencsar, Vrba** and **Metin** in [11]. The reported circuit uses all grounded passive components (three capacitors and three resistors) and also provides independent control CO and FO. This circuit has four different output voltages available at high output impedance nodes.

An electronically tunable TOQSO circuit employing four CCCIIs, three capacitors, and one resistor has been reported by **Maheshwari** and **Verma** in [12]. The scheme used for the realisation of presented TOQSO is based on a cascade connection of three current mode first order low-pass filters with gain in feedback. The CO and FO of the presented oscillator can be controlled electronically through the bias currents.

In [13], a topology of third-order sinusoidal oscillator consisting of a voltage mode second order low pass filter in feedback with inverting integrator was reported by **Maheshwari** and **Khan**. The presented structure was used to implement a TOQSO circuit employing four current controlled second-generation current conveyors (CCCII) and three capacitors. The reported circuit provides non-interacting control of FO and CO.

Maheshwari [14], presented a current mode(CM)/voltage mode(VM) TOQSO employing three CCCIIs and three capacitors. The scheme of the reported circuit is based on a cascade connection of an inverting lossy integrator and two lossless integrators with a unity feedback. This circuit offers non-interacting control of CO and

FO and also provides voltage as well as current quadrature outputs. This circuit is reproduced here in Fig. 5.4.

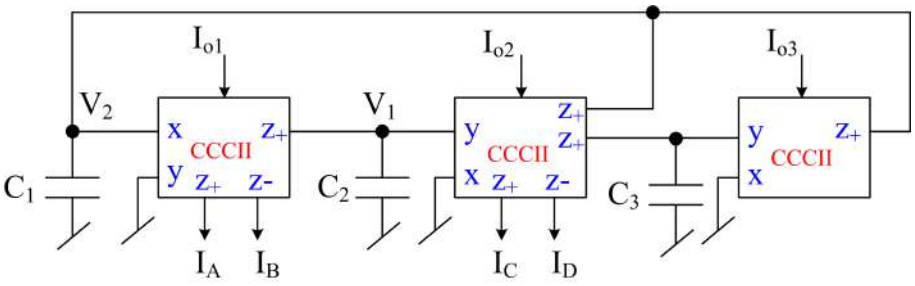


Figure 5.4: Third-order sinusoidal oscillators using CCCIIs presented by Maheshwari [14].

Chaturvedi and **Maheshwari** [15] reported a TOQSO employing three DVCCs, three resistors and three grounded capacitors. The presented circuit provides voltage and current quadrature outputs. However, the CO and FO of the presented circuit can not be adjusted independently.

In [16], **Maheshwari** presented a differential voltage current conveyors (DVCCs) based TOQSO that employs three DVCCs with all grounded passive components (three grounded resistors and three grounded capacitors). The functional block diagram of the TOQSO is based on second order low pass filter and one inverting integrator in a feedback loop. The presented circuit enjoys independent control of both CO and FO and also provides VM and CM quadrature outputs.

In [17], two multiple-output second generation current conveyors (MO-CCII), three grounded capacitors and three resistors based TOQSO was reported by **Horng**. The presented configuration has independent control of CO and FO which can be adjusted through resistors. The presented circuit provides quadrature outputs in voltage mode as well as in current mode also.

Wareechol, Knobnob and **Kumngern** [18] reported a single fully differential second generation current conveyor (FDCCII) based TOQSO circuit using three

resistors and three grounded capacitors. This circuit offers independent tunability feature of CO and FO. Both voltage as well as current quadrature outputs are also available in the presented circuit.

In [19], **Roy** and **Pal** reported two new configurations of TOQSOs employing two VDCCs, three grounded resistors and three grounded capacitors. The CO and FO of the reported oscillators have independent electronic control with voltage and current quadrature outputs. These two circuits have been tested in PSPICE with VDCC implemented in CMOS technology and also verified using off-the-shelf available IC AD844 type CFOAs.

In [20], a current-mode TOQSO using one differential difference current conveyor (DDCC), a voltage differencing transconductance amplifier (VDTA), three capacitors and one resistor has been presented by **Phanruttanachai** and **Jaikla**. The scheme of the reported TOQSO is based on a cascade connection of second order inverting low pass filter in a feedback with non-inverting lossless integrator. The CO and FO of this circuit can be controlled independently.

An inverting second order low pass filter in a feedback with a non-inverting integrator based voltage mode TOQSO has been presented by **Kwawsibsam, Sreewirote** and **Jaikla** in [21]. For the implementation of TOQSO, one DDCC, two OTAs, one resistor and three grounded capacitors have been used. The CO and FO of the oscillator can be adjusted electronically and independently.

A current mode TOQSO employing three CDTAs and three capacitors was presented by Horng in [22] which is shown in Fig. 5.5. Although the presented circuit has independent control of CO but does not provide non-interacting control of FO. One of the input terminals of the CDTA is left open which is not beneficial from the view point of IC implementation.

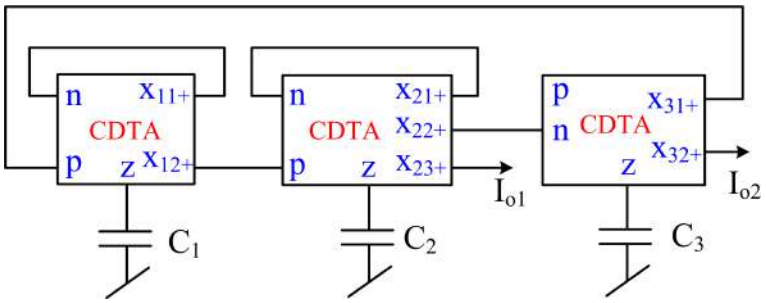


Figure 5.5: Current mode TOQSO using CDTAs reported by Horng [22]

Two TOQSOs with four explicit current outputs have been presented by **Jin, Wang** and **Sun** in [23]. The first circuit employs two CDTAs and three grounded capacitors while in the second circuit, three CDTAs and three capacitors have been employed. The presented TOQSOs have independent electronic control of CO and FO. Layout and experimental results have been provided for the validation of the theoretical propositions.

Single current differencing cascaded transconductance amplifier (CDCTA) and three capacitors based TOQSO has been reported by **Kumngern** and **Torteanchai** in [24]. The CO and FO of this oscillator can be controlled electronically and independently through bias currents. The presented circuit provides three voltage outputs and four current outputs and can also be used for amplitude modulation.

Lawanwisut and **Siripruchyanun** presented a TOQSO[25] employing two current-controlled current conveyor transconductance amplifiers (CCCCTAs) and three capacitors. The basic functional block diagram used for the realization of presented TOSQO is a cascade of an inverting second order low pass filter and a non-inverting integrator. The CO and FO of the presented oscillator circuit have independent electronic control feature .

A single modified current-controlled current conveyor transconductance amplifier (MCCCCTA) and three capacitors based TOQSO was reported by **Kumngern**

and **Chanwutitum** in [26] which is shown in Fig. 5.6. This presented circuit can generate two quadrature voltage outputs and four quadrature current outputs. The CO and FO the reported TOQSO can be controlled electronically and independently through bias currents.

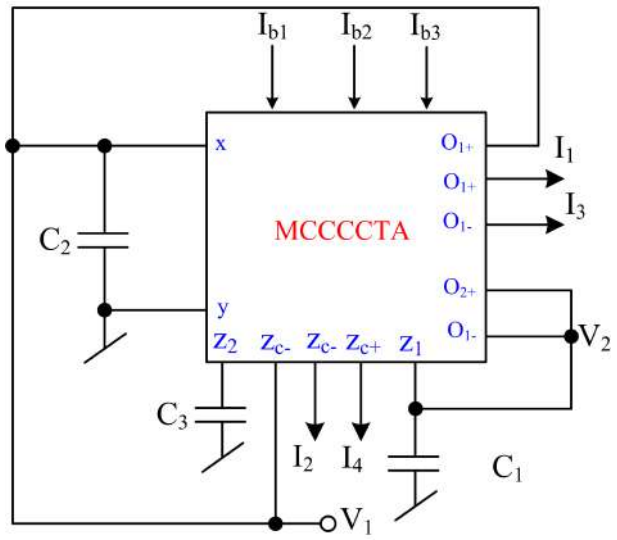


Figure 5.6: Third-order quadrature sinusoidal oscillator using MCCCCTA presented by Kumngern and Chanwutitum [26].

Chen, Hwang and **Ku**[27], presented a resistorless third-order quadrature oscillator configuration whose realization is based on combination of an inverting lossy integrator and two lossless integrators. This circuit uses two multiple-output current controlled current conveyor transconductance amplifiers (MO-CCCCTAs) and three grounded capacitors. The CO and FO of he reported TOQSO can be controlled independently with electronic control feature. This circuit is also suitable for generation of amplitude modulation (AM) and amplitude shift keying (ASK) signals.

In [28], **Pandey** and **Pandey** reported a new approach for the realization of TOQSO which employs a second order high pass filter and a differentiator in the feedback. Based on this approach, two different TOQSOs using two differential

voltage current conveyor transconductance amplifiers (DVCCTAs), three capacitors and one resistor have been reported. The CO and FO of both the TOQSOs can be controlled independently. One of the reported circuits has been depicted in Fig. 5.7.

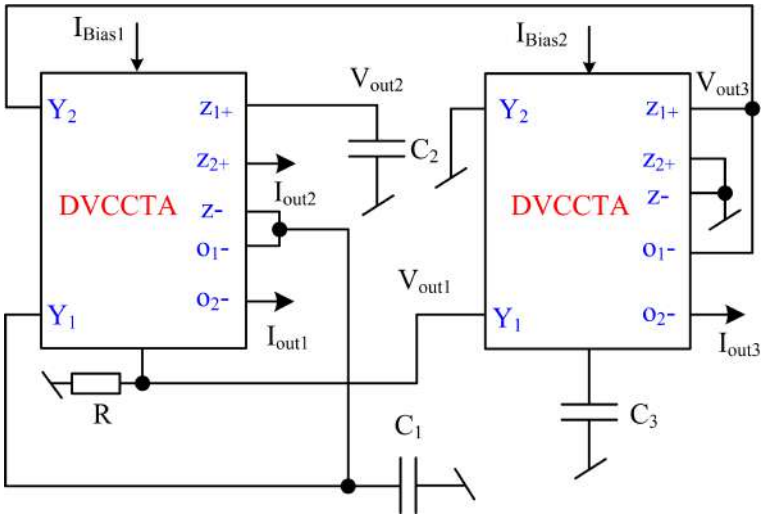


Figure 5.7: Third-order quadrature sinusoidal oscillator using DVCCTAs presented by Pandey and Pandey [28].

A voltage mode second order low pass filter and a VM non-inverting integrator in a feedback loop has been used to implement a TOQSO by **Chen, Hwang** and **Ku** [29]. The reported TOQSO circuit employs, two multiple-output DVCCTAs, three capacitors and two resistors. The circuit provides both VM and CM quadrature outputs with independent control of CO and FO and also generate AM and ASK signals.

In [30], **Khaw-Ngam, Kumngern** and **Khateb** presented a mixed-mode TOQSO circuit employing a modified current-controlled current follower transconductance amplifier (MCCFTA) and three grounded capacitors. The presented circuit has voltage as well as explicit current quadrature outputs and also provides the orthogonal tunability of CO and FO.

In [31], an approach for the realization of TOQSO comprising a second order low pass filter in a feedback with an inverting integrator was presented by **Chen, Hwang**

and **Ku**. This TOQSO employs two VDTAs, and three grounded capacitors. This circuit offers independent control of FO and CO and is also suitable for generation of AM/ASK signals. The presented circuit provides both voltage and current quadrature outputs.

Another VDTA-based TOQSO structure has been reported by **Chen, Wang, Chen** and **Huang** [32] employing two multi-output VDTAs and three grounded capacitors. The reported circuit has electronic independent control of CO and FO and also provides quadrature output voltage and output current. This reported circuit can also provide AM/ASK signals which may find applications in communication systems.

In [33], **Malhotra, Ahalawat, Kumar, Pandey** and **Pandey** presented a TOQSO which is based on a combination of two lossy integrators followed by a lossless integrator in a closed loop. This circuit employs three voltage differencing buffered amplifiers (VDBAs), three grounded capacitors and two grounded resistors. Although this circuit has low output impedance which is suitable for easy cascadibility in VM but it does not offer independent control of CO and FO.

Another VDBA based TOQSO has been reported in [34] by **Pushkar**. The presented TOQSO circuit is based on a cascade connection of non-inverting LPF and an inverting integrator with a unity feedback loop. The circuit employs two VDBAs, three capacitors, and one resistor. Out of the three capacitors, two are grounded while the third capacitor is floating. The CO and FO of the reported circuit can be controlled independently through different transconductances and also the circuit offers quadrature voltage outputs.

In [35], two voltage differencing inverting buffered amplifiers (VDIBAs), three grounded capacitors and a resistor based TOQSO has been presented by **Pushkar** and **Bhaskar**.

The reported circuit used an approach which consists a non-inverting LPF and an inverting integrator with a unity feedback loop. The reported TOQSO also enjoys independent electronic control of CO and FO with quadrature output voltages.

In [36], a single modified current controlled current follower transconductance amplifier based four phase current mode TOQSO has been presented by **Kumngern** and **Torteanchai**. The reported circuit offers independent electronic control of CO and FO.

A TOQSO has been presented by **Channumsin** and **Jantakun** [37] using two VDTA and three grounded capacitors . The reported circuit has both voltage and current outputs and also has independent control of CO and FO. The presented TOQSO can also be used easily in the generation of amplitude modulation (AM)/ amplitude shift keying (ASK) communication signals.

Phatsornsiri, Lamun, Kumngern and **Torteanchai** [38] presented a TOQSO employing two VDTA and three grounded capacitors. The reported circuit offers independent electronic control of CO and FO with current quadrature outputs. This circuit does not exploit the full capability of VDTA as one of the input terminals of VDTA is grounded.

In [39], another CDTA based electronically tunable TOQSO circuit was presented by **Horng, Lee** and **Wu**. The presented circuit uses three CDTAs and three capacitors. This circuit offers non-interacting control of CO and FO. Both voltage as well as current mode quadrature outputs are available.

In [40], one current controlled current differencing transconductance amplifier (CC-CDTA), one OTA and three capacitors were employed to realize a TOQSO by **Kumngern** and **Junnapiya**. The presented oscillator offers independent adjustment of

CO and FO both.

5.2 Third Order Oscillators Employing OTRAs

Recently various configurations of third order sinusoidal oscillators employing OTRAs have also been reported in the open literature [41–48]. Since, this chapter deals with TOSOs employing OTRAs, therefore, a brief survey of these TOSOs [41–48] is now presented.

In [41], **Pandey, Pandey** and **Paul** presented a third order sinusoidal oscillator using two OTRAs, four resistors and three capacitors. The CO and FO of the reported circuit does not have independent control and also, matching condition is required to satisfy CO and FO. The intrinsic current differencing property of the OTRA has not been utilised as one of the input terminals of OTRA is grounded. Furthermore, in this reported circuit, passive resistors have been implemented with MOS resistors (preferred for IC implementation).

In [42], two different topologies of TOQSOs using three OTRAs, five resistors and three capacitors have been reported by **Pandey, Pandey, Komanapalli** and **Anurag** which is shown in Fig. 5.8. One of these circuits uses a cascade connection of inverting lossy integrator and two lossless integrators with a unity feedback whereas in second topology, a cascade connection of one lossless and two lossy integrators with a unity feedback has been employed. Out of these two configurations, one TOQSO has independent tunability of CO and FO, however, both the circuits have not utilized the intrinsic property of OTRA.

Three OTRAs, six resistors and three capacitors based TOQSO has been reported in [43] by **Komanapalli, Pandey** and **Pandey**. The presentd circuit does not

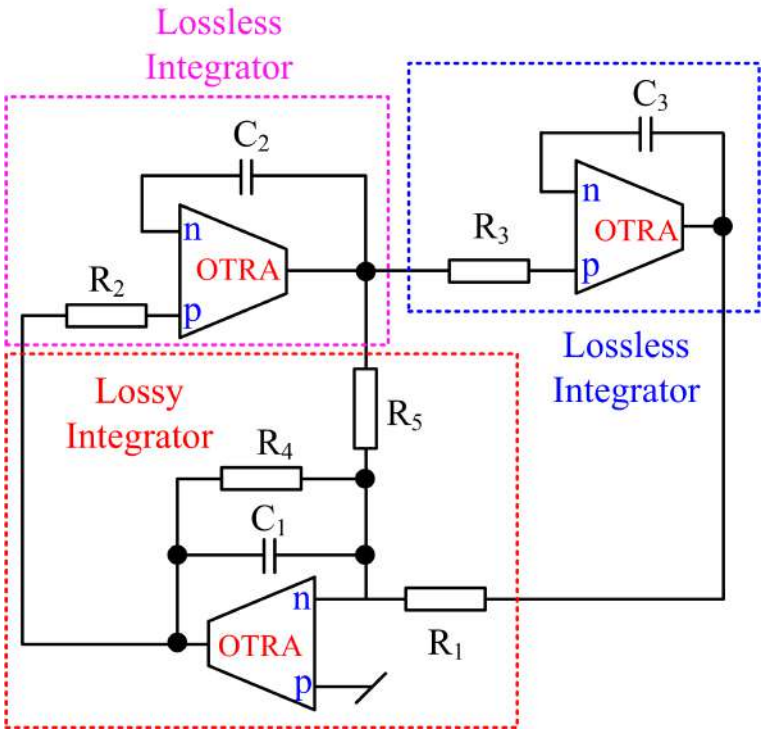


Figure 5.8: Third-order sinusoidal oscillators employing OTRAs [42]

provide independent control of CO and FO and also requires matching constraints of resistors. The intrinsic property of OTRA has also been not utilized.

Two different topologies of TOQSOs have been presented by **Nagar** and **Paul** in [44] wherein, the first structure employs an inverting amplifier and second-order low pass filter and the second structure consists an inverting differentiator and a second-order high pass filter (as shown in Fig. 5.9. The reported circuits employ two OTRAs , three resistors and three capacitors without utilizing the intrinsic property of OTRA. The CO and FO of the reported circuits cannot be controlled independently. For the viability of the presented TOQSOs, simulation and experimental results have been provided.

Kumngern and **Kansiri** presented a TOQSO [45], employing three OTRAs, six resistors and three capacitors. Although, the reported oscillator offers independent

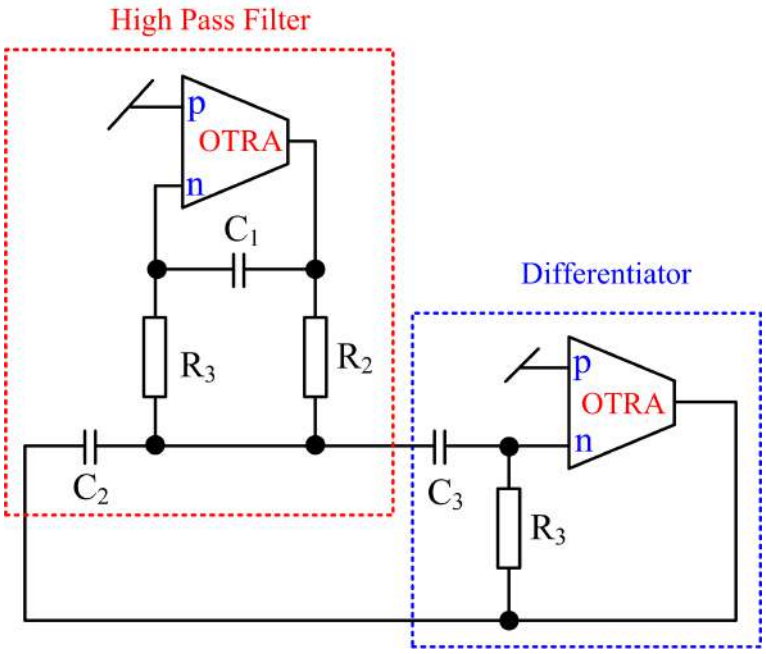


Figure 5.9: Second order high pass filter and differentiator approach based TOQSO using OTRAs [44]

control of CO and FO however, one of the input terminals of OTRA is left open which may cause noise injection in monolithic implementation.

Another configuration of TOQSO using two OTRAs, four resistors, and three capacitors has been presented by **Nagar** and **Paul** in [46]. The CO and FO of the reported configuration offers orthogonal controllability feature. Furthermore, the circuit has been implemented with MOS resistors by replacing passive resistors.

While most of the works described above require two to three OTRAs, in [47] and [48], the authors came up with a single OTRA based TOSOs. In [47], single OTRA, three resistors and three capacitors based TOSO has been presented by **Chein**. The reported circuit has capacitor control of oscillation frequency and requires equal valued resistors.

Komanapalli, Pandey and **Pandey** [48] reported a TOSO circuit using a single OTRA, three resistors and three capacitors. The CO and FO of this oscillator can not be adjusted independently.

In light of the above description of the reported OTRA-based TOQSOs, it thus, emerges that no TOQSO has been reported yet in the open literature so far, employing OTRAs that can provide independent adjustment of CO and FO utilizing the intrinsic property of OTRA. Furthermore, no TOSO employing a single OTRA is available in the open literature that can provide independent tunability of CO and FO while fully utilizing the intrinsic property of OTRA.

Thus, in this chapter we have proposed three new TOSO configurations using OTRAs. The first two configurations are voltage mode TOQSOs which employ three OTRAs, six resistors and three virtually grounded capacitors with independent control of CO and FO and also utilize the intrinsic property of the OTRAs. The third configuration is a single OTRA-based TOSO employing three resistors and three capacitors. The proposed TOSO provides independent control of CO and FO with equal valued capacitors.

5.3 Two New Third-Order Quadrature Sinusoidal Oscillator Configurations Employing OTRAs[1]

In this section, we present two new TOQSOs which employ three OTRAs, six resistors and three virtually grounded capacitors. These circuits are shown in Fig. 5.10. It may be noted that the OTRAs used in Fig. 5.10 utilize their intrinsic property which is beneficial from the view point of IC implementation.

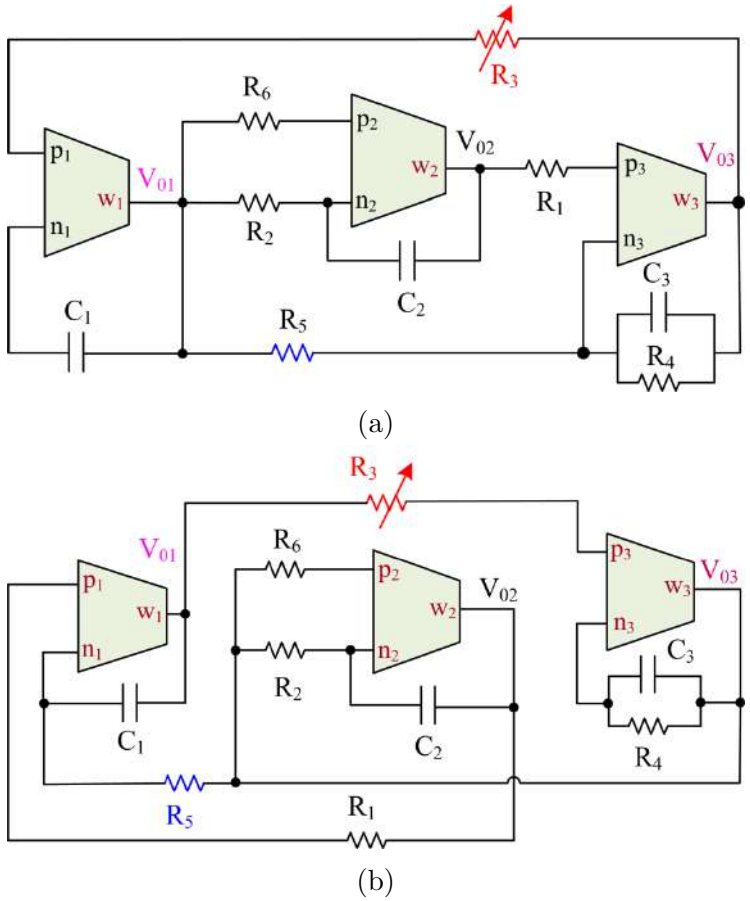


Figure 5.10: Proposed new third order quadrature sinusoidal oscillator configurations

The circuit analysis (using ideal OTRAs) of the circuits of Fig. 5.10 yields the

[1]The material presented in this section has been prepared for the possible possible publication: D. R. Bhaskar, Garima, Pragati Kumar and Ajishek Raj, "Third-Order Quadrature Sinusoidal Oscillators Employing OTRAs with Independent Control of Oscillation and Frequency"

following characteristic equation (CE) for both the proposed TOQSOs:

$$s^3C_1C_2C_3R_1R_2R_3R_4R_5R_6+s^2C_1C_2R_1R_2R_3R_5R_6+sC_2R_1R_2R_4R_6+R_4R_5(R_6-R_2)=0 \tag{5.1}$$

Applying Routh-Hurwitz's criterion on equation 5.1, the CO and FO of the presented TOQSOs can be obtained as:

$$CO: \qquad R_5=\frac{C_2R_1R_2R_6}{C_3R_4(R_6-R_2)} \tag{5.2}$$

$$FO: \qquad f_0=\sqrt{\frac{\left(\frac{R_4}{R_3}\right)\left(1-\frac{R_2}{R_6}\right)}{C_1C_2R_1R_2}} \tag{5.3}$$

From equations 5.2 and 5.3, it can be seen that the proposed oscillators have independent CO and FO tunability features. The CO of the TOQSOs can be controlled independently by resistor R_5 while FO can be tuned independently through resistor R_3.

It is interesting to mention here that the two output voltages of both the proposed TOQSOs are in quadrature and their relationships can be expressed as:

$$Fig.\ 5.10a \qquad \frac{V_{01}}{V_{03}}=\frac{1}{sC_1R_3} \tag{5.4}$$

$$Fig.\ 5.10b \qquad \frac{V_{03}}{V_{02}}=\frac{1}{sC_2R_6}\left(\frac{1}{sC_1R_3}\right) \tag{5.5}$$

From equations 5.4 and 5.5, it is noted that the output voltages V_{01} and V_{03} for the circuit of Fig. 5.10a and V_{02} and V_{03} for the oscillator circuit of Fig. 5.10b are in quadrature.

5.3.1 Non-Ideal Analysis and Sensitivity Analysis

5.3.1.1 Effect of Non-Idealities on the proposed TOQSOs

The behaviour of the proposed TOQSOs under the non-ideal conditions has also been examined using a non-ideal model of the OTRA which is shown in Fig. 5.11.

For obtaining the non-ideal model of OTRA, we have neglected the parasitic

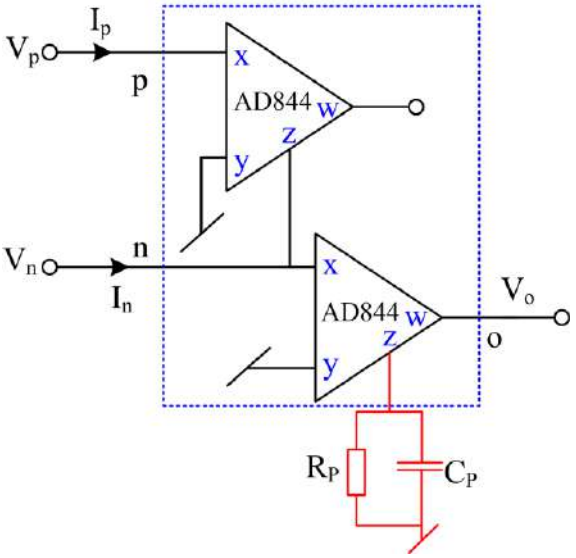


Figure 5.11: Non-ideal model of OTRA implemented with AD844s [49]

resistances associated with X-terminals of both the CFOAs. Simple circuit analysis of the circuit shown in Fig. 5.11 shows that:

$$V_0 = (I_p - I_n)\left(\frac{R_p}{sC_pR_p + 1}\right) \tag{5.6}$$

where

$$R_m(s) = \frac{R_0}{1 + \frac{s}{\omega_0}} \tag{5.7}$$

For frequencies much larger than ω_0, $R_m(s)$ reduces to:

$$R_m(s) = \frac{1}{sC_p} \tag{5.8}$$

Using equation 5.7, the non-ideal CE of the proposed TOQSOs has been obtained and expressed as:

$$\begin{aligned} s^3C_1C_2C_3R_1R_2R_3R_4R_5R_6 + s^2R_1R_2R_3R_5R_6\left(\tfrac{C_3(C_1+C_2)}{R_m} + C_1C_2\left(1+\tfrac{R_4}{R_m}\right)\right) + \\ sR_1R_2R_4R_6\left(\tfrac{R_3R_3}{R_m^2R_4}\left(\left(C_1+C_2\right)\left(R_m+R_4\right)+C_3R_4\right)+C_2\right) + \\ \tfrac{R_1R_2R_3R_5R_6(R_4+R_m)}{R_m^3} - \left(\tfrac{R_1R_2R_4R_6}{R_m} - R_4R_5\left(R_6-R_2\right)\right) \end{aligned} = 0 \tag{5.9}$$

Non-ideal CO and FO are obtained by applying Routh-Hurwitz criterion on equation (5.9), as:

$$\begin{aligned} & C_1C_2C_3\left(\frac{R_1R_2R_3R_5R_6(R_4+R_m)}{R_m^3}-\frac{R_1R_2R_4R_6}{R_m}-R_4R_5\left(R_6-R_2\right)\right)= \\ CO: \quad & R_1R_2R_6\left(\frac{R_3R_5}{R_m^2R_4}\left(\left(C_1+C_2\right)\left(R_m+R_4\right)+C_3R_4\right)+C_2\right) \\ & \left(\frac{C_3(C_1+C_2)}{R_m}+C_1C_2\left(1+\frac{R_4}{R_m}\right)\right) \end{aligned} \tag{5.10}$$

$$FO: \omega_0^{/}=\sqrt{\frac{\left(\frac{R_4}{R_3}\right)\left(1-\frac{R_2}{R_6}\right)}{R_1R_2\left(C_1C_2+C_p\left(C_1+C_2\right)+C_p^2\right)}} \tag{5.11}$$

From equations (5.10) and (5.11), it can be clearly seen that the CO and FO of the proposed TOQSOs are affected by the non-idealities inherent in the OTRA, but at higher frequencies, the value of C_p is very small, the expressions of CO and FO become ideal one.

5.3.2 Sensitivity Analysis

The tolerances in component values cause the deviation in the response of actual oscillator from the ideal response. Therefore, we have evaluated the sensitivity of FO with respect to passive elements. The sensitivity of a function can be calculated using the classical definition:

$$S_x^{F(x)}=\frac{x}{F(x)}\frac{\partial F(x)}{\partial x} \tag{5.12}$$

where F(x) denotes a circuit parameter and x denotes the parameter of interest. The sensitivities of FO with respect to parameter of interest have been evaluated and are given by:

$$\begin{gathered} S_{R_4}^{\omega_0}=\frac{1}{2},\ S_{R_1}^{\omega_0}=\ S_{R_3}^{\omega_0}=,\ S_{C_1}^{\omega_0}=\ S_{C_2}^{\omega_0}=\frac{-1}{2} \\ S_{R_2}^{\omega_0}=\frac{-1}{2}\frac{1}{1-\frac{R_6}{R_2}},\ S_{R_6}^{\omega_0}=\frac{-1}{2}\frac{1}{1-\frac{R_6}{R_2}} \end{gathered} \tag{5.13}$$

$$S_{C_1}^{\omega/} = \frac{-1}{2}\left(\frac{1+\frac{C_p}{C_2}}{1+\frac{C_p}{C_1}+\frac{C_p}{C_2}+\frac{C_p^2}{C_1C_2}}\right), \quad S_{C_2}^{\omega/} = \frac{-1}{2}\left(\frac{1+\frac{C_p}{C_1}}{1+\frac{C_p}{C_1}+\frac{C_p}{C_2}+\frac{C_p^2}{C_1C_2}}\right)$$
$$S_{C_p}^{\omega/} = \frac{-1}{2}\left(\frac{1}{1+\frac{C_1C_2}{C_p(C_1+C_2+C_p)}}\right) \tag{5.14}$$

From equations (5.13) and (5.14), it can be observed that the sensitivities of FO with respect to passive components lie between $-0.5 \leq S_x^{\omega_0} \leq 0.5$ and below -0.5 or 0 in case of non-ideal FO with parasitic effect.

5.3.3 Simulation and Experimental Results

Performance of the proposed TOQSO circuits has been tested using PSPICE simulations. The OTRA has been implemented with macro model of AD844 type CFOAs [50]. The implementation of OTRA using AD844 has been demonstrated in Fig. 5.12. For the biasing of AD844, the power supply voltages (V_{DD} and V_{SS}) were set at ±10V.

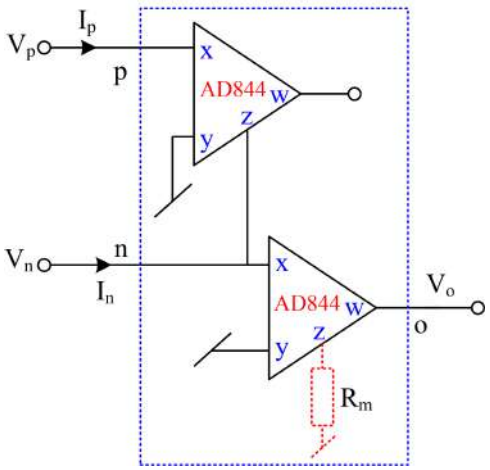
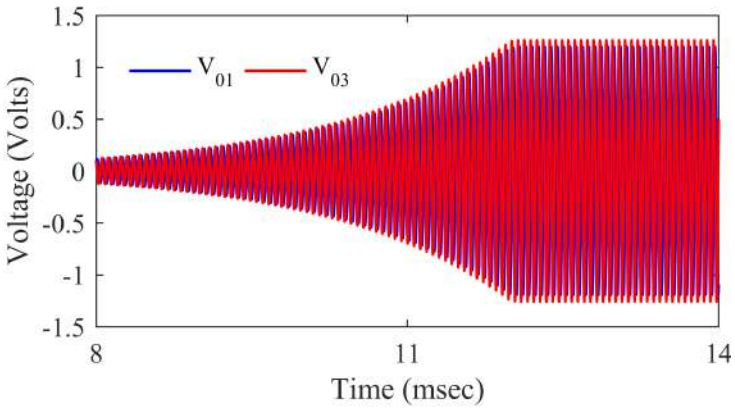
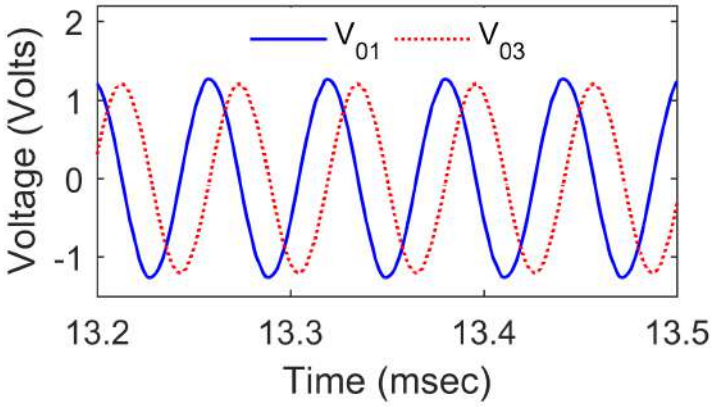


Figure 5.12: Implementation of OTRA using AD844 CFOAs

Both the proposed TOQSOs were designed for a nominal frequency of oscillation of 16.61 kHz for which the passive components were selected as: $R_1 = 5k\Omega, R_2 = R_4 =$ 1kΩ, $R_3 =$ 10kΩ, $R_5 =$ 9.16kΩ, $R_6 =$ 2.2kΩ with equal valued capacitors of 1nF. Fig. 5.13 and Fig. 5.14 demonstrate the simulated transient and steady-state responses of the TOQSOs presented in Fig. 5.10a and Fig. 5.10b respectively.

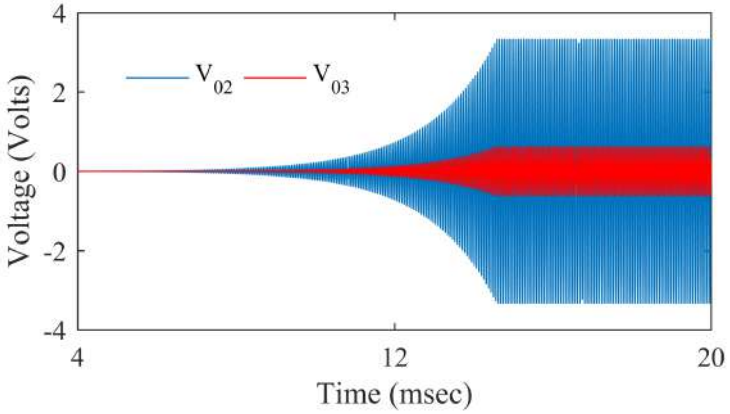


(a)

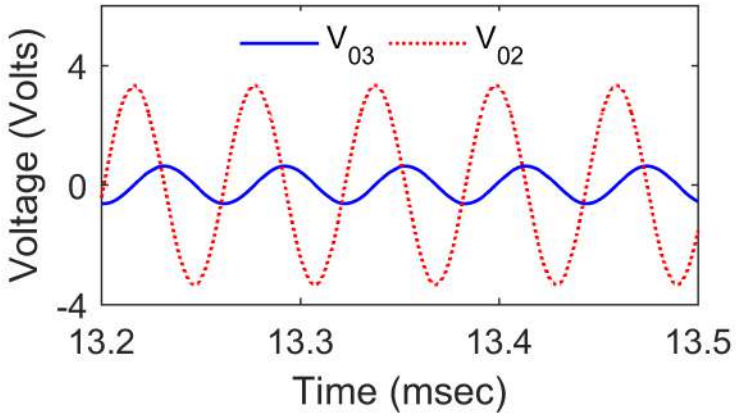


(b)

Figure 5.13: Simulated transient and steady state responses of Fig. 5.10a



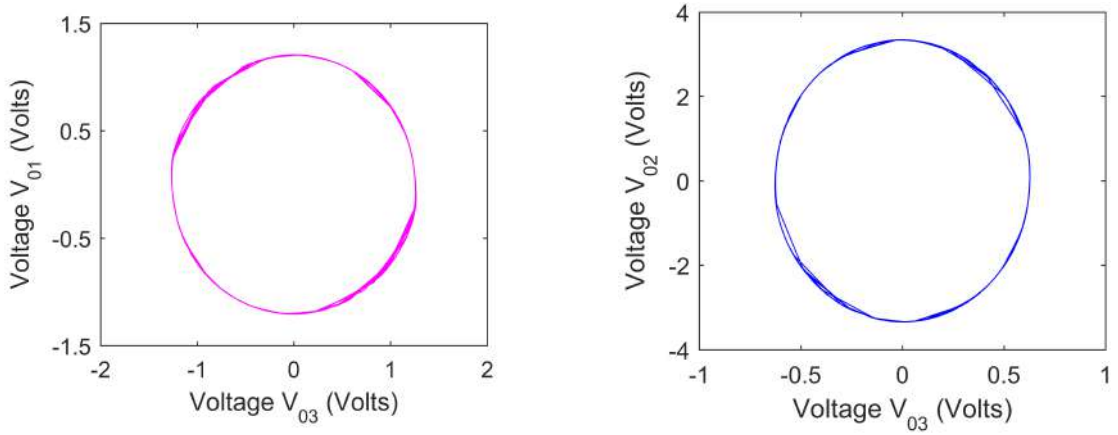
(a)



(b)

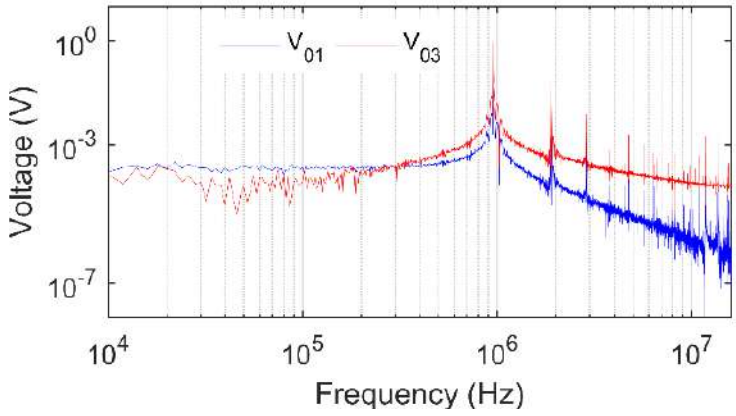
Figure 5.14: Simulated transient and steady state responses of Fig. 5.10b

The simulated FO obtained for Fig. 5.10a and Fig. 5.10b are found to be 16.493 kHz and 16.5 kHz respectively which are very close to the designed value (16.61 kHz). The Lissajous patterns (X-Y plots) of proposed oscillators are demonstrated and the corresponding simulated responses have been depicted in Fig. 5.15. The frequency spectrum of the proposed TOQSOs have been given in Fig. 5.16. The variation in FO for both the oscillator circuits has been carried out by varying R_3 and the same has been displayed in Fig. 5.17a. The variations of %THD for circuit of Fig. 5.10b have been demonstrated in Fig. 5.17b.

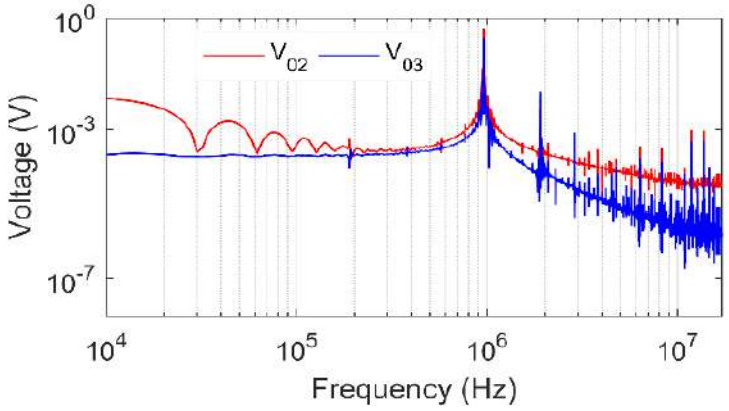


(a) (b)

Figure 5.15: Lissajous patterns of the proposed TOQSO (a)Fig. 5.10a, (b) Fig. 5.10b

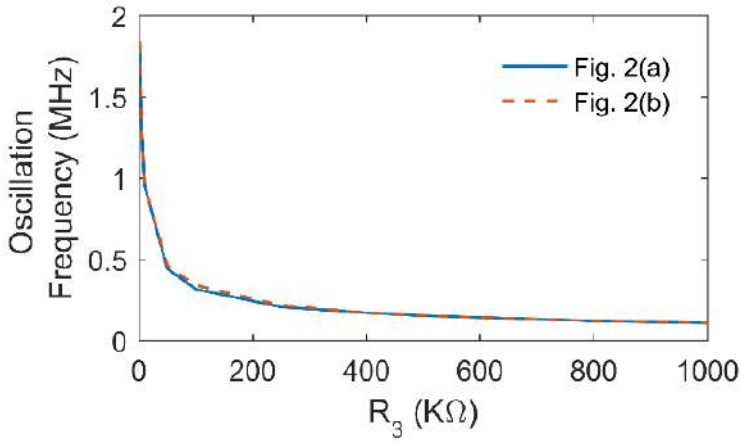


(a)

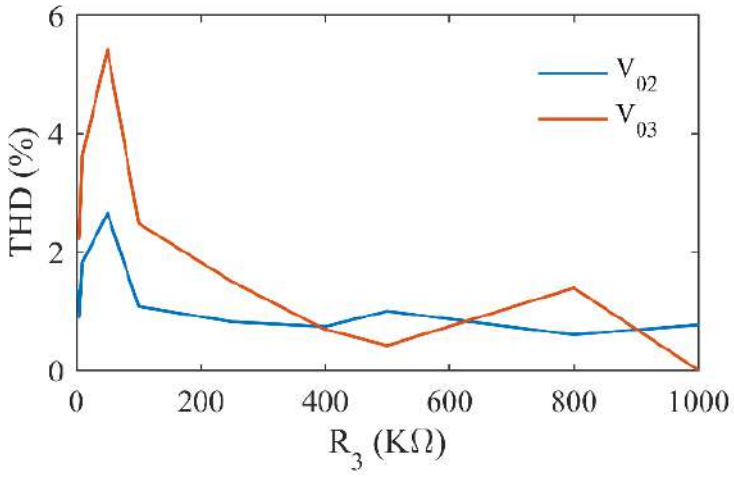


(b)

Figure 5.16: Frequency spectrum of the proposed TOQSO (a)Fig. 5.10a, (b) Fig. 5.10b



(a)



(b)

Figure 5.17: Variation in frequency with resistor R_3 for both the proposed TOQSOs (b) %THD for the circuit shown in Fig. 5.10b

5.3.3.1 Experimental Results

The presented TOQSOs have also been tested experimentally using OTRAs implemented with commercially available off-the-shelf CFOA ICs (as shown in Fig. 5.12), 5% tolerance resistors and 10% tolerance capacitors. The experimental snapshot of the bread-boarded TOQSO of Fig. 5.10b has been shown in Fig. 5.18.

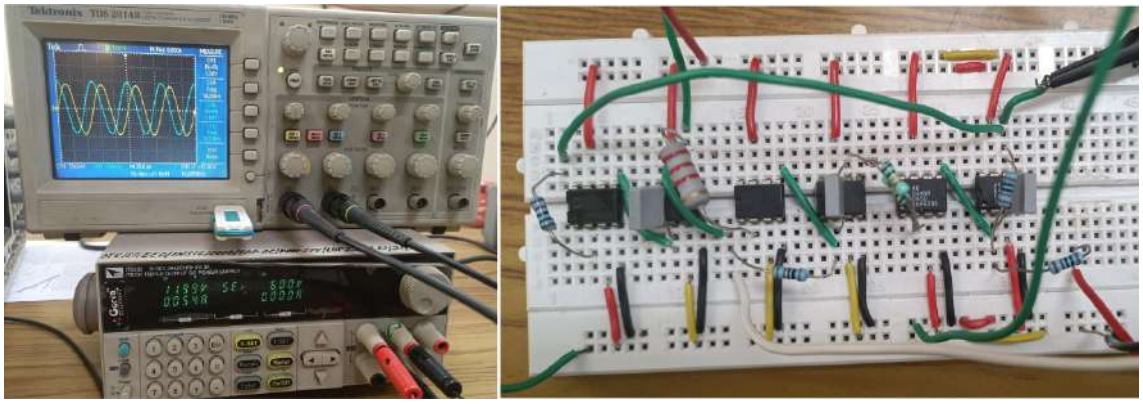


Figure 5.18: Snapshot of the experimental set-up for Fig. 5.10b

For the experimentation, TOQSOs were designed for the nominal frequency of 16.65 kHz for which the passive components were chosen as: $R_1 = 5\text{k}\Omega$, $R_2 = 1\text{k}\Omega$, $R_3 = 10\text{k}\Omega$, $R_4 = 1\text{k}\Omega$, $R_6 = 2.2\text{k}\Omega$, $C_1 = C_2 = C_3 = 1\text{nF}$ and $R_5 = 1\text{k}\Omega + 10\text{k}\Omega$ pot. The experimentally obtained transient responses and frequency spectra of the quadrature output voltages of Fig. 5.10a and Fig. 5.10b have been displayed in Fig.

5.19 and Fig. 5.20 respectively. The percentage total harmonic distortion (%THD) of the quadrature voltage waveforms of the presented TOQSOs (V_{01} and V_{03} for Fig. 5.10a and V_{02} and V_{03} for Fig. 5.10b) was recorded experimentally using Keysight DSO X3034 .

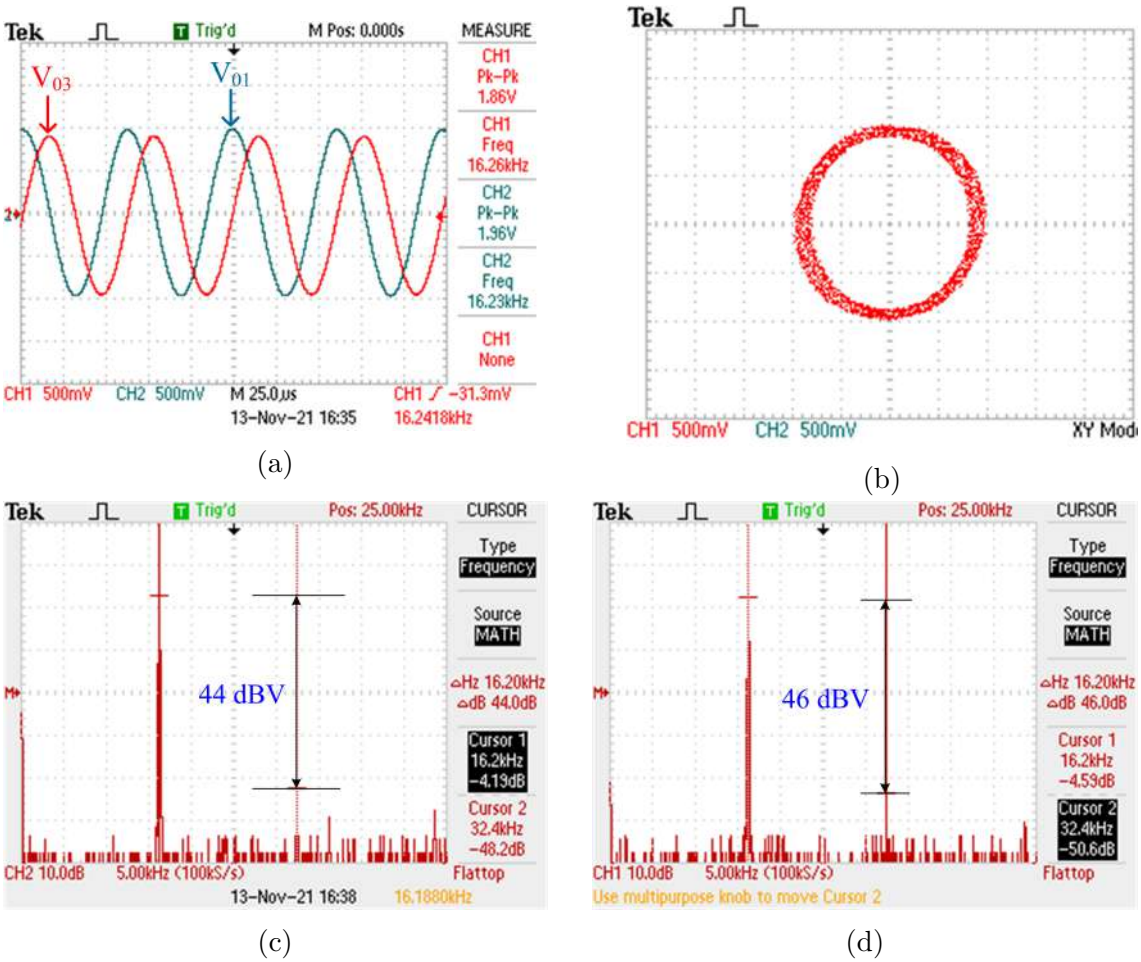


Figure 5.19: Experimental results of Fig. 5.10 (a) Quadrature waveforms (b) Lissajous pattern (c) Frequency spectrum of V_{01} and (d) Frequency spectrum of V_{03}

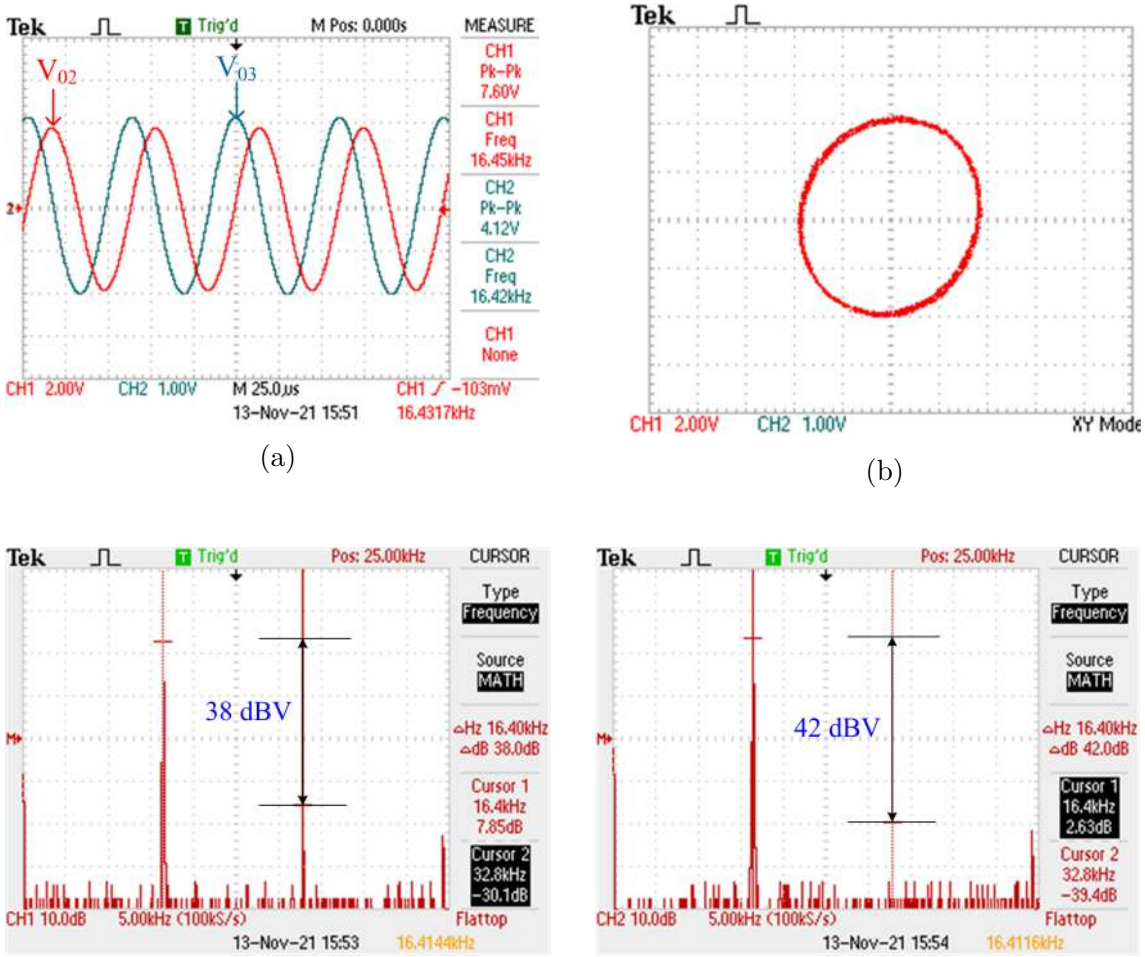
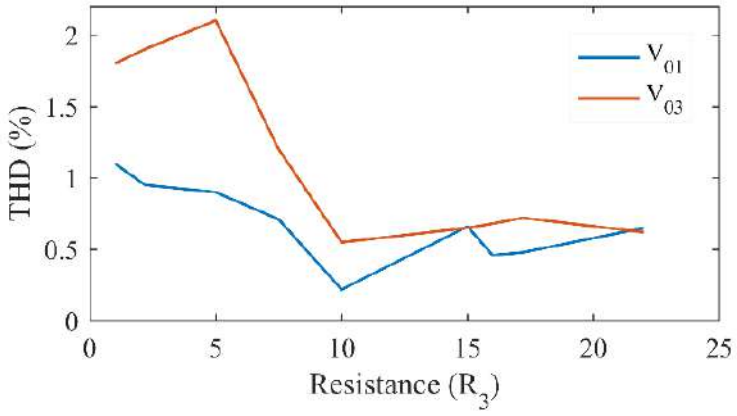


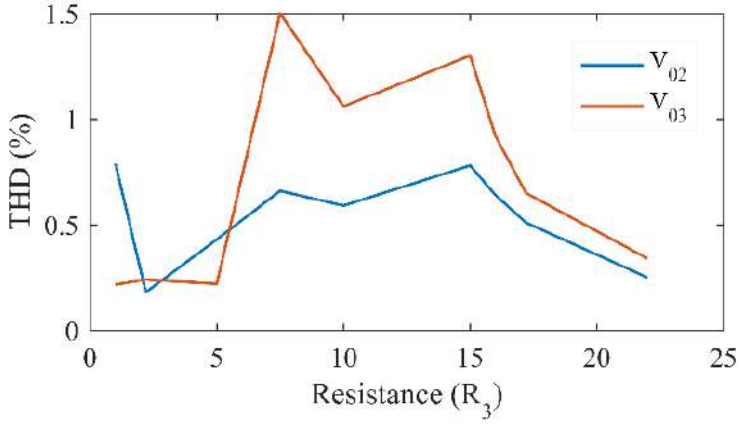
Figure 5.20: Experimental results of Fig. 5.10b (a) Quadrature waveforms (b) Lissajous pattern (c) Frequency spectrum of V_{03} and (d) Frequency spectrum of V_{02}

The experimentally obtained frequencies for both the oscillator circuits were found to be 16.26 kHz and 16.45 kHz against the theoretical value of 16.65 kHz. The maximum %THDs for both the quadrature voltages of the proposed circuits were found to be less than 2% and 1.5% respectively. The variation of %THD with resistor R_3 for the quadrature output voltages for the circuits of Fig. 5.10a and Fig. 5.10b have been displayed in Fig. 5.21a and Fig. 5.21b respectively.

The tunability of the FO for both the TOQSOs was also demonstrated experimentally by varying the resistor R_3 from 1kΩ to 22kΩ and correspondingly, the frequency was varied from 45.81kHz to 11.16kHz and the same have been displayed in Fig. 5.22a.



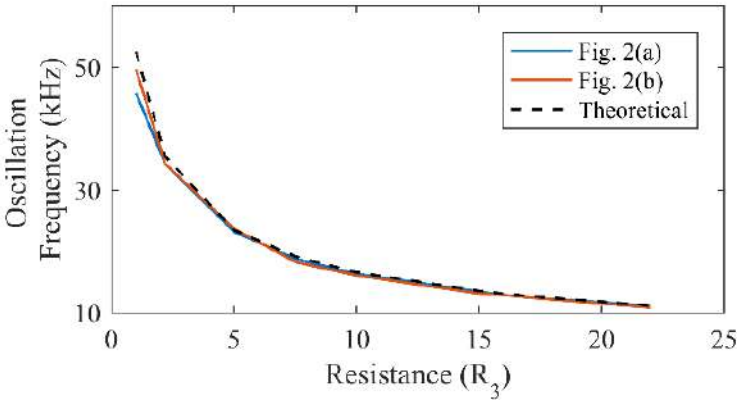
(a)



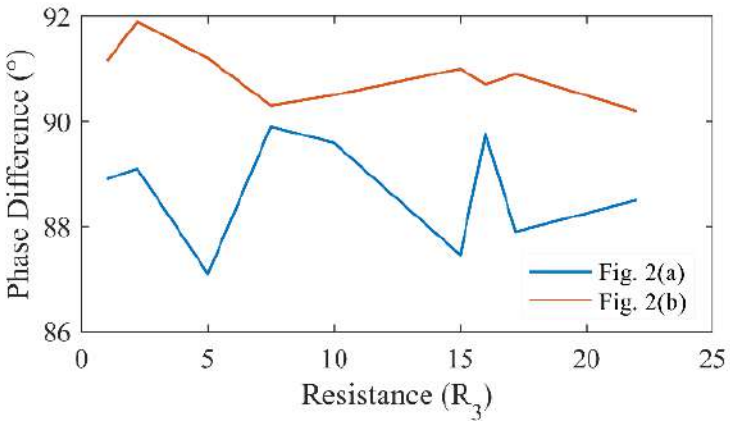
(b)

Figure 5.21: Variation of %THD with R_3 for the quadrature output voltages for the circuits of (a) Fig. 5.10a and (b) Fig. 5.10b

The experimentally obtained phase error between quadrature output voltages was also examined and corresponding results have been displayed in Fig. 5.22b for the TOQSOs of Fig. 5.10a and Fig. 5.10b.



(a)



(b)

Figure 5.22: (a) Variation in FO with resistor R_3 , (b) Phase difference between the quadrature output voltages

These simulation and experimental results, thus, validate the functionality of the proposed TOQSOs.

5.4 Single OTRA-based Third-Order Sinusoidal Oscillator with Independent Controllability of CO and FO[2]

In section 5.3, two TOQSOs employing two OTRAs along with six resistors and three virtually grounded capacitors have been presented. Both the TOQSO circuits have independent control of CO and FO through seperate resistors. A large number of active and passive components in a circuit results in more power dissipation. Thus, in this section, we present a single OTRA-based third order sinusoidal oscillator (TOSO) circuit which employs canonic number of resistors (03) and virtually grounded capacitors (03) with independent control of CO and FO. The proposed TOSO circuit is given in Fig. 5.23.

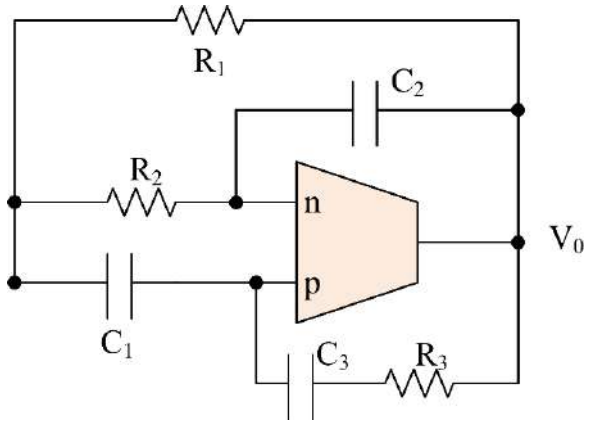


Figure 5.23: Proposed third order sinusoidal oscillator configuration

Assuming ideal OTRA, the CE of the TOSO circuit of Fig. 5.23 is given by:

$$\begin{aligned} s^3C_1C_2C_3R_1R_2R_3 + s^2C_3R_3\left(C_2R_1 + C_2R_2 - C_1R_2\right) + s^2C_1R_1R_2\left(C_2 - C_3\right) \\ +s\left(C_3R_3 - C_1R_2 + \left(C_2 - C_3\right)\left(R_1 + R_2\right)\right) + 1 = 0 \end{aligned} \tag{5.15}$$

For sustained oscillations, one of the roots of the (5.15) should lies in the left half of s-plane while two of the roots of the equation (5.15) must lie on the imeginary

[2]The material presented in this section has been prepared for the possible publication in journal: Garima, D. R. Bhaskar and Pragati Kumar "Single OTRA-based Third-Order Sinusoidal Oscillator with Independent Control of CO and FO".

axis (jω). These roots can be calculated by applying Routh-Hurwitz criterion on the equation (5.15) as:

$$\begin{aligned} CO: \quad & C_1C_2C_3R_1R_2R_3 \geq (C_3R_3\left(C_2R_1+C_2R_2-C_1R_2\right)+C_1\left(C_2-C_3\right)R_1R_2) \\ & \left(C_3R_3-C_1R_2+\left(C_2-C_3\right)\left(R_1+R_2\right)\right) \\ FO: \quad & \omega_0=\sqrt{\frac{C_3R_3-C_1R_2+C_2(R_1+R_2)-C_3(R_1+R_2)}{C_1C_2C_3R_1R_2R_3}} \end{aligned} \tag{5.16}$$

For independent controllability of CO and FO of the TOSO shown in Fig. 5.23, a special case is considered assuming $C_1 = C_2 = C_3 = C$, reducing equation (5.15) to:

$$s^3C^3R_1R_2R_3+s^2C^2R_1R_3+sC\left(R_3-R_2\right)+1=0 \tag{5.17}$$

With the condition stated above, CO and FO of equation (5.16), turns out to be:

$$\begin{aligned} CO: \quad & R_2=\tfrac{R_3}{2} \\ FO: \quad & \omega_0=\sqrt{\tfrac{1}{C^2R_1R_3}} \end{aligned} \tag{5.18}$$

The equation (5.18) shows that the CO and FO of the proposed TOSO can be controlled independently i.e., CO of the TOSO can be set by resistor R_2 while FO can be independently tuned through resistor R_1.

5.4.1 Effect of Non-Idealities of OTRA

The behaviour of the proposed TOSO under non-ideal conditions has also been examined using a non-ideal model of the CMOS OTRA proposed in [49], given as under:

$$R_m(s)=\frac{R_0}{1+\frac{s}{\omega_0}} \tag{5.19}$$

At higher frequencies ($\omega >> \omega_0$), equation (5.19) reduced to:

$$R_m(s)=\frac{1}{sC_p} \tag{5.20}$$

where $C_p = \frac{1}{R_0\omega_0}$ Using equation (5.20), the non-ideal CE of the proposed TOSO has been evaluated and expressed as:

$$s^3C^3R_1R_2R_3 + s^2C^2R_1R_3 + sC\left(R_3 - R_2\right) + sC\left(\frac{R_1R_2}{R_m}\right) + \left(1 + \left(\frac{R_1R_2}{R_m}\right)\right) = 0 \tag{5.21}$$

Substituting the value of R_m in equation (5.21), we get:

$$s^3C^3R_1R_2R_3 + s^2C^2R_1R_3 + s^2CC_pR_1R_2 + sC\left(R_3 - R_2\right) + sC_p\left(R_1 + R_2\right) + 1 = 0 \tag{5.22}$$

Now, the non-ideal CO and FO of the proposed TOSO can be obtained from equation eq4.181, and may be written as::

$$\begin{aligned} CO: \quad & 2R_2\left(1 - \tfrac{C_p}{C} - \tfrac{C_pR_2}{2CR_3} + \tfrac{C_p^2R_2}{2C^2R_3} - \tfrac{C_p^2R_1}{2C^2R_3}\right) = R_3 + \tfrac{C_p}{C} \\ FO: \quad & \omega_0^{/} = \sqrt{\frac{1}{C^2R_1R_3\left(1 + \frac{C_pR_2}{CR_3}\right)}} \end{aligned} \tag{5.23}$$

A careful observation of equation (5.23) shows that the effect of non-idealities of OTRA on the FO of the proposed TOSO can be minimized by taking external capacitors C higher than the value of C_p within the restrictions of the maximum and minimum values of capacitors possible to be used in conjunction with OTRA.

5.4.2 Sensitivity Analysis

The sensitivities of FO of the proposed TOSO shown in Fig. 5.23 with various parameters have also been evaluated using the classical definition which is given in equation (5.24):

$$S_x^{F(x)} = \frac{x}{F(x)}\frac{\partial F(x)}{\partial x} \tag{5.24}$$

where F(x) denotes a circuit parameter and x denotes parameter of interest.

The sensitivities of FO with respect to passive components and parasitic can be evaluated as:

$$S_{R1}^{\omega_0} = -0.5, S_{R2}^{\omega_0} = -0.5, S_C^{\omega_0} = -1, \tag{5.25}$$

From equation (5.25), it can be seen that the sensitivities of FO with respect to various parameters lie between $-0.5 \leq S_x^{F(x)} \leq 1$

5.4.3 Simulation Results

Performance of the proposed TOSO circuit has been tested using exemplary CMOS OTRA derived from [51] implemented in 0.18μm with TSMC technology parameters. The MOS implementation of OTRA has been shown in Fig. 5.24 and the aspect ratios of the various MOSFETs used have been given in Table 5.1.

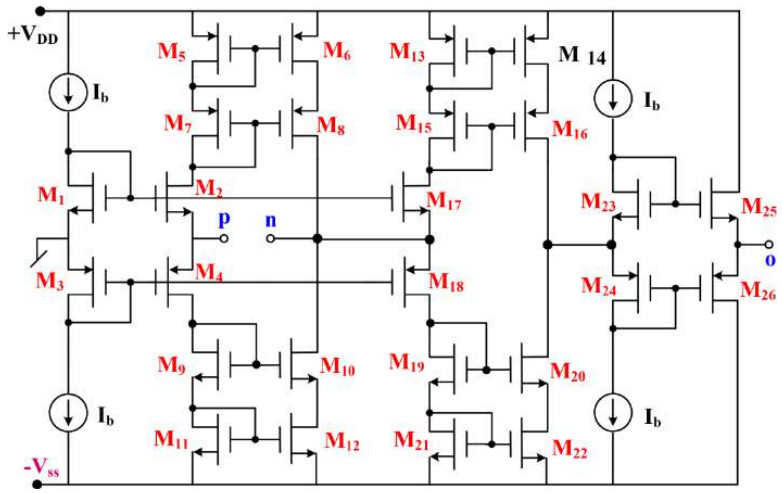


Figure 5.24: CMOS OTRA

Table 5.1: Aspect ratios of MOSFETs shown in Fig. 5.24

MOSFETs	Aspect Ratio (W/L) in μm
$M_1, M_2, M_{17}, M_{23}, M_{25}$	50/0.5
$M_3, M_4, M_{18}, M_{24}, M_{26}$	100/0.5
$M_5 - M_{16}$,$M_{19} - M_{22}$	3.33/0.5

For biasing the OTRA, the power supply voltages (V_{DD} and V_{SS}) were taken as $\pm$0.9V and the bias currents (I_b) were set at 40 μA.

The proposed TOSO was designed for a nominal frequency of oscillation of value 15.9 kHz. To obtain this value of FO, the passive components used in Fig. 5.23 were taken as: $R_1 = R_3 = 10k\Omega, R_2 = 6k\Omega$ and equal valued capacitors of value 1nF. Fig. 5.25 demonstrates the steady-state responses and the frequency spectra

of the output voltage of the circuit of Fig. 5.23.

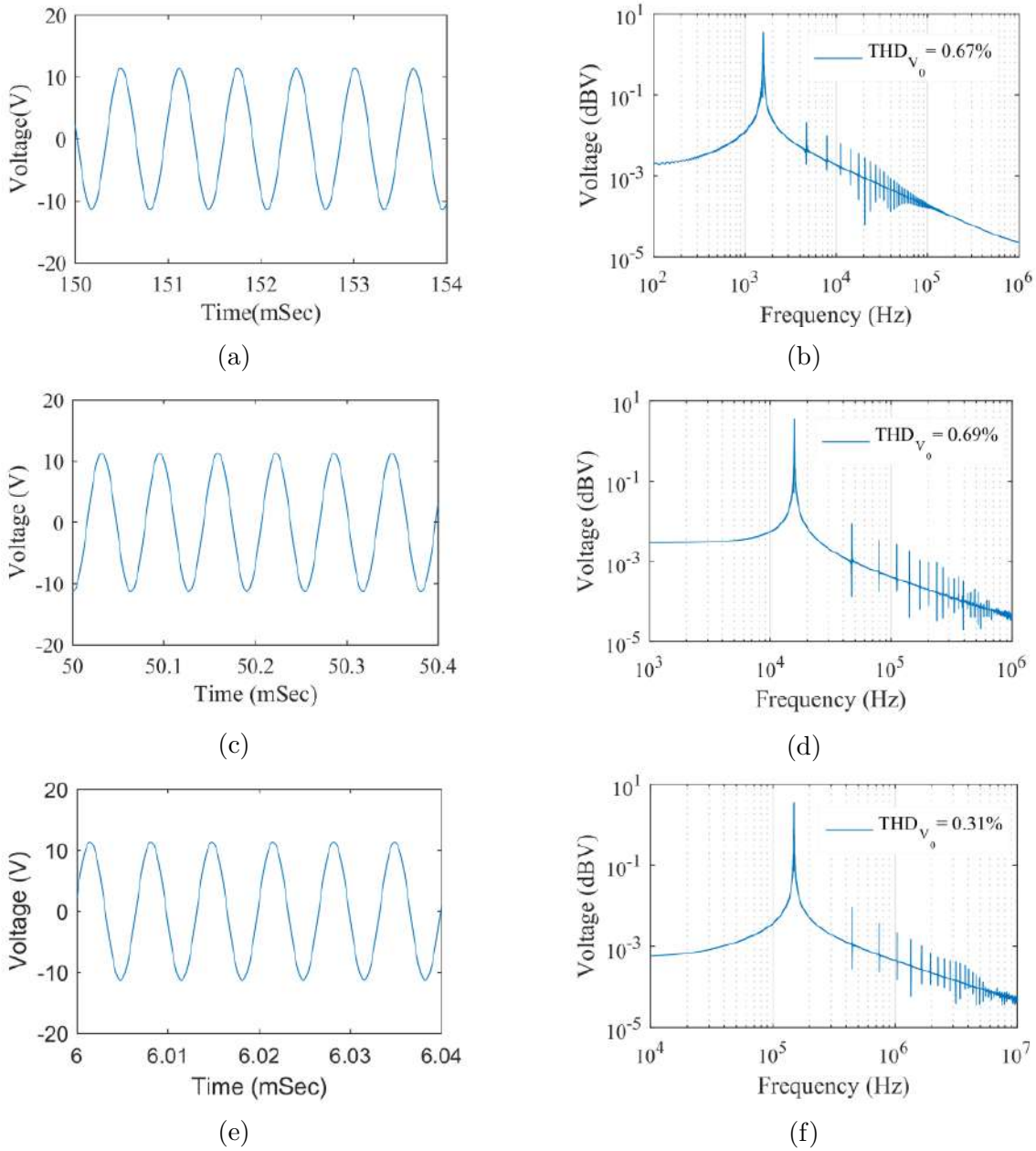


Figure 5.25: Simulated steady state responses and their frequency spectra of the circuit of Fig. 5.23

5.4.4 Experimental Results

To justify the functionality of the proposed TOSO circuit shown in Fig. 5.23, the circuit was bread-boarded using OTRA implemented with commercialy available

off-the-shelf IC AD844, as given in Fig. 5.12.

The snapshot of experimental set-up of the proposed TOSO of Fig. 5.23 has been displayed in Fig. 5.26.

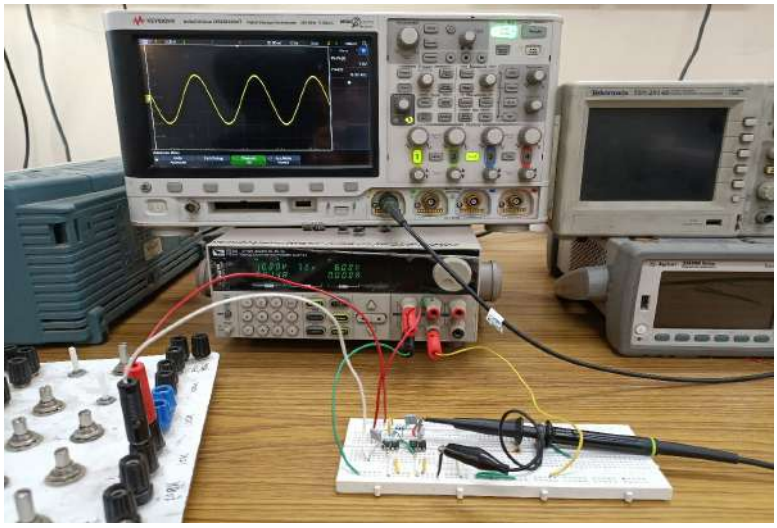
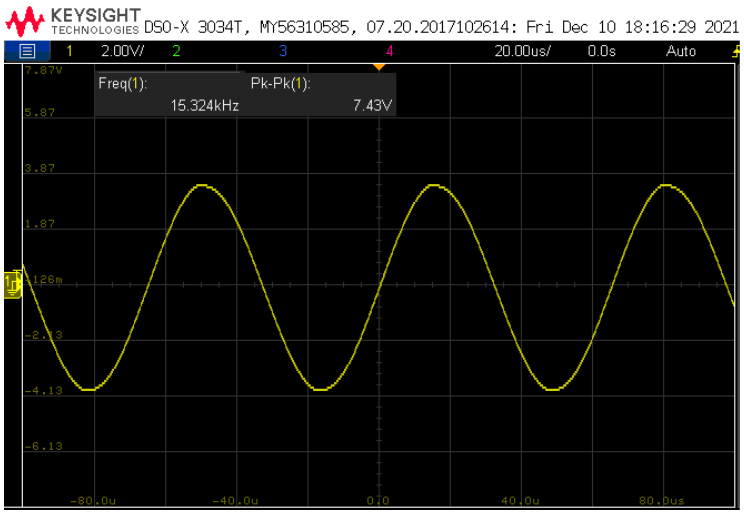
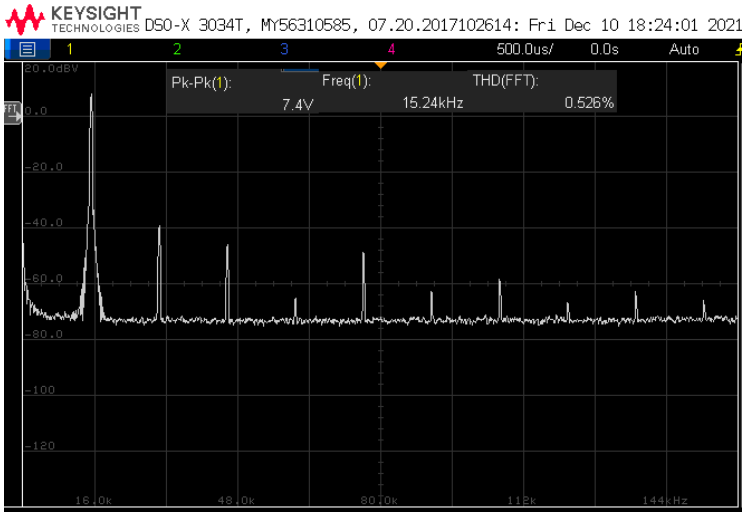


Figure 5.26: Snapshot of the experimental set-up for Fig. 5.23

For the experimental verification, proposed TOSO was designed for the nominal frequency of 15.9 kHz for which the passive components (resistors with 5% tolerances and capacitors with 10% tolerances) were chosen as: $R_1 = 10k\Omega, R_3 = 10k\Omega, C_1 = C_2 = C_3 = 1$nF and $R_3 = 1k\Omega + 10k\Omega$ pot. The experimentally obtained transient response and frequency spectrum of the output voltage of the circuit of Fig. 5.23 have been displayed in Fig. 5.27.



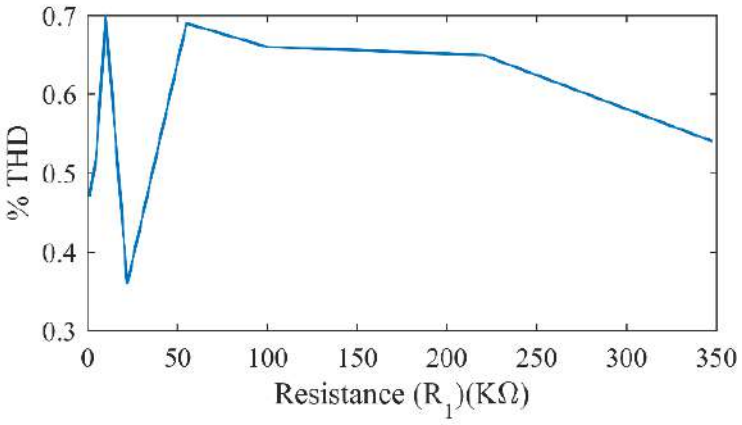
(a)



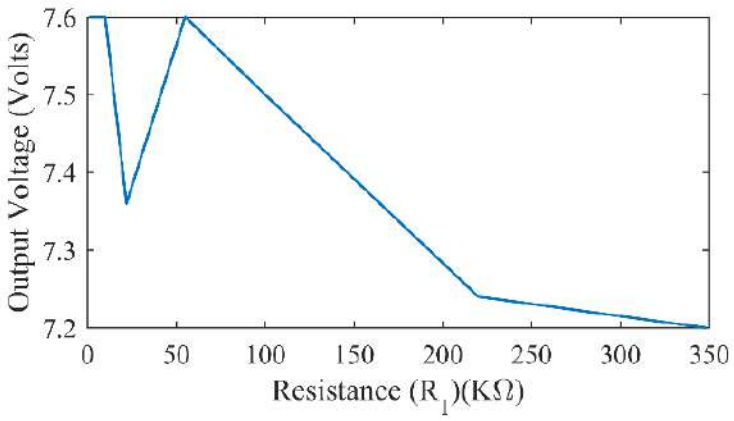
(b)

Figure 5.27: Experimental results (a) time response of output voltage and (b) frequency spectrum of the circuit of Fig. 5.23

The percentage total harmonic distortion (%THD) of the voltage waveform of the presented TOSO for Fig. 5.23 was recorded experimentally using Keysight X3034 DSO and the maximum %THD were found to be 0.7%. The variation of %THD with resistor R_1 for the output voltage of circuits of Fig. 5.23 has been displayed in Fig. 5.28a and in Fig. 5.28b, the variation of output voltage with resistor R_1 has been displayed. The variation of FO with respect to variation in R_1 has been depicted in Fig. 5.29.



(a)



(b)

Figure 5.28: (a) Experimental variation of %THD with resistor R_1 (b) Experimental variation of output voltage with resistor R_1

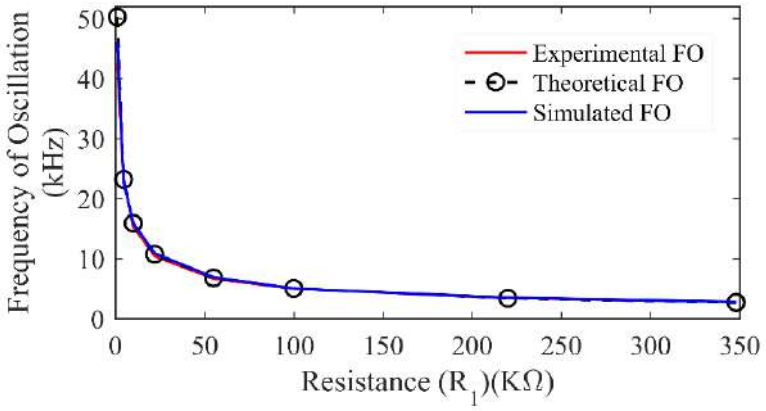


Figure 5.29: Variation in FO for different values of resistor R_1

Thus, the above simulated and experimental results validated the workability of the proposed TOSO.

5.5 Concluding Remarks

The main contributions made in this chapter can be summarized as follows:
Two new configurations of TOQSOs employing three OTRAs, six resistors and three virtually grounded capacitors have been presented. The intrinsic property of OTRA (current differencing property which is useful to reduce the noise injection into the monolitic integration and also reduce the silicon chip area in IC implementation) has been utilized to derive the TOQSOs. The CO of both the proposed circuits have independent controllabilty with FO while FO of the proposed TOQSO circuits can also be tuned independently. Non-ideal and sensitivity analyses for both the proposed TOQSO circuits have been carried out using a one-pole model of the OTRA. It is found that there is insignificant % error between ideal and non-ideal FO. Simulation results have been included along with the experimental results to verify the validity of the proposed TOQSO circuits. For simulation validation, OTRA implemented with macro model of AD844 type CFOAs has been used. The proposed circuits were breadboarded also for experimental validation using OTRA implemented with off-the-shelf AD844 ICs.
We have also presented a single OTRA based third order sinusoidal oscillator circuit with three resistors and three virtually grounded capacitors. The proposed circuit has independent controllability of CO and FO. Sensitivity analysis has also been carried out and the sensitivities of FO with respect to active and passive components are found to be low. The workability of the proposed circuit has been validated using CMOS OTRA implemented in 0.18 μm CMOS technology parameters and also experimental results have been appended using OTRA implemented with commercially available analog ICS AD844.

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Chapter 6

Conclusions and Future scope

6.1 Conclusions

In this thesis, we have proposed novel circuits of immittance simulators, capacitance multiplier, biquad filters and third-order harmonic/quadrature oscillators realized with operational transresistance amplifiers. All the circuits proposed in this thesis exploit the intrinsic current differencing property of the OTRA, by utilizing both the input terminals of all the OTRAs employed, a feature which is present in very few of the prevously reported OTRA-based circuits. In the following we present a summary of the main contributions of the thesis.

Chapter 1 of this thesis describes the overview of the implementation of OTRA of different kinds. A brief overview of previously reported circuits presenting the linear and non-linear applications of OTRA has also been presented. The behavioural model of the OTRA used to validate the novel works has been discussed. The characterization of the OTRA (DC characteristic, magnitude and phase responses) has also been presented using PSPICE simulations.

In **Chapter 2**, we have presented two new configurations of grounded series/parallel lossy inductors employing a single OTRA. The first proposed circuit provides a grounded series lossy inductor simulator employing a single OTRA, one buffer, two

resistors and two capacitors. A capacitor matching constraint is also required for the realization. The realized value of inductance can be independently controlled without changing the resistance value which is in series connection with inductor. Non-ideal analysis has also been carried out with one-pole model of OTRA and compared with the ideal proposition. Functionality of the proposed circuit has been validated with PSPICE simulations using CMOS OTRA implemented in 0.18μm TSMC technology parameters. Application example has also been demonstrated using the proposed configuration.

The second configuration, on the other hand realizes a grounded parallel lossy inductor employing a single OTRA, five resistors and one virtually grounded capacitor. The proposed circuit can also be configured as a lossless inductor subject to matching constraints. The value of both lossy as well as lossless inductance can be controlled independently by a grounded resistor. Application examples of the proposed lossy inductor has also been demonstrated by realizing a second order HPF and BPF. The proposed circuit has been validated using PSPICE simulations employing a CMOS OTRA and also tested experimentally with OTRA implemented with off-the-shelf available IC AD844s. To check the robustness of the proposed parallel lossy inductor circuit, Monte Carlo simulations and temperature analysis have been carried out.

Chapter 3 of the thesis deals with the realization of a capacitance multiplier circuit using single OTRA:

The proposed circuit employs one OTRA, one voltage buffer, three virtually grounded resistors and a capacitor. The presented circuit can provide both positive as well as negative multiplication factors of a grounded capacitor with the proper selection of resistances. Furthermore, the proposed circuit has also been converted into MOS-C configuration replacing passive resistors by identical MOS transistors operating in linear region. Non-ideal analysis incorporating the non-idealities of the OTRA has also been carried out to explain the deviation from the ideal values. The positive

CM circuit has been found to work satisfactorily in the frequency range of 100 Hz - 1 MHz while the negative CM circuit has been found to work satisfactorily in the frequency range of 100 Hz - 100 kHz. Application examples of proposed capacitance multiplier in capacitance cancellation and first order low pass filter have also been discussed. Simulation results using CMOS OTRA implemented with 0.18 μm TSMC technology parameters have been presented to validate the workability of the proposed capacitance multiplier circuit. Various advanced analyses i.e., Monte-Carlo simulations, process corner and temperature analysis have been carried out for the justification of robustness of the proposed circuit. In order to validate the functionality of the proposed circuit experimentally, two analog ICs AD844 were breadboarded to implement OTRA and demonstrate the sample experimental results.

In **Chapter 4**, we have presented second-order multifunctional filter configurations using one/three OTRAs. The first circuit is based on single-input-single-output configuration. It uses one OTRA and four admittances. Depending on the choice(s) of branch admittance(s), high-pass, band-pass and low-pass responses can be obtained. The filter parameters namely the cut-off frequency, quality factor and the relevant gain of these filters are orthogonally controllable. The maximum value of pole quality factor is 0.5 in these filters. The second and third proposed circuits in this chapter, on the other hand belong to the single-input-multiple-output type employing three OTRAs, seven resistors and two virtually grounded capacitors. High-pass, band-pass and low-pass outputs are simultaneously available from three low output impedance nodes. The pole quality factor of the three filters can be adjusted independently. Also, for a given cut-off frequency, the bandwidth can be adjusted independently. Finally, the relevant gain of the filters can be adjusted independently.

Chapter 5 of the thesis deals with realization of third-order sinusoidal oscillators.

We have presented three new circuits of third-order sinusoidal oscillators. First two circuits have quadrature output voltages available at low impedance nodes while the third circuit is a single-phase third-order sinusoidal oscillator. In all the three circuits, the intrinsic current-differencing property of the OTRA, requiring none of its input-terminals to remain open/directly connected to ground, has been utilized. This helps to reduce the noise . The CO and FO of the first two circuits are controlled independently while in the third circuit, for equal valued capacitors, CO and FO can be controlled independently. PSPICE simulations using CMOS OTRAs, OTRAs realized with CFOA ICs AD844 and experimental results have been presented to establish the workability of the circuits.

6.2 Future Scope

In this thesis, several new circuits of analog active inductance simulators, capacitance multiplier, biquadratic active filters, third order sinusoidal oscillators have been proposed employing operational transresistance amplifiers. But the class of the circuits reported can not be said to be exhausted completely. The work reported in this thesis can be extended in the following directions:

(i) Realization of lossless gyrator circuit with both ports grounded using OTRAs.

(ii) Realization of a lossless grounded inductor (positive) using a single OTRA, a single capacitor and any number of resistors.

(iii) Realization of floating impedance of any kind using OTRAs.

(iv) Realization of capacitance multiplier circuits employing single OTRA with canonic number of resistors (two) and a grounded capacitor.

(v) Implementation of analog filters of SIMO type with lesser numner of active and passive components having full utilization of both input terminals of the OTRA.

(vi) Minimal realization of third-order quadrature sinusoidal oscillators providing independent control of CO and FO.

(vii) Realization of single OTRA based third-order sinusoidal oscillator without any passive component matching constraints.

Thus, there is enough scope for extending the work presented in this thesis.