QUANTUM ATK ANALYSIS OF SILICON NANOWIRE FET WITH A CYLINDRICAL METALLIC WRAP-AROUND GATE VARIED WITH DIELECTRICS

Report submitted towards the partial
fulfilment of the requirements for the award
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PHYSICS

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May 2022

CANDIDATE'S DECLARATION

I hereby certify that the work, which is presented in the Dissertation-II entitled "**Quantum ATK analysis of silicon nanowire FET with a cylindrical metallic wrap-around gate varied with dielectrics**" in fulfilment of the requirement for the award of the Degree of Master in Science in Physics and submitted to the Department of Applied Physics, Delhi Technological University, Delhi is an authentic record of our own, carried out during a period from January to May 2022, under the supervision of **Prof. Rishu Chaujar.**

The work presented in this report has not been submitted and not under consideration for the award for any other course/degree of this or any other Institute/University. The work has been communicated in peer reviewed Scopus indexed conference & journal with the following details:

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I hereby certify that the project Dissertation titled “Quantum ATK analysis of silicon nanowire FET with a cylindrical metallic wrap-around gate varied with Dielectrics” which is submitted by RAHUL SHARMA (2K20/MSCPHY/25), TRIPTI GAUR (2K20/MSCPHY/40) [Masters in Physics], Delhi Technological University, Delhi. A documentation of the project work completed by students under my supervision, in full fulfilment of the requirement for the award of the Masters of Science degree. To the best of my knowledge, this work has never been presented in part or in full for a degree or diploma at this university or anywhere else.

RChaujar

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Date:10.05.22

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ABSTRACT

In this work, the application of dielectrics to the Silicon Nanowire Gate All Around Field Effect Transistor is discussed. Employing quantum ATK software, device is studied at three distinct dielectric constants (4,9,25). Sub-threshold circumstances such as subthreshold slope, I_{ON} and I_{OFF} currents are explored at each dielectric. Calculated parameters and results were compared to three different dielectrics (4,9,25) with the same channel length. The I_{ON} /I_{OFF} ratio for dielectric 4,9,25 was determined to be 0.86 x 10^7, 0.22 x 10^7, and 0.12 x10^7 for the mentioned device, respectively. The subthreshold slopes were computed as 298.416 mV/dec, 285.8914 mV/dec, and 190.66 mV/dec for the same three dielectrics (4,9,25 respectively). Also, transmission spectrum was also calculated without dielectric explaining the transport of electrons at gate voltage, V_G = 0.5V. Many further analyzes were carried out to see how the proposed device may be used for sensing applications.

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List of Abbreviations

CMOS	Complementary Metal Oxide Semiconductor
VLSI	Very Large-Scale Integration
DG	Double gate
SCE	Short channel effect
SiNW FET	Silicon Nanowire Field Effect Transistor
GAA -	Gate All Around
MRI -	Magnetic Resonance Imaging
CT	Computed Tomography
ATK	Atomistix ToolKit
DFT	Density Afunctional Theory

CHAPTER 1
INTRODUCTION

CHAPTER 1: INTRODUCTION

1.1 CMOS Technology: Developments and Challenges

In 1975, Gordon Moore amended his prognosis, indicating that the doubling will occur every two years on average. "Moore's Law" is the name given to this predictive model, has served as a benchmark for the semiconductor industry, motivating them to push harder to breach technological barriers through ongoing innovation [1].

Figure 1.1 shows that, in accordance with Moore's Law Every year, the transistor count per chip has risen. The semiconductor industry has faced numerous hurdles over the years in order to maintain its growth [2]. The first big setback occurred in the early 2000s, when the technology node was reduced to less than 90 nanometers. Heat became trapped inside the chips as a result of the fast clock speed and compact device size, eventually making them too hot to use. In order to stay up with Moore's law, the industry put a stop to clock speed increases and produced multi-core CPUs [3].

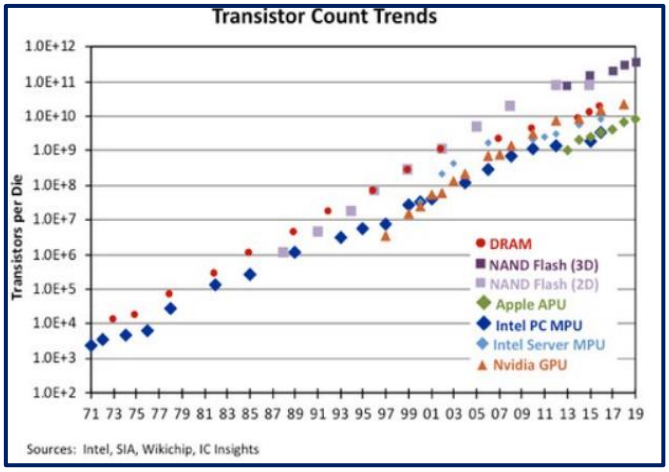

Figure 1.1. Intel's Microprocessor transistor count [4]

Short Channel Effects (SCEs) and gate leakage current resulted when the technological node and gate length and oxide thickness shrank. The semiconductor industry has come up with a variety of modifications to the fundamental Si-based MOSFET structure over the years in order to keep those non-ideal effects under check and continue scaling [5].

Another notable short channel effect is the Hot Carrier Effect, also known as Impact Ionization, in which the carrier electrons in an n-MOSFET gain much greater energy than average electrons due to enhanced lateral electric fields caused by shorter channel length [6]. Due to impact ionization, these “Hot Electrons” strike Silicon atoms and generate electron-hole pairs, resulting in a channel-to-substrate current. If the "Hot Electrons" accumulate enough energy, they may be able to break through the channel-oxide barrier and damage the gate oxide material. This phenomenon can be avoided by separating the channel from the substrate physically and using a thick high-oxide layer [7]. Some other non-ideal phenomenon linked with aggressive transistor growth is Gate Oxide Breakdown. The gate oxide thickness shrinks as the feature length of a transistor generation shrinks, making it more susceptible to electrostatic breakdown. This is a primary cause of contemporary transistor failure and a serious threat to device dependability. The use of thick high-gate oxides can help with the breakdown problem while maintaining the gate capacitance required by constant scaling [8]. Thicker gate oxides also lessen gate leakage current by reducing Quantum Mechanical tunneling at the channel-oxide contact. Intel is already deploying high-gate oxide transistors in their 45 nm and beyond technological nodes [9].

One of the most critical variables determining transistor scaling is subthreshold current. Because today's gadgets operate at such low voltages, the threshold voltage is really no higher when compared to off-voltage. Even if the V_T is low, this causes high drain current, which is one of the main causes of heating in off-state devices [10]. Subthreshold Slope (SS), which represents the voltage necessary in millivolts to lower the drain current by a factor of ten lesser than the threshold conditions (V_T), illustrates intensity of

undesired current. Traditional MOSFET structures, however, are limited to an SS of 60 m V/dec. Gate-all-round (GAA) FET and Fin FET transistor architectures with a higher degree of gate control can easily exceed the theoretical limit of SS [11].

1.2 Metal Oxide Semiconductor Field Effect Transistor

Figure 1.2 shows a MOSFET design. When it comes to VLI, researchers are constantly concentrating on reducing the transistors in order to improve their efficiency [12]. Now-a-days, the industry of semiconductors and microprocessors are progressing to the point where many nano scaled transistors may operate with low power and cheap cost designs. Scaling the device to the nanoscale scale causes problems such as SCE's, tunnelling effects, and threshold voltage effects, among others, this reduces efficiency and complicate production. This review article covers not only scaling problems and solutions, but also a deep examination of silicon nanowire and other unique nano FETs [13].

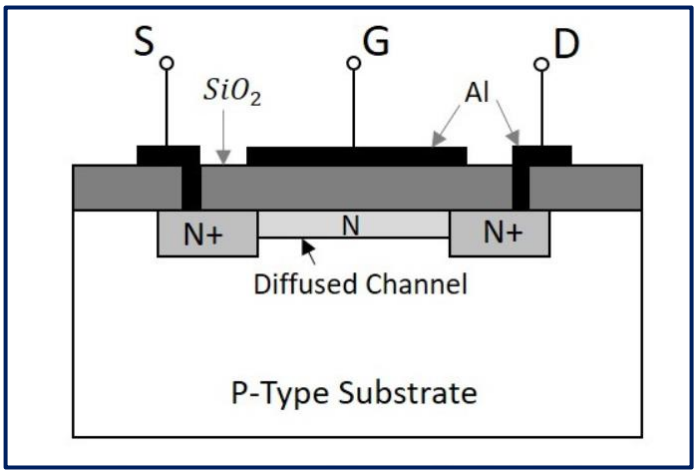

Figure 1.2. N-MOS structure [14]

1.2.1 MOSFET Operation

The MOSFET is a form of enclosed transistor manufactured by supervised oxidation, often silicon. The supplied voltage will produce charges in the metal plates of a traditional parallel plate capacitor and counter charges in the semiconductor's interfacial layer, as expected [15]. The primary capability of the MOSFET is to generate and change a conducting layer comprised of minority carriers at the semiconductor–oxide interface [16].

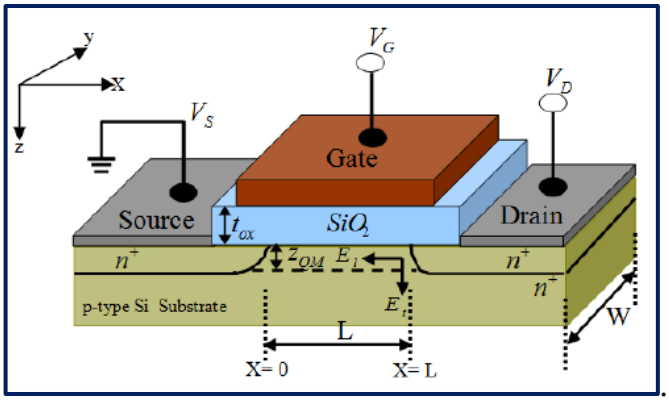

Fig 1.2.1. Quantum confinement effect shown in an n-channel MOSFET [17]

Because a p-type substrate is employed in n-MOS transistors, when $V_g>0$ is applied, holes begin to move away from the common region [18]. When the gate voltage is increased higher, the depletion layer penetrates the substrate deeper, and electrons begin to inject, producing a pathway. For an n-type substrate, the channel created by a p-MOS transistor is made up of holes. MOSFETs are classified into two categories based on how they operate [19].

1.2.2 Enhancement Mode

In Enhancement mode, in case no voltage is fed to gate electrode of MOSFET, a conducting channel does not exist between the metal regions. Switching the device ON, a particular minimum gate voltage must be applied to initiate the channel [20].

1.2.3 Depletion Mode

Even when no gate voltage is provided to a depletion-mode MOSFET, a conducting channel (inversion layer) exists. In this situation, the gadget will be turned off by the threshold voltage [21].

1.3 Downsides of Conventional MOSFETs and Their Limitations

Conventional bulk metal-on-silicon (MOS) devices are commonly used in large-scale integrated circuits. However, due to their reduced size, they are not ideal for the small-channel applications. Due to the presence of both gate-drain and gate-source overlap, the device's longitudinal field is increased [22]. The increasing number of parasitic capacitances in a device makes it unsustainable and consumes more energy. Downscaling of a device requires proper scaling of its gate length and width, thickness of oxide layer, and other dimensions [23].

1.3.1 Short Channel Effects (SCEs)

Gate electrode controls electrostatics of device's channel in long channel MOSFETs, but the source and drain regulate the electrostatics of the channel in short channel MOSFETs. Furthermore, as the size of the channel is minimized, the drain current increases, making switching easier but also lowering the threshold voltage [24].

1.3.2 Velocity Saturation

The value of the lateral electric field grows in a short channel device, resulting in charge carrier velocity saturation at around 10^7 cm/sec. As a result, the device current obtained is smaller than the drain current predicted by the mobility model [25].

1.3.3 Surface Scattering

The inversion layer formed in the device is confined to a very narrow region in the silicon near the silicon-insulator interface. Due to the increment in lateral electric field inside channel of short channel MOSFET and also the electric field applied vertically, charge carriers experience collision among them while accelerating towards the drain region causing degradation of mobility. This is known as surface scattering which lead to reduction in drain current [26].

1.3.4 Hot Carrier Effects

In short channel device, value of electric increases in the channel regions causing the carriers to move at high velocity. This acquired high kinetic energy could cause impact ionization which ultimately leads to degradation of insulator layer causing gate leakage current. These high energy charge carriers are called hot-carriers. These can also lead to undesirable substrate current [27].

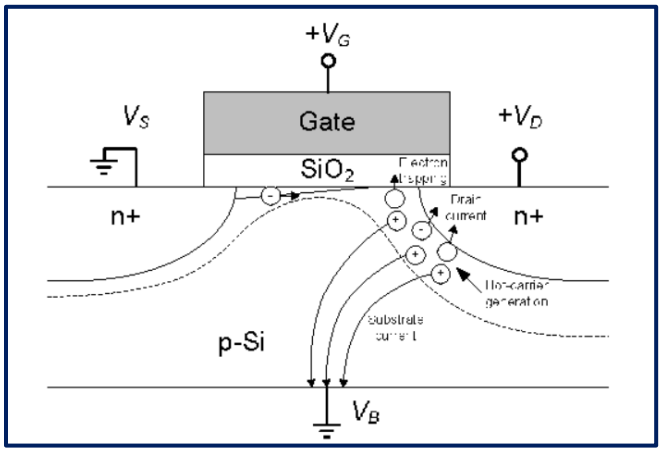

Fig. 1.3.4. Representation of Hot carrier effects [28]

1.4 Gate-all-round (GAA) FET:

The use of numerous gate transistors significantly reduces the impact of small channels and improves performance. The Nanowire itself serves as the substrate in a silicon Nanowire transistor [29]. Nanowires come in a variety of device shapes, including rectangular and cylindrical. The transistors are created as a cylindrical gate, or gate all around structures depending on the shape of the nanowires [30].

Unlike planar MOSFETs, silicon Nanowire FETs contain metal connections. That is, instead of degenerately doped semiconductors, the above-mentioned connections are constructed of metals. As a result, physical contact qualities have a significant impact on device performance. Also, annealing can result in the development of practically ohmic contacts, resulting in a substantial rise in ON current and apparent carrier mobility [31]. While the twin gate FET construction increases device performance by increasing drain current and transconductance, as well as improving short channel reliability, the misalignment of two gates might reduce device performance when compared to the single gate structure. The variation from intended behavior produced by gate misalignment might occur from either overlapped or non-overlapping regions. The symmetric dual gate structure is studied in this research [32].

1.4.1 Problems with Double Gate FET structure

While the double gate FET construction increases device performance by increasing drain current and transconductance, as well as improving short channel reliability, the misalignment of two gates might reduce device performance when compared to the single gate structure [40]. Overlapping any gate electrode with the source or drain can change the device attributes since the gate now controls the overlapped part of the source or drain. The departure from intended behavior produced by gate misalignment might occur from either overlapped or non-overlapping regions. The symmetric dual gate structure is considered in this study [33].

1.5 Literature Review

1.5.1 Biosensors

“Biosensor R&D is a widely researched discipline that has been researched because Biosensors are simple, rapid, low-cost, very sensitive, and selective, and they aid in the development of next-generation medications such as customized therapy and ultrasensitive point-of-care disease marker detection” [34]. From the perspective of smart biomaterials, this chapter reviewed traditional biosensors and biosensing techniques and emphasized current breakthroughs in essentials. Surface chemistry developments that have opened up a slew of new possibilities for creating target molecule recognition systems. Biosensor development will be accelerated and biological disciplines will be transformed as a result of the synthesis of a wide range of interdisciplinary knowledge [35].

1.5.2 For biomedical purposes, a 3D-printed device with embedded biosensors

Biosensors play an important role in every aspect lives, and their importance in making our lives easier cannot be overstated. Even the healthcare system is reliant on biosensors in this technological age. The integration of 3D printing technology with custom-made biosensors is the need of the hour. The ground-breaking technology allows for the procedure to be utilized in conjunction with MRI and CT are examples of imaging techniques scanning, allowing for a thorough examination of a patient's dataset. Biosensors are used by healthcare professionals in diagnostics, prostheses, teaching, organ transplantation, and even prevention [36].

1.6 The Rationale for Selecting Silicon Nanowire

Silicon CMOS is perhaps the nanoelectronics industry's favored technology since several decades. Due to their exceptional qualities, MOSFETs have evolved into one of the most important components of VLSI. A MOSFET's channel length is lowered during scaling down the device, deviations from long channel behavior are predicted. As a result, due to their greatly improved electrical and optical features, In the present semiconductor business, silicon nanowire transistors have gotten a lot of interest as a potential replacement for traditional MOSFETs [37].

It was reported that the carrier mobility of small-diameter SiNWs is high. The ability to fabricate high-performance FETs requires a high carrier mobility. Since SiNWs consist of high surface-to-vol. ratio, comparatively mass carriers may be easily regulated by a modest electrical field applied to the gate, these SiNWs-related nano FETs are extremely sensitive [38].

1.7 Aim & Purpose of the Study

The key goals of this project can be classified into four sections.

1. Designing the Hydrogen Passivated Gate All Around (GAA) Silicon Nanowire FET using Quantum ATK software.

2. We've used three distinct computational methods to determine the nanowire's band structure: DFT-GGA, DFT-MGGA, and the Extended Hückel technique

3. We utilized NEGF for transport of electrons and semi-empirical calculator to perform the calculations.

4. For each dielectric, subthreshold conditions such as subthreshold slope, I_{ON}, and I_{OFF} currents are investigated. Three alternative dielectrics (4,9,25) with the same channel length were compared to the calculated parameters and. In addition, a transmission spectrum without dielectric was calculated to describe electron transport at gate voltage.

CHAPTER 2

DEVICE STRUCTURE & SIMULATION IN QUANTUM ATK

CHAPTER 2: DEVICE STRUCTURE & SIMULATION IN QUANTUM ATK

2.1 QUANTUM ATK

Since 2003, professional software programmers have collaborated with academic researchers to produce Quantum ATK, an integrated set of atomic-scale modelling tools. Electronic structures can be calculated using density functional theory or Hamiltonians, bound or reactive empirical force fields in a range of parametrizations, using quantum ATK simulation engines.

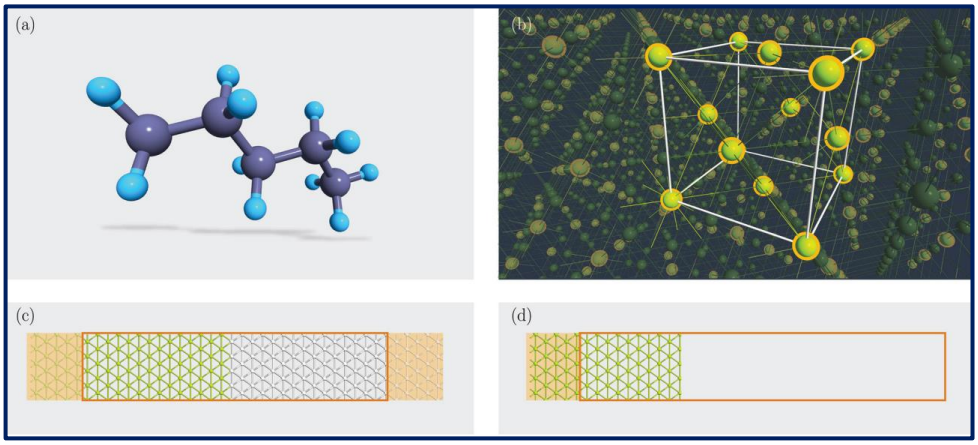

Fig 2.1. Quantum ATK accommodates atomistic configurations. (a) A pentane molecule's molecular configuration. (b) A gold crystal in its bulk structure. (c,d) A gold-silver interface device arrangement. In the left-right transport direction, both electrodes are semi-infinite [39].

In this situation, the device is periodic in both perpendicular directions to the transport direction, whereas a nanosheet or nanotube device would be the non- pierodic in one. A gold surface's surface arrangement. A left electrode (transparent yellow) and a central area make up the structure (orange box). The easy continuous integration of numerous computational in a single platform allows for the easy integration of various simulation approaches in unprogrammable processes. We give four separate application examples in addition to a basic overview and a number of implementation specifics not previously released.

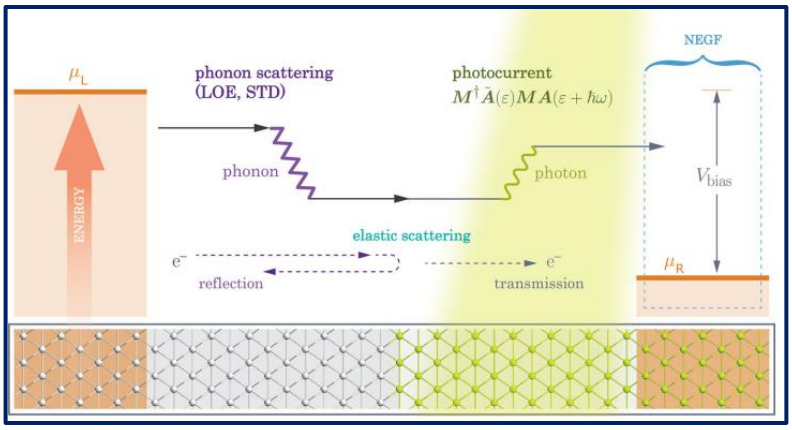

Fig. 2.2. Quantum ATK depiction of the NEGF quantum transport module [39]

Quantum ATK's distinctive feature is device system simulation. Unlike most DFT device simulation algorithms, Quantum ATK was built from the ground up to offer the maximum accuracy [40].

2.2 Simulation & Material Level Modeling

2.2.1 Building a Silicon Nanowire (111)

The first stage is to set up and optimize the Si (111) nanowire shape. For this, you should utilize the ATK-DFT calculator. We next use three distinct computational methods to determine the nanowire's band structure: DFT-GGA, DFT-MGGA, and the Extended Hückel technique [41].

- To begin, go to Add. To find the diamond phase of silicon, search the database for "silicon FCC."
- To the Stash, add the Silicon (alpha) bulk configuration.
- Take the default (111) cleave direction and click Next

Then, using the Bulk Tools Repeat, replicate the wire in the C directions eight times. Follow these steps to finish the nanowire:

Center the structure in all directions with the Coordinate Tools Center tool; and apply the hydrogen passivation to the nanowire with Coordinate Tools Custom Passivator tool.

2.2.2 Constructing the Si (111) nanowires

To compute device characteristics like ON-OFF ratio, zero-bias transmission spectrum and, after that, use the Extended Hückel model to construct the network device, combining the silicon nanowire's gate and doping [42].

2.2.3 Hydrogen Passivation

Hydrogen passivation is the process of creating hydrogen silicon bonds to protect silicon material surfaces from chemical reactions. Reactive dangling bonds on silicon atoms may be present in recently made silicon-based materials. These dangling bonds can change the material's band gap energy, influencing its semiconductor characteristics. Furthermore, air-sensitive reactive dangling bonds can be passivated with hydrogen to improve the material's stability and lifetime. Hydrogen passivation is accomplished by employing various hydrogen sources, including: Molecular H_2, Atomic H produced in plasma, Firing of hydrogenated Si nitride (SiN:H) & Hydrogen Fluoride [43].

2.2.4 Construct the SiNW GAA device

1. Build the Si (111) FET device from the bulk nanowire arrangement using Device from Bulk tool. For the electrode lengths, use the default suggestion.
2. The first stage is to set up and optimize the Si (111) nanowire shape. For this, you should utilize the ATK-DFT calculator. We next use three distinct computational methods to determine the nanowire's band structure: DFT-GGA, DFT-MGGA, and the Extended Hückel technique [44].

Next, define the metallic wrap-around gate using the Miscellaneous Spatial areas tool:

1. First, create a new metallic region with a 0 Volt value.
2. To make a cylindrical zone, go to Geometry and select Tube.

Enter the parameters indicated in the image below to define the tube's geometry. Along A and B, the cylinder will stretch to the simulation cell's edge, and along C, it will cover the majority of the nanowire's middle portion.

2.2.5 P-i-N DOPING

Finally, doping the Si (111) wire is put into the nanowire. Instead of introducing dopant atoms explicitly, which would result in a very high doping concentration for this very small device, the device is done with p-i-n junction which provides various quantities of electrons. The Fermi levels of the two electrodes will shift as a result, resulting in a built-in potential in the device [45]. Doping Type: p-type; Type of doping: n-type; Value of dopants for both left and right electrode: $4x10^{19}$ $e/cm^{3.}$ Finally, a dielectric is placed within the FET with a voltage of 1.0 V, and the dielectric constants are varied as 4,9,25 for further calculations. For these three dielectrics, simulations were done.

2.2.6. Simulations Performed in Quantum ATK

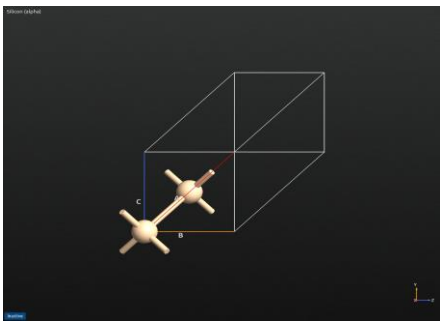

Fig. 2.3. Silicon (alpha)

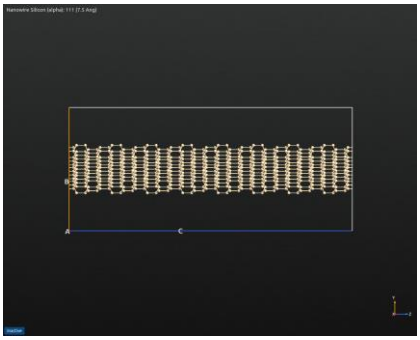

Fig. 2.4. Silicon Nanowire (111)

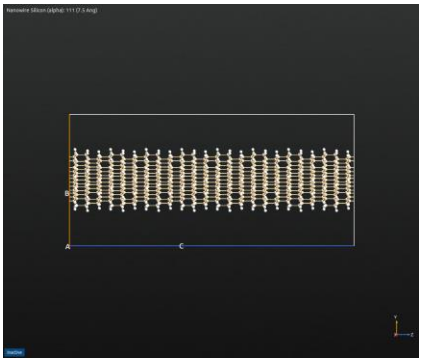

Fig. 2.5. Hydrogen Passivated Device

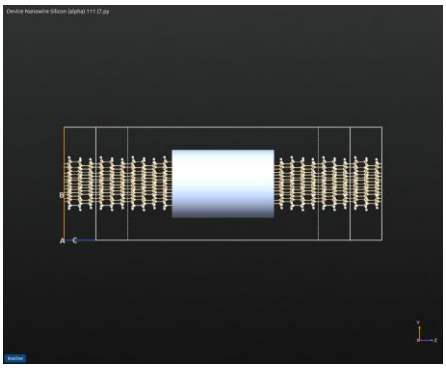

Fig. 2.6. Metallic Gate applied to the device

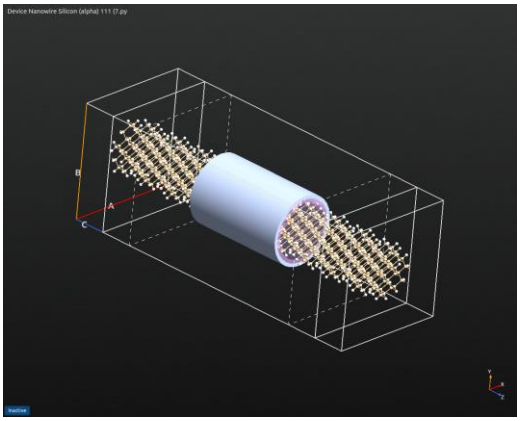

Fig. 2.7. SiNW FET with Dielectric applied

Table 1: Device's physical parameters used in the structure

Parameter	**Parameter used**			
Spatial metaheuristic parameters	**Optimizer Method**	**Force tolerance**	**The most processes possible**	**Max. force component**
	Brenner	0.05 eV/Å	10	0.035085 eV/Å
Temperature	300 K			
k-points sampling (a, b, c) for device configuration	1,1,101			
Density Mesh Cut-off	10			
Hückel-Basis set	**Atom**	**Basic type**	**Vacuum level**	
	Silicon	alpha	0 eV	
	Hydrogen	Hoffmann Hydrogen	0 eV	
Poisson solver	Boundary conditions	**A**	**B**	**C**
		Neumann	Neumann	Dirichlet

CHAPTER 3

RESULTS AND DISCUSSION

CHAPTER 3: RESULTS AND DISCUSSION

We've discussed following numerical results carried electrical characterization, by varying dielectrics I_D-V_{GS}, I_D-V_{DS}, and transmission of electrons in silicon nanowire transistors in the nanoscale range. Different values of dielectric constant are taken into account (K=4ε, 9ε,25ε) and their analog characteristics are then being compared. The Transfer (gate source) characteristics are shown in Figure 2. Once the dielectric constant shifts from one value to another, i.e., from a lower (4ε) to a higher(25ε) value, the device drive current increases.

4.1 Device Electrical Characteristics at various dielectric constants

4.1.1 Plot of the ON-OFF ratio

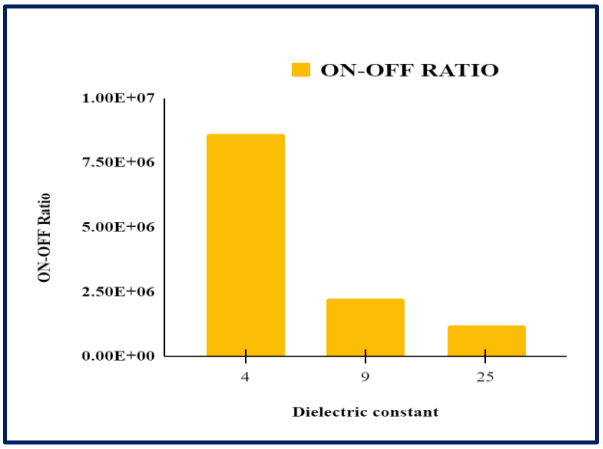

Fig. 4.1.1. The ON-OFF ratio

From Fig. 4.1.1., In terms of dielectric constant, the ON-OFF current ratio for three different dielectrics of Cylindrical Gate All Around FET based SiNW is shown in the graph above. According to the C_{ox} =

$\varepsilon_o\varepsilon_x / t_{ox}$ equation, as the dielectric constant rises, so does the value of oxide capacitance, C_{ox}, and hence the value of both ON and OFF state currents. The device's sensitivity improves as the current in the OFF-state increases. One of the most important characteristics in digital logic applications is the I_{ON}/I_{OFF} ratio. For dielectric constants 4 and 9 and 25, respectively, it was found to be 8.6×10^6, 2.25×10^6, and 1.2×10^6 in the simulation.

4.1.2 Plot of Saturation voltage

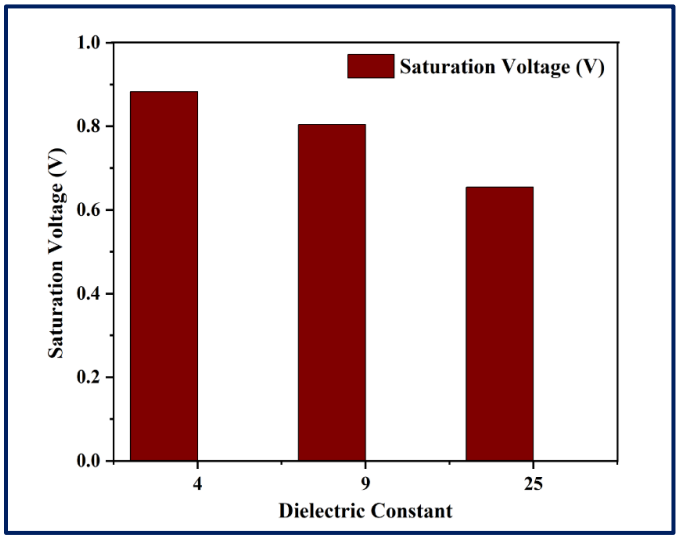

Fig. 4.1.2. Saturation Voltage at different dielectric constants

As shown in Fig. 4.1.2., The saturation voltage shifts from higher to lower values as we increase the dielectric constant. This could be explained by the presence of interface trap charges, which increases as k-values rise.

The log scale fluctuation of drain current with various source and drain doping concentrations is shown, with a fixed Drain bias of 0.5V. The barrier grows slightly higher but also thinner as the Fermi level rises, resulting in a drop in thermionic emission but an increase in drain current.

4.1.3 Plot of Subthreshold Slope

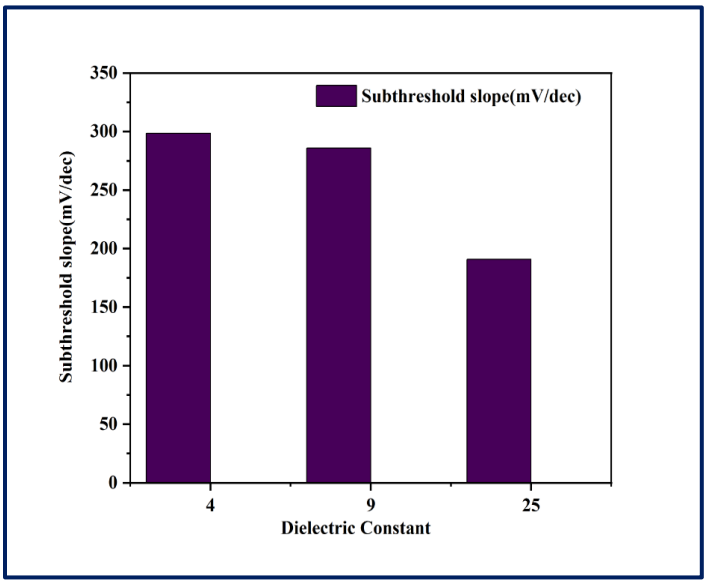

Fig. 4.1.3. Plot of SS at different dielectric constant

The major performance limiters for new devices include growing SS values due to SCEs, which must be suppressed for the device to perform better overall. From fig 4.1.3, the lower SS values also lead to better gate electrostatic control on the channel and the possibility of using a gate oxide with a high dielectric constant for digital logic switching.

Table 2: Simulation yielded device properties.

Output	**Various Dielectric constants used**		
	4	**9**	**25**
Threshold Current (A)	2.1573×10^{-10}	2.3350×10^{-10}	2.5025×10^{-10}
Saturation Voltage (V)	0.883	0.804	0.654
ON-OFF Ratio	8.60×10^{6}	2.25×10^{6}	1.20×10^{6}
Subthreshold Slope (mV/dec)	298.416	285.8914	190.766

4.2 THE TRANSMISSION SPECTRUM

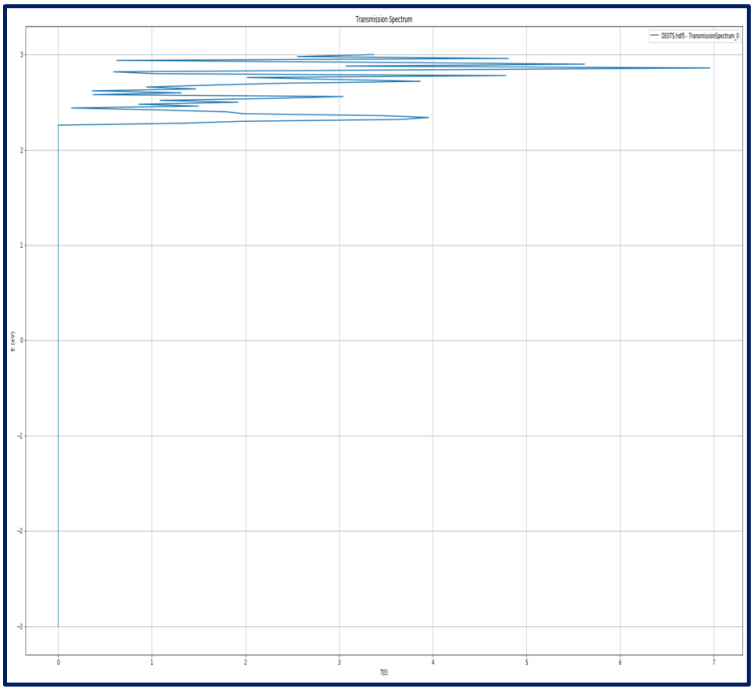

Fig. 4.2 Transmission spectrum of SiNW FET without Dielectric

From fig. 4.2, the SiNW FET transmission spectrum was estimated in addition to the I-V curves. As illustrated in Figure 1, the transmission spectra of doped and undoped FETs are similar. Undoped FETs have no gap at Fermi energy level, & spectrum intensity around the Fermi energy level is quite high. Two peaks in the conduction band can be found at 0.6 and 2.1 eV. A transmission channel is formed through the contact region when the valence bands and conduction bands of both electrodes overlap, and electrons are carried from the left to the right electrode.

CHAPTER 5

CONCLUSION

CHAPTER 5: CONCLUSIONS

In this paper, we've set up and run computations for a field effect transistor-based silicon nanowire. By defining the structure of a hydrogen passivated Si (111) nanowire and constructing a cylindrical wrap-around gate field-effect transistor (FET). Finally, we estimated the on-off ratio, Subthreshold slope, threshold voltage for three different dielectrics (4,9,25), and transmission spectrum without dielectric. The ballistic transport characteristics of the SiNW (GAA) FET are calculated using the NEGF formalism in the simulator. Electrostatics, on the other hand, is defined by solving coupled 1D Schrödinger-Poisson equations. The Quantum ATK software is totally physically precise and can be used to compute the SiNW (GAA) FET's ultimate performance limit and investigate the impacts of multiple physical parameter variations on the device's performance. Based on the results of the built silicon nanowire FET, the work compares the performance of various dielectrics. Because Nanowire FETs have a high fabrication cost, modelling their effectiveness and improving their design criteria is a smart idea. Simulation results provide insight into the behavior of existing semiconductor devices and circuits, reducing fabrication costs and reducing time to market. The study compares gate oxide performance based on performance and SCEs variables. The optimized device has a 10^7 I_{ON} - I_{OFF} ratio, an SS of 190.77mv/Dec, and a 654-mV threshold voltage. Because of the improved performance generated by utilizing dielectric 25, this device is helpful for switching and sensor applications.

CHAPTER 6

SCOPE OF WORK

CHAPTER 6: SCOPE OF WORK

Semiconductor nanowires have piqued scientists' curiosity and are thought to be one of the most promising prospects for forthcoming nanostructured materials and microchips. Applications of Silicon Nanowire FET on gas sensor can be studied using the stated software. SiNW sensors have been used to detect proteins, DNA, pH, drug discovery, glucose, arrays for parallel molecular detection, and gas sensors in experiments.

For future aspect the Quantum ATK software can also be examined for further evaluations for the SiNW FET device. Graphene sheets, carbon nano-tube can be designed for the evaluation of the devices too.

To comprehend more about the transmission spectrum and how it changes with different gate voltages. When the channel length is reduced, the electron density in the channel region increases. A transmission pathway can be presented, which is a visual representation of carrier flow through a channel constructed. Sensors FET are very useful i.e., f or instance, for sensing pollutants in our atmosphere. As a matter of fact, SiNW FET can be used for a variety of applications in our daily life.

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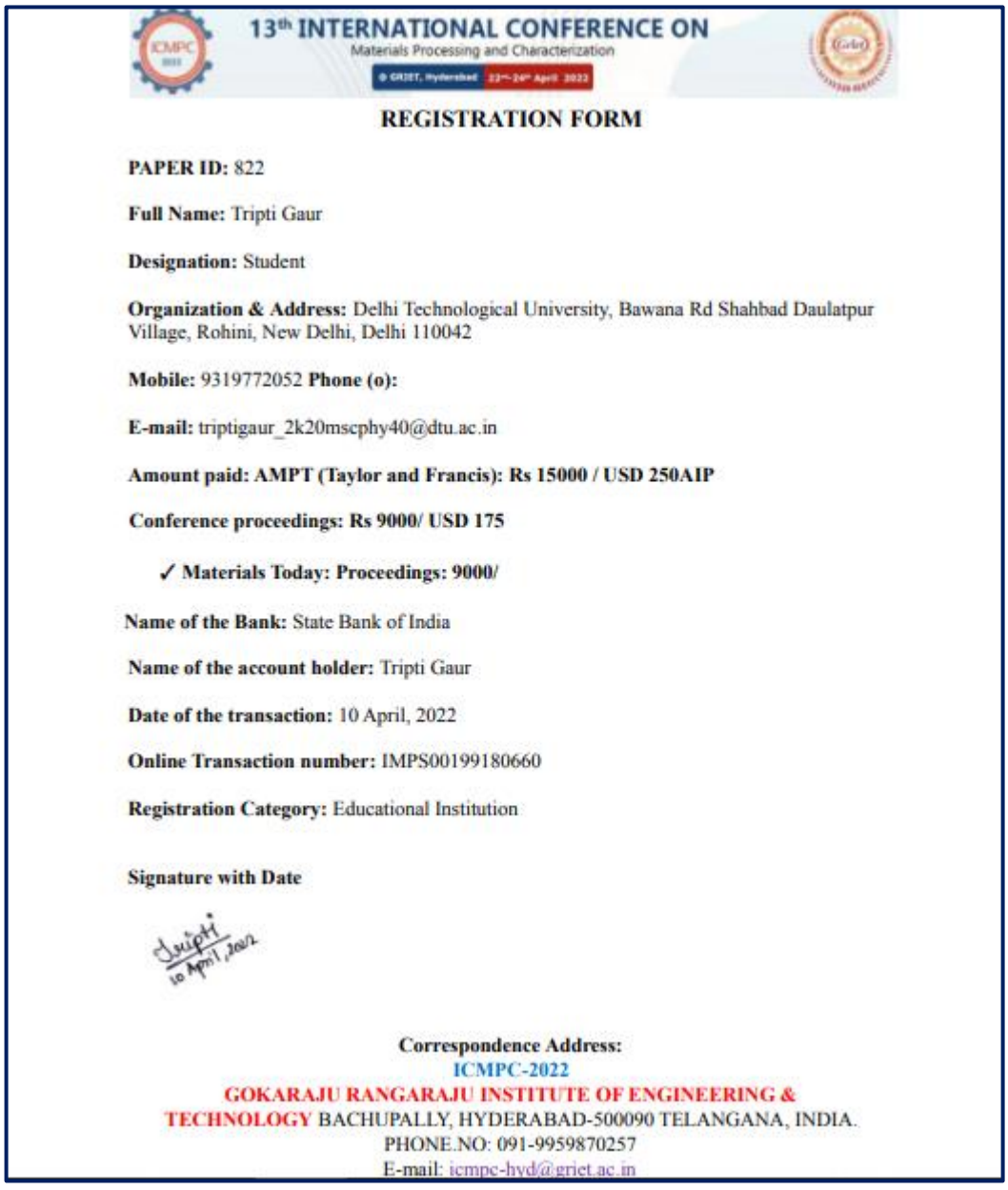

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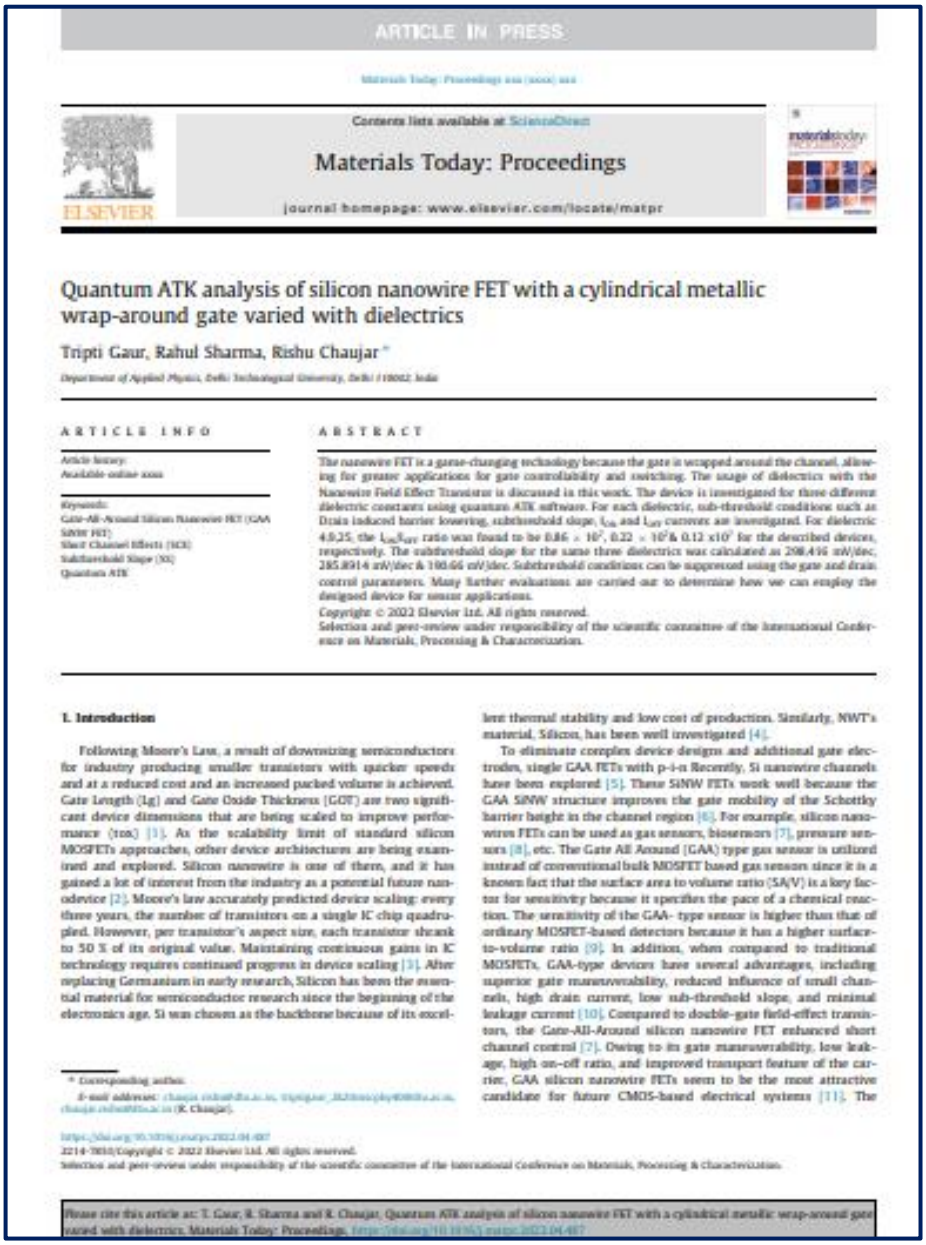

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Quantum ATK analysis of silicon nanowire FET with a cylindrical metallic wrap-around gate varied with dielectrics

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ABSTRACT

The nanowire FET is a game-changing technology because the gate is wrapped around the channel, allowing for greater applications for gate controllability and switching. The usage of dielectrics with the Nanowire Field Effect Transistors is discussed in this work. The device is investigated for three different dielectric constants using quantum ATK software. For each dielectric, sub-threshold conditions such as Drain induced barrier lowering, subthreshold slope, I_{ON} and I_{OFF} currents are investigated. For dielectric 4.0,25, the I_{ON}/I_{OFF} ratio was found to be 0.86×10^7, 0.22×10^7& 0.12×10^7 for the described devices, respectively. The subthreshold slope for the same three dielectrics was calculated as 298.496 mV/dec, 285.8914 mV/dec & 100.66 mV/dec. Subthreshold conditions can be suppressed using the gate and drain control parameters. Many further evaluations are carried out to determine how we can employ the designed device for sensor applications.

Selection and peer-review under responsibility of the scientific committee of the International Conference on Materials, Processing & Characterization.

1. Introduction

Following Moore's Law, a result of downsizing semiconductors for industry producing smaller transistors with quicker speeds and at a reduced cost and an increased packed volume is achieved. Gate Length (Lg) and Gate Oxide Thickness (GOT) are two significant device dimensions that are being scaled to improve performance (ToX) [1]. As the scalability limit of standard silicon MOSFETs approaches, other device architectures are being examined and explored. Silicon nanowire is one of them, and it has gained a lot of interest from the industry as a potential future nanodevice [2]. Moore's law accurately predicted device scaling: every three years, the number of transistors on a single IC chip quadrupled. However, per transistor's aspect size, each transistor shrank to 50 % of its original value. Maintaining continuous gains in IC technology requires continued progress in device scaling [3]. After replacing Germanium in early research, Silicon has been the essential material for semiconductor research since the beginning of the electronics age. Si was chosen as the backbone because of its excellent thermal stability and low cost of production. Similarly, NWT's material, Silicon, has been well investigated [4].

To eliminate complex device designs and additional gate electrodes, single GAA FETs with p-i-n Recently, Si nanowire channels have been explored [5]. These SiNW FETs work well because the GAA SiNW structure improves the gate mobility of the Schottky barrier height in the channel region [6]. For example, silicon nanowires FETs can be used as gas sensors, biosensors [7], pressure sensors [8], etc. The Gate All Around (GAA) type gas sensor is utilized instead of conventional bulk MOSFET based gas sensors since it is a known fact that the surface area to volume ratio (SA/V) is a key factor for sensitivity because it specifies the pace of a chemical reaction. The sensitivity of the GAA- type sensor is higher than that of ordinary MOSFET-based detectors because it has a higher surface-to-volume ratio [9]. In addition, when compared to traditional MOSFETs, GAA-type devices have several advantages, including superior gate maneuverability, reduced influence of small channels, high drain current, low sub-threshold slope, and minimal leakage current [10]. Compared to double-gate field-effect transistors, the Gate-All-Around silicon nanowire FET enhanced short channel control [7]. Owing to its gate maneuverability, low leakage, high on–off ratio, and improved transport feature of the carrier, GAA silicon nanowire FETs seem to be the most attractive candidate for future CMOS-based electrical systems [11]. The

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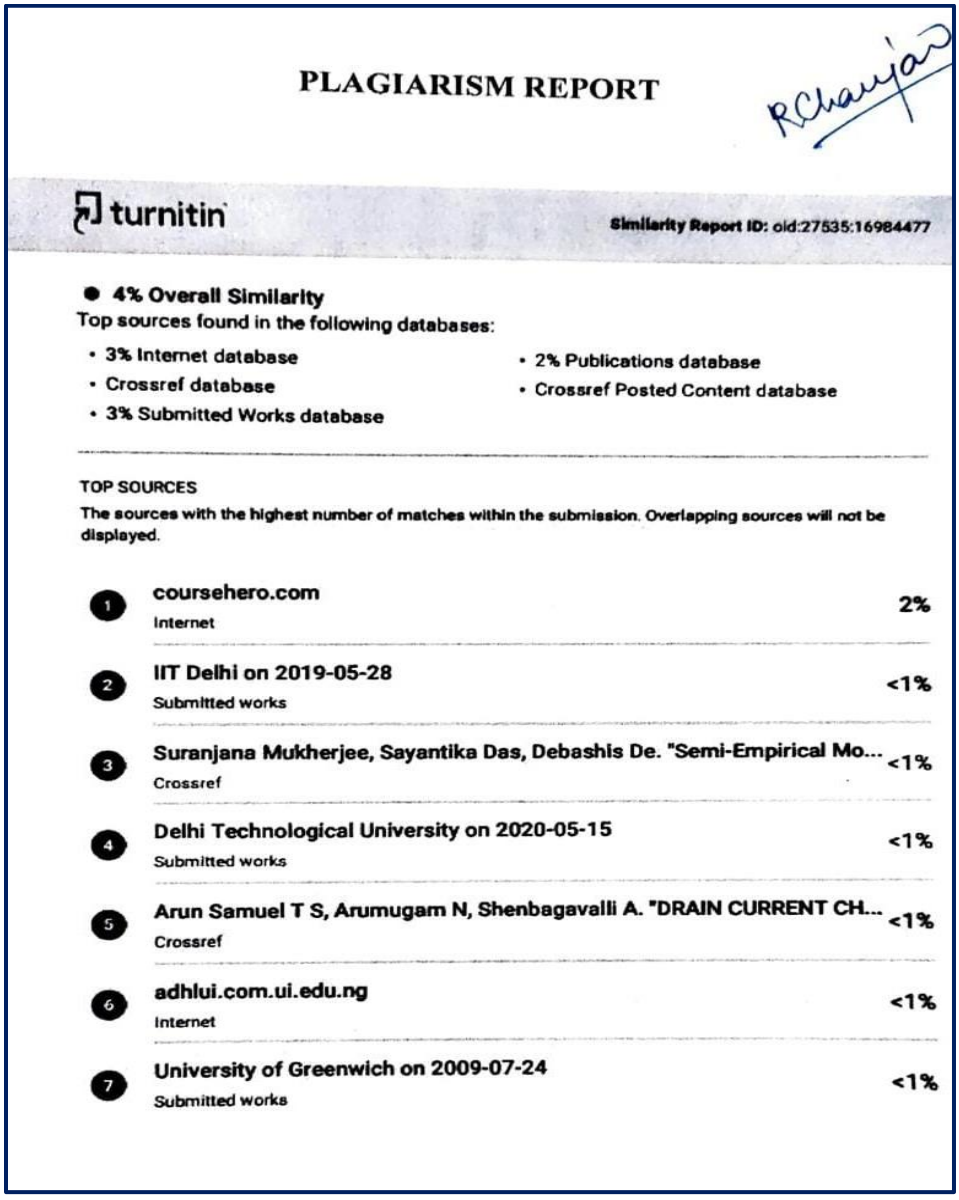

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