**Thesis**

on

# Study and Modeling of Single and Multi Layer Graphene Field Effect Transistor Structures with Various Dielectric

submitted in the partial fulfilment of the requirements for the Degree of

**DOCTOR OF PHILOSOPHY**

by


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# CERTIFICATE

This is to certify that the work which is being presented in this thesis **"Study and Modeling of Single and Multi Layer Graphene Field Effect Transistor Structures with Various Dielectric"**, in partial fulfilment of the requirement for the Doctor of Philosophy in the Department of Electronics and Communication Engineering at Delhi Technological University, Delhi is an authentic record of my own work carried under the supervision of Dr. Deva Nand, Assistant Professor, Department of Electronics and Communication Engineering, Delhi Technological University. The matter presented in this research plan has not been submitted by me for the award of any other degree of this or any other Institute/University. If there is any copyright with this matter, then I will be responsible for any legal dispute.

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Roll no. 2K17/Ph.D./EC/03

This is to certify that the above statement made by the candidate is correct and true to the best of my knowledge and belief.

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## List of abbreviations used

**Gr-**Graphene

**hBN-**hexagonal boron nitride

**2D-**Two dimensional

**nm-**Nanometer

**GFETs**–Graphene field effect transistors

**QC**- Quantum capacitance

**MFT**-McKelvey's flux theory

**CMOS**-Complementary Metal Oxide Semiconductor

**HDs**-harmonic distortions

**IMs-**Intermodulation distortions

**NEMS**-Nano Electronics Mechanical System

**MEMS**-Micro Electronics Mechanical System

# LIST OF PUBLICATIONS

**Journals**

**Published**

1. Munindra, Deva Nand, "Nonlinearity, Scaling Trends of Quasi-Ballistic Graphene Field Effect Transistors Targeting RF Applications" Journal of Computational Electronics, vol. 20, pp. 2379- 2386, 2021. https://doi.org/10.1007/s10825-021-01772-x (SCIE) Impact factor 1.730.
2. Munindra, Deva Nand, "Nonlinearity Analysis of Quantum Capacitance and its Effect on Nano- Graphene Field Effect Transistor characteristics" Journal of Electronic Materials, vol. 51, issue 7, 2022. htt[s://doi.org/10.1007/s11664-002-09639-y, (SCI & SCIE), Impact factor 1.746.
3. Munindra, Deva Nand, "Study of Electronic Properties of Single and Few Layer Graphene gr/hBN Heterostructure" IJRECE, vol. 7, issue no. 2, pp. 1515-1554, 2019. (Scopus).

**Conferences:**

1. Munindra, Deva Nand, "Non-linearity of the Single Layer Graphene Field Effect Transistors" an oral contribution in11th International Conference on RECENT PROGRESS IN GRAPHENE AND TWO-DIMENSIONAL MATERIALS RESEARCH CONFERENCE (RPGR-2019), 2019, Matsue, JAPAN.
2. Munindra, Deva Nand, "Study of Non-linearity of Bilayer Graphene Field Effect Transistors" an oral contribution in IEEE 14th International Conference on Nanotechnology Materials and Devices Conference (IEEE-NMDC-2019), 2019, Stockholm, SWEDEN.
3. Munindra, Deva Nand, A.K. Upadhaya, "Evaluation of Graphene FET Model in Quasi-Ballistic Regime for Frequency Doubler Circuit" a poster contribution 5th International

Conference on Emerging Electronics (ICEE-2020), 2020, IIT-Delhi.

4. Munindra, Om Prakash Verma, “Analysis of Quantum Capacitance Effect and Velocity Saturation in Graphene- Metal-Oxide-Semiconductor Field Effect Transistor with Large Area Graphene Channels” an oral contribution in 10th International Conference on RECENT PROGRESS IN GRAPHENE AND TWO-DIMENSIONAL MATERIALS RESEARCH CONFERENCE (RPGR-2018), October 22-25, 2018 in Guilin (China).

# Chapter one

# Introduction and Motivation

## 1.1 INTRODUCTION

A transistor is the most important component of computer and electronic devices, which is facing the problem of performance limitations of conventional Integrated circuits, as it is the biggest challenge for the electronics, semiconductor industry and information technology. The reduction of dimensions in silicon-based transistors faces great challenges as dimensions approach atomic sizes and physical limits will be eventually reached. A great deal of research has been centred on new 2-D material graphene that can overcome these limitations. Thus, to make our computers smart and fast we have to replace the silicon material with graphene, it has enormous electrical conductivity and many research's almost in every space of life has proved graphene as the material of the future. The Discovery of graphene raises the prospect of a new class of nanoelectronics devices based on the extraordinary physical properties of this one-atom-thick layer of carbon. Unlike other two-dimensional electron layers in semiconductors, where the charge carriers become immobile at low densities, the carrier mobility in graphene can remain high, even when their density vanishes at the Dirac point.

The high electron mobility of graphene (200000 $cm^2V^{-1}S^{-1}$) [1] makes graphene-based field effect transistors (GFETs) excellent candidates for replacing silicon-based nanometer Complementary Metal Oxide Semiconductor (CMOS). High transconductance gain ($g_m$) and saturation region for GFETs drain current facilitates the use of GFETs as a voltage-controlled current source and the design of analog circuits. Until now, drain current saturation has been observed in long gate GFET devices, but now short gate also presents unsatisfying current saturation behavior, Bilayer graphene comes out as an alternate and improves the current

saturation behavior for GFET Devices. Lateral graphene heterostructure is another solution for current saturation improvement for high-frequency GFETs. Some of the physical models have been developed by the researcher, which does not have closed expressions and so need numerical methods and expressions which avail us of simple mathematical models for different parameters for GFETs. Since Graphene is a miracle material which has extraordinary properties: like high mobility, very high thermal conductivity, optically transparent, and stability at the atomic level. It is the two-dimensional single atomic layer of 0.342 nm thickness. It is stronger than steel and even lighter in weight. This material is of importance and interest that a European organization named graphene flagship is fabricating and integrating ICs at the industrial level named by 2D-Experimental Plot line (EPL). Figure 1.1 graphene electronics product from the fabrication lab to market MGFET-4D, MGFET-4P, and GFET-S20 chip from Graphenea. GFET-S20 contains 36 GFETs applicable for sensing applications.

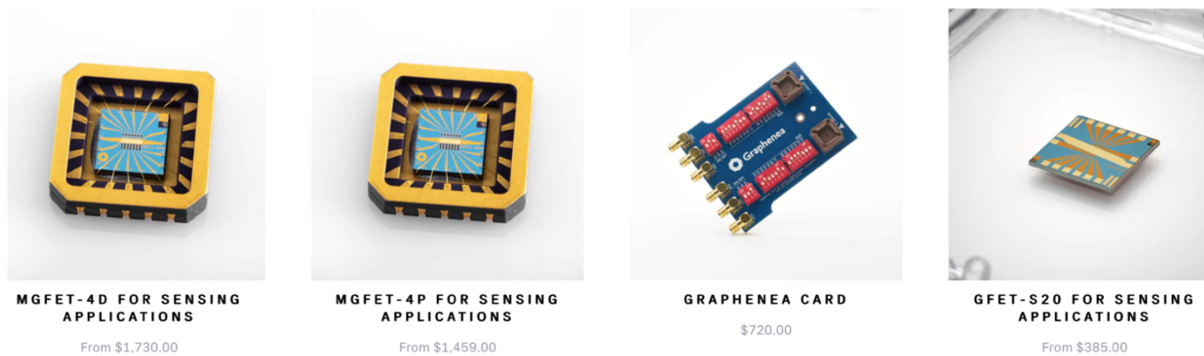



Figure 1.1 The MGFET-4D, MGFET-4P GFET-S20, chip from Graphenea provides 36 graphene devices distributed in four quadrants with the devices in the centre of the chip and the probe pads located near the periphery of the chip [65].

### 1.2 Motivation Graphene Flagship

Graphene flagship is the world's biggest platform for graphene and 2D materials research, innovation, production, industrialization and collaboration. The Graphene Flagship was launched in 2013 by the European Commission with a budget of one billion Euros. Graphene flagship is the collaboration of 22 countries, 167 Core partners, 1200 members and 100 associate members. Funded by the European Commission graphene flagship is the home for

the 19 research centres including industry (48%), Academia (34%) with 4500 publications and 333 patents. For the innovation, the graphene flagship is associated with the 11 spearhead projects of 16 companies. In 2022 graphene flagship starts its 2D materials Semiconductor foundry named by 2D-Experimental Plot line (EPL). Figure 1.2 Plan of action for the year 2022 and functional summary of development in the year 2022. Figure 1.3 Extraordinary properties of graphene towards its electronic applications with wafer-scale integration [2].

Figure 1.2 Plan of action for 2022 and functional summary of development in 2021Of Graphene Flagship [2].

### 1.3 LIMITLESS POSSIBILITIES OF THE LIMITLESS LAYERS OF GRAPHENE AND GRAPHENE COMPOSITE

The birth of limitless layers in 2004 is the outcome of years of research by the chunk of graphite and sticky tape. Now just 17 years later we have a vast family of layered materials and vast

opportunities for solo layered materials or the composite of the layer materials. Graphene is a single atomic thin/thick layer of carbon atom in a hexagonal structure with extraordinary thermal and electrical conductivity, stronger than steel and harder than diamond even though highly flexible. Graphene layers with twisted orientation are highly researchable layered materials of semiconductor industries and digital device applications. Graphene composite is highly recommended in electronic industries for RF electronic applications and its spintronic applications. Graphene composite with lithium is highly recommended for optoelectronics applications and photovoltaic industries' solar panels. Graphene's extraordinary thermal conductivity found its application in electro mechanics, microelectronic mechanical systems (MEMS) and nanoelectronics mechanical systems (NEMS). Graphene is also versatile in aviation and automation industries, many of them foundries like Lufthansa and Mercedes are aiming for a fully automotive battery module. Graphene heterostructure and twistronics are also two new filed to understand the behaviour of layered materials. A small angle twist in the two-graphene layer stack could change electrical conductivity unimaginably from superconductive to insulator. Wearable and communicable electronic device applications are also aiming the high flexibility just because of graphene properties. The extremely thin layer of graphene could also pave the way for the printable, wearable and flexible internet of things (IoT) ideals. Graphene and layered materials are also promising to design and develop sensor and sensor-based products for biomedical, health and safe environments for the habitat in an urban area. Graphene technology like compact $NO_2$ is efficient to clean and save urban city air with help of graphene photocatalyst. Pure water is the best and primary food integrant for human health graphene is also helpful to produce compact and cost-effective water filters. The strong spin-orbit coupling and magnetic properties of graphene are encouraging for spintronic devices. The theoretical investigation of graphene spin devices has extended the conventional approach of quantum simulation by developing brute force for making the simulation realistic. The experimental study of graphene heterostructure, and encapsulation of graphene layer into

two 2D materials layers demonstrate the charge particle interaction swapped by gate potential and exchange of spin-orbit coupling. Self-lubricating property of graphene-metal composites could replace the lubricating grease in the low-voltage circuit breakers. The grease-free and maintenance-free low circuit voltage breakers could be monumental as well as sustainable for fault detection in electrical grids. The self-lubricating technology of graphene composite is developed at graphene flagship initially for electrical contacts and now is scaled up for the circuit breaker application. Thin film technology perovskite would have increased the power efficiency of solar panels with reduced the cost since silicon solar cells have reached their theoretical upper power conversion efficiency. The estimated cost of solar power based on thin film perovskite is $0.3 per watt with 25% power conversion efficiency. Graphene flagship's GRAPES project aims to revolutionize the Photovoltaic industries as it combines two different technology new thin-film perovskite solar cells and silicon tandem cells on graphene and layered materials. GRAPES project is aiming to design, fabricate characterize and install 20 $m^2$ solar panels with 23 % power conversion by 2023 [2].

Graphene transducer-enabled image sensor-based broadband super pixel camera would be capable to detect visible infra-red rays ranges (400 nm to 700nm wavelength corresponds to 450 THz to 750 THz) using a single focal plane array [2]. The broadband camera would have a resolution of 80 x 60 super pixels. The graphene flagship project used three different materials with a graphene transducer (colloidal quantum dots, pyroelectric thin film and nanoparticle oxides with narrow band gap) to a developed absorber material solution to read full spectral visible infra-red band. The functionality of this camera is tested successfully at CMOS wafer integrated with graphene patterns named readout integrated circuit (ROIC) for its first version 80 x 60 super pixel. This ROIC makes it possible to integrate graphene and photosensitive materials. The fabrication of silicon/graphene composite electrodes in lithium-ion batteries used as anode has been done in 2020 through the GrEEnBat project. The advantage of silicon/graphene electrode is increased cyclability of the batteries by 60% along with the

efficient energy density of silicon batteries [2]. Graphene flagship aims to develop a fully functional silicon/graphene battery module for an automotive application like an electric car by the end of the year 2025. The ultimate goal of sustainable development will be fulfilled by using green technology lithium-ion battery material which helps us to reduce the release of greenhouse gases. The high electrothermal conductivity property of graphene helps GICE teams to characterize and develop the graphene heater element to resolve the ice accumulation on aeroplane wings, rudders and propellers. Ice accumulation on aircraft surfaces is very dangerous and could be solved by graphene's lightweight, highly efficient, and flexible properties. GICE project team hosted by graphene flagship has developed the Ice detector and also tested it in laboratories. Lufthansa technique and graphene also host an AEROGraFT project, which is aiming to produce and replace aircraft state of art HEPA filters with graphene-based self-clean filters.

### 1.4 Graphene Electronics and its wafer-scale integration

The extraordinary electrical conductivity of the graphene layer is highly versatile in the electronics world and its wafer scale integration is highly motivational for the limited silicon electronics industry. Extremely flexible, super thin, supper conductive and sustainable development supportive properties of graphene prove it ideal layer material for RF electronics.

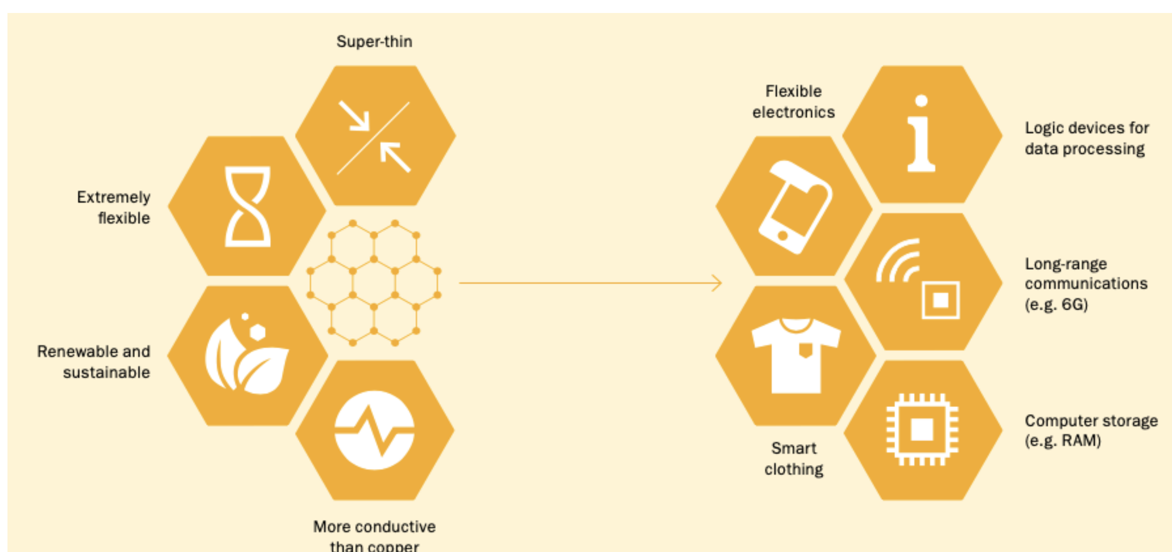



Figure 1.3 Extraordinary properties of graphene towards its electronic applications with wafer-scale integration [2].

## 1.5 RESEARCH OBJECTIVES AND FINDINGS OF THE THESIS

### 1.5.1 To explore and implement a closed form model of GFET, using effective mobility.

- A quasi-analytic model for single-layer GFETs with large area graphene is presented. Drain current formulation with velocity saturation effect and role of quantum capacitance over the total capacitance is explained with the precise output and transfer characteristics of the proposed GFET model.
- The effect of enhanced quantum capacitance value at nanometre technology adds nonlinearity to the transfer and output drain characteristics of the proposed GFETs model.
- The fitting parameter addition in velocity saturation has improved the drain current characteristic by avoiding the early saturation stage. Modelling and simulation of the GFETs model have provided a high drain current when compared with the results of the well-established experimental work.
- Dual gate control along with the nonlinearity study of single-layer large area graphene field effect transistor is done.

### 1.5.2 To study and formulate the non-linearity and linearity characteristic behaviour of the quasi-ballistic GFETs model.

- An explicit nonlinearity characteristic behaviour of the ballistic transport approach GFET presented in this work has significant importance Since the nonlinearity of the particular devices is a great source of noise in the nanoelectronics device application based on GFETs.
- This work is a Comparison of GFETs at various scaling channel lengths for the proposed model and simulation results with better drain current values. Better drain current at nanometre technology is a big achievement of this modelling and simulation work.

- The higher frequency response of the GFETs model in comparison to conventional MOSFETs technology at the same channel length is the paramount potential of this work.
- The explicit quantum capacitance drives the drain current formulation and also presents the nonlinearity of characteristic curves of the GFETs at nanometre technology. Since noise is always a key element to disturb the performance of the FETs and GFETs in real-world electronic devices and circuits, the study of nonlinearity to the transfer as well as output characteristics is our contribution to the modelling and simulation of the quasi-ballistic GFETs.

**1.5.3** To drive and formulate scalable closed form quasi-ballistic GFETs model.

- TCAD simulation setup and device structure setup of ballistic and quasi-ballistic GFETs at four different channel lengths (140, 240, 300 and 1000 nm) are done from quasi-ballistic to ballistic transport nature of charge carrier in graphene channel.
- The entire simulation process is done in four independent steps device structure for 1000nm, 300nm 240nm and 140nm, which follows similar basic device structure formation fundamentals like all of them are four terminal devices. 500nm thick silicon base with 22nm/10nm back gate contact, 285nm (300-15) thick back gate oxide hBN, atomically thick single-layer graphene, 15nm thick top gate oxide hBN and the source, drain and gate contacts similar to the back-gate thickness. Graphene has been modified with the established poly-silicon properties like electron mobility MUN, hole mobility MUP, energy band gap EG at room temperature and work function.

**1.5.4** To explore and simulate the electronic properties of graphene on various 2D dielectric beds.

- The electronic properties of single layer and bilayer graphene, along with graphene over the hBN layer (gr/hBN heterostructure) are studied and well demonstrated.
- The electronic band diagram, current density and charge carrier density concerning the thickness of graphene layer over gr/hBN heterostructure have been find.
- An energy band gap widening is observed from the single and bilayer graphene encapsulated in the hBN dielectric sheet.

### 1.5.5 Scope and applications of this thesis work

- RF frequency response of this work is very much comparable to the graphene FET RF mixer and subharmonic mixer, high voltage gain Amplifier, and frequency doubler circuits.
- Modelling and simulation done for the nonlinearity of single layer large area GFET and quasi-ballistic GFET are very much applicable for the quantum computation of the RF electronics circuits based on these devices.
- Modelling and simulation done for the nonlinearity of single layer large area GFET and quasi-ballistic GFET are very much applicable for the VLSI and circuit design module for the latest nanoelectronics applications.
- Modelling and simulation of the devices we have modelled can be modelled on various CAD tools COGENDA TCAD, SILVACO and SENTAURUS TCAD, and COMSOL.
- The GFETs model we have studied is technically similar to the GFETs used in the GFET-S20, MGFET-4D, and MGFET-4P graphene chips available in the market for sensing applications.

# Chapter two

# Literature survey

## 2.1 INTRODUCTION

The transistors of the recent internet of things amenities like mobile, computers and laptops are 5nm across (M2 chip of MacBook air 2021). The atomic size of silicon is 0.21nm, which means 24 to 25 atoms are present in today's transistors. This simply indicates the atomistic limitations of the silicon transistors. Silicon technology advancement in future years in table 2.1 is compared by the semiconductor foundries with different technologies. The advancement of silicon transistors beyond 1nm is not possible even after 2026 because of short channel effects at 1nm or 10Aungstrom and if possible, only and only in industry and academic partnerships. Academics always suggest 2D material graphene as a semimetal for electronics applications. Table 2.2 Comparison of the physical parameter of these transistors by ITRS.

Table 2.1 Comparison of recent transistor technology by fabricating semiconductor foundries.

| Name\Years | 2018 | 2019 | 2020 | 2021 | 2022 | 2023 | 2024 | 2025 |
|---|---|---|---|---|---|---|---|---|
| TSMC | 7nm | | 5nm | 5nm | 3nm FinFET | 3nm+ FinFET | | 2nm GAA |
| SAMSUNG | 8nm | | 5nm | | 3nm GAA | 3nm+ GAA | | 2nm |
| INTEL | | 10nm | | 7nm | 4nm | 3nm | 20A | 18A |

Based on the official data published by INTEL, SAMSUNG AND TSMC [102-104]

Table 2.2 ITRS-International Roadmap for Semiconductor devices trends for MOS devices

| **Year** | **2009** | **2012** | **2015** | **2018** | **2021** |
|---|---|---|---|---|---|
| physical size length (nm) | 34 | 24 | 17 | 12 | 8.4 |
| MPU physical gate length (nm) (Lg) | 20 | 14 | 10 | 7 | 5 |
| Supply voltage $V_{dd}$ (V) | 1.0 | 0.9 | 0.8 | 0.7 | 0.65 |
| Number of transistors per chip (Millions) | 878 | 1106 | 2212 | 4424 | 8848 |
| Oxide thickness (nm) (0.02Lg) | 1.4 | 1.3 | 0.9 | 0.64 | 0.44 |
| Max power dissipation with heat sink(W) | 180 | 190 | 218 | 215 | 288 |

## 2.2 LITERATURE SURVEY

### 2.2.1 RISE OF GRAPHENE

The rise of graphene presents the electric field behaviour of a few atomically thick or thin carbon layers. Heart of the modern world electronics is all about a particular material's behaviour in the presence of another's electric field and so, we called it as electric field effect. since the semiconductor world is just reached the limits of performance improvement and scaling of parameters for the conventional silicon technology, so after the researcher's hard work and continuous efforts. we land with organic conductors and carbon nanotubes at the same time electronics are also being exposed to the transition metal, and tend to use it for all-metallic transistors, for very long. however electronic field screening through metal is only less than one nm (<1nm) so, this article reports a mechanical exfoliation produced monocrystalline graphite films, which was just a few atomic thick and even under some ambient condition thermally stable. Figure 2.1 Graphene the mother of all carbon forms graphite, graphene is a fundamental 2D building material for all (0D, 1D,3D) dimensions carbon 0D Buckyballs, 1D nanotube and 3D graphite stack [3].

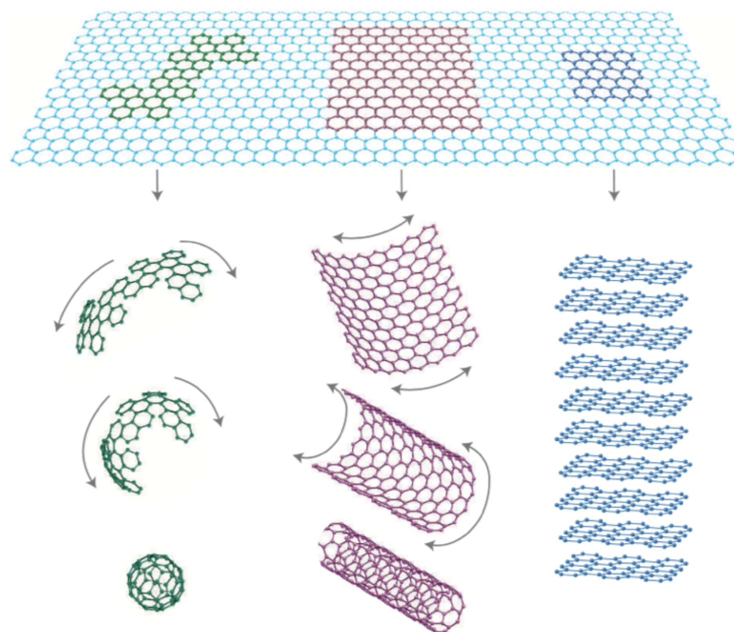


Figure 2.1 Graphene the mother of all carbon forms graphite, graphene is a fundamental 2D building material for all (0D, 1D,3D) dimensions carbon 0D Buckyballs, 1D nanotube and 3D graphite stack [3].

This report presents the electric field effect in a naturally exfoliated occurring few layers of graphene [1-2], as the first novel 2D material. Before this, it was unbelievable that planner graphene (carbon form) could be found in the free form at the nanometer (atomic) level. Above all these myths and beliefs they have been done this and able to produce a graphene sheet of one atomic thick, even developed electronic devices based on this and study their electronic properties. This graphene sheet shows superb high-quality 2D electronic ballistic transport at submicron lengths. This is highly remarkable to get such an efficient conducting atomically thick semi-metallic layer. A metallic field effect transistor has been prepared by using the conducting channel as 2D electron gas and hole gases switched by the voltage tuning. To explore more about the electronic properties of these mechanically exfoliated (from highly oriented pyrolytic graphite) sheets from a single layer (SLG) to few-layer graphene (FLG) ranges from less than one nm to hundreds of nm respectively, has been processed in multi-terminal Hall bar devices and put on top of oxidized Si at the base so that gate can be controlled by applying gate voltage (Vg). All the FLG (1, 2, 3 layers) devices exhibited identical electronic properties for 2D semimetal, unlike the multilayer graphene to the properties of 3D graphite.

### 2.2.2 LIMITATIONS OF GFET STRUCTURE TOWARDS DEVICE LOGICS, WHILE HAVING SCOPE FOR HIGH FREQUENCY TRANSISTORS

The absence of bandgap in pure graphene Flack is the main concern of graphene-based device logic application, which also limits its scope in digital electronics [4-6]. So, it is unlikely to see that graphene will be able to make it into high–performance ICs for logic application as a planer channel 2D material. However, the CVD-grown graphene layer and graphene growth over SiC could be a possible option for high-frequency and analog electronic devices and circuits [5].

### 2.2.3 GRAPHENE ELECTRONIC PROPERTIES AND ITS LIMIT ON THE $SiO_2$ PLATFORM

The intrinsic and extrinsic performance limits and expectations of graphene on $SiO_2$ devices have been shown by numerous articles. An unexpected/surprising prediction has been come out with the fact of linear dispersion relation in wave vector k and 2D energy, is that we may have resistivity (due to isotropic scattered-phonons) independent of charge density n. This has been predicted and lightens up [7] that the acoustic phonon scattering and an intrinsic limit of 30 Ω resistivity in graphene, which is also found independent of n, at room temperature. With the technology relevancy fit carrier density is $10^{12}$ $cm^{-2}$, very high intrinsic carrier mobility 2 x $10^5$ $cm^2/Vs$ [5-6] (which is more than ever known inorganic semiconductor as InSb of value approx. 7.7 x $10^4$ $cm^2/Vs$, CNTs of value approx. 1 x $10^5$ $cm^2/Vs$) and electron acoustically scattered mean free path is > 2μm.

While the extrinsic scattering due to surface phonons of the $SiO_2$ substrate shows resistivity strongly dependent on temperature above ~ 200K and it limits the mobility value to 4 x $10^4$ $cm^2/Vs$ approx. at room temperature. So, to develop quality graphene-based electronics, a quality graphene sample is not enough one also needs a surface scattering and roughness-free, impurity-free and surface optical-free substrate for the graphene layer [7]. Furthermore, near charge neutrality and substrate-induced disorder creates inhomogeneous patterns of electron and hole puddles. Because of these many surface interface problems of graphene with the substrate, it exhibited characteristics far inferior to the expected intrinsic properties. A novel approach for substrate engineering is developed is graphene-based vertical heterostructures [9]. Figure 2.2 Energy momentum graph shows six contact points of valance and conduction band called Dirac point.

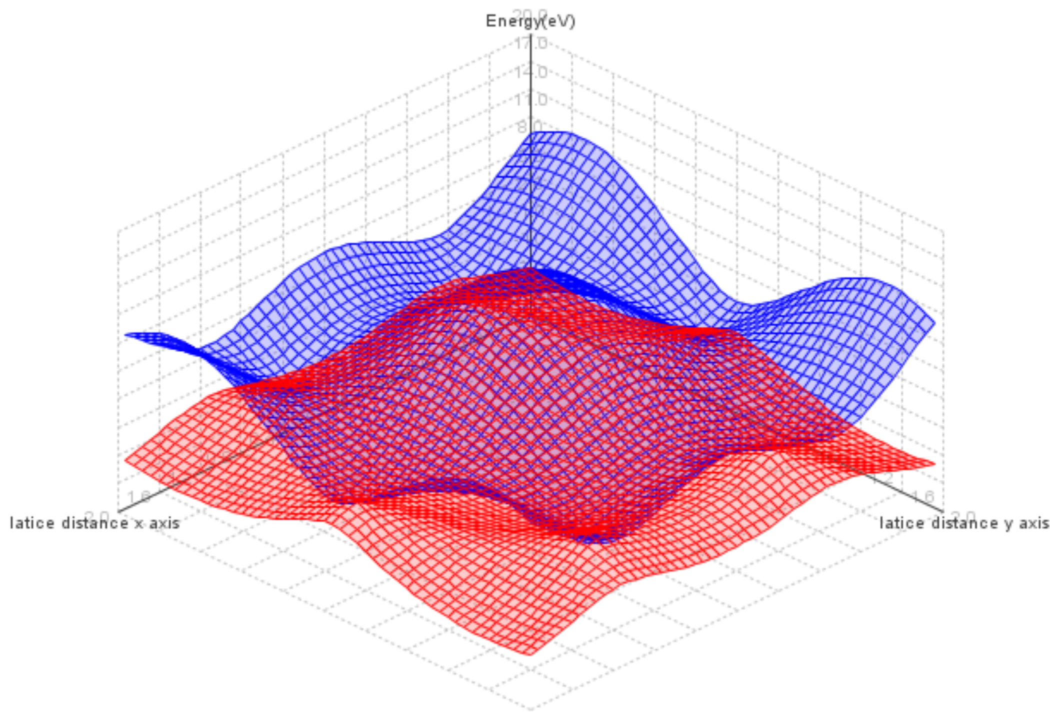



Figure 2.2 Energy momentum graph shows six contact points of valance and conduction band called Dirac point.

Graphene-based FETs on conventional oxide ($SiO_2$) beds show highly disordered and degraded properties that are very menial as compared to the pristine graphene layer [8]. Although GFETs electronics quality is being upgraded by suspending the graphene channel on the above substrate and by hydrogenating the graphene channel to the nanopore and nanomesh FETs. These geometry arrangements have also imposed limitations on device architecture and functionality. So, the very needed and technology-matched 2D dielectric material Hexagonal boron nitride (hBN) [6-8] is an appealing substrate to the GFETs. It has an atomic size dangling bond-free smooth surface and has a must-needed bandgap (5.97) [10] along with large enough surface optical phonon modes. Graphene and the graphene-based device show appealing high-frequency gain and other characteristics for RF and analog circuits design [11].

### 2.3 PREPARATION METHODS AND SPECIFIC PROPERTIES OF GRAPHENE AND OTHER 2D MATERIALS

First and foremost, the preparation method by the birth of graphene in Manchester university 2004 is the scotch tape method. The impossible task of isolation of single-layer graphene ever is done and the finding of electric field effect in the graphene layer bless K.S. Novoselov and A.K. Geim sir with the noble prize in 2010. Scotch tape method or mechanical exfoliation of graphene was initially very promising with exceptional electronic property for graphene electronic applications but after researching a decade liquid phase exfoliation (or chemical exfoliation), graphene production on SiC and CVD growth of graphene are providing highly productive graphene layer. The separation of graphite crystal using the surface tension of non-aqueous liquid into graphene platelets or we can say graphene sheets is liquid phase exfoliation. Liquid phase or chemical exfoliation also uses graphene oxide by oxidizing the graphite crystal to produce very low conductive graphene for battery electrodes to develop fully automobile applications. CVD-grown graphene or graphene transferred on dielectric layers like hBN and $HfO_2$ is the best production method of graphene, this method leads to provide the intrinsic mobility of the graphene layer.

Table 2.3| Summary of properties of application-specific graphene prepared by different Methodology

| **Method of Preparation** | **Crystal Size (um)** | **Sample Size (nm)** | **Mobility ($cm^2V^{-1}S^{-1}$)** | **Applications** |
|---|---|---|---|---|
| Mechanical [1] exfoliation | >1000 | >1 | >2x$10^5$ m | Research |
| Chemical exfoliation | <= 0.1 | Infinite as layers overlaps | 100 (overlaps layers) | Coating Biomedical |
| Chem. Ex. Via. Graph. oxide | ~100 | Infinite as layers overlaps | 1(overlaps layers) | Energy storage Bat. electrode |
| CVD [3] | 1000 | ~1000 | 10000 | Nano-electronics |
| Graphene on SiC/hBN/$HfO_2$ | 50 | 100 | 10000 | High frequency transistor |

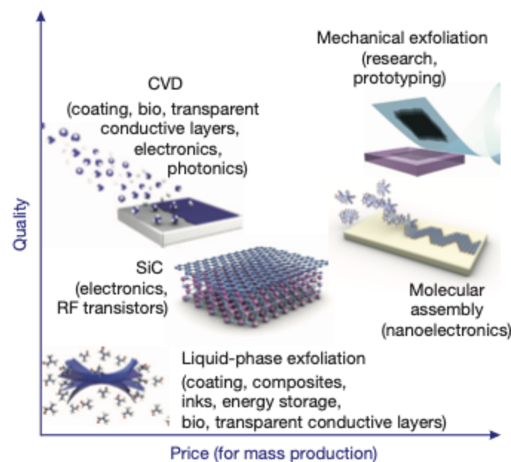



Figure 2.3 Method of graphene preparation with applications of the particular graphene sheet [6].

The summary of the preparation method of graphene given in table 2.3 is application specific. Figure 2.3 Method of graphene preparation with applications of the particular graphene sheet [6]. Chemical vapour deposition grew graphene sheet and transfer technology of graphene on dielectric/silicon base surface is highly conduct electrically and thermally. Both of these properties are highly commendable for graphene-based RF electronic devices. Exemplary high voltage gain amplifiers or frequency doubler circuits are the graphene RF electronics available in the market. Finding bandgap in graphene and the required magnitude of on/off ratio for digital electronics is still a challenge for graphene electronics, however graphene heterostructure with hBN, $MoS_2$ and $HfO_2$ is under research. Graphene heterostructure has published marvellous results supporting graphene optoelectronics, and flexible electronic applications. A comparison of graphene properties with other 2D materials is given in table 2.4. Graphene channel length and their compatibility according to rigidity, tunability and density are summarized in table 2.5. The supremacy of graphene over all the 2D layer materials conductivity-wise and tenability-wise can be found in the tables. Figure 2.4 molecular layered structure of graphene other 2D layered materials [09].

Table 2.4 | solid-state properties of 2D layered crystalline materials at 300k [12].

| **2D material** | **Electrical properties Mobility and $V_{sat}$ ($cm^2$/V sec) & ($cm^2$/sec)** | **Optical Band gap and Band type** | **RF Applications** |
|---|---|---|---|
| Graphene 1, 4, 11 | 3-5 x $10^4$ and 1-5 x $10^7$ | 0 and D | High Voltage Gain Amplifier |
| 1L MoS2 13, 16, | 10-130 and 4 x $10^6$ | 1.8 and D | Flexible nanoelectronics display devices |
| Bulk MoS2 13, 14 | 30-500 and 3 x $10^6$ | 1.2 and I | Flexible nanoelectronics display devices |
| 1L WSe2 13, 15 | 140-250 and 4 x $10^6$ | 1.7 and D | TFET as frequency multiplier |
| Bulk WSe2 13,93 | 500 and NA | 1.2 and I | Frequency multiplier |
| h-BN 17, 18 | NA and NA | 5.9 and D | 2D dielectric |
| Phosphorene 19, 20 | 50-1000 and NA | 0.3-2 and D | Flexible electronics |

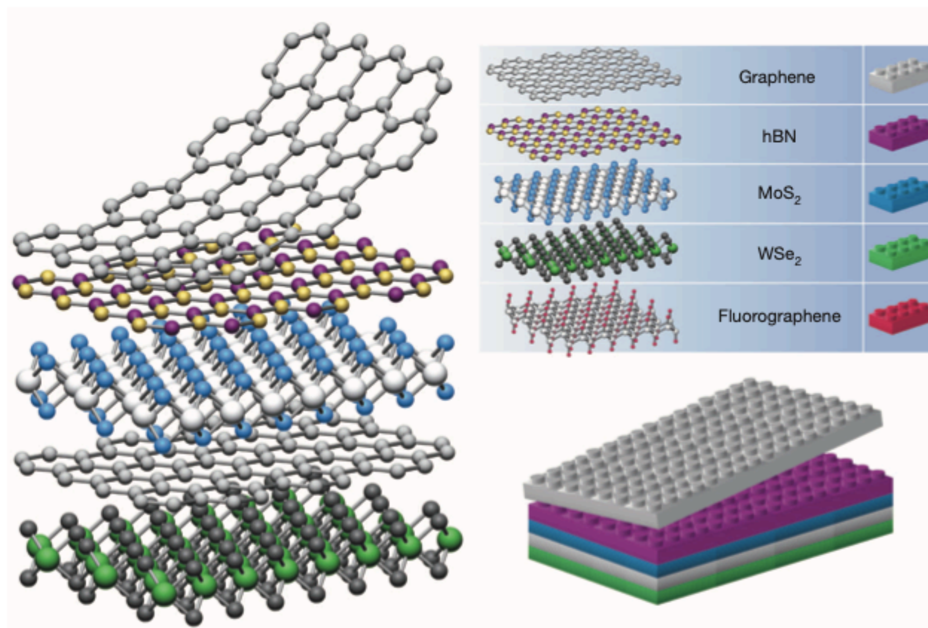



Figure 2.4 molecular layered structure of graphene other 2D layered materials [09]

Graphene channel length, graphene channels in different configurations and their comparison with other 2D materials channel is given in table 2.5. Graphene products from lab to market can be found in table 2.6. Figure 2.5 a) Graphene and other 2d materials with their b) flexible electronic applications [12] c) sub-Nano channels [21]. The heat sink capacity of graphene because of its high thermal conductivity has been utilized in Huawei 20X model smartphone for its supercool vapour chamber technology. TeamGroup and Momodesign also have developed a product using graphene's high thermal conductivity is now in the market. Graphenea produced mGFET-4D, mGFET-4P, and GFET-S20 graphene chip and card for the sensor application like biosensor with great readout capabilities. Chongqing Graphene Technology has processed CVD grew graphene sheets for touch panels with remarkable flexibility. The versatile sports manufacturing company has designed highly strong tennis and squash rackets.

Table 2.5 | Summary of the promising sub-nanometre-scale channel [21]

| **2D Materials** | **Nanometer channel lengths** | **Structural tunability, channel rigidness and density for nanoelectronics devices** |
|---|---|---|
| Graphene | Graphene fluidic channels 22, 23<br>34 to 1000nm | Low in tunability, which is depends on channel size, highly rigid and moderate channel density |
| Graphene oxide | a ~ 46 to 66nm (dry) 24<br>a ~ 86 to 104 nm (wet) | Moderate tunability, tuned by oxidation degree, lowly rigid and moderate channel density |
| $WSe_2$ | NA | Moderate tunability, tuned by sheet size and layer by layer functionality, moderate rigid and moderate channel density |
| hBN | a ~ 19nm (dry) 25<br>a ~ 80 to 183 nm (wet) | Moderate tunability, tuned by sheet size and layer by layer functionality, moderate rigid and moderate channel density |
| $MoS_2$ | a ~ 30 nm (dry) 26<br>a ~ 90 nm (wet) | Moderate tunability, tuned by sheet size and layer by layer functionality, moderate rigid and moderate channel density |

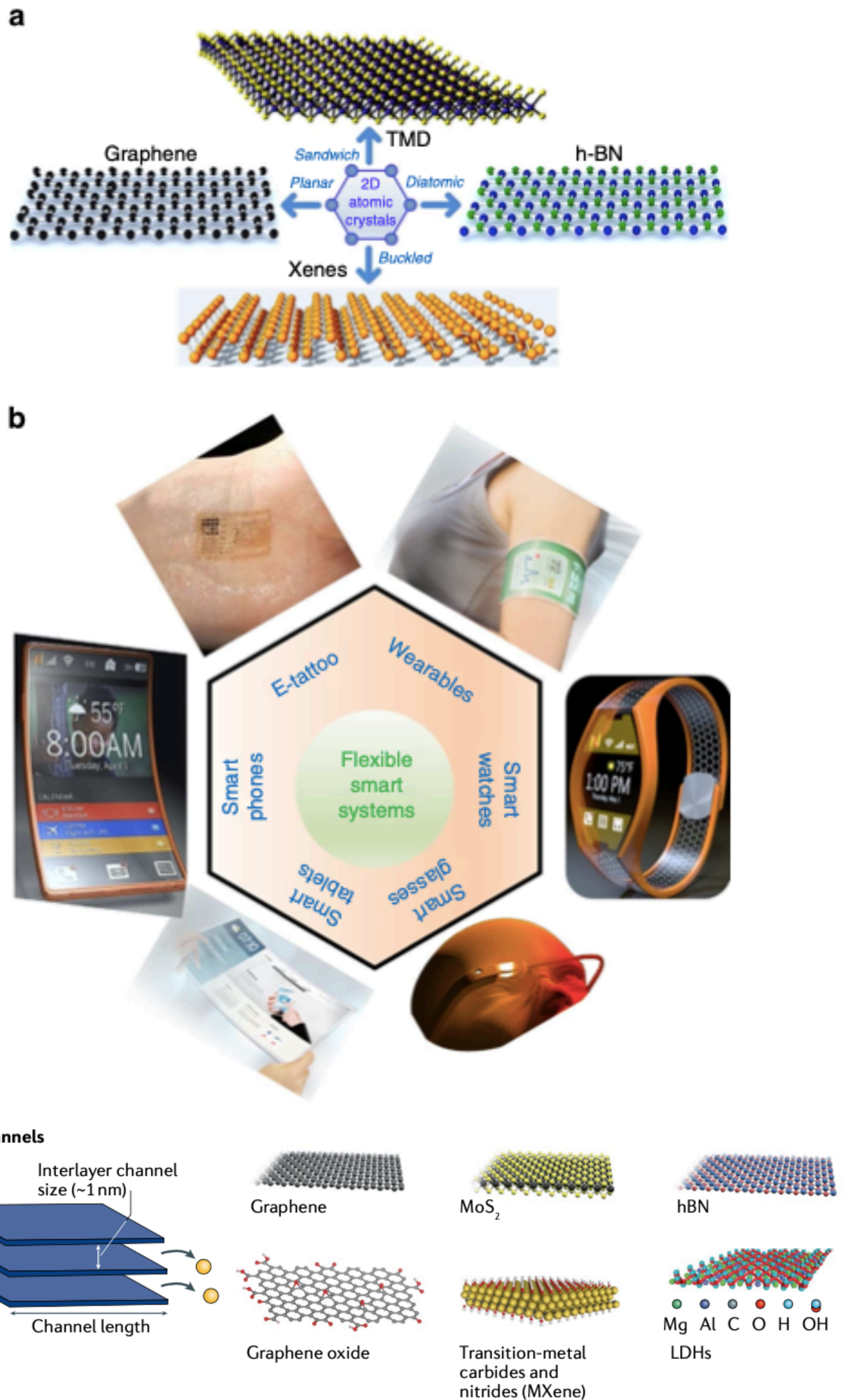



Figure 2.5 a) Graphene and other 2d materials with their b) flexible electronic applications [12] c) sub-Nano channels [21].

Table 2.6 List of graphene-based product travels out of laboratories [27].

| Company | Product (model) | Graphene properties utilized and Features |
|---|---|---|
| 1.Huawei | Smartphone (Mate 20 X) | Thermal, Graphene film as a heat sink for cooling 28 |
| 2.TeamGroup | Solid-state drives (Cardea Zero M.2 PCIe SSD) | Thermal, Graphene heat spreader for efficient SSD cooling 29 |
| 3.Momodesign | Helmet (FGTR Graphene 1.0) | Thermal, mechanical, and Graphene film for efficient heat dissipation 30 |
| 4.HEAD | Tennis racquet, Ski (GrapheneXT) | Mechanical, Graphene for light weight, flexibility and robustness 31 |
| 5.Nanomedical diagnostics | Biosensor (Agile) | Electrical, Graphene FET as a biochemical sensor 32 |
| 6.Graphenea | Transistor array (GFET-S10) | Electrical, FETs on SiO2 with CVD graphene and 1,000 cm2 V s–1 mobility 33 (https://www.Graphenea.com) |
| 7.Chongqing Graphene Tech. | Smartphone | Electrical, Optical and Mechanical, Flexible touch screen for mobile phone 34 |
| 8.Graphene Flagship | Communication link (modulator and detector) | Electrical, Optical, and All-graphene optical communication link at 25 Gb s–1 35 |
| 9.CalBattery | Lithium battery electrode | Silicon–graphene composite anode 36 |

### 2.4 Modelling of GFETs

The very first Graphene based FET [37] is comes in 2007, and technological advancement is very fast. In a few next years, interesting GFET models are reported with the intrinsic transit frequency comparable to higher than similar size CMOS nanometer technology [38-42]. Few other compacts and fundamental physics-based quasi-analytic modelling for graphene heterostructure field effect transistor (GFETs) with large area graphene are described with time as well as research technology advancement [43]. GFETs modelling based on basic physics exploring drain current, capacitance and charge parameters for graphene channel are reported in [44-47].

In electronics applied amplifier, a small signal is amplified and operated in ON state and RF signals are to be superimposed onto DC gate-source voltage but what is more important to improve is the figure of merit (FoM) like cut-off frequency or intrinsic gain with high transconductance. The compact model is benchmarked with measured current-voltage characteristics with accuracy for prototype devices and predictive behavior. The explicit compact model of drain current [44] has been extended in [45] to explore the AC and transient behavior of the GFET. Both of these physical frameworks are field effect models based on the drift-diffusion charge carrier transport mechanism. The Ward-Dutton charge partition scheme is implemented to model the source-drain charge together with transconductance and self-capacitance.

Furthermore, scalable large signal Graphene based Field effect model has been implemented on the SPICE, Cadence or ADS and Verilog-A platforms [48-55]. A comprehensive simple and compact mathematical model provides graphene field effect transistor's physical parameters [49] and their closed form formulas like $g_m$, $r_0$, $C_{gs}$ and $C_{gd}$. While [48] presents a scalable and compact graphene FET model analyzing its electrical properties. An accurate hardware descriptive language programmable GFET is modelled in [50]. Unlike other GFETs models [51] formulate an accurate drain current with effective carrier mobility calculation, which differentiates in electron and hole considering mobility variations against carrier density. A series of two large signal graphene FETs model intrinsic capacitance [52] and benchmark performance analysis [53] provide Verilog implementable graphene transistor modelling. In 2017, a year later model of a large-signal compact monolayer Graphene FET targeting RF circuits is reported [54].

Some unique and conventional or obsolete but always important structure (BJT) technology has been modelled for DC and RF performance analysis of Graphene Base Transistor [55] with an ideal limit of unity common base current gain. Graphene-based transistors (GBTs) are quite different from GFETs. Two insulating layers sandwiched graphene to form a vertical stack that separates the emitter from the collector. GBTs operates similarly to conventional hot electron transistor electrons travel from the emitter towards the collector by tunneling through the emitter-base insulator (EBI) and the base-collector insulator (CBI), hence the charge travels through a high mobile graphene sheet. Although in GBTs base is very thin but the high mobility of the graphene is expected to reduce the base resistance.

The DC functionality of the GBTs has been proven experimentally by the "A Graphene-based hot electron transistor" and others. But no RF measurements are available and the potential for RF operations has been done by simulation only. "Modeling, simulation, and design of vertical graphene base transistor," suggested that the intrinsic device may be capable of reaching cutoff frequencies ($f_T$) in the terahertz range. Whereas observed output resistance and intrinsic gain are larger than for GFETs which are confirmed in "DC and small signal numerical simulation of a graphene-base transistor for terahertz operation. Therefore, it is expected that GBTs can overcome the typical limitation of GFETs. Continuous research efforts and search for a favorable graphene transistor configuration exploring resistance, Negative differential resistance and conductance have been modelled [56-59].

A short-channel contact-induced negative differential resistance GFETs model using non-equilibrium green's function (NEGF) to explore ballistic transport nature in the channel [56]. A boron nitride substrates GFET model explains pseudosaturation and negative differential conductance (NDC) behavior using NEGF to solve a tight binding Hamiltonian for graphene [57]. Targeting high voltage gain negative differential resistance (NDR) monolayer

Graphene based FETs model investigates numerical feasibility itself [58]. Dual gate GFETs model introducing Debye length to calculate drain current-voltage heuristically [59]. Since graphene has exceptional carrier mobility so it must travel ballistically through the channel but due to the lack of suitable substrate interface scattering and substrate surface roughness does not allow ballistic transport in earlier models. Even though some hard work is done, produce ballistic and quasi-ballistic transport models explain backscattering using Mekelvey's flux theory approach [60-63].

A short-channel ballistic regime GFETs model analysis and optimize device model for analog and RF applications [60]. An explicit quasi-ballistic transport model for graphene with only a few fitting parameters to calculate drain-to-source current is reported in [61]. A less than 9% normalized root mean square error and electronic design tool development supportive quasi-ballistic model for graphene-based FET is presented in [62]. The latest Quasi-ballistic GFETs model to determine the backscattering coefficient for a charge, capacitance and current is reported in [63]. A GFET model to investigate graphene transistors' electrostatic discharge (ESD) behavior is published recently [64].

### 2.4.1 FUNDAMENTAL PHYSICS BASED MODELLING

The modelling of graphene field effect transistors (GFETs) is categorized majorly into four types 1) fundamental physics-based model 2) explicit drain current and capacitance model 3) drift-diffusion model 4) Quasi-ballistic or flux-based model. The fundamental physics-based model starts with the properties graphene layer which is used as the channel in the GFETs and formulates the energy levels present in graphene material, no. of energy states, the density of states, electron and hole density of graphene channel. Quantum mechanics theory also constitutes density of states, kinetic energy, mean free path length, and electron density of charged particles in solid-state semiconductors.

- The density of electrons (N, E (kinetic energy) is given) [93]

$$\frac{\mathrm{dN}}{4\pi(\mathrm{p}\sim)2\mathrm{dp}\sim} = \frac{N}{(2\pi m_o kT)^{3/2}} + \exp\left[\frac{(\mathrm{p}\sim)2}{(2m_o kT)}\right]$$

- Kinetic energy

$$E = \frac{\hbar^2 \psi^2}{2m_o} = \frac{\hbar^2 k^2}{2m_o}$$

- Mean free path ($\lambda$ ) length

$$\lambda = \frac{\hbar^2}{2m_o}\psi$$

- Electron density of the Conduction band (C.B.) [93]

$$n = \left(\frac{2\pi m *_n K_B T}{h}\right)^{3/2} \int_0^\infty \left[\frac{|E|}{\exp\{|E| - \frac{(E_F - E_c)}{K_B T}\} + 1}\right] dE$$

$n = NC\left[\exp \frac{(E_F - E_c)}{K_B T}\right]$ Boltzmann's approx. of FDI only when the distance between Fermi-level and C.B is more than the 3KT(quantum limit). Lorentz model (Lorentz assumed that electron velocities and momenta varied in accordance with the classical Maxwell-Boltzmann distribution law.) a brief introduction of classical theory to present electrical versus thermal conductivity model of semiconductor to reformulate the electron density in an energy band.

- Classical momentum (scattering not given)

$$p\sim = (3m_o kT)^{1/2}$$

- Ratio of thermal to electrical conductivity

$$\frac{k}{\sigma} = 3\left(\frac{k}{e}\right)^2 T \quad \text{(Wiedemann and Franz exp model 1853)}$$

- Reformulated mean free path ($\lambda$ ) length

$$\tau = m/\rho n e^2, \ \lambda = V_0\, \tau$$

- Lorentz model (Lorentz assumed that electron velocities and momenta varied in accordance with the classical Maxwell-Boltzmann distribution law) [93].

$$\mathrm{dN} = \frac{4\pi N(\mathrm{p}\sim)2}{(2\pi m_o kT)^{3/2}} + \exp\left[\frac{(\mathrm{p}\sim)2}{(2m_o kT)}\right]$$

Use of these classical and quantum mechanics theories to formulate the density of states, charge carrier concentration, quantum capacitance and drain current for graphene FETs. Fermi Dirac integral (FDI) is also very handful to calculate the fundamental physics for the graphene channel and GFETs.

- DOS (density of states) of graphene layer [81].

$$N(E) = g_s g_v \frac{Ak^2}{4\pi(\hbar v_{\mathrm{f}})^2}$$

- Now use charge carrier density and Fermi level to find carrier concentration i.e. no. of holes and electron [81].

$$p = \int_{-Ecv}^{\infty} \frac{2}{\pi} \frac{|E|}{(\hbar v_{\mathrm{f}})^2} \left[ \frac{1}{exp\frac{(E + E_F)}{K_B T} + 1} \right] dE$$

- Thus, total charge density can be found.

$$Q_{gr} = \frac{2}{\pi} \frac{q|E|}{(\hbar v_{\mathrm{f}})^2} \int_{0}^{\infty} \left[ \frac{1}{exp\frac{(E - E_F)}{K_B T} + 1} - \frac{1}{exp\frac{(E + E_F)}{K_B T} + 1} \right] dE$$

- Now use total charge carrier density to calculate quantum capacitance.

$$\mathrm{C_q} = -\frac{\mathrm{d}Q_{gr}}{\mathrm{d}V_{gr}}$$

- Drain current [43, 44]

$$\mathrm{I_d} = \mathrm{q}\mu W \frac{\mu \int_0^{V_{ds}} \rho_{gr} dV}{L - \mu \int_0^{V_{ds}} \frac{1}{v_{sat}} dV}$$

- Quantum capacitance [42]

$$\mathrm{C_q} = -\frac{2q}{\pi} \frac{qV_{CH} K_B T}{(\hbar v f)^2} \ln\left[2\left(1 + cosh\frac{qV_{CH}}{K_B T}\right)\right]$$

- Channel potential

$$V_{CH} = \frac{C_{box}}{\mathrm{C_t + C_b + 0.5\,C_q}} [(V_{gs_t} - V(x)/2) - (V_{gs_b} - V(x)/2)]$$

### 2.4.2 EXPLICIT DRAIN CURRENT BASED MODEL

2) Explicit drain current model keeps it compact and concentrates to formulate drain current and quantum capacitance using the electric potential of the graphene channel. Drain current is here simple product of charge carrier mobility, width/length ratio, and channel potential term. While the integration of charge density over drain voltage and integration of inverse velocity of saturation of charge particle is interestingly complex. Integration of charge density is also including the puddle charge which means electron to electron and hole to hole and electron to hole interaction is also an active part to generate charge particles in the graphene channel of GFETs other than thermal agitation.

- Drain current [61,62]

$$I_{DS} = \mu_{(n,p)} W \frac{\int_0^{V_{ds}} (|Q_{(n,p)}| + q\, n_{(puddle)}/2) dV}{L + \mu \int_0^{V_{ds}} \frac{1}{v_{sat}} dV}$$

- Quantum capacitance [42]

$$C_q = -\frac{2q^2}{\pi} \frac{q|V_{CH}|}{(\hbar v_f)^2}$$

- Channel potential [44]

$$V_{CH} = \frac{-(C_t + C_b) + \sqrt{(C_t + C_b)^2 \pm k C_q \{ (V_{gs} - V_{gs0} - V(x)) C_t + (V_{bs} - V_{bs0} - V(x)) C_b \}}}{\pm k C_q}$$

Where the positive and negative sign is depends on that if, $\{ (V_{gs} - V_{gs0} - V(x)) C_t + (V_{bs} - V_{bs0} - V(x)) C_b \}$ is > (<) 0.

### 2.4.3 QUASI-BALLISTIC TRANSPORT(FLUX) BASED MODEL

Fundamental physics-based model Considered charge carrier and explicit drain current model considered electric potential a basic element to modelled the solid-state physics of GFETs. While quasi-ballistic model considered electric flux a basic element for modelling solid state physics of the ballistically and quasi-ballistically transported charge carrier in the ]graphene

channel of GFETs. The complexity of the integration of saturation velocity is solved in this modelling, however, backscattering coefficients ($r_{bs}$) add complexity to this modelling. A modified FDI is applied to integration and to calculate the flux of the graphene channel in quasi-ballistic GFETs. 4) Drift and diffusion modelling are very conventional means basically deals with resistance at the input and at the output of FETs, due to very high electrical and thermal conductivity of graphene we do not concern too much for input and output resistance of GFET models. Drift-diffusion is also not our scope of GFETs modelling and simulation, so the drift and diffusion modelling in detail can be found [43-44]. Contact resistance and quantum capacitance is big deal for graphene devices, so in this thesis, we focus on fundamental physics-based and quasi-ballistic flux-based modelling. Quantum capacitance is the parameter of big concern for our models. The Quantum capacitance model leads modelling of the drain current and to the nonlinearity of the GFET models.

- Drain current [63,64]

$$I_{DS} = \frac{Wn(0)V_{Th}(1\text{-}r_{bs})[1\text{-}\mathrm{I}_1(\omega_F - \omega_{DS})/\mathrm{I}_1(\omega_F)]}{[(1 + r_{bs} + (1\text{-}r_{bs})\mathrm{I}_1(\omega_F - \omega_{DS})/\mathrm{I}_1(\omega_F)]}$$

- Flux (or potential) to drive drain current

$$I_{DS} = Wq[F^{+}(0) - F^{-}(0)]$$

- Where flux can be written as

$$F^{+}(0) = N_{2D}\ V_{th}\ \Im_1(\omega_F)$$

- When $\mathrm{I}_1(\omega_F)$ is the Fermi-Dirac integral of order one defined by Blakemore.

## 2.5 GFETs Structures

A single-layer graphene flack is being used as the transport channel in GFETs. The 2D cross-sectional View of the GFET structure is shown above in Fig. 2.6, in which gate length is extended from x (0 to L) source end to drain end, which is approx. 1000nm. This model contains a top gate and a back gate, so one can use it as a single and double gate. This modelled structure also has top gate oxide ($t_{ox}$) of 15 nm thickness of hexagonal boron nitride (hBN) shown below the gate and back gate oxide ($SiO_2$) thickness of approx. 300nm above on the P-type silicon (100) base of thickness 500nm. Top gate, source and a drain electrode on top single layer graphene flack made of a stack of Ti/Au of thickness 70/50nm respectively. Fig. 2.7 is showing a graphene heterostructure with a few layers of hBN on a silicon body.

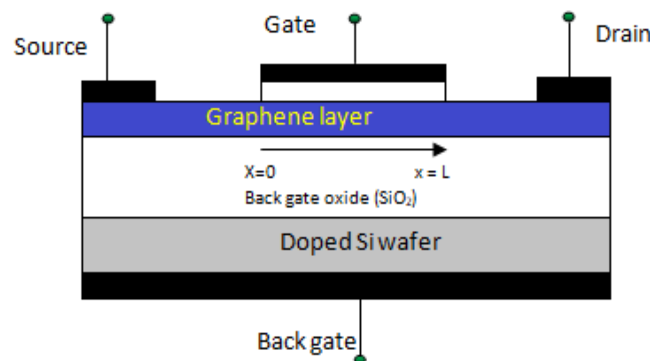



Figure 2.6 Two-dimensional Cross-sectional view of the basic Graphene Field Effect Transistors

Cr/Au(10/30nm)
S
hBN(5nm)
D
Graphene 1(.334nm)
hBN(5nm)
Graphene 1(.334nm)
hBN(5nm)
SiO2(300nm)
Si(500nm)

Figure 2.7 Two-dimensional Cross-sectional view of the heterostructure Graphene Field Effect Transistors.

### 2.6 Research Gaps

Based on the literature survey following research gaps are identified.

**2.6.1** Unexplored important parameters of the GFETs modelling.

**2.6.2** Linearity and non-linearity of GFET models have not developed enough for all regions and transport approaches.

**2.6.3** Unavailability of a high-performance ballistic/quasi-ballistic transport model for GFETs.

**2.6.4** Limitations of Graphene-SiO2 and scope for the other 2D dielectric materials.

### 2.7 Research Objectives

Based on the literature survey and research gaps following research objectives are identified.

**2.7.1** To explore and implement a closed-form model of GFET, using effective mobility.

**2.7.2** To study and formulate the non-linearity and linearity characteristic behaviour of the quasi-ballistic GFETs model.

**2.7.3** To drive and formulate scalable closed form quasi-ballistic GFETs model.

**2.7.4** To explore and simulate the electronic properties of graphene on various 2D dielectric beds.

# Chapter three

## Study of Electronic Properties of Single and Bilayer Graphene gr/hBN Heterostructure

### 3.1 INTRODUCTION

Graphene is of high-interest 2D material for electronics applications [1-2], because of its very high electron mobility [3-5] of 200000$cm^2V^{-1}S^{-1}$ in its pure suspended state. It is just out of imagination thoughts that an atomically thick/thin material could be thermally stable. Although graphene shows marvellous electronic qualities in its pristine thin film form these properties are being deteriorated by the supporting semiconductor material and oxides [6-7]. The mean free path greater than 2 microns at high carrier density $10^{12}$ $cm^{-2}$ with a big low down in intrinsic mobility to extrinsic mobility from 2 x $10^5$ to 4 x $10^4$ $cm^2$/Vsec for graphene at room temperature seeks to find a new substrate choice for graphene-based electronics [6]. Graphene electronic devices exhibit many inferior characteristics on $SiO_2$ as expected of intrinsic graphene properties [7]. Thus, the Research advancements come in terms of various 2D Dielectric materials like BN, BCN, etc. Specially hBN (hexagonal Boron Nitride) is found best suitable 2D material that supports graphene flack and provides a wonderful Gr/hBN interface along with keeping graphene's superb electronic qualities [8-10]. A dangling bond-free smooth surface and atomically matched structure of hBN is an appealing substrate for graphene electronic applications [8]. Even after solving substrate issues graphene-based field effect devices lagging regularly for bandgap, which is very useful to graphene device logic applications. Bilayer graphene gr/hBN heterostructure i.e. graphene layers stacked with hBN layer as insulating isomorph of graphite produce a bandgap along with a good current ON/OFF ratio [11, 18]. Gr/hBN heterostructure in its lateral tunnelling structure is compared with gr/$MoS_2$ heterostructure and shows an approximate current ON/OFF ratio of 50 [11]. Another

different structure named encapsulated means a graphene layer captured by an hBN oxide at both top and bottom end also explores the scope and possibility of gr/hBN heterostructure and provides great results for graphene electronics [66-67]. A comparison of gr/hBN heterostructure with (graphene nanoribbon) GNR/hBN heterostructure suggests that gr/hBN heterostructure are better graphene structure option for graphene-based electronics devices [68].

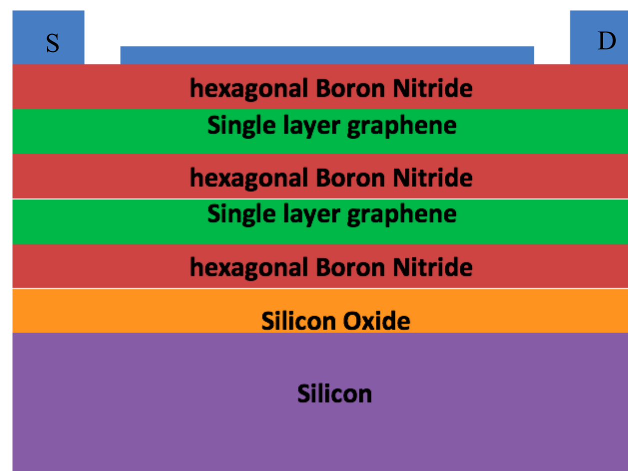



Figure 3.1 Single layer Gr/hBN Heterostructure Fits for GFETs, with source, drain at top ends and gate in top middle with Ag/Cu metal.

Literature [69-74] has explored gr/hBN heterostructure electronically such as electronic highways (transports) in bilayer graphene [69], the study of gr/hBN Van der Walls heterostructure [70-71] interlayer or layer by layer Dirac fermions formation, cross-sectional images and buried interface properties [72], Scanning Tunnelling Microscopy (STM) based locale electronic properties [73] and interlayer tunnelling insight [74-77] of gr/hBN heterostructure. Figure 3.1 shows a gr/hBN i. e. graphene layer of atomic thickness is encapsulated by the hexagonal Boron Nitride layer of the almost same thickness, and so provides a stable structure with appropriate band gap and much needed and improved current on-off ratio.

This paper is organized into three sections, Section one introduces graphene (2D material) properties and the pros and cons of substrates for graphene-like hBN. Section two discusses and explains the band diagram electronically, current density and charge carrier density concerning the thickness of graphene layer stacked over hBN, gr/hBN heterostructure followed by simulation results. Section-III concludes the paper that gr/hBN heterostructure is the appealing graphene electronic device structure.

### 3.2 Result and Discussion

This section discusses and demonstrates single-layer graphene, bilayer and graphene heterostructure (encapsulated by top and bottom of hBN layers) electronic properties developed by the AFORS-HET CAD tool. Electronic properties of a single layer of a thickness (.342nm) [2] and bilayer graphene of a thickness (.684nm), with a bandgap of approx. 0.24 eV and encapsulation of them with the single layer hBN layer at the top and bottom end (gr/hBN) heterostructure is being explained graphically. Bandgap and other basic properties such as Nv, Nc, electron affinity and permittivity of the single layer and bilayer graphene are given [1]. Bandgap, thickness and other basic properties of the hBN layer are accounted for on behalf of [7] where thickness is almost the same as (0.334nm) as of the graphene layer, but with the band gap of 5.97 eV [9].

Figures 3.2 and 3.4 graphically explore the bandgap, current density of am-bipolar nature graphene and the change in concentration of the graphene single layer and encapsulated graphene layer by the hBN layer top and down respectively, over the thickness of material layers. Figure 3.3 Bilayer graphene electronic properties with band diagram, current density and charge carrier concentration along with zero rate of generation and recombination of charge carriers versus thickness of the particular layer demonstrated.

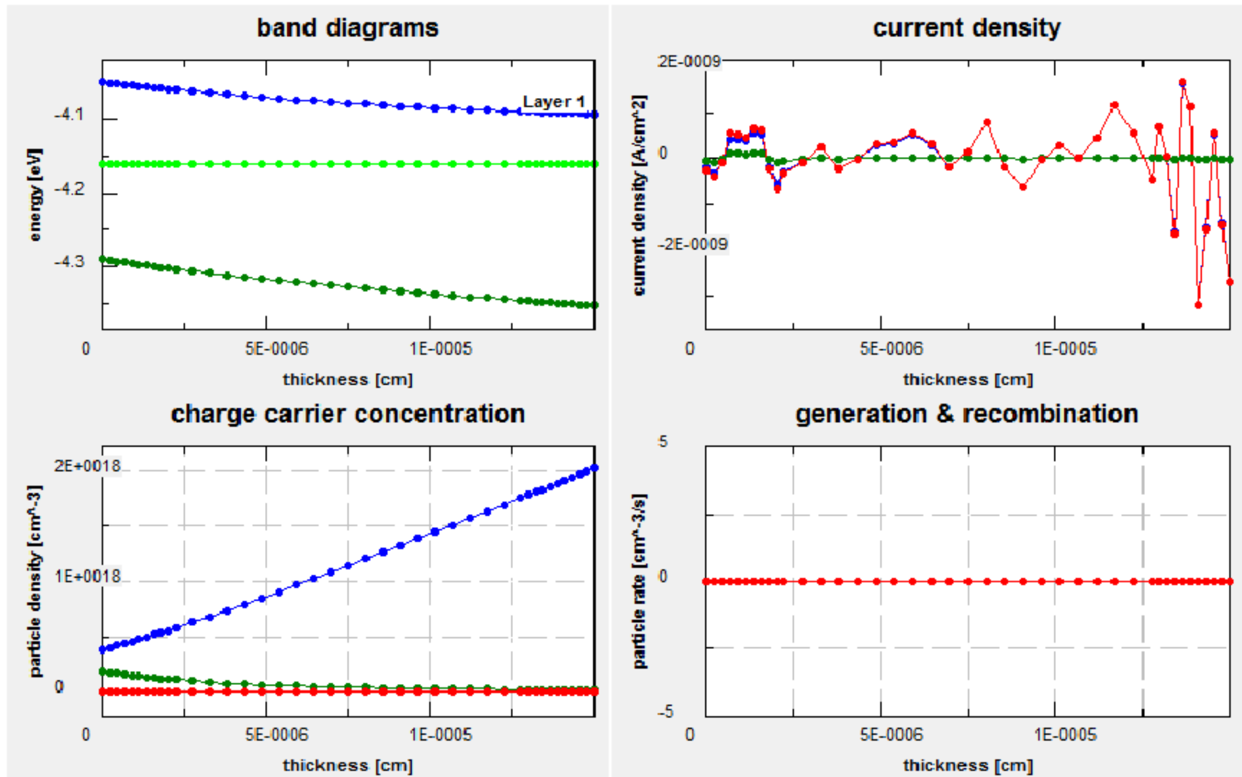



Figure 3. 2 Single layer graphene electronics property with band diagram, current density and charge carrier concentration along with zero rate of generation and recombination of charge carriers versus thickness of the particular layer.

The electronic band diagram, current density and charge carrier density concerning the thickness of graphene layer over gr/hBN heterostructure have been presented. Figure 3.4 Single layer graphene encapsulated by single hBN layers on top and bottom, electronic properties with band diagram, current density and charge carrier concentration along with zero rate of generation and recombination of charge carriers versus thickness of the particular layer. Figure 3.5 bilayer graphene encapsulated by single hBN layers on top and bottom graphene, electronic properties with band diagram, current density and charge carrier concentration along with zero rate of generation and recombination of charge carriers. Similarly, 3.3 and 3.5 explain results, like bandgap, current density carrier concentration and recombination and generation during the transport with the layer for bilayer graphene and encapsulated bilayer graphene by the hBN layer top and down respectively, over the variation of thickness of the material layer.

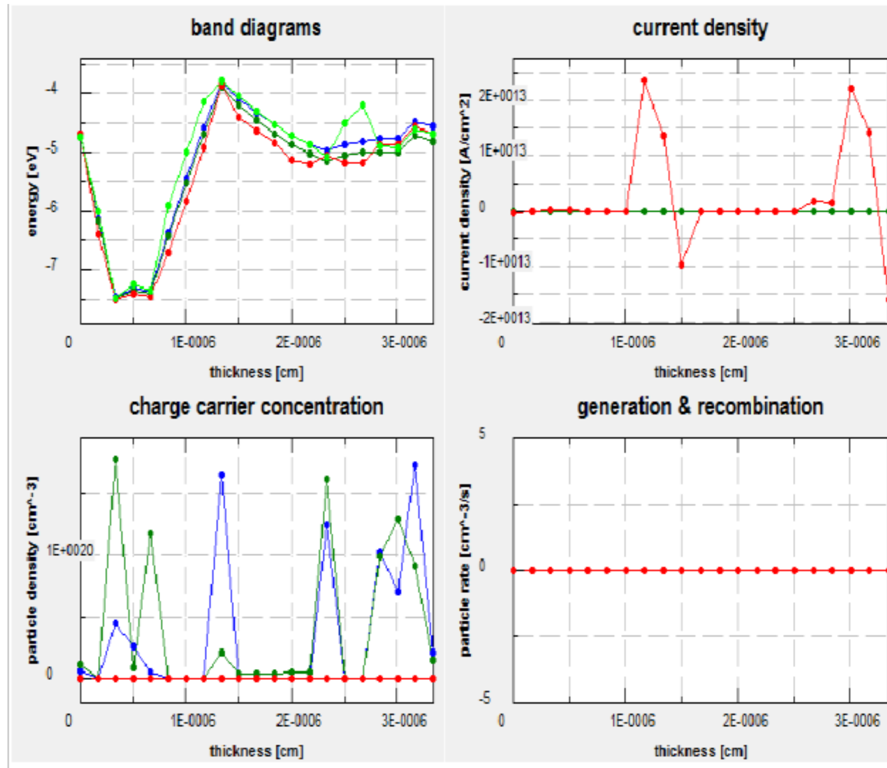



Figure 3.3 Bilayer graphene electronic properties with band diagram, current density and charge carrier concentration along with zero rate of generation and recombination of charge carriers versus thickness of the particular layer.

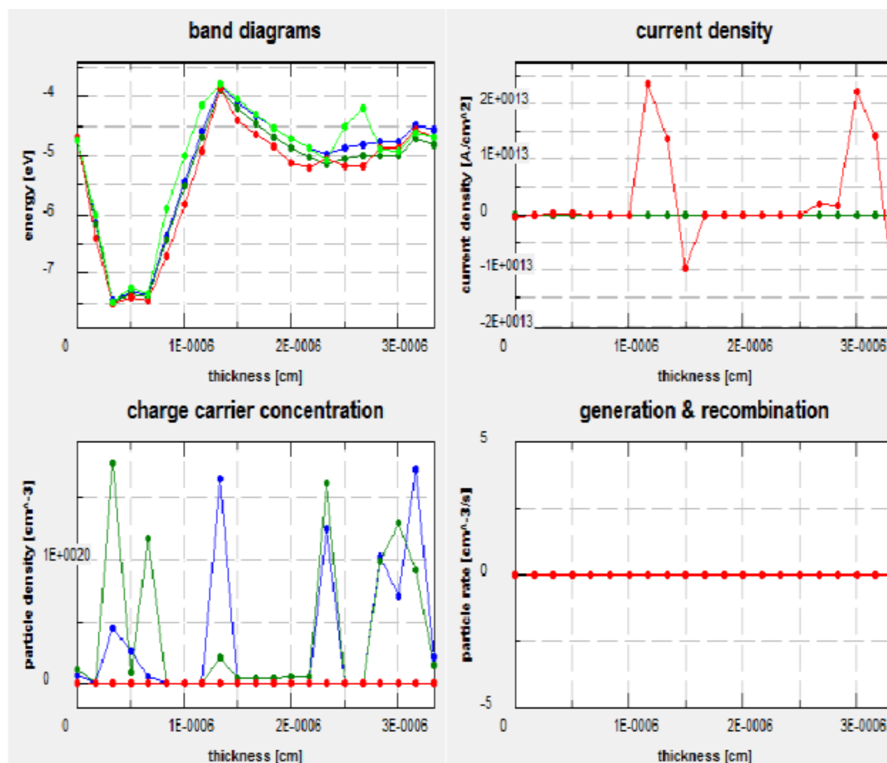



Figure 3.4 Single layer graphene encapsulated by single hBN layers on top and bottom, electronic properties with band diagram, current density and charge carrier concentration along with zero rate of generation and recombination of charge carriers versus thickness of the particular layer.

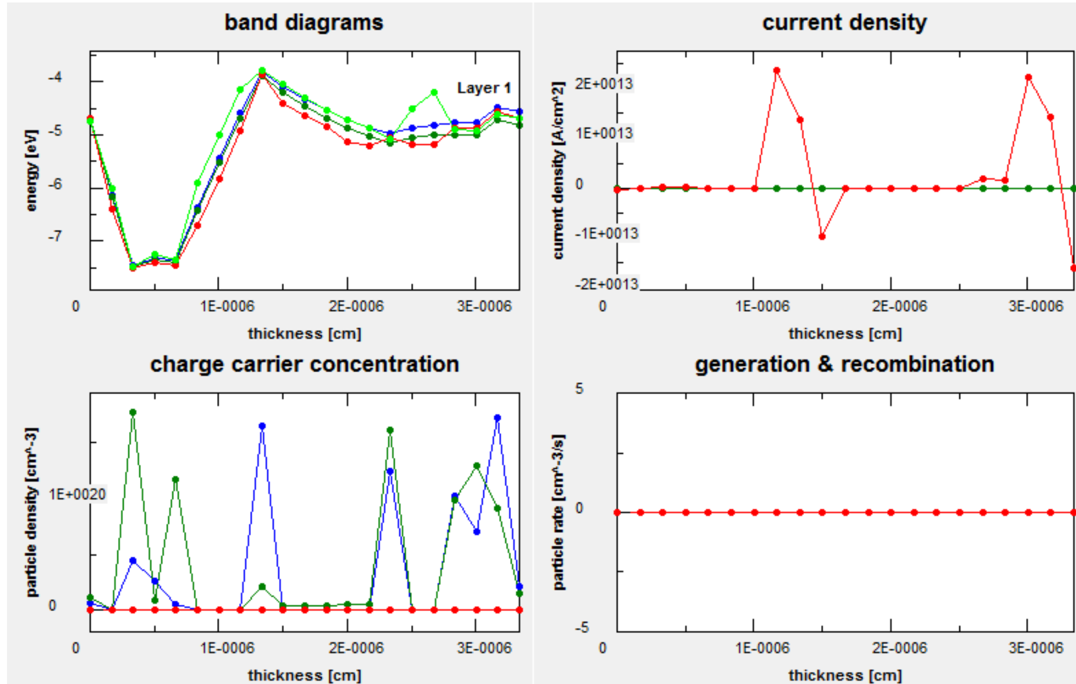



Figure 3.5 bilayer graphene encapsulated by single hBN layers on top and bottom graphene, electronic properties with band diagram, current density and charge carrier concentration along with zero rate of generation and recombination of charge carriers.

### 3.3 COMPRESSION

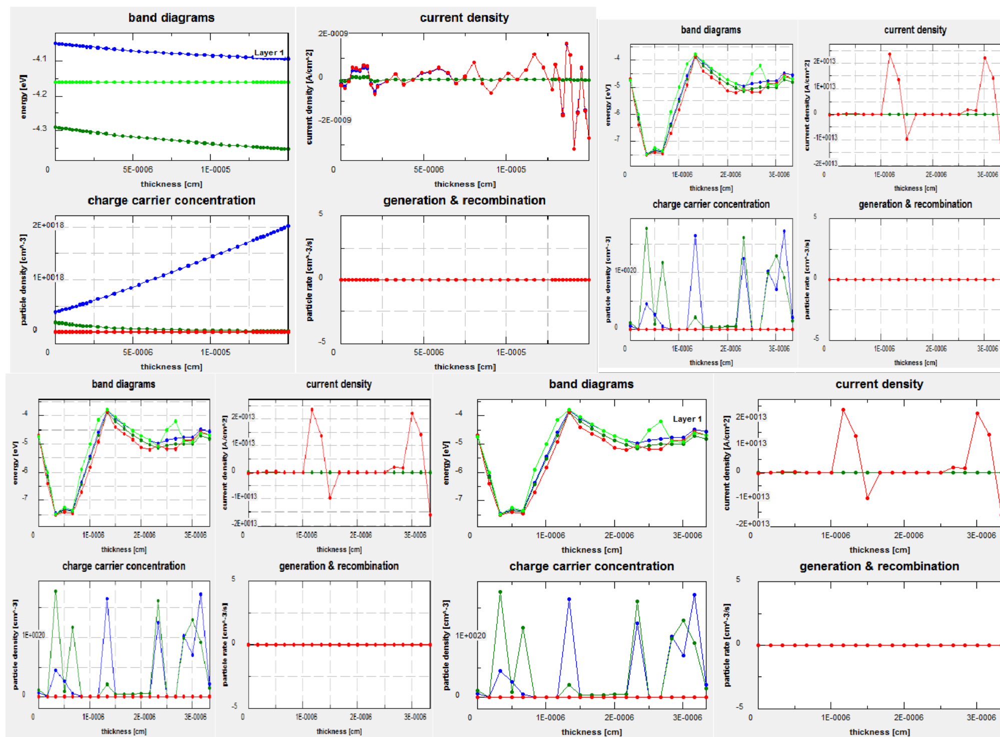



Figure 3.6. Comparison of a single layer, bilayer, single layer encapsulated, and bilayer encapsulated graphene sheet bandgap, current density, carrier concentration and interaction rate of the carrier in the graphene layer.

### 3.4 Chapter summary

The electronic properties of single layer and bilayer graphene, along with graphene over the hBN layer (gr/hBN heterostructure) are studied and well demonstrated. The electronic band diagram, current density and charge carrier density concerning the thickness of graphene layer over gr/hBN heterostructure have been presented. An energy band gap widening is observed from the single and bilayer graphene encapsulated in the hBN dielectric sheet.

# Chapter four

## Nonlinearity Analysis of Quantum Capacitance and its Effect on Nano-GFET characteristics

### 4.1 INTRODUCTION

Heart of the electronic devices is always the ability of a particular material to control its electronic properties in the presence of another electric field. Since the semiconductor industry is already out of scaling limits for silicon-based devices. So, this industry needs the next excellent alternative to silicon. Graphene, after its first physically stable noble experimentation in 2004 is promising to be the next alternative to silicon. Graphene is a single atomic (carbon) thin or thick layer (~$3.34 \times 10^{-10}$ m) so it is called a 2-D material [1-5], along with a high charge carrier mobility [2] of value more than $10^5$ $cm^2$/V-sec and even thermodynamically stable. The CVD-grown graphene layer and graphene growth over a base other than silicon could be a possible option for high-frequency and analog electronic devices and circuits [4-5]. The very first physical demonstration of the field emission effect in graphene layers comes in the form of an experimental device in 2007 [38]. As the technological advancement is very fast, few next year's interesting GFETs models with the intrinsic transit frequency and the maximum frequency of GFETs operation are comparable and higher than similar size CMOS nanometer technology [39-41]. The current saturation effect in a single layer [78] and bilayer layer graphene [79], with a high value of transconductance and transistor resistance, directly affect the GFETs performance. Gate/channel length of graphene has an impact on the operating frequency of the proposed GFETs model, therefore, besides the high resistance and transconductance values, graphene RF circuits find their application in defense in real life, so this is the main focus of this particular work. Other important, compacts and fundamental physics-based quasi-analytic modelling for (GFETs) with large area graphene are also given in

the literature [42]. Some other work like GFETs modelling based on basic physics explores drain current, capacitance, and charge parameters for graphene channels [43-45]. An explicit compact model of drain current [43] has been extended in [44] to explore the AC and transient behaviour of the GFETs. Both of these physical frameworks are field effect models based on the drift-diffusion charge carrier transport mechanism. The Ward-Dutton charge partition scheme is implemented to model the source-drain charge together with transconductance and self-capacitance. These [46-47] compact model is benchmarked with measured current-voltage characteristic with accuracy for prototype devices and predictive behaviour. Also, a few comprehensive simple and compact mathematical model provides graphene field effect transistors' physical parameters closed form formulas like $g_m$, $r_0$, $C_{gs,}$ and $C_{gd}$. Many other comprehensive, compact and analytical modelling of GFETs gate capacitance and quantum capacitance as dependent modelling parameters have already been done. But all of them either are limited to modelling and simulation of GFETs characteristics like some latest GFETs models [48-50] or are complex or are practically preposterous i.e. not very up-to-date regarding nonlinearity of GFETs with no future application in the device and circuits [51-53]. The latest GFETs model is a quasi-ballistic transported charge carrier good to find its application in recent developed and designed electronics MOS device modelling and simulation [80]. The proposed model keeping its nature lucid mathematically presents the explicit quantum capacitance, drive the drain current formulation using it and also presents the nonlinearity of characteristic curves of the GFETs at nanometer technology. Since noise is always a key element to disturb the performance of the FETs and GFETs in real-world electronic devices and circuits, the study of nonlinearity to the transfer as well as output characteristics is our addiction to the modelling and simulation of the GFETs. Dual gate control along with the nonlinearity study has been given in transfer characteristic curves in the result and discussion section. Dual gate control to large area graphene GFETs is also a new concept for the proposed GFET modelling at 300nm technology.

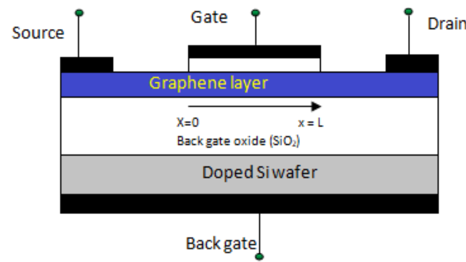
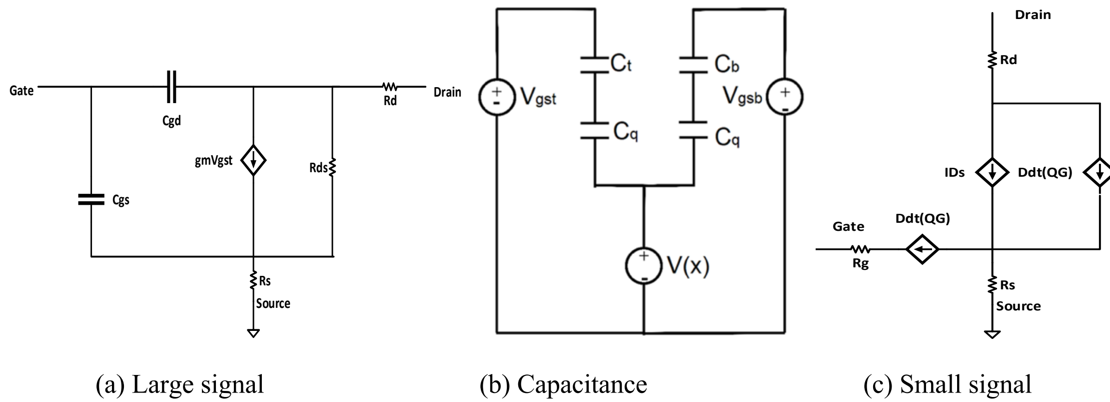



Figure 4.1 2-D Cross-sectional view of the proposed GFETs.




(a) Large signal (b) Capacitance (c) Small signal

Figure 4.2 (a), (b), (c) Equivalent circuit of the proposed GFETs (all h-parameter symbols have their usual meaning).

The structure of this paper is as follows, the detailed explanation of the physic-based GFET model starts from charge carrier concentration and density of states in section II analytical model. Furthermore, section II explains quantum capacitance which leads to the drain current formulation and helps to plot the graphical results for the GFET at 1000nm and 300nm channel length. Where this is noticeable that the source is grounded. Section III discussed and compares the experimental results with the proposed model results. Finally, section IV concludes this GFET model.

## 4.2 Analytical Model

### 4.2.1 Device structure of GFETs

The proposed compact model is based on a well-established dual-gate MOS structure which is shown in Fig. 4.1 as a 2-D cross-sectional view of proposed GFETs, which consists of two gates (top and back gate), a large area graphene sheet as a channel placed on the thick $SiO_2$ back-gate oxide layer (300 nm and 1000nm), where heavily doped silicon wafer act as a back gate. This article emphasizes p-type GFETs, while a similar approach also applies to the n-type GFETs. The $C_{gs}$ and $C_{gd}$ are gate to source and gate to drain capacitance. $R_{ds}$, $R_d$ and $R_s$ are the drain to source resistance, drain resistance and source resistance respectively as shown in Fig. 4.2. (a), This paper produces a fundamental physical model of GFETs for large area graphene (1000nm length, 0.342 thick and 1000nm width (which can be taken even few of micrometre)). V(x) is shown above in Fig. 4.2 (b) as channel voltage, which is variable and depends on x's value from 0(0) to L ($V_{Ds}$). While $C_t$, $C_b$ and $C_q$ are top gate capacitance, back gate capacitance and, quantum capacitance respectively and $V_{gs_t}$ and $V_{gs_b}$ applied internal voltages. $V_{ds}$ and $V_{BG}$ are the externally applied drain to source and back gate voltage. A small signal equivalent circuit of the proposed GFETs is also shown in Fig.4.2 (c) where $R_s$, $R_d$ and $R_g$ are the source, drain and gate resistance respectively.

### 4.2.2 Formulation of charge carrier sheet density ($\rho_{gr}$) and quantum capacitance calculation ($C_q$)

2-D Energy and wave vector relation for the mobile $\pi$ electrons in graphene can be formulated [81] as $E(k) = s\ h\ v_f|k|$ while s is equal to +1 in the conduction band and equal to -1 in valance band for the first Brillouin zone (BZ) in graphene layers. Where (h) is the reduced form of Planck's constant and Fermi velocity ($v_f$) is of high magnitude equal to $1x10^8$cm/s along with $|k|$ a 2D x-y plane wave vector at the origin $|k| = 0$ is referred to "Dirac point."

Each Dirac point is double fold spin degeneracy $g_s$ = 2 and contains double valley $g_v$ = 2, thus the number of states in a graphene layer is

$$N(E) = g_s g_v \frac{Ak^2}{4\pi(\hbar v_f)^2} \quad (1)$$

here A is an area of the particular layer since the linear charge density of states [82] for an intrinsic graphene layer is a differential form of the number of the state of the particular layer concerning the energy of the particular states, which can be expressed as,

$$\rho_{gr} = \frac{1}{A}\frac{dN}{dE} = \frac{2}{\pi}\frac{|E|}{(\hbar v_f)^2} \quad (2)$$

and so, to calculate the charge carriers (hole) concentration in a 2D graphene sheet based on fundamental physics can be formulated as

$$p = \int_{-\infty}^{Ecv} \rho_{gr}(E)[1 - f(E)]dE \quad (3)$$

after replacing f(E) as the Fermi-Dirac distribution function and $\rho_{gr}(E)$ too, the no. of holes in the graphene sheet can be written as follows, where $Ecv$ work as reference energy (i.e., it will be taken $Ecv = 0$)

$$p = \int_{-Ecv}^{\infty} \frac{2}{\pi}\frac{|E|}{(\hbar v_f)^2}\left[\frac{1}{exp\frac{(E+E_F)}{K_B T}+1}\right]dE \quad (4)$$

similarly, no. of the electron in graphene channel concerning field dependent charge carrier can be represented as

$$n = \int_{0}^{\infty} \frac{2}{\pi}\frac{|E|}{(\hbar v_f)^2}\left[\frac{1}{exp\frac{(E-E_F)}{K_B T}+1}\right]dE \quad (5)$$

Thus, the total charge ($Q_{net}$) is equal to $(p - n)$ and could be utilized to estimate total charge sheet density $Q_{gr}$, which is equal to $q * (p - n)$ as follows

$$Q_{gr} = \frac{2}{\pi}\frac{q|E|}{(\hbar v_f)^2}\int_{0}^{\infty}\left[\frac{1}{exp\frac{(E-E_F)}{K_B T}+1} - \frac{1}{exp\frac{(E+E_F)}{K_B T}+1}\right]dE \quad (6)$$

the quantum capacitance of the proposed device is $\mathrm{C_q}$ which can be calculated [80] as the differential of the channel sheet charge density $Q_{gr}$ with respect to $V_{gr}$, where $V_{gr}$ is graphene channel voltage

$$\mathrm{C_q} = -\frac{\mathrm{d}Q_{gr}}{\mathrm{d}V_{gr}} \tag{7}$$

while the minus sign here reflects the impact of more and more positive voltage applied to gate directly increasing the positive channel voltage i.e. more negative charge results in the graphene layer.

$$\mathrm{C_q} = -\frac{\mathrm{d}}{\mathrm{d}V_{gr}}\left\{\frac{2}{\pi}\frac{q|E|}{(\hbar v f)^2}\int_0^{\infty}\left[\frac{1}{exp\frac{(E-E_F)}{K_BT}+1}-\frac{1}{exp\frac{(E+E_F)}{K_BT}+1}\right]dE\right\} \tag{8}$$

To solve the integral term in the above equation, take constants outside and substitute exponential term $exp\frac{(E \pm E_F)}{K_BT} \pm 1$ by x and $dE$ by $\frac{K_BT}{x}dx$ we get simplified equation as

$$\mathrm{C_q} = -\frac{\mathrm{d}}{\mathrm{d}V_{gr}}\left(\frac{2}{\pi}\frac{q}{(\hbar v f)^2}\right)\left\{\left[\int_A^{\infty}|K_BTlnx - E_F|\frac{1}{x} * \frac{K_BT}{x}\right]dx - \left[\int_B^{\infty}|K_BTlnx + E_F|\frac{1}{x} * \frac{K_BT}{x}\right]dx\right\} \tag{9}$$

a simplified quantum capacitance formulated above in equation (9) can be rewritten as

$$\mathrm{C_q} = -\frac{\mathrm{d}}{\mathrm{d}V_{gr}}\left(\frac{2}{\pi}\frac{q}{(\hbar v f)^2}\right)\{part\ A' + Part\ B'\} \tag{10}$$

by dividing integral into two parts and naming as $part\ A'$and $Part\ B'$ as

$$\int_A^{\infty}|K_BTlnx - E_F|\frac{1}{x} * \frac{K_BT}{x}dx \tag{11}$$

$$\int_B^{\infty}|K_BTlnx + E_F|\frac{1}{x} * \frac{K_BT}{x}dx \tag{12}$$

where A is exp ($E_F/K_BT$ + 1) and B is exp (-($E_F/K_BT$ + 1)), so after putting limits in exponential term and replacing x = 0 and by solving Eqn. (11) and (12) by two-part integral substitution method we get a combined solution for both $part\ A'$and $Part\ B'$ and further depends on the

positive and negative the sign as given in Eqn. (13), where $K_B T ln x \pm E_F$ as part I and $\frac{1}{x} * \frac{K_B T}{x}$ as part II,

$$\int_{A,B}^{\infty} |K_B T ln x \pm E_F| * \frac{1}{x} * \frac{K_B T}{x} dx \tag{13}$$

Now assuming $E_F$ as constant since $E_F = q.V_{ch}$ and by following standard mathematical rules to solve this integral and after applying limits we get solved part as given below

$$\frac{(K_B T)^2}{A}(lnA + 1) - E_F \frac{(K_B T)}{A} \tag{14}$$

similarly, after solving part II

$$\frac{(K_B T)^2}{B}(lnB + 1) + E_F \frac{(K_B T)}{B} \tag{15}$$

Now by sum-up $part\ A'$and $Part\ B'$, one could represent a solved integral in quantum capacitance as follows

$$\mathrm{C_q} = -\frac{\mathrm{d}}{\mathrm{d}V_{gr}}\left(\frac{2}{\pi}\frac{q}{(\hbar v f)^2}\right)\left\{\left[\frac{(K_B T)^2}{A}(lnA + 1) - E_F \frac{(K_B T)}{A}\right] - \left[\frac{(K_B T)^2}{B}(lnB + 1) + E_F \frac{(K_B T)}{B}\right]\right\} \tag{16}$$

By substituting the value of A and B, and after performing some basic algebraic mathematics, the quantum capacitance can be represented in a simple formula as given below

$$\mathrm{C_q} = -\frac{\mathrm{d}}{\mathrm{d}V_{gr}}\left(\frac{2}{\pi}\frac{q}{(\hbar v f)^2}\right)\left\{\left[\frac{(K_B T)^2}{exp\frac{(E_F)}{K_B T}+1} - \frac{(K_B T)^2}{exp\frac{(-E_F)}{K_B T}+1}\right]\right\} \tag{17}$$

By making further mathematical efforts to the above exponential terms and replacing them by the hyperbolic trigonometric formula's quantum capacitance could be present as

$$\mathrm{C_q} = -\frac{2q}{\pi}\frac{(K_B T)^2}{(\hbar v f)^2}\frac{d}{dV_{gr}}\left[\frac{2sinh\frac{qV_{gr}}{K_B T}}{2\left(1+cosh\frac{qV_{gr}}{K_B T}\right)}\right] \tag{18}$$

By using reverse engineering, we can write quantum capacitance [42] even more simplified as given in logarithmic term

$$\mathrm{C_q} = -\frac{2q}{\pi}\frac{qV_{gr}K_BT}{(\hbar vf)^2}\ln\left[2\left(1+cosh\frac{qV_{gr}}{K_BT}\right)\right] \tag{19}$$

For the $q\,V_{gr} \gg K_BT$ condition, Eqn. (19) will be simplified to the following single term formula

$$\mathrm{C_q} = -\frac{2q^2}{\pi}\frac{q|V_{gr}|}{(\hbar vf)^2} \tag{20}$$

As like total charge density in Eqn. (6) has been used to formulate quantum capacitance accurately, channel voltage $V_{gr}$ and quantum capacitance $\mathrm{C_q}$ have useful significance to formulate $\rho_{gr}$. So, that by using basic mathematics technique of two equations and two variable drain current can be formulated by using $\rho_{gr}$.

$$Q_{gr} = -\int \mathrm{C_q} * dV_{gr} = -\frac{1}{2}\,\mathrm{C_q}V_{gr} \tag{21}$$

$$\rho_{gr} = \frac{Q_{gr}}{q} = \left|\frac{-\frac{1}{2}CqV_{gr}}{q}\right| \tag{22}$$

while channel voltage $V_{gr}$ directly can be calculated by using basic technique KVL and KCL form the given Fig. 2 (c) and can be expressed as

$$V_{gr} = \frac{1}{\mathrm{C_t} + \mathrm{C_b} + 0.5\,\mathrm{C_q}}\{[V_{gs_t} - V(x)]C_t - [V_{gs_b} - V(x)]C_b\} \tag{23}$$

The pre-factor of $\frac{1}{2}$ with $C_q$ is because of its dependency on $V_{gr}$ and now by putting Eqn. (23) in Eqn. (22) we get a simple a second order algebraic Eqn.

$$C_q{}^2 + (C_t + C_b\,)C_q - [V_{gs_t} - V(x)]C_t - [V_{gs_b} - V(x)]C_b = 0 \tag{24}$$

Thus by rearrange the equation we get a quadratic equation of $C_q$ in terms of $V_{gs_t}$, $V_{gs_b}$ and $V(x)$. Where $V(x)$ is the channel voltage depending on x (0 to L) and the value of $V(x)$ of at (x = 0) is 0V, while at (x = L) is $V_{ds}$V.

### 4.3 Drain current calculation

For drain current calculation at very first we need to focus on charge charier velocity $v = v(x)$ mainly through the channel (x =0 to L) from (1). A low saturation velocity characteristic is shown by Monte Carlo simulation [82] at the steady state is

$$v = \frac{\mu E}{1+\frac{\mu|E|}{v_{sat}}} \tag{25}$$

Where E represents the electric field, μ is the carrier mobility and $v_{sat}$is saturation velocity at low field. The carrier velocity, especially $v_{sat}$ of graphene channel at the $SiO_2$ platform is strongly affected by rare interfacial scattering of phonons. Experimental work has been talked about the two dominated optical phonons at $SiO_2$ and graphene interface. They have been shown a magnitude of 59meV and 155meV respectively but one can describe this phenomenon by a single phonon only with enough accuracy and with the energy of $\hbar\Omega$. By the approach used [83] to calculate $v_{sat}$, $v_{sat}$ depends on charge carrier sheet density ($\rho_s$) and the phonons effective energy **Ω**.

$$v_{sat} = \frac{\Omega}{\sqrt{\pi\rho_{gr}}} \tag{26}$$

Charge carrier-interaction phenomenon in graphene-MOSFET channel introduces a new term as $0.5 + A.V^2(x)$ [51, 52] to correct the calculation of $v_{sat}$ to one decimal point at the channel drain end. Now Eqn. (26) will become as,

$$v_{sat} = \frac{\Omega}{(\pi\rho_{gr})^{0.5+A.V^2(x)}} \tag{27}$$

here A is a dimensionless important factor of order $10^{-3}$, when $\rho_s$ is of magnitude $10^{12}$ $cm^{-2}$ and the final unit will be cm/s. Now using E = $(-\frac{dV}{dx})$ and Eqn. (20) drain current ($I_d$) becomes

$$I_d = -q\rho_{gr}\frac{\frac{\mu(-\frac{dV}{dx})}{1+\frac{\mu(-\frac{dV}{dx})}{v_{sat}}}}{}W \tag{28}$$

after integrating left side 0 to x and 0 V to $V_{ds}$V right side, since $V = V(x)$, is a function of the channel length and by changing the variable of separation $I_d$ becomes. Because the pristine graphene layer and GFET graphene channel are two different forms of material, graphene as channel deals with scattering and inhomogeneity of the electrostatic potential. Two pivotal elements must be counted in the drain current: the first is the effect of the inhomogeneity of the electrostatic potential [84, 85] and the second is the interface trap states that will contribute to the DOS of large-area graphene, which also cause scattering nonlinearity characteristics [62, 63].

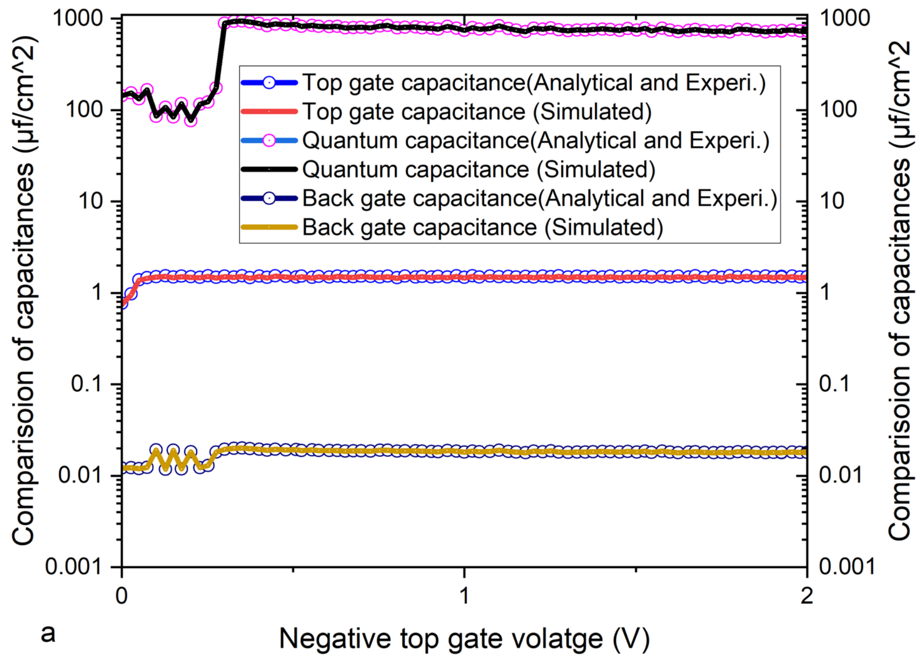
$$I_d = q\mu W\frac{\mu\int_0^{V_{ds}}\rho_{gr}dV}{L-\mu\int_0^{V_{ds}}\frac{1}{v_{sat}}dV} \tag{29}$$

$$I_d = -\frac{\mu W}{2L_{eff}} * \frac{C_t}{C_t + C_b + 0.5\, C_q}\{(V_{gs_t} - V(x)/2) - (V_{gs_b} - V(x)/2)\} \tag{30}$$

$$L_{eff} = L - \frac{\mu}{\Omega}\left\{\left[\log\left(\frac{\pi C_q}{2q}\right) + \log[(V_{gs_t} - V_{ds})C_t + (V_{gs_b} - V_{ds})C_b]\right] * \left[0.5\, V_{ds} + \frac{A\, {V_{ds}}^3}{3}\right] + \right.$$
$$\left.\int_0^{V_{ds}} \{(\frac{2q}{\pi C_q}) + \frac{(C_t+C_b)}{[(V_{gs_t} - V_{ds})C_t + (V_{gs_b} - V_{ds})C_b]}\} * \left[0.5\, V_{ds} + \frac{A\, {V_{ds}}^3}{3}\right]\right. \tag{31}$$

### 4.4 Results and Discussion

To investigate the quantum capacitance effect on gate capacitance, a basic MOS structure without the back gate of oxide thickness (300nm) and top gate oxide of the thickness (3nm,), zero voltage as $V_{gs_t}, V_{gs_b}$ and $V_{Ds}$ is arranged for the proposed GFETs model. Quantum capacitance of the single layer GFETs is presented in this analytical model enhanced and impact the overall gate capacitance concerning the relation $C_q = C_{ox} * C_q/(C_q + C_{ox})$.



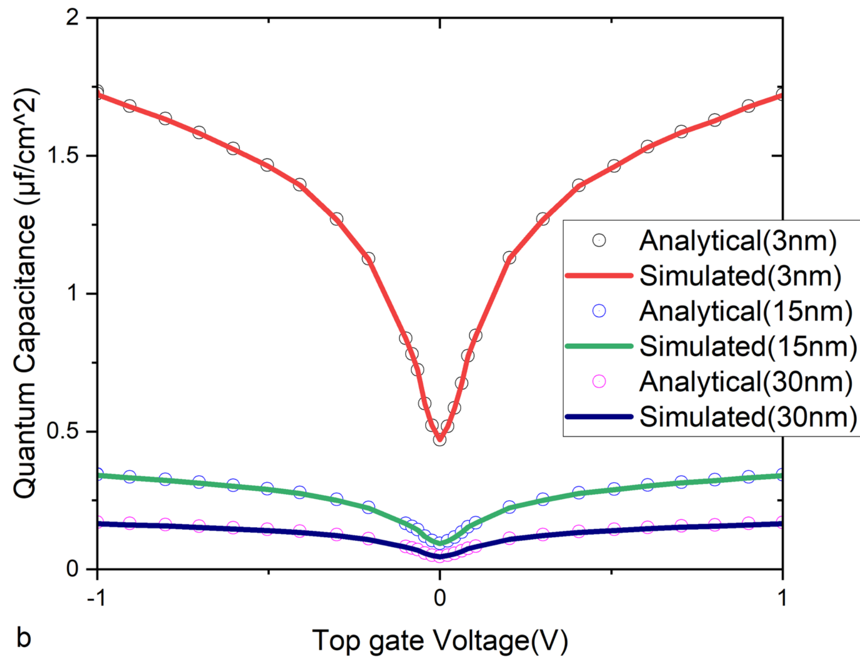
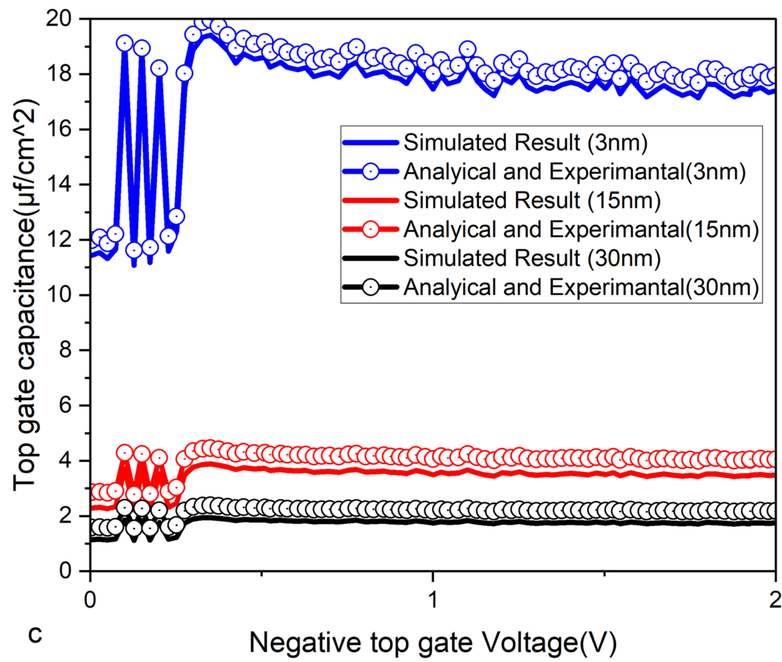




Figure 4.3(a, b) Quantum capacitance effect on overall gate capacitance vs gate voltage. Fig. 4.3.a presents the comparative results of the capacitance; a comparison of analytical model results is done with simulation results and with the experimental results [78]. Fig. 4.3. b the quantum capacitance investigated at different top gate oxide thicknesses (3nm, 15nm, and 30nm).



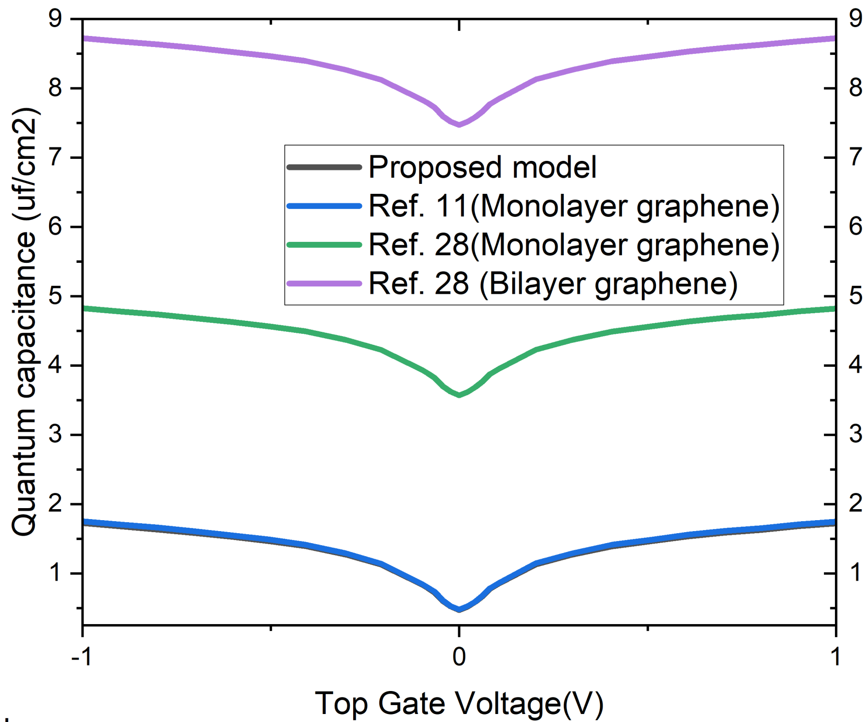




Figure 4.3 (c, d) Quantum capacitance effect on overall gate capacitance vs gate voltage. Fig. 4.3.c top gate capacitance of the proposed model is investigated with respect to the top gate oxide thickness (3nm, 15m, and 30nm). Fig 4.3.d quantum capacitance is compared with different GFET structures at 1000nm channel length.

One of the most significant aspects of nanometer technology GFETs is that quantum capacitance plays a pivotal role in device characterization. Fig. 4.3 elaborate graphically on how the quantum capacitance influence the total gate capacitance at 300nm and 1000nm channel length. The proposed model provides better numerical values of Cq (1.5 f/cm^2 for the proposed model while for experimental results it is comparative and for other GFET structures is much higher as shown in graph 4.3.d) at the 1000nm channel length. The insight investigation of proposed model capacitances (top gate and quantum capacitance) at different top gate oxide thicknesses is presented in figure 4.3. The numerical valve and impact of quantum capacitance are increasing with decreasing in the top gate oxide thickness (ranges) 30nm to 3nm). The comparison of Quantum capacitance (Fig. 4.3.d) of the proposed model with the experimental result is done at 1000nm, H (56meV), and with the monolayer graphene H(55meV). Thus, the simulated results (with line) and analytical (with symbol) are comparable to the available literature. Table 1 explains the numerical values of all significant parameters and dimensions of the GFETs model.

Table 4.1 Dimensions and parameters of the modeled GFETs devices

| **Parameter** | **GFET 1 [78]** | **GFET 300nm(proposed)** |
|---|---|---|
| **L (μm)** | 1 | .3 |
| **W (μm)** | 2.1 | 2.1 |
| **$t_{ox}$ (nm)** | 15 | 15 |
| **$t_{box}$ (nm)** | 285 | 285 |
| **$V_{gs\text{-}top}$ (V)** | 1.45 | .95 |
| **$V_{gs\text{-}back}$ (V)** | 2.7 | 2.7 |
| **p** | $1.5*10^{12}$ | $3*10^{12}$ |
| **$\mu_n$ ($cm^2$/V.s)** | 1500 | 2500 |
| **$\mu_p$ ($cm^2$/V.s)** | 1500 | 2500 |
| **H (meV)** | 56 | 99 |
| **λ (nm)** | 10-100 | 100-300 |

Fig. 4.4 and Fig. 4.5 have explained graphically the transfer characteristic and output characteristic of the proposed GFETs model and compare it with the experimental work [78] mentioned as GFET1 in table 1. GFET1 features a high dielectric 2D gate material $HfO_2$ on exfoliated graphene channel and $SiO_2$ is the back-gate dielectric. The output characteristic of the proposed model in Fig. 4.5, has been shown to coherence with the [78], with the applied voltage at source (0V), negative drain voltage (-2 to 0V), top-gate (sweep from -0.75 to 0.75 V) as it can easily view in a graph with the back-gate voltage of -40 V. In the same manner transfer characteristic of the GFETs both analytical and simulated is compared with [78] in Fig. 4.5. The nonlinearity characteristic behaviour of the GFET at 300nm channel has been shown in Fig. 4.4, 4.5 and 4.6. Dirac-point shift has been shown in Fig.4.4 after applying an external gate to source voltage for single-layer graphene, while for the conventional MOSFETs Dirac point has the same contact point of Conduction and valance band.

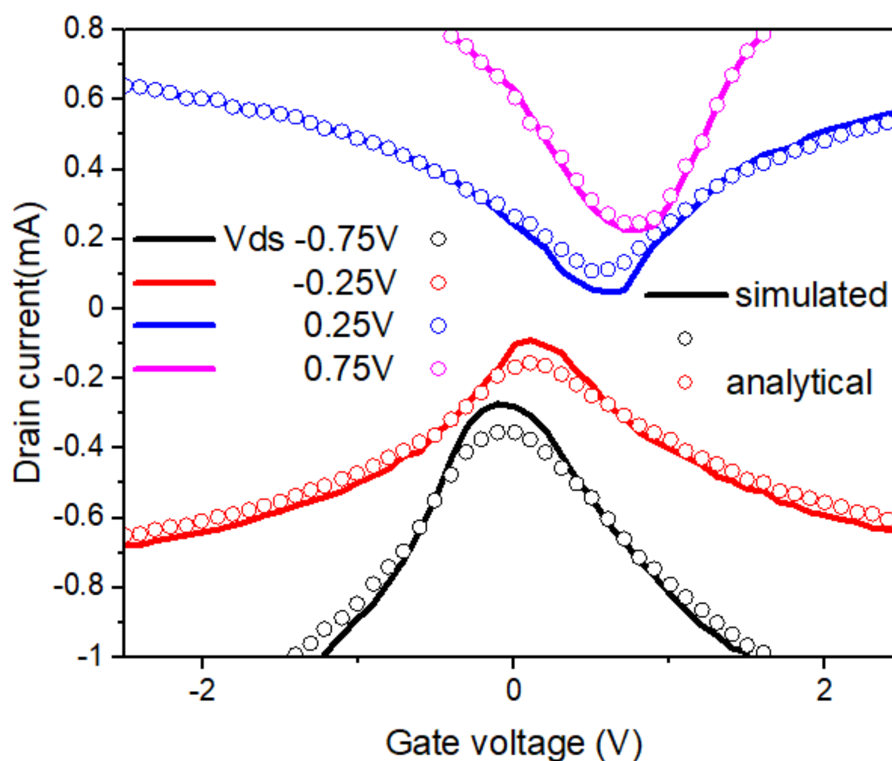
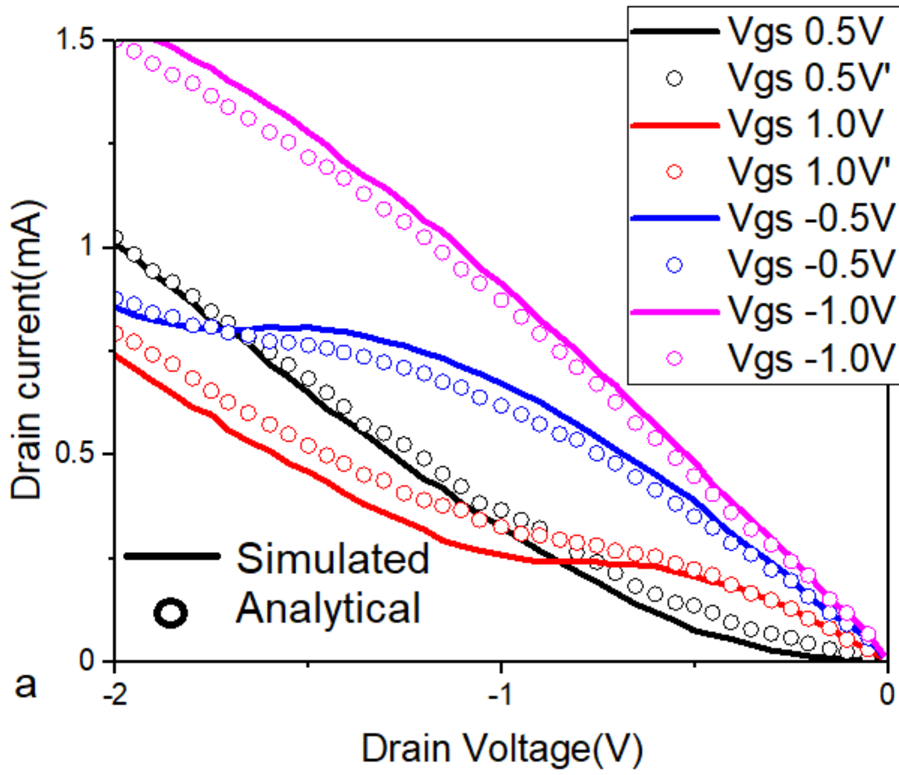
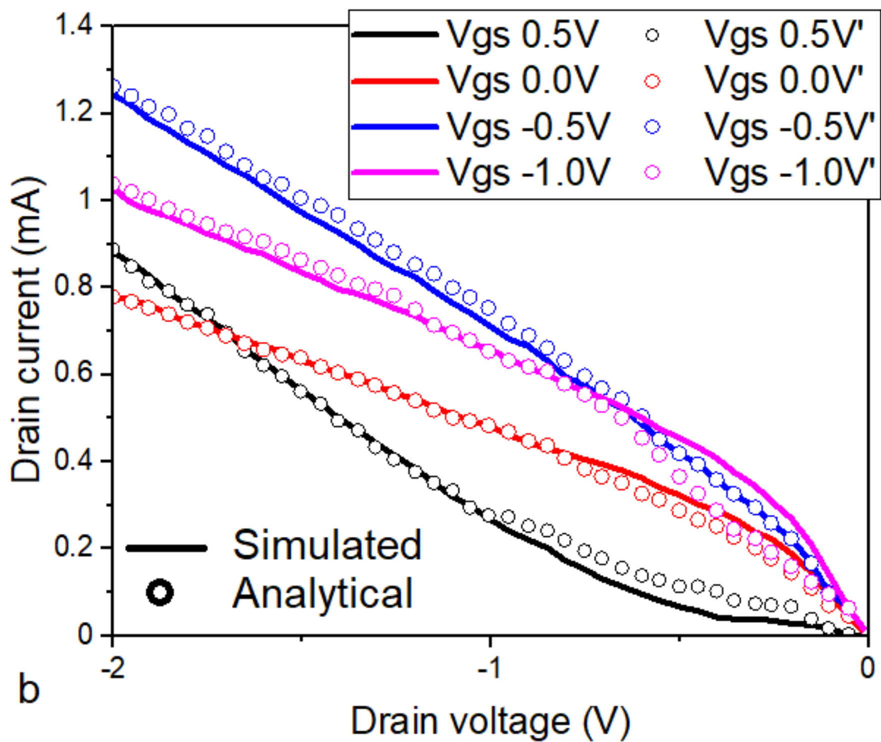
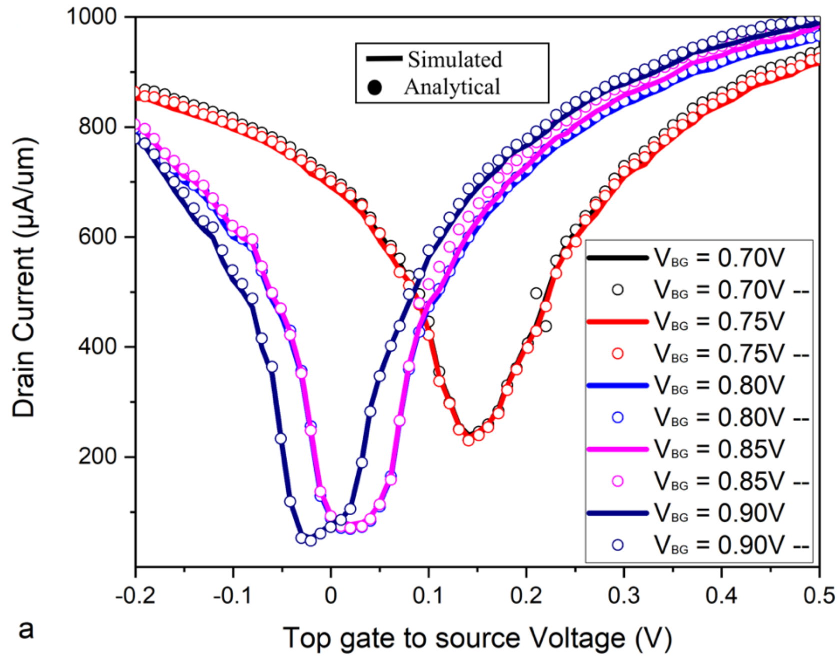



Figure 4.4 Transfer characteristic of the proposed model i.e. drain current vs top-gate voltage for the proposed GFETs model.




Figures 4.5. a and 4.5.b: Output characteristic of the proposed model i.e. drain current vs drain to source voltage for the GFETs model at 1000nm in 4.5. a and 300nm in4. 5. b.



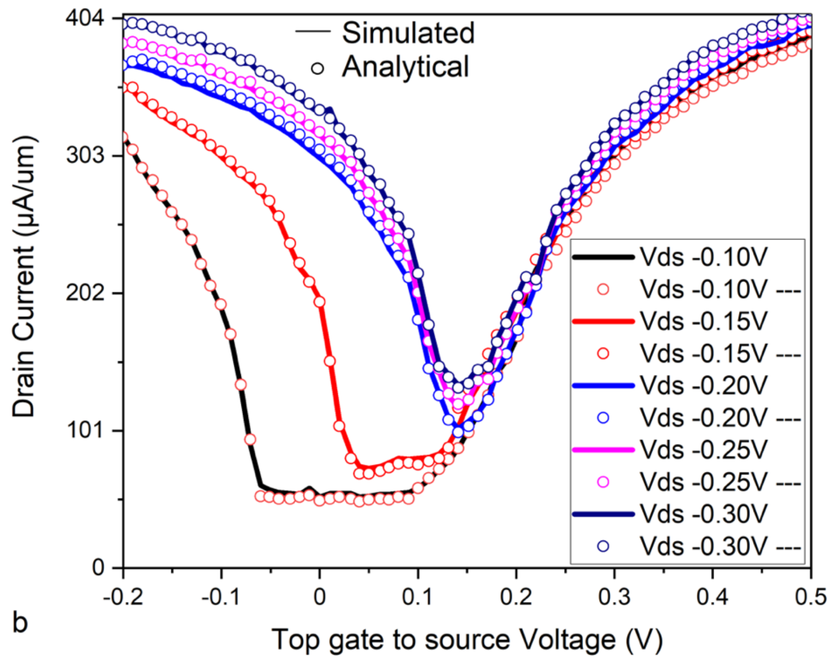




Figure 4.6. a and 4.6. b: Transfer characteristic of the proposed model i.e. drain current vs drain to source voltage for the GFETs model. Top gate control by $V_{ds}$ and back gate control by $V_{BG}$ over drain current are presented in this graph (while for this dual gate control an exception is considered that the graphene sheet is not a large area sheet). $V_{ds}$ and $V_{BG}$ are the externally applied drain to source and back gate voltage.

This Dirac-point shift in transfer characteristic and kink presented in the output characteristics is proof of the nonlinear behaviour of the GFETs. This nonlinear behaviour is tending to enhanced when the channel length of the GFETs is being decreased from 1000nm to 100nm and below that value as is given in the latest accepted paper [80]. The dual gate control is graphically present in Fig. 4.6 at the same time nonlinear behaviour of the GFETs can be observed very easily in Fig 4.6. a and b. Here we concentrate on the nonlinearity of the transfer characteristics of the Proposed model. A flat line drain current has been shown in fig. 4.6. a for -0.1 to 0.1V gate to source voltage and beyond this it has shown gradual increment, which is normal in electronic device characteristic curves but a flat drain current shows a nonlinearity in the transfer characteristic curve.

### 4.5 CHAPTER SUMMARY

A quasi-analytic model for single-layer GFETs with large area graphene is presented. Drain current formulation with velocity saturation effect and role of quantum capacitance over the total capacitance is explained with the precise output and transfer characteristics of the proposed GFET model, which facilitate the readers a simple mathematical GFET model. The effect of enhanced quantum capacitance value at nanometer technology adds nonlinearity to the transfer and output drain characteristics of the proposed GFETs model has been presented. The fitting parameter addition in velocity saturation has improved the drain current characteristic by avoiding the early saturation stage. The modelling and simulation of the GFETs model have presented and compared the results with the well-established experimental work and it will surely befit the reader to understand the basic physic of the GFETs.

# Chapter five

## Nonlinearity, Scaling Trends of Quasi-Ballistic Graphene Field Effect Transistors Targeting RF Applications

### 5.1 INTRODUCTION

GFETs modelling and simulation play an important role in the research and development of the Technology Computer-Aided Design (TCAD) tools which are dedicated to 2D electronic device design. Electronic device designing tools are useful to simulate and develop advanced device structure and circuit applications. Conventional FETs modelling was dedicated to silicon technology only. Since silicon technology-based electronics has reached its scalable limit. Further, channel length scaling for the Si-based MOSFET produces many short channel effects and thermal heat in the integrated circuits (ICs). Thus, for the advancement of technology with time and hilarious research interest in the two-dimensional MOSFET technology recently, graphene is found as a novel electronic material. Graphene is an atomically thick 2D material with exceptional electronic properties. Graphene is the most promising and research interest 2D material for future electronic devices as it has very high electron mobility ($2 \times 10^5$ $cm^2V^{-1}S^{-1}$), [1-3]. While graphene on silicon oxide base degrades its most fascinating properties (very high electron mobility ~ $10^4$ $cm^2V^{-1}S^{-1}$) The literature [4-6] has also reported on the scope of graphene-based high-speed and RF electronics applications. The hexagonal Boron Nitride (hBN) is an appealing and supporting 2D dielectric material that has shown three to four times improved electron mobility ($4 \times 10^4$ $cm^2V^{-1}S^{-1}$) as a comparison to the $SiO_2$ as reported in [7]. Hexagonal Boron Nitride (hBN) as 2D dielectric material also supports improving the RF performance metrics like high-intrinsic transit frequency and unity-power-gain frequency of GFETs. Modelling and simulation of the graphene FETs with a base as Sio2/hBN has been reported since the discovery of graphene. Graphene-based FETs

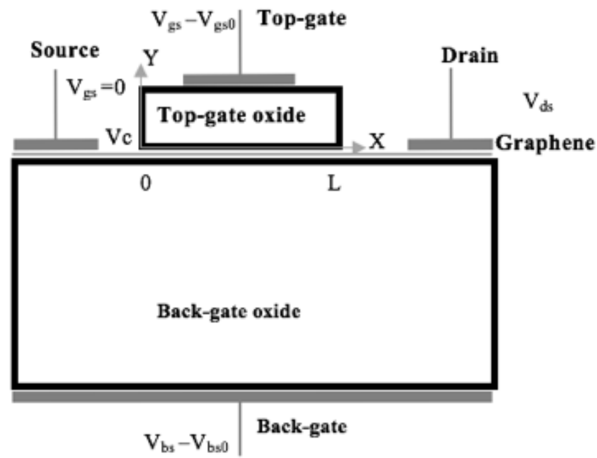
modelling was reported for the very first time as a graphene field effect device in 2007 [38]. Many other GFETs modelling has also reported the intrinsic transit frequency comparable to or higher than similar size CMOS nanometre technology [39-41], some other reports drain current formulation for the GFETs based on drift-diffusion equation [45, 48, 51, 52]. A virtual source technique, basic physics based [43, 44, 46] and quasi-ballistic transport mechanism or MFT based [60-63] also has been reported. Two best-fit transport approaches of an electron through the channel used for the formulation of drain current are Landauer's charge-based and Mckelvey's flux based. The first approach is based on Landauer's charge carrier coherence concept, applicable to only low-level voltage and temperature [60]. The second approach is the Mckelvey flux theory-based. MFT techniques are compatible with standard circuit simulators for circuit designing and they can be used to analyse the GFET Model [62-63]. At the same time, Landauer's approaches discussed above are not sufficient to capture all magnificent regions of GFETs along with quasi-ballistic transport mobility of charge carriers in the atomic size graphene. The focus of the proposed work is quasi-ballistic and ballistic transport GFETs, which explores the very long mean free path (300 ±100nm) for carrier density ~10 $cm^{-2}$ at room temperature with sigma tight bonding leads to collision-free transport i.e. ballistic transport approach [3]. The linearity of the GFET models is also an important performance metric because for RF devices and circuits a very weak signal is processed in presence of strong interference. Since only a few models are reported the linearity and nonlinearity study of the GFETs, such as Static nonlinearity [86] and RF linearity [87] of GFETs explains the nonlinear impact of the single layer graphene at the nanometre technology of diffusive transport approach only. Since the graphene channel is ballistically transported at nm technology, there is scope for the study of nonlinearity for the quasi-ballistic and ballistic GFETs.

This work has been presented in five sections introduction, device structure and simulation setup, static nonlinearity model, result and discussion and conclusion. An appendix is also present in this work defining the explicit drain current expression which is help full to

find the HDs and IMs. The introduction section explains GFET's various modelling and enlightens the scope and research interest for finding the unique and novel way to find the nonlinear study of quasi-ballistic GFETs, which is also a novelty of this work.

### 5.2 DEVICE STRUCTURE AND SIMULATION SETUP

TCAD simulation setup and device structure setup of ballistic and quasi-ballistic GFETs at four different channel lengths (140, 240, 300 and 1000 nm) are done from quasi-ballistic to ballistic transport nature of charge carrier in graphene channel i.e. start from 1000nm which is relatively are quasi-ballistic in nature to 140nm channel length which is ballistic in nature. Thus it is very clear that this entire simulation process is done in four independent steps device structure for 1000nm, 300nm 240nm and 140nm, which follows similar basic device structure formation fundamentals like all of them are four terminal devices with brown colour 500nm thick silicon base on blue/black colour 22nm/10nm back gate contact, 285nm (300-15) thick back gate oxide hBN, atomically thick red colour single-layer graphene and 15nm thick top gate oxide hBN again along with the source, drain and gate contacts similar to the back gate thickness. Figure 5.1.a cross-sectional view of the proposed GFET device with the basic electrostatic parametric details, in figure 5.1. b equivalent capacitance of the GFET model, in figure 5.1.c view of the proposed model GFET with the equivalent capacitance of the GFET model of GFET. Graphene has been modified with the established red colour poly-silicon properties like electron mobility MUN, hole mobility MUP, energy band gap $E_G$ at room temperature and work function.

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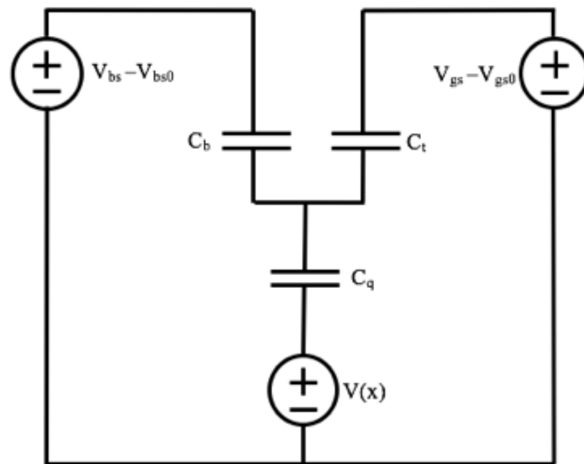


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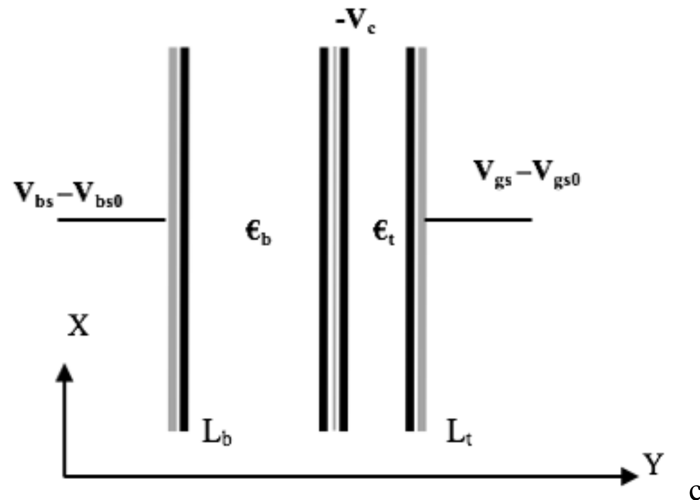


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Figure 5.1.a cross-sectional view of the proposed GFET device with the basic electrostatic parametric details, in figure 5.1. b equivalent capacitance of the GFET model, in figure 5.1.c view of the proposed model GFET with the equivalent capacitance of the GFET model of GFET.

### 5.3 STATIC NONLINEARITY MODEL

The static nonlinearity of GFETs under a quasi-ballistic regime can be calculated by expanding drain current as Taylor series

$$I_{DS} = x_1V_{GS} + x_2V_{GS}^2 + x_3V_{GS}^3 + \cdots + x_nV_{GS}^n \quad (1)$$

where $x_1, x_2 \ldots\ldots x_n$are Taylor's series coefficients and $V_{GS}$ is the gate to source voltage. while draining current [20] formulation based on McKelvey's flux theory (MFT)

$$I_{DS} = \frac{Wn(x)V_{Th}(1-r_{bs})[1-£_1(\omega_F-\omega_{DS})/£_1(\omega_F)]}{(1+r_{bs}(1-r_{bs})£_1(\omega_F-\omega_{DS})/£_1(\omega_F)]} \quad (2)$$

W is here the width of GFET, n(x) is charge carrier concentration in graphene channel as an ensemble of field-dependent charge carrier density, $n_E$ and field independent charge carrier density called residual carrier density. So, the total carrier concentration contributing to the calculation of drain current can be represented mathematically [62] as $n(x) = n_{EF} + n_{Res}$where field dependent density of carrier is of more important at large value of $V_{CH}$ than (q $V_{CH} \gg K_BT$) can be written mathematically [63].

$$n_{EF} = \frac{q\pi(K_BT)^2}{(\hbar vf)^2} + \frac{(q)^3V_{CH}|V_{CH}|}{\pi(\hbar vf)^2} \quad (3)$$

with the usual meaning of symbols, field independent charge carrier is also an ensemble of thermally excited ($n_i$) and electron-hole puddles adding carriers [91].

$$n_{pud} = \frac{2}{\pi(\hbar vf)^2}(\Delta^2/2 + \pi^2(K_BT)^2/6) \quad (4)$$

and 2D degenerated thermal velocity $V_{Th}$ of graphene layers is found independent of $V_{GS}$ (gate to source voltage), which can be arranged in equations [90] $V_{Th-2D} = V_{Th}\sqrt{\pi}/2$ after putting 2 for (2D) graphene sheet. Now the next element of drain current is backscattering coefficient $r_{bs}$, is another parameter independent of $V_{GS}$ directly, and can be solve mathematically as [50, 63]

$$r_{bs} = \frac{\left(\frac{1.5\, V_{ds}\mu_{eff}}{2LK_BT\lambda}\right)}{\frac{q|E|}{2K_BT}\left(1+\coth\left(\frac{Lq|E|}{2K_BT}\right)\right)+\lambda^{-1}} \tag{5}$$

with λ as the mean free path in the graphene channel which can be formulated mathematically as $\lambda = \hbar\mu(\sqrt{\pi n}/2)$. Where symbols have their usual meaning. $\mu_{eff}$ is the quasi-ballistic phenomenal effective mobility given by Matthiessen's rule [88], which could be described mathematically as

$$\frac{1}{\mu_{eff}} = \frac{1}{\mu_0} + \frac{1}{\mu_B} \tag{6}$$

where $\mu_0$ is $16\epsilon_g(\hbar vf)^2/q^3 n_{imp}$ formulated in [92, 93] i. e. this part of mobility is inversely proportional to the injected impurity and has the important role of scattering. Now the ballistic transport contributing mobility $\mu_B$ is $q\ L\ /m * V_{Th-2D}$ i. e. ballistic phenomenal mobility is inversely proportional to the thermal velocity. So, it is very obvious that total or effective mobility depends on both factor impurity as well as very thermal velocity into the two-dimensional material graphene and is independent of the gate to source voltage $V_{GS}$. One more parameter in drain current is $£_1(\omega_F - \omega_{DS})/£_1(\omega_F)$, is the Fermi-Dirac integral of order one defined by Blakemore. Where $\omega_F$ is equal to $(E_F\ - E_C)/K_BT$ and $\omega_{DS}$ is equal to $(qV_{DS})/K_BT$ with $E_F$ is equal to $qV_{CH}$. So, first $\omega_F$ Fermi-Dirac integral is also depending upon the gate to source voltage $V_{GS}$. The additional and interesting fact is that $V_{CH}$ is one more parameter depends on $V_{GS}$in the drain current formulation [89], which could be elaborate mathematically as a function of parametric capacitances in the channel of 2D GFET.

$$I_{DS} = \frac{A\left(B+CV_{CH}^2(x)\right)(1-r_{bs})[1-£_1(\omega_F-\omega_{DS})/£_1(\omega_F)]}{(1+r_{bs}+(1-r_{bs})£_1(\omega_F-\omega_{DS})/£_1(\omega_F)]} \tag{8}$$

where A, B and C are constants of value $W.V_{Th}$, $q\pi(\ K_BT)^2/3(\hbar v_F)^2$ and $q^3/\pi(\hbar v_F)^2$ are respectively when all elementary constant has their usual meaning. Note that here in (7) the carrier density n(*x*) parameter includes Electric field dependent and independent but for the further calculation only $n_{EF}$ part is used and residual carrier density to minimize the leakage

current. By simplifying and modifying the drain current (8) in the appendix and using (7) a direct relationship between the gate voltages and reference voltages can be modelled as

$$I_{DS} = \frac{AB+AC\left(\frac{1}{C_{tox} + C_{box} + 0.5\,C_q}(V_{gs_{top}} - \frac{\dot{V}(x)}{2})C_{tox} - (V_{gs_{back}} - \frac{V(x)}{2})C_{box}\right)^{2} P[R]}{[(1+P-Q)(R)]} \quad (9)$$

where P, Q and R, are fitting parameters, $\frac{1.5\,V_{ds}\mu_{eff}}{2L\,K_B T\lambda}$, $\frac{1.5\,V_{ds}\mu_{eff}}{(2L\,K_B T\lambda)^2}$and $exp - \frac{V_{ds}}{K_B T}$, respectively function of drain voltage, effective mobility, mean free path and Channel length as mention in appendix with details.

Linearity and nonlinearity of GFET under ballistic transportation phenomenon, as stated above in (1) can be calculated by differentiating the drain current ($I_{DS}$) concerning gate to source voltage ($V_{GS}$). Thus, finding the coefficient of the Taylor series to elaborate the nonlinearity of GFET as reported by S. Rodriguez [86] can be done in this way $(V_{gs} - V_{gs0} - V_{ds})$. The unknown coefficients of Taylor's series can be found by simply differentiating the drain current equation of the Bilayer GFET. Taylor's series $(X_1, X_2, X_3)$ coefficients can be used further to formulate the harmonic distortion (HD) and intermodulation Distortions as follows

$$x_1 = \frac{\delta I_{DS}}{\delta V_{GS}}\bigg| = \frac{AC(2V_{gs_{top}} * C_{tox}^2 + 2V_{bs_{back}} * C_{box}^2 - 2V_{gs_{top}} * C_{tox} * 2V_{bs_{back}} * C_{tox})P[R]}{C_{tox} + C_{box} + 0.5\,C_q[(1+P-Q)(R)]} \quad (10)$$

$$x_2 = \frac{\delta 2 I_{DS}}{\delta V3_{GS}}\bigg| = -\frac{AC(2C_{tox}^2 + 2C_{box}^2 - 2V_{gs_{top}} * C_{tox} * 2V_{bs_{back}} * C_{box})P[R]}{C_{tox} + C_{box} + 0.5\,C_q[(1+P-Q)(R)]} \quad (11)$$

$$x_3 = \frac{\delta 3 I_{DS}}{\delta V3_{GS}}\bigg| = \frac{AC(2*2C_{tox} * C_{box})P[R]}{C_{tox} + C_{box} + 0.5\,C_q[(1+P-Q)(R)]} \quad (12)$$

these coefficients can be used for further calculation regards finding the nonlinearity for the quasi-ballistic transport approached GFET, which can represent mathematically as harmonic distortion and intermodulation of the order first, second and third as follows. Since order one is the basic and useful information of the device model so harmonic distortion of the second order is

$$\mathrm{HD}_2 = \frac{1}{2}\left|\frac{x_2}{x_1}\right| V_{GS} = \frac{(2C_{tox}^2+2C_{box}^2-2V_{gs_{top}}*C_{tox}*2V_{bs_{back}}*C_{box})V_m}{(2V_{gs_{top}}*C_{tox}^2+2V_{bs_{back}}*C_{box}^2-2V_{gs_{top}}*C_{tox}*2V_{bs_{back}}*C_{tox})} \quad (13)$$

and the harmonic distortion of third order is

$$\mathrm{HD}_3 = \frac{1}{4}\left|\frac{x_3}{x_1}\right| V_{GS}^2 = \frac{(C_{tox}*C_{box})V_m^2}{(2V_{gs_{top}}*C_{tox}^2+2V_{bs_{back}}*C_{box}^2-2V_{gs_{top}}*C_{tox}*2V_{bs_{back}}*C_{tox})} \quad (14)$$

Similarly, to find the intermodulation distortion of order one is very simple and so intermodulation distortion of order second is

$$\mathrm{IM}_2 = \left|\frac{x_2}{x_1}\right| V_{GS} = \frac{(2C_{tox}^2+2C_{box}^2-2V_{gs_{top}}*C_{tox}*2V_{bs_{back}}*C_{box})V_m}{(2V_{gs_{top}}*C_{tox}^2+2V_{bs_{back}}*C_{box}^2-2V_{gs_{top}}*C_{tox}*2V_{bs_{back}}*C_{tox})} \quad (15)$$

And the intermodulation distortion of third order

$$\mathrm{IM}_3 = \frac{3}{4}\left|\frac{x_3}{x_1}\right| V_{GS}^2 = \frac{3(C_{tox}*C_{box})V_m^2}{4(2V_{gs_{top}}*C_{tox}^2+2V_{bs_{back}}*C_{box}^2-2V_{gs_{top}}*C_{tox}*2V_{bs_{back}}*C_{tox})} \quad (16)$$

### 5.4 RESULT AND DISCUSSION

The nonlinear study of the quasi-ballistic GFETs can be done statically as well as by the observation of potential performance at high frequency. The high-frequency performance of GFETs gets affected due to the presence of the parasitic capacitances at short channel length that adds a nonlinearity effect to the GFETs characteristic. The above section explains static nonlinearity in mathematical equations and this section present and validates the graphical and tabular form of the nonlinearity of the GFETs under the quasi-ballistic regime in a very novel way. Nonlinearity affects and influences the GFETs performance by the addition of harmonic and intermodulation distortions, which results in lowering the gain of the GFETs, shifts in the DC offsets, and cross modulation of the AM/PM, etc.

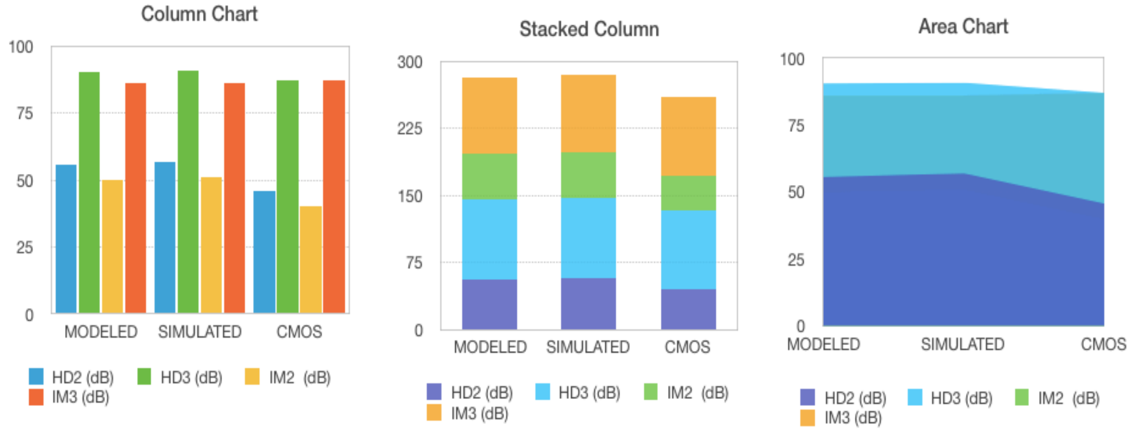


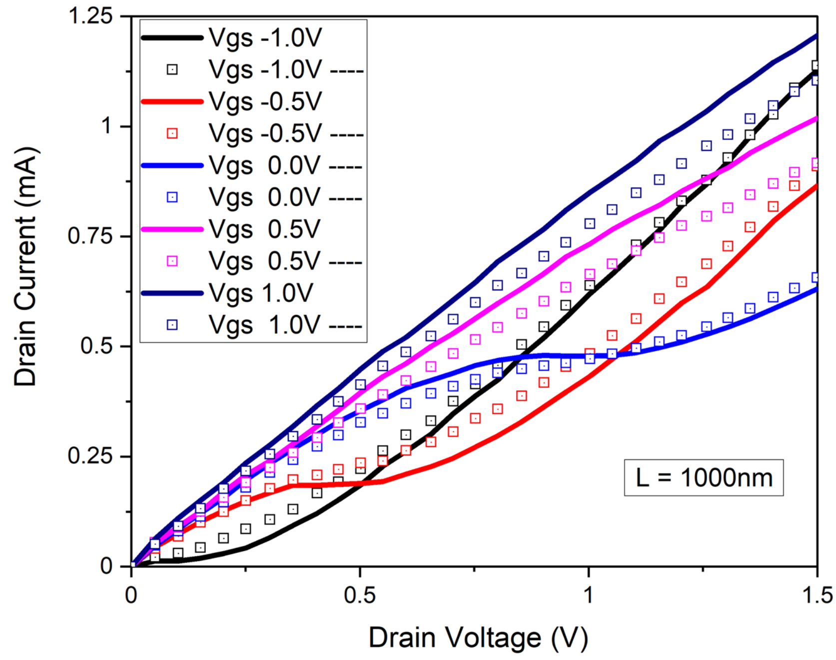

Figure 5.2: Non-linear behaviour of the bilayer graphene field effect transistors (GFET) shown with bar graph as the static nonlinearity by the column, stacked and area chart for the proposed modelled, and CMOS field effect devices.

Table 5.1 listed the nonlinearity characteristics of the high-frequency operation of GFETs.

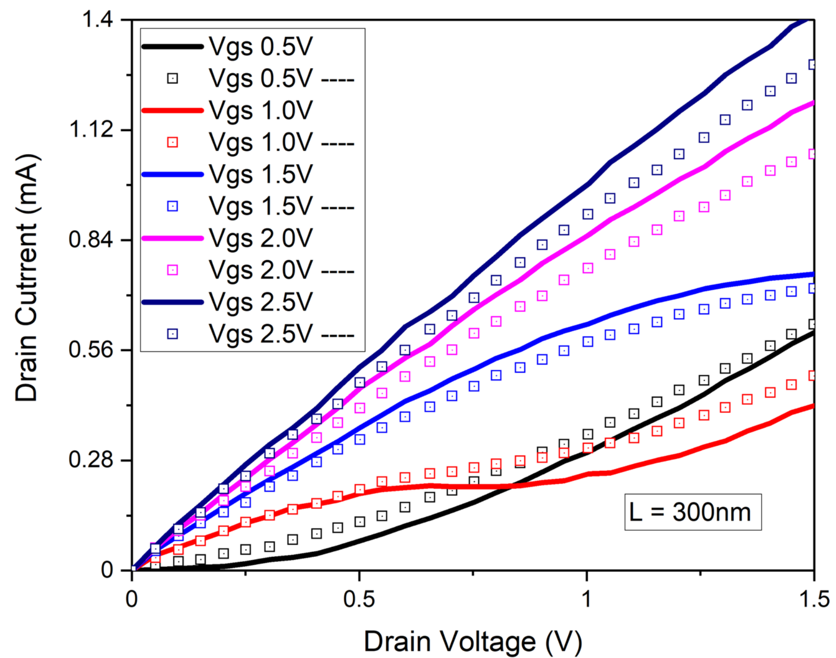
| **Ref.** | **Operating Frequency** | **IIP3 (dBm)** | **Conversion loss (dB)** | **L(um)** |
|---|---|---|---|---|
| [94] GFET RF MIXER | 10MHz | 13.8 | ~30 to 40 | 2 |
| [95] GFET MIXER | 30GHz | 12.8 | 19 | 0.5 |
| [96] GFET MIXER | NA | 4.9 | 20-22 | 1 |
| [97] GFET MIXER | NA | 22 | ~15 | 0.25 |
| [97] GFET MIXER | NA | 27 | 10 | 2 |
| [98] graphene mixer | 2GHz | 19 | 5 | 0.75 |
| [99] RF amplifier | 4.3GHz | 30 | 10 | 0.24 |
| [100] Linearity of GFETs | 300MHz | 20 | 15 | 0.5 |
| [101] Linearity of GFETs | NA | 17 | 17 | 2.4 |
| [87] RF nonlinearity of GFETs | NA | 13.8 | 22 | 0.44 |
| Proposed | 30GHz | 12.6 | 18.4 | 0.14 |
| proposed | 30GHz | 12.8 | 18.8 | 0.30 |

Table 5.1 present and compare the RF nonlinearity characteristic of the GFETs at different channel length and frequency. Table 5.1 also presents IIP3 (input intercept points) of the third order and total gain compression for the available and proposed model. The bar graph given in Fig. 5.2 shows the static and RF nonlinearity by the column, stacked, and area chart for the proposed modelled, and CMOS field effect devices. The analytical outcomes of the proposed GFET model and simulated result values are compared with the CMOS technology with help of harmonic distortions and intermodulation distortions of second order and third order. HDs and IMs are validating the nonlinear character of the proposed ballistic GFET model.

This section validates and compares the dynamic nonlinear characteristic curves of ballistic transport nature GFET at various channel lengths (L = 140, 240, 300, and 1000 nm) as shown in figure 5.3. Nonlinearity effects can be very easily visualized in figure 5.3.a, 5.3.b, 5.3.c, and 5.3.d, at very low gate voltage I-V characteristic curve show nonlinear gradual increment and turn with kinks at a higher value of drain voltage. Characteristic curve crossover for the different gate voltages can be easily seen in figure 3. which is because of these kinks in the I-V characteristic curves. These crossovers in characteristic curves for the increasing gate voltage prove and justify the linearity, scaling and nonlinearity of the characteristic behaviour of drain current of the ballistic approached GFETs. The scaling of channel length and nonlinearity of drain current is very much related as seen in all four graphs of figure 5.3 at various channel lengths of (L = 140, 240, 300, and 1000 nm) for increasing drain to source voltage (from 0 to 2 V). Figure 5.3. a drain current versus drain voltage output characteristic curve is showing the highly nonlinear behaviour of the curve at 1000nm. Figure 5.3. b at 300nm also shows nonlinearity at low (0 to 1V) drain voltage and shows linear shape after 1V drain voltage value. Figure 5.3. c shows the almost linear curve of current and voltage, while a kink is present at 1.25V at a low gate voltage value and this kink is absent at a higher value of gate voltage.

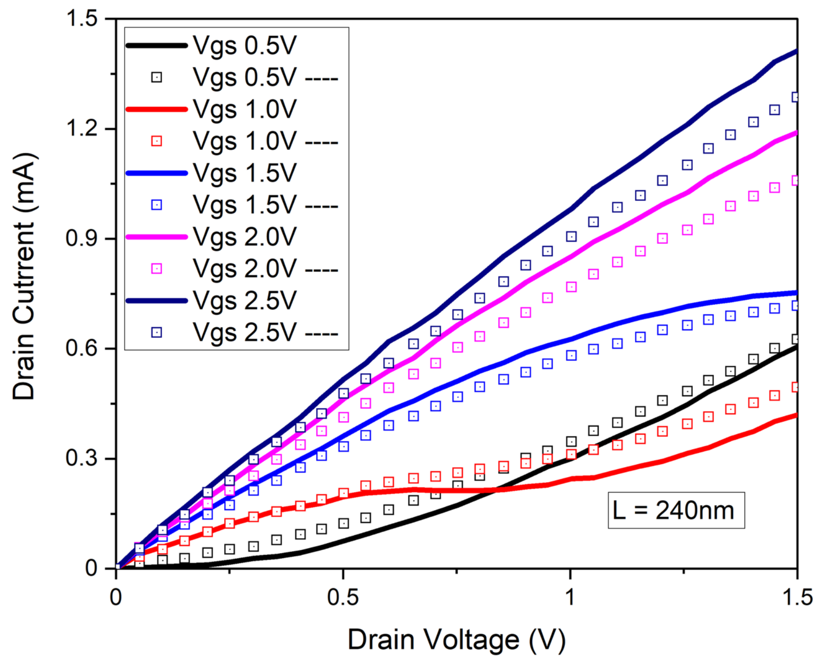



a

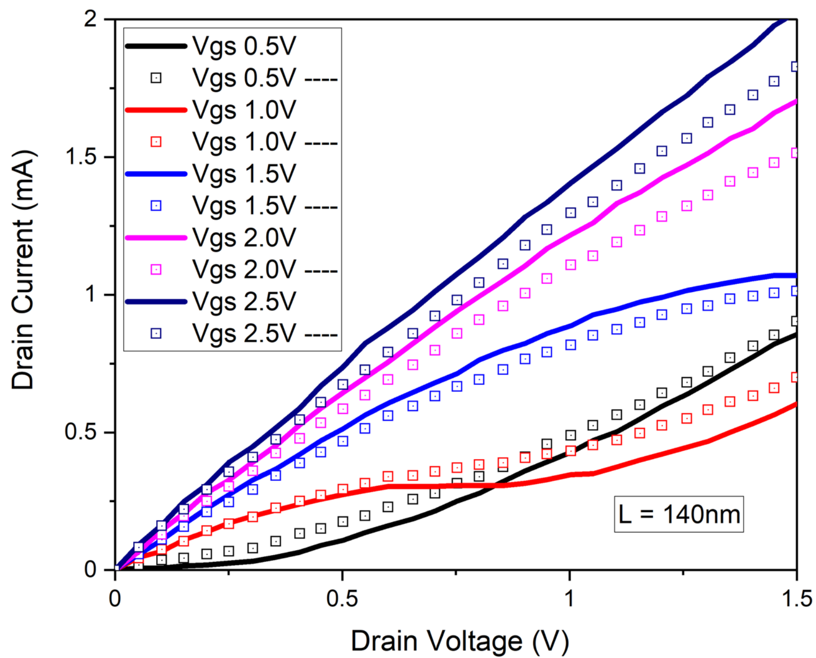



b

Figure 5.3(a,b ) : Non-linear characteristic behavior of the quasi-ballistic GFETs. figure 3. a $I_{ds}$ vs $V_{ds}$ output characteristic curve is showing highly nonlinear behavior of curve at 1000nm. Figure. 3. b at 300nm also shows nonlinearity at low (0 to 1V) drain voltage and shows linear shape after 1V drain voltage value.




c




d

Figure 5.3.c shows the almost linear curve of current and voltage at 240nm, while a kink is present at 1.25V at a low gate voltage value. Figure 3.d is shown the linear curve of output drain current and voltage at all (0 to 2V) drain voltage at 140nm. All the simulated results are shown in figure 3 are drawn by lines while all the analytical outcome values are drawn by squares (symbols).

Figure 5.3. d is shown the linear curve of output drain current and voltage at all (0 to 2V) drain voltage. This work inspired by the static nonlinearity of the non-ballistic transport approach [86], presents the static and dynamic nonlinearity of the quasi-ballistic GFETs model. The validation and comparison have been done with help of bar graphs (figure 5.2), RF frequency nonlinearity table 5.1, and dynamic nonlinearity drains current characteristic (figure 5.3). The dynamic nonlinear characteristic behaviour very well matched and compared with the reported work [42, 81]. All the simulated results are shown in Fig. 5.3 are drawn by lines while all the analytical outcome values are drawn by squares (symbols).

## 5.5 CHAPTER SUMMARY

Since the nonlinearity of the particular devices is a great source of noise in the nanoelectronics device application based on GFETs. So, the linearity and nonlinearity of the ballistic transport approach GFETs is of paramount necessity. Thus, an explicit nonlinearity characteristic behaviour of the ballistic transport approach GFET presented in this work has a significant importance in this advanced nanotech era. This work is a comparison of GFETs at various scaling channel lengths for the proposed model and simulation results in line graph. Higher frequency response of the GFETs model in comparison to conventional MOSFETs technology at the same channel length is the paramount potential of this work.

# Chapter Six

## Conclusion and Future scope

### 6.1 INTRODUCTION

The electronic properties of single layer and bilayer graphene, along with graphene over the hBN layer (gr/hBN heterostructure) are studied and well demonstrated. The electronic band diagram, current density and charge carrier density concerning the thickness of graphene layer over gr/hBN heterostructure have been presented. A quasi-analytic model for single-layer GFETs with large area graphene is presented. Drain current formulation with velocity saturation effect and role of quantum capacitance over the total capacitance is explained with the precise output and transfer characteristics of the proposed GFET model, which facilitate the readers a simple mathematical GFET model. The effect of enhanced quantum capacitance value at nanometer technology adds nonlinearity to the transfer and output drain characteristics of the proposed GFETs model has been presented. Thus, the modelling and simulation of the GFETs model have presented and compared the results with the well-established experimental work and it will surely befit the reader to understand the basic physic of the GFETs.

Since the nonlinearity of the particular devices is a great source of noise in the nanoelectronics device application based on GFETs. So, the linearity and nonlinearity of the ballistic transport approach GFETs are of paramount necessity. Thus, an explicit nonlinearity characteristic behaviour of the ballistic transport approach GFET presented in this work has significant importance in this advanced nanotech era. This work is a comparison of GFETs at various scaling channel lengths for the proposed model and simulation results in a line graph.

## 6.2 Future Scope

### 6.2.1 Design and development of Graphene nanoelectronics real-world electronics devices and circuits

The Design and development of Graphene heterostructure nanoelectronics real-world electronic devices and circuits such as a low sub-threshold digital logic, a high voltage inverter, a static random-access memory, a back gated Bi-GFET with displacement electric field RF mixer with low losses and dual gate Bi-GFET.

### 6.2.2 Temperature and process variability of the GFETs modelling done in my doctorate work

Nonlinearity, Scaling Trends of Quasi-Ballistic GFETs for RF Applications of chapter five is the radio (GHz) frequency static linearity and nonlinearity performance potential analyzed for the ballistic approach GFET under the ballistic transport regime. The proposed model explores close mathematical expressions for Harmonic distortion, intermodulation distortion, and interception points and also depicted them in graphical form with help of Mekelvey's flux theory (MFT). Nonlinearity Analysis of Quantum Capacitance and its Effect on GFETs with large area graphene is simple, compact, and fundamental physics-based quasi-analytic model for Single-layer graphene field effect transistors (GFETs) with large area graphene. The basic device physics of the two-dimensional (2D) graphene channel is studied analytically. This modelling leads to the precise drain current calculation of the GFETs. The drain current calculation for GFETs starts from charge carrier concentration, its density of states and quantum capacitance (QC). QC depends on the channel voltage as a function of the gate to source voltage $V_{gs}$ and drain to source voltage $V_{ds}$ primarily. The formulation of the drain current with velocity saturation has been done by the Monte Carlo simulation method. The temperature and process variability study of these models along with quantum capacitive nonlinearity at 22nm to 5nm technology will be futuristic for research and development of

graphene nanoelectronics. Temperature and process variability study of single layer large area GFETs and quasi-ballistic at 22nm to 5nm technology of recent days home electronics could give us transient linear and nonlinear characteristic of the models. Detailed study of temperature and process variability could have solved the thermal heat dissipation problem in nanoelectronics structures. Thus, temperature and process study of the proposed model will be the future scope of this work.

### 6.3 MODELLING AND SIMULATION AND REALIZATION OF THE GFETS DEVICES WITH HELP OF EULER'S AND LAGRANGE'S FOR CALCULUS OF VARIABLE (COV) AND INTEGRAL EQUATIONS (IE).

To maximize and to find the extremal of drain current for the GFETs device have been modelled during the doctorate work, and the study of COV and IE over the graphene channel would prove novelty. The electrostatic properties of graphene-based nanomaterials, their heterostructure and their interaction with external electric field charge by solving the boundary value problem (BVP) with the help of green function formalism and the corresponding Poisson equation. The green function can be formulated for the electrostatic potential of the particular layer as graphene and other 2D materials are layer structures. The purpose of this research proposal is to state and solve the BVP of graphene with and without interaction with other 2D materials by the green function (GF) method. So, we are trying to use a simple mathematical technic (green function or Poisson equation which is a part of a differential equation) to solve a complex problem (the electrostatics of 2D materials and their BVP). Application of COV and IE over the formulated green function will maximize the drain current in the channel region.

### 6.4 DESIGN AND DEVELOPMENT OF GRAPHENE BASED SPORTS HAND RACKETS FOR MULTIPLE GAMES

The circular form of the graphene sheet, CNT carbon nanotubes is a useful and highly strong metal for the design and development of the sports hand rackets such as badminton, squash and tennis rackets. Now a day most of the hand rackets in the Indian market are from a foreign company which adds excise and 300% to 400% taxes on their manufacturing cost. This cost could be reduced with the indigenous racket manufacturing labs and industries in future with CNT metallization with steel.

### 6.5 CHAPTER SUMMARY

Nonlinearity, Scaling Trends of Quasi-Ballistic GFETs for RF Applications of chapter five is the radio (GHz) frequency static linearity and nonlinearity performance potential analyzed for the ballistic approach GFET under the ballistic transport regime. Nonlinearity Analysis of Quantum Capacitance and its Effect on GFETs with large area graphene is simple, compact, and fundamental physics-based quasi-analytic model for Single-layer graphene field effect transistors (GFETs) with large area graphene. The Design and development of Graphene heterostructure nanoelectronics real-world electronic devices and circuits such as a low sub-threshold digital logic, a high voltage inverter, a static random-access memory, a back gated Bi-GFET with displacement electric field RF mixer with low losses and dual gate Bi-GFET would be interesting future applications of graphene nanoelectronics. To maximize and to find the extremal of drain current for the GFETs device modelled during the doctorate work, and the study of COV and IE over the graphene channel would prove novelty for future study. The circular form of the graphene sheet, CNT carbon nanotubes is a useful and highly strong metal for the design and development of the sports hand rackets such as badminton, squash and tennis rackets.

# Appendix:

The drain current for the four terminal GFET devices can be modified for simplicity of the calculation and to make modelling effective to the EDA tool developers. From (3) and (4) total charge density can be compiled as

$$n(x) = \frac{(q)^3 V_{CH}|V_{CH}|}{\pi(\hbar v_f)^2} + C \ldots.. \quad (17)$$

where $C$ here is constant with the useful scientific values of the symbols used in (3) and (4) and $\boldsymbol{v_f}$ Fermi velocity is $10^6$ m/sec at room temperature [1]. For the particular value of extrinsic electric field (E), fixed channel length (140nm, 300nm) and mean free path length, mentioned in detail in the introduction section backscattering coefficient ($r_{bs}$) could also be simplified in an explicit math equation from (5) as a function of $V_{ds}$ and $\mu_{eff}$, where $C$ is again constant with other notations as usual scientific symbols

$$r_{bs} = \left(\frac{1.5\, V_{ds}\mu_{eff}}{2L\, K_B T \lambda}\right) / C \quad (18)$$

and Fermi-Dirac integral solved by Blackmore [39, 26] of order one can also be simplified more explicitly as a function of $V_{ds}$ only as

$$£_1(\omega_F) = \int_0^\infty \left[\frac{1}{1+exp\frac{(E-E_F)}{K_B T}}\right] dE \quad (19)$$

and which can be approximated as $exp-\frac{(E-E_F)}{K_B T}$ and so $£_1(\omega_F - \omega_{DS})/£_1(\omega_F)$ can be a function of drain voltage only as $exp-\frac{V_{ds}}{K_B T}$ after simplification of the exponential math's. Thus, a proper drain current and gate voltage relation can be present mathematically as

$$I_{DS} = \frac{A\left(B+CV_{CH}^2(x)\right)\left(1-\frac{1.5\, V_{ds}\mu_{eff}}{2L\, K_B T\lambda}\right)\left[1-e^{-Vds/kBT}\right]}{\left[\left(1+\frac{1.5\, V_{ds}\mu_{eff}}{2L\, K_B T\lambda}-\left(\frac{1.5\, V_{ds}\mu_{eff}}{2L\, K_B T\lambda}\right)^2\right)\left(e^{-Vds/kBT}\right)\right]} \quad (20)$$