SRAM DESIGNS FOR NANOMETER TECHNOLOGIES

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CERTIFICATE

This is to certify that the thesis entitled ─ **SRAM DESIGNS FOR NANOMETER TECHNOLOGIES** submitted by **Monica Gupta** (2K17/PhD/EC/11) to the Department of Electronics and Communication Engineering, Delhi Technological University for the award of the degree of Doctor of Philosophy is based on the original research work carried out by her under our guidance and supervision. In our opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree. It is further certified that the work presented in this thesis is not submitted to any other university or institution for the award of any degree or diploma.
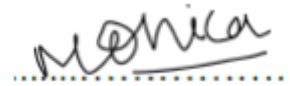
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CANDIDATE'S DECLARATION

I hereby certify that the research work, which is being presented in the thesis, titled,

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ABSTRACT

High performance applications, such as biomedical and wireless sensor networks, require low power circuits for extended time operation. Supply voltage scaling in such systems is an effective way to lower the power consumption. Although voltage scaling has benefits, it has brought serious challenges for designing reliable digital circuits including Static Random Access Memories (SRAMs). Further, as SRAM occupies a significant area on SoC, the memory failures may lead to complete collapse of the system.

The conventional 6T SRAM cell has been the industry standard for a long time. However, it has limitation in operating reliably at lower voltages due to reduced margins and other performance related issues. Therefore, conventional 8T SRAM cell with improved margins has emerged as the potential substitute for its 6T counterpart. In nanometer regime, the leakages and PVT-variations become significant culminating into degraded performance and restricting its usage in sub-threshold region in small-geometry devices.

As sub-threshold leakage dominates the total leakages in SRAM cell in nanoscale devices, the classification of sub-threshold leakage reduction techniques and their impact on performance parameters under various operating conditions need extensive analysis. The available techniques are classified as those addressing leakage current component at the level of latch, bitline and read port levels; and their impact on major performance parameters is evaluated. Since the performance of a technique is also susceptible to PVT-variations, this aspect is also considered for suggesting the best suitable operating conditions for a technique falling under each classification. A low leakage SRAM cell based on the use of leakage reduction techniques is also presented. The latch and bitline leakages are respectively addressed through Multi threshold CMOS and Negative

wordline techniques in the cell. Further, Multi threshold CMOS technique is applied to non-critical transistors in the latch core to avoid its degrading effect.

There are issues in read and write operation of nanometer SRAMs and isolated read port is popular technique used to address this. The trade-off existing between the read current and read bitline leakages needs examination. To address this issue, two new SRAM cells with an isolated read port are proposed in this work. In the first proposed cell, the write performance is improved by incorporating write assist transistor with single ended write to reduce power consumption. An attempt is made to achieve high read current values by removing the stacking of MOS transistors in the read port. The second proposed cell addresses yet another issue of nanometer SRAM cells i.e. read bitline leakages. It uses compensation transistor which suppresses and equalizes read bitline leakages in un-accessed cells irrespective of the stored data resulting in low and data-independent leakages in SRAM cell. Additionally, it provides the reverse current in accessed cell to maintain high read bitline voltage while compensating read bitline leakages in un-accessed cell. The reduced stacking effect of transistors further helps in maintaining reasonable values of read current resulting in significant improvement in all the read performance parameters. For improvement in write mode, the proposed cell employs faster differential write.

With reduced supply voltage and device scaling, the issue of PVT-variations has also emerged as a serious design challenge for nanometer SRAMs. This issue is addressed in the literature by incorporating Schmitt-trigger inverters for latch core in SRAM cells. However, a Schmitt-trigger based SRAM cell that can address the major performance parameters in all the three operating modes is not available in literature. In this regard, a new Schmitt-trigger based SRAM cell is presented that provides data-independent

tolerance against PVT-variations in all the three modes. The proposed cell provides better write performance due to the presence of novel combination of Negative bitline write assist technique with modified Schmitt-trigger action. Further, fully-gated grounded scheme is used in isolated read port to reduce read bitline leakages.

FinFET is emerging as an alternative to CMOS technology due to its good scaling ability, high ON current, reduced V_{th} variations, better sub-threshold slope and short-channel effect. Therefore, an attempt is made to propose a FinFET based SRAM cell with an isolated read port that can address the issues of existing cells such as reduced stability of stored data, increased bitline load capacitance, increased leakages etc. The proposed cell achieve better data stability due to the isolation of internal storage nodes from external bitlines. The read bitline leakages are also reduced in un-accessed cells by maintaining similar operating conditions in the read port, independent of stored data values. Further, the increased driving strength of FinFET based cell results in high read current values providing significant improvement in read performance parameters. Additionally, the use of write assist transistor helps in quick charging of internal storage nodes resulting in faster write operation.

In the thesis, the performance of all the proposed SRAM cells is analyzed and compared based on various standard cell metrics. The functionality of proposed cells is verified in all the three operating modes and performance simulations are done using 32 nm bulk CMOS PTM model parameters. Further, the performance of FinFET based cell is verified using 22 nm FinFET PTM model parameters.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

ABBREVIATIONS

SRAM   Static Random Access Memory
WL   Word line
WWL   Write wordline
RWL   Read wordline
BL   Bitline
BLB   Bitline bar
RBL   Read bitline
SNM   Static noise margin
HSNM   Hold static noise margin
RSNM   Read static noise margin
WSNM   Write static noise margin
WM   Write margin
DRV   Data retention voltage
MTCMOS   Multi-threshold CMOS
SB   Substrate-bias
DM   Drowsy mode
NWL   Negative wordline
LBB   Leakage biased bitline
SE   Stack-effect
DCPR   Dynamic control of power rails
VCG   Virtual cell ground
PVT   Process-voltage-temperature
SCE   Short channel effect
RDF   Random dopant fluctuations
ITRS   International Technology Roadmap for Semiconductors
HVT   High threshold voltage
MVT   Multiple threshold voltage
LVT   Low threshold voltage

CHAPTER 1

INTRODUCTION

1.1 Background

SRAM plays a key role in memory organization of a computer system as shown in Fig. 1.1. It occupies a significant chip area and thus is considered as a critical component on system-on-chip such as in portable devices, microelectronic applications, sensor networks, biomedical implants etc. [1-11]. Thus, there is a need of fast, robust, high density SRAMs [12-13].
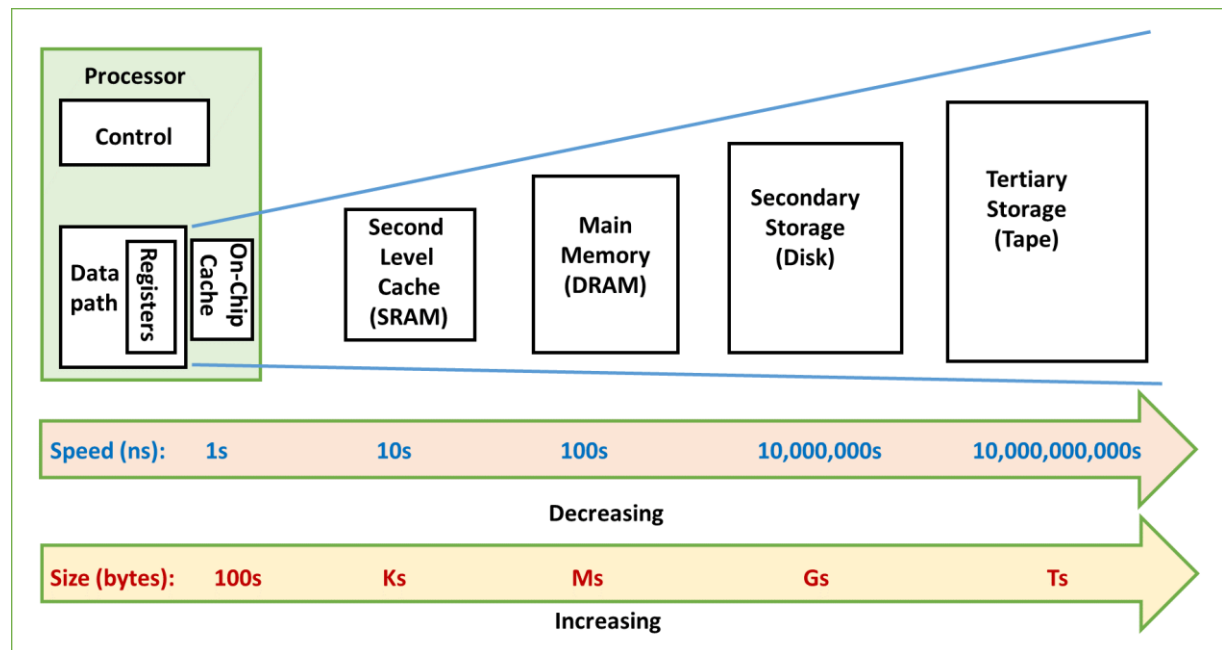
Fig. 1.1 Memory hierarchy of modern computer system [1]

1.1.1 SRAM architecture [1][10]

A typical SRAM architecture for 4 Kb SRAM (Fig. 1.2) consists of an SRAM array, in which the SRAM cells are arranged over multiple rows and columns, along with the decoders, read-write column circuitry and control logic. A brief description on different blocks is as under:

SRAM array: It consists of a regular arrangement of SRAM cells organized in various rows and columns (N rows and M columns) where each cell can store one bit of data. For example, a 4 Kb SRAM consists of 4096 SRAM cells arranged over 128 rows and 32 columns. Now, to access these cells for read and write operations, different types of peripheral circuitry such as

a row address decoder, pre-charge circuit, sense amplifier, write driver circuit and multiplexers are needed.

Row address decoder: The data in the SRAM array is usually stored in non-interleaved and interleaved ways [1]. In non-interleaved arrangement, one word is stored per row whereas in an interleaved arrangement one bit of multiple words are stored per row. So, to read/write data in a specific SRAM cell, initially a row is selected out of the given N rows using a row address decoder. The row address decoder pulls the corresponding wordline (WL) high using a word line driver circuitry. After this, the multiplexers select a specific column using a complementary pair of bitlines, BL and BLB. The bitlines are then driven by write driver circuit or sense amplifier through various control signals depending upon the type of memory operation to be performed.
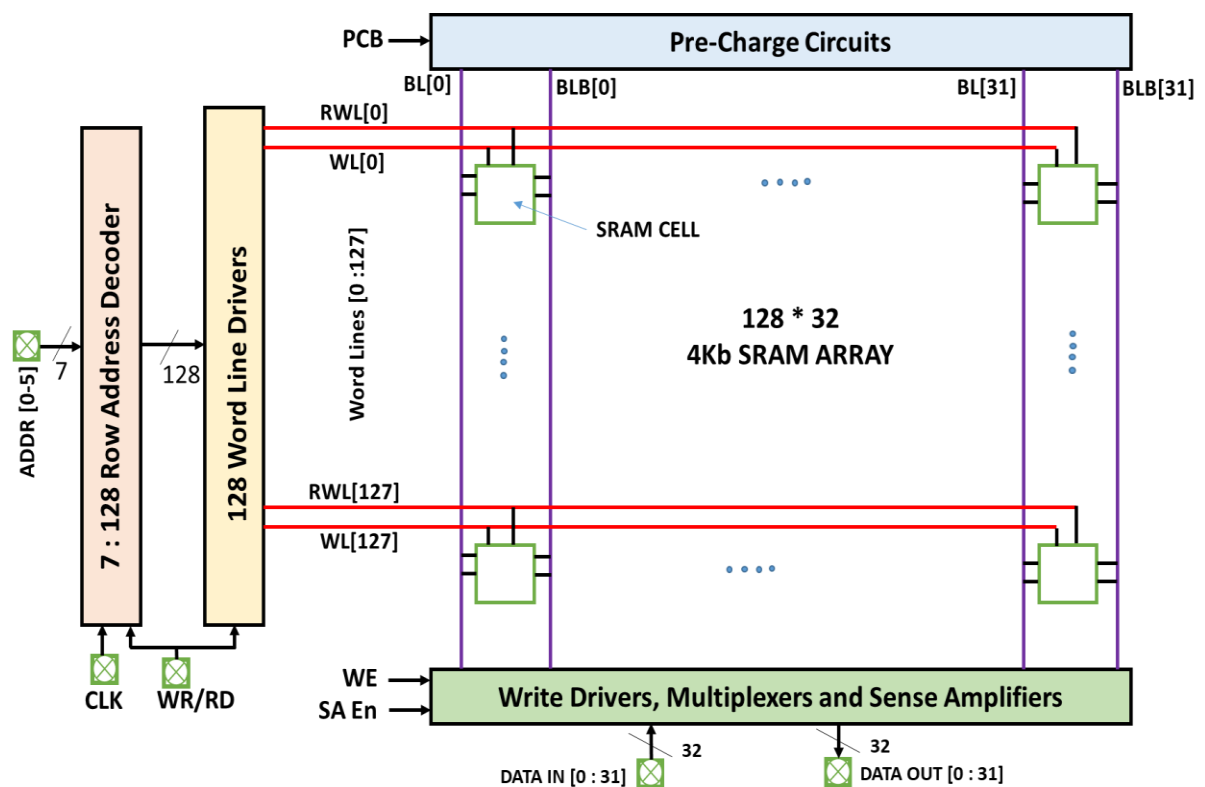
Fig. 1.2 SRAM architecture [10]

Pre-charge circuit: The pre-charge circuit is used to pull the bitline pair (BL and BLB) towards supply voltage (V_{DD}) using an active low control signal PCB prior to read/write operation on the SRAM cell. Two such implementation are shown in Fig. 1.3. The circuit in Fig. 1.3(a) shows the basic implementation using two pMOS transistors P1 and P2. The circuit in Fig. 1.3(b) that helps in maintaining equalized voltages on the bitlines uses an extra pMOS transistor (P3) and improves voltage swing between the bitlines during read operation.

(a)   *(b)*
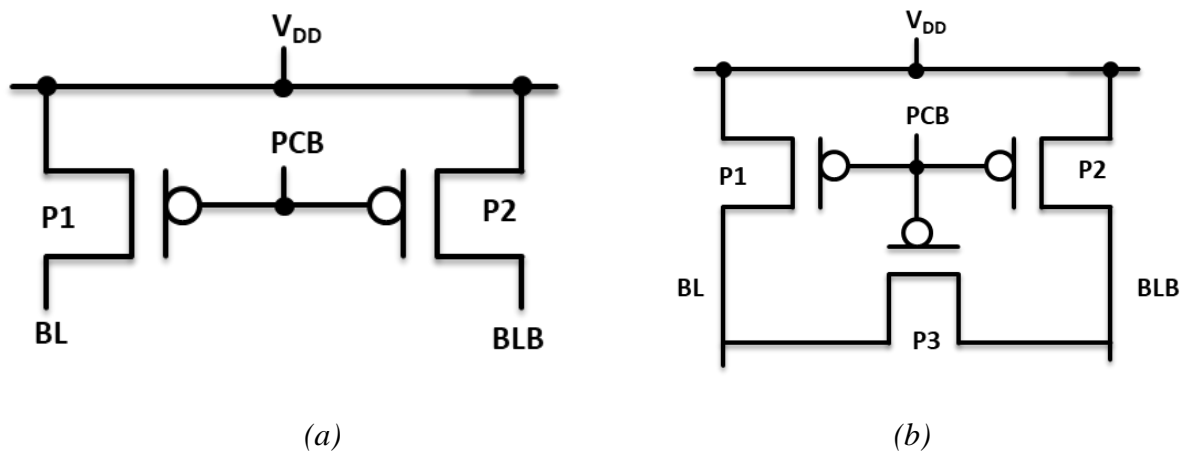
Fig. 1.3 Pre-charge circuit for SRAM [1]

Sense amplifier: A sense amplifier is considered as a key peripheral component while designing large memories as it has a strong impact on the read access time of the SRAM cell. The main function of the sense amplifier is to convert the small differential voltage developed on the bitlines during read operation to full swing output voltage. The sense amplifier enable signal, SA En (shown in Fig. 1.2) activates the sense amplifier for sensing the stored data in SRAM cell and completes the read operation. The large bitline capacitance, process variations, device mismatch, timing and layout constraints are some of the challenges that need to be dealt with while designing SRAM memories. Various types of sense amplifiers such as current-mirror based differential, latch-type, transmission-gate based sense amplifiers are available in the literature [1].

4

Write drivers: A write driver is used to pull down the voltage of internal storage node holding '1' below the WM of SRAM cell. This is done using write enable signal, WE (Fig. 1.2) which activates the driver circuit and provides the discharging path for the storage node of the accessed cell. Due to the large bitline capacitance, the write drivers are always designed with non-minimal width and length. Pass-gate and AND-gate based circuits are some of the most commonly used write drivers [1].

1.1.2 Conventional 6T SRAM cell

There are numerous circuit realizations for the SRAM cell. The cells are classified according to the number of transistors used in their implementation. The structure of conventional 6T SRAM cell is shown in Fig. 1.4.

Fig. 1.4 Schematic of Conventional 6T SRAM cell

The conventional cell consists of six transistors and hence the name is given as 6T SRAM cell. The four transistors form the cross-coupled latch (MUL-MDL, MUR-MDR) to store the complementary data at internal storage nodes D and DB. The other two transistors (MAL, MAR) are used to access the internal storage nodes D and DB using wordline (WL) for performing read and write operation on the SRAM cell. The transistor pairs: MAL-MAR,

MDL-MDR and MUL-MUR are respectively called access, pull-down and pull-up transistors. The cell can be operated in three different modes: hold, write and read.

Hold mode

In the hold mode, the SRAM cell maintains the voltage levels on internal storage nodes, D and DB. The wordline WL is pulled low using write driver while the bitlines are pre-charged to V_{DD} using pre-charge circuit. It is assumed that the cell is currently storing '1' at node D and '0' at node DB. This turns the transistors MDL and MUR OFF. The transistors MAR and MAL are already OFF as the wordline is low. This isolates the internal storage nodes from the external circuit. In this state, the noise immunity of the latch is maximum.

Write mode

In this mode, the new data values are written into the cell. To perform the write operation, initially the data to be written is applied on the bitlines through the write driver circuit and then the wordline WL is pulled high. This turns both the access transistors, MAL and MAR, ON. The write operation always starts at the node storing '1'. The voltage at this node is pulled-down below the WM of the cell. The feedback action of the cross-coupled inverter structure then helps in flipping the stored values quickly. However, this can happen only if the charging current flowing through the pull-up transistor towards the node storing '1' is smaller than the discharging current through the access transistor. Therefore, for write operation to be completed successfully, access transistors must be stronger than the pull-up transistors. This is estimated by means of the pull-up ratio which is usually set between 1 and 1.5.

$$Pull - up \ ratio = \frac{\left(\frac{W}{L}\right)_{MAL,MAR}}{\left(\frac{W}{L}\right)_{MUL,MUR}} \ .... \ (\mathbf{1})$$

Read Mode

The read operation begins by pulling the wordline WL high. This connects the pre-charged bitlines to the internal storage nodes, D and DB. A read path is set up through the access transistor and pull-down transistor through the internal node storing value '0'. This read current (I_{ON}) helps in discharging the pre-charged bitline towards low level. The sense amplifier then senses this fall in voltage at the corresponding bitline for reading the stored data. However, for this to happen the charging current through the access transistor towards the node storing '0' should be smaller than the discharging current flowing through the corresponding pull-down transistor. This requires that the strength of the pull-down transistor should be more than the strength of access transistor, which is defined by means of a cell ratio and it is usually set equal to 2.

$$Cell\ ratio = \frac{\left(\frac{W}{L}\right)_{MDL,MDR}}{\left(\frac{W}{L}\right)_{MAL,MAR}} \quad \dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots\dots.. \quad (2)$$

1.1.3 SRAM cell metrics [2-126]

The following standard cell metrics are used in the literature to compare the performance of various SRAM cells:

1.1.3.1 Data stability

Maintaining the stability of stored data at internal storage nodes in the presence of disturbance is a major concern in nanometer regime during hold and read modes. The static immunity to disturbances like process and mismatch variations, bulk static noise, supply ring offset, quasi static temperature changes are well characterized by means of the Static Noise Margin (SNM). The noise margin is calculated as the amount of noise voltage required at the input of a long

chain of inverters such that it has the maximum tendency to upset the logic levels. Such a setup is equivalent to two cross-coupled inverters connected back-to-back as in a SRAM cell.

Hold static noise margin (HSNM)

It is calculated by superimposing the characteristics of one inverter on the characteristics of other inverter of the cross-coupled inverter structure of SRAM cell by sweeping either one of the internal nodes (D or DB) from GND to V_{DD} in the hold mode [18]. The side length of the largest square that can be embedded into the smaller lobe (in case of asymmetric cell structure) or any of the lobe (in case of symmetric cell structure) of the butterfly curve gives the estimate of HSNM.

Read static noise margin (RSNM)

The butterfly curve obtained by plotting the characteristics of one inverter superimposed on the mirror image of the characteristics of the other inverter in the read mode is used to calculate the RSNM. The butterfly curve in this case usually has smaller lobes compared to that in hold mode. The side length of biggest square in smallest lobe gives us the RSNM.

Data retention voltage (DRV)

The data stored in the cell becomes unstable as the cell supply reduces below particular value. The supply voltage at which the latch attains metastability and can maintain just sufficient voltages at its internal storage nodes is called DRV [27]. Usually, the cells are operated well above this value to compensate for the effect of Process-Supply voltage-temperature (PVT)-variations.

1.1.3.2 Write ability

The write ability of the SRAM cell is determined by its ability to overwrite the stored value at the given supply voltage.

Write static noise margin (WSNM)

To calculate this parameter, the feedback loop is disconnected and the SRAM cell is put in write mode. The characteristics of one inverter is then superimposed on the other. It is to be noted that the butterfly curve in this case has only one lobe.

Write margin (WM)

It is used to get an idea about the ease with which the new data value can be written into the cell. The smaller is the value of this parameter, the harder it will be to write into the cell. The larger its value, more easy it would be to overwrite the value stored in the cell. Therefore, the moderate value of this parameter is desirable. The write margin is measured using combined wordline margin method as suggested by Makino et al. [8]. To estimate this parameter, the wordline WL is swept from GND to V_{DD}. The voltage difference between V_{DD} and the value of WL at which the stored values cross each other gives the estimate of this parameter.

1.1.3.3 Minimum supply voltage (V_{min})

It is defined as the minimum supply voltage level required for the cell to perform all the three basic operations - read, write and hold operations. The supply voltage at which the area under the butterfly curve becomes zero during read and hold modes is respectively referred to as read V_{min} and hold V_{min}. Similarly, the supply voltage at which the WM becomes negligible in write mode is known as write V_{min}. The maximum value out of these determines the V_{min} of the cell.

1.1.3.4 Delay performance

The delay is measured as the time required to complete the specified operation in SRAM cell.

Read access time (T_{READ_ACCESS})

The time required to perform read operation is evaluated in terms of T_{READ_ACCESS}. The T_{READ_ACCESS} for SRAM cells performing differential sensing, is defined as the time required for the bitlines to develop 50 mV or 100 mV of differential voltage after the wordline is activated along a row [59]. A current-mirror based differential sense amplifier is used for sensing the data [1]. For SRAM cells employing single ended sensing, T_{READ_ACCESS} is estimated as the time required for RBL to discharge from V_{DD} to GND after the activation of wordline. For such SRAM cells, a hierarchical bitline-sensing design is used [126].

Write access time (T_{WRITE_ACCESS})

The T_{WRITE_ACCESS} is analyzed by considering both T_{WRITE_ACCESS} ('1') and T_{WRITE_ACCESS} ('0'). The T_{WRITE_ACCESS} ('1') is estimated as the time required by internal storage node to charge to 90 % of supply voltage value when wordline is pulled high during write operation. Similarly, T_{WRITE_ACCESS} ('0') is defined as the time required by the internal node to discharge to 10 % of the supply voltage value after the activation of wordline [59].

1.1.3.5 Power consumption

The total power consumption comprises of dynamic power consumption and leakage power consumption of the cell.

Dynamic power consumption (P_{DYN})

Dynamic power consumption includes read power and write power consumptions.

Read power consumption (P_{READ})

It is defined as the power consumption of the switching nodes/ transistors when the cell performs the read operation.

Write power consumption (P_{WRITE})

It is defined as the power consumption of the switching nodes/ transistors when the cell is performing the write operation.

Leakage power consumption (P_{LEAK})

It is the power consumption of the cell in hold mode. It consists of the sub-threshold leakage current (I_{SUB}), gate direct tunnelling current (I_{GATE}) and junction tunnelling current (I_{JUNC}) of all the MOS transistors. Out of all leakage components, I_{SUB} is the largest contributor of the total leakage current in the sub-threshold region.

1.1.3.6 Miscellaneous

Besides the metrics described above, the following metrics are equally important:

$I_{ON/OFF}$ ratio

This parameter determines the number of SRAM cells that can share the peripheral circuitry along the column and thus, plays a major role in determining the peripheral requirements for implementing a larger array. The read bitline (RBL) leakages pull down the bitline and cause a false read resulting in read failures. Therefore, it is necessary to maintain a reasonable value of this parameter under all operating conditions.

RBL voltage swing (ΔV_{RBL})

The ΔV_{RBL} is defined as the worst-case difference in RBL voltage for read '1' and read '0' operation [57]. For successful read operation, RBL voltage for read '1' should be greater than RBL voltage for read '0'; otherwise, a read failure occurs due to negative ΔV_{RBL} [50].

Area

The smaller area is desirable to reduce the cost. However, there exists a trade-off between the area and cell performance particularly at lower technology nodes and sub-threshold region.

1.1.4 Issues with conventional 6T SRAM cell [1-120]:

The conventional 6T SRAM cell is an industry standard since long time due to faster differential read and write operations and compact area [14]. For successful operation of the cell in read and write modes it needs stronger nMOS pull-down (MDL, MDR), medium strength nMOS access (MAL, MAR) and weaker pMOS pull-up (MUL, MUR) transistors (Fig. 1.4). However, at lower supply voltages the cell sizing becomes less effective resulting in deteriorated read and write performance. The increased PVT-variations exaggerate the situation and may lead to increased memory failures.

Destructive read operation: During read operation, the read current flows through the access and pull-down transistors connected to internal node storing '0'. Due to the voltage divider action between the access and pull-down transistors, the voltage at this node increases slightly. If the increased voltage is greater than the switching threshold voltage of the other inverter then the regenerative action of the cross-coupled inverter structure is triggered resulting in flipping of stored values. This is known as **destructive read operation**.

Read-write conflict issue: In the conventional 6T SRAM cell, the write performance can be improved by increasing the strength of access transistors. However, this deteriorates the read performance of the cell. Similarly, when an attempt is made to improve the read performance of the cell, write performance degrades. This is known as **read-write conflict issue**.

To overcome these issues, the alternate approaches are used that include use of different assist techniques or assist circuits for performance improvemen [62-120]. Alternatively, the new SRAM cell topologies [2-6][10-15][32-61] are introduced by adding one or more transistors to the existing SRAM cell designs.

1.2 Literature Review and Scope of Work

The growing need for high density SRAMs has motivated the designers to reduce the MOS channel length from submicron to nanometer scale to increase the number of SRAM cells per unit chip area. The presence of huge number of SRAM cells on a limited chip area in turn causes problem of high power consumption and excessive leakages in small geometry devices. To curb these problems, voltage scaling on smaller devices is applied. However, it leads to degraded read and write performance in SRAM cell that further exaggerates under PVT-variations.

1.2.1 Challenges in SRAM cell design with scaling [2][52][68-74]

The device scaling on SRAMs reduces the parasitic capacitances and provides faster operation. As per Moore's law, scaling of the minimum MOS length by about 30 %, doubles the number of transistors on a given chip area and decreases the parasitics by 30 %. Further, the scaling of supply voltage results in significant reduction of dynamic power consumption due to its quadratic relationship with supply voltage. In addition, it reduces the tendency of ultra-thin

13

oxides to breakdown in small geometry devices. However, this imposes some serious design challenges for SRAM designers as described below:

Data stability

In the SRAM cell, direct access of internal nodes during read operation makes it vulnerable to external noise, causing degraded RSNM and may even result in destructive read operation. The conventional 6T SRAM cell fails due to read margin deterioration below 800 mV at 65 nm [52].

Write ability

Similarly, to perform a successful write operation, the access transistors must be made wider than the pull-up transistors to enhance their current conducting capability. This was not a concern for cell operating in strong inversion but in sub-threshold region the impact of process variations becomes much more prominent specifically at slow-nMOS and fast-pMOS (SF) corner. At SF corner, the pMOS transistor becomes stronger than nMOS transistor resulting in increased write failures. This problem is further exaggerated at lower temperature due to increased subthreshold-slope of pMOS transistor than nMOS transistor resulting in increased driving strength of pMOS transistor. Due to this, the 6T SRAM cell loses write ability below 700 mV at 65 nm and 600 mV at 32 nm [2][52].

Leakage power consumption

Dynamic power consumption dominates at high supply voltages whereas leakage power shows dominance in sub-threshold region and causes increased total power consumption. If the leakages of the entire column pulls down the bitline below the offset voltage of sense amplifier during read operation then there may be false read operation.

PVT-variations

Due to the exponential dependence of the sub-threshold leakage current on the threshold voltage of the transistors, even a small variation in threshold voltage causes large changes in the sub-threshold leakage current. This leads to increased read and write failure probabilities in SRAM cell.

1.2.2 State-of-the-art SRAM cell designs [2-6][10-15][32-61][116-120]

The various SRAM cell topologies are introduced in the literature to address the performance issues of conventional 6T SRAM cell [2-6][10-15][32-61][116-120]. These topologies use extra transistors to provide improved performance at lower supply voltages in nanometer regime. Some of the most popular SRAM cell designs are discussed next.

The 7T SRAM cells [33][116] and 9T SRAM cell [117] provide faster write by cutting the feedback loop using extra nMOS transistors during write operation. In addition, in [33] use of low-threshold voltage pull-down transistor is suggested to further ease the writing process. The strong feedback mechanism of the cross-coupled latch is retained during read and hold modes to maintain the stability of stored data. The conventional 8T SRAM cell [4] performs differential write in the same manner as is done in 6T SRAM cell. However, it isolates the internal nodes from external bitlines using a decoupled read port, thus, providing improved read stability. The 9T SRAM cell [38] provides an alternate way to isolate the internal nodes from the external bitlines. The disadvantage is the doubling of the number of transistors connected per bitline resulting in increased bitline load capacitance and longer discharge times. The 10T SRAM cell [51] uses a novel isolated read port design to improve the read stability and reduce the RBL leakages. However, the read current is reduced due to the increased stacking effect of the transistors. The 11T SRAM cell [59] and 10T SRAM cells [118][119][120] use an isolated read port and a Schmitt-trigger action to provide improved

read stability and inverter characteristics. The Schmitt-trigger action helps in modifying the switching voltage of the latch inverters depending upon the direction in which the node voltages change due to PVT-variations. The result is improved noise immunity of the cell under PVT-variations. In addition, the Schmitt-trigger action is disabled [59] or feedback loop is weakened [118] or disabled [119][120] during write operation for easing the writing process. The 12T SRAM cell [60] uses an innovative write-assist technique to improve the write performance in sub-threshold region. It uses data-dependent feedback-path cutting technique by disabling one of the pull-down paths to GND during write operation. The fully-gated ground scheme is used to reduce the RBL leakages. However, the increased bitline load capacitance due to connection of more transistors per SRAM cell to bitlines deteriorates the time required to complete the write operation. The presence of multiple leakage paths also has a degrading effect on the cell performance.

1.2.3 Performance improvement [2-115]

In the literature, the research on SRAM is mainly focused towards improving read and write performance, leakage reduction and PVT-variation tolerance. The chances of achieving lower failure probability and higher yield are becoming thin with increasing process variation. Thus, novel designs and techniques are developed and adopted at the cost of area, power dissipation, or speed to improve SRAM cell performance.

1.2.3.1 Approaches to improve read performance

The read performance of the SRAM cell can be improved by using either read assist techniques or read assist circuits.

Read assist techniques

This includes techniques like World line underdrive (WLUD) [6][37], Suppressed bitline (SBL) [37][43][84], Negative V_{SS} (NV$_{SS}$) [37][43] and Asymmetrical cell sizing [2][14]. These

16

techniques are aimed towards enhancing the cell ratio by strengthening the pull-down transistor compared to access transistors. The WLUD technique improves the RSNM but decreases the read current and degrades the WM. In the SBL technique, the bitlines are pre-charged to voltages lower than the full V_{DD}. It incurs overhead of voltage generator circuit and hence increased power consumption and area. The NVss approach reduces the read disturbance but decreases the stability of stored data in other cells sharing the same row. An asymmetrical cell sizing increases the area drastically with subsequent increase in leakages.

Read assist circuits

When the improvement through assist techniques is less than the target value it is clear that SRAM topologies with read assist circuits are required [4][12][47-49][51][57][86]. The read operation in conventional 6T SRAM cell shows degraded RSNM values as the internal node lies directly in the read current path that affects the voltage level at storage node resulting in reduced data stability. The read assist circuits provide separate discharge path for the read current as is done in conventional 8T SRAM cell [4]. However, the read port transistors need to be up-sized to maintain low T_{READ_ACCESS} resulting in increased RBL leakage current. The circuit in [47] uses a stacking effect of three transistors to reduce the RBL leakages but suffers from degraded read current values and high access time. The next circuit [48], provides a low resistance read current path in the accessed cell and alternatively keeps the RBL voltage at V_{DD} by providing the leakage current path to RBL through un-accessed cells in the same column. However, the drawback is the significant increase in static power consumption.

It can be deduced that SRAM cell designed with available read assist techniques/circuits in nanometer regime maintains lower values of read current, with higher read access times. So, the design of read port with enhanced read current values to improve the read performance of the cell is explored in this work.

1.2.3.2 Approaches to improve write performance

The write performance of the SRAM cell can be improved by using either write assist techniques or write assist circuits.

Write assist techniques

It includes the techniques such as Negative bitline (NBL) [6], Boosted bitline (BBL) [77], Boosted negative bitline (BNBL) [77], Transient voltage collapse (TVC) [36], Wordline over drive (WLOD) [9], Raising global V_{DD} (RGV) [43] and Cell ground boosting (CGB) [77]. These approaches are aimed towards enhancing the pull-up ratio of the cell thereby making the access transistors stronger than pull-up transistors. The techniques like WLOD, NBL, RBV, BBL, BNBL make the access transistor stronger compared to the pull-up transistor. The remaining techniques such as TVC and CGB weaken the latch compared to the access transistor. Most of these techniques either degrades the HSNM of other cells on same row or require elaborate control of global or local V_{DD} except those that work on bitlines such as NBL, BBL and BNBL techniques. The techniques that work on bitlines either incorporate negative charge pumps or apply optimum value of charge to boost capacitor for implementation.

Write assist circuits

When the improvement through assist techniques is less than the target value, the new SRAM topologies are introduced to improve the write performance [2][12-13][35][52]. The circuit in [2] removes the pull down transistor from one of the latch inverter to provide faster write '0' operation whereas an extra transistor is used in [13] to weaken the feedback loop of cross coupled latch structure during write operation to ease out the writing process. The circuit in [35] interrupts the supply to one of the inverters thereby decreasing the resistance of the positive feedback loop and hence easing the writing process. The other circuit in [52] interrupts the cell supply during write operation and connects it to weak source through pMOS transistor

instead of floating the supply voltage completely through a power switch. The advantage is that the other cells in the same row are saved from the retention problem of stored data.

It is observed that the existing designs for SRAM cell improve the write performance with either no change or degradation of read performance. Therefore, a design that can provide improvement in both read as well as write performance needs to be explored.

1.2.3.3 Approaches to reduce leakages

As per ITRS roadmap, power consumption is a major concern in portable devices [72]. It is addressed by reducing either dynamic or leakage power consumption. It is worth mentioning that at high supply voltages, dynamic power consumption is dominant, however, as the technology scales the leakage power consumption becomes critical specifically in sub-threshold region. To address this issue, the leakage current in SRAM cell can be classified as latch, bitline and RBL (in cell with isolated read port) leakage currents and correspondingly, the leakage reduction techniques can be classified as latch, bitline and read port leakage reduction techniques. The techniques in each category can be used to target a particular leakage component within the cell.

Latch leakage reduction techniques

As latch is the integral part of a cell, therefore these techniques can be applied to different SRAM cells to achieve the purpose. This category includes techniques such as Multi-threshold CMOS (MTCMOS) [12][32][92-93], Substrate-bias (SB) [9][94-96] and Drowsy mode (DM) [27][49][73][78][88][97-98] techniques. The MTCMOS technique suggests the use of high-threshold voltage MOS transistors in latch to lower the latch leakages of the cell. The SB technique provides the alternate way to accomplish the same objective. The DM technique lowers the cell supply in order to reduce the drain to source voltage across the transistors resulting in reduction of leakages.

Bitline leakage reduction techniques

The negative wordline (NWL) [38][74][81][99][102] and leakage biased bitline (LBB) [103-105] techniques fall under this category. In the NWL technique, the access transistors are biased in super cut-off region by applying a negative gate voltage instead of GND during hold mode whereas in LBB technique, the bitlines of inactivated sub-banks in hierarchical bitline architecture are left in floating state. This biases the bitlines at random voltage levels depending on the leakage from the un-accessed cells connected to the same column and helps in reducing the overall leakage in the column.

Read port leakage reduction techniques

This category includes the stack-effect (SE) [4][20][47][59][107-108], dynamic control of power rails (DCPR) [50] and virtual cell ground (VCG) [4][34][56] techniques to reduce the RBL leakages of an isolated read port. The SE technique uses reverse-biasing effect whereas DCPR and VCG techniques adjust the voltage supply (V_{DD}) and ground level (GND) respectively to reduce the drain to source voltage across the read port resulting in reduced leakages [114].

Further, in nanometer regime there exist a substantial increase in the power consumption due to leakages which is of small magnitude otherwise [71][89]. It is pertinent to mention here that the above techniques are applied at higher technology nodes therefore their suitability at lower node in the presence of PVT-variations is explored in this work. Further, a novel SRAM cell with reduced leakage current values is designed in the thesis.

1.2.3.4 Approaches to improve PVT-variation tolerance

Process variation is the naturally occurring variation in the attributes of transistors when it is fabricated [28]. The sources of variations are gate oxide thickness, device geometry and

random dopant fluctuations. The Process-Voltage-Temperature (PVT) induced variations in the MOS behavior are addressed through changes in threshold voltage of the MOS transistors. Pelgrom's law states that the threshold (or other process related) mismatch between two adjacent identically drawn transistors increases inversely with the gate area [28]. The effect of process variation becomes more prominent at smaller technology nodes (< 65 nm). This causes the performance of a particular metric of SRAM cell to degrade and hence reduces the overall yield. To address this issue, various PVT-variation tolerant SRAM topologies are available in literature [10][53][59][61].

It is observed that the existing Schmitt-trigger based SRAM cells have degraded write ability, low read stability and poor I_{ON}/I_{OFF} ratio and reflect data-dependent tolerance against PVT-variations. Thus, the design of Schmitt-trigger based SRAM cell with enhanced performance is addressed in this thesis.

1.2.4 What is next at 28 nm and beyond? [121-134]

With on-going device and supply voltage scaling, conventional planar CMOS technology suffers from increased susceptibility to process variation, random dopant fluctuation (RDF), short channel effects, leakages, inability to write at ultra-low voltages etc. In a bulk CMOS transistor, current flows from the source to the drain through a channel. As chip designers scale transistors at each node, the channel length becomes shorter. As a result, the transistor may suffer from **short-channel effects** (SCE) which degrades the sub-threshold slope or turn-off characteristics in a device. Another issue is **transistor variability** due to which a given bulk CMOS transistor may perform differently from its nominal behavior. It may produce random differences in threshold voltage of devices, a phenomenon popularly known as **random dopant fluctuation** (RDF). To overcome the issues associated with bulk CMOS technology, several alternatives like the use of modified topologies and high permittivity gate dielectric are

being explored [10][53][59][61][125-127]. The other option is to use improved transistor technology for designing SRAM cell at lower technology nodes such as SOI FET [121-122] and FinFET [123-134]. The novel transistor structure such as FinFET, which promise better transistor aspect ratio, better scalability, low power consumption, better control on channel and higher channel mobility, has emerged as the leading candidate for next generation electronic devices.

The FinFET based SRAM designs in [133][134] use common port for performing read and write operations. Due to this, the designs suffer from read-write conflict issue resulting in degradation of performance of the cell in read and write modes. Thus, a novel FinFET based SRAM design with improved read as well as write performance is explored in this thesis.

1.3 Objectives

Based on the literature review and the research gaps identified thereafter, the following objectives are set for the research work:

- Design of SRAM with improved read and write performance for nanometer regime.

- Design of low leakage SRAM in sub-threshold region.

- A process variation tolerant SRAM design for nanometer regime.

- Use of improved transistor technology for performance improvement in SRAM.

1.4 Organization of the Thesis

The research work is structured in six chapters including this introductory chapter. Following is the brief description of chapters:

Chapter 1:

This chapter gives a background, literature review of existing SRAM cell designs, and objectives set for exploring new SRAM cell designs for nanometer technologies.

Chapter 2:

This chapter presents a comprehensive review of leakage reduction techniques prevailing in SRAM by classifying them in three categories namely latch, bitline and read port. The performance of the techniques are evaluated in terms of leakage reduction capability along with the impact on major performance parameters in three operating modes through extensive simulative investigations. The performance at different PVT corners and technology nodes is captured to demonstrate the efficacy of each technique with PVT-variations and technology scaling. A low-leakage SRAM cell that implements leakage reduction techniques for leakage reduction at different levels in SRAM cell is presented. In addition, it aims for improved read and write performance.

Chapter 3:

This chapter is devoted to the design of two SRAM cells, which successfully overcomes the read-write conflict issue, and provide improved read and write performance. The first design, achieves high read current values, improved RSNM and WSNM. The second design aims for low and data-independent RBL leakages, high I_{ON}/I_{OFF} ratio, low read access time, large RBL voltage swing and faster write in near threshold and sub-threshold regions.

Chapter 4:

This chapter extends into the designing of a PVT-variation tolerant Schmitt-trigger based SRAM cell. The idea is to enhance the performance of SRAM cell in all the operating modes. The cell uses techniques for improving the write ability and read performance in the sub-threshold region of operation. The reduced write, read and hold failure probabilities translates into reduction in minimum supply voltage required for accomplishing the memory operations.

Chapter 5:

This chapter exploits the possibility of designing SRAM under 28 nm technology node. In the nanometer regime, maintaining the performance under 28 nm is becoming difficult with bulk CMOS technology. FinFET is emerging as the most promising substitute for planar CMOS technology due to good scaling ability, high ON current, reduced V_{th} variations, better subthreshold-slope and SCE. A SRAM cell design below 28 nm node is worked upon in this chapter.

Chapter 6:

This chapter summarizes the work presented in the thesis and the future scope of the work.

CHAPTER 2

SRAM CELL DESIGN WITH LOW LEAKAGE IN SUB-THRESHOLD

REGION

The content and results of the following papers have been reported in this chapter:

1. Gupta M, Gupta K, Pandey N, "Comparative **Analysis of the Design Techniques for Low Leakage SRAMs at 32nm**", Journal of Microprocessors and Microsystems, Elsevier, 85, 1-19, 2021. **(SCI Journal with Impact Factor: 1.526)**

2. Gupta M, Gupta K, Pandey N, "**A Design of Low Leakage Cache Memory Cell for High Performance Processors**", *Journal of Information and Optimization Sciences, 40(2),* Taylor and Francis, 279-290, 2019.

2.1   Introduction

In nanometer regime, when many SRAM cells are integrated over a smaller chip area, there is substantial increase in power consumption due to leakages which is of small magnitude otherwise [71][89]. It is pertinent to mention here that sub-threshold leakage current is one of the major contributors in leakage power and needs consideration [50][90].

The sub-threshold leakages present in conventional SRAM cells are classified in section 2.2 of this chapter based on their origin within the cell. Further, a comprehensive review of the existing techniques that address sub-threshold leakage current at different levels in the conventional design of SRAM cell is done in section 2.3 [9][12][24][27][32][34][38][47-49][53][56][59][73-74][76][78][81][84][88][92-108]. The objective of this review is to quantify the impact of available leakage reduction techniques on SRAM cell performance under PVT-variations so that a suitable technique may be used in nanometer regime. This is done by classifying the existing techniques as latch, bitline and read port leakage reduction techniques, based on the leakage current component addressed through them within the cell. The impact of techniques in each category is then evaluated on major performance parameters. Since the performance of a technique is also susceptible to PVT-variations and technology scaling at lower technology nodes [91], therefore, this aspect is also considered for determining the best suitable operating conditions for their usage. In addition, a Proposed cell I with low leakage is presented in section 2.4. It is based on the use of NWL and MTCMOS techniques for reducing bitline and latch leakages respectively. The structure, functional verification and the performance comparison of the proposed cell with existing cells are also discussed in the same section. The conclusions are drawn in section 2.5.

2.2 Leakage current components in conventional SRAM cells

In this section, a brief review of various leakage current components existing in conventional SRAM cells is presented. In the 6T SRAM cell, two components of leakage current are identified based on their origin within the cell. The first component is the latch leakage current (I_{LATCH_LEAK}) that flows from cell supply to GND through non-conducting latch transistors. The bitline leakage current (I_{BL_LEAK}) is the second component that flows from BL/BLB to GND through non-conducting access transistors. One more leakage current component is defined for cells with decoupled read port, such as conventional 8T SRAM cell, and is named as read port leakage current (I_{RBL_LEAK}). A pictorial representation for leakage currents in conventional 6T and 8T SRAM cells storing logic '0' at D during hold mode is shown in Fig. 2.1(a) and Fig. 2.1(b) respectively. In nanometer regime, the leakage current becomes a critical performance parameter as the diffusion of the charge carriers in the source and drain regions is increased which results in a current flow in non-conducting transistors [93]. This leakage current affects the overall performance of the memory (such as number of SRAM cells connected to sense amplifiers, speed of operation etc.) and makes the cell more sensitive to variations [91]. Therefore, various techniques are used to suppress the leakage current.

(a)

(b)

Fig. 2.1 Leakage currents in conventional SRAM cells (a) 6T (b) 8T SRAM cells [4]

2.3 Classification of leakage reduction techniques

The existing techniques are classified in three categories namely latch leakage reduction techniques, bitline leakage reduction techniques and read port leakage reduction techniques based on leakage current origin. The techniques suggest either a circuit level modification in cell topology/multiple supply rails or at device level by using improved MOS transistors.

2.3.1 Latch leakage reduction techniques [9][12][24][27][32][34][38][47-49][53][56][59][73-74][76][78][81][84][88][92-108]

The techniques in this category aim at reducing the leakage current generated within the latch in a SRAM cell. As latch is the integral part of a cell, therefore these techniques can be applied to different SRAM cells to achieve the purpose. A detailed description on the techniques is presented below.

2.3.1.1 Multi-threshold CMOS technique (MTCMOS) [12][32][92-93]

This technique suggests the use of high-threshold voltage (HVT) MOS transistors in latch while typical-threshold voltage transistors to be used in the remaining cell. The presence of HVT MOS transistors lowers the I_{LATCH_LEAK} of the cell. A schematic of 6T SRAM cell using MTCMOS technique is depicted in Fig. 2.2(a) where the transistors with bold lines denote HVT MOS transistors. The modification of the threshold voltages is done at fabrication level by changing the doping profiles of the selected transistors yielding a low-leakage SRAM cell.
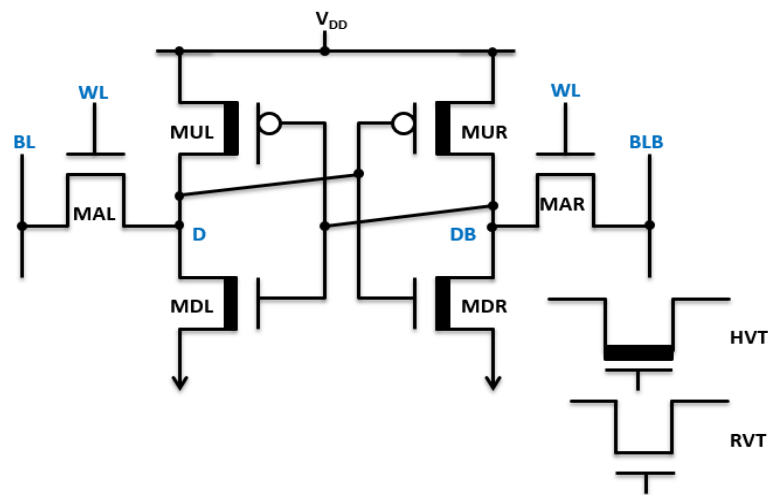
(a)
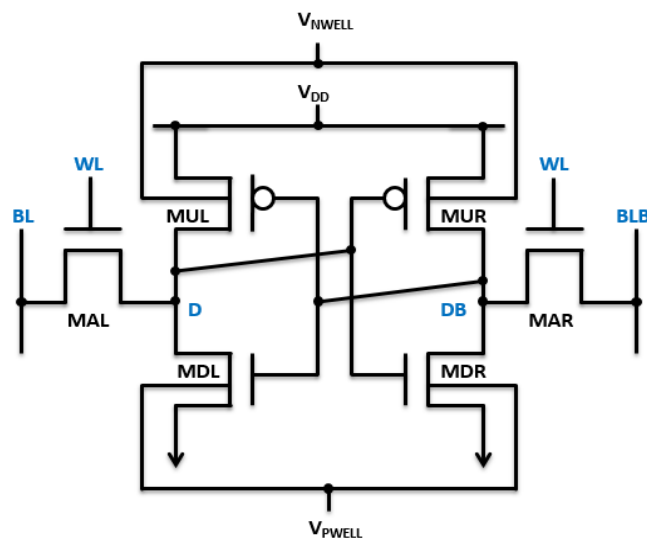
(b)
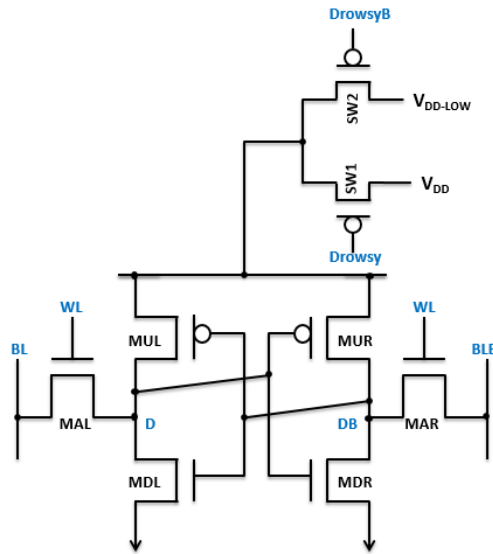
(c)

Fig. 2.2 Schematic of 6T SRAM cell with (a) MTCMOS (b) SB (c) DM techniques

2.3.1.2 Substrate-bias technique (SB) [9][94-96]

This technique presents an alternate way to accomplish the same objective. The threshold voltage of the latch transistor is varied by adjusting the bias voltages of p-wells and n-wells. The n-well voltage (V_{NWELL}) is set higher than V_{DD} while the p-well voltage (V_{PWELL}) is set lower than GND to enhance the body bias effect as shown in Fig. 2.2(b). A large offset voltage ($|V_{NWELL} - V_{DD}| = |0 - V_{PWELL}|$) is required to cause a significant reduction in I_{LATCH_LEAK}. In hold mode, the non-zero offset voltage increases the threshold voltage while in read or write mode it is set to zero by changing the bias conditions.

2.3.1.3 Drowsy mode technique (DM) [27][49][73][78][88][97-98]

In this technique, the latch transistors in 6T SRAM cell is made to operate in Drowsy mode wherein the supply voltage is lowered from V_{DD} to V_{DD-LOW} in order to reduce drain to source voltage across the transistors. This is realized with the help of two MOS-based switches SW1 and SW2 operated using control signals Drowsy and its compliment DrowsyB respectively as shown in Fig. 2.2(c). A reduction in I_{LATCH_LEAK} is observed due

to lower drain induced barrier lowering effect and reduced gate leakage. It is worth mentioning that the full collapse of supply voltage in 6T SRAM cell using DM technique should be avoided, as it would lead to loss of data. The cell supply voltage is generally kept above its DRV. Additionally, with dynamic supply variation, it is ensured that supply voltage is restored to its optimum value before the contents of the cell are accessed for read or write operation. The different architectures to reduce the area overhead by sharing the floating supply rails amongst the cells on a single column are available in the literature.

2.3.1.4 Comparative analysis

The SRAM cells using the discussed latch leakage reduction techniques are simulated and their performances are compared using SPICE simulations with conventional 6T SRAM cell in terms of leakage reduction capability, read performance and hold stability using 32 nm bulk CMOS PTM model parameters. The performance parameters namely, leakage current (I_{LATCH_LEAK}), read current (I_{ON}) and HSNM are measured. The SRAM cells are simulated at different temperatures (-40 ˚C, 25 ˚C and 125 ˚C) by varying the supply voltage from 0.4 V to 1.1 V across all process corners (TT, FS, SF, SS, FF; T: Typical, F: Fast, S: Slow) [88] to observe the effect of collective variations. As the leakage is process corner dependent and the ratio of leakage at FF corner to that at SS corner is usually high. So, for fair comparison, the performance of all the techniques is compared at maximum leakage corner (FF). In SB technique the V_{NWELL} and V_{PWELL} of the latch transistors are set at 20 % above V_{DD} and 20 % below GND respectively during hold mode. In the same mode for DM technique, the supply rail is lowered 20 % below nominal supply.

Leakage reduction capabilities : The reduction in leakage current I_{LATCH_LEAK} obtained for the SRAM cells using different techniques at all operating conditions is plotted in Fig. 2.3 to Fig. 2.5. It can be observed in Fig. 2.3(a) that at -40 ˚C I_{LATCH_LEAK} for SRAM using MTCMOS technique is reduced by 60 % at 1.1 V and 81.4 % at 0.4 V. With SB technique,

the percentage reduction in I_{LATCH_LEAK} is 42.4 % at 1.1 V and 44.3 % at 0.4 V showing marginal change (Fig. 2.3(b)). However, the SRAM cell using DM technique (Fig. 2.3(c)) shows a high reduction percentage of 95.1 % at 1.1 V which reduces to 66.3 % at 0.4 V. Thus, at high supply voltages DM technique exhibits the best leakage reduction capabilities while MTCMOS technique is suited for sub-threshold region. At 25 ˚C, out of the three techniques only MTCMOS shows improved leakage reduction capabilities with reduction percentages increasing to 93.6 % and 81 % respectively at 0.4 V and 1.1 V as shown in Fig. 2.4(a). The SB and DM techniques offers reasonable performance at 0.4 V with 44 % and 60 % leakage reduction respectively (Fig. 2.4(b) & (c)). The leakage reduction using SB technique improves to 60.3 % at 1.1 V while that using DM technique reduces to 90.7 % at the same voltage. Thus, MTCMOS technique shows continuously better performance than others at moderate temperatures particularly in sub-threshold region. As the temperature further increases from 25 ˚C to 125 ˚C, the same trend is observed with respect to all the techniques. The MTCMOS technique shows better leakage reduction capabilities over the others at all the voltages as depicted in Fig. 2.5. Thus, it can be concluded that a SRAM cell designed using MTCMOS technique has improved leakage performance with the increase in temperature especially in sub-threshold region.

(a)

Reduction in I_{LATCH_LEAK} with SB at T = -40°C

44.3% reduction @ (FF,0.4V, -40°C)

42.4% reduction @ (FF,1.1V, -40°C)

(b)

Reduction in I_{LATCH_LEAK} with DM at T = -40°C

66.3% reduction @ (FF,0.4V, -40°C)

95.1% reduction @ (FF,1.1V, -40°C)
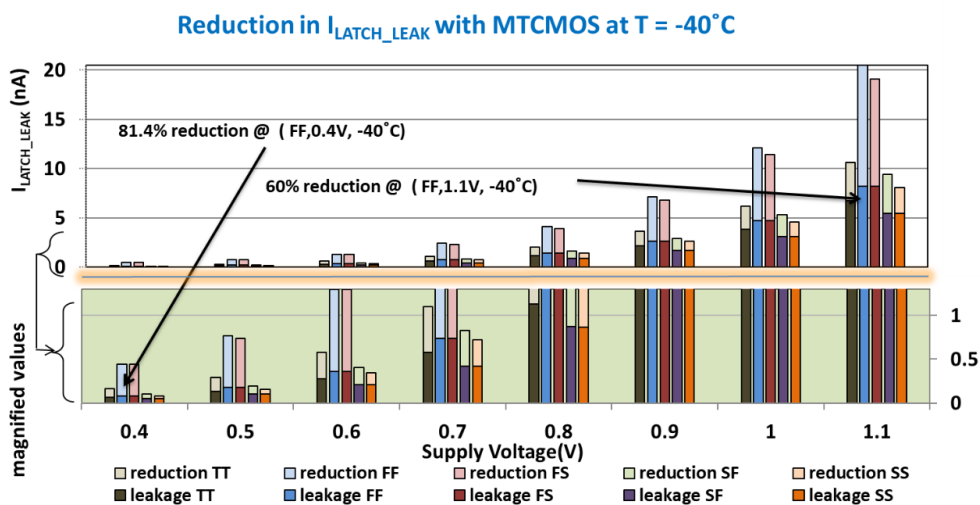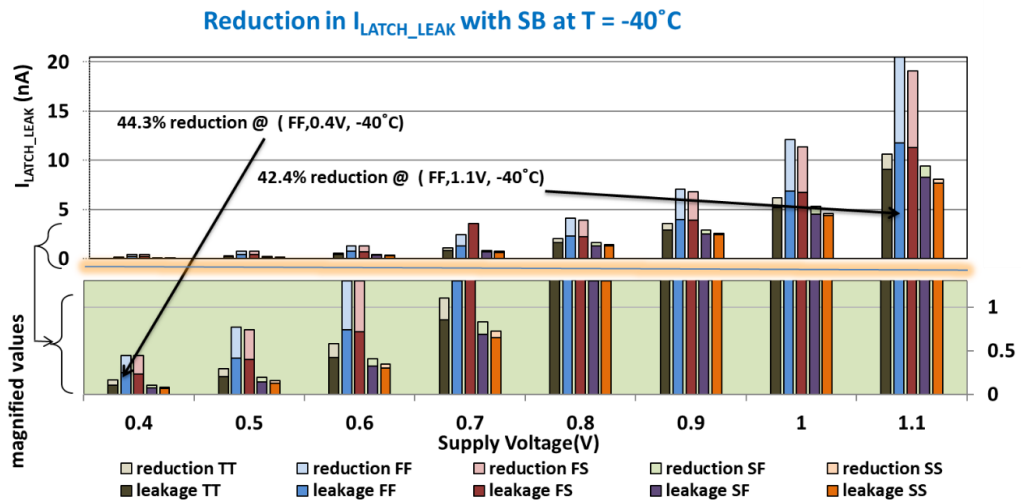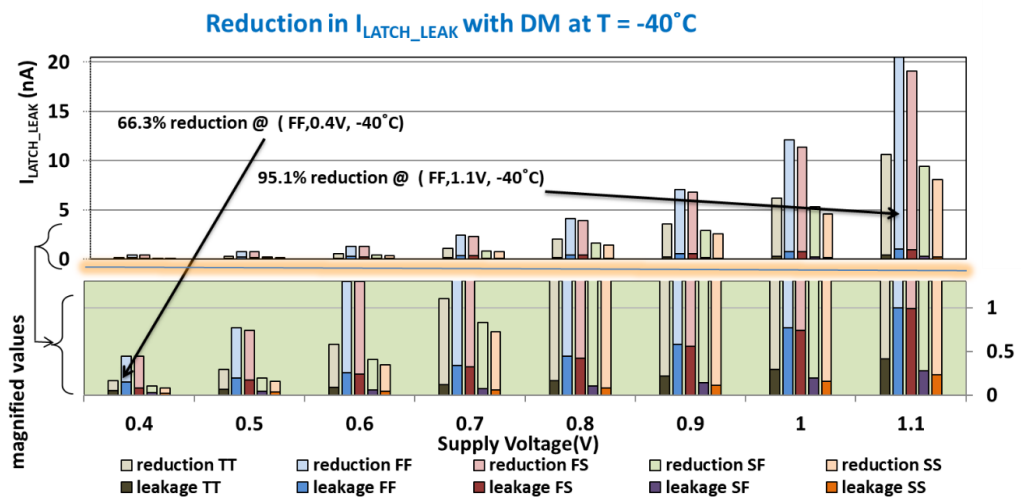
(c)

Fig. 2.3 Effect on I_{LATCH_LEAK} at T = -40 ℃

(a)

(b)

Reduction in I_LATCH_LEAK with DM at T = 25°C

(c)

Fig. 2.4 Effect on I_LATCH_LEAK at T = 25 °C
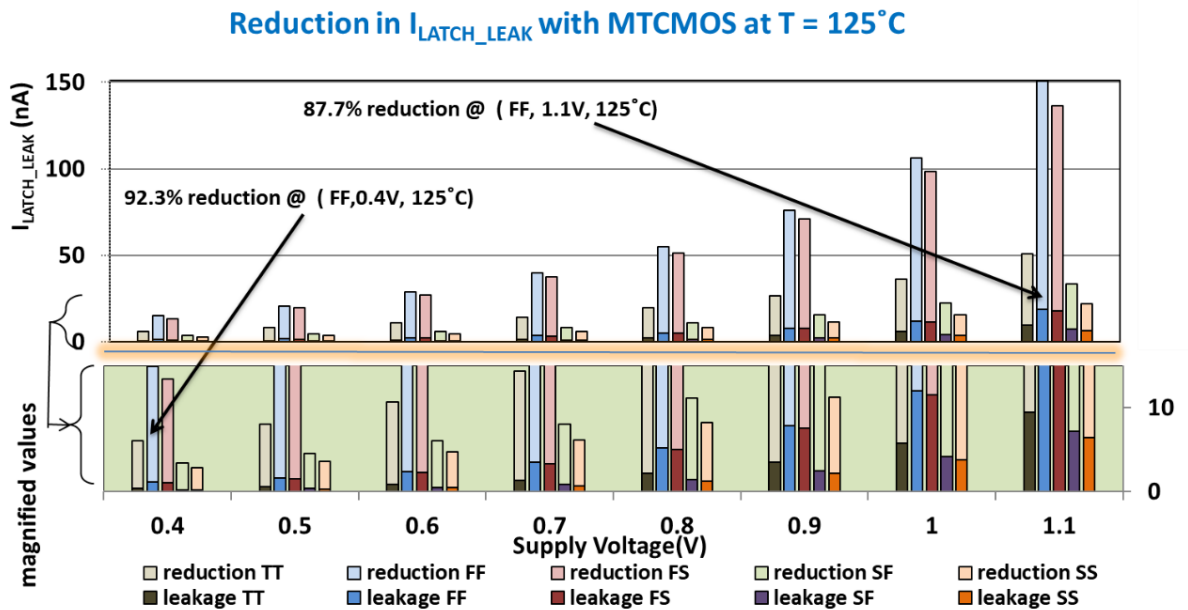
Reduction in I_LATCH_LEAK with MTCMOS at T = 125°C

(a)

(b)
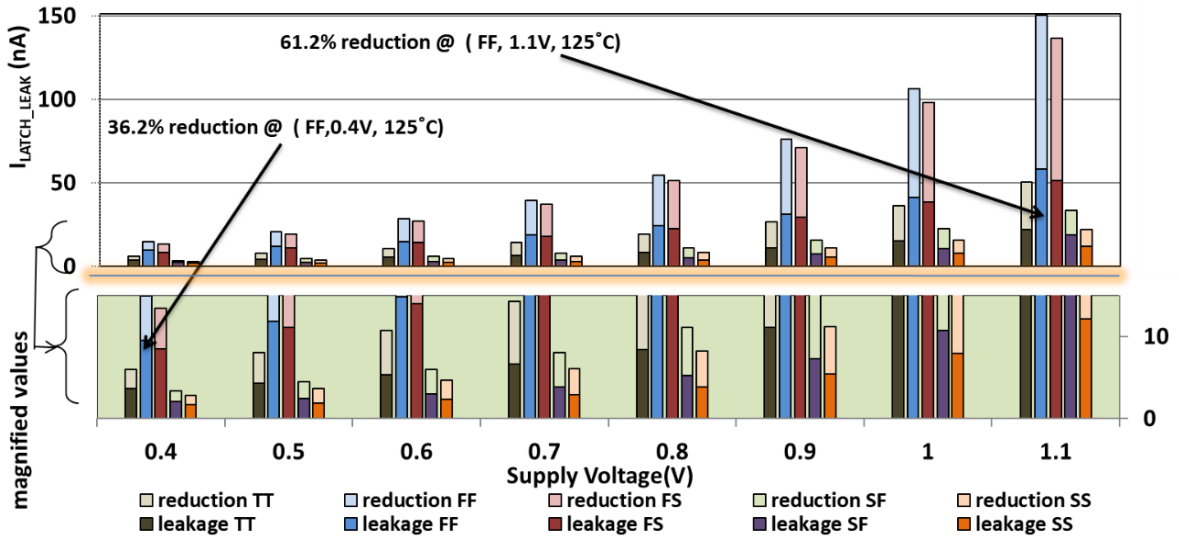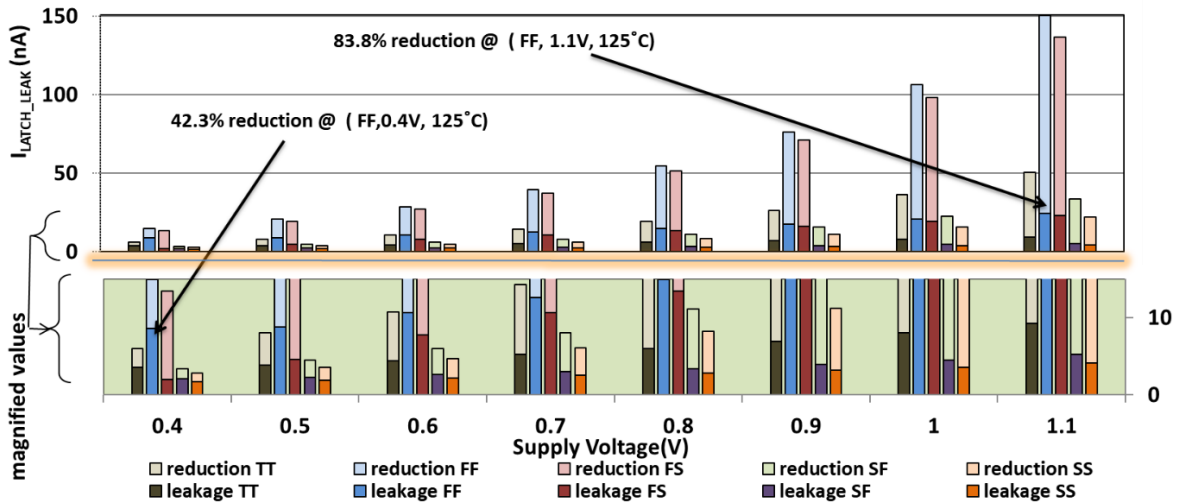
(c)

Fig. 2.5 Effect on I_{LATCH_LEAK} at T = 125 ˚C

Impact on read performance : The read current is measured for the SRAM cells. It may be noted that the SRAM cell with SB technique maintains the same read current values as the conventional cell since the threshold voltage of latch transistors is set to their nominal values during read or write operation by adjusting the Substrate bias voltages. Similarly,

DM technique based cell operates at the optimum supply voltage in read/write mode, therefore, it also shows the same read current values as the conventional cell. The read current values for MTCMOS based SRAM cell at different temperatures is plotted in Fig. 2.6. It is observed that read current is reduced in the sub-threshold region at all temperatures. Alternatively, the impact of technique at higher temperature and voltages shows negligible effect on read current with about 8 % reduction in read current at 1.1 V and FF corner.
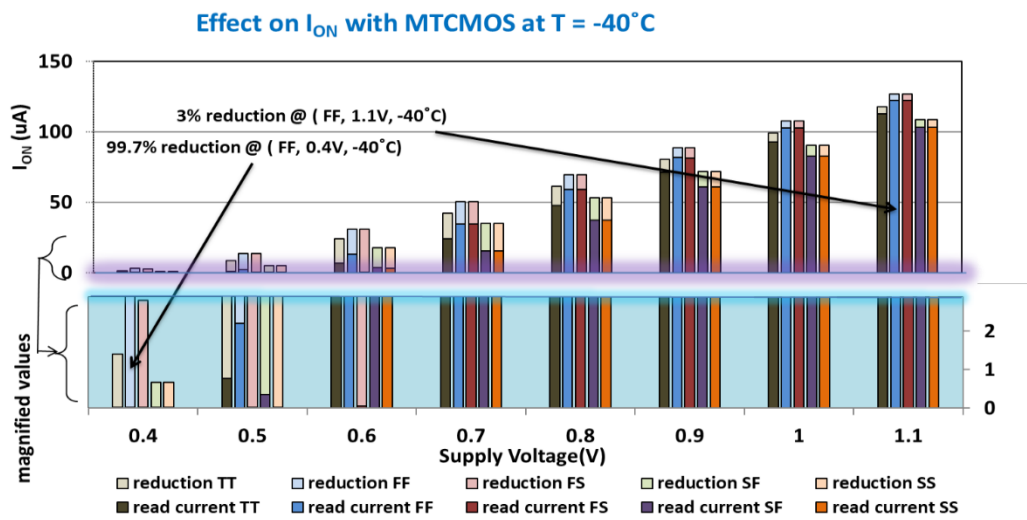
(a)
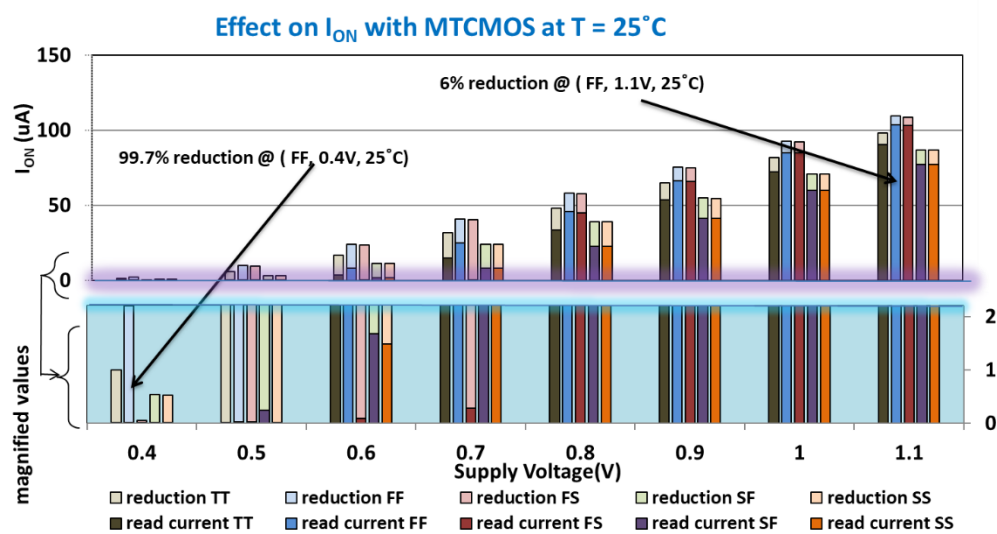
(b)
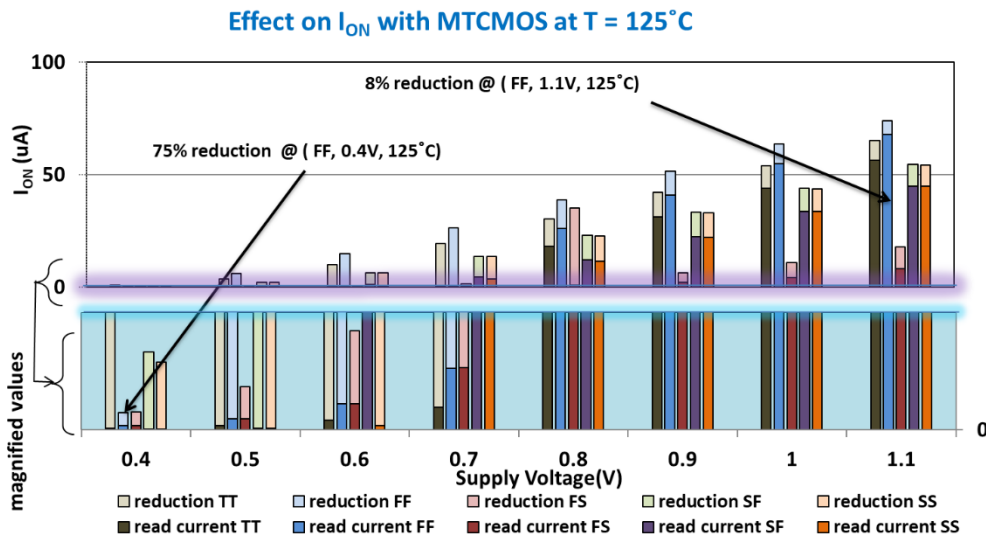
(c)

Fig. 2.6 Effect on I_ON with MTCMOS technique at (a) -40 ℃ (b) 25 ℃ (c) 125 ℃

Impact on hold stability : The HSNM of all the SRAM cells is measured and the percentage change in the HSNM with respect to the conventional cell is plotted in Fig. 2.7. The MTCMOS based cell (Fig. 2.7(a)) shows improvement in HSNM values at all corners at 1.1 V with up to 19 % improvement at FF corner.
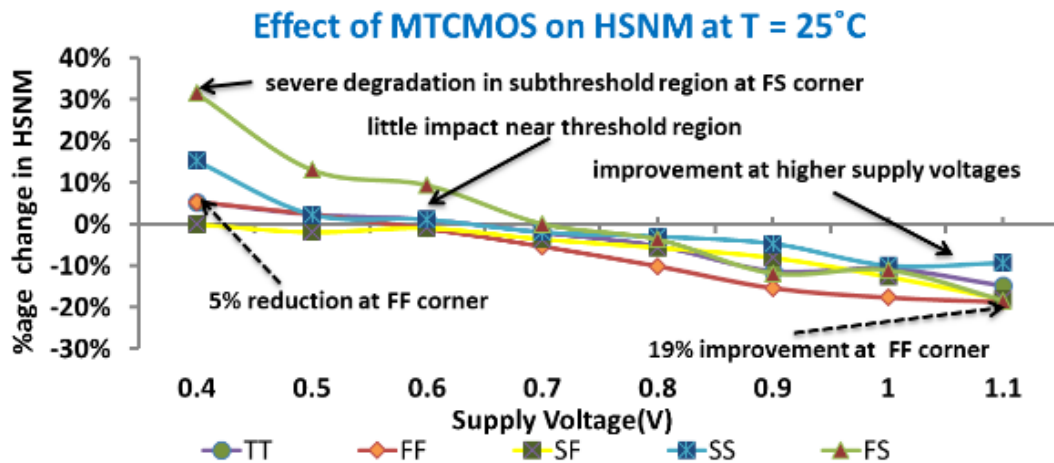
(a)
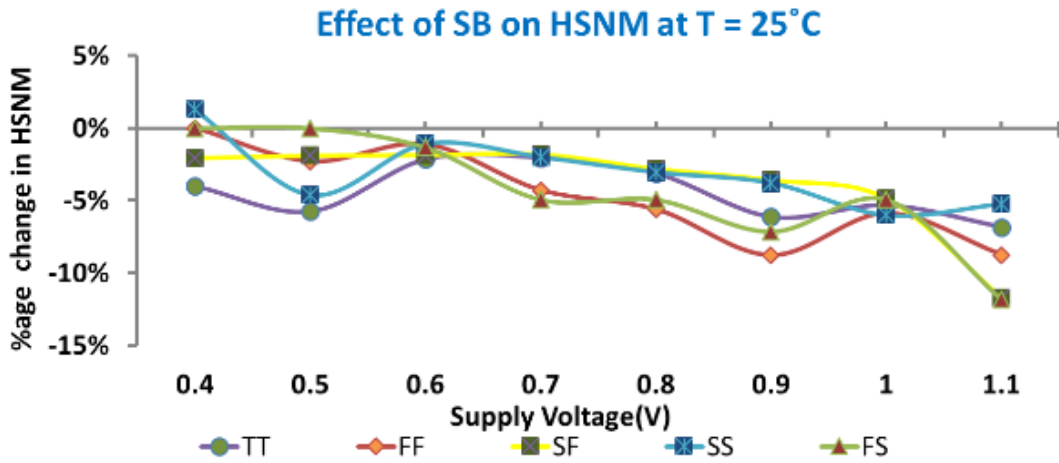
(b)
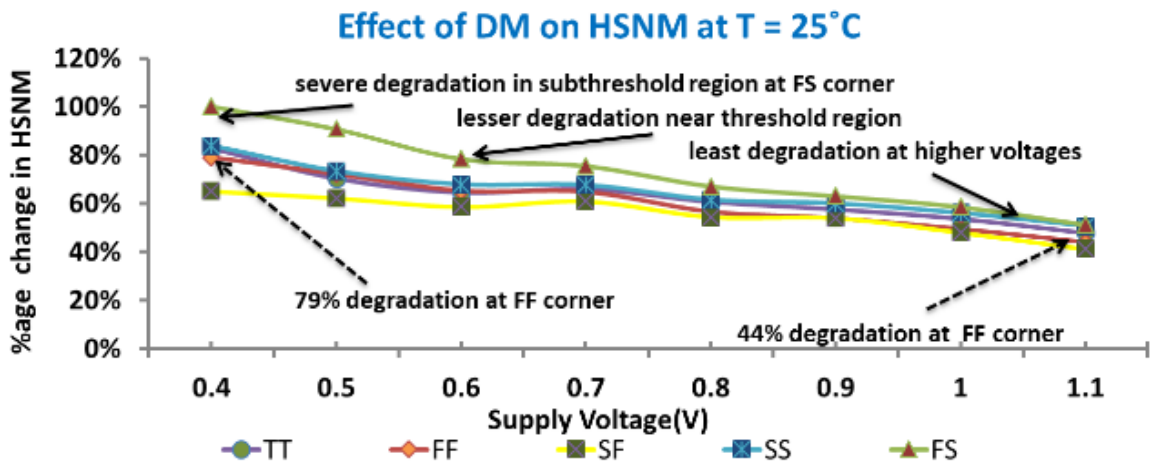
(c)

Fig. 2.7 Effect on HSNM at 25 ˚C

However, as the supply voltage scales down, the HSNM degrades with up to 31 % reduction

in the sub-threshold region making the stored data unstable. In SB technique (Fig. 2.7(b)),

significant improvements are observed in HSNM with respect to conventional SRAM cell

at all voltages with up to 12 % improvement at SF corner. Even as the supply voltage scales

down, no significant degradation of HSNM values is seen at 0.4 V. The dynamic variation

of supply voltages in DM technique leads to substantial reduction in HSNM of the cell

thereby making cell unsteady in hold mode. The plots in Fig. 2.7(c) confirms the

preposition. The severe degradation in HSNM of the 6T SRAM cell in the presence of this technique especially in sub-threshold region poses a challenge and makes it unsuitable at lower voltages.

Performance comparison : The simulative investigations on latch leakage reduction techniques are summarized in Table 2.1 for quick access. The techniques have been compared based on read performance and hold stability in addition to the leakage reduction capabilities in order to determine the best suitable operating conditions in which the corresponding technique can be used. It can be observed from the results that MTCMOS and DM techniques are more suitable at high supply voltages with MTCMOS preferable at high temperatures. The SB technique, on the other hand, shows moderate performance throughout the supply voltage and temperature range. In addition, none of the technique is tolerant to PVT-variations.

Table 2.1: Performance comparison of latch leakage reduction techniques [48][84][95][99-101]

Techniques	MTCMOS	SB	DM
Leakage	Overall good but more effective at low voltages	Less effective compared to other two and shows better impact at high voltages	Less effective than MTCMOS and shows better impact at high voltages
Read current	Decreases at low voltages	No impact	No impact
Hold stability	Decreases at low voltages	No much impact	Severe degradation at low voltages
PVT-variation tolerant	No	No	No
Suitable temperature	High temperatures	-40 ˚C to 125 ˚C	-40 ˚C to 125 ˚C
Suitable supply voltage	High voltages	0.4 V to 1.1 V	High voltages
Remarks	No area overhead. Requirement of additional implant processing steps.	Requirement of twin or triple well processes and extra time to bias the wells properly.	Area overhead. Requirement of multiple supply rails. Extra time to switch between drowsy and non-drowsy mode.

The performance evaluation of all the leakage reduction techniques for SRAM cells is carried out at different technology nodes in sub-threshold region and 25 ˚C. The SRAM

cell performance parameters namely RSNM, WM and DRV are also considered for completeness. The results with and without techniques are captured and changes observed in percentages at different technology nodes are summarized in Table 2.2. The results for latch leakage reduction techniques indicate that the efficacy of MTCMOS technique in suppressing leakage current remains significant across the technology nodes in comparison to SB and DM techniques. It is also noted that MTCMOS technique being static in nature has degrading effect on read stability of the SRAM cell. However, a significant improvement in write ability and minimum retention voltage is also observed. Additionally, a significant improvement in minimum retention voltage and severe degradation in hold stability are also observed with SB and DM techniques respectively.

Table 2.2: Comparison of latch leakage reduction techniques at different technology nodes [48][84][95][99-101]

Techniques	MTCMOS			SB			DM		
	90 nm	65 nm	32 nm	90 nm	65 nm	32 nm	90 nm	65 nm	32 nm
Leakage	-97.0 %	-94.4 %	-90.5 %	-75.9 %	-74.1 %	-45.2 %	-12.8 %	-17.1 %	-54.1 %
Read current	-93.8 %	-99.9 %	-99.8 %	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect
Hold stability	-3.8 %	-5 %	-5.3 %	+6 %	+5 %	+4 %	-75 %	-78 %	-83 %
Read stability	-74.6 %	-61.9 %	-99.9 %	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect
Write ability	+106.3 %	+102.7 %	+83.2 %	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect
Minimum retention voltage	-70.2 %	-62.1 %	-45.3 %	-37.9 %	-31.8 %	-20.9 %	Negligible Effect	Negligible Effect	Negligible effect

2.3.2. Bitline leakage reduction techniques [38][49-50][74][81][84][99][102-105]

A typical SRAM array has memory cells arranged in rows and columns such that all the cells in a particular column perform memory operation through common bitlines (BL, BLB). During a read operation, read current I_{ON} and bitline leakage current I_{BL_LEAK} flow through the accessed cell and the un-accessed cells respectively in a column as depicted in Fig. 2.8(a).

(a)

(b)

42

(c)
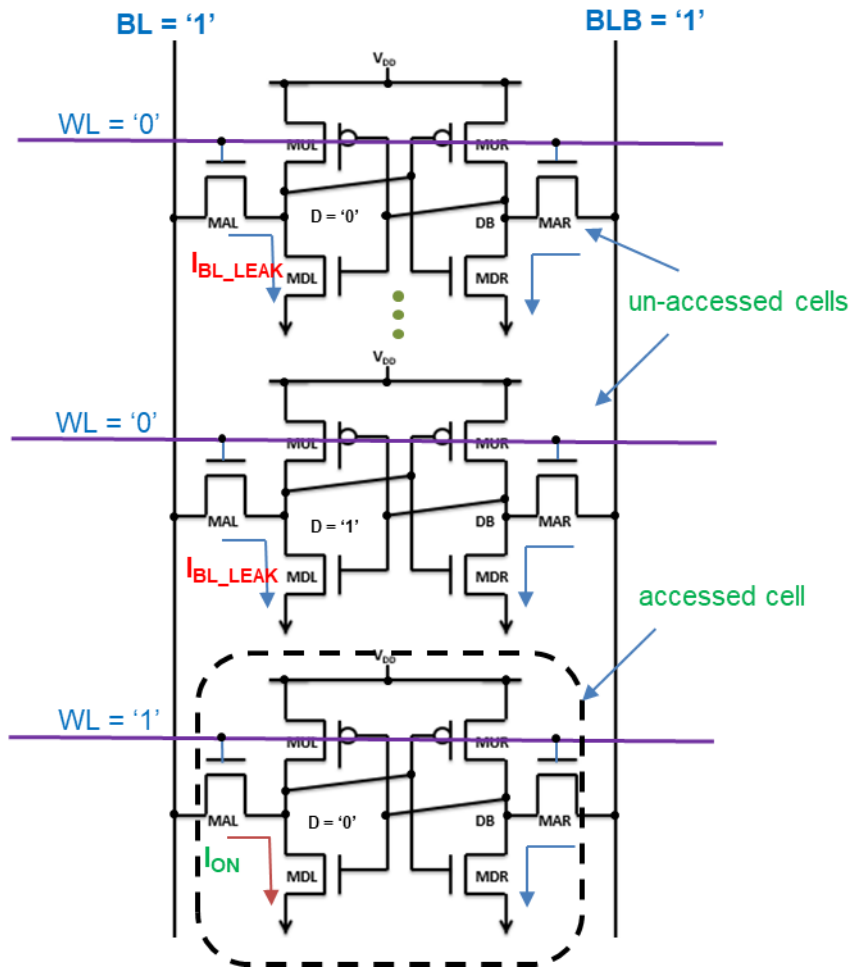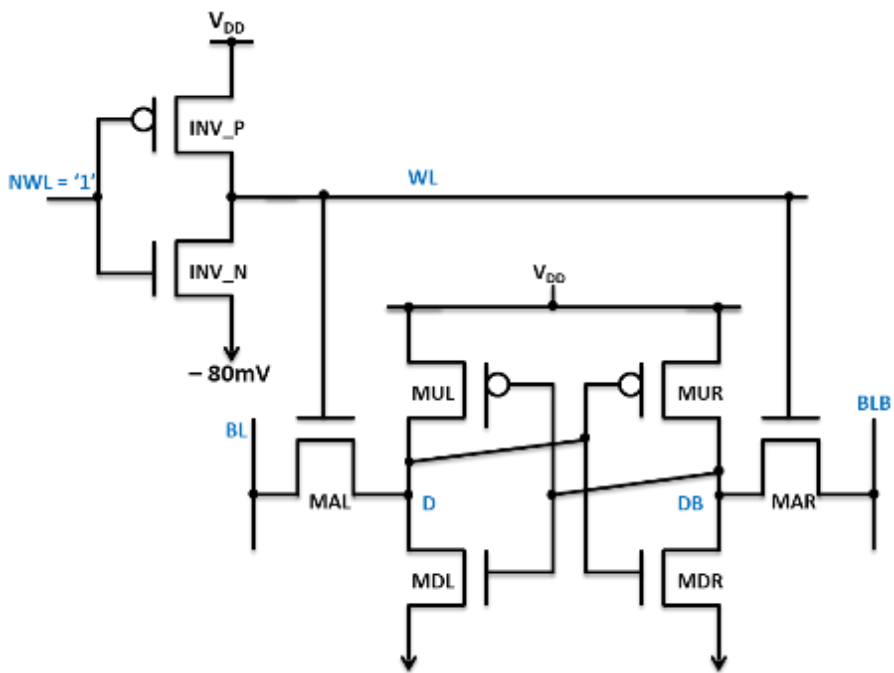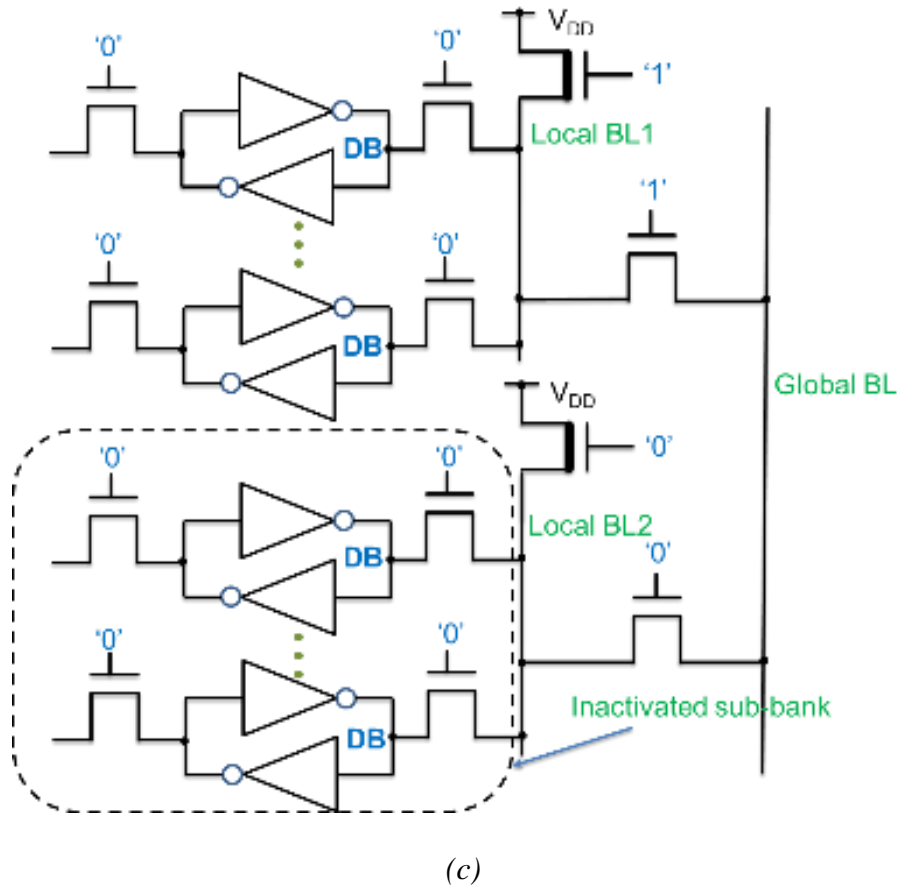
Fig. 2.8 (a) Flow of current in accessed and un-accessed cells (b) Schematic of 6T SRAM cell with NWL technique (c) Sub-banks with LBB technique in Hierarchical bitline architecture

The value of bitline leakage current I_{BL_LEAK} depends on the data value stored at the corresponding internal nodes (D or DB) in un-accessed cells [50]. It is worth mentioning that the leakage current I_{BL_LEAK} is higher when logic '0' is stored at node D than the case when it stores '1'. As the number of cells sharing the bitline increases, the ratio I_{ON}/I_{BL_LEAK} decreases which in turn leads to higher read failures [49]. This imposes limitation on the number of SRAM cells that may be connected in a particular column in high density SRAMs [99]. The bitline leakage reduction techniques are very useful in such cases. In this sub-section, the techniques for reducing the bitline leakage current are covered. The first obvious technique is to downsize the access transistors but it directly impacts the read and

write performance of SRAM cell so it is not a preferred choice. Alternate techniques and their advantages are discussed further.

2.3.2.1. Negative Wordline technique (NWL) [38][74][81][99][102]

In this technique, the access transistors are biased in super cut-off region by applying a negative gate voltage instead of GND during the hold mode as shown in Fig. 2.8(b). In SRAM cell based on NWL technique, an additional inverter (INV_P, INV_N) generates an appropriate WL signal to drive the access transistors. In the hold mode, negative gate-to-source voltage lowers the leakage current due to their exponential relationship in this region. Conversely, in read or write mode, the gate voltage is set to the nominal value as in conventional structure to achieve same performance.

2.3.2.2. Leakage biased bitline technique (LBB) [103-105]

The LBB technique is applicable to memories with hierarchical bitline architecture that comprises of sub-banks each having an individual set of local bitlines and pre-charge circuit. In this arrangement, only one sub-bank is activated at any given instance and others remain inactivated. A significant leakage current flows in the inactivated memory sub-banks. This current can be reduced by following LBB technique wherein pre-charge nMOS transistors with high threshold voltage is added in each sub-bank as shown in Fig. 2.8(c). It remains OFF in inactivated sub-banks while it conducts in the activated sub-bank. The local bitlines are in floating state in inactivated sub-banks and are biased at random voltage levels depending on the leakage from the un-accessed cells. In other words, the leakage current self-bias the bitlines of an inactivated sub-bank. In the figure as can be seen (Fig. 2.8(c)) the local BL2 of the inactivated sub-bank is disconnected from the pre-charge supply by keeping the nMOS pre-charge transistor OFF. By assuming the case that logic zero is stored (DB = '0') in all the cells then the Local BL2 will be biased to GND due to

leakage current. Similarly, if all the cells store logic '1' then Local BL2 will be biased at V_{DD}. If half of the cells store '0' then the local BL2 will be biased somewhere at $V_{DD}/2$. Thus, the local bitline voltage is random and depends on the data stored in the column. It is observed that the technique results in memory array with lower leakage currents.

2.3.2.3. Comparative analysis

The SRAM based on the above techniques is implemented and the values of I_{BL_LEAK}, I_{ON}/I_{BL_LEAK} ratio and HSNM are measured. The simulations for the conditions specified earlier are performed and the corresponding results are plotted in Fig. 2.9 to Fig. 2.11. For NWL technique, a negative voltage generator of -80mV is used. For LBB technique, the theoretical concept is verified by simulating a column of SRAM cells storing equal number of ones and zeroes. In this condition the Local BL get biased at $V_{DD}/2$.

Leakage reduction capabilities : At -40 ˚C, the NWL technique achieves 69.2 % leakage reduction at 1.1 V which further increases to 80.9 % at 0.4 V as shown in Fig. 2.9(a). The opposite trend is observed with LBB technique, which offers 92.9 % reduction at 1.1 V and reduces to 62.2 % reduction at 0.4 V as depicted in Fig. 2.9(b). Thus, at lower temperatures, NWL technique gives best results at lower voltages while LBB technique gives best results at higher voltages. The plots for the I_{BL_LEAK} with PVT-variations at 25 ˚C (Fig. 2.10) reveals the same trend as at -40˚C. With further increase in temperature to 125 ˚C, a decrease in percentage leakage reduction in I_{BL_LEAK} is observed (Fig. 2.11) for both the techniques over the entire voltage range. The percentage leakage reduction is 75 % and 47.1 % at 0.4 V at maximum leakage corner with NWL and LBB techniques respectively. It is worth mentioning that both the techniques provide same leakage performance at SS-SF and FF-FS corners at all temperatures.

Reduction in I_{BL_LEAK} with NWL at T = -40°C

80.9% reduction @ (FF,0.4V, -40°C)

69.2% reduction @ (FF,1.1V, -40°C)

(a)

Reduction in I_{BL_LEAK} with LBB at T = -40°C

62.2% reduction @ (FF,0.4V, -40°C)

92.9% reduction @ (FF,1.1V, -40°C)
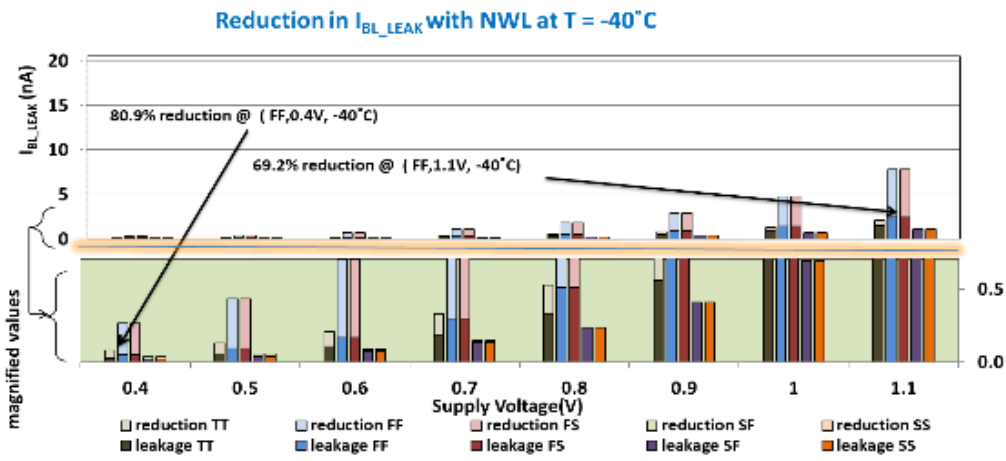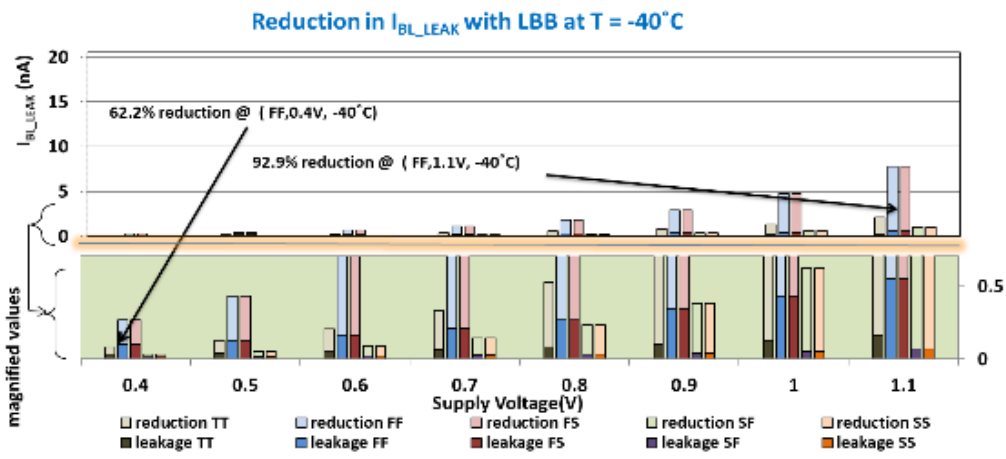
(b)

Fig. 2.9 Effect on I_{BL_LEAK} at T = -40 °C

Reduction in I_{BL_LEAK} with NWL at T = 25°C

78.2% reduction @ (FF, 1.1V, 25°C)

82.9% reduction @ (FF,0.4V, 25°C)

(a)

46
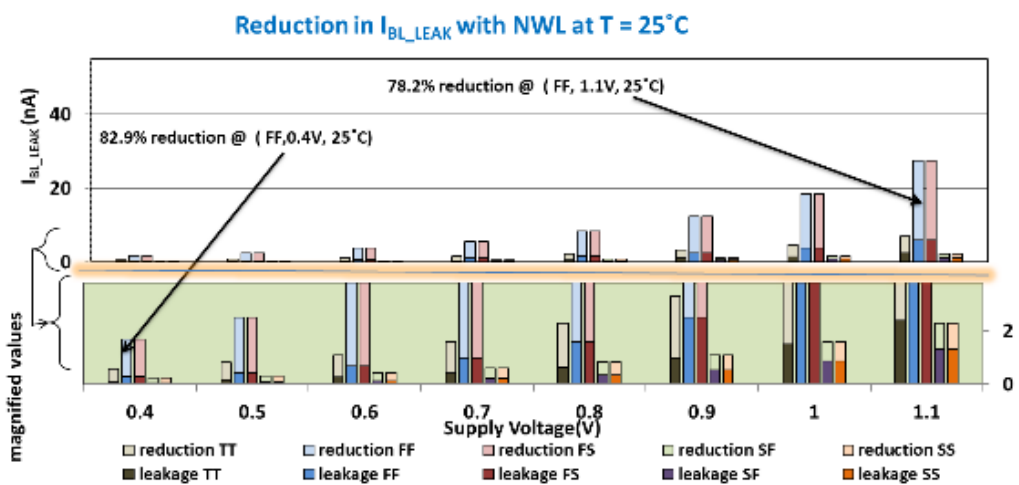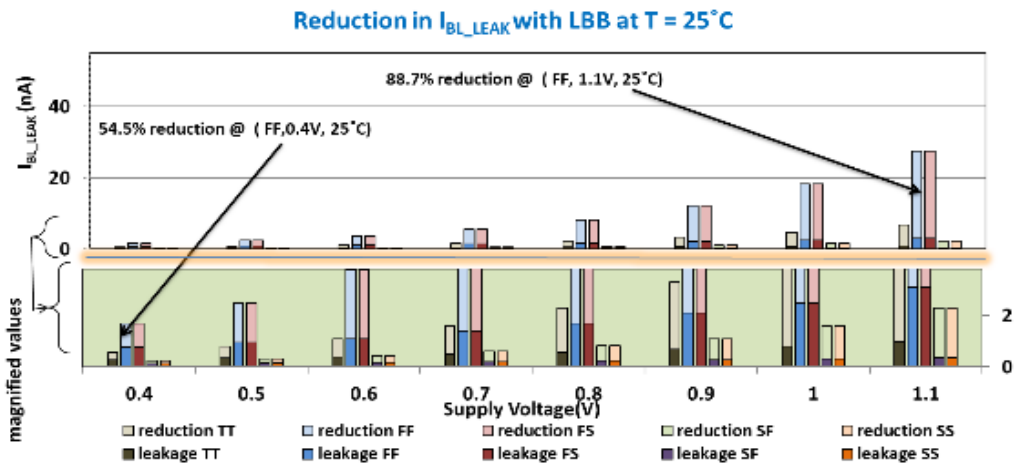
(b)

Fig. 2.10 Effect on I_{BL_LEAK} at T = 25 ˚C
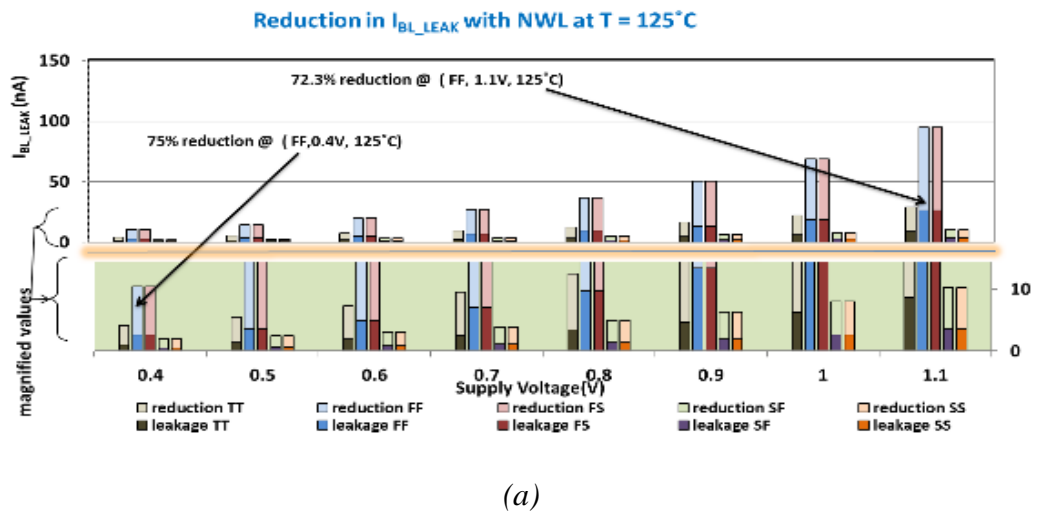
(a)
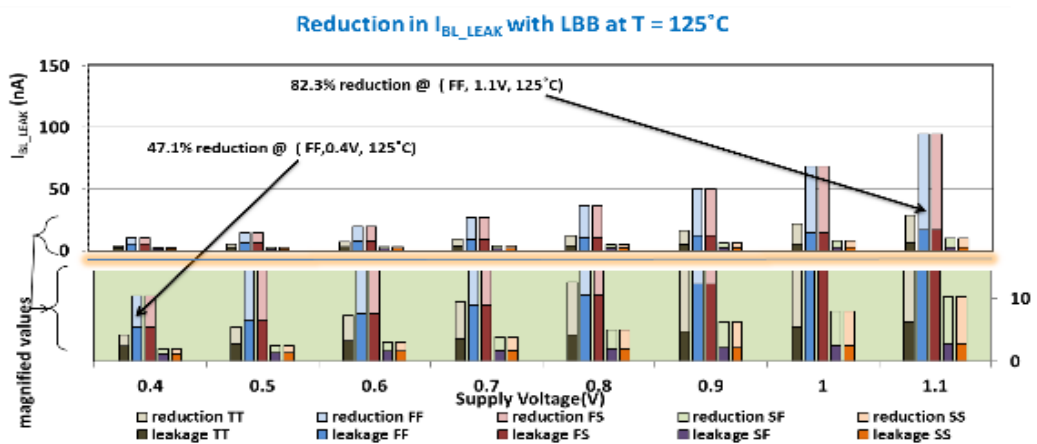
(b)

Fig. 2.11 Effect on I_{BL_LEAK} at T = 125 ˚C

Impact on read performance : The read performance of NWL technique evaluated in terms of I_{ON}/I_{BL_LEAK} ratio improves as the temperature increases from -40 ˚C to 25 ˚C and then degrades with further increase in temperature as demonstrated in Fig. 2.12. The degradation at high temperatures is due to reduced I_{ON} values superimposed with inability of the technique to suppress leakages at these temperatures. Also, an improving trend as supply voltage scales from 1.1 V to 0.4 V is also inferred.

(a)

(b)
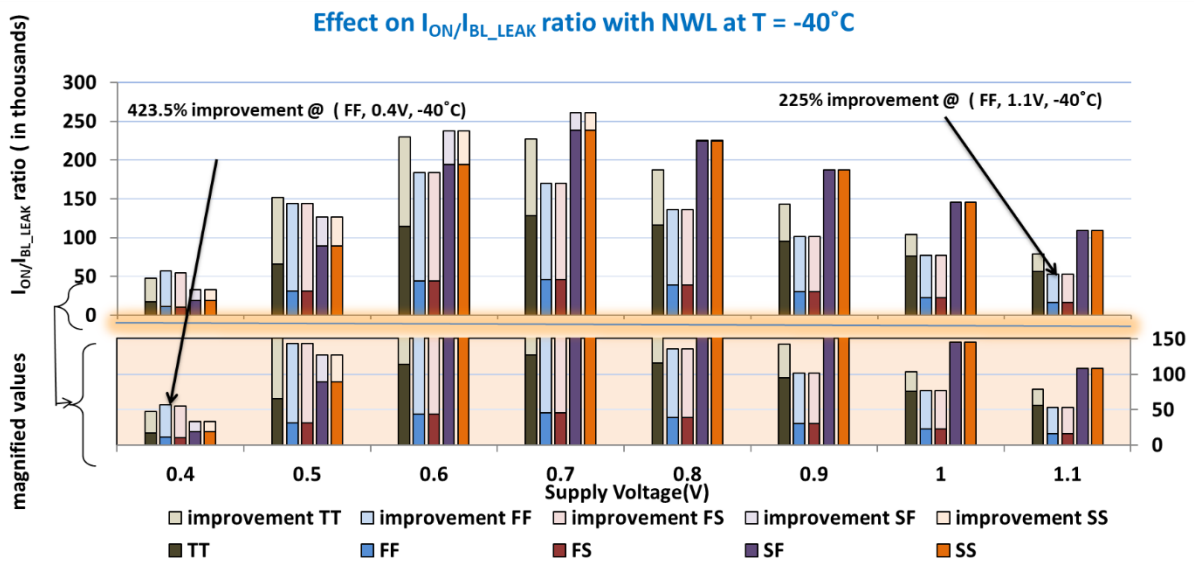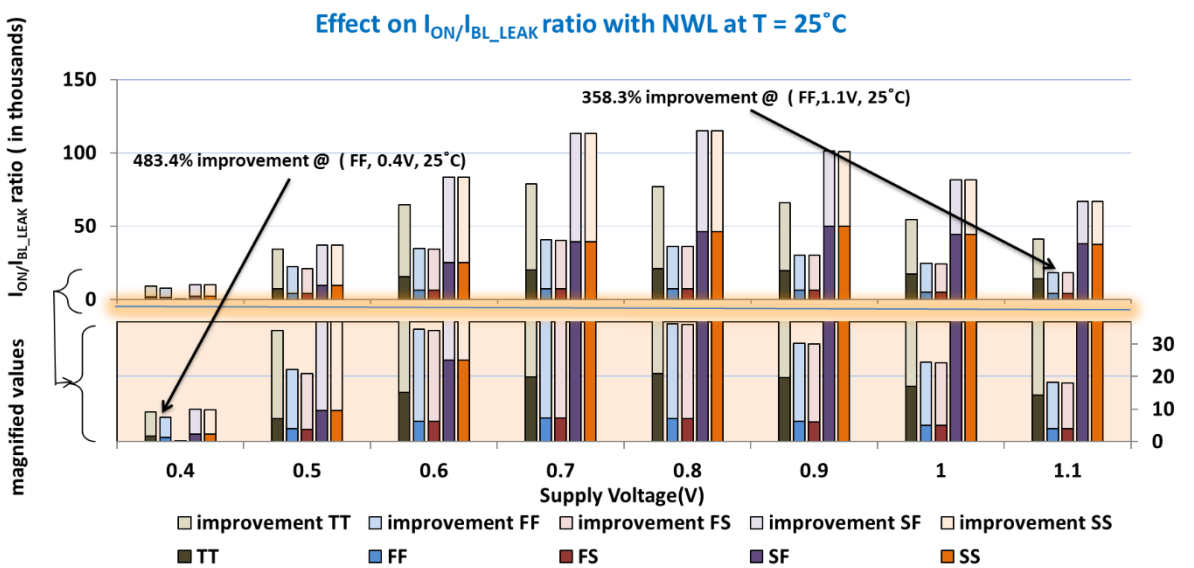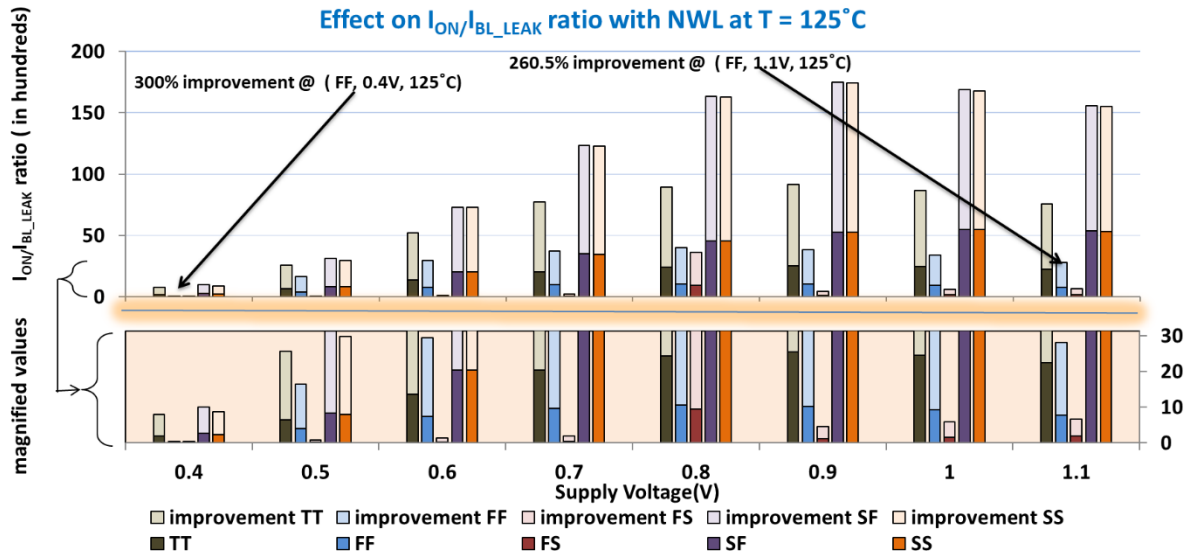
Fig. 2.12 Effect on I_{ON}/I_{BL_LEAK} ratio with NWL technique

Thus, it becomes clear from the results that the NWL technique offers the best read performance at moderate temperatures and lower voltages particularly in sub-threshold region. The LBB technique is not considered since it focuses on the leakage reduction in inactivated sub-banks.

Impact on hold stability : The HSNM results for the cells at 25 ˚C are plotted in Fig. 2.13. The results (Fig. 2.13(a)) show that NWL technique has negligible effect on noise immunity of the cell especially at 0.4 V. However, a degradation in HSNM near 0.6 V at FF corner is observed. The HSNM results for LBB technique (Fig. 2.13(b)) show that like NWL technique it exhibits insignificant impact on HSNM, except for a slight degradation at SS corner near 0.4 V.

(a)

(b)
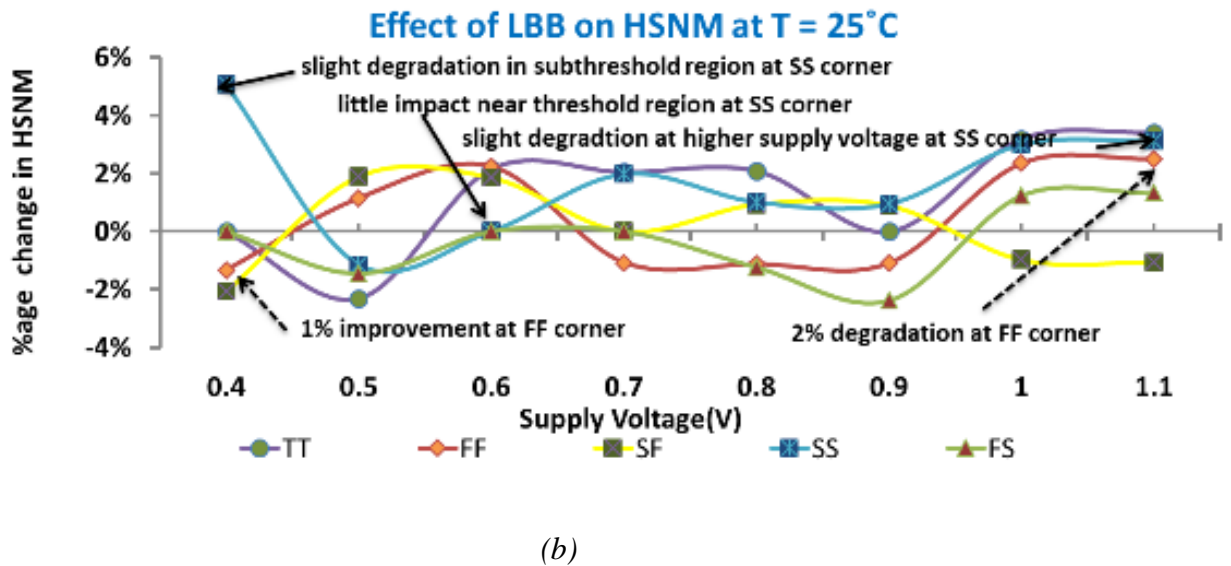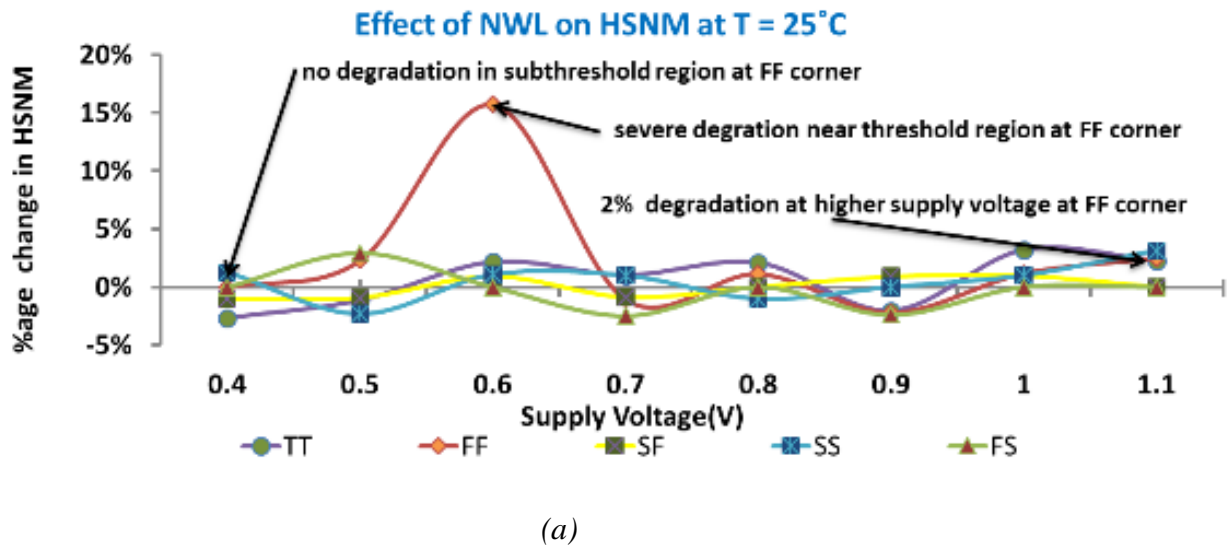
Fig. 2.13 Effect on HSNM at 25 ˚C

Performance comparison:

The performance of bitline leakage reduction techniques is outlined in Table 2.3 for quick comparison. The results indicate that the NWL technique is more suitable at low supply voltages and moderate temperatures whereas the LBB techniques is more appropriate for use at high supply voltages and low temperatures. Both, the techniques show improved tolerance to PVT-variations.

Table 2.3: Performance comparison of bitline leakage reduction techniques [84][104-105]

Techniques	NWL	LBB
Leakage	Overall good but more effective at low voltages	Overall good but more effective at high voltages
Read current to leakage current ratio	Improves at all voltages	No impact
Hold stability	Degradation at moderate voltages	Slight degradation at low voltages
PVT-variation tolerant	Yes	Yes
Suitable temperature	Moderate temperatures	Low temperatures
Suitable supply voltage	Low voltages	High voltages
Remarks	Good alternative to HVT MOS transistors at low voltages. Requirement of negative voltage generator.	Can be used to deactivate read paths in SRAM array with decoupled read ports. Pre-charge phase is deferred when the corresponding part of the memory is accessed for read/write operation.

The technology comparison of both bitline leakage reduction techniques for SRAM cells is carried out in sub-threshold region and 25 ˚C. From the results in Table 2.4, it is observed that for the techniques aimed at reducing bitline leakages, the effectiveness of NWL technique remains high in contrast to LBB technique with technology scaling. In addition, a significant improvement in read current to leakage current ratio is noted with NWL technique at the cost of minimum retention voltage. There is no impact of LBB technique on read/write parameters as it focuses on the leakage reduction in inactivated sub-banks.

Table 2.4: Comparison of bitline leakage reduction techniques at different technology

nodes [84][104-105]

Techniques	NWL			LBB		
	90 nm	65 nm	32 nm	90 nm	65 nm	32 nm
Leakage	-87.6 %	-85.2 %	-81.1 %	-27.7 %	-36.5 %	-50.5 %
Read current to leakage current ratio	+703.8 %	+577.8 %	+425.7 %	No Effect	No Effect	No Effect
Hold stability	Negligible Effect	Negligible Effect	Negligible effect	No Effect	No Effect	No Effect
Read stability	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect
Write ability	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect
Minimum retention voltage	+15.7 %	+12.9 %	+12.6 %	No Effect	No Effect	No Effect

2.3.3. Read port leakage reduction techniques [4][24][34][47][49-50][53][56][59][76] [84][89][106-108]

The techniques covered in this sub-section are applicable to SRAM cells with an isolated decoupled read port. The cells maintain a separate read port with a RBL common to all the cells in a column. During a read '0' operation, I_{ON} flows through the pre-charged RBL in the accessed cell to lower the RBL voltage whereas it remains high otherwise. Sense amplifier then senses the change in RBL voltage and produces the valid output. Thus, this arrangement provides SNM-free read operation as now the read current flows through the read port transistors. However, the simultaneous data dependent leakage flow (I_{RBL_LEAK}) in un-accessed cells may lead to the sensing of wrong data levels. Therefore, in the recent years the focus is shifted towards reducing the RBL leakage in read ports [4, 22, 36]. Various techniques, to address I_{RBL_LEAK}, are discussed below:

2.3.3.1. Stack effect [4][47][59][76][107-108]

The Stack effect is one of the commonly used technique to reduce leakages in digital circuits. The approach is inherently static in nature as it provides the reverse biasing effect in both active mode and hold mode. There exists a variety of read ports that are designed on the basis of Stack effect. The read ports with a stack of two (Fig. 2.14(a)) and three transistors (Fig. 2.14(b)) respectively are used in conventional 8T [4] and 9T [47] SRAM

cells. The read port of 9T [47] cell splits the RWL driven MOS transistor M1 of 8T [4] into M1a and M1b to enhance the stacking effect. The additional OFF transistor in un-accessed cells increases the source-biasing effect hence causes lowering of I_{RBL_LEAK} values.

2.3.3.2. Dynamic control of power rails (DCPR) [50]

In this technique, the I_{RBL_LEAK} is suppressed by dynamically controlling the power rails of the read port. A virtually powered four transistor read port is shown in Fig. 2.14(c). It has a CMOS inverter (M1, M2) and transmission gate (M3, M4) whose power supply and control signal voltages are adjusted according to the operating mode of the cell. In the hold mode, the power rails (VVDD and VVSS) of the inverter and pre-charge level of RBL are kept at $V_{DD}/2$. The transmission gate control signals C and CB are set to '1' and '0' respectively thereby isolating the RBL from node 'X'. The voltage at node 'X' is raised to $V_{DD}/2$ via transistor M1 or M2 depending upon the value stored at internal node DB. This makes the potential of drain and source terminals of M3 and M4 equal thereby reducing I_{RBL_LEAK} significantly. During read mode, the power rails VVDD and VVSS are connected to V_{DD} and GND respectively. The control signal C is set to '0' whereas the complementary control signal CB is set to '1' thereby connecting the RBL (pre-charged to $V_{DD}/2$) to node 'X'. The use of transmission gate in place of single nMOS transistor improves the reading efficiency during read '1' operation.

2.3.3.3. Virtual cell ground (VCG) [4][34][56]

The VCG technique suggests (Fig. 2.14(d)) the use of virtual ground in SRAM cells. In this technique, the virtual ground terminal (RGND) of the read port is connected to high voltage during hold and write modes and to GND during read mode. The effect of such an arrangement is the significant reduction in I_{RBL_LEAK} due to reduced drain to source voltage across the read port. This technique is versatile in the sense that it can be applied to the

SRAM cells with either differential [56] or single ended read ports [4] very easily. The outcome is the significant reduction in I_{RBL_LEAK} and highly improved I_{ON}/I_{RBL_LEAK} ratio that results in tremendous increase in the number of memory cells that can be stacked per RBL.

(a)   *(b)*

(c)   *(d)*
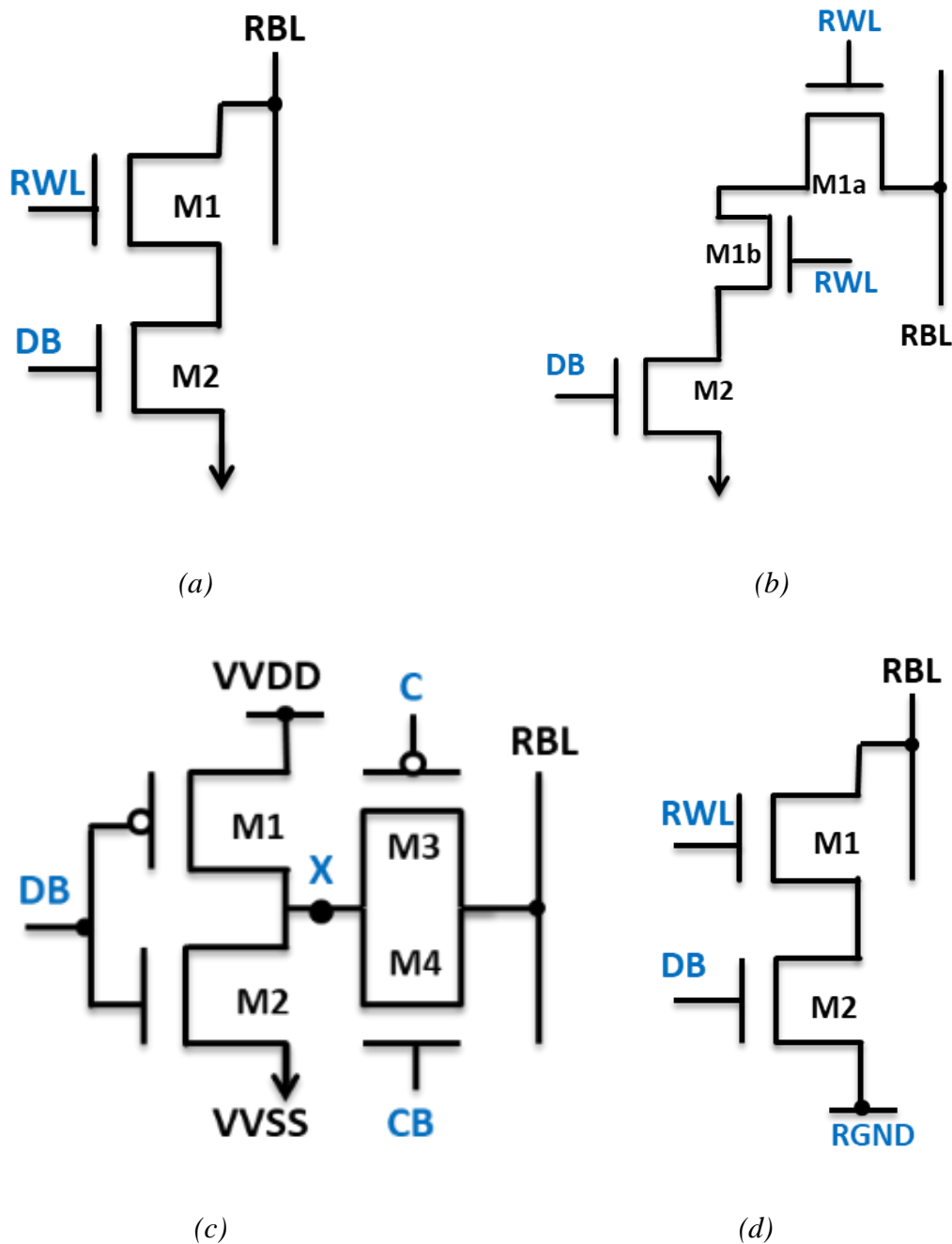
Fig. 2.14 Read ports using (a,b) Stack effect (c) DCPR (d) VCG techniques

2.3.3.4. Comparative analysis

The comparison of all the techniques is done by simulating different SRAM cells with the conditions as previously mentioned (in sub-section 3.1). The results related to leakage reduction capability, read performance and hold stability are discussed in this sub-section.

Leakage reduction capabilities : At -40 ˚C (Fig. 2.15), it can be observed that stacking effect lowers I_{RBL_LEAK} by 93.1 % and 91.1 % at 1.1 V and 0.4 V respectively. The DCPR technique provides 96.1 % leakage reduction at 1.1 V and 85.7 % at 0.4 V while VCG technique reduces leakage by merely 4.8 % at 1.1 V and 72 % at 0.4 V. Therefore, it can be concluded that Stack effect and DCPR techniques are effective over the entire supply voltage range at lower temperatures while VCG technique works well at lower voltages only. As the temperature is increased to 25˚C, Stack effect technique offer higher reduction at high supply voltages whereas it decreases at lower voltages as shown in Fig. 2.16(a). The DCPR technique (Fig. 2.16(b)) on the other hand provides the impeccable performance irrespective of changes in temperature. The performance of VCG technique, improves with increase in temperature as the percentage leakage reduction increases to 30.3% at 1.1 V and 95.4 % at 0.4 V as reflected in Fig. 2.16(c). At 125 ˚C, a similar trend is observed for all the techniques as shown in Fig. 2.17. Therefore, it can be concluded that both Stack effect and DCPR techniques have extremely good leakage reduction capabilities over the entire supply voltage range while VCG technique is good at low voltages particularly in sub-threshold region. It can be seen from the leakage reduction results plotted in Fig. 2.15 to Fig. 2.17 that all the three techniques show same leakage reduction capabilities at FF-FS and SF-SS corners at all temperatures particularly below 0.9 V.
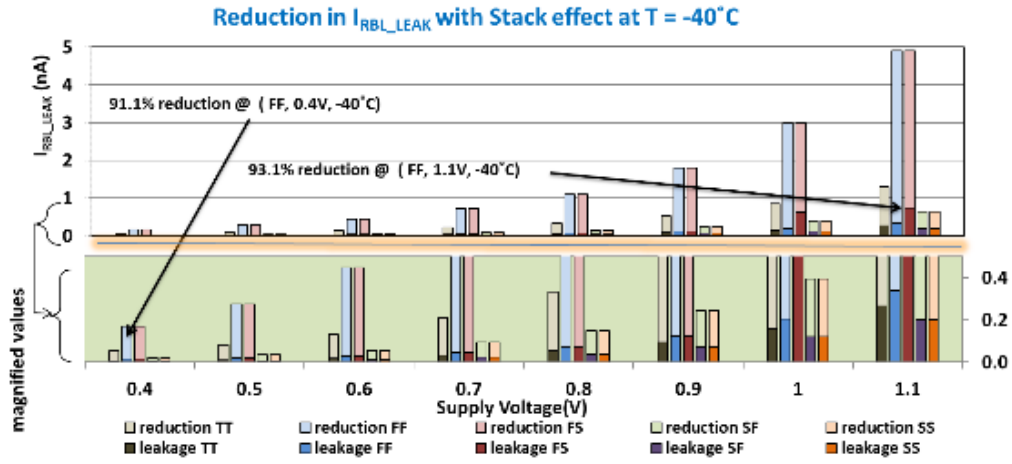
(a)
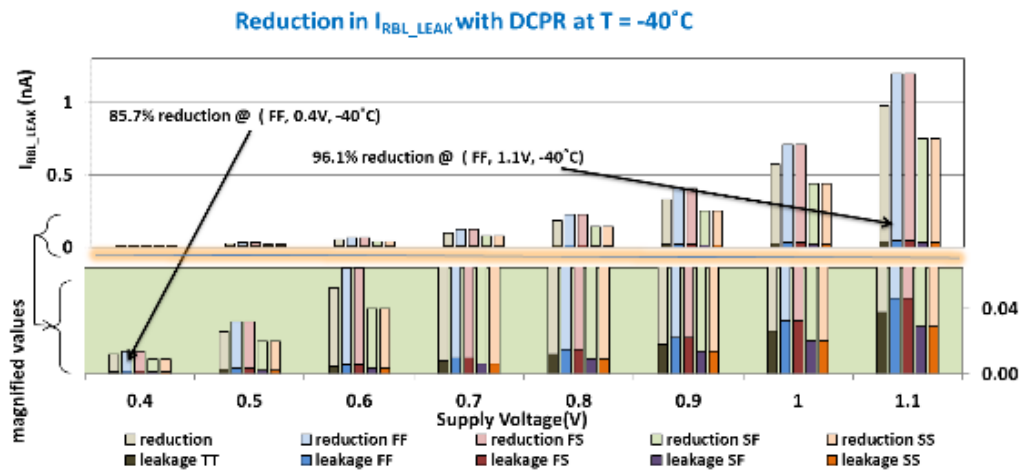
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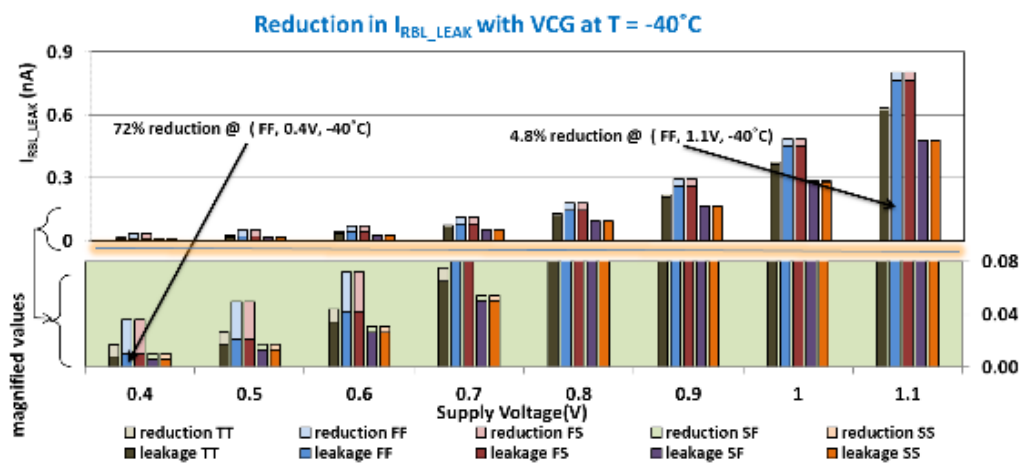
(c)

Fig. 2.15 Effect on I_RBL_LEAK at T = -40 °C

56
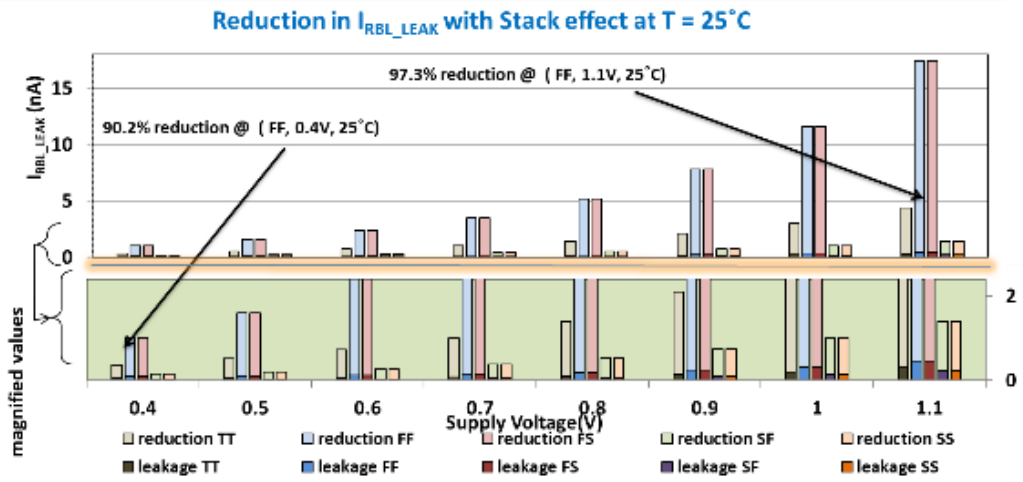
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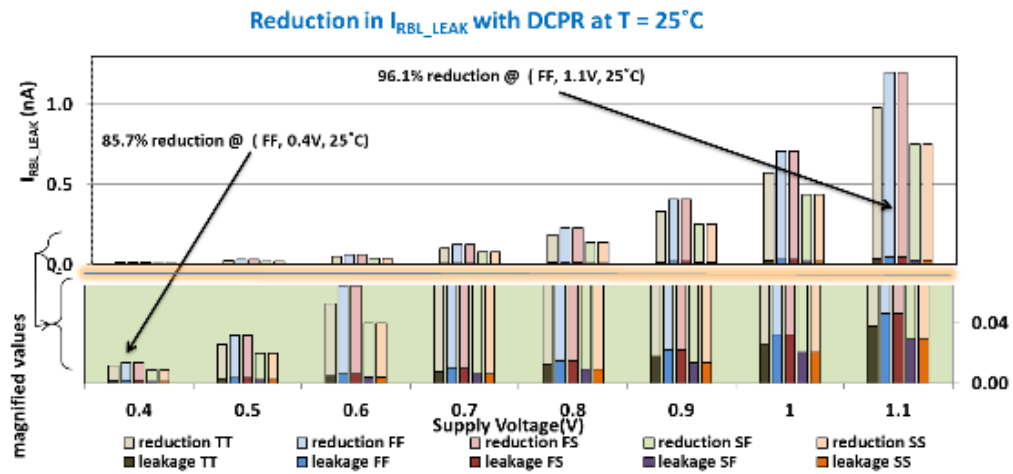
(b)
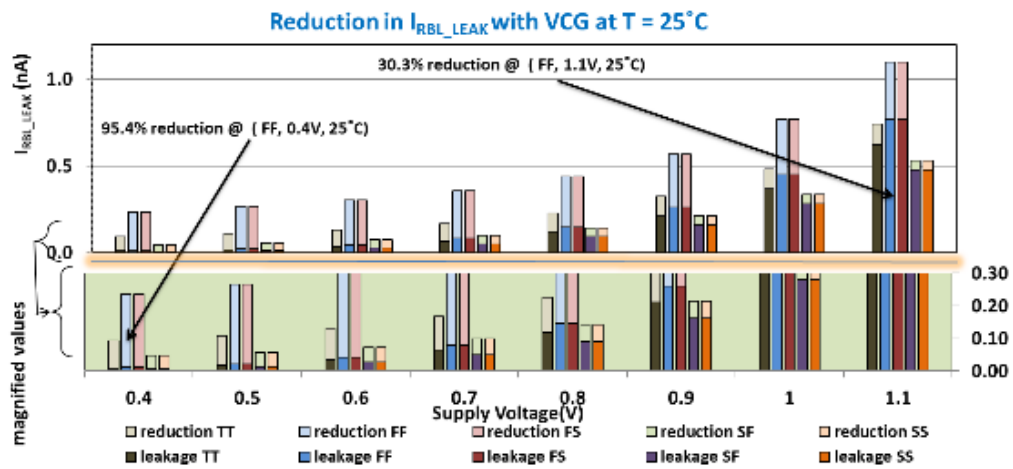
(c)

Fig. 2.16 Effect on I$_{RBL\_LEAK}$ at T = 25 ˚C
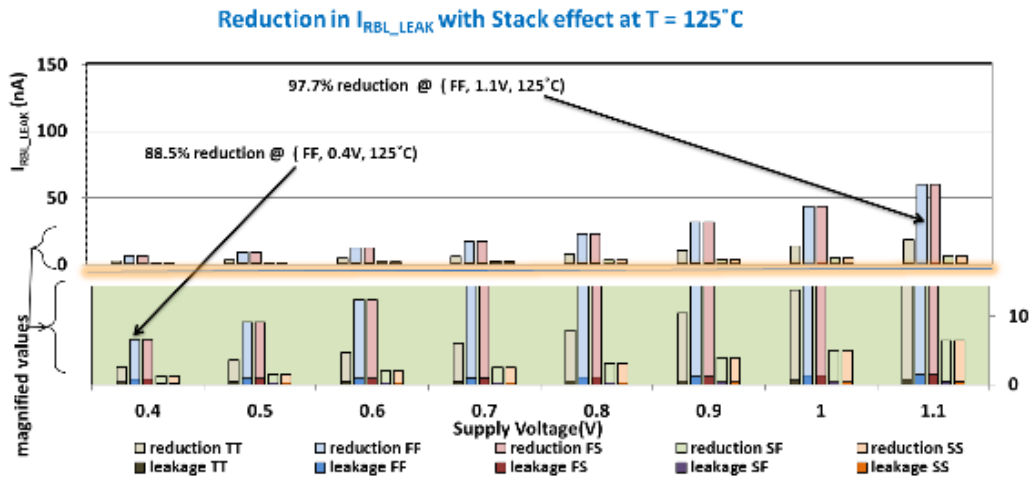
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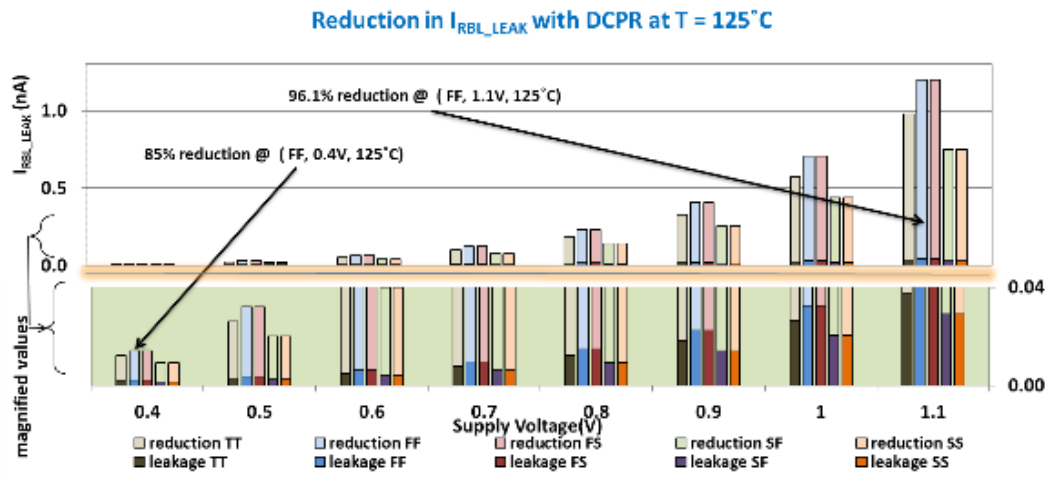
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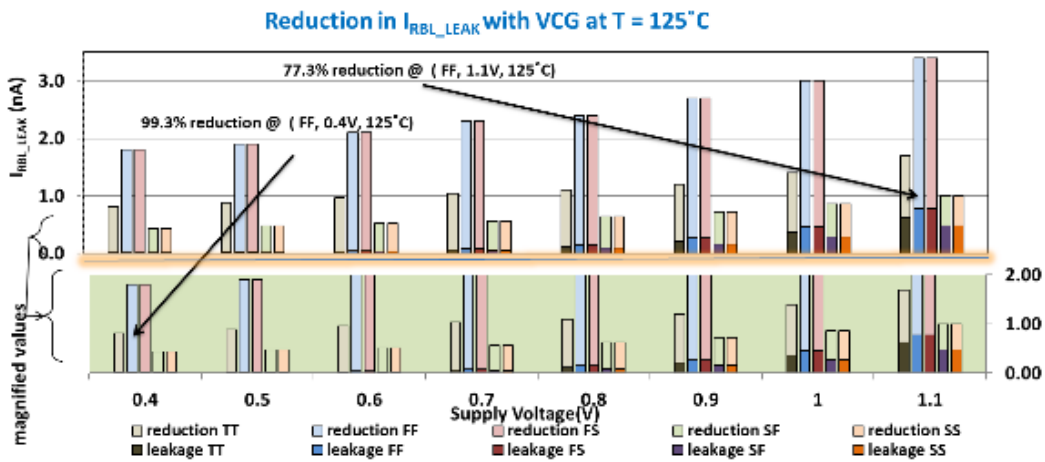
(c)

Fig. 2.17 Effect on I_{RBL_leak} at T = 125 °C

Impact on read performance: The impact of Stack effect, DCPR and VCG techniques on read performance is captured in terms of I_{ON}/I_{RBL_LEAK} ratio and is plotted for -40 ˚C, 25 ˚C and 125 ˚C in Fig. 2.18, Fig. 2.19 and Fig. 2.20 respectively. It can be observed for the read port design, based on Stack effect technique that both I_{RBL_LEAK} and I_{ON} values are reduced at all process corners, temperatures and supply voltages. However, due to more effect on leakages, the improvement in I_{ON}/I_{RBL_LEAK} ratio is achieved irrespective of operating conditions. Since the other two techniques are dynamic in nature so there is no effect on read current values but, due to reduced leakages, there are subsequent changes in I_{ON}/I_{RBL_LEAK} ratio of read port. At -40 ˚C, the percentage improvement in I_{ON}/I_{RBL_LEAK} ratio for Stack effect technique is 477.9 % at 1.1 V and 292.1 % at 0.4 V. With the DCPR technique, improvement in I_{ON}/I_{RBL_LEAK} ratio is 2491.8 % and 600 % at 1.1 V and 0.4 V respectively. Similarly, in case of VCG technique it is merely 5.1 % at 1.1 V and 257.4 % at 0.4 V. It is to be noted that though all the techniques achieve significant improvement in I_{ON}/I_{RBL_LEAK} ratio but out of all three techniques, DCPR technique gives the highest improvement over the entire voltage range. At 25 ˚C (Fig. 2.19), the percentage improvement of Stack effect technique in I_{ON}/I_{RBL_LEAK} ratio increases to 1335.6 % at 1.1 V and reduces to 242.7 % at 0.4 V due to its strong leakage reduction capabilities at high supply voltages and reduced read current values at lower voltages. The performance of DCPR technique remains unchanged with increase in temperature while that of VCG technique improves. For VCG technique, I_{ON}/I_{RBL_LEAK} ratio increases to 43.5 % and 2076.9 % at 1.1 V and 0.4 V respectively. As the temperature increases from 25 ˚C to 125 ˚C (Fig. 2.20), the percentage improvement in I_{ON}/I_{RBL_LEAK} ratio for Stack effect technique further rises to 1439.1 % at 1.1 V and drops to 196.2 % at 0.4 V due to the reasons mentioned earlier. However, as the result shows, the percentage improvement remains significant throughout the voltage range irrespective of temperatures even though it shows

better results at higher temperature. This makes the VCG technique, preferred choice at extremely higher temperatures for achieving high performance with leakage resilience. The DCPR technique keeps on achieving the same performance irrespective of changes in temperature. For VCG technique, significant improvement of more than four orders of magnitude is observed at 0.4 V. Thus, it can be concluded that with extremely good results at lower voltages, the VCG technique is best for use in sub-threshold region at higher temperatures for low power SRAM designs.
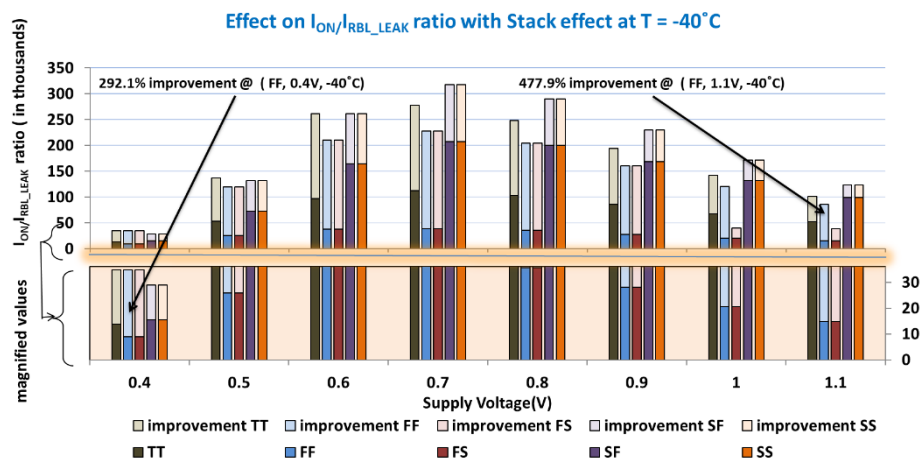
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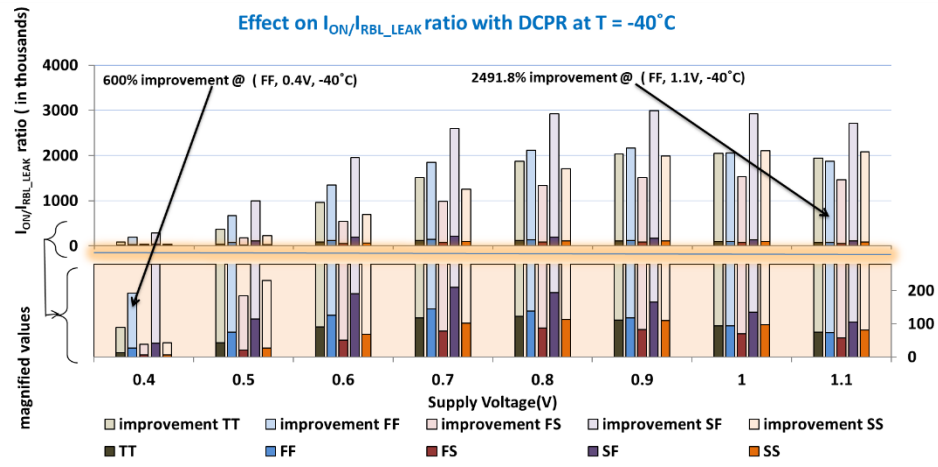
(b)
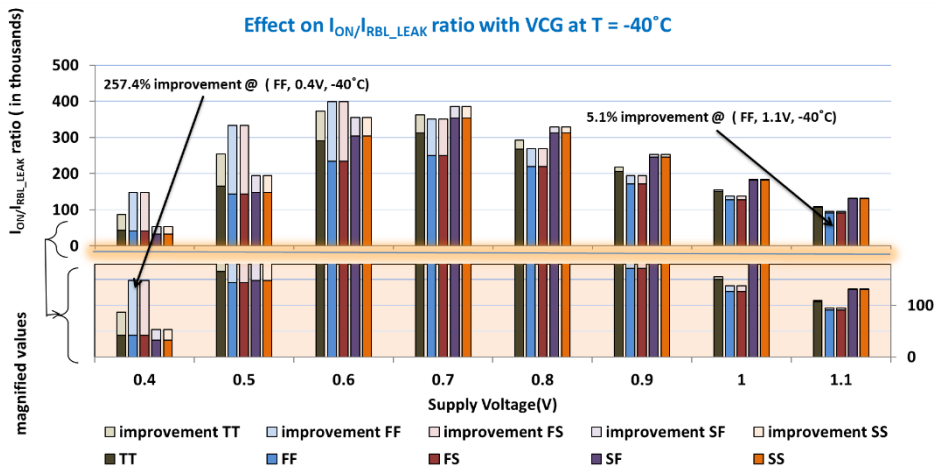
(c)

Fig. 2.18 Effect on I_{ON}/I_{RBL_LEAK} ratio at T = -40 °C
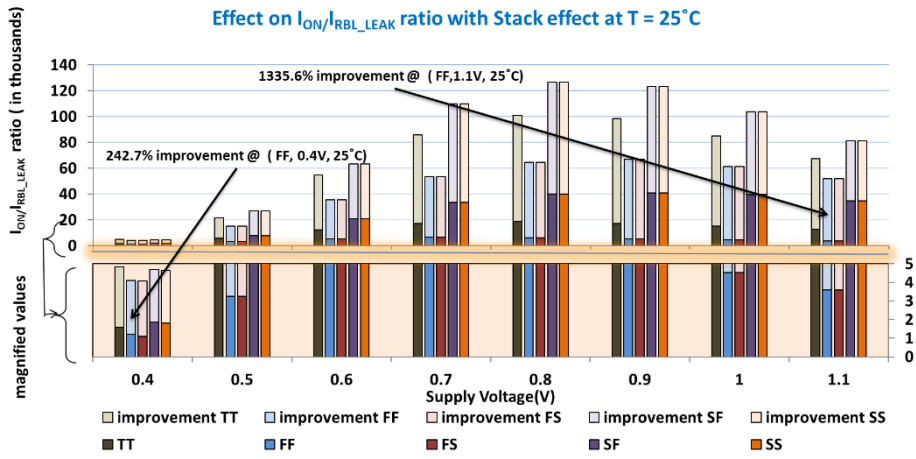
(a)
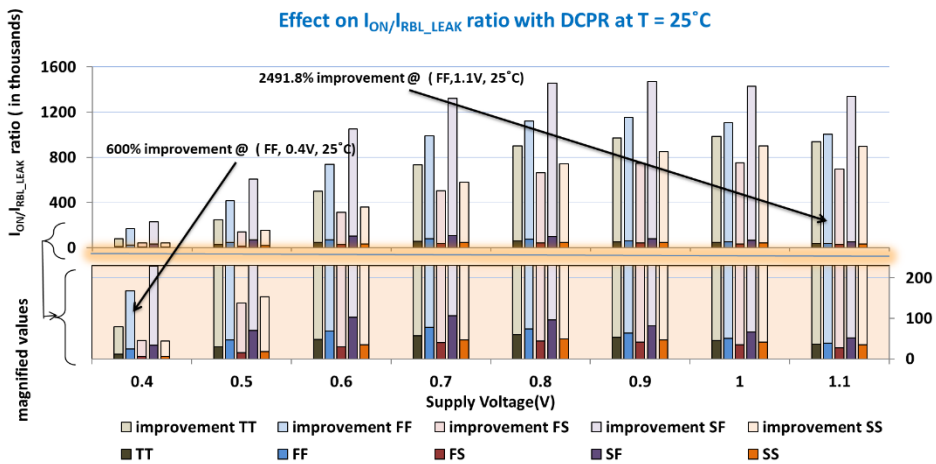
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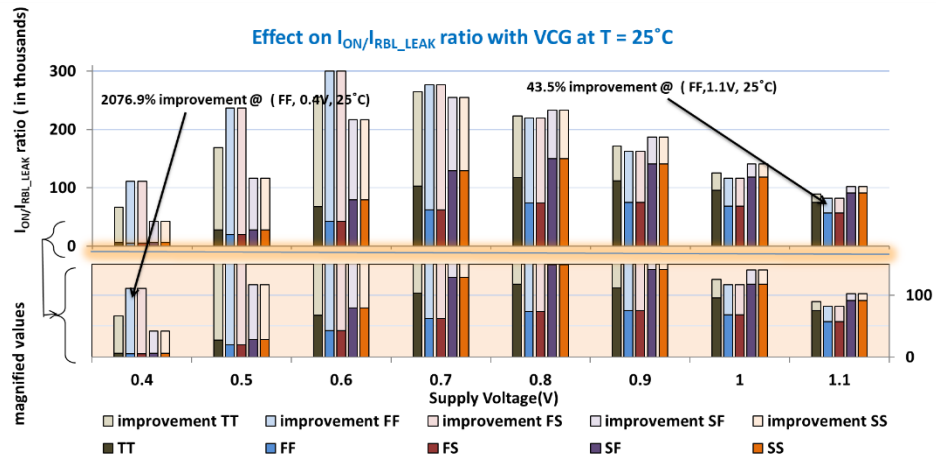
(c)

Fig. 2.19 Effect on I_{ON}/I_{RBL_LEAK} ratio at T = 25 °C
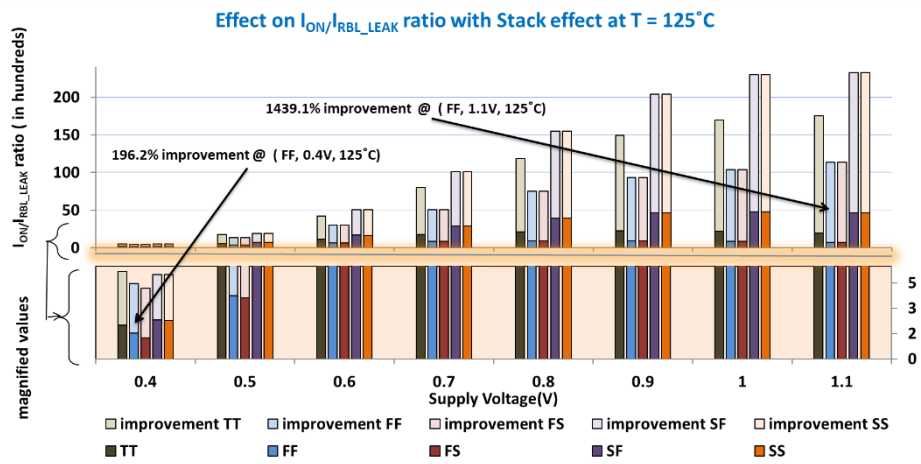
(a)
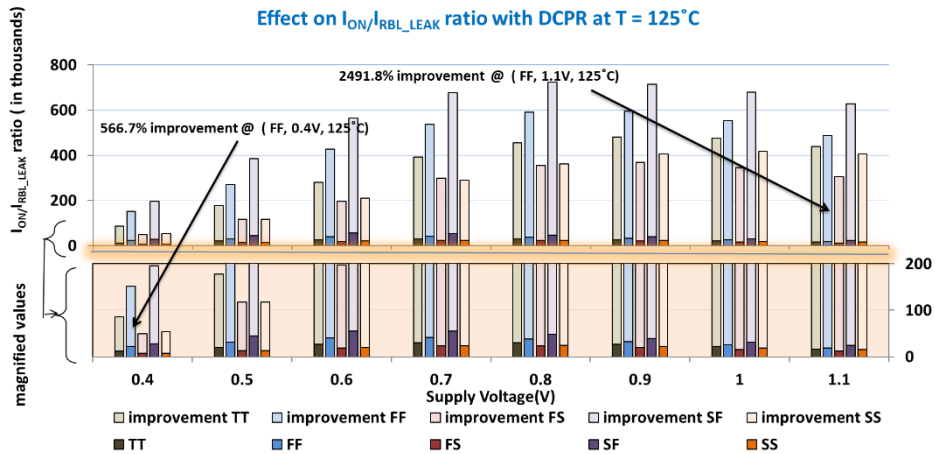
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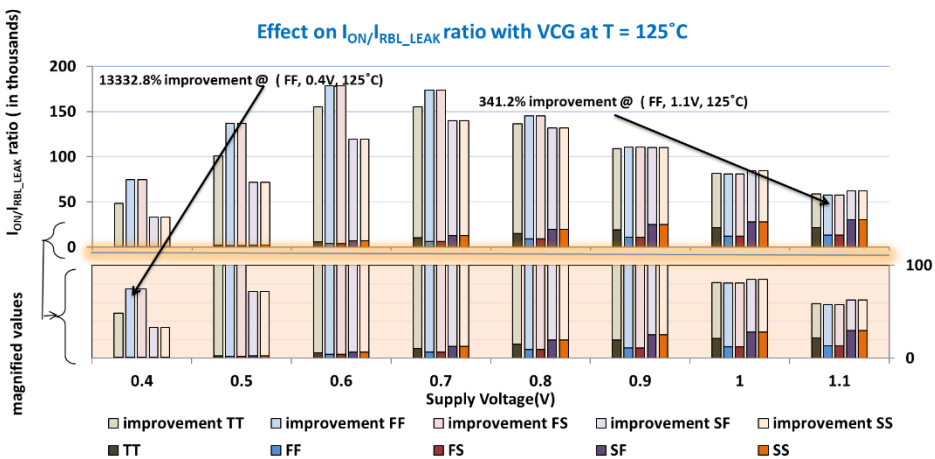
(c)

Fig. 2.20 Effect on I_{ON}/I_{RBL_LEAK} ratio at T = 125 ˚C

Impact on hold stability: The hold stability expressed in terms of HSNM at 25 ˚C for all the techniques is captured and plotted in Fig. 2.21. It is observed that none of the techniques show any effect on HSNM values and the values vary only as corner and/or supply voltage change. Thus, the hold stability is greatly affected by increase in variability and the factors which are internal to the latch such as pull-up, pull-down ratio etc. [24][53].

(a)

(b)

(c)
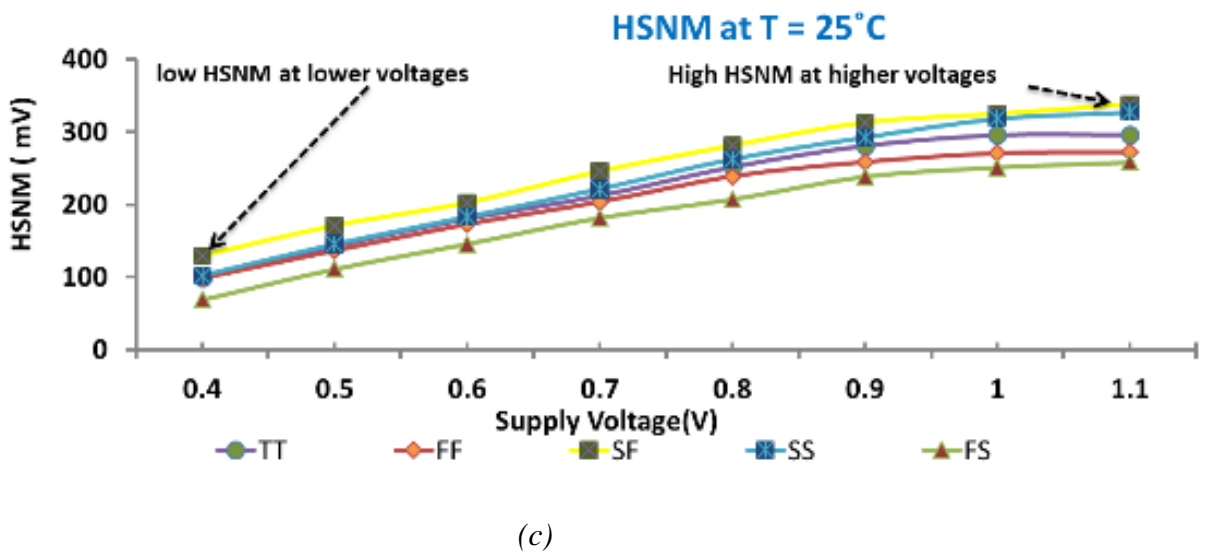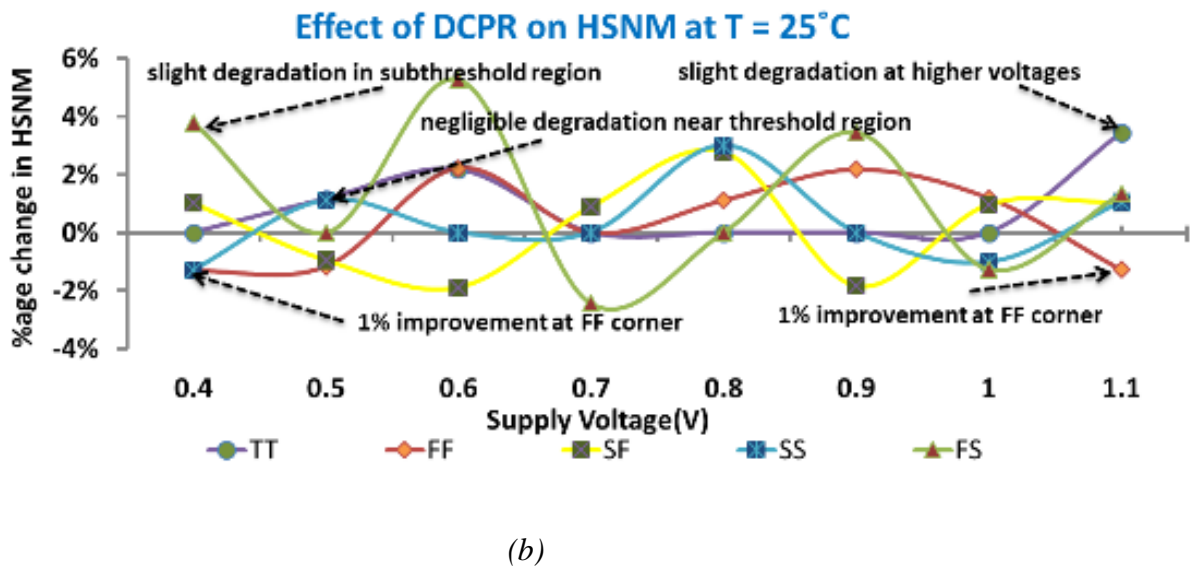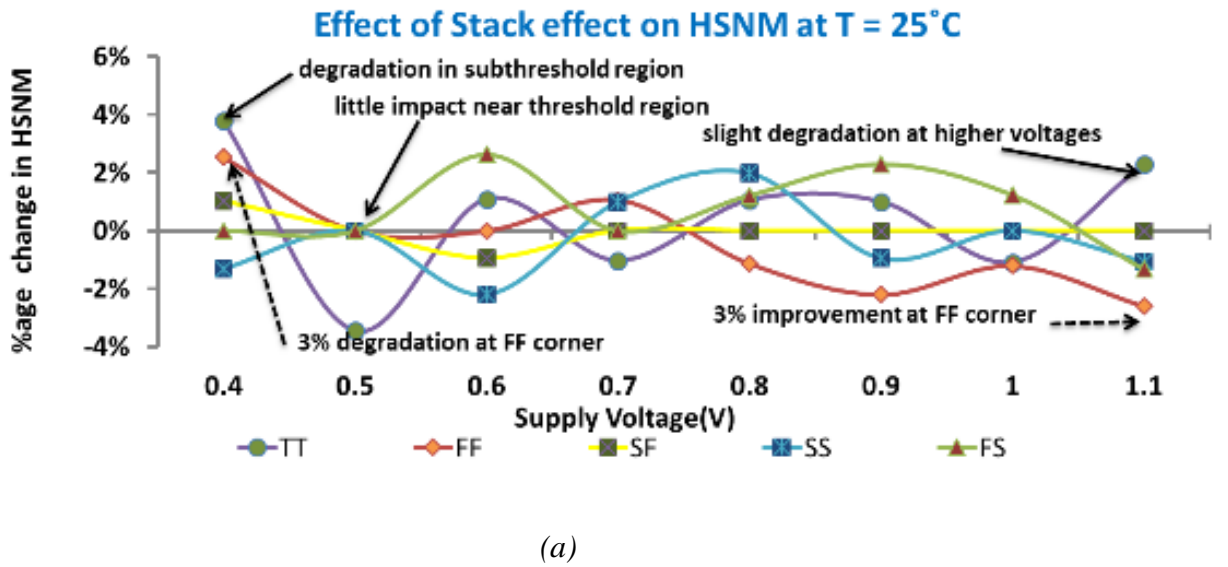
Fig. 2.21 Effect on HSNM at 25 °C

Performance comparison : The performance of read port leakage reduction techniques are tabulated on the basis of leakage, read performance and stability in Table 2.5 for quick comparison. The results indicate that the Stack effect and DCPR techniques are more effective at high supply voltages and low-to-moderate temperatures in contrast to VCG technique which is more suitable at low supply voltages and high temperatures. It is also noted that all the techniques show improved tolerance to PVT-variations.

Table 2.5: Performance comparison of read port leakage reduction techniques [24][34][53][56][59][84]

Techniques	STACK EFFECT	DCPR	VCG
Leakage	Overall good but more effective at high voltages	Overall good but more effective at high voltages	Effective at low voltages
Read current to leakage current ratio	More improvement at high voltages	More improvement at high voltages	More improvement at low voltages
Hold stability	No effect	No effect	No effect
PVT-variation tolerant	Yes	Yes	Yes
Suitable temperature	Low to moderate temperatures	-40 °C to 125 °C	High temperatures
Suitable supply voltage	High voltages	High voltages	Low voltages
Remarks	Degraded read current values at high temperatures. Use of extra transistors.	Requirement of multiple supply rails.	Requirement of multiple ground rails.

The comparison of all read port reduction techniques at different technology nodes (Table 2.6), reveal the impeccable leakage reduction capability across the technology nodes. However, VCG technique retains significantly high leakage reduction percentage compared to the other two. In addition, no impact of any technique on cell stability, write ability and minimum retention voltage is observed as all the techniques are applied on the SRAM cell with isolated read port.

Table 2.6: Comparison of read port leakage reduction techniques at different technology

nodes [24][34][53][56][59][84]

Techniques	STACK EFFECT			DCPR			VCG		
	90 nm	65 nm	32 nm	90 nm	65 nm	32 nm	90 nm	65 nm	32 nm
Leakage	-81 %	-84.6 %	-89.2 %	-84.0 %	-87.2 %	-85.8 %	-98.7 %	-95.9 %	-90.8 %
Read current to leakage current ratio	+115.5 %	+145.5 %	+206.2 %	+525 %	+680 %	+605.9 %	+7800 %	+2333 %	+984.9 %
Hold stability	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect
Read stability	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect
Write ability	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect
Minimum retention voltage	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect	No Effect

2.4 Design of SRAM cell with low leakage

This section presents a low leakage SRAM cell that offers improved read stability and write ability in addition to reduced leakages. The cell employs NWL technique to bias the OFF transistors in super cut-off region and reduce bitline leakages. In addition, it uses MTCMOS technique to address the latch leakages due to its best leakage reduction capabilities. To reduce the degrading impact of MTCMOS technique on other cell performance parameters, the technique is applied only on non-critical transistors of latch.

2.4.1 Proposed cell I

The schematic of Proposed cell I that performs single ended read and differential write operations is shown in Fig. 2.22(a). It consists of three transistors (MUR, MUL and MDL) based latch structure for bit storage. It uses RBL, a read assist circuit (M1, M2) and a read wordline (RWL) control signal for performing single ended read operation. The write wordline (WWL) control signal along with complementary pair of write bitlines (WBL/WBLB) are used for performing a faster differential write operation. To reduce leakages in the cell, the MTCMOS technique is employed for latch implementation wherein the transistors MUL and MUR are HVT implemented whereas the write critical transistor MDL is having typical threshold voltage. In addition, to provide robust hold '1' state MAR is LVT implemented.

(a)
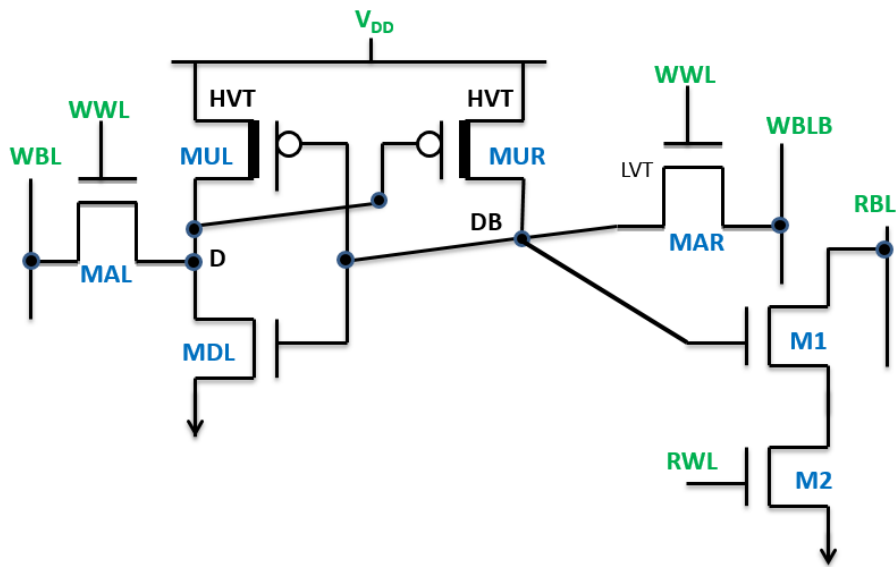
CONTROL SIGNAL	MODE	READ	WRITE	HOLD
WWL		0	1	0
RWL		1	0	0

(b)

Fig. 2.22 Proposed cell I (a) Schematic (b) Operating conditions

2.4.1.1 Operation

The Proposed cell I can be operated in read, write and hold modes as per the operating conditions specified in Fig. 2.22(b). In addition, the WBLB is kept low except when writing '1' at node DB.

Read mode

The RWL driven M2 acts as a switch to connect RBL to GND in the read mode. When DB is '1' (D = '0') then the transistor M1 turns ON and conducts heavy read current through M1 and M2 due to improved W/L ratio of the read circuit (Table 2.7). Therefore, RBL

discharges quickly through M2. A sense amplifier then senses the change in RBL voltage and completes the read operation. Similarly, if DB is '0' (D = '1') then the transistor M1 stays OFF and there is no change in RBL voltage. Due to the presence of separate discharge path for the read current (through M1 and M2), the RSNM is almost equal to HSNM.

Write mode

This cell employs faster differential write operation using complementary WBLs and WWL. The bitlines are driven in opposite direction to ease the writing process. For a write '1' operation, with WWL = '1', MAL turns ON and due to very high V_{DS} quickly charges the node D towards logic high. Simultaneously, node DB discharges quickly through ON access transistor MAR towards GND. The proposed cell provides improved write ability at low power consumption with no much area overhead.

Hold mode

In this mode, WWL and RWL are maintained at low level which isolate the internal nodes from noises through external bitlines. Since only the leakages can change the voltages at the internal nodes in this mode therefore the immunity of cell against noise is maximum in this state [76][114]. In proposed cell, the transistors, which generate the leakage current are either sized minimum or are HVT implemented in latch structure. To reduce the leakages further in cell, NWL leakage reduction technique [81] is implemented on the proposed cell. In this technique, the voltage at the gate of the OFF MOS transistors, MAL and MAR, are increased negatively so that the transistors are biased in super cut-off region and have reduced leakages.

2.4.1.2 Simulation results

The conventional 6T cell, 7T_taw [12] cell and Proposed cell I are implemented and simulated using 32 nm bulk CMOS PTM model parameters. The comparison among the

cells are done on the basis of I_{LEAK} and other important performance parameters such as RSNM, I_{ON}, WSNM, HSNM and DRV. All the SPICE simulations are carried out at a supply voltage of 0.4 V and temperature 27 ˚C. The dimensions, i.e., width to length ratio (W/L) of all the transistors are specified in the Table 2.7 in lambda (λ) as per lambda rule of layout specification.

Table 2.7: Aspect ratio of transistors

SRAM Cells	Transistors (λ = 18 nm)							
	MUL	MUR	MAL	MAR	MDL	MDR	M1	M2
Conventional 6T	3λ/2λ	3λ/2λ	4λ/2λ	4λ/2λ	8λ/2λ	8λ/2λ	-	-
7T_taw [12]	3λ/2λ	3λ/2λ	4λ/2λ	-	8λ/2λ	8λ/2λ	3λ/2λ	3λ/2λ
Proposed cell I	3λ/2λ	3λ/2λ	6λ/2λ	8λ/2λ	8λ/2λ	-	4λ/2λ	4λ/2λ

Read mode

The SRAM cells are implemented to operate in the read mode and parameters RSNM and I_{ON} are calculated for comparison.

RSNM

From the RSNM values plotted in Fig. 2.23, it can be observed that the proposed cell provides 63.4 % and 12.5 % higher RSNM compared to Conventional 6T and 7T_taw cells respectively. This shows that during read operation the stored data remains more resistant to noise in the proposed cell compared to conventional 6T and 7T_taw cells.
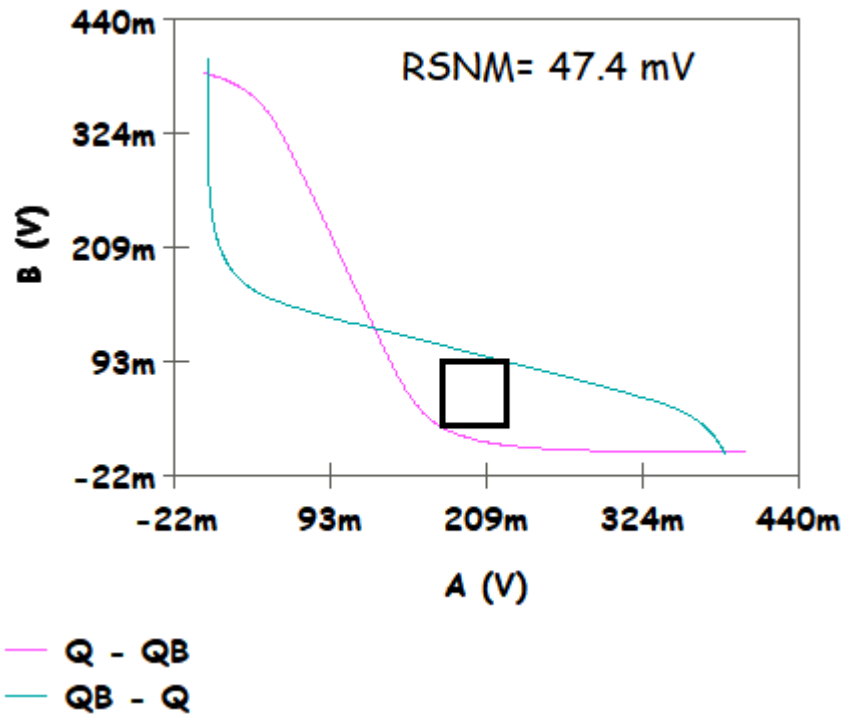
(a)
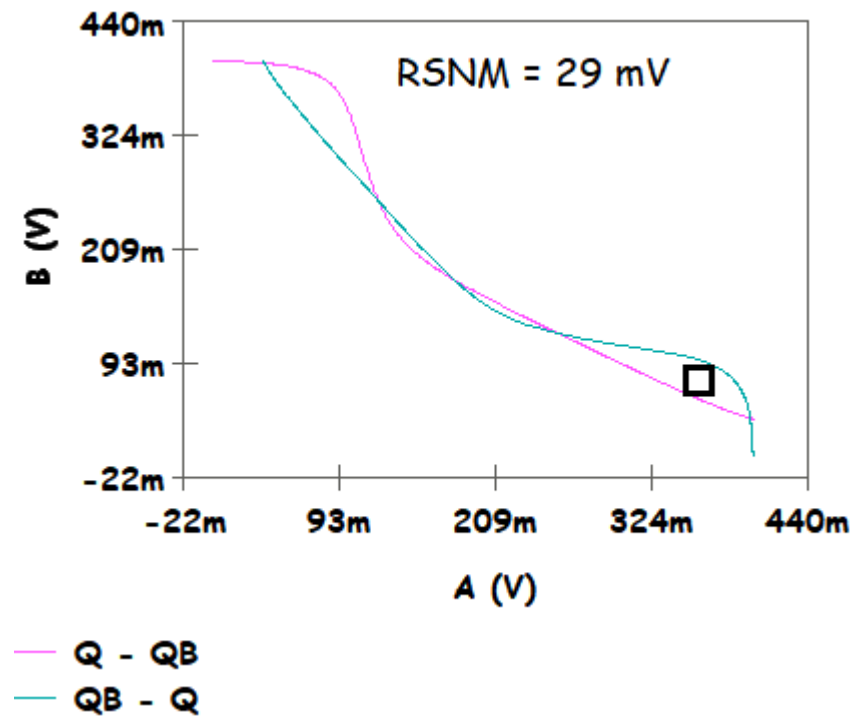
(b)
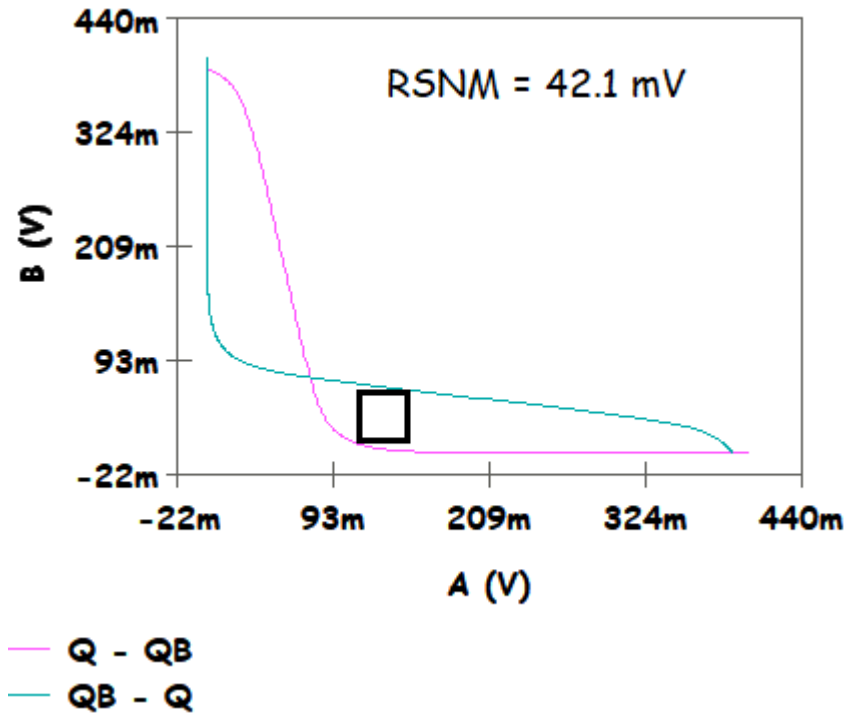
(c)

Fig. 2.23 RSNM at V_{DD} = 0.4 V for (a) Proposed cell I (b) Conventional 6T (c) 7T_taw

SRAM cells

I_{ON}

The variation of I_{ON} values with supply voltage and temperature is shown in Fig. 2.24. It can be noted that the proposed cell provides 8.9 % and 151.3 % higher I_{ON} than conventional 6T and 7T_taw cells in sub-threshold region. This validates that the RBL discharges faster in proposed cell as compared to the other two cells under similar operating conditions. The result also shows the robust performance of the proposed cell across different values of supply voltage and temperature.
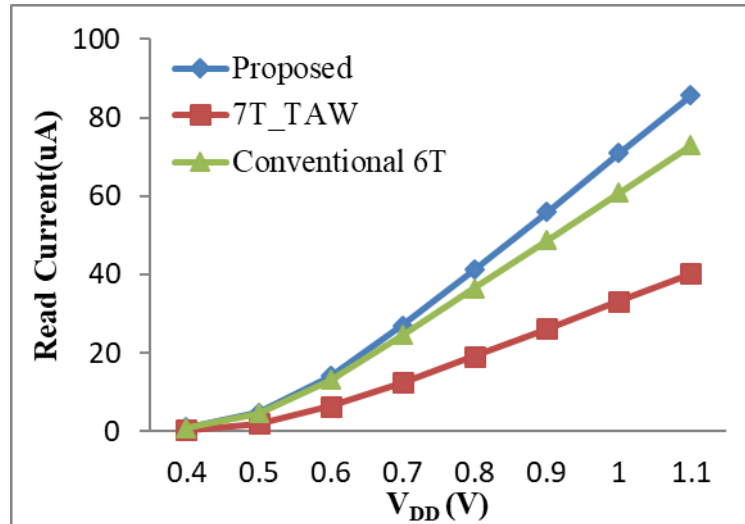
(a)
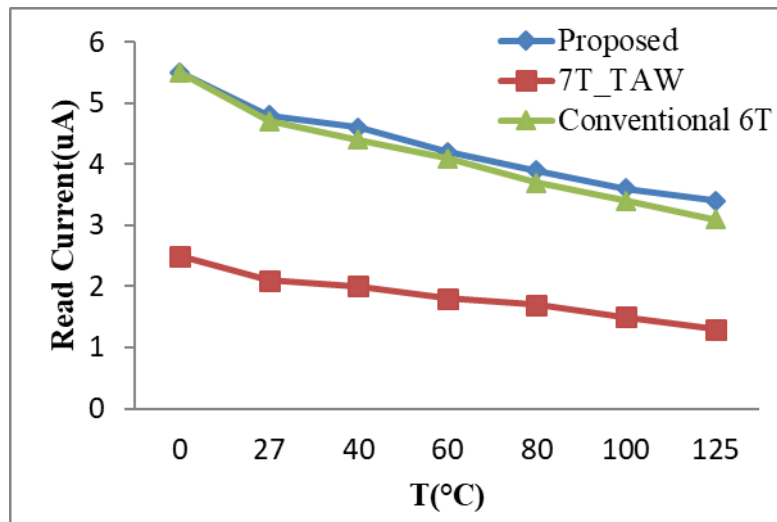
(b)

Fig. 2.24 I_{ON} of Proposed cell I, Conventional 6T and 7T_taw cells under (a) Supply voltage variations at 27 °C and (b) Temperature variations at V_{DD} = 0.4 V

Write mode

All the SRAM cells are implemented to operate in the write mode. The use of HVT pull-up transistors results in the tremendous improvement in the noise immunity of the proposed cell in terms of WSNM.

WSNM

The WSNM is evaluated for all the cells and the corresponding values are shown in Fig. 2.25. It is apparent from the graph that the proposed cell shows improvement of 21 % and 16.4 % in WSNM in comparison to conventional 6T and 7T_taw in sub-threshold region.
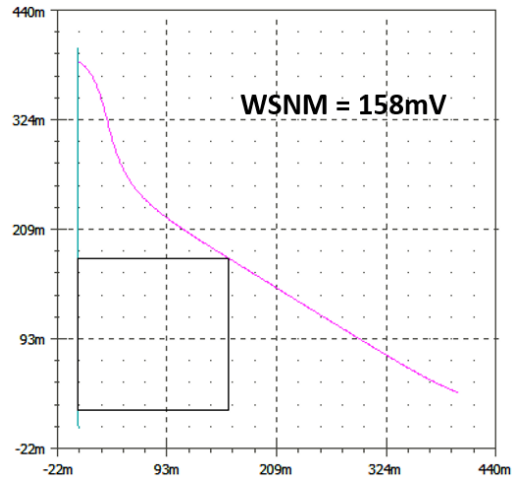
(a)
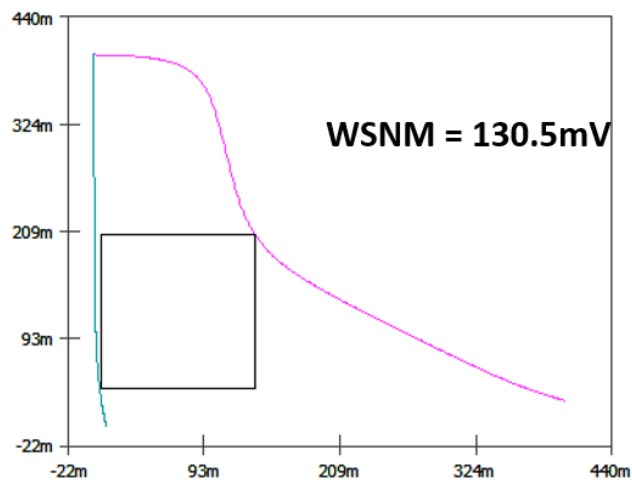
(b)
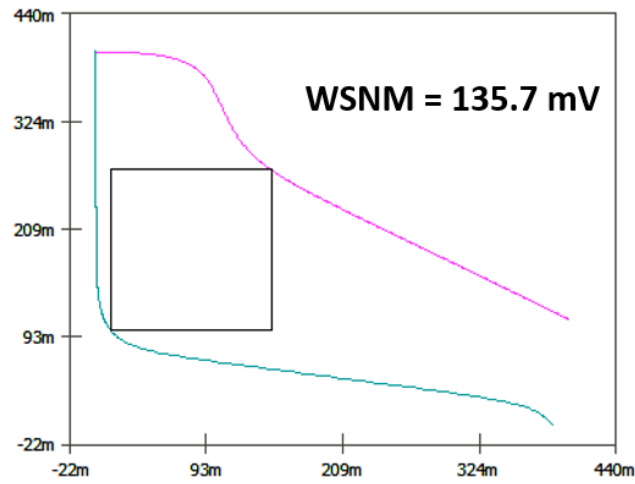
(c)

Fig. 2.25 WSNM at V$_{DD}$ = 0.4 V for (a) Proposed cell I (b) Conventional 6T (c) 7T_taw

SRAM cells

Hold mode

All the SRAM cells are implemented to operate in the hold mode and the important parameters namely HSNM, DRV and I$_{LEAK}$ are estimated for comparison.

HSNM

The results in Fig. 2.26 shows an improvement of 12.5 % in HSNM values for proposed cell compared to 7T_taw cell in sub-threshold region indicating more stability for stored data against noise compared to 7T_taw cell.
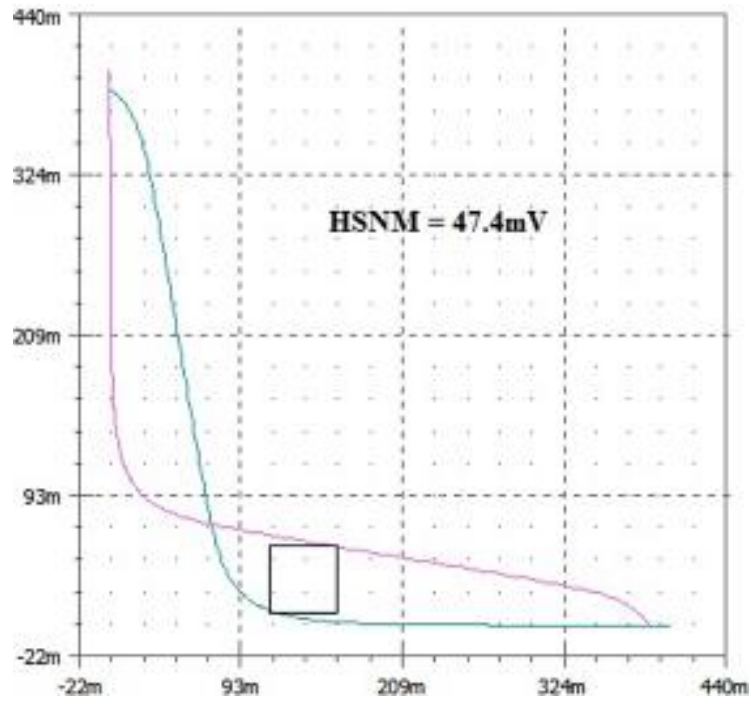
(a)
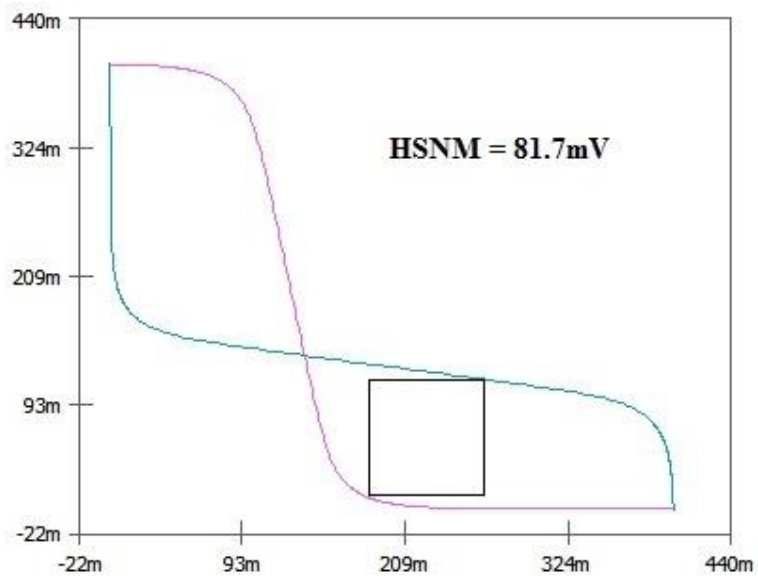
(b)
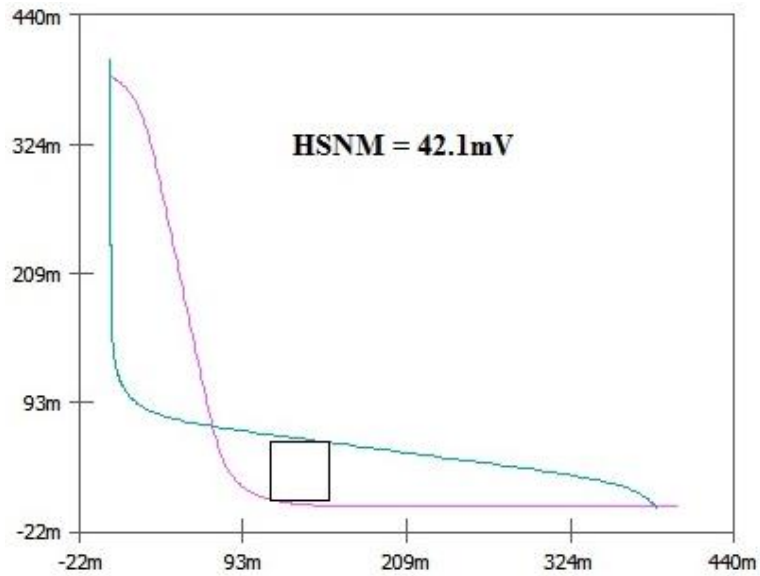
(c)

Fig. 2.26 HSNM at V_{DD} = 0.4 V for (a) Proposed cell I (b) Conventional 6T (c) 7T_taw

SRAM cells

DRV

The DRV values are calculated and plotted in Fig. 2.27. The result shows that the proposed

cell achieves 18 % improved DRV value compared to 7T_taw cell.
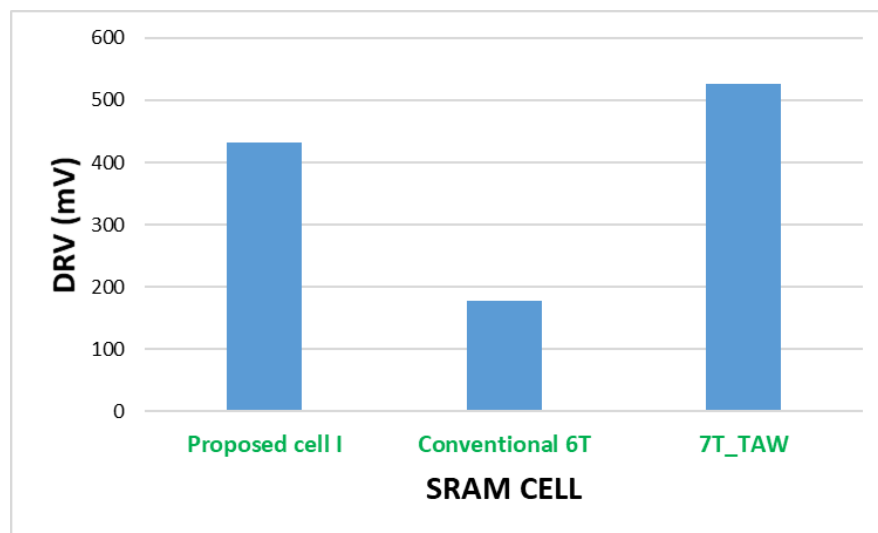
Fig. 2.27 DRV for Proposed cell I, Conventional 6T and 7T_taw SRAM cells

I_{LEAK}

The variation of I_{LEAK} with supply voltage is shown in Fig. 2.28. The cell shows 32 % and 37.5 % reduction in leakages with MTCMOS technique when compared to conventional 6T and 7T_taw cells respectively in sub-threshold region ($V_{DD} = 0.4$ V). In the presence of both NWL and MTCMOS techniques the leakage are reduced further. For NWL technique, the access transistors are overdriven in hold mode by applying -80 mV at WWL. A significant reduction of 54 % and 57.8 % is observed in I_{LEAK} as compared to conventional 6T cell and 7T_taw cells respectively at 0.4 V.
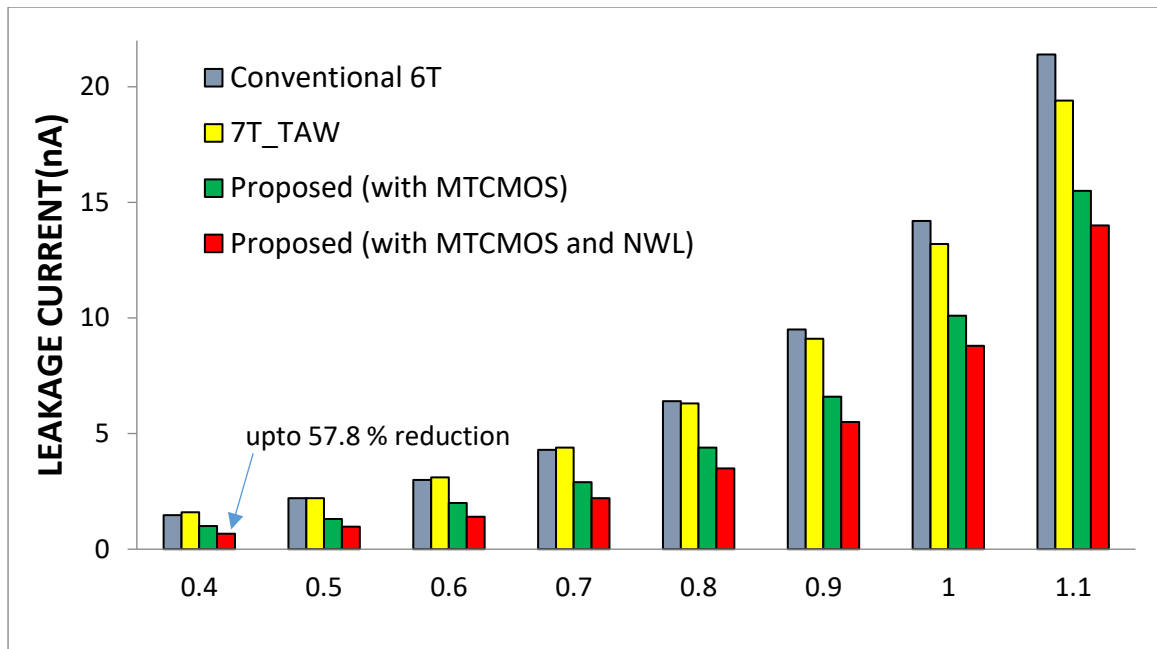
Fig. 2.28 I_{LEAK} for Proposed cell I (with MTCMOS only and with both MTCMOS and NWL), Conventional 6T and 7T_taw SRAM cells

Comparative analysis

The comparison results of SRAM cells at $V_{DD} = 0.4$ V and T = 27 ˚C is shown in Table 2.8. The results reveal that the proposed cell provides significant improvement in all

performance parameters except hold stability and thus can be used at 32 nm in sub-threshold region.

Table 2.8: Performance comparison at V_{DD} = 0.4 V and T = 27 ˚C

MODE	PARAMETER	CONVENTIONAL 6T	7T_TAW	PROPOSED CELL I
READ	RSNM (mV)	29	42.1	47.4
	I_{ON} (µA)	0.9	0.39	0.98
WRITE	WSNM (mV)	130.5	135.7	158
HOLD	HSNM (mV)	81.7	42.1	47.4
	DRV (mV)	177.9	526.5	431.3
	P_{LEAK} (nW)	0.588	0.64	0.40 (with MTCMOS)
				0.2704 (with MTCMOS and NWL)

2.5 Conclusions

The comparative analysis of existing leakage reduction techniques for SRAM cell reveals some significant aspects of each technique. It is observed that for reducing latch leakages, MTCMOS is more suitable at high supply voltages and temperatures whereas DM technique is more suitable at high supply voltages and over the temperature range from -40 ˚C to 125 ˚C. The SB technique is suitable over the entire temperature (-40 ˚C to 125 ˚C) and voltages range (0.4 V to 1.1 V). It is also found that all the techniques show strong impact of process variations on the leakage reduction capabilities. To suppress the bitline leakages, results for both NWL and LBB techniques show significant leakage reduction across temperature and supply voltage range. The suitable operating conditions for NWL

technique are moderate temperatures and low voltages. The LBB technique reduces the leakage through memory sub-bank significantly at low temperatures and high supply voltages independent of the values stored in the cell. Both, the techniques show lesser impact of process variations on the leakage reduction capabilities. For reducing read port leakages, the results show that the Stack effect technique gives extremely high percentage reduction in leakages across all voltages and temperatures but at higher temperature, there exists a trade-off between read performance and leakage reduction capabilities making this technique suitable for low to moderate temperatures. The DCPR technique, on the other hand, achieves extremely good results at high supply voltages and over a temperature range from -40 ˚C to 125 ˚C while VCG technique is suitable for use at high temperatures and low voltages. It is also observed that all the three techniques Stack effect, DCPR and VCG techniques possess tolerance for leakages against process variations.

On performing the technology comparison on all the leakage reduction techniques, it is observed that the efficacy of all the techniques in suppressing the leakage current changes with technology node. In addition, all the techniques bear either positive or no impact on read-write performance of the SRAM cell except MTCMOS technique. The MTCMOS technique provides a significant improvement in write ability and minimum retention voltage of the SRAM cell but at the cost of read stability.

A low leakage Proposed cell I based on the use of NWL and MTCMOS leakage reduction techniques, is also presented. The proposed cell provides up to 37.5 % reduction in I_{LEAK} at 0.4 V compared to other SRAM cells with MTCMOS technique alone. The leakage reduction % age increases to 57.8 % in the presence of both MTCMOS and NWL techniques showing the impeccable performance of leakage reduction techniques in sub-threshold region. To reduce the impact of MTCMOS technique on cell performance, the technique is employed only on non-critical transistors of latch. The use of three MOS

transistors in latch realization of SRAM is suggested to reduce area overhead and provide robust hold '0' state. In addition, the proposed cell shows significant improvement of 1.6X, 1.2X and 1.1X in RSNM, WSNM and I_{ON} respectively compared to conventional structure. An improvement of 1.1X, 1.2X, 2.5X and 1.1X is observed in RSNM, WSNM, I_{ON} and HSNM respectively at 0.4 V compared to 7T_taw SRAM cell.

CHAPTER 3

SRAM CELL DESIGN WITH IMPROVED READ AND WRITE

PERFORMANCE

The content and results of the following papers have been reported in this chapter:

1. Gupta M, Gupta K, Pandey N, " **A Data-Independent 9T SRAM Cell with Enhanced I_{ON}/I_{OFF} Ratio and RBL Voltage Swing in Near Threshold and Sub-Threshold Region**", International Journal of Circuit Theory and Applications, Wiley, 49, 953-969, 2021. **(SCI Journal with Impact Factor: 2.038)**

2. Gupta M, Gupta K, Pandey N, "**A 32-nm Sub-Threshold 9T SRAM Cell with Improved Read and Write performance**", *International Conference on Advances in Computing, Communication Control and Networking (ICACCCN)*, IEEE, 781-787, 2018

3.1 Introduction

The increasing leakages in nanometer regime were addressed in chapter 2 of this thesis. Now, this chapter focusses on yet another important aspect of SRAM in sub-threshold region that is read and write performance of the cell. The conventional 6T SRAM cell shows degraded performance due to read-write conflict issue especially at low voltages. Various assist techniques are available in literature to improve the performance in one of the operating mode but with either degradation or no change in performance of the cell in other mode. An alternate method to resolve this issue is to decouple read-write ports.

Several SRAM cells with isolated read ports having two to four transistors (2T-4T) are presented in [12][47-49][51][57][86]. However, the available read ports suffer due to trade-off between the read current and RBL leakages. So, in view of this two new SRAM cells are proposed in this chapter. Both the cells incorporate novel isolated read port designs for performance improvement in read mode. The Proposed cell II improves the read performance by removing the stacking of transistors in read port thus providing significant improvement in read current values whereas the Proposed cell III accomplish the same objective by overcoming the trade-off between read current values and RBL leakages. Further, the write performance is improved by employing write assist circuit with single ended write and faster differential write in Proposed cell II and III respectively.

The existing SRAM cell designs are reviewed in section 3.2 of this chapter. The section 3.3 presents, Proposed cell II and III along with their functional verification in all the three operating modes. The performance comparison of the proposed cells with comprehensive comparative investigation across different operating conditions is also included in same section. Finally, the conclusions are drawn in section 3.4.

3.2 Existing SRAM cell designs with improved read and write performance

To overcome the problems associated with conventional 6T SRAM cell, the conventional 8T SRAM cell (8T_conv) [4] is introduced to provide improved read performance with no effect on write performance (Fig. 3.1(a)). The cell performs single-ended read and faster differential write operation. The new data is written into the cell through the two access transistors MAL and MAR driven by WWL control signal. The isolated read port has two transistors M1 and M2 driven by RWL control signal and internal data storage node DB value respectively. The RBL is pre-charged to V_{DD} at the beginning of read cycle using pre-charge signal, PC_r (Fig. 3.1(b)). During a read '0' operation, read current I_{ON} flows through the read port as both M1 and M2 are ON. The RBL thus gets discharged from V_{DD} to V2 as marked in Fig. 3.1(c). Alternatively, for a read '1' operation RBL should be maintained at V_{DD}. Thus, in ideal situation ΔV_{RBL} is (V_{DD}-V2). However due to device scaling, the presence of non-conducting transistors in the accessed as well as the un-accessed cells lead to leakage current in the column. An illustration during read '1' operation is shown in Fig. 3.1(b). In the accessed cell the leakage current (I_{L_AC}) flows as the internal data node DB stores '0' value. Analogously, in the un-accessed cells, the leakage currents I_{L_UC1} and I_{L_UC2} flow with DB data value of '0' and '1' respectively. The worst value out of the two is usually I_{L_UC2} and is considered as I_{OFF}. Due to these leakages, the RBL voltage is reduced from V_{DD} to the level marked as V1 or V1'. Thus, ΔV_{RBL} reduces to (V1 – V2) or (V1' – V2) from ideal situation. The high and data-dependent leakage currents affect the various other parameters associated with the read port namely, I_{ON}/I_{OFF} ratio, ΔV_{RBL} and T_{READ_ACCESS}.

(a)

(b)
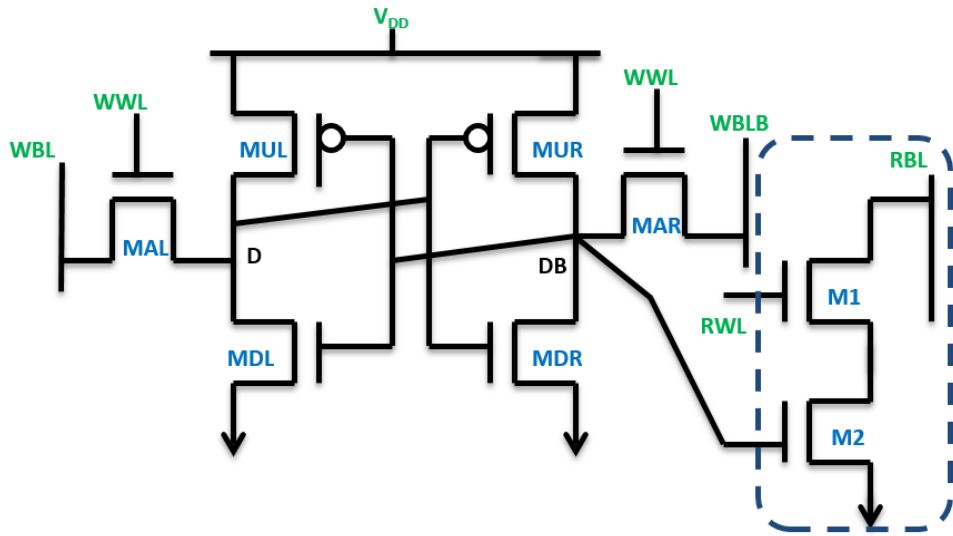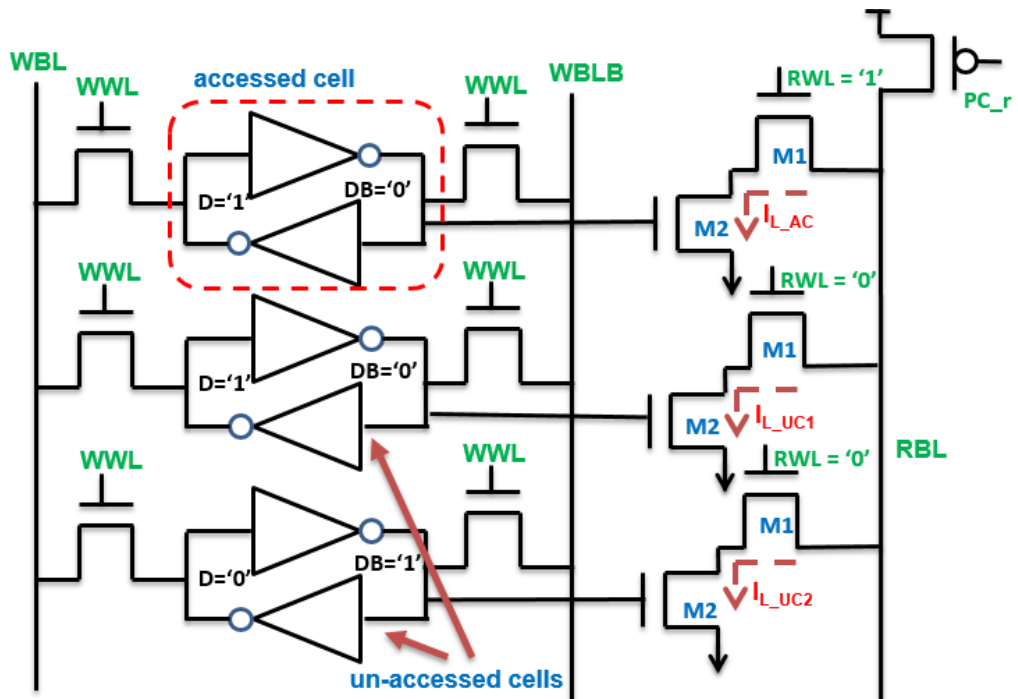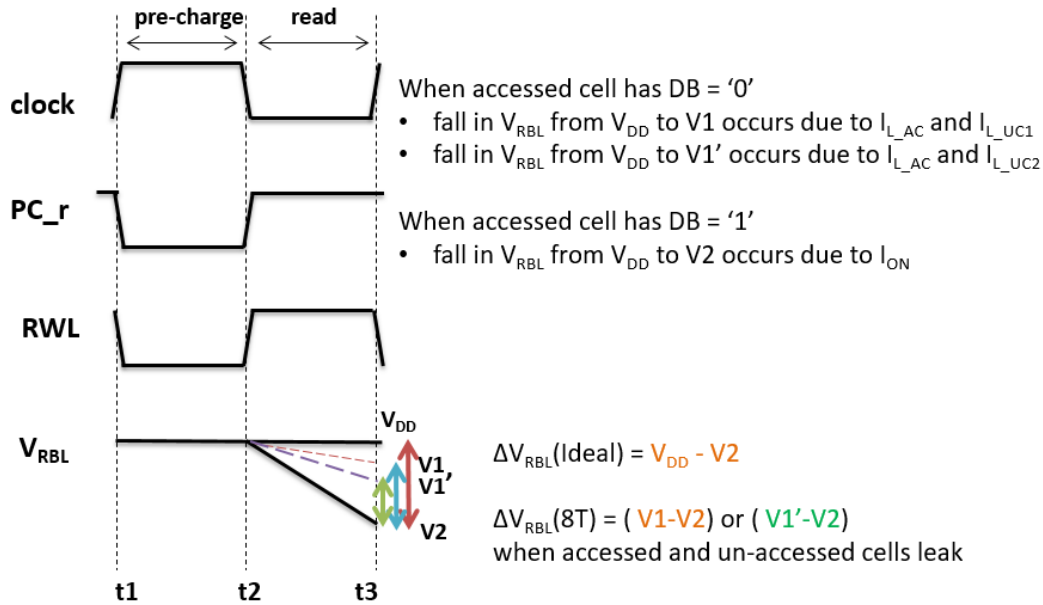
Fig. 3.1 Conventional 8T SRAM cell [4] (a) Read operation (b) Leakage current components in accessed and un-accessed cells (c) Impact of leakage currents on ΔV_{RBL}

Several SRAM cells with modified read ports, with two-to-four transistors, addressing these issues are suggested in literature [12][47-49][51][57][86]. In 2T read port of 7T_taw [12] cell the read port transistors are interchanged with respect to conventional 8T SRAM cell. The arrangement reduces the drain-to-source voltage (V_{DS}) across the ON transistor and suppresses I_{L_UC2} slightly. The ΔV_{RBL} and I_{ON}/I_{OFF} ratio are then improved compared to conventional structure. However, due to high and data-dependent leakage in un-accessed cells, the problem of high read failure persists. The 9T_ver [47] cell with 3T read port suggests an alternate way to suppress the leakage current. It introduces the stacking effect by splitting the RWL driven transistor of earlier read ports. The leakage currents are reduced at the cost of slight increase in area. However, there is significant reduction in read current values leading to increase in T_{READ_ACCESS} while maintaining data-dependent leakages. Another SRAM structure, 9T_wang [48] having 3T read port suggests the use of compensation transistor (CT) to design a data-independent read port. This makes I_{L_UC1} and

I_{L_UC2} almost equal in un-accessed cells resulting in data independency but at the cost of high leakages. Thus, the read port though data-independent shows deteriorated performance in terms of degraded I_{ON}/I_{OFF} ratio and ΔV_{RBL}. The 10T_cal [51] cell with 4T read port although provides substantial reduction in I_{L_AC} and I_{L_UC1} nevertheless, it translates into little improvement in the read performance parameters. Additionally, the increased I_{L_UC2} results in degraded I_{ON}/I_{OFF} ratio in near threshold and sub-threshold regions. Another 4T read port in 10T_sh [57] cell suppresses I_{L_AC} in accessed cell and offers data-independent leakages in un-accessed cell. However, this data independency is achieved at the cost of increasing I_{L_UC1} and making it equal to I_{L_UC2}. The high leakage currents in un-accessed cell yields marginal improvement in ΔV_{RBL} and I_{ON}/I_{OFF} ratio at lower voltages. In 9T_pasa [49] cell, the 4T read port offers reduced leakage I_{L_UC2} in un-accessed cell, and provides significantly improved ΔV_{RBL}. The leakage currents I_{L_UC1} and I_{L_UC2} remains comparable at higher V_{DD} but deviates significantly from each other at lower V_{DD} thus resulting in data-dependency issues especially in near threshold and sub-threshold regions. In the next 4T read port in 10T_chris [86] cell, the compensation transistor reduces I_{L_UC2} and makes it equal to I_{L_UC1} thus providing data-independent leakage current in un-accessed cells even at lower voltages. The reduced leakages result in improved ΔV_{RBL}. The cell, however, bears the repercussions of stacking effect on read current I_{ON}, and thus suffers from degraded I_{ON}/I_{OFF} ratio and T_{READ_ACCESS}.

3.3 Design of SRAM cell with improved read and write performance

The available SRAM cells attempt to improve read performance without degrading the write performance. However, the designs with an isolated read port focus on leakage reduction in either un-accessed cell or accessed cell but at the cost of limitation on read current values. This necessitates a new design that can optimize all the read performance parameters and maintains high read current values. In addition, the write performance in

sub-threshold region also needs consideration. Therefore, in view of this two new SRAM cells are proposed in this chapter. Both the cells, Proposed cell II and III, incorporate an isolated read port to provide extremely high read stability that is almost equal to the hold stability of SRAM cell. The Proposed cell II provides single ended writing to reduce power consumption. The use of write assist transistor helps in faster charging of storage nodes during write operation. In addition, the novel read port design aims for high read current values for faster reading by removing the stacking of transistors in read port. The use of NWL technique helps in reducing the leakages in SRAM cell. The Proposed cell III uses differential write for faster writing. Further, for read performance improvement, it incorporates compensation transistor in novel read port design to addresses all the leakage components of the un-accessed and accessed cells while maintaining the reasonable values of read current.

3.3.1 Proposed cell II

The schematic of Proposed cell II that performs single ended read and write operations is shown in Fig. 3.2(a). It consists of the basic two cross-coupled inverters formed by transistors (MUR-MDR, MUL-MDL1) for bit storage. It uses RBL, read assist circuit (M1, M2, M3) and control signal RWLB for performing single ended read operation. The WBL, transistors MDL2 and MAL along with the control signals WWL and its complement WWLB are used to perform single ended write operation. The nMOS transistor MDL2 weakens the pull-down path during write operation. Its inclusion does not account for area overhead as the width of the two series connected nMOS transistors (MDL1, MDL2) is halved in comparison to the existing ones.

(a)
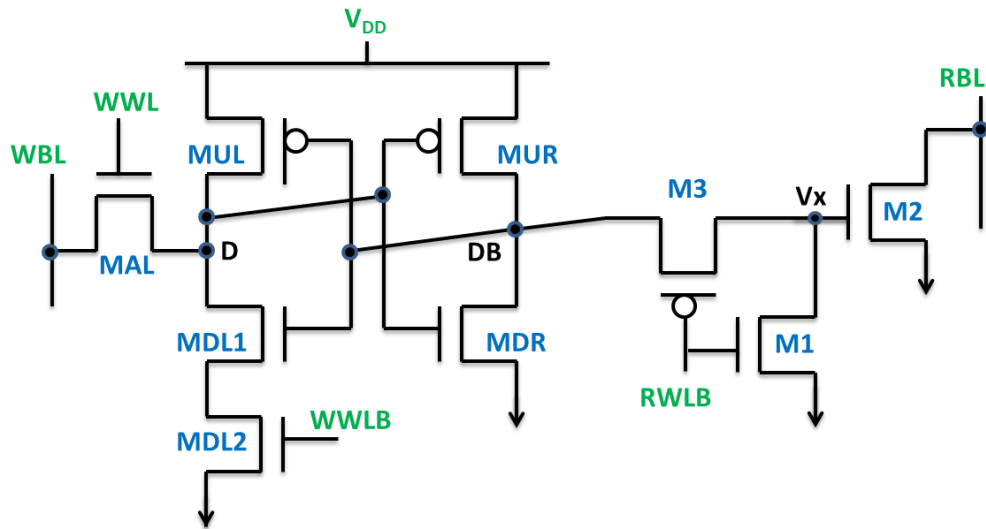
CONTROL SIGNAL / MODE	READ	WRITE	HOLD
WWL	0	1	0
WWLB	1	0	1
RWLB	0	1	1

(b)

Fig. 3.2 Proposed cell II (a) Schematic (b) Operating conditions

3.3.1.1 Operation

The Proposed cell II can be operated in write, read and hold mode as per the operating conditions specified in Fig. 3.2(b).

Read mode

During read mode, the transistor M3 driven by active-low control signal RWLB connects internal node DB to node Vx. If DB is '1' (D = '0') then the transistor M2 turns ON and discharges RBL quickly due to the absence of stacking effect of MOS transistors in read port. The sense amplifier then senses the drop in RBL voltage and completes the read

operation. Similarly, if DB is '0' (D = '1') then the transistor M2 stays OFF and there is no change in the voltage of RBL.

Write mode

In this mode, WWL and its complement WWLB are driven high and low respectively which weakens the pull-down of latch to ease the writing process. For a write '1' operation, with WWL = '1' and WWLB = '0', the path to GND is open (MDL2 is OFF) and thus the voltage at node D rises quickly. The proposed cell provides improved write ability at lower power consumption with no area overhead as it uses only single bitline and single access transistor during write operation.

Hold mode

In this mode, WWL goes low while WWLB and RWLB become high. The transistors MAL and M2 turn off, isolating the internal nodes from external interference. The transistor MDL2 conducts and connects the source of MDL1 to GND. No change at node voltages is possible except due to the flow of leakage current in this mode. In proposed cell, the transistors that produce the leakage current, are either minimum sized or have smaller drain to source voltage. The leakages are further reduced in sub-threshold region by implementing NWL technique on proposed cell [81]. In this scheme, the gate of the OFF access nMOS transistor, MAL is overdriven in hold mode by decreasing the voltage at its gate terminal. The gate terminal voltage can only be lowered until there is no problem due to gate-oxide reliability or the gate tunneling current (GIDL) is negligible. The advantages of this approach are that the performance of the cell in the active mode remains unchanged and no precise control of VG is required in hold mode.

3.3.1.2 Simulation results

In this section, the performance of Proposed cell II, conventional 6T and 7T_taw cells are compared on the basis of RSNM, I_{ON}, WSNM, HSNM, DRV and I_{LEAK}. All the SPICE simulations are carried out using 32 nm bulk CMOS PTM model parameters at 0.4 V. The aspect ratios (W/L) of the transistors are listed in the Table 3.1.

Table 3.1: Aspect ratio of transistors

SRAM Cells	Transistors ($\lambda = 18$ nm)								
	MUL	MUR	MAL	MAR	MDL	MDR	M1	M2	M3
Conventional 6T	$3\lambda/2\lambda$	$3\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$8\lambda/2\lambda$	$8\lambda/2\lambda$	-	-	-
7T_taw [12]	$3\lambda/2\lambda$	$3\lambda/2\lambda$	$4\lambda/2\lambda$	-	$8\lambda/2\lambda$	$8\lambda/2\lambda$	$3\lambda/2\lambda$	$3\lambda/2\lambda$	-
Proposed cell II	$3\lambda/2\lambda$	$3\lambda/2\lambda$	$4\lambda/2\lambda$	-	$4\lambda/2\lambda$	$8\lambda/2\lambda$	$3\lambda/2\lambda$	$3\lambda/2\lambda$	$3\lambda/2\lambda$

<u>*Read mode*</u>

All the cells are configured to operate in the read mode. The butterfly curve is obtained for the cells to measure RSNM. The read current is measured with respect to the node storing '0'.

RSNM

From the plots shown in Fig. 3.3, it can be observed that the proposed cell provides 169 % and 115 % higher RSNM compared to conventional 6T and 7T_taw cells respectively. This shows that the data remains immune to noise during reading operation in the proposed cell in comparison to conventional 6T and 7T_taw cells.
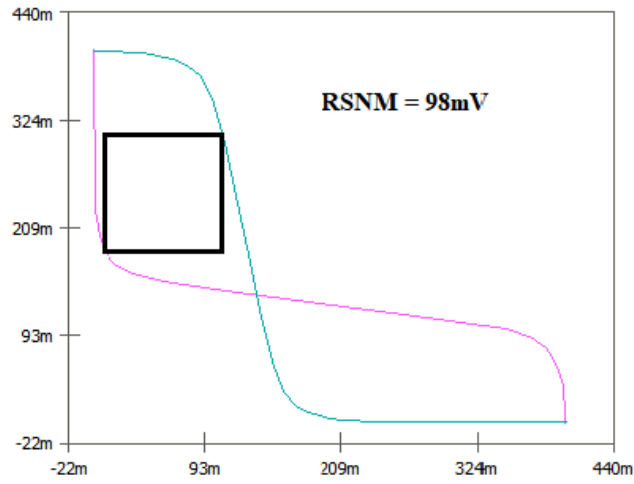
(a)
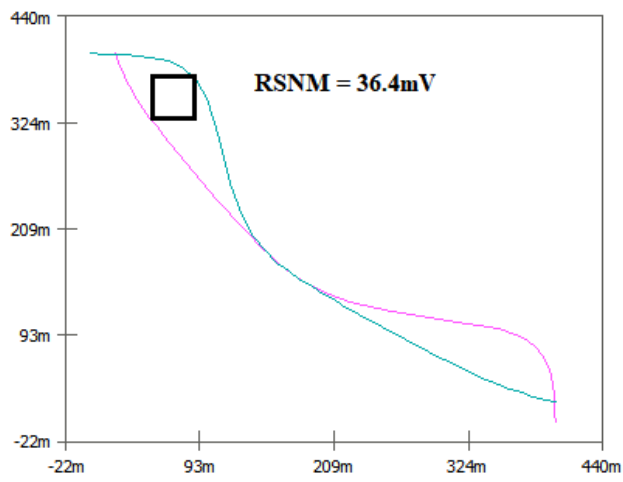
(b)
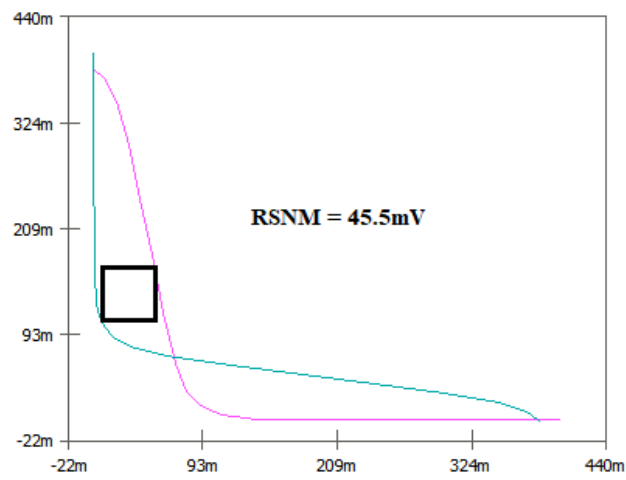
(c)

Fig. 3.3 RSNM at V_{DD} = 0.4 V and T = 27 °C for (a) Proposed cell II (b) Conventional 6T(c) 7T_taw SRAM cells

I_{ON}

The I_{ON} values for all the three SRAM cell configurations by varying the supply voltage and temperature are shown in Fig. 3.4. It can be observed that the proposed cell provides 24.3 % and 207.6 % higher I_{ON} compared to conventional 6T and 7T_taw cells in the sub-threshold region. This signifies that the voltage on RBL fall faster in proposed cell as compared to conventional 6T and 7T_taw cells under similar conditions. The results also show the robustness of the proposed cell against varying operating conditions.
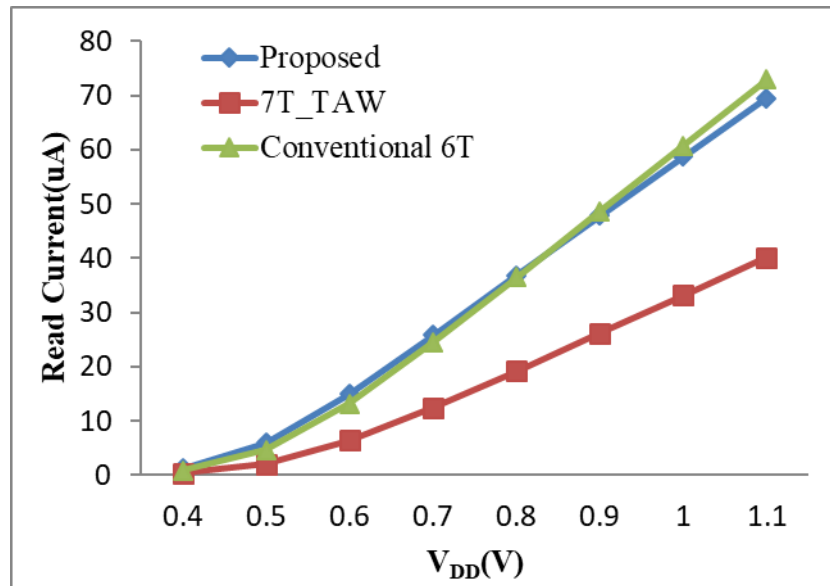
(a)
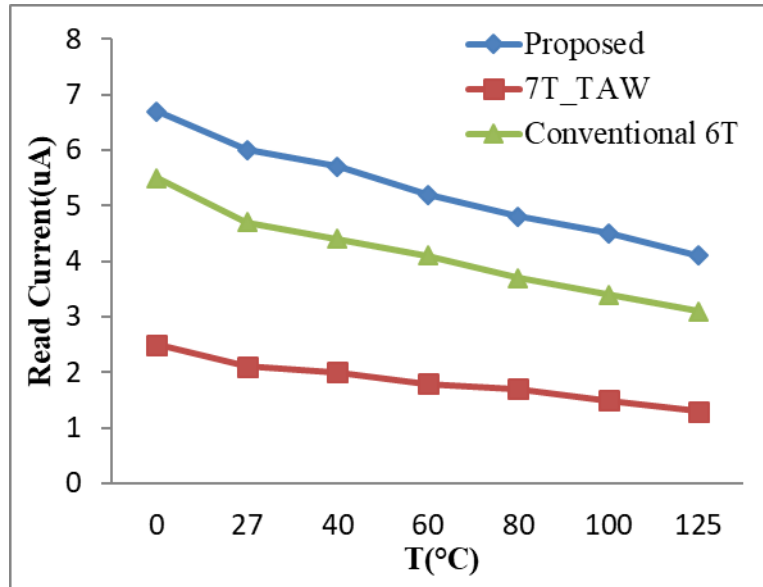
(b)

Fig. 3.4 I$_{ON}$ for Proposed cell II, Conventional 6T and 7T_taw cells under (a) Supply voltage variations and (b) Temperature variations

Write mode

All the cells are configured to operate in the write mode. In the Proposed cell II, a write assist transistor (MDL2) is used to weaken the pull-down path instead of using HVT transistors as used in 7T_taw. The result is a tremendous improvement in the noise immunity, which is measured using WSNM.

WSNM

The results in Fig. 3.5 indicate that the proposed cell shows 22.6 % and 15 % improved WSNM in comparison to conventional 6T and 7T_taw in sub-threshold region indicating the robust performance of proposed cell during write operation.

(a)

(b)

WSNM = 146.9mV
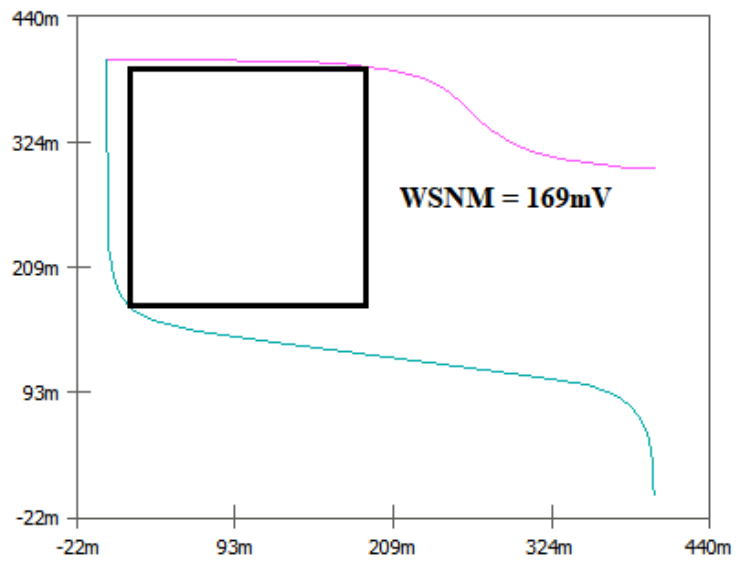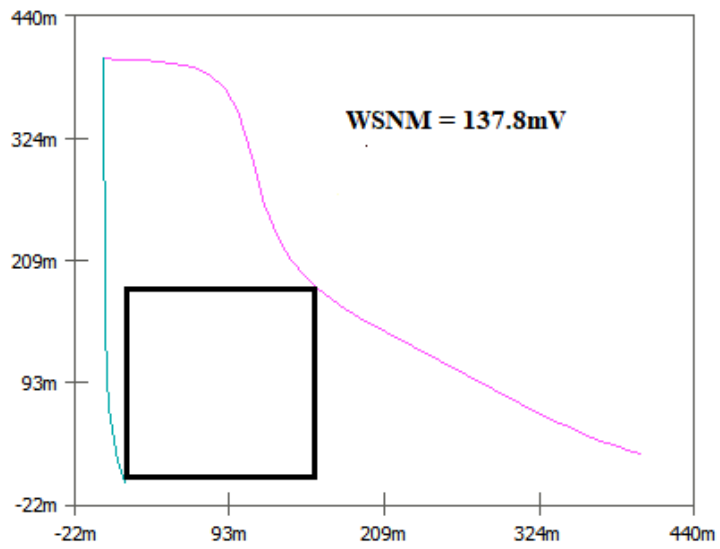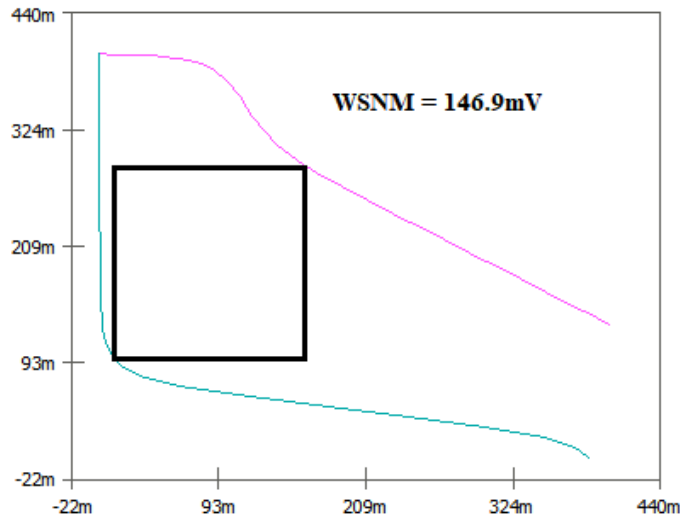
(c)

Fig. 3.5 WSNM at V_{DD} = 0.4 V and T=27 °C for (a) Proposed cell II (b) Conventional 6T (c) 7T_taw SRAM cells

Hold mode

All the cells are configured to operate in the hold mode and the key parameters namely HSNM, DRV and I_{LEAK} are evaluated for comparison.

HSNM

The results plotted in Fig. 3.6 shows that the proposed cell provides 115% higher HSNM compared to 7T_taw cell in sub-threshold region indicating that the stored data is more stable against noise in proposed cell. The values are, however, comparable to that of conventional 6T cell.
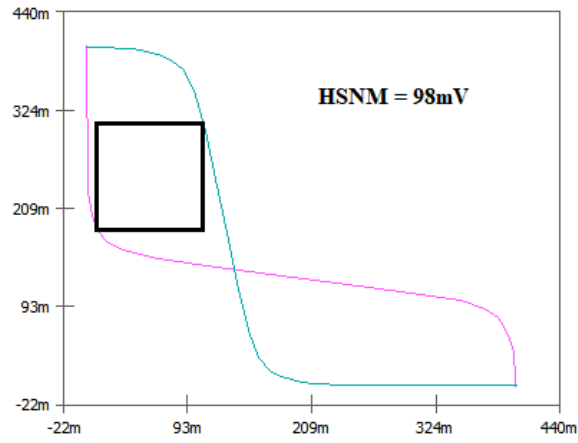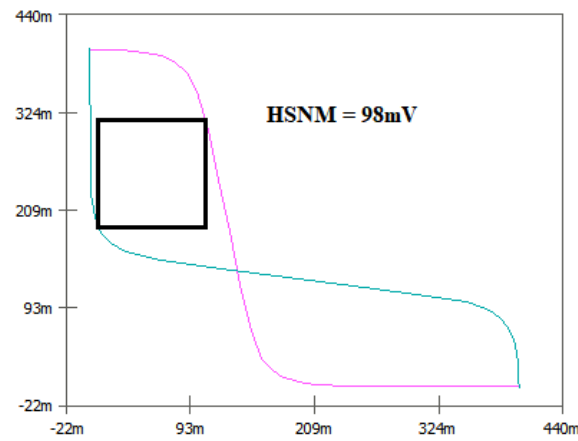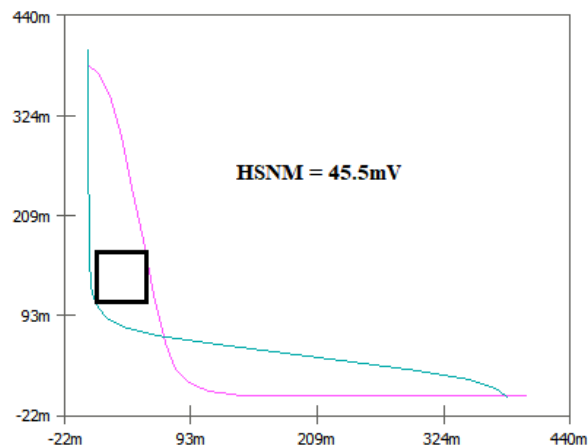
Fig. 3.6 HSNM at V_{DD} = 0.4 V and T = 27 °C for (a) Proposed cell II (b) Conventional

6T (c) 7T_taw SRAM cells

DRV

The cell shows 64 % improvement in DRV over 7T_taw cell whereas the value is slightly
higher compared to conventional 6T cell as shown in Fig. 3.7.
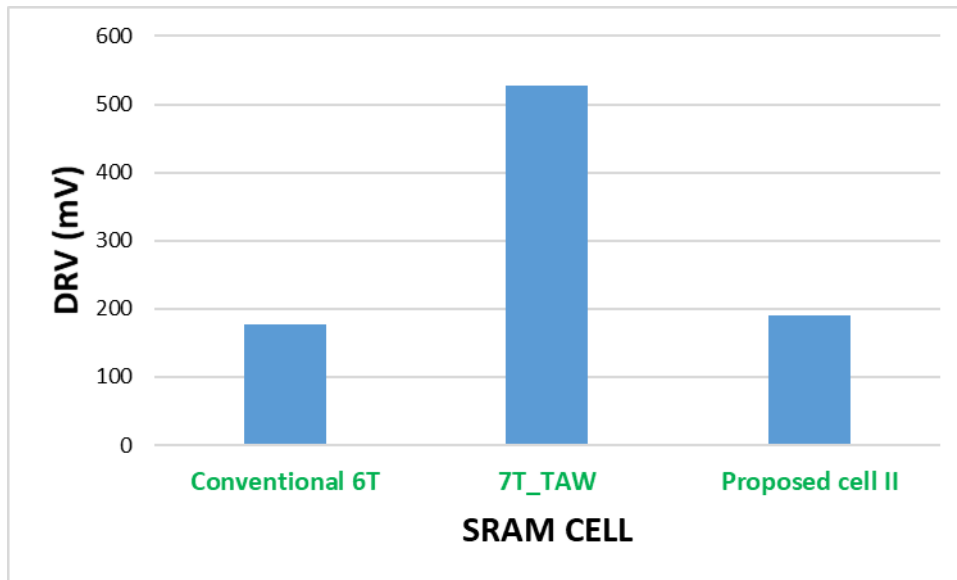
Fig. 3.7 DRV for Proposed cell II, Conventional 6T and 7T_taw SRAM cells

The worst-case DRV under 6σ global process and 1σ local mismatch variations is 313.7
mV at 27 °C (D = '0'; DB = '1') as shown in Fig. 3.8. This indicates that the proposed cell
is able to retain the stored data even at 313.7 mV, verifying its robust hold performance in
sub-threshold region.
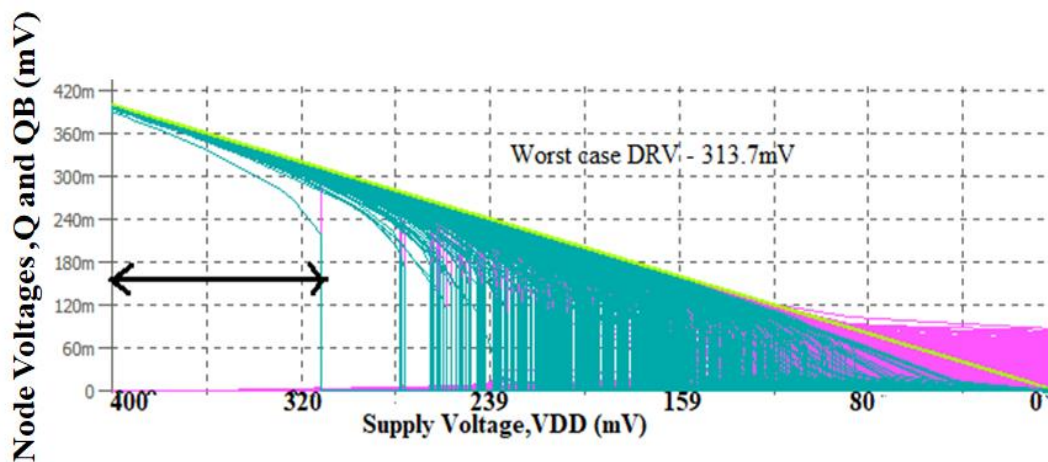
*Fig. 3.8 Worst-case DRV of the Proposed cell II at T = 27 °C under 6σ global process
and 1σ local mismatch variations*

I_{LEAK}

A plot of I_{LEAK} [16] is shown in Fig. 3.9 at different supply voltages. It is found that the leakage values of all the cells are comparable. However, the values in the proposed cell can be suppressed by using NWL technique [81]. The OFF access transistors are overdriven in hold mode by applying -80 mV at WWL. A reduction of 4.7 % and 12.5 % is achieved compared to conventional 6T cell and 7T_taw cells respectively at 0.4 V.
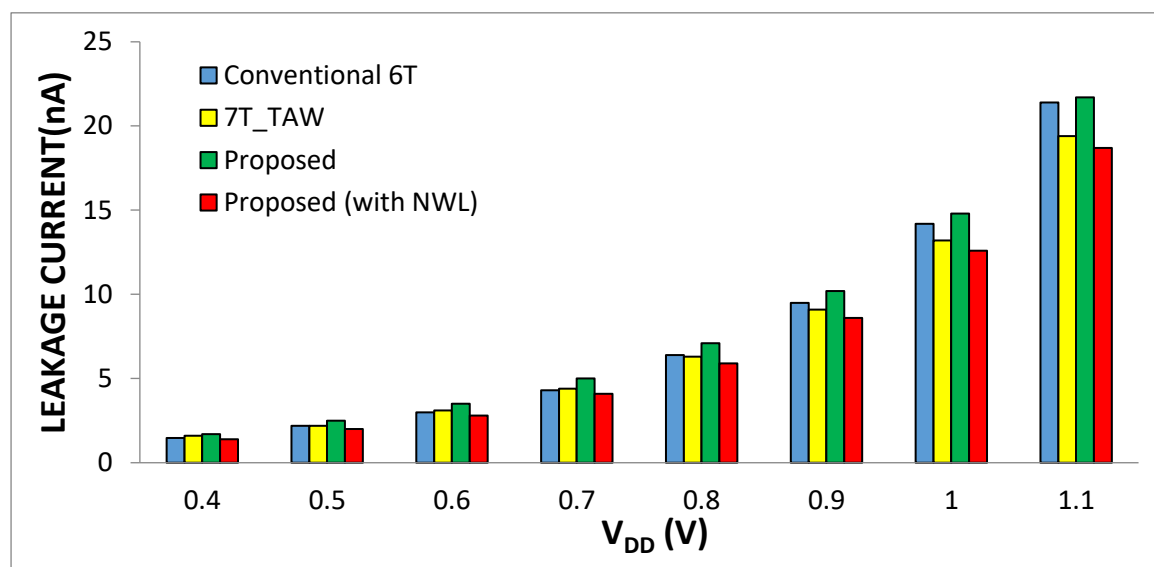
Fig. 3.9 I_{LEAK} for Proposed cell II (with and without NWL), Conventional 6T and 7T_taw SRAM cells

3.3.2 Proposed cell III

The schematic of the Proposed cell III with a novel read port is presented in Fig. 3.10(a). It consists of cross-coupled inverter pair (MUL-MDL and MUR-MDR), a differential write port (access transistors MAL-MAR, control signal WWL and complementary WBLs) for one-bit data storage and write operation, respectively. The novel three transistor-based read port performs single ended read and employs two nMOS transistors M1 and M2 driven by control signal RWL and internal data node DB respectively. The source terminal of M2 (RGND) is connected to row decoder that is maintained at GND and V_{DD} for the accessed and un-accessed cells, respectively. The transistors M1 and M2 provide a conditional

discharge path for RBL during read operation as RGND is connected to GND. The third transistor M3 is an LVT implemented pMOS driven by RWL which serves two purposes. It acts as a compensation transistor in accessed cell during read '1' operation, whereas it suppresses and equalizes RBL leakage component in un-accessed cells irrespective of the stored data.

(a)
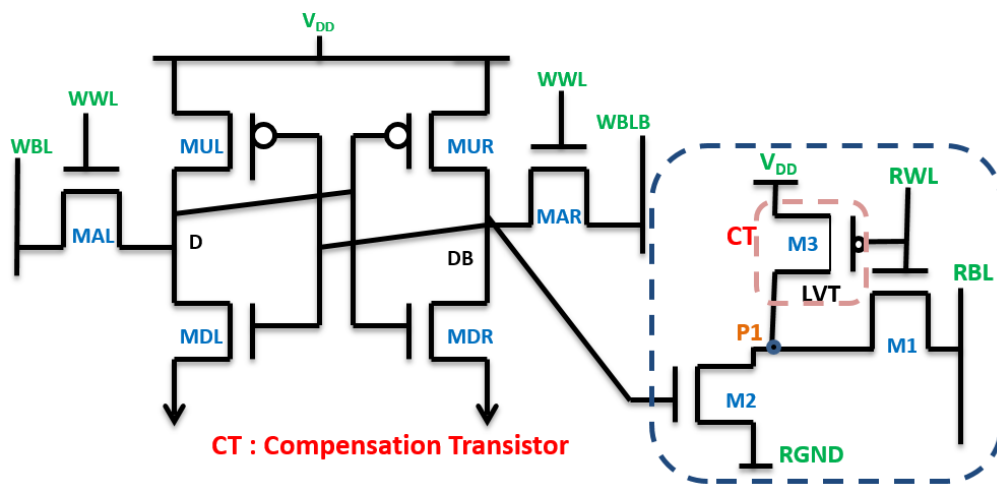
CONTROL SIGNAL MODE	WRITE	READ	HOLD
WWL	V_{DD}	GND	GND
RWL	GND	V_{DD}	GND
RGND	V_{DD}	GND	V_{DD}

(b)

Fig. 3.10 Proposed cell III (a) Schematic (b) Operating conditions

3.3.2.1 Operation

The control signals for different operations in the proposed cell are specified in Fig. 3.10(b). In the write mode, the new data are loaded on the complementary WBLs, and WWL is

asserted. The differential mode in proposed cell enables fast writing at lower voltages. The proposed cell shows worst-case WM ('0') of 80 mV and WM ('1') of 75 mV at 0.4 V under process variations as shown in Fig. 3.11. The observed values are optimum as higher values make the cell more susceptible to noise, whereas lower values make it difficult to write.
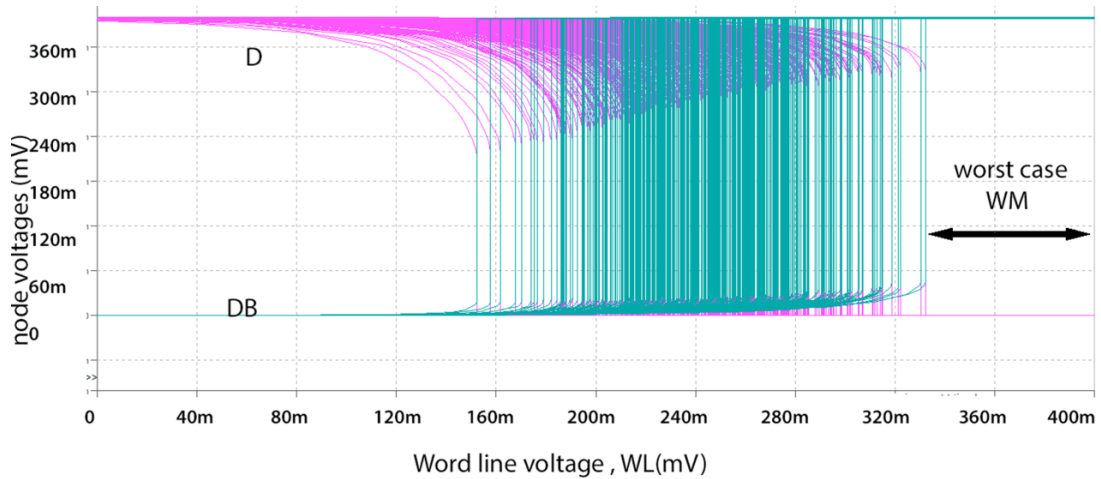
(a)
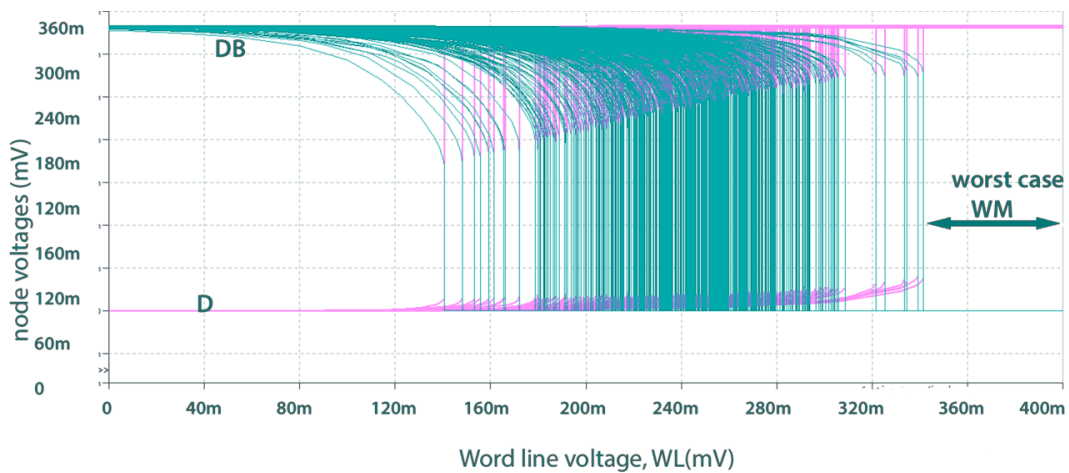
(b)

Fig. 3.11 WM (a) Worst-case WM ('0') (b) Worst-case WM ('1') for the Proposed cell III at V_{DD} = 0.4 V under 6σ global process and 1σ local mismatch variations (500 points)

During read '0' operation (DB = '1') in an accessed cell, a read current I_{ON} flows through ON transistors M1 and M2, while M3 remains OFF. Since the read path has only two

transistors, therefore, I_{ON} is higher than the existing read ports having more than two stacked transistors and is maintained even at lower voltages. Analogously, during read '1' operation (DB = '0'), M2 is OFF and a low-to-high transition on RWL (at gate of M3) augments the capacitive coupling effect at node P1 (drain of M3) leading to the flow of leakage current I_{L_AC} in opposite direction. This reverse current acts as a compensating current and compensates for the RBL leakage of the un-accessed cells and helps RBL to charge back to higher voltage [87]. Simultaneously, in the un-accessed cell with RWL as low and RGND at V_{DD}, the voltage at node P1 reaches V_{DD} as M3 conducts, and M2 remains OFF, irrespective of stored data. In order to ensure the maintenance of high voltage at node P1, a 500 points Monte Carlo simulation (6σ global process and 1σ local mismatch variations) was performed and the node P1 voltage distribution was plotted for both DB = '0' and DB = '1' in un-accessed cell.

(a)

102
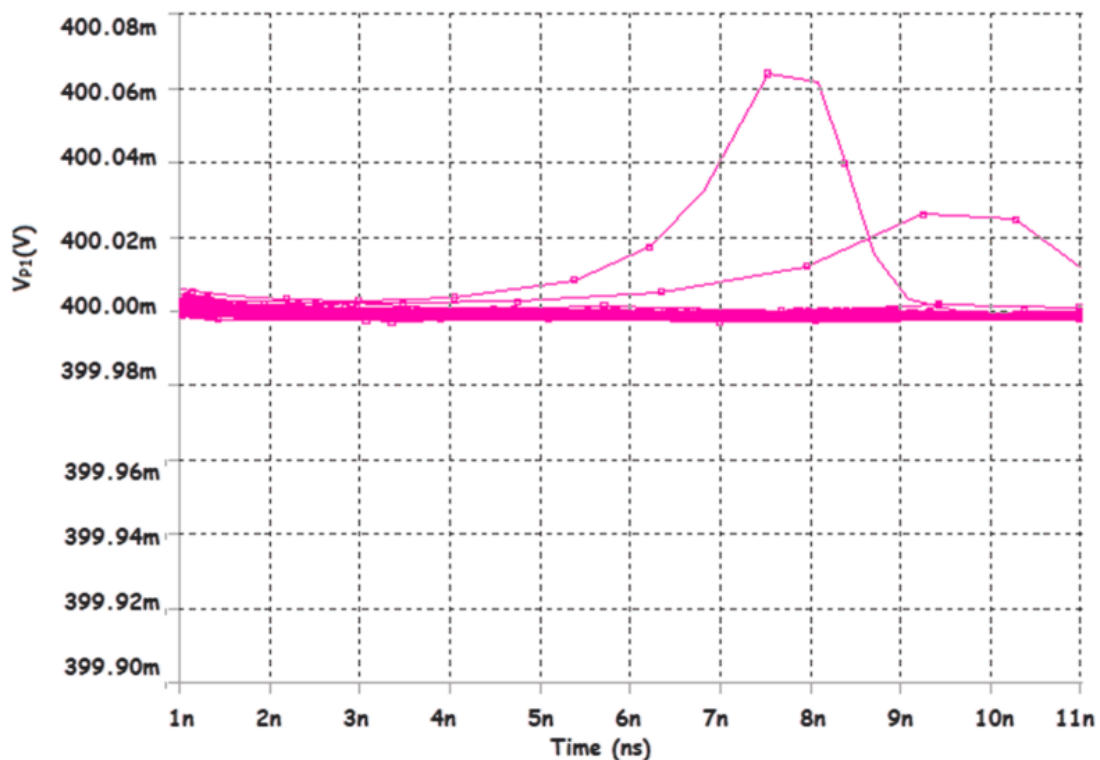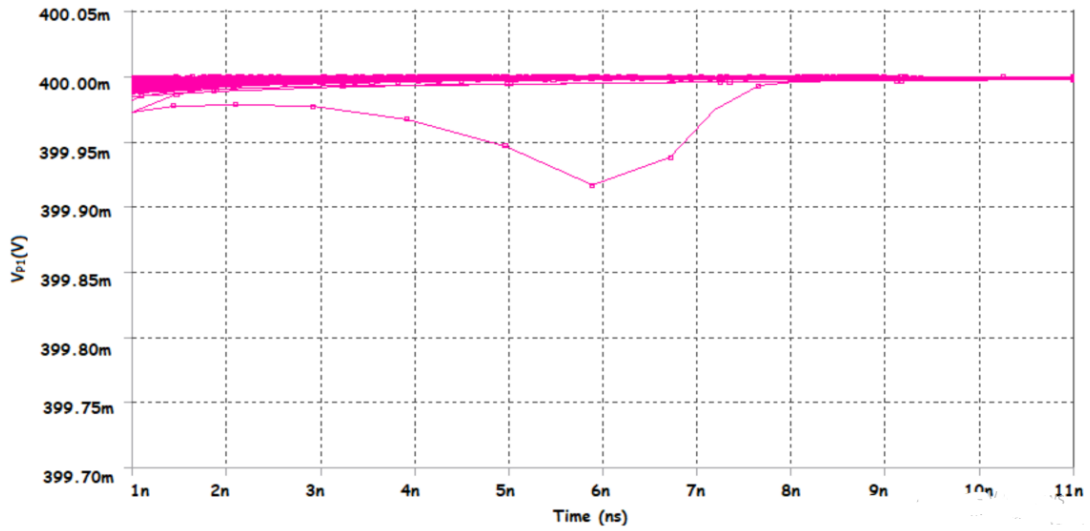
(b)

Fig. 3.12 P1 node voltage distribution in un-accessed cell for (a) DB = '0' and (b) DB = '1' at V_{DD} = 0.4 V under 6σ global process and 1σ local mismatch variations (500 points)

As seen in Fig. 3.12, the worst-case P1 node voltage at V_{DD} = 0.4 V remains closer to V_{DD} for both the cases (DB = '0' and DB = '1') under process variations. The V_{DS} of M1 is reduced, and the RBL leakage current of the read port in un-accessed cell is suppressed. Also, the leakage currents, I_{L_UC1} and I_{L_UC2}, are equalized as P1 remains at same potential in both the cases and makes the read port leakage data- independent. This further helps to maintain the required difference in magnitude of read '0' and read '1' current in proposed cell for proper sensing of stored data as shown in Fig. 3.13(a). This is not possible in case of conventional 8T SRAM cell (Fig. 3.13(b)) due to high magnitude and large data-dependency of RBL leakage currents.
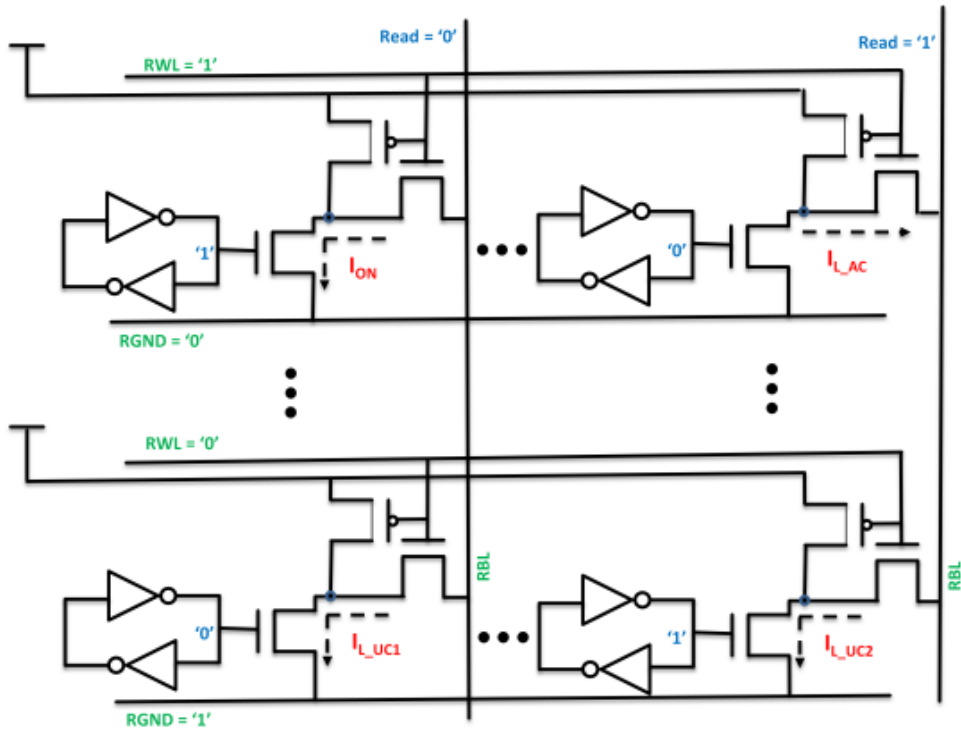
I_{L_UC2} is reduced and made equal to I_{L_UC1}, $\therefore I_{LEAK}(max) = I_{LEAK}(min)$

The single ended sensing in proposed cell with high I_{ON} and low data-independent RBL leakages always ensures following condition along the column in an array

$$I_{ON} + 127 * I_{LEAK} > 128 * I_{LEAK}$$

(a)
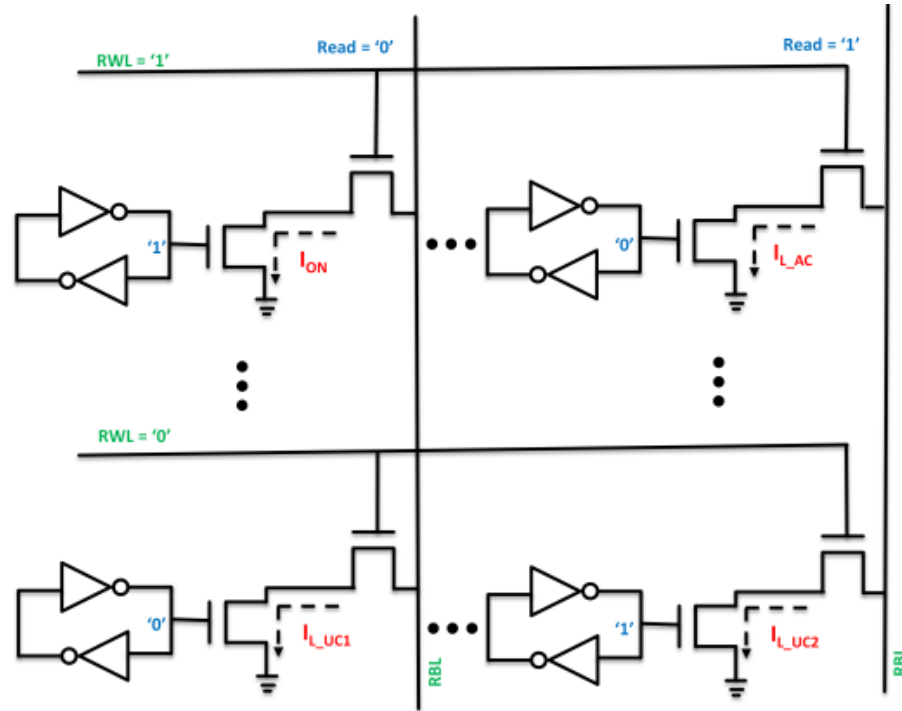
I_{L_UC2} **is much higher than** I_{L_UC1} **,** $\therefore I_{LEAK}(\text{max}) = I_{L\_UC2}$

The single ended sensing in 8T_conv cell with high and data-dependent RBL leakages leads to following condition along the column in an array

$I_{ON} + 127 * I_{L\_UC1} < 128 * I_{L\_UC2}$ or $I_{ON} + 127 * I_{L\_UC1} < I_{L\_AC} + 127 * I_{L\_UC2}$

(b)

Fig. 3.13 RBL leakages in (a) Proposed cell III (b) Conventional 8T [4] SRAM cell

The ΔV_{RBL} is shown in Fig. 3.14(a). Due to the reverse flow of I_{L_AC} and reduced leakages during read '1' operation, the RBL voltage level rises from V_{DD} to V1. Additionally, the high read current, during read '0' operation, helps RBL to discharge faster to V2 leading to improvement in the ΔV_{RBL} from $(V_{DD} - V2)$ to $(V1 - V2)$. Fig. 3.14(b) shows the butterfly curve for the proposed cell in hold mode. The curve was obtained after a 500 points MC simulation under 6σ global process and 1σ local mismatch variations. As can be seen, the proposed cell maintains the butterfly curve even at low supply voltage of 0.4 V, thus ensuring the stability of data in hold mode at lower voltages. It is clear from the above

discussion that the Proposed cell III achieves improved read performance parameter at lower supply voltages.
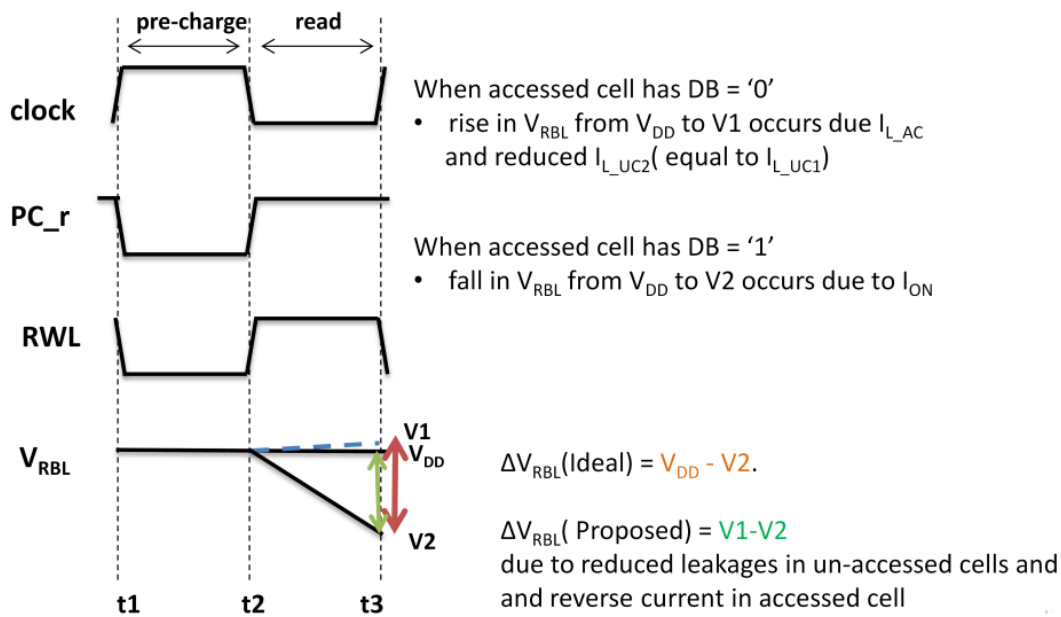
(a)
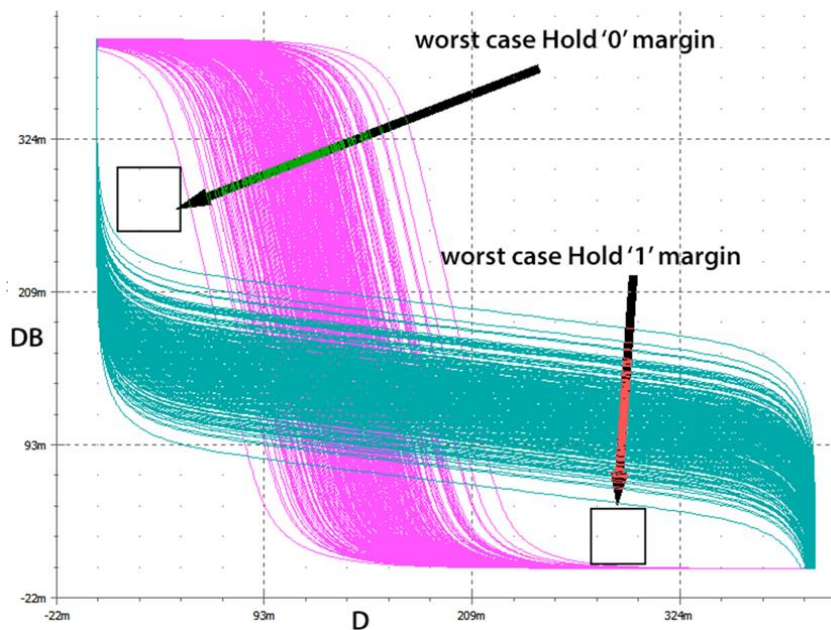
(b)

Fig. 3.14 (a) Impact of leakage currents on ΔV_{RBL} (b) Worst-case Hold '0' margin and Hold '1' margin for the Proposed cell III at V_{DD} = 0.4 V under 6σ global process and 1σ local mismatch variations (500 points)

3.3.2.2 Simulation results

To evaluate the performance of the Proposed cell III, a column containing 128 cells is simulated using 32 nm bulk CMOS PTM model parameters. The existing SRAM cells, discussed in section 3.2, are simulated and their read port performance is captured for completeness. The aspect ratio of the transistors is tabulated in Table 3.2. The simulation results of the cells at typical process corner, 27 ˚C for near threshold (V_{DD} = 0.5 V) and sub-threshold (V_{DD} = 0.3 V) regions, are listed in Table 3.3. The results pertaining to the performance parameter along with the effect of PVT-variations are discussed individually in the subsections.

Table 3.2: Aspect ratio of transistors

SRAM cells	Transistors (λ = 18 nm)					
	MUL/MUR	MAL/MAR	MDL/MDR	M1/M2	M3	M4
8T_conv [4]	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	-	-
7T_taw [12]	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	-	-
9T_ver [47]	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	-
9T_wang [48]	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	-
10T_chris [86]	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ
10T_cal [51]	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ
10T_sh [57]	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ
9T_pasa [49]	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ
Proposed cell III	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	4λ/2λ	-

Table 3.3: Typical values of performance parameter at TT corner, 27 ˚C

Category	SRAM cells		$V_{DD} = 0.3$ V	$V_{DD} = 0.5$ V
2T	8T_conv [4]	I_{ON}/I_{OFF} ratio	319	5,872
		ΔV_{RBL}	Fails	Low
		T_{READ_ACCESS} (ps)	45,031	1,454
	7T_taw [12]	I_{ON}/I_{OFF} ratio	399	31,659
		ΔV_{RBL}	Fails	Low
		T_{READ_ACCESS} (ps)	44,833	1,480
3T	9T_ver [47]	I_{ON}/I_{OFF} ratio	564	15,933
		ΔV_{RBL}	Fails	High
		T_{READ_ACCESS} (ps)	79,127	2,467
	9T_wang [48]	I_{ON}/I_{OFF} ratio	309	5,875
		ΔV_{RBL}	Fails	Low
		T_{READ_ACCESS} (ps)	15,692	1,212
4T	10T_chris [86]	I_{ON}/I_{OFF} ratio	14,533	108,280
		ΔV_{RBL}	High	High
		T_{READ_ACCESS} (ps)	102,345	2,606
	10T_cal [51]	I_{ON}/I_{OFF} ratio	1,073	52,960
		ΔV_{RBL}	Low	High
		T_{READ_ACCESS} (ps)	100,339	2,528
	10T_sh [57]	I_{ON}/I_{OFF} ratio	559	15,933
		ΔV_{RBL}	Low	High
		T_{READ_ACCESS} (ps)	67,260	2,419
	9T_pasa [49]	I_{ON}/I_{OFF} ratio	14,533	107,595
		ΔV_{RBL}	High	High
		T_{READ_ACCESS} (ps)	101,985	2,592
3T(PROPOSED)	Proposed cell III	I_{ON}/I_{OFF} ratio	22,733	182,390
		ΔV_{RBL}	High	High
		T_{READ_ACCESS} (ps)	65,463	1,527

I_{ON}/I_{OFF} ratio

It can be observed in Table 3.3 that all the cells show low I_{ON}/I_{OFF} ratio in near threshold value, except proposed, 10T_chris, and 9T_pasa cells with proposed cell showing the best performance among all. The poor performance of other cells is attributed to the degraded I_{ON} values in comparison to I_{OFF} values in this region. As the voltage scales down, the decreasing I_{ON} values as well as increasing I_{OFF} values result in even more performance degradation in sub-threshold region. The impact of voltage scaling is low in proposed, 10T_chris, and 9T_pasa SRAM cells, with proposed SRAM cell showing 1.68X and 1.69X higher value in comparison to 10T_chris and 9T_pasa, respectively. The result exemplifies the ability of the proposed cell to suppress the leakage current while maintaining better read performance even in sub-threshold region where almost all the SRAM cells fail to register reasonable values.

Fig. 3.15(a) shows the effect of process variations on I_{ON}/I_{OFF} ratio of all cells with "red curve" representing the performance of proposed cell in all the graphs. It is worth noting that as the process corner changes from SS to FF, the ratio of all the cells plummets to negligible values while that of proposed, 10T_chris, and 9T_pasa become even better. This is because as nMOS and pMOS become faster, I_{ON} as well as I_{OFF} values increase, but due to the additional leakage reduction ability of the cells, there is a negligible increase in leakage current resulting in improved values. In fact, the proposed cell shows remarkable performance with 1.62X and 1.61X higher I_{ON}/I_{OFF} ratio compared to 10T_chris and 9T_pasa cells, respectively, at FF corner in near threshold region. Due to similar performance, the curves for 10T_chris and 9T_pasa overlap in the figure.

Similarly, Fig. 3.15(b) captures the impact of temperature on the performance of the cells. As the temperature increases from −40 ˚C to 125 ˚C, the leakage current increases resulting in degraded performance at higher temperature in all SRAM cells. However, the proposed

cell shows extremely good performance across all the temperatures. In fact, at highest temperature in near threshold region, the proposed cell shows 1.6X, 33.2X, 85.7X, 1.6X, 85.7X, 155.4X, 122.6X, and 163.2X better I_{ON}/I_{OFF} ratio compared to 10T_chris, 10T_cal, 10T_sh, 9T_pasa, 9T_ver, 9T_wang, 7T_sh, and 8T_conv cells, respectively.
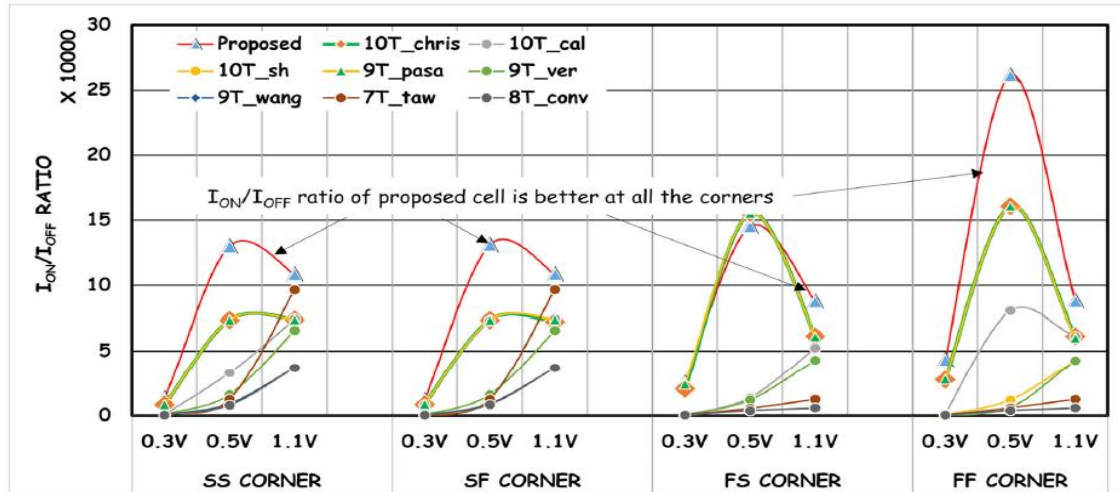
(a)
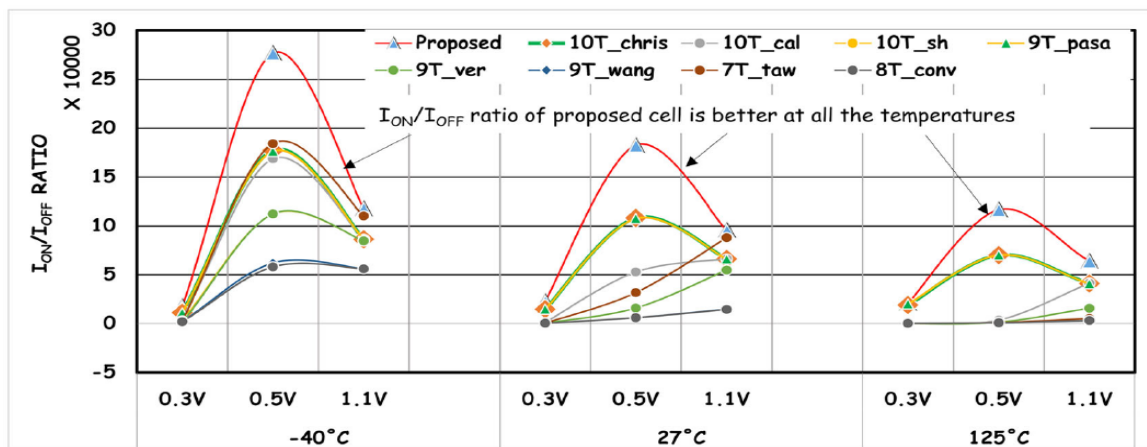
(b)

Fig. 3.15 Effect of (a) process corners (at T = 27 ˚C) and (b) temperature (at TT corner) on I_{ON}/I_{OFF} ratio

Data-independent RBL leakages

To evaluate the data-dependent nature of leakages in un-accessed cells, three different data patterns are assumed to be stored in the cells along the column. The stored value at DB node is considered to be '1' for all the un-accessed cells in Case 1 and half of the un-accessed cells in Case 2, while Case 3 assumes that all the un-accessed cells store '0'. The corresponding discharge of voltage of RBL (which otherwise should remain high as DB = '0' in accessed cell) due to leakage in these cells is then monitored with respect to time [49].

Case 1 represents the worst-case situation wherein the maximum leakage current (I_{L_UC2}) flows through all un-accessed cells due to which RBL discharges quickly towards '0'. In Case 2, half of the un-accessed cells draws leakage current I_{L_UC1} while the remaining cells draw I_{L_UC2}; therefore, due to data-dependent leakages, RBL discharges slowly towards logic '0' in comparison to previous case. Similarly, in Case 3, the leakage current I_{L_UC1} flows through all the un-accessed cells resulting in slow discharging of the RBL line. Simulations are done for the above three cases in near threshold region.

The drop in RBL voltage with respect to time for the three cases (when it should not be discharged) is shown in Fig. 3.16 for the proposed cell and in Fig. 3.17 for its counterparts. As can be seen, the RBL voltage discharges to approximately 499 mV when RWL is asserted at 100 ns in the proposed cell, whereas for other cells, the situation is completely different.

The result confirms high and data-dependent leakage issues in 9T_ver, 7T_taw, and 8T_conv cells as RBL discharges to 488 mV, 466.6 mV, and 447.7 mV, respectively, from 500 mV in the worst-case. Thus, these cells have high read failures [57][86], though the leakage in 10T_cal cell is data-dependent but RBL discharge is very small (497.1 mV). Further, the 9T_wang and 10T_sh cells show data-independent leakages but suffer from

high leakage current with RBL discharging to 447.9 mV and 488 mV, respectively. The situation gets worsen during read '1' operation specifically at higher temperatures that may lead to false sensing of data. The proposed, 10T_chris, and 9T_pasa cells show low and data-independent leakages since RBL discharge is negligible even at 170 ns.
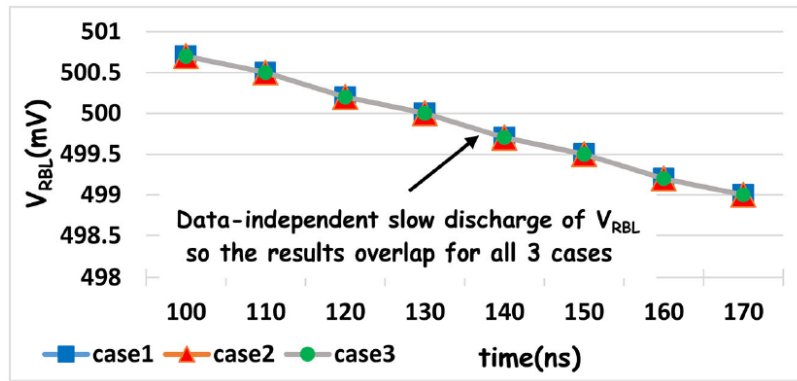
Fig. 3.16 RBL voltage of the Proposed cell III for three different data patterns in un-accessed cells
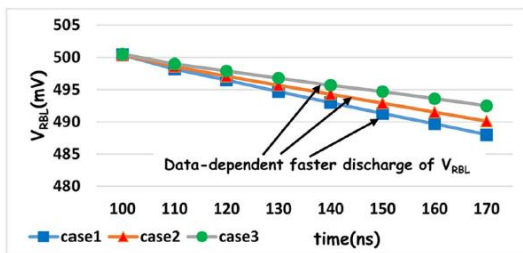
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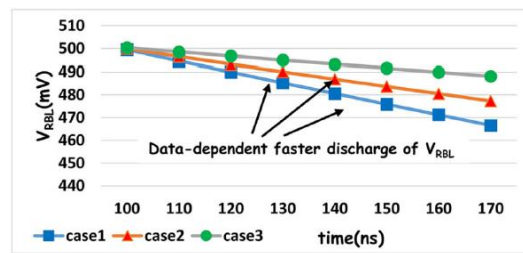
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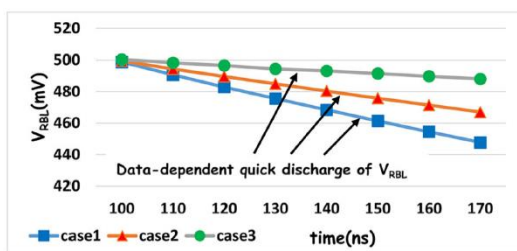
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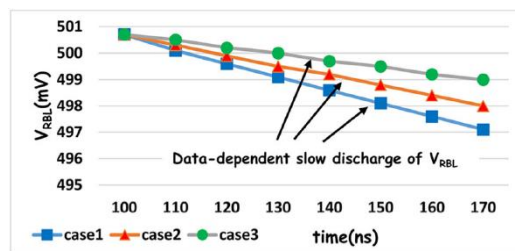
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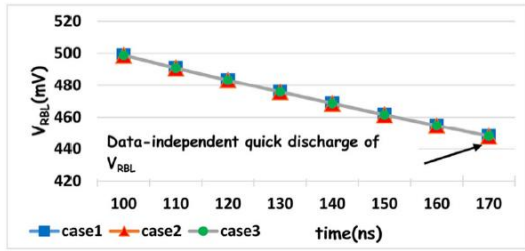
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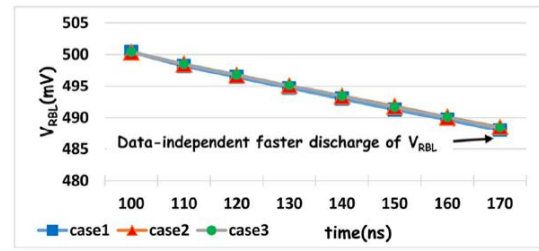
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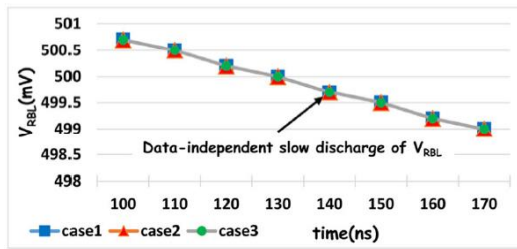
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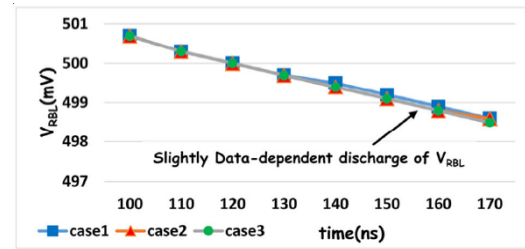
(h)

Fig 3.17 RBL voltage of existing cells for three different data patterns in un-accessed cells (a) 9T_ver, (b) 7T_taw, (c) 8T_conv, (d) 10T_cal, (e) 9T_wang, (f) 10T_sh, (g) 10T_chris, and (h) 9T_pasa SRAM cells

ΔV$_{RBL}$

For the values of ΔV$_{RBL}$, listed in Table 3.3, it is observed that all 2T or 3T read port-based SRAM cells show poor performance except 9T_ver cell at 0.5 V while the 4T-based read ports shows remarkable performance in this respect. At 0.3 V, all 2T and 3T read port-based cells fail to maintain positive values of ΔV$_{RBL}$ and suffer from read failures. The performance of 4T read port-based SRAM cells 10T_sh and 10T_cal degrade due to increase in sub-threshold leakage current. In case of 9T_pasa, 10T_chris, and proposed cells, the data-independent compensation suppress leakages and helps in maintaining high value of ΔV$_{RBL}$ even in sub-threshold region.

The effect of process corners on ΔV_{RBL} captured in Fig. 3.18(a) identifies FS corner as the worst corner across all the cells. This happens because as the nMOS becomes faster and pMOS becomes slower, the leakages through all the un-accessed cells increase sharply degrading their performance. The SRAM cells with 2T, 3T, and 4T (10T_cal and 10T_sh) read ports fail to maintain positive values of ΔV_{RBL} at FS and FF corners and hence suffer from read failures. However, the proposed, 10T_chris, and 9T_pasa cells show reasonable performance irrespective of process corners.

Similarly, with respect to temperature variation, the cells show their worst performance at 125 ˚C, respectively, as shown in Fig. 3.18(b). The SRAM cells with 2T, 3T read ports fail at 125 ˚C irrespective of supply voltage depicting degradation of ΔV_{RBL} at higher temperatures. Additionally, 10T_cal and 10T_sh fail at 125 ˚C in sub-threshold region while the proposed, 10T_chris, and 9T_pasa cells maintain reasonable ΔV_{RBL} at all temperatures. Thus, it can be concluded that all the cells except proposed, 10T_chris, and 9T_pasa cells are more prone to read failures due to PVT-variations.
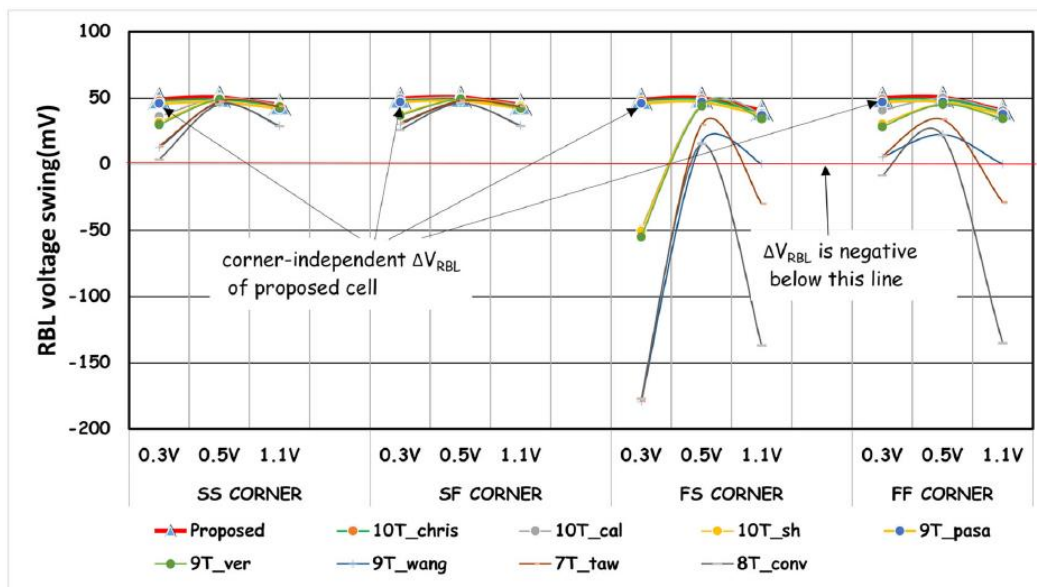
(a)
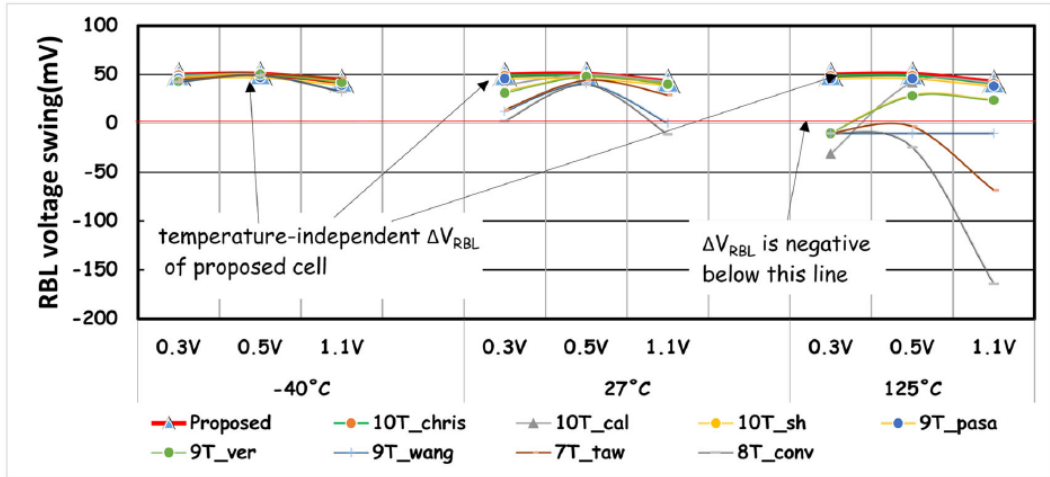
(b)

Fig. 3.18 Effect of (a) process corners (at T = 27 ˚C) and (b) temperature (at TT corner) on ΔV$_{RBL}$

T$_{READ\_ACCESS}$

The T$_{READ\_ACCESS}$ values listed in Table 3.3 shows an increasing trend with scaling down of the supply voltage from 0.5 V to 0.3 V at TT corner. It is worth mentioning that the read access failure occurs if RBL fails to discharge below 50 mV or discharges below this value even before RWL is turned ON [57]. The proposed cell shows better results compared to other SRAM cells apart from 8T_conv, 7T_taw, and 9T_wang cells in sub-threshold region as the rest of the cells suffers from degraded read current values due to more transistors in the read path. The results for process corner variations shown in Fig. 3.19(a) depict a decrease in T$_{READ\_ACCESS}$ as process corner changes from SS to FF. This can be attributed to increased read current flowing through faster nMOS transistors in read ports at FF corner. It is worth mentioning that at FS corner, in 8T_conv and 7T_taw SRAM cells, the RBL discharges below 50 mV due to high leakages even before RWL turns ON resulting in read failures. The impact of temperature is represented in Fig. 3.19(b). It is seen that as the temperature increases from −40 ˚C to 27 ˚C, the T$_{READ\_ACCESS}$ decreases in cells due to

115

the faster discharging of RBL owing to increased read current values with proposed cell showing the best performance. However, the situation is entirely different at higher temperatures. At 125 ˚C, due to sharp increase in leakage current in sub-threshold region (0.3 V) as well as the inability of 2T and 3T read port-based SRAM cells to maintain leakage current under limits, the cells suffer from read failure with RBL discharging below 50 mV even before RWL is activated in these cells during read operation. It has also been observed that 9T_wang fails throughout the supply voltage range (1.1 to 0.3 V) at higher temperature due to extremely high leakage current in un-accessed cells which discharges RBL to lower voltages irrespective of the data stored at internal node in accessed cell. Thus, it can be concluded that though 2T and 3T read port-based SRAM cells show better results than proposed cell at TT corner and 27 ˚C but under PVT-variations, these cells suffer from read failure whereas proposed cell continues to show reasonable performance across all corners, supply voltages, and temperatures.

(a)

Read access time(ps)

Legend: Proposed, 10T_chris, 10T_cal, 10T_sh, 9T_pasa, 9T_ver, 9T_wang, 7T_taw, 8T_conv

Tread_access of proposed cell is better than all 4T read port-based cells across all temperatures
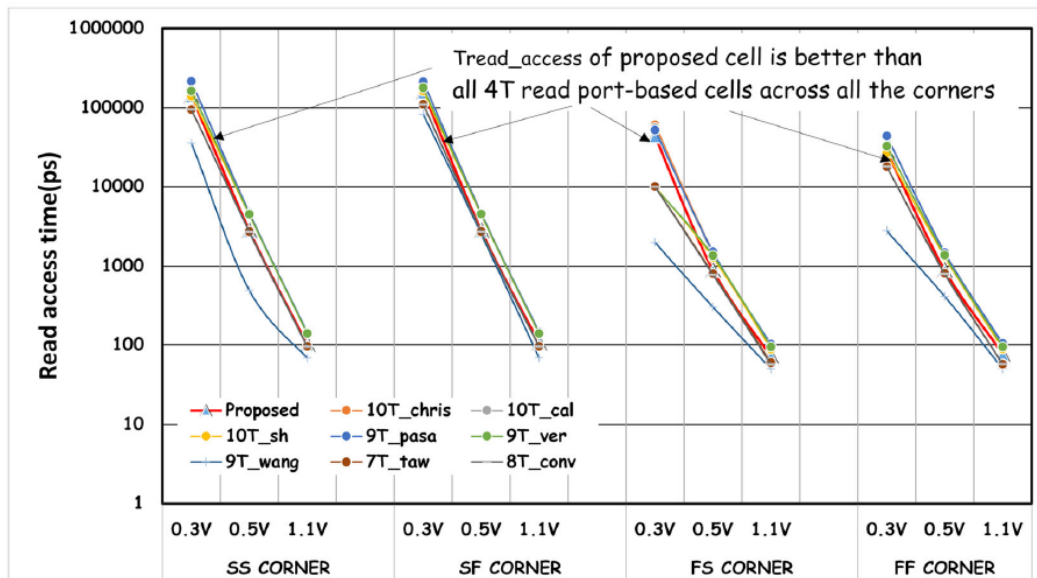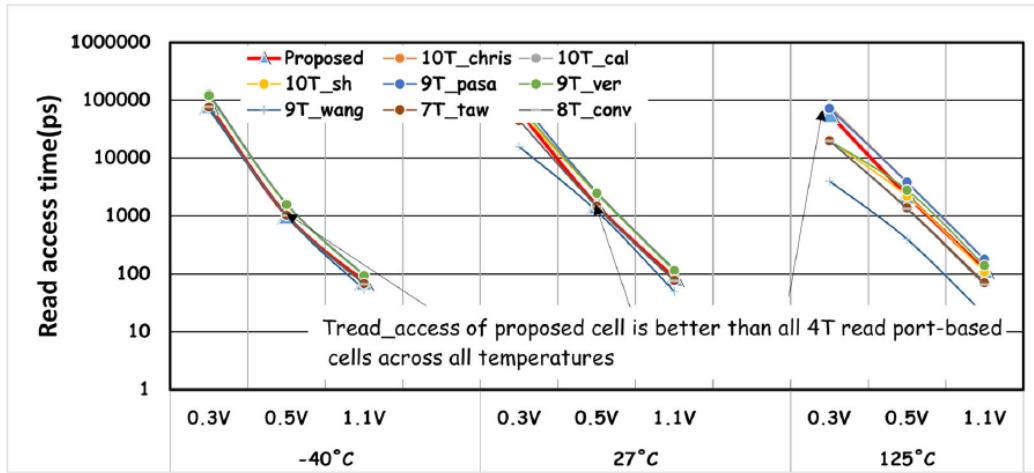
(b)

Fig. 3.19 Effect of (a) process corners (at T = 27 ˚C) and (b) temperature (at TT corner)

on T_{READ_ACCESS}

Thus, it can be concluded that though 2T and 3T read port-based SRAM cells show better results than proposed cell at TT corner and 27 ˚C but under PVT-variations, these cells suffer from read failure whereas proposed cell continues to show reasonable performance across all corners, supply voltages, and temperatures.

3.4 Conclusions

In this chapter, Proposed cell II and III with improved read and write performance are presented. The proposed cells resolve the read-write conflict issue of existing cells by isolating the read port from internal storage nodes. The read port performance is further enhanced by removing the stacking of MOS transistors in the read port thereby achieving significantly high read current values in Proposed cell II . Alternately, in Proposed cell III, a compensation transistor is incorporated in the read port to compensate for the leakages in accessed and un-accessed cells while maintaining reasonable values of read current. This resolves the trade-off between read current values and RBL leakages in Proposed cell III

and results in significant improvement in read port performance parameters. Further the write performance is improved by employing write assist transistor to weaken the pull down path during single ended write operation in Proposed cell II and by employing faster differential write in Proposed cell III.

The Proposed cell II shows 2.7X, 1.2X and 1.2X improvement in RSNM, WSNM and I_{ON} values compared to conventional structure. The improvement achieved with respect to 7T_taw SRAM cell in RSNM, WSNM, I_{ON} and DRV are 2.2X, 1.2X, 3.1X, 2.0X and 2.8X respectively at 0.4 V supply voltage. The leakages in proposed cell are reduced by employing the NWL technique. The cell responds well to the technique and shows significant reduction in I_{LEAK} values compared to other SRAM cells.

The Proposed cell III achieves larger ΔV_{RBL} compared to other 2T, 3T, and some 4T read port-based SRAM cells. The T_{READ_ACCESS} is up to 1.5X, 1.7X, and 1.3X lesser as compared to existing 4T read port-based SRAM cells at 0.3, 0.5, and 1.1 V, respectively, at TT corner and 27C. It also provides up to 73.5X, 31X, and 6.6X higher I_{ON}/I_{OFF} ratio compared to 2T, 3T, and some 4T read port-based SRAM cells under similar operating conditions allowing the greater potential for area savings. The cell also shows less sensitivity to PVT-variations, whereas the other cells fail at one operating condition or the other. In addition, the cell provides faster differential writing with worst-case WM '0' and '1' as 80 mV and 75 mV respectively under process variations at a supply voltage of 0.4 V.

CHAPTER 4

SRAM CELL DESIGN WITH PVT-VARIATION TOLERANCE

The content and results of the following paper has been reported in this chapter

Gupta M, Gupta K, Pandey N, " **A Novel PVT-Variation Tolerant Schmitt-Trigger Based 12T SRAM Cell with Improved Write Ability and High I_{ON}/I_{OFF} Ratio in Sub-Threshold Region**", International Journal of Circuit Theory and Applications, Wiley,1-22,2021 **(SCI Journal with Impact Factor: 2.038)**.

4.1 Introduction

The SRAM cell designs with improved read and/or write performance are addressed in Chapter 3. The sensitivity of SRAM to PVT-variations [53] is an equally important issue in designs operating at lower technology nodes and reduced supply voltages, especially in sub-threshold region, as it may lead to high memory failures [45][109]. It is suggested in the literature that the sensitivity to PVT-variations may be improved by replacing CMOS inverters of conventional 6T SRAM core by Schmitt-trigger (ST) inverters as it has an inbuilt ability of adaptively changing the switching threshold voltage against variations.

This chapter deals with the design of SRAM cell with PVT-variation tolerance i.e. ST based SRAM cells. The existing ST based SRAM cells [53][59][61][107] are briefly reviewed in section 4.2. It is observed that a ST based SRAM cell that can simultaneously address degraded write ability, low read stability and poor I_{ON}/I_{OFF} ratio and the issue of data-dependent tolerance against PVT-variations is not addressed in literature. Therefore, a novel PVT-variation tolerant SRAM cell that can improve performance in read, write and hold modes is proposed in the section 4.3 and is termed as Proposed cell IV. Thereafter, the functionality of the proposed cell is verified in all the three operating modes and its performance is compared with the existing ST based and some most recent SRAM cells in terms of various standard cell metrics. The plot of failure probabilities and subsequent estimation of minimum supply voltage in each operating mode is also carried out to ascertain the improved PVT-variation tolerant behavior of the proposed cell.

4.2 Existing SRAM cell designs with PVT-variation tolerance

The 8T_conv [4] SRAM cell decouples the read and write ports to eliminate the read/write conflict issue of conventional 6T SRAM cell. It provides a read-disturb free memory operation and achieves significant improvement in read stability as access is performed

through an isolated read port. However, the cell possesses a limitation of low I_{ON}/I_{OFF} ratio, poor write ability and PVT-variations induced memory failures in the sub-threshold region. Device sizing overcomes few limitations but its efficacy reduces at lower voltages. Different SRAM cell designs having tolerance against PVT-variations and improved write ability in comparison to 8T_conv [4] cell are introduced in literature [53][59-61][107]. The SRAM cells suggested in [53][59][61][107] use ST action for modulating the threshold voltage of the inverters so as to reduce their sensitivity against PVT-variations, whereas, the SRAM cell in [60] uses an innovative write assist technique to improve the write ability in sub-threshold region. The two ST SRAM cells, introduced by Kulkarni et al. are referred to as 10T_st1 [53] and 10T_st2 [107] cells respectively from here on. The SRAM cells presented by Sayeed et al., Sachdeva et al. and Sharma et al. are referred to as 11T_say [59], 12T_ash [61] and 12T_vish [60] cells from hereafter.

In 10T_st1 [53] cell, the ST action controlling feedback transistors are driven by internal storage nodes rendering it dependent upon the values stored at the internal nodes. The ST action remains OFF in the branch storing '0'. In the hold mode, this provides a low resistance pull-down path for the node storing '0' and prevents the node holding '1' from discharging due to leakages or PVT-variations, thereby providing significant improvement in hold stability. In the read mode, the read current passes through the node storing '0' and raises the voltage at this node. The absence of ST action in this branch and presence of a stack of three transistors in the read path lowers the read stability and read current (I_{ON}) values respectively [51][54][107]. This reduces the I_{ON}/I_{OFF} ratio and increases the read failures [107]. In addition, the presence of ST action in write mode negatively affects the write ability and makes the cell difficult to write.

In 10T_st2 [107] cell, the feedback transistors are driven by separate control signal so the ST action remains active if the signal is kept high. The ST action is kept active in read and

write modes, and inactive in hold mode. The cell provides improved write ability and read stability due to the presence of multiple leakage paths during write mode and reading of virtual node during read mode respectively. In addition, the read path consists of two transistors resulting in improved I_{ON} values and better access time. However, the absence of ST action in the hold mode degrades the hold stability in the cell. In addition, the connection of two access transistors per SRAM cell to each bitline adds to the bitline capacitance and increases leakages during hold mode. Thus, the cell has reduced I_{ON}/I_{OFF} ratio, degraded hold stability and more power consumption with longer discharge time [38][59].

In 11T_say [59] cell, the gate terminal of feedback transistors are connected to internal nodes while the drain terminals are connected to a separate control signal which is the compliment of wordline signal. The control signal is kept low during write mode to disable the ST action. A row-based control signal VGND is used to address low-voltage write problem and mitigate the half-select cell issue. However, due to single-ended writing, it suffers from extremely poor write ability and increased T_{WRITE_ACCESS}. The floating-ground write-assist technique fails to improve the write ability of the cell in sub-threshold region. The use of an isolated read port and presence of ST action during hold mode provides improved read stability and hold stability respectively. However, the use of similar read port, as is used in 8T_conv [4] SRAM cell, leads to read related issues like high read port leakages and poor I_{ON}/I_{OFF} ratio.

The 12T_ash [61] cell, uses the internal nodes to drive the feedback transistors. Thus, the ST action remains inactive in the branch of the latch that stores '0' just as the case with 10T_st1 [53] cell. This improves the hold stability but negatively influences the write ability of the cell. The use of differential write along with the use of two write-assist transistors improves the write ability marginally. During hold mode, the presence of

wordline driven ON pull-up/pull-down write-assist transistor in the latch increases the leakage and makes the data stored at internal node unstable. During read mode, the read current passes through a stack of three MOS transistors. This reduces the read current values and adversely affects the T_{READ_ACCESS} and I_{ON}/I_{OFF} ratio. In addition, the flow of read current through internal storage node and absence of ST action in the same branch raises the voltage at internal node and reduces the read stability of the cell. The control signals controlling the write-assist transistors are both row-based. This renders the data stored in row half-select cells unstable during write operation.

To address the read/write related issues that are not resolved by ST based SRAM cells, the 12T_vish [60] cell, uses an innovative write-assist technique to improve the write ability in sub-threshold region. It uses data-dependent feedback-path cutting technique by turning OFF either of the pull down transistors during write operation. The advantage is that it uses the bitline pairs to weaken the feedback loop of cross-coupled latch and assist the write operation. The isolated read port improves the read stability and use of fully-gated ground scheme reduces the read port leakages. However, the technique suffers from few major drawbacks. First, the cell suffers from high T_{WRITE_ACCESS} due to the presence of a stack of two access transistors like the one used in [55] that further degrades under PVT-variations. Next, it suffers from high leakages and bitline load capacitance due to the connection of two transistors per SRAM cell to BLB and three transistors to BL. This deteriorates the I_{ON}/I_{OFF} ratio and increases the power consumption. The hold stability is also low compared to the ST based SRAM cells due to the presence of two ON transistors and one OFF transistor in each inverter of a latch during hold mode.

It is thus clear that a ST based SRAM cell which simultaneously address degraded write ability, destructive read operation, poor I_{ON}/I_{OFF} ratio and data-dependent tolerance against PVT-variations is not available in literature. Therefore, there is a need of an improvised

SRAM cell design that can use some effective technique to speed-up the write operation and improve write ability without degrading other performance parameters. The isolated read port provides high read stability but suffers from high read port leakage that needs to be addressed. Additionally, the immunity of the SRAM cell against PVT-variations should be improved in both read and hold modes independent of values stored at internal storage nodes. All these concerns are addressed in the proposed cell with the help of modified ST action, Negative bitline technique and fully-gated ground scheme with almost no trade-off among the performance parameters.

4.3 Design of SRAM cell with PVT-variation tolerance

To address the issues of existing PVT-variation tolerant SRAM cells, a novel PVT-variation tolerant ST based SRAM Cell with improved performance in all the three operating modes in sub-threshold region is presented.

4.3.1 Proposed cell IV

The schematic of the Proposed cell IV is shown in Fig. 4.1(a). It employs two back to back connected ST inverters (Inverter1 : MUL-MDL-MDL2-MFL; Inverter2 : MUR-MDR-MDR2-MFR) with write access transistors (MAL, MAR) and isolated read port (M1, M2). The cell exhibits differential write wherein the control signal, WWL, drives the access transistors and connects the internal nodes to complementary WBLs. The RBL in isolated read port along with WBL accomplishes the differential read operation in the cell. The differential read in proposed cell offers faster differential sensing over single ended read. The two column-based signals (WL_Y1 and WL_Y2) controls the ST action in the cell during memory operation.
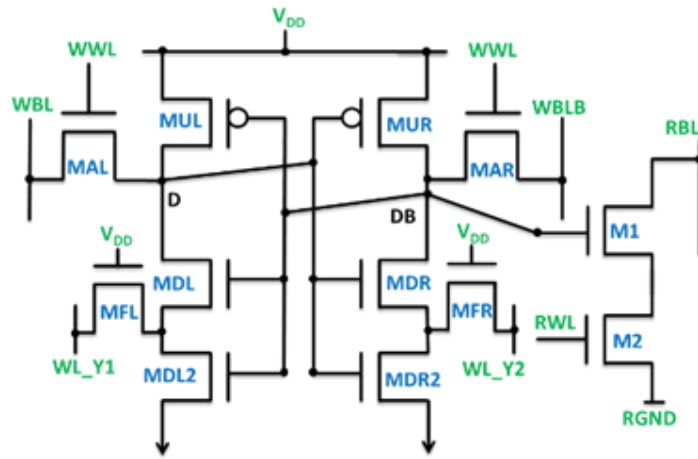
(a)

Control Signals Mode of Operation	Read	Write '0'	Write '1'	Hold
WWL	0	1	1	0
WL_Y1	1	0	1	1
WL_Y2	1	1	0	1
RWL	1	0	0	0
RGND	0	1	1	1

(b)

Fig. 4.1 Proposed cell IV (a) Schematic (b) Operating conditions

4.3.1.1 Operation

In the Proposed cell IV, the transistors MFL and MFR are responsible for ST action in all the three operating modes. In read and hold modes, the ST action provides tolerance against PVT-variations whereas during write mode it assists the write operation in improving the write ability of the cell.

Write mode

The write operation uses the combination of Negative bitline write-assist technique (NBL) [112] and ST action for improved write ability especially in sub-threshold region. The operating condition mentioned in Fig. 4.1(b) are maintained in the write mode. The timing diagram to illustrate the sequencing of the signals is drawn in Fig. 4.2(a). During a write '1' operation, WBL is asserted high whereas WBLB is pulled towards negative voltage (V_{NBL}) through the write driver as shown in Fig. 4.2(b). The signals WL_Y1 and WL_Y2 are set at high and low voltage levels respectively. The WWL signal is enabled at the negative edge of the clock cycle in the accessed cell. In Inverter1, the ST action due to MFL causes increase in threshold voltage (V_{th}) of MDL. This reduces the driving strength of the pull-down path (MDL, MDL2) which favors the charging of node D. On the other hand, in Inverter2, the node DB discharges quickly due to two favoring effects. The discharging current through MAR is increased due to negative voltage (VNBL) at WBLB. In addition, the formation of an auxiliary leakage path through MFR, provides an alternative discharge path, thus, considerable improvement in write ability of the Proposed cell IV is observed. Due to the symmetrical structure of the SRAM cell, the write '0' operation is also performed in the similar manner.

Read mode

The Proposed cell IV exhibits differential read wherein pre-charged bitline, WBL, acts as the reference voltage while RBL conditionally discharges depending upon the value stored at node DB (Fig. 4.2(c)) to provide faster differential sensing through current-mirror based differential sense amplifier [1]. A differential sensing helps to reject the common-mode noise that may be induced on both the bitlines due to power spikes, capacitive coupling between bitlines or between wordline and bitline. During read mode, the operating conditions as indicated in Fig. 4.1(b) are maintained. The RGND signal is pulled low and

RWL is enabled in the accessed cell at the negative edge of the clock cycle as shown in the timing diagram (Fig. 4.2(a)). This enables the RBL to discharge quickly towards '0' leading to the flow of read current (I_{ON}) when DB stores '1' value. The signals WL_Y1 and WL_Y2 are held high to activate the ST action and prevent the internal node voltages to flip during read operation thereby improving the read stability. The sense amplifier enable signal (SAE) is activated at the end of the read cycle to complete the read operation. The RGND signal, being row-based, is kept low in un-accessed cells along the column. The use of fully-gated ground scheme reduces read-port leakage (I_{OFF}) in such cells and improves I_{ON}/I_{OFF} ratio significantly.

Hold mode

During hold mode, any changes in the voltage at internal nodes due to PVT-variations is counteracted by the ST action of transistors MFL/MFR and the stacking effect of pull-down transistors (MDL-MDL2, MDR-MDR2) thereby improving the robustness of Proposed cell IV in sub-threshold region.

(a)

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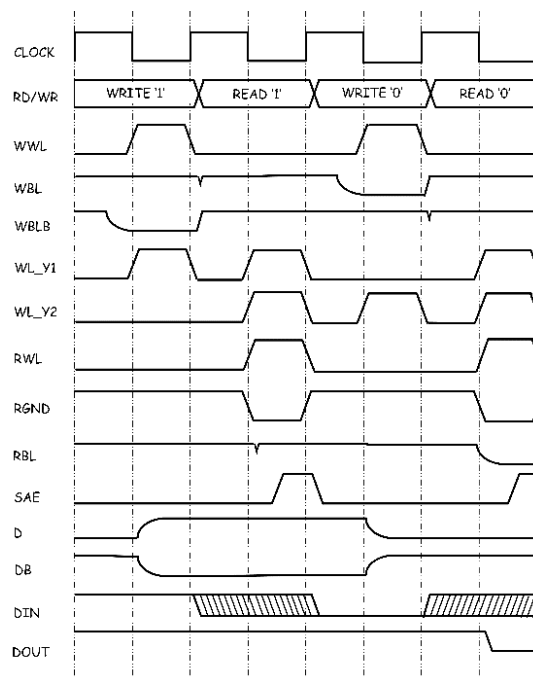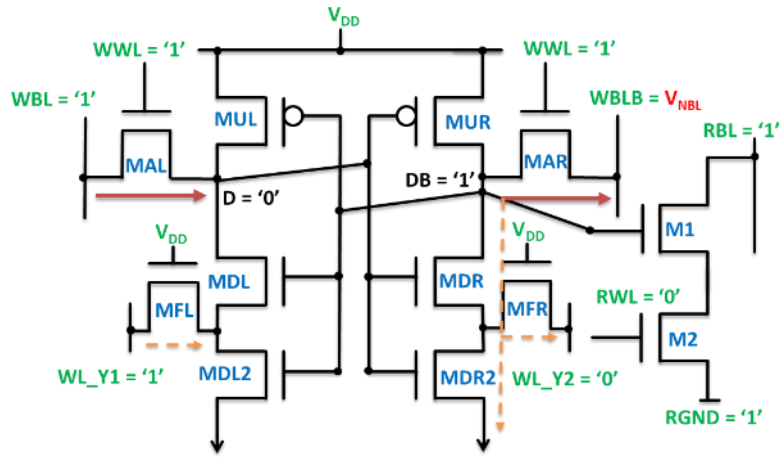
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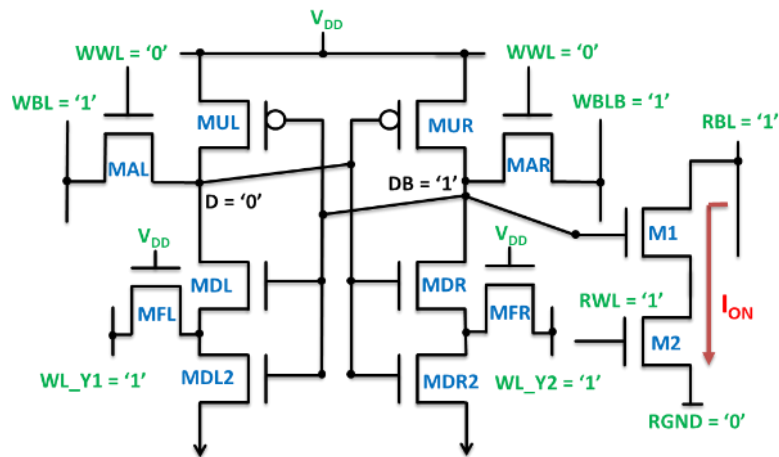
(c)

Fig. 4.2 Proposed cell IV (a) Timing diagram (b) Write operation (c) Read operation

4.3.1.2 Simulation results

In this section, the performance of the Proposed cell IV is compared with the existing cells through the SPICE simulations using 32 nm bulk CMOS PTM model parameters. The typical threshold voltages for nMOS and pMOS transistors are 0.501 V and -0.452 V respectively. The transistor sizing for all cells is mentioned in Table 4.1. The simulation results of the cells at typical corner and 27 ˚C for different supply voltages are evaluated in write, read and hold modes. The results pertaining to various SRAM metrics during write,

read and hold modes are discussed individually in the subsections. The sensitivity of cell performance with PVT-variations [107] is evaluated in terms of failure probabilities and subsequent estimation of minimum supply voltage in each operating mode is also carried out.

Table 4.1: Aspect ratio of transistors

SRAM Cells	Transistors ($\lambda = 18$ nm)							
	MUL/ MUR	MDL/ MDR	MDL2/ MDR2	MAL/ MAR	MAL2/ MAR2	MFL/ MFR	MUL2/ MDL3	M1/ M2
8T_conv[4]	$4\lambda/2\lambda$	$4\lambda/2\lambda$	-	$4\lambda/2\lambda$	-	-	-	$4\lambda/2\lambda$
10T_st1[53]	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	-	$4\lambda/2\lambda$	-	-
10T_st2[107]	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	-	$4\lambda/2\lambda$	-	-
11T_say[59]	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$ /-	-	$4\lambda/2\lambda$	-	$4\lambda/2\lambda$
12T_ash[61]	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	-	$4\lambda/2\lambda$	$4\lambda/2\lambda$	-
12T_vish[60]	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	-	-	$4\lambda/2\lambda$
PROPOSED CELL IV	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	$4\lambda/2\lambda$	-	$4\lambda/2\lambda$	-	$4\lambda/2\lambda$

Process-variation tolerance :

The proposed SRAM cell incorporates ST inverter as depicted in Fig. 4.3(a). The VTC of the proposed and 8T_conv [4] cells at TT, FS and SF corners and 0.3 V are shown in Fig. 4.3(b) and Fig. 4.3(c) respectively. A reduced variation of 34.9 % (from 274 mV to 178.2 mV) in the switching threshold voltage is observed for proposed cell in comparison to 8T_conv [4] cell. It clearly thus indicates that the proposed cell offers better tolerance to PVT-variations in comparison to 8T_conv [4] cell.
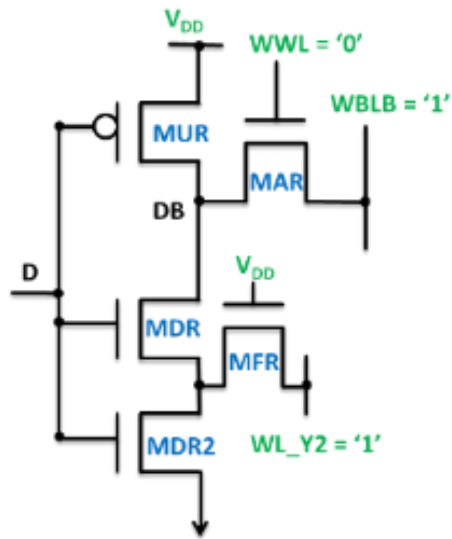
(a)
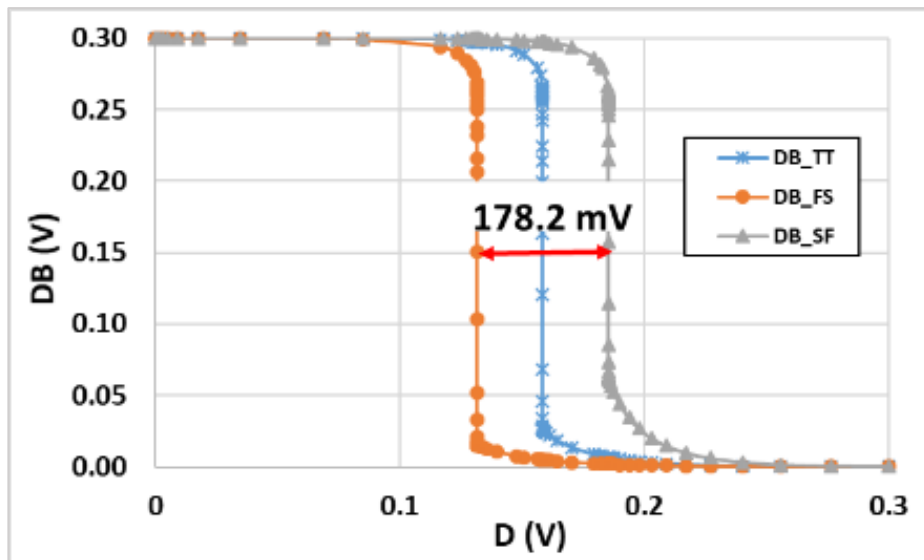
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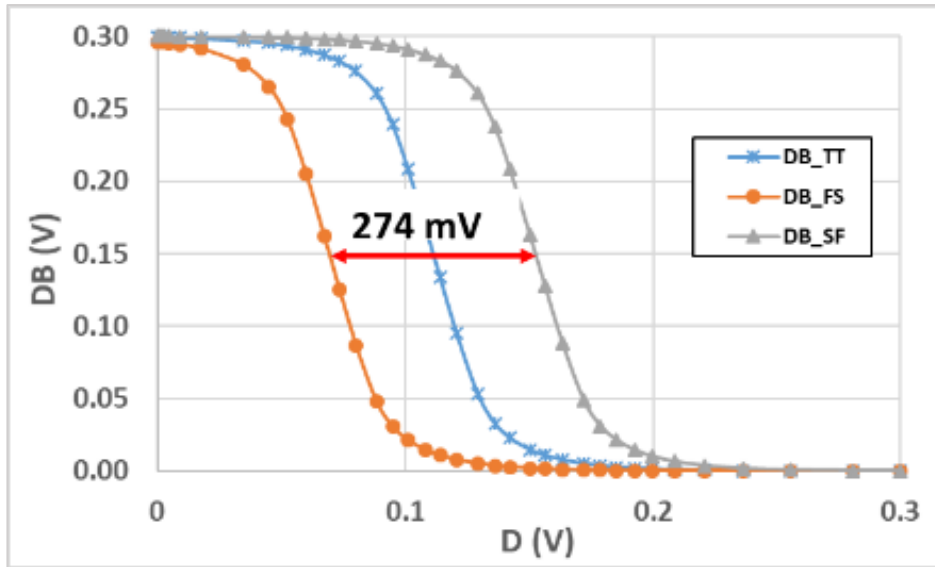
(c)

Fig 4.3 (a) Schematic of ST inverter (b) VTC of Proposed cell IV (c) VTC of 8T_conv cell [4]

Write mode

The comparison of write performance amongst various SRAM cells is done in terms of WM (for measuring write ability), T_{WRITE_ACCESS} and P_{WRITE}.

WM

The WM of the SRAM cells are plotted in Fig. 4.4(a) at different supply voltages. The proposed cell shows 173 %, 211 %, 130 %, 97 %, 91 % and 39 % higher WM compared to 8T_conv [4], 11T_say [59], 10T_st1 [53], 10T_st2 [107], 12T_ash [61] and 12T_vish [60] respectively at 0.3 V. The auxiliary leakage path provided by the feedback transistor, the increased discharging current through the access transistor due to NBL write-assist technique at node storing '1' coupled with the increased threshold voltage of the pull-down transistor storing '0' due to ST action expedites the writing process in the proposed cell compared to other cells. The proposed cell has worst-case WM of 180 mV at 0.3 V under 6σ global process and 1σ local mismatch variations (1000 points) as shown in Fig. 4.4(b).
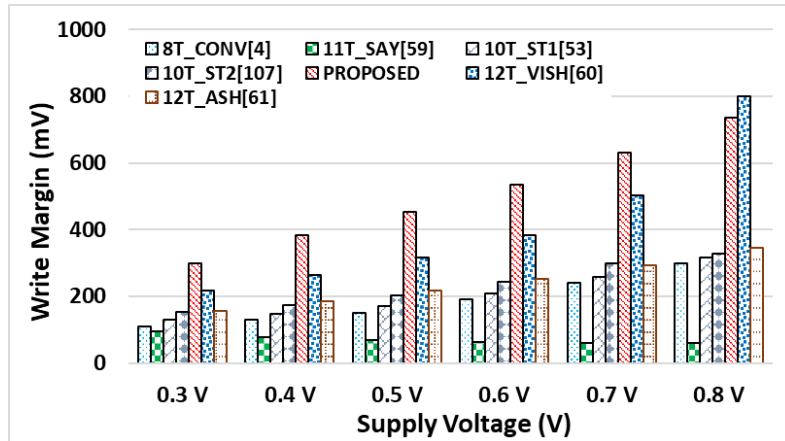
(a)
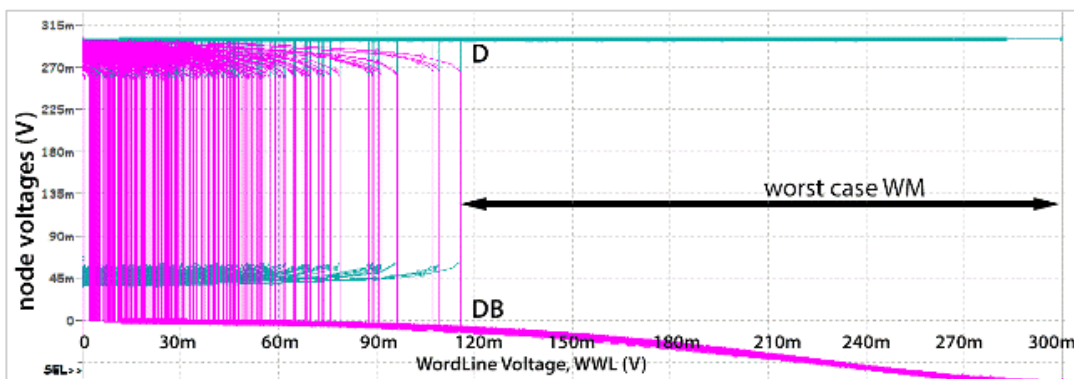
(b)
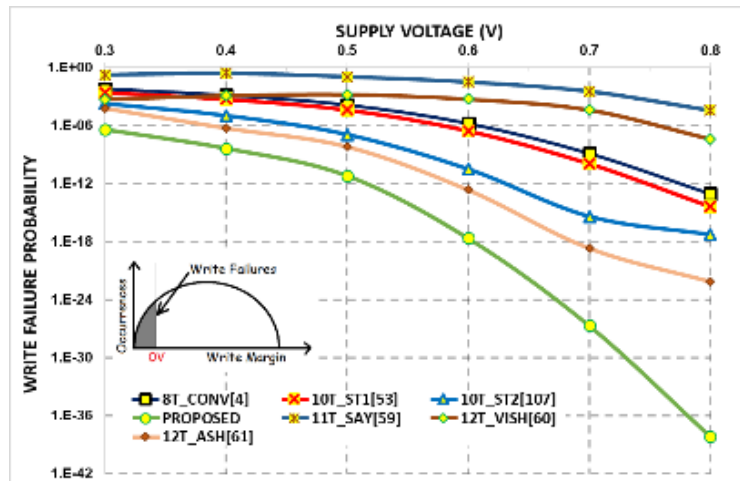
(c)

Fig. 4.4 WM (a) Effect of supply voltage on WM (27 ℃, TT corner) (b) Worst-case WM

for the Proposed cell IV under 6σ global process and 1σ local mismatch variations (1000

points) (c) Effect of PVT-variations on WM in terms of write failure probability

Write failure probability

The WM varies in the presence of PVT-variations due to the changes in the threshold voltage of the transistors. The SRAM cell designed for high WM may fail to accomplish a successful write operation at low supply voltages due to PVT-variations. To estimate the worst-case write ability of the cell under such conditions requires millions of Monte Carlo simulations, which are computationally extensive. So, an alternate method to evaluate the performance of the cell is mentioned in [107], which helps to estimate the failure probability of the SRAM cell under PVT-variations using only few runs. The 6σ probability at which the WM reduces to 0 mV is 1E-9 and the corresponding supply voltage is known as the write V_{min} [59][107]. In this method, the threshold voltage of each transistor is changed one by one and then the WM is estimated for each change. The mean value and the standard deviation denoted as WMmean and WMsd is calculated over all values. The formula to calculate the write failure probability, P_{WFP}, of the cell is:

$$P_{WFP} = \int_{-\infty}^{-(WMmean/WMsd)} \frac{1}{\sqrt{2\pi}} e^{\left(\frac{-y^2}{2}\right)} dy \quad …………………… \quad (1)$$

The plot of write failure probability at different supply voltages is shown in Fig. 7(c) and the corresponding value of write V_{min} is tabulated in Table 4.2. The plot shows that the use of novel combination of NBL technique and ST action in proposed cell works well at all supply voltages and results in lower values of failure probabilities. This in turn translates into a least write V_{min} of 425 mV for the proposed cell.

T~WRITE_ACCESS~

The plots in Fig. 4.5(a) and Fig. 4.5(b) show the T~WRITE_ACCESS~ ('1') and T~WRITE_ACCESS~ ('0') at typical-best-worst process corners respectively. The Proposed cell IV reduces the T~WRITE_ACCESS~ ('1') by 84 %, 88 %, 85 %, 94 % and 93 % over 8T_conv[4], 10T_st1[53],

10T_st2[107], 12T_ash[61] and 12T_vish[60] SRAM cells respectively at a supply voltage of 0.3 V and SF corner. At FS corner, the percentage reduction is 75 %, 81 %, 78 %, 90 %, 81 % and 94 % lesser compared to 8T_conv [4], 10T_st1[53], 10T_st2[107], 12T_ash [61], 12T_vish [60] and 11T_say [59] respectively at the same supply voltage. During write '0' operation, the time required for proposed SRAM cell is 94 %, 95 %, 95 %, 89 %, 98 % and 99 % lesser in comparison to 8T_conv [4], 10T_st1[53], 10T_st2[107], 12T_ash [61], 12T_vish [60] and 11T_say [59] respectively at a supply voltage of 0.3 V and SF corner. Similarly, compared to the same SRAM cells, the time taken at FS corner is 90 %, 92 %, 92 %, 91 %, 96 % and 92 % lesser under similar operating conditions validating the improved write performance of the proposed cell irrespective of process corner and supply voltage. It is worth noting that the 11T_say [59] SRAM cell, which performs single-ended write operation suffers from degraded T_{WRITE_ACCESS} ('1') specifically at SF corner and thus fails to write '1' into the cell over the entire supply voltage range. For the cells, with differential write operation, SF corner and FS corner are the best and worst corners respectively during write '1' operation. Alternatively, for write '0' operation FS corner is the best corner while the performance degrades at SF corner corroborating the fact that, for write '0' operation, SF corner is the worst corner for all.
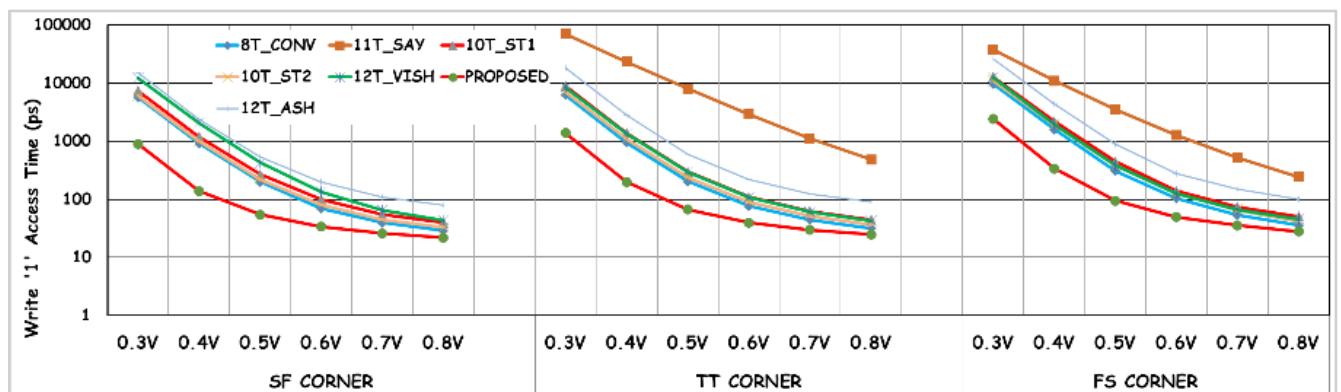
(a)
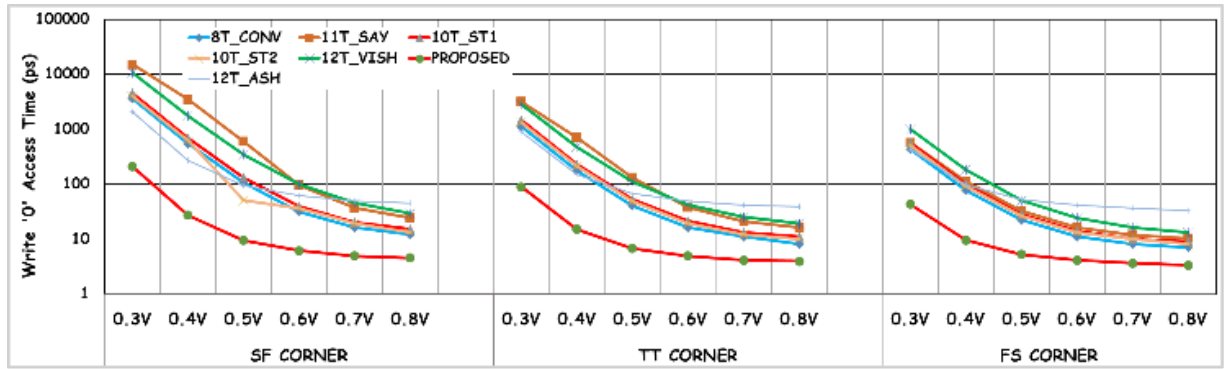
(b)

Fig. 4.5 T_{WRITE_ACCESS} T_{WRITE_ACCESS} *(a)* T_{WRITE_ACCESS} *('1') (b)* T_{WRITE_ACCESS} *('0') at different supply voltages and corners*

P_{WRITE}

The power consumed during write '1' and '0' operations are plotted in Fig. 4.6 at different supply voltages. It is clear from the graphs that 11T_say [59] consumes least power among all the SRAM cells due to the use of single ended write operation.
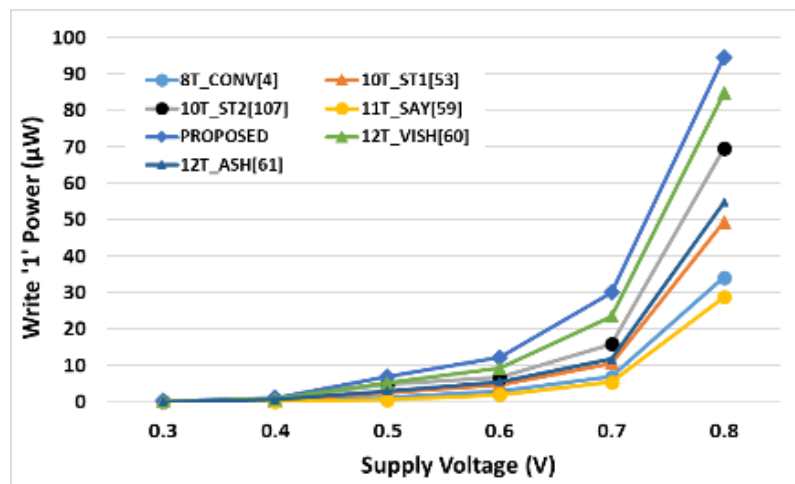
(a)
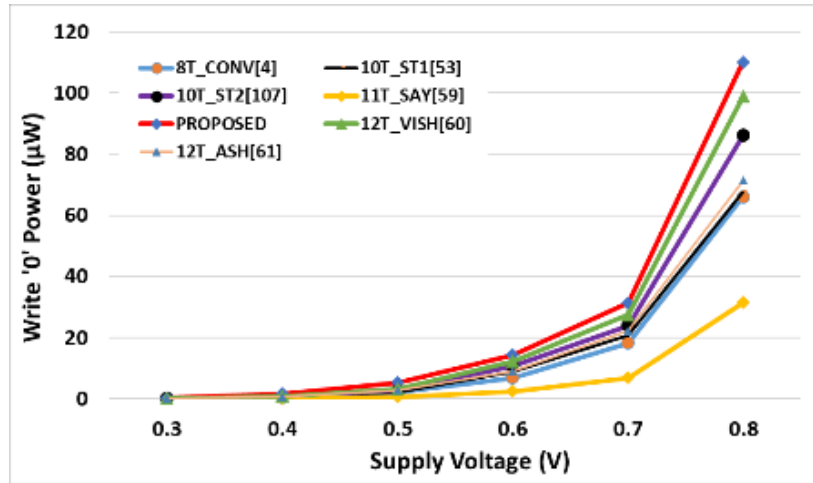
(b)

Fig. 4.6 P_{WRITE} (a) P_{WRITE} ('1') (b) P_{WRITE} ('0') at different supply voltages (27 ˚C, TT corner)

Read mode

In the read mode, the performance parameters namely, RSNM, read failure probability, read V_{min}, I_{ON}/I_{OFF} ratio, T_{READ_ACCESS} and P_{READ} are evaluated.

RSNM

The RSNM of the cells is measured and the values are plotted in Fig. 4.7(a) for different supply voltages. The proposed cell with isolated read port achieves 47 %, 41 % and 29 % higher RSNM values at a supply voltage of 0.3 V over 12T_ash [61], 10T_st1 [53] and 10T_st2 [107] SRAM cells respectively. The same trend is seen at higher voltages. The 10T_st1 [53] and 12T_ash [61] show poor performance due to the flow of read current through internal storage nodes during read mode whereas in 10T_st2 [107] the presence of additional leakage paths lowers the stability of stored data. The proposed cell has worst-case RSNM of 31.3 mV at 0.3 V under 6σ global process and 1σ local mismatch variations (1000 points) as shown in Fig. 4.7(b).
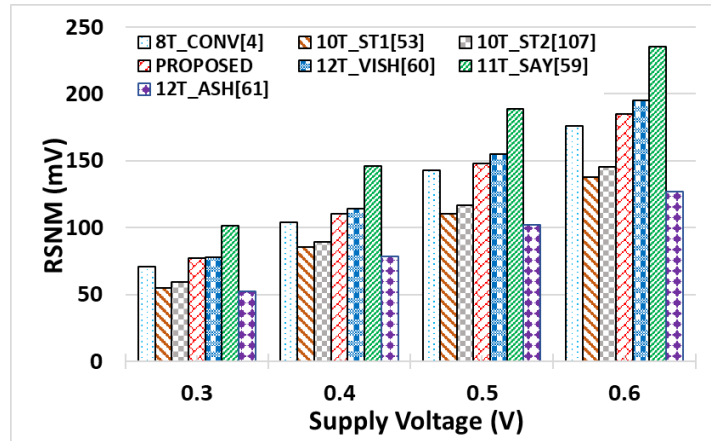
(a)
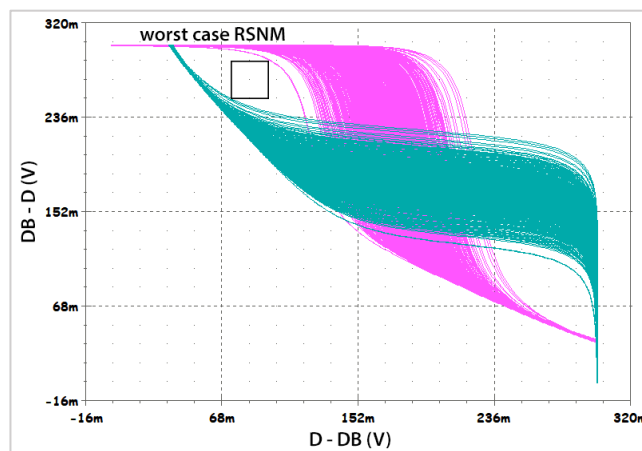
(b)
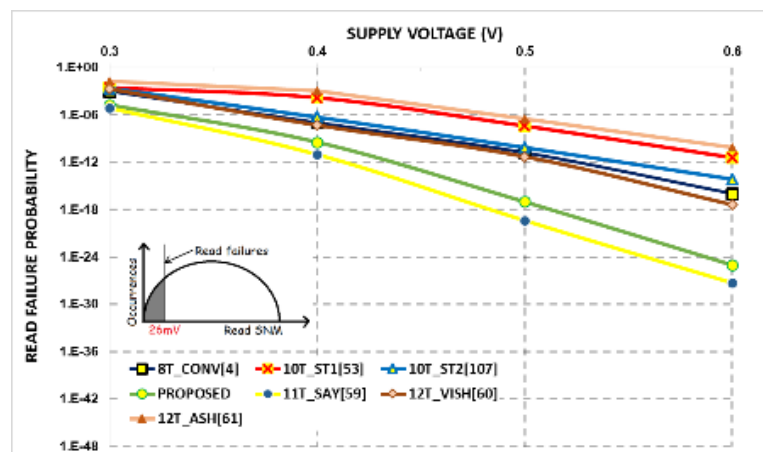
(c)

Fig. 4.7 RSNM (a) Effect of supply voltage on RSNM (27 ˚C, TT corner) (b) Worst-case

RSNM for the Proposed cell IV under 6σ global process and 1σ local mismatch variations

(1000 points) (c) Effect of PVT-variations on RSNM in terms of read failure probability

Read failure probability

The effect of PVT-variations on RSNM is calculated using a more efficient and cost-effective method mentioned in [107] instead of Monte Carlo simulations. The 6σ probability at which the RSNM reduces to 26 mV is 1E-9 and the corresponding supply voltage is known as the read V_{min} [59][107]. The formula to calculate the read failure probability, P_{RFP}, is

$$P_{RFP} = \int_{-\infty}^{-(RSNMmean/RSNMsd)} \frac{1}{\sqrt{2\pi}} e^{\left(\frac{-y^2}{2}\right)} dy \quad .... (2)$$

where RSNMmean and RSNMsd are the mean and standard deviation of all the RSNM values calculated by changing threshold voltage of each transistor one by one.

Fig. 4.7(c) shows the plot of read failure probability at different supply voltages. As can be seen, the proposed cell has lower read failure probabilities than 10T_st1 [53], 10T_st2 [107], 12T_ash [61], 12T_vish [60] and 8T_conv [4] SRAM cells. All this is attributed to the presence of data-independent ST action in latch and use of isolated read port that help retain node voltages even in the presence of PVT-variations in proposed cell resulting in lower failure probabilities. The lower read failure probability in turn translates into lower read V_{min} of 390 mV in proposed cell.

I_{ON}/I_{OFF} ratio

The effect of varying supply voltages and temperatures on I_{ON}/I_{OFF} ratio for the proposed and 8T_conv [4] SRAM cells is captured in Fig. 4.8. This ratio degrades significantly in 8T_conv [4] cell due to increased read port leakage especially in sub-threshold region [18]. The proposed cell provides an improvement of 48 %, 37 % and 27 % at -40 ˚C, 27 ˚C and 125 ˚C respectively over 8T_conv [4] SRAM cell at a supply voltage of 0.3 V. A similar trend is observed at higher voltages.

138
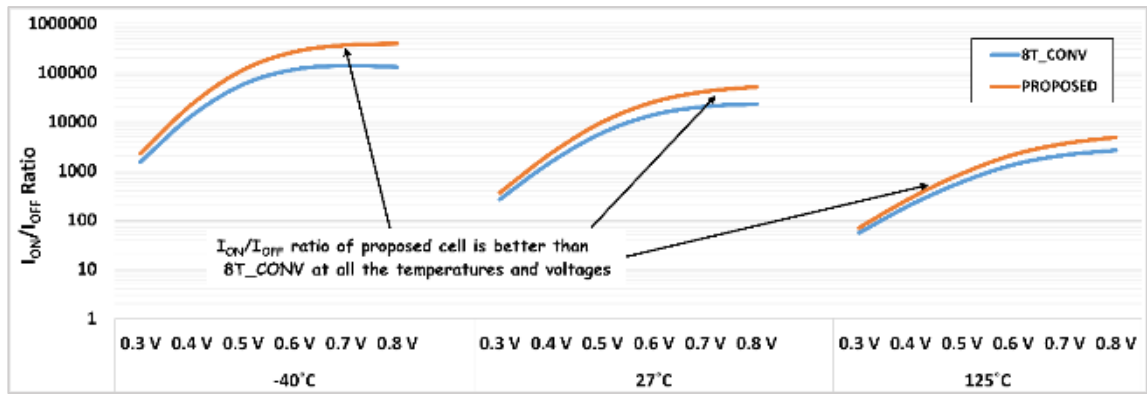
Fig. 4.8 Effect of supply voltage and temperature on I_{ON}/I_{OFF} ratio for Proposed cell IV and 8T_conv [4] SRAM cells

A plot of I_{ON}/I_{OFF} ratio, for the other SRAM cells is depicted in Fig. 4.9. The proposed cell attains nearly 114 %, 169 %, 37 %, 82 % and 38% improvement in the performance parameter compared to 10T_st1 [53], 10T_st2 [107], 11T_say [59], 12T_ash [61] and 12T_vish [60] cells at 0.3 V. The proposed cell shows similar performance at higher voltages thereby increasing the scope for creating larger SRAM arrays.
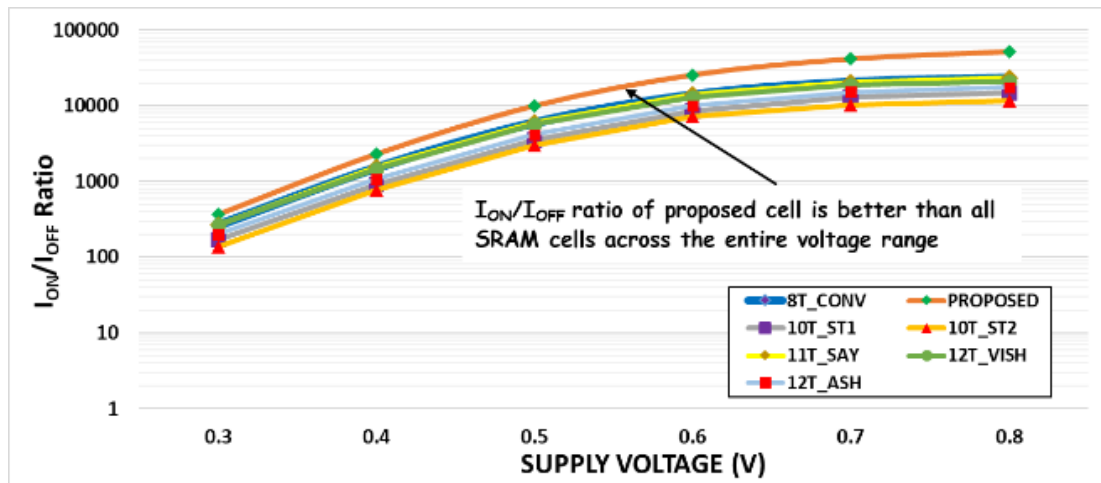
Fig. 4.9 I_{ON}/I_{OFF} ratio at different supply voltages (27 ˚C, TT corner)

T_{READ_ACCESS}

The T_{READ_ACCESS} values are plotted in Fig. 4.10 for all the SRAM cells. The results shows that the proposed cell takes 36 %, 86 %, 83 %, 36 %, 12 % and 3 % lesser T_{READ_ACCESS} at supply voltage of 0.3 V compared to 12T_ash [61], 8T_conv [4], 11T_say [59], 10T_st1 [53], 10T_st2 [107] and 12T_vish [60] SRAM cells respectively. A significant improvement is also seen at higher voltages.
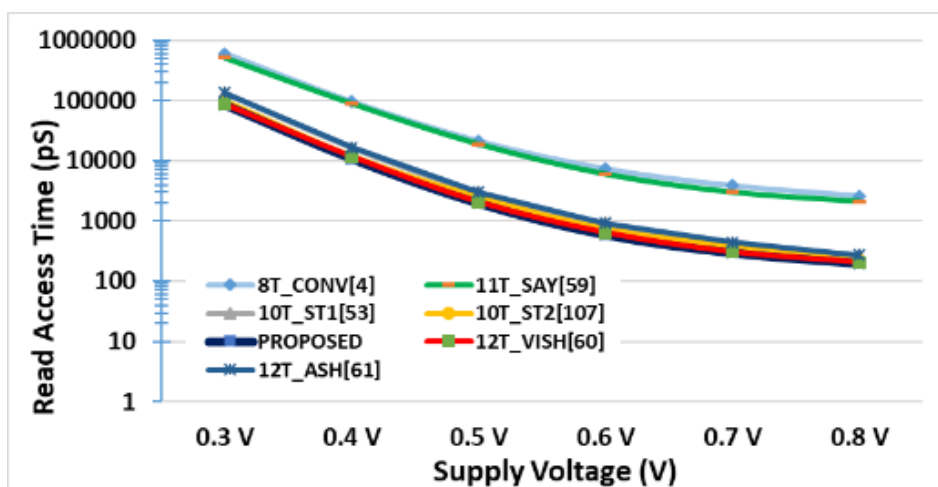
Fig. 4.10 T_{READ_ACCESS} at different supply voltages (27 ˚C, TT corner)

P_{READ}

The power consumed by each cell during read mode is plotted in Fig. 4.11 at different supply voltages. The results show that the proposed cell consumes 9 % and 6 % lesser power compared to 12T_vish [60] and 10T_st2 [107] SRAM cells at 0.3 V respectively. At a supply voltage of 0.8 V, the power consumed is 25 % and 17 % lesser compared to the same cells. This is due to high capacitive bitline load of these cells as mentioned in Section 2. It is also noted that the SRAM cells, 8T_conv [4] and 11T_say [59], consume lesser power due to the use of single ended sensing in these cells.

140
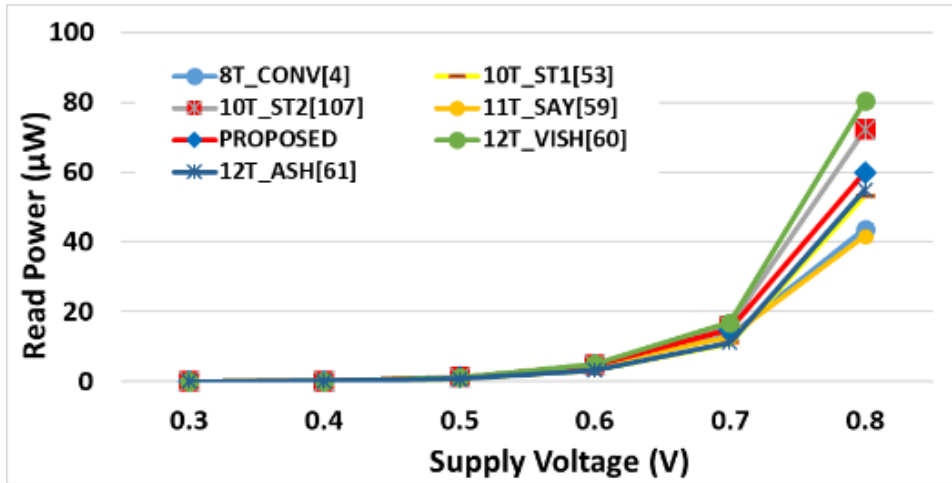
Fig. 4.11 P$_{READ}$ at different supply voltages (27 °C, TT corner)

Hold mode

The performance of the cell in the hold mode is compared on the basis of HSNM, hold failure probability, hold V$_{min}$ and P$_{LEAK}$.

HSNM

The HSNM for different SRAM cells is plotted in Fig. 4.12(a) at different supply voltages. The proposed cell offers about 6 %, 25 %, 13 % and 45 % higher HSNM values at 0.3 V compared to 12T_ash [61], 8T_conv [4], 12T_vish [60] and 10T_st2 [107] SRAM cells respectively.
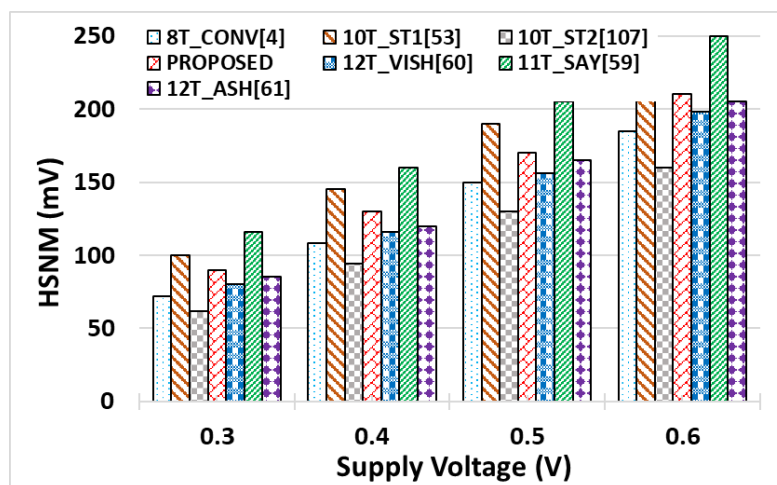
(a)
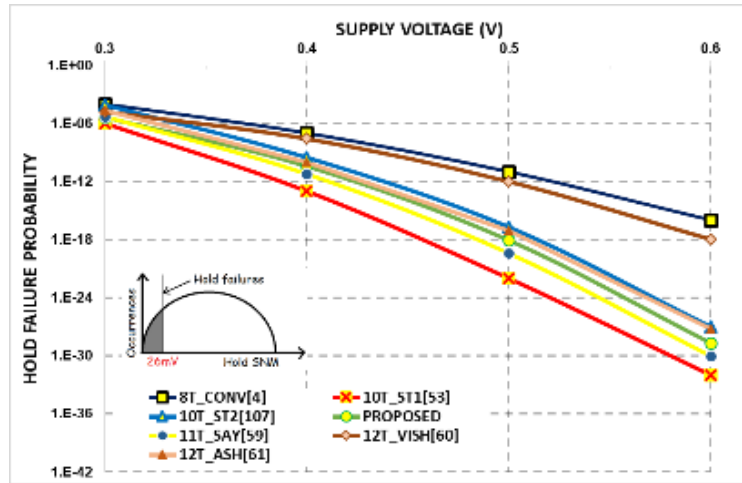
(b)

Fig. 4.12 HSNM (a) Effect of supply voltage on HSNM (27 ˚C, TT corner) (b) Effect of PVT-variations on HSNM in terms of hold failure probability

Hold failure probability

The HSNM varies with the change in the threshold voltage of the transistors due to PVT-variations [127]. The 6σ probability at which the HSNM goes below 26 mV is 1E-9 and the corresponding supply voltage is known as the hold V_{min} [59][107]. The formula to calculate the hold failure probability, P_{HFP}, is

$$P_{HFP} = \int_{-\infty}^{-(HSNMmean/HSNMsd)} \frac{1}{\sqrt{2\pi}} e^{\left(\frac{-y^2}{2}\right)} dy \; ... \, ... \, ... \, ... \, ... \, ... \, ... \, ... \, ... \; (3)$$

where HSNMmean is the mean value and HSNMsd is the standard deviation of all the HSNM values calculated for all the transistors of the cell by changing their threshold voltages one by one. The hold failure probability for all the SRAM cells at different supply voltages is plotted in Fig. 4.12(b). The SRAM cells with lesser leakages and stronger ST action have lower hold failure probabilities and hence low hold V_{min}. It is worth mentioning that the proposed cell has lower hold failure probabilities than 10T_st2 [107], 12T_vish [60], 12T_ash [61] and 8T_conv [4] SRAM cells and achieves a hold V_{min} of 372 mV.

142

The total leakage power consumed by the SRAM cells is plotted in Fig. 4.13 at different supply voltages. The stacking effect lowers the leakage current [107] [113]. Consequently, the ST SRAM cells employing stack of pull-down transistors in latch structure or 12_vish [60] SRAM cell having stack of two access transistors consume lesser leakage power. The presence of multiple leakage paths in 10T_st2 [107] and 12T_vish [60] SRAM cells add to the power consumption. The high read port leakages, such as in 8T_conv [4] and 11T_say [59] SRAM cells, increase the power consumption during hold mode. The SRAM cell with a greater number of bitlines also suffers from higher leakages. The proposed cell consumes approximately 31 % and 22 % lesser leakage power compared to 8T_conv [4] cell at 0.3 V and 0.8 V respectively.
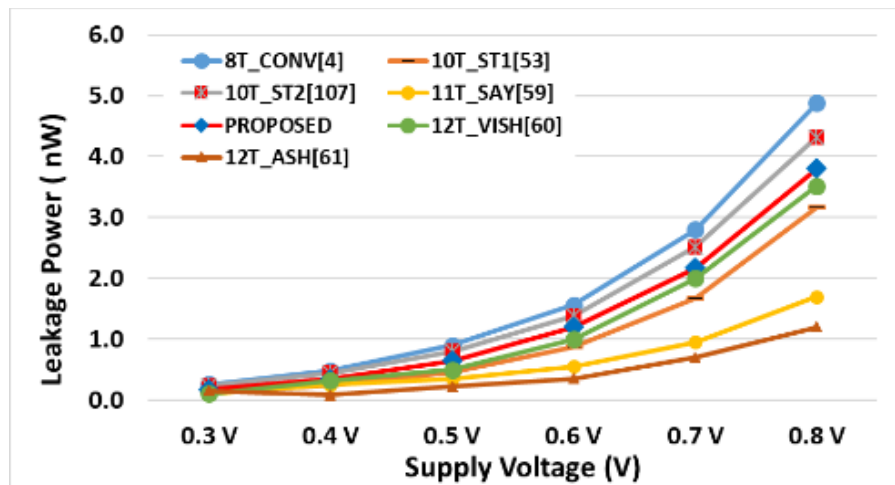
Fig. 4.13 P_LEAK at different supply voltages (27 ˚C, TT corner)

Comparative analysis

The performance of the existing cells (discussed in section 4.2) and proposed cell at V_{DD} = 0.3 V, T = 27 ˚C, TT corner for each operating mode is summarized in Table 4.2. The best performance for each parameter is highlighted with bold font. It can be noted that it is

extremely difficult to maintain good performance in all the three operating modes in existing cells specifically in sub-threshold region due to the trade-off among performance parameters. The proposed cell overcomes the trade-off by employing the modified ST action along with use of negative bitline and fully-gated ground scheme. It can be observed that the proposed cell provides the best write ability (in terms of write margin), write access times, write V_{min}, read access time and I_{ON}/I_{OFF} ratio. The proposed cell achieves the lowest overall V_{min} of 425 mV, the least among all the cells considered for comparison, thus, enabling the proposed cell to perform memory operations successfully in sub-threshold region under PVT-variations.

Table 4.2: Performance comparison at V_{DD} = 0.3 V and T = 27 ˚C

	Parameters	8T_conv	10T_st1	10T_st2	11T_say	12T_vish	12T_ash	PROPOSED CELL IV
Write	**WM(mV)**	110	131	152	97	216	157	**245**
mode	T_{WRITE_ACCESS} **('1') (ps)**	5570	7660	6460	45400	10480	18200	**1350**
	T_{WRITE_ACCESS} **('0') (ps)**	1105	1450	1320	3125	2800	842	**123**
	P_{WRITE} **('1') (µW)**	0.07	0.08	0.13	**0.05**	0.17	0.10	0.25
	P_{WRITE} **('0') (µW)**	0.09	0.10	0.13	**0.07**	0.16	0.11	0.26
	Write Vmin (mV)	712	680	556	970	850	518	**425**
Read	**RSNM (mV)**	70.5	54.7	59.5	**101.4**	78	52.5	77
mode	T_{READ_ACCESS} **(ps)**	601908	134342	98000	520000	89000	135691	**86000**
	I_{ON}/I_{OFF} **ratio**	267	171	136	298	310	201	**366**
	P_{READ} **(µW)**	0.017	**0.013**	0.02	0.016	0.021	0.014	0.022
	Read Vmin (mV)	455	540	470	**373**	445	563	390
Hold	**HSNM (mV)**	72	100	62	**116**	80	85	90
mode	P_{LEAK} **(µW)**	0.258	0.126	0.253	**0.096**	0.241	0.177	0.237
	Hold Vmin (mV)	450	**345**	390	367	430	378	372
Overall Vmin	**Vmin (mV)**	712	680	556	970	850	563	**425**

Bold values indicate the best value of each parameter

4.4 Conclusions

In this chapter, a PVT-variation tolerant ST based Proposed cell IV is presented. The proposed cell removes the bottleneck associated with write ability in sub-threshold region by using a novel combination of NBL technique and modified ST action. The auxiliary leakage path provided by the feedback transistor, the increased discharging current due to NBL write-assist technique at node storing '1' coupled with the increased threshold voltage of the pull down transistor storing '0' due to ST action expedites the writing process in the proposed cell. This in turn manifests itself into higher WMs, lower write failure probabilities and least write V_{min} of 425 mV. The proposed cell takes up to 94 % and 99 % lesser T_{WRITE_ACCESS} ('1') and T_{WRITE_ACCESS} ('0') compared to other SRAM cells at 0.3 V. The data-independent ST action significantly reduces the sensitivity of the cell towards PVT-variations in both read and hold modes. It shows up to 41 % higher RSNM values and exhibits lower read failure probabilities, which in turn translates into read V_{min} of 390 mV. It shows up to 45 % higher HSNM and a hold V_{min} of 372 mV. Additionally, fully-gated ground scheme reduces read port leakages resulting in an improvement of up to 169 % in I_{ON}/I_{OFF} ratio. The differential sensing leads to up to 86 % reduction in T_{READ_ACCESS}. Additionally, about 31 % reduction in P_{LEAK} is also observed at 0.3 V. The overall V_{min} of proposed cell is observed to be 425 mV at 32 nm making it suitable for sub-threshold operation where the impact of PVT-variations is immense on the performance of the other SRAM cells.

CHAPTER 5

SRAM CELL DESIGN WITH IMPROVED TRANSISTOR TECHNOLOGY

The content and results of the following paper has been reported in this chapter

Gupta M, Gupta K, Pandey N, "**A 22nm 10T FinFET SRAM Cell with Improved Read and Write performance in Sub-Threshold Region**", 8*th International Conference on Signal Processing and Integrated Networks (SPIN)*, IEEE, pp. 452-457, 2021.

5.1   Introduction

The CMOS based SRAM cell designs discussed in previous chapters can work well above 28 nm technology node. However, maintaining the performance under 28 nm is becoming difficult with bulk CMOS transistors [126]. The FinFETs are emerging as the most promising substitute for planar CMOS technology due to good scaling ability, high ON current, reduced V_{th} variations, better sub-threshold slope and SCE [125][127]. Various FinFET based SRAM cell designs that work under 28 nm technology node are available in literature [133][134]. However, these SRAM cells suffer due to the trade-off among performance parameters.

In this chapter, the existing FinFET based SRAM cells are reviewed in section 5.2. The Proposed cell V that addresses the issues of existing FinFET based SRAM cells is presented in section 5.3. The functionality of the proposed design is verified and its performance is compared with the existing FinFET and some most recent CMOS based cells. The conclusions are drawn in section 5.4.

5.2 Existing FinFET based SRAM cell designs

The FinFET based SRAM cells provide better ON current and reduced V_{th} variations compared to their CMOS counterparts. However, for these cells to perform all memory operations appropriate read and write assist techniques or improved SRAM cell topologies are required. Some recent FinFET based SRAM cell designs available in literature are discussed next. The design in [133] performs differential read and write operations using a common set of complementary bitlines. Due to the connection of two transistors per SRAM cell on each bitline it suffers from increased bitline load capacitance degrading the access times and increasing the power consumption. In addition, the presence of multiple leakage paths reduces the stability of stored data during hold mode. The other FinFET based design in [134] uses single bitline for performing read and write operations to reduce the overall

power consumption. For further reduction in power requirements, it does not pre-charge the bitline prior to performing the read operation rather the accessed cell charges the bitline to V_{DD} when the stored data is '1'. However, it suffers from many drawbacks. First, the connection of two transistors per SRAM cell to bitline increases the bitline loading capacitance. Second, the SRAM cell constructed using minimum-sized transistors is unable to charge the large bitline load capacitance to V_{DD} effectively during read '1' operation. In addition, due to the flow of current through the intermediate nodes, the cell becomes prone to destructive read operation especially in sub-threshold region. This necessitates a new FinFET based SRAM cell design that can address these issues to provide improved read and write performance in sub-threshold region.

5.3 Design of SRAM with improved transistor technology

To address the performance issues of existing CMOS and FinFET based SRAM cells, such as reduced stability of stored data, increased bitline load capacitance with longer discharge time and increased leakages, a Proposed cell V is presented next.

5.3.1 Proposed cell V

The schematic of the Proposed cell V is presented in Fig. 5.1(a). It performs single-ended read and write operations. The structure of proposed cell comprises of basic latch structure (MUL-MDL and MUR-MDR) to store one bit of information in a complementary way at its internal storage nodes D and DB. It performs write operation using access transistor MAL, wordline signal WWL and corresponding bitline WBL. A write assist transistor MDL2, driven by complementary signal WWLB, is incorporated in the latch structure to assist the write operation. An isolated read port (M1, M2, and M3) is used to accomplish the read operation using wordline signal RWL along with the bitline RBL. A transistor M4 is introduced to enhance the read performance of the cell.

(a)
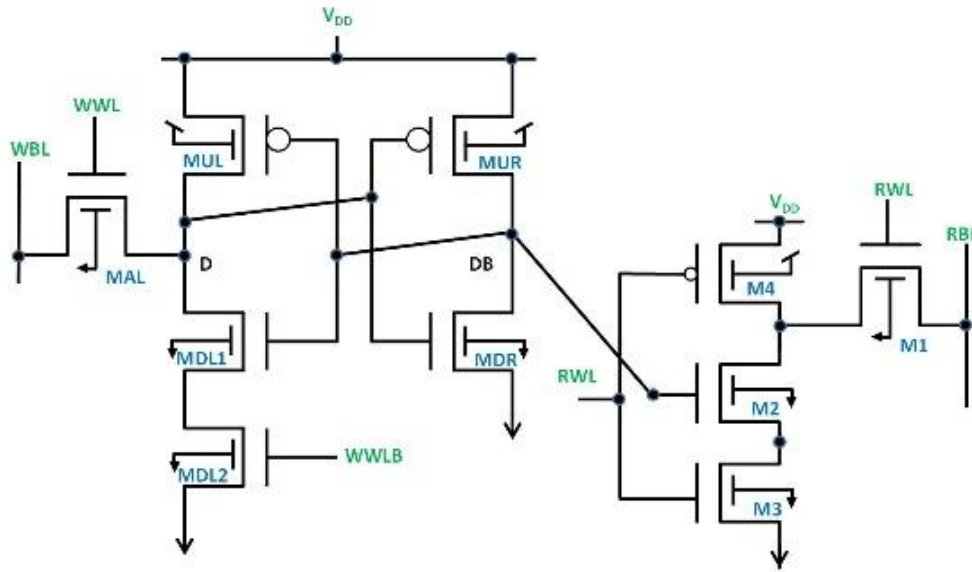
Mode / Control signal	Read	Write	Hold
WWL	0	1	0
WWLB	1	0	1
RWL	1	0	0

(b)

Fig. 5.1 Proposed cell V (a) Schematic (b) Operating conditions

5.3.1.1 Operation

The Proposed cell V can be operated in three different operating modes: write, read and hold as per the operating conditions mentioned in Fig. 5.1(b).

Write mode

During write operation, the new value is applied on WBL through the write driver. The complementary signals WWL and WWLB are then pulled high and low respectively in the accessed cell. To improve the write performance, a write assist transistor (MDL2) driven

by control signal WWLB turns OFF and disables the path between storage node D and GND. This helps the node voltages to flip quickly during write operation without disrupting the strong feedback mechanism of the latch structure. The advantage is that the write performance of the accessed cell is improved without causing the stability issues in the other cells connected to the same column.

Read mode

At the beginning, RBL is pre-charged using pre-charge circuit to V_{DD} and then RWL signal is turned high in the accessed cell along the row. Now, if DB holds '1' then RBL voltage reduces or it remains high otherwise. The change in RBL voltage is further used for sensing the stored data and complete the operation. Usually, the RBL leakage current that flows through the isolated read port of an un-accessed cell (having RWL low) is data-dependent. Due to this, the RBL voltage discharges even when the accessed cell holds '0' at DB resulting in reduced ΔV_{RBL} and wrong sensing of stored data. To get over this problem, a transistor M4 is incorporated in the cell. The transistor M4 turns ON in the un-accessed cells and maintains a voltage close to V_{DD} at drain of M4 irrespective of the value stored at DB. This reduces the drain to source voltage across M1. The result is significant reduction in RBL leakage current independent of stored data. Thus, achieving low and data-independent RBL leakages and improved ΔV_{RBL}. The high read current of FinFET based cell provides significant improvement in T_{READ_ACCESS} in sub-threshold region

Hold mode

Both the wordline signals (RWL and WWL) are kept low while WWLB is held high during this mode. This isolates the internal storage nodes from the WBL and RBL. The write assist transistor MDL2 conducts and connects the pull-down transistor MDL1 to GND. In

addition, the stacking effect of two pull-down transistors (MDL1 and MDL2) decreases the leakages resulting in high stability of stored data [76].

5.3.1.2 Simulation results

The performance of the Proposed cell V is evaluated and compared with 8T_conv[4], 10T_cal[51], 10T_sh[57] and 7T_EN[134] SRAM cells based on standard cell metrics in different operating modes. All the SPICE simulations are performed using 22 nm FinFET and bulk CMOS PTM model parameters as mentioned in Table 5.1.

Table 5.1: FinFET and CMOS parameters

FinFET parameters		CMOS parameters	
name	**value**	**name**	**value**
Gate length	22 nm	**Length of channel**	22 nm
Oxide thickness	1.1 nm	**Channel width**	44 nm
Fin thickness	15 nm	**Threshold voltage nMOS, V_{thn}**	0.68858 V
Fin height	28 nm	**Threshold voltage pMOS, V_{thp}**	-0.63745 V
Source/drain doping	3e26 cm^{-3}		
SS	75 mV/decade		
DIBL	59 mV/V		

Write mode

The key parameters such as write ability and T_{WRITE_ACCESS} are evaluated for comparison. The write ability is measured in terms of WM.

WM

The WM is measured (Fig. 5.2(a)) and the corresponding values are displayed in Fig. 5.2(b) and Fig. 5.2(c) for WM ('1') and ('0') respectively at different voltages. As can be seen,

151

the proposed cell provides reasonable values of WM ('1') at all voltages. The improvement achieved in WM ('1') is 299 %, 123 % and 322 % compared to 8T_conv, 10T_sh and 10T_cal cells respectively at 0.3 V. The proposed cell also provides improvement in WM ('0') (Fig. 5.2(c)) at higher voltages whereas the performance remains comparable to other cells at lower voltages. It is worth mentioning that proposed and 7T_EN SRAM cells provide similar performance as both perform single-ended write operation by weakening the latch.
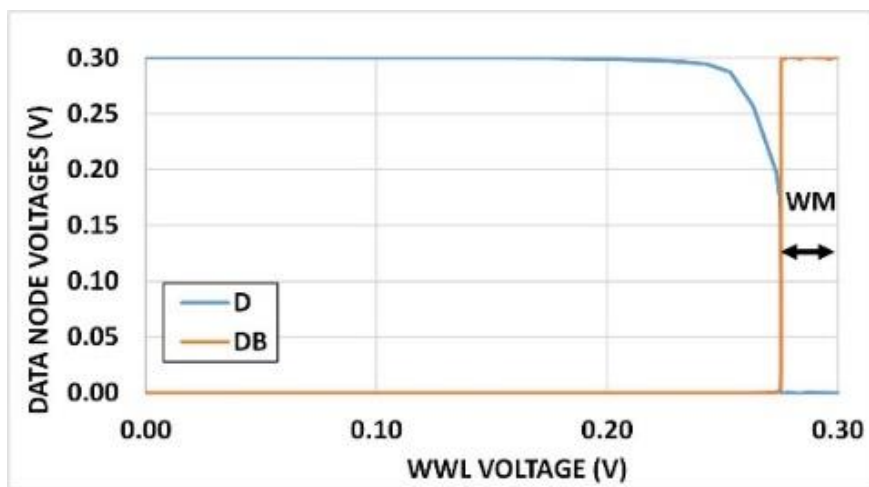
(a)
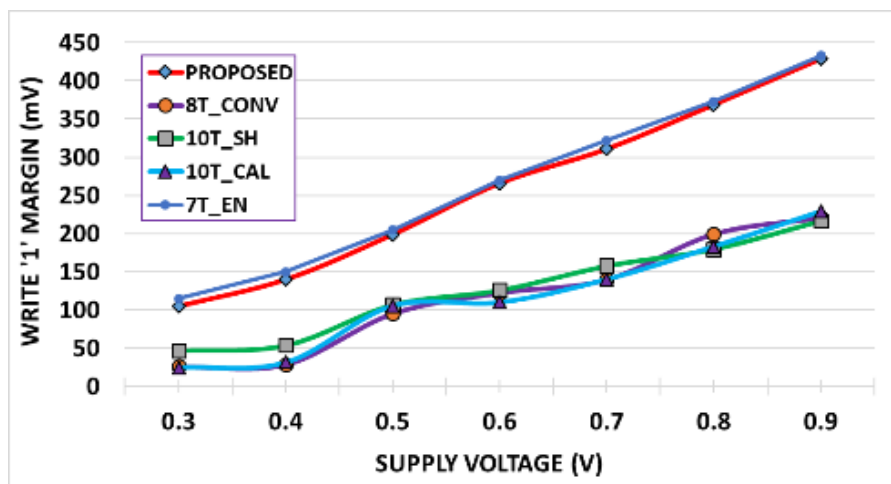
(b)
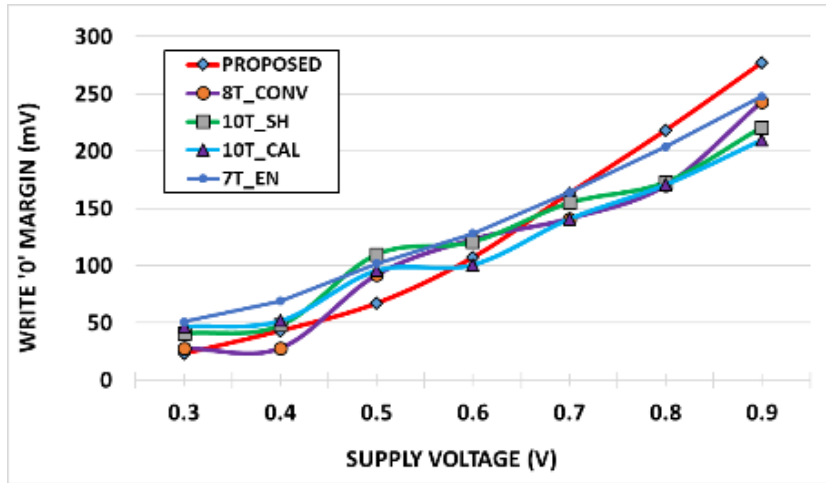
(c)

Fig. 5.2 WM at 27 °C (a) Simulated plot for Proposed cell V (b) WM ('1') (c) WM ('0')

T$_{\text{WRITE\_ACCESS}}$

The plots in Fig. 5.3 show the estimated values of T$_{\text{WRITE\_ACCESS}}$ at different voltages. The proposed cell shows up to 98.6 % and 99.5 % improvement in T$_{\text{WRITE\_ACCESS}}$ ('1') and ('0') respectively over other cells at 0.3 V.
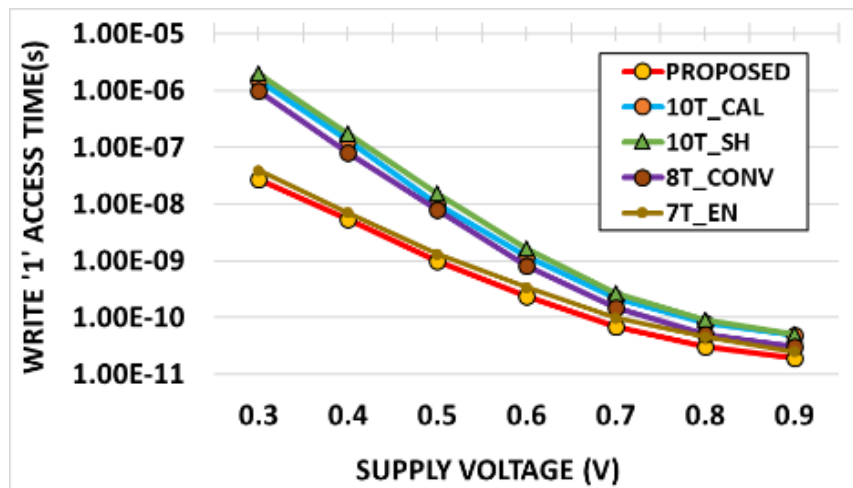
(a)
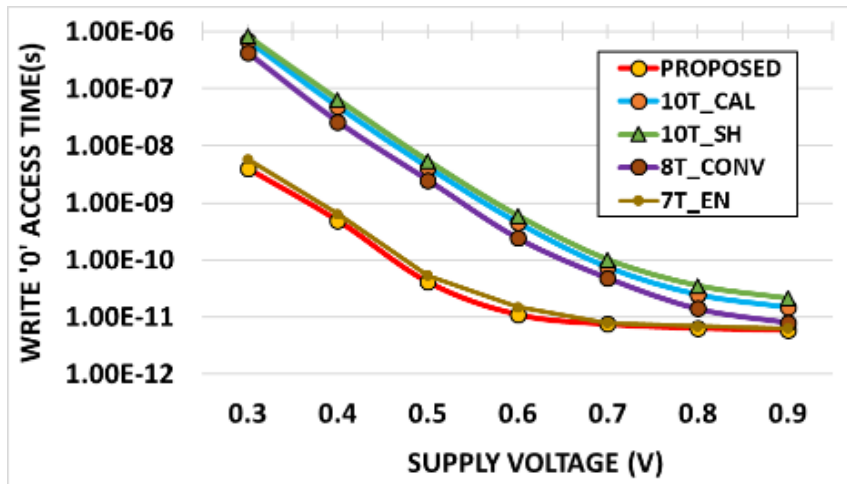
(b)

Fig. 5.3 T$_{WRITE\_ACCESS}$ at 27 °C (a) T$_{WRITE\_ACCESS}$ ('1') (b) T$_{WRITE\_ACCESS}$ ('0')

<u>*Read mode*</u>

In this mode, the RSNM is measured to gauge the impact of external interference on stored data. The time to read the stored data is evaluated as T$_{READ\_ACCESS}$. The ΔV_{RBL} is captured to measure the ability of the design to correctly sense the stored value as '0' and '1' during read cycle.

RSNM

The RSNM is measured as shown in Fig. 5.4(a) at 0.3 V. It can be observed that the proposed cell shows significant improvement in read stability in comparison to 8T_conv cell due to more steeper characteristics. The results in Fig. 5.4(b) shows that the proposed cell achieves 19 %, 16 %, 21 % and 26 % improvement in RSNM value compared to 8T_conv, 10T_sh, 10T_cal and 7T_EN cells respectively.
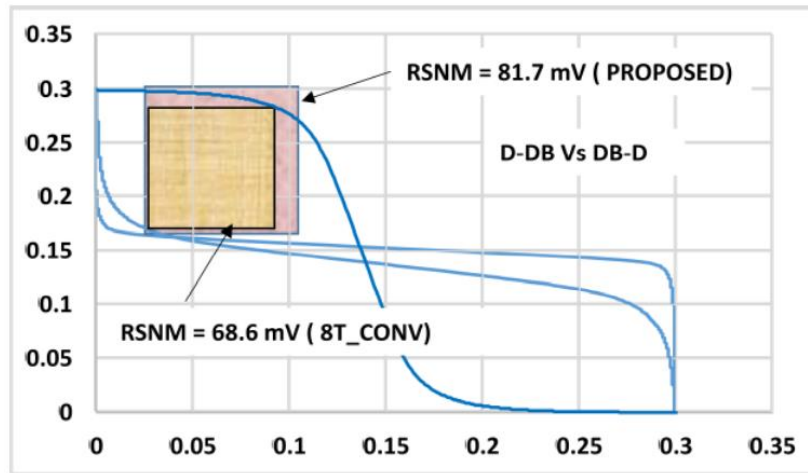
(a)
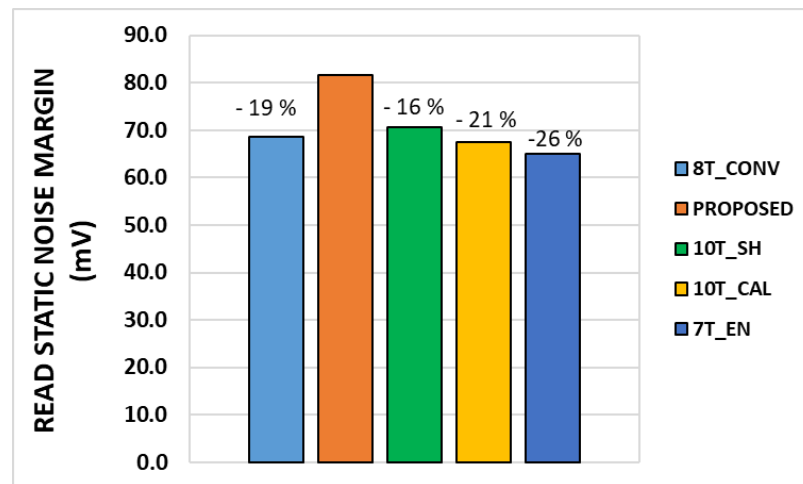
(b)

Fig. 5.4 RSNM (a) Simulated butterfly curves (b) RSNM values at 0.3 V and 27 °C

T<small>READ_ACCESS</small>

The T<small>READ_ACCESS</small> is measured at different supply voltages for all the cells and the values are plotted in Fig. 5.5. The proposed cell provides significant reduction in Tread values irrespective of supply voltage. An improvement of up to 99.9 % is observed compared to other cells in the sub-threshold region.
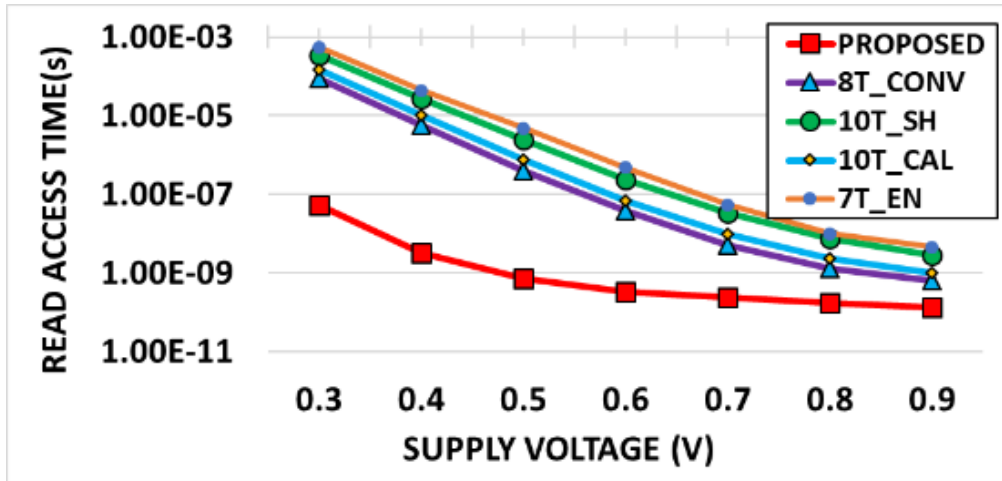
Fig. 5.5 T_{READ_ACCESS} at 27 °C

ΔV$_{RBL}$

The normalized values of ΔV$_{RBL}$ for all the cells are captured at different voltages and are plotted in Fig. 5.6. The results depict that the proposed cell achieves an improvement of 70 %, 49 %, 37 % and 67 % in comparison to 8T_conv, 10T_sh, 10T_cal and 7T_EN cells respectively in sub-threshold region.
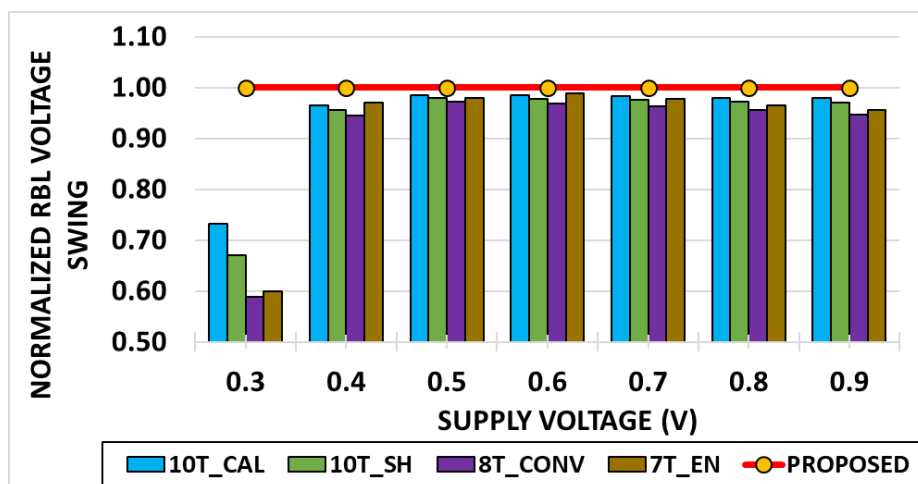
Fig. 5.6 Normalized ΔV$_{RBL}$ at 27 °C

Hold mode

The key parameters namely HSNM, DRV and P$_{LEAK}$ are estimated and compared in this mode.

156

HSNM

The stability of stored data at complementary nodes D and DB in the presence of leakages is measured using HSNM (Fig. 5.7). An improvement of 17 %, 14 %, 21 % and 25 % is seen in HSNM values for proposed cell with respect to 8T_conv, 10T_sh, 10_CAL and 7T_EN cells respectively at 0.3 V.
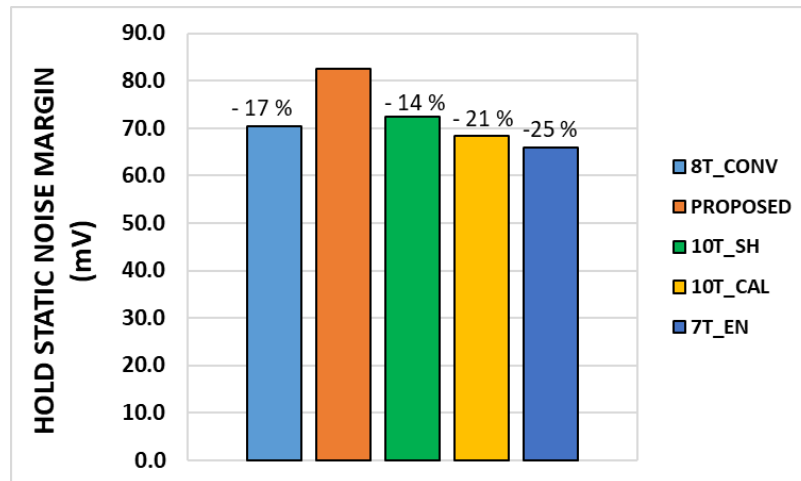
Fig. 5.7 HSNM at 0.3 V and 27 °C

DRV

The plot of DRV in Fig. 5.8 at different supply voltages shows that the proposed cell provides impeccable performance across all voltages. A percentage improvement of 77 %, 82 %, 83 % and 19 % is observed compared to 8T_conv, 10T_sh, 10_CAL and 7T_EN cells respectively at 0.3 V.
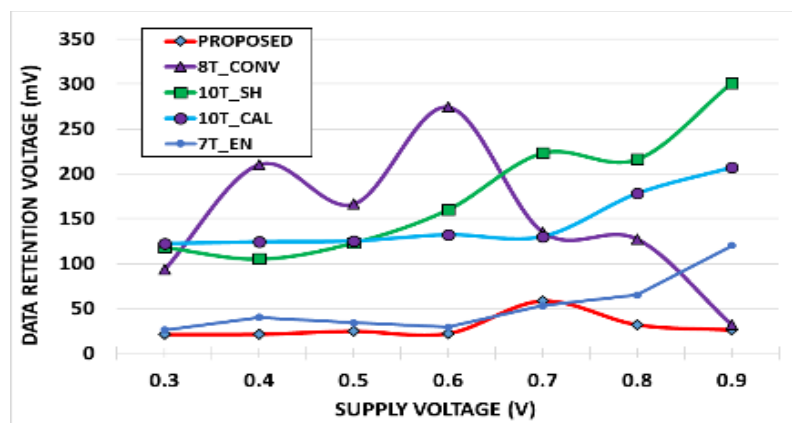
Fig. 5.8 DRV at 27 °C

P<small>LEAK</small>

A plot of P<small>LEAK</small> at different supply voltages (Fig. 5.9) depicts that values are comparable for all the cells in sub-threshold region. At higher voltages, the leakage power of proposed cell is more as the write assist transistor (MDL2) remains ON during hold mode and increases the overall leakage current of the latch structure compared to other cells.
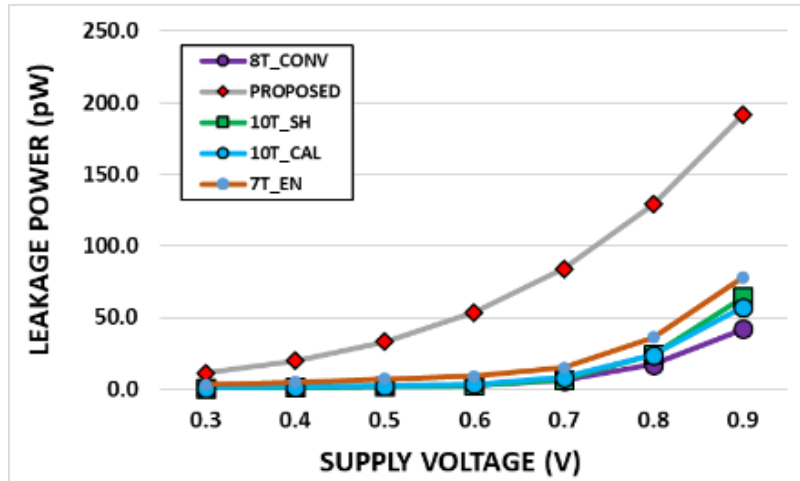
Fig. 5.9 P<small>LEAK</small> at 27 °C

Comparative analysis

The comparison results of all SRAM cells at $V_{DD} = 0.3$ V and T = 27 ˚C is shown in Table 5.2. The results reveal that the proposed cell provides significant improvement in all performance parameters except leakage power consumption. Thus, it can be used at lower technology nodes in sub-threshold region.

Table 5.2: Performance comparison at V_{DD} = 0.3 V and T = 27 ˚C

MODE	PARAMETER	8T_CONV	10T_SH	10T_CAL	7T_EN	PROPOSED V
Write	WM (mV)	26	47	25	55	105
	T_{WRITE_ACCESS} (ns)	1012	2053	1501	39.1	27.2
Read	RSNM (mV)	68.6	70.5	67.5	65	81.7
	T_{READ_ACCESS} (ns)	90000	340000	152000	560000	53.4
	ΔV_{RBL} (mV)	29.4	33.5	36.6	30	50
Hold	HSNM (mV)	70.3	72.3	68.3	66	82.5
	DRV (mV)	93	118	122	26	21
	P_{LEAK} (pW)	0.71	0.73	0.92	3.1	11.2

5.4 Conclusions

For sub-threshold operation, a FinFET based Proposed cell V providing improved write and read performance is presented in this chapter. The proposed cell is implemented at 22 nm technology node and shows an improvement of up to 322 % and 99.5 % in WM and T_{WRITE_ACCESS} respectively in write mode over other cells due to the presence of write assist transistor that eases the writing process. A 21 %, 99.9 % and 70 % improvement is also observed in RSNM, T_{READ_ACCESS} and ΔV_{RBL} respectively in read mode due to high read current values and, low and data-independent RBL leakages. It also shows up to 21 % and 83 % improvement in HSNM and DRV respectively in hold mode.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

This thesis presents the SRAM cell designs for nanometer technologies. The proposed designs attempt to address the limitations of existing designs at low supply voltages especially in sub-threshold region and provide the improved performance. This chapter summarizes the findings and identifies the future scope.

6.1 Summary of the work done

The chapter 1 presents a brief overview of SRAM array architecture. The structure of the conventional SRAM cell, various standard cell metrics that are used to quantify the performance of the SRAM cell and the issues related to its performance are also covered. Further, the approaches and techniques that may be used to improve the different aspects of SRAM cell performance are also discussed briefly in the chapter.

In chapter 2, the existing leakage reduction techniques for SRAM cells are classified based on leakage current component addressed through them within the cell and their leakage reduction capabilities are analyzed under PVT-variations. The impact of techniques on major performance parameters is included. For more conclusive comparison the impact of technology scaling is also evaluated to determine the best suitable operating conditions for a technique falling under each classification. Further, a low leakage SRAM cell is also proposed in the chapter. The Proposed cell I employs NWL technique to bias the OFF transistors in super cut-off region and reduce the BL leakages. In addition, it uses MTCMOS technique for latch implementation as the technique is observed to provide the best latch leakage current reduction capabilities. To reduce the deteriorating impact of MTCMOS technique on other performance parameters of SRAM cell, the technique is applied only on non-critical latch transistors.

Chapter 3 briefly describes the existing SRAM cells with improved read and/or write performance. It is noted that the existing cells has either enhanced read or write performance due to trade-off among the performance parameters. In view of these two new SRAM cells with an isolated read port are proposed to resolve the read-write conflict issue. Further, the Proposed cell II, incorporates write assist transistor with single ended write to reduce power consumption and a read port with no stacking of MOS transistors to achieve significant improvement in read current values. However, it was observed that the RBL leakages are also increasing with read current values. Therefore, to overcome this drawback Proposed cell III is presented. The Proposed cell III suggests the use of compensation transistor in read port that serves multiple functions. It suppresses RBL leakages in un-accessed cells independent of stored data values and provides compensating current in accessed cell to compensate for the RBL leakages in un-accessed cells. The reduced stacking effect of transistors further helps in maintaining reasonable values of read current resulting in significant improvement in all the read performance parameters. For improvement in write mode, the cell employs faster differential write.

With continuous scaling down of device dimensions and supply voltages, the SRAMs are becoming vulnerable to PVT-variations leading to increasing chances of failure. Therefore, Chapter 4 of this thesis extends into the designing of PVT-variation tolerant SRAM cells. Initially, the existing PVT-variation tolerant SRAM cells are briefly reviewed and the areas of improvement are highlighted. This is followed by presentation of a PVT-variation tolerant SRAM cell based on the use of novel configuration of Schmitt-trigger inverter that provides data-independent tolerance against PVT-variations in all the three modes. The proposed cell employs a novel combination of Negative bitline write-assist technique along with modified Schmitt-

trigger action for improved write performance. The isolated read port design implements fully-gated ground scheme to reduce read port leakages whereas the differential read operation makes the process faster.

For low power applications, the FINFET is an amenable choice as it offers improved ON current, reduced V_{th} variations and better subthreshold slope. Considering this, the focus of chapter 5 is on the design of the SRAM cell with improved transistor technology. A FinFET based Proposed cell V at 22 nm is presented in this chapter. The proposed cell addresses the issues present in existing CMOS and FinFET based SRAM cells such as reduced stability of stored data, increased bitline load capacitance with longer discharge time and increased leakages. The isolation of internal storage nodes from external bitlines improves data stability. The RBL leakages are reduced by maintaining similar operating conditions in un-accessed cells independent of stored data values. Additionally, the increased driving strength of FinFET based cell results in high read current values providing significant improvement in read performance parameters. The use of write assist transistor helps in quick charging of internal storage nodes resulting in faster write operation.

6.2 Future Scope

In this work, the different SRAM cell designs for nanometer technologies are explored and several contributions are made to improve the different aspects of SRAM cell performance. The work primarily focused on modifying the existing cell designs for improving performance or presenting a new SRAM cell designs altogether. There are several dimensions where the work may be extended further; following are some of the possibilities:

a) The data stored at the internal nodes of SRAM cell may get greatly affected when the high-energy radiation particles strike it; a problem commonly known as single event upsets (SEUs). Therefore, SRAMs are the most radiation-sensitive part of the SoC, an issue that is exacerbated with device and technology scaling; and is becoming a major reliability concern in SRAMs in space applications, where the radiations are high. Therefore, the designs presented in chapter 3 and 4 may be modified further to make them more robust against radiations.

b) Since the memory architecture plays a crucial role in handling the issue of increased bitline capacitances. Therefore, there is a requirement to work on improved memory architectures for constructing large SRAMs.

c) The higher parasitics due to three-dimensional structure, corner effect and high fabrication cost of FinFET has challenged its usage below 5 nm. The other improved transistor technologies such as Nanosheet FETs, Nanowire FETs, CNTFETs are emerging as an alternative to FinFETs. Therefore, there is a need to explore these transistor technologies for designing SRAMs in nanometer-regime.

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PUBLICATIONS

List of Journal Papers:

1. M. Gupta, K. Gupta, N. Pandey, " **A Data-Independent 9T SRAM Cell with Enhanced I_{ON}/I_{OFF} Ratio and RBL Voltage Swing in Near Threshold and Sub-Threshold Region**", International Journal of Circuit Theory and Applications, Wiley, 49, 4, 953-969, 2021. **(SCI Journal with Impact Factor: 2.038)**

2. M. Gupta, K. Gupta, N. Pandey, "**Comparative Analysis of the Design Techniques for Low Leakage SRAMs at 32nm**", Journal of Microprocessors and Microsystems, Elsevier, 85, 1-19, 2021. **(SCI Journal with Impact Factor: 1.526)**

3. M. Gupta, K. Gupta, N. Pandey, "A **Novel PVT-Variation Tolerant Schmitt-Trigger Based 12T SRAM Cell with Improved Write Ability and High I_{ON}/I_{OFF} Ratio in Sub-Threshold Region**", International Journal of Circuit Theory and Applications, Wiley, 49, 11, 3789-3810, 2021. **(SCI Journal with Impact Factor: 2.038)**

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