SIMULATION AND ANALYSIS OF OPTICAL LOGIC GATES

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE

OF

MASTER OF TECHNOLOGY
IN
MICROWAVE AND OPTICAL COMMUNICATION

Submitted by:

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2K20/MOC/02

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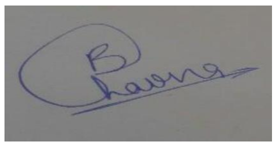
CANDIDATE'S DECLARATION

I, Bhavna Prasad (2K20/MOC/02) student of M. Tech (Microwave and Optical Communication Engineering), hereby declare that the Major Project-II dissertation titled "**SIMULATION AND ANALYSIS OF OPTICAL LOGIC GATES**" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship, or other similar title or recognition.



Place: Delhi **Bhavna Prasad**

Date: 30/05/2022

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CERTIFICATE

I hereby certify that the Major Project-II dissertation titled "**SIMULATION AND ANALYSIS OF OPTICAL LOGIC GATES**" which is submitted by Bhavna Prasad (2K20/MOC/02) in the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology is a record of project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date: 30/05/2022

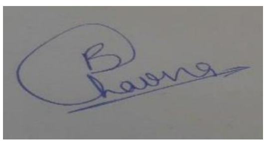
Dr. YASHNA SHARMA

SUPERVISOR

ACKNOWLEDGEMENT

The success and outcome of this project required a lot of guidance and assistance from many people, and I am extremely fortunate to get this all along with the completion of my project work. Whatever I have done is only due to such guidance and assistance and I would not forget to thank them.

I owe my profound gratitude to my project guide **Dr. Yashna Sharma** for giving me the opportunity to do this work. **Dr. Yashna Sharma** to ok keen interest in my project work and guided me throughout, till the completion of the project work by providing all the necessary information, constant encouragement, sincere criticism, and a sympathetic attitude.



BHAVNA PRASAD

ABSTRACT

Optical logic gates are designed to perform same functions in optical domain as Boolean logic gates performs in digital domain. The basic gates are OR, NOT and AND. NAND and NOR are universal gates and XOR and XNOR are derived Gates. Here, these gates are implemented in LUMERICAL by using finite difference time domain. The structure consist of a Y shaped cavity in silver film layer which is on the top of silicon dioxide substrate. There are two input ports to provide different input according to amplitude requirement and a single output to obtain the output according to logic function. Here the substrate is made up of SiO2 layer and the signal path has no element the signal is transmitting in Air. The air gap is created in the Ag metal. The range of the simulation is 400 to 700 nm.

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CHAPTER 1
INTRODUCTION

1.1 OVERVIEW

There is always a question striking that how and in what way are computers able to send data between its components? The computers earlier uses switches which were programmed for "on" and "off" so that it can control transmission of data. The switches are easy understandable, now they are not used because they were slow. There are many technologies to replace switches, which are vacuum tubes, different generations of microchips and transistors. Now a days switches are not in use still there are function are still in use to send data. Different functions are used by the set of different name and symbols and these are basically known as Logic gates. Logic Gate represents the relationship between various classical logical and the gate name in the logic part represents that the logic gates can transfer the signal to the different part of the large circuit which is basically similar to a stoplight directing the traffic.

The following are the examples of the logical situations:

1. For example a gumball machine in this machine there can be two inputs. Input A will be we have to insert a coin and input B will be to click the button. So, in the outcome if we want a ball we have to do both which means we have to insert a coin and push the button (AND)

2. If there is a common bulb which has two switches in different rooms. These switches will be input of the bulb. And the bulb is on when either of the two switches are on. (OR)

3. Magnets are very good example of XOR gate. The two poles north and South Pole can be considered as two inputs. In magnet when there is same pole they repel each other and when there are different poles they attract each other (Exclusive or, XOR, in this when both conditions are true then output is false).

The system which shows above logical conditions are Logic Gates like AND, OR, XOR and many others. Logic gates are drawn with functionality of gate which is represented by AND, OR, XOR gates.

The input ports are generally represented on the left hand side and output ports are represented on right hand side.

The logical function is represented through logical table where logic 0 represents the false condition while 1 represents the true condition.

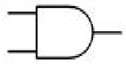
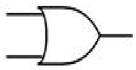
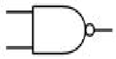
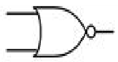
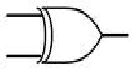
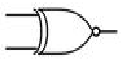
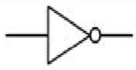
Logic Gate	Symbol	Description	Boolean
AND		Output is at logic 1 when, and only when all its inputs are at logic 1,otherwise the output is at logic 0.	$X = A \cdot B$
OR		Output is at logic 1 when one or more are at logic 1.If all inputs are at logic 0,output is at logic 0.	$X = A + B$
NAND		Output is at logic 0 when,and only when all its inputs are at logic 1,otherwise the output is at logic 1	$X = \overline{A \cdot B}$
NOR		Output is at logic 0 when one or more of its inputs are at logic 1.If all the inputs are at logic 0,the output is at logic 1.	$X = \overline{A + B}$
XOR		Output is at logic 1 when one and Only one of its inputs is at logic 1. Otherwise is it logic 0.	$X = A \oplus B$
XNOR		Output is at logic 0 when one and only one of its inputs is at logic1.Otherwise it is logic 1. Similar to XOR but inverted.	$X = \overline{A \oplus B}$
NOT		Output is at logic 0 when its only input is at logic 1, and at logic 1 when its only input is at logic 0.That's why it is called and INVERTER	$X = \overline{A}$

Fig 1. Description of all logic gates

1.2 DESIGNING OF GATES

The optical logic gates are designed using a SiO2 substrate and a Y coupler on it as shown in the figure below. There are two input ports to provide different input according to amplitude requirement and a single output to obtain the output according to logic function. Here the substrate is made up pf SiO2 layer and the signal path has no element the signal is transmitting in Air. The air gap is created in the Ag metal.

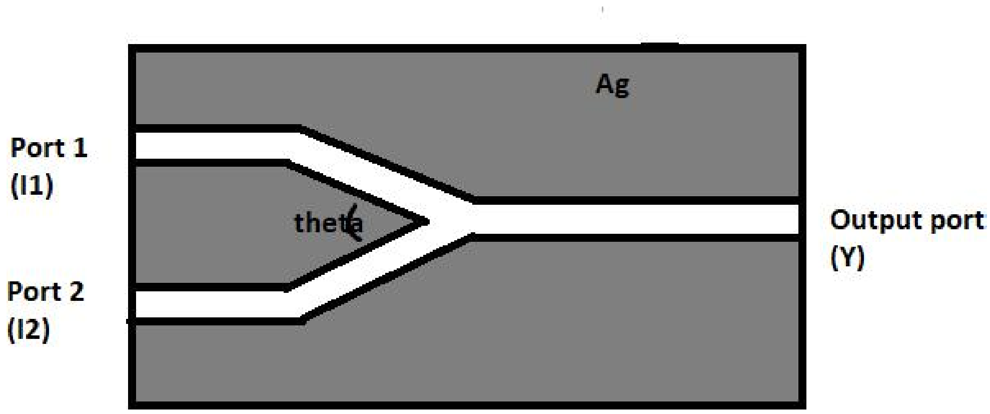


Fig 2. Front view structure of gate based on slot film

The thickness of the Ag metal and SiO2 layer is taken as 100nm and the angle of the coupler is 30 degree. The path for the transmission is 60nm wide. The permittivity of SiO2 is 2.13.

For, FDTD simulation the boundary conditions are taken to be periodic for all the boundaries.

The frequency range is 400 to 700 nm.

DFT monitors and Time monitors are used to view the results and spectrum.

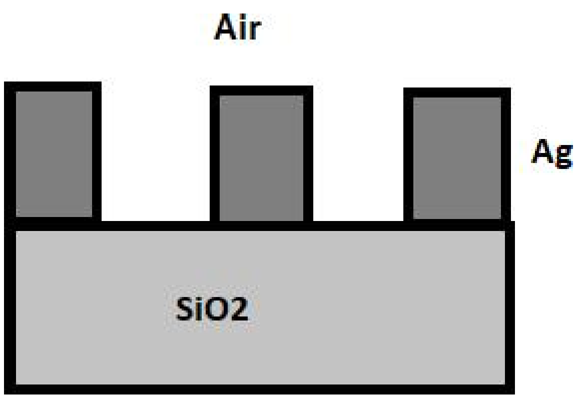


Fig 3. Side view structure of gate based on slot film

CHAPTER 2
LITERATURE OVERVIEW

2.1 OPTICAL LOGIC GATES

Optical Logic gates are the device used for transmission of light form input to output based on the different logic gates functions. For example – if we talk about AND logic gate the output of the gate will be according to AND function i.e. until we get all the input as high we will not get output.

Logical Gates works at two different levels of voltages one is the positive level and other one is the zero Level since Logic gates are digital components. These works on two states on and off. In the voltage zero, it is off state while for the voltage 1 it is on state. The range of the on state varies from 3.5 to 5 Volts and the range can be lower for some of the applications.

The state at the inputs of Logic Gates compares the state at the inputs and it decides what should be the output according to the input. A Logic Gate is either active or on according to the rules if they are correctly met. At the On state of the logic gates dictates the electricity which is flowing through the logic gate.

Truth tables indicates the state of the output depending upon the input and the Boolean Logic are the electronic versions of Logic Gates.

And optical logical gate are the optical version of digital logic gate and these gates are used to perform logical functions in photonics domain.

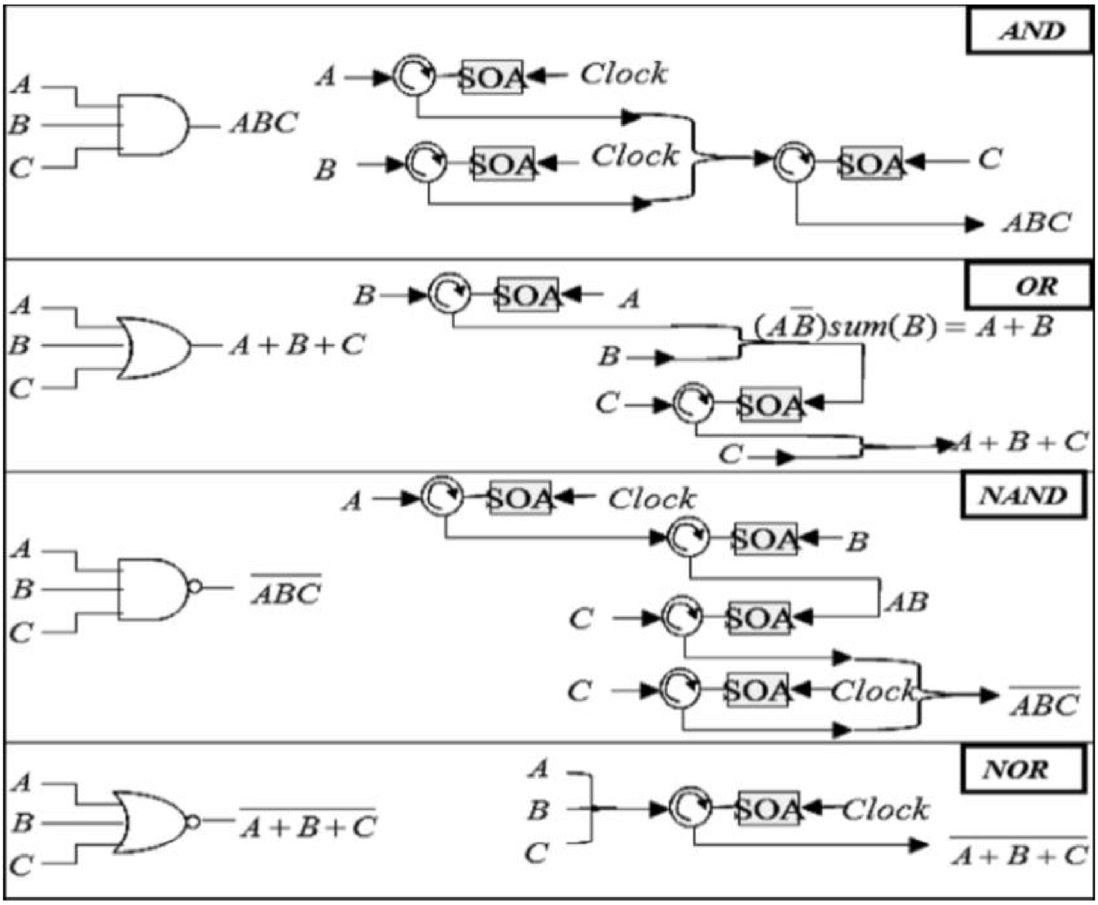


Fig 4. Designing using different amplifiers

2.1.1 BASIC LOGIC GATES:

AND GATE

The optical AND gate is a digital logic gate which is used to function same as logical AND in optical domain. The symbol, expression and truth table of the gate is mentioned below. The output is high when the both the inputs are high is one input is low then the output is low.

Symbol-

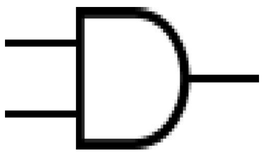


Fig 5. Symbol of AND Gate

Expression-

$$Y = A.B$$

Truth table-

Table 1. Truth table of AND Gate

INPUT		**OUTPUT**
A	**B**	**Y**
0	0	0
0	1	0
1	0	0
1	1	1

OR GATE

The optical OR gate is a digital logic gate which is used to function same as logical OR in optical domain. The symbol, expression and truth table of the gate is mentioned below. The output is high when any of the inputs is high is both input arw low then the output is low.

Symbol-

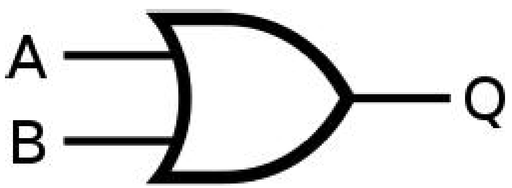


Fig 6. Symbol of OR Gate

Expression-

$$Y = A+B$$

Truth table-

Table 2. Truth table of OR Gate

INPUT		**OUTPUT**
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	1

NOT GATE

The optical NOT gate is a inverter which means if we give any input it will give inverted output.

Symbol-

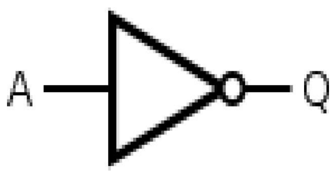


Fig 7. Symbol of NOT Gate

Expression-

$$Y = \bar{A}$$

Truth table-

Table 3. Truth table of NOT Gate

INPUT (A)	**OUTPUT (Y)**
0	1
1	0

2.1.2 UNIVERSAL LOGIC GATES:

NAND GATE

In electronics, a NAND gate is a combination of NOT and AND gate. The output is first AND then it is inverted. This means when both inputs are high we will get a low output.

Symbol-

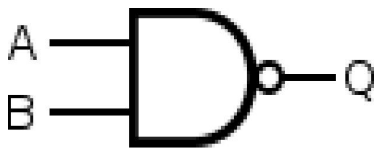


Fig 8. Symbol of NAND Gate

Expression-

$$Y = \overline{A.B}$$

Truth table-

Table 4. Truth table of NAND Gate

INPUT		OUTPUT
A	**B**	**Y**
0	0	1
0	1	1
1	0	1
1	1	0

NOR GATE

In electronics, a NOR gate is a combination of NOT and OR gate. The output is first added then it is inverted. This means when both inputs are low we will get a high output.

Symbol-

Fig 9. Symbol of NOR Gate

Expression-

$$Y = \overline{A+B}$$

Truth table-

Table 5. Truth table of NOR Gate

INPUT		OUTPUT
A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	0

2.1.3 DERIVED GATES

XOR GATE

This are called derived gates because they are derived from the basic AND, OR and NOT gates. They can be made from universal gates also. Then function of this gate if any one input is high we get high output and if there are same input at both the places we get a low input. Symbol,, expression and truth table are shown below.

Symbol-

Fig 10. Symbol of XOR Gate

Expression-

$$Y = \Theta = A.\overline{B} + \overline{A}.B = A \text{ xor } B$$

Truth table-

Table 6. Truth table of XOR Gate

INPUT		**OUTPUT**
A	**B**	**Y**
0	0	0
0	1	1
1	0	1
1	1	0

XNOR GATE

This are called derived gates because they are derived from the basic AND, OR and NOT gates. They can be made from universal gates also. Then function of this gate if any one input is high we get low output and if there are same input at both the places we get a high input. Symbol, expression and truth table are shown below.

Symbol-

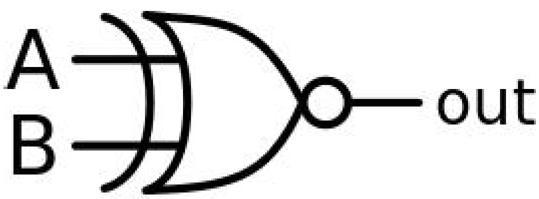


Fig 11. Symbol of XNOR Gate

Expression-

$$Y = A \odot B = A.B + \overline{A}.\overline{B} \; = \overline{x \quad y}$$

Truth table-

Table 7. Truth table of XNOR Gate

INPUT		OUTPUT
A	**B**	**Y**
0	0	1
0	1	0
1	0	0
1	1	1

2.2 Derivation of all gates from Universal logic gates

Using NAND Gate-

NOT Gate

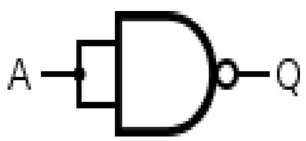


Fig 12. NOT Gate using NAND Gate

AND Gate

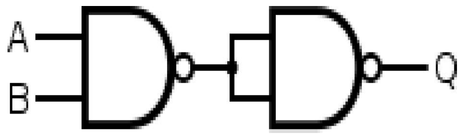


Fig 13. AND Gate using NAND Gate

NAND Gate

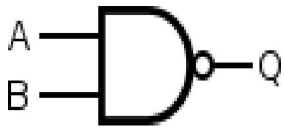


Fig 14. NAND Gate using NAND Gate

OR Gate

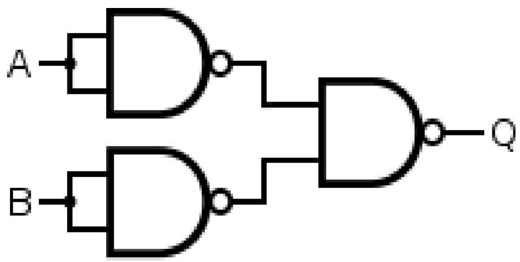


Fig 15. OR Gate using NAND Gate

NOR Gate

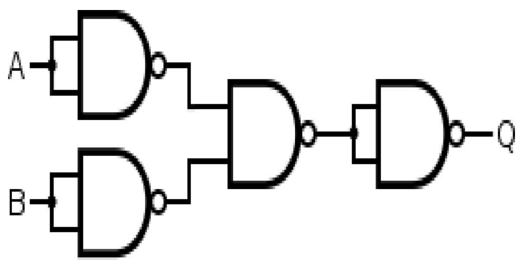


Fig 16. NOR Gate using NAND Gate

XOR Gate

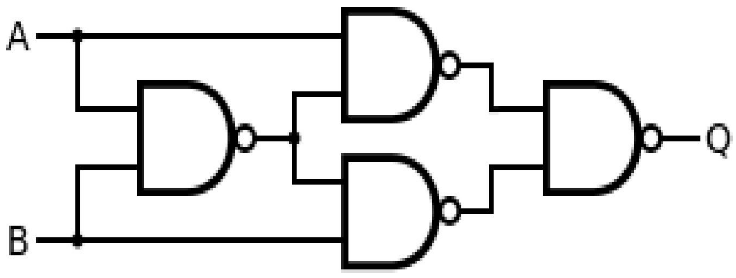


Fig 17. XOR Gate using NAND Gate

XNOR Gate

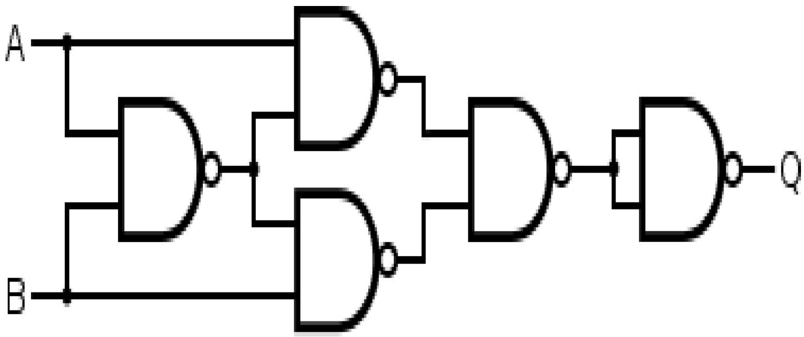


Fig 18. XNOR Gate using NAND Gate

Using NOR Gate-

NOT Gate

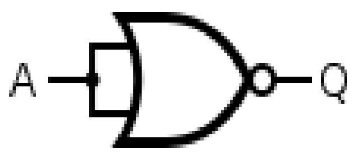


Fig 19. NOT Gate using NOR Gate

AND Gate

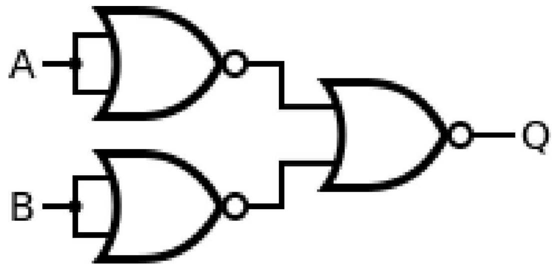


Fig 20. AND Gate using NOR Gate

NAND Gate

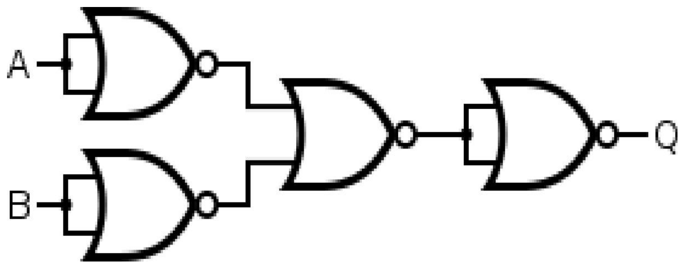


Fig 21. NAND Gate using NOR Gate

OR Gate

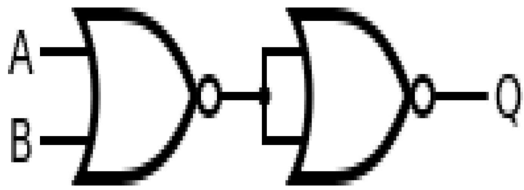


Fig 22. OR Gate using NOR Gate

NOR Gate

Fig 23. NOR Gate using NOR Gate

XOR Gate

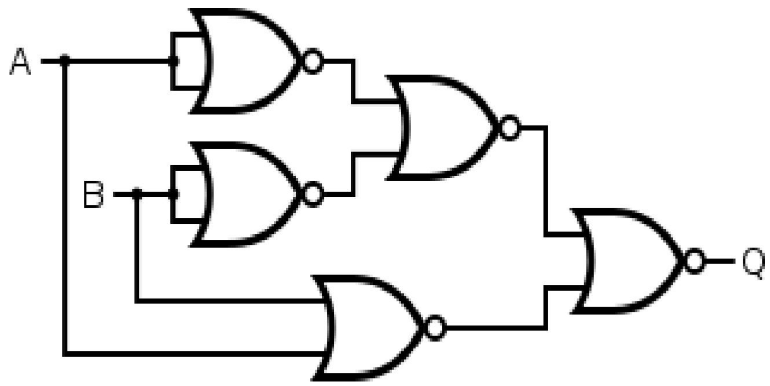


Fig 24. XOR Gate using NOR Gate

XNOR Gate

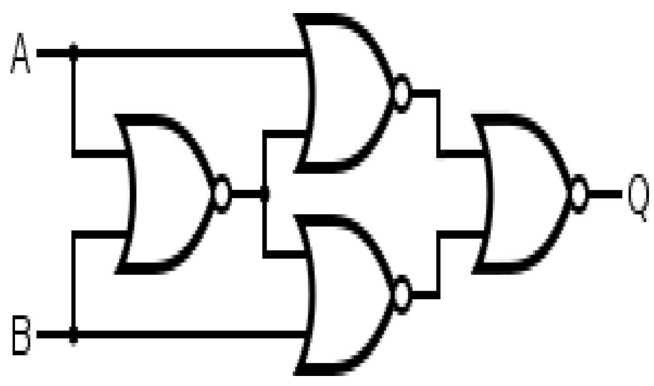


Fig 25. XNOR Gate using NOR Gate

Here, we are using LUMERICAL as a simulation tool to study these gates in optics and check we are getting the desired result or not.

Results given by the student are not correct,
and need major corrections before the date of viva.
Even after multiple reminders, she has failed to
incorporate these changes.

CHAPTER 3

SIMULATIONS

3.1 INPUTS-

In the fig shown below, the spectrum which is represented it is in time domain. The following spectrum represent the high input given at input port. For low input the spectrum will be of straight line at y = 0 axis.

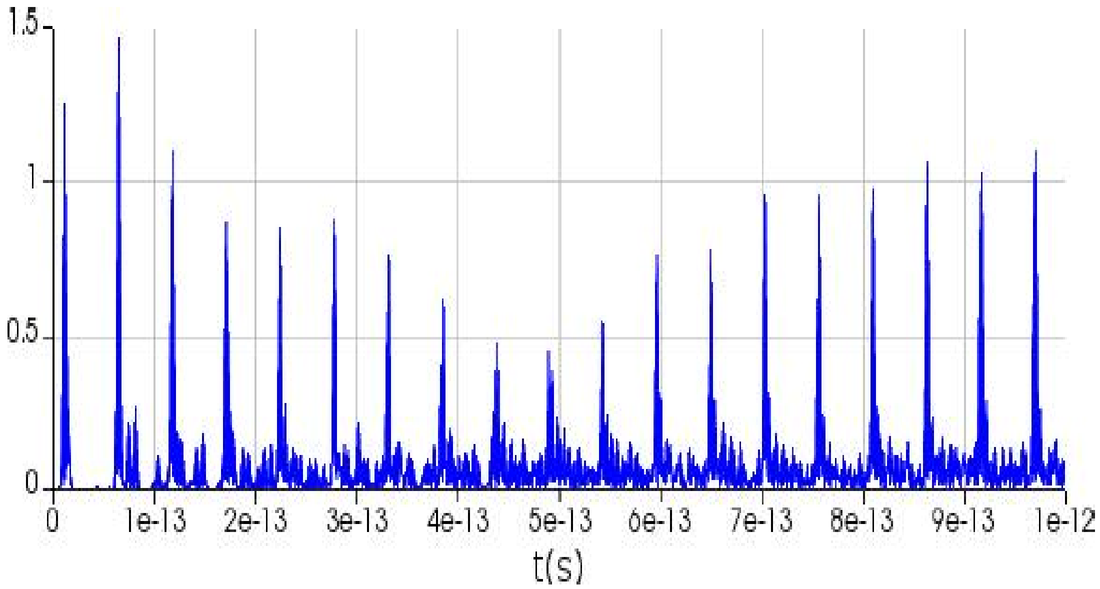


Fig 26. Time domain monitor for input 1

3.2 DESIGN OF GATE-

The following figures represent the different simulation views of our design.

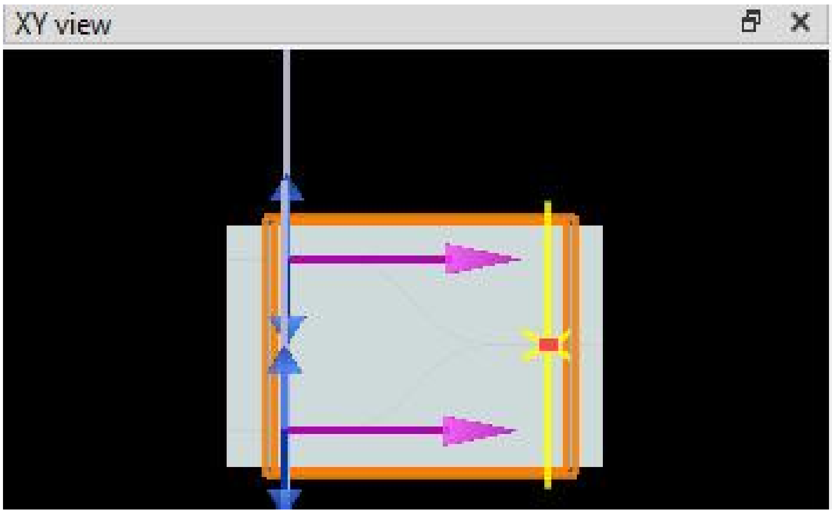


Fig 27. XY VIEW

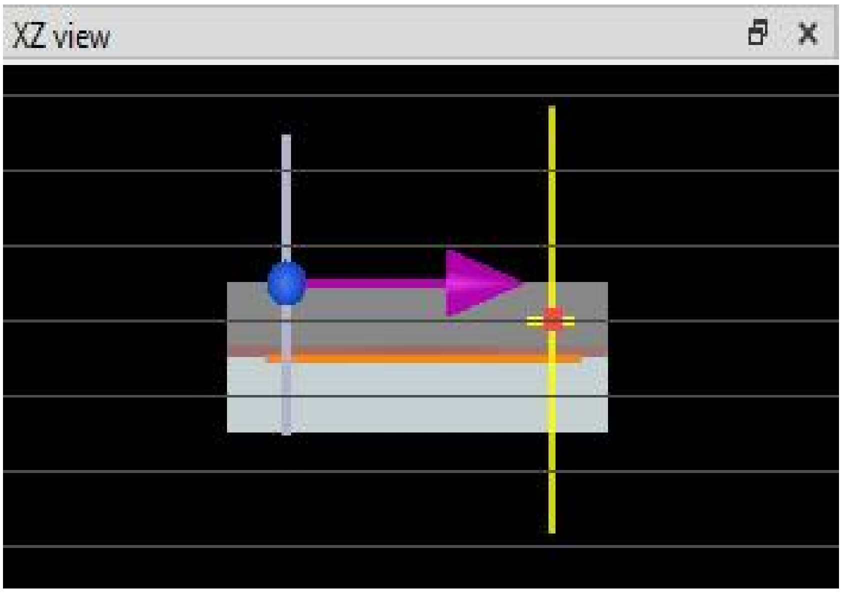


Fig 28. XZ VIEW

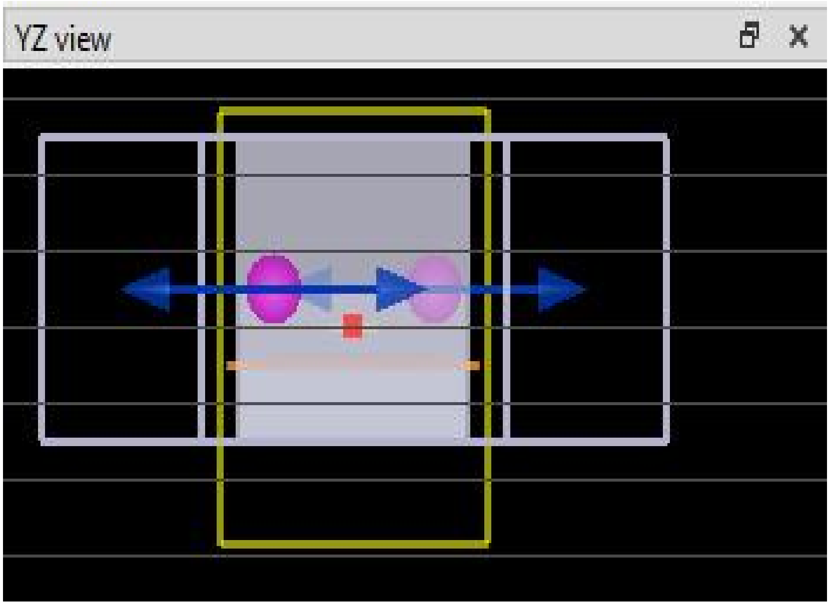


Fig 29. YZ VIEW

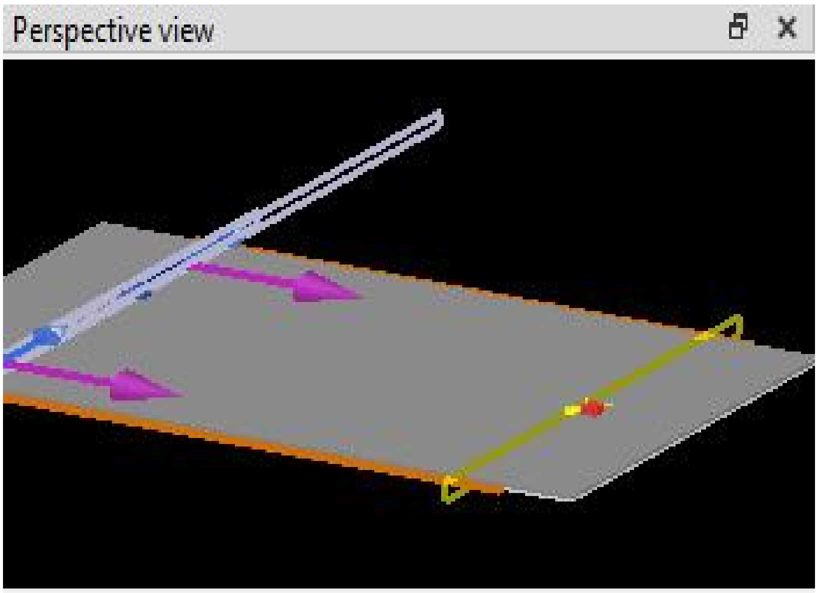


Fig 30. PERSPECTIVE VIEW

CHAPTER 4
RESULT AND OBSERVATIONS

4.1 RESULT

OR GATE-

So, for OR Gate we create a constructive inputs i.e. the input in electrical part can be said to be as between 0V to 5V. For low input we have taken amplitude equals to 0 and for high input we have taken input equals to 1.

So, output of the OR Gate for different combinations are,

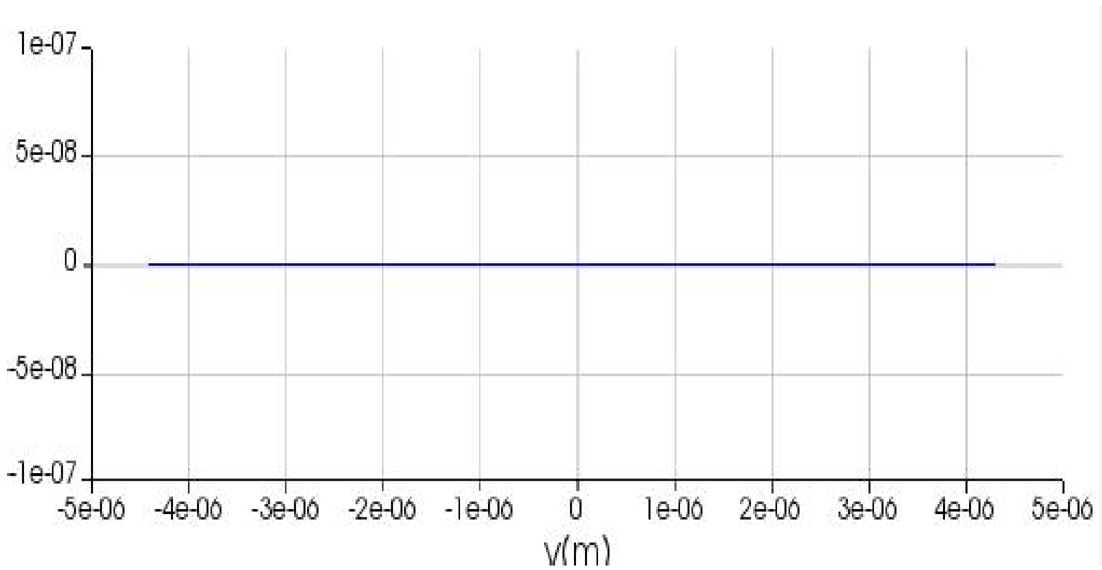


Fig 31. A =0, B=0

For (0,1) input fig 32 represents the electric field of the OR Gate. As the there is one input high we have got some result. The spectrum is not symmetry because there are some errors also. The similar result is for (1,0) and (1,1) inputs also.

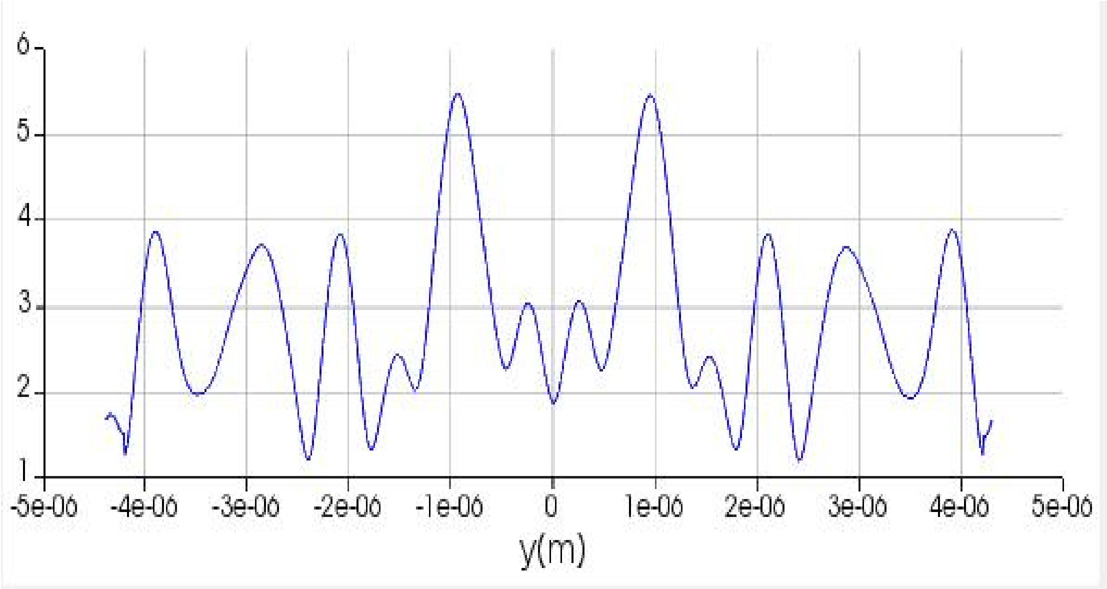


Fig 32. A =0, B=1

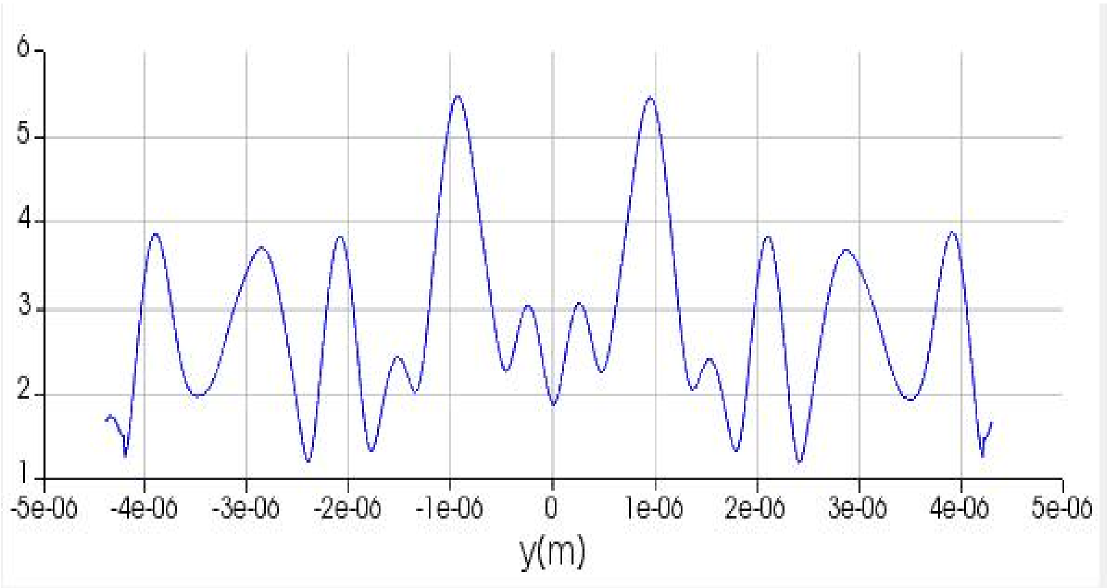


Fig 33. A =1, B=0

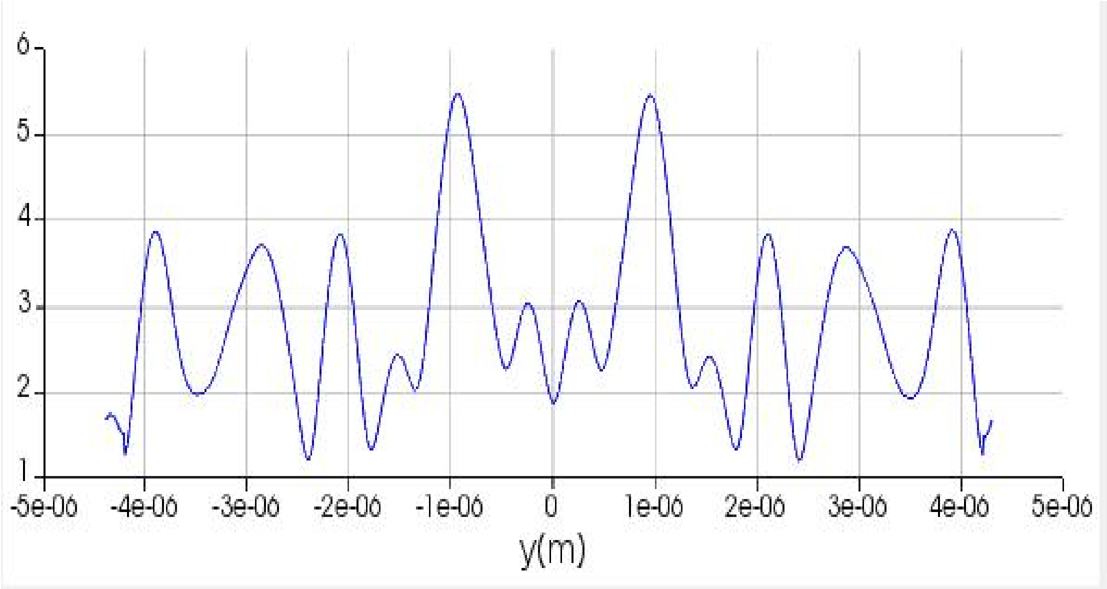


Fig 34. A =1, B=1

AND GATE-

So, for AND Gate we create a constructive inputs i.e. the input in electrical part can be said to be as between 0V to 5V. For low input we have taken amplitude equals to 0 and for high input we have taken input equals to 5. Here the inputs should be more than the threshold value and less than maximum input.

So, output of the AND Gate for different combinations are,

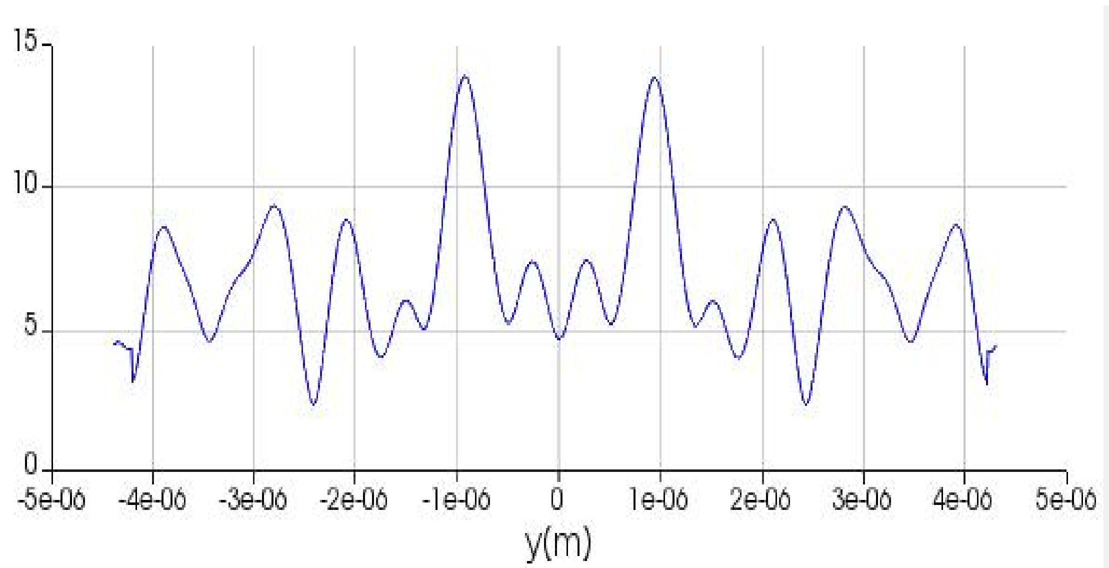


Fig 35. A =1, B=1

As the above Gate is AND Gate, so in fig 35. It is showing some result. And we can see that compared to AND gate the output of electric field has higher amplitude. This is because we have taken high amplitude in input side also to make it work as AND gate.

And below are the output is any of the input is low. This means we haven't got any output for (0,0),(0,1) and (1,0).

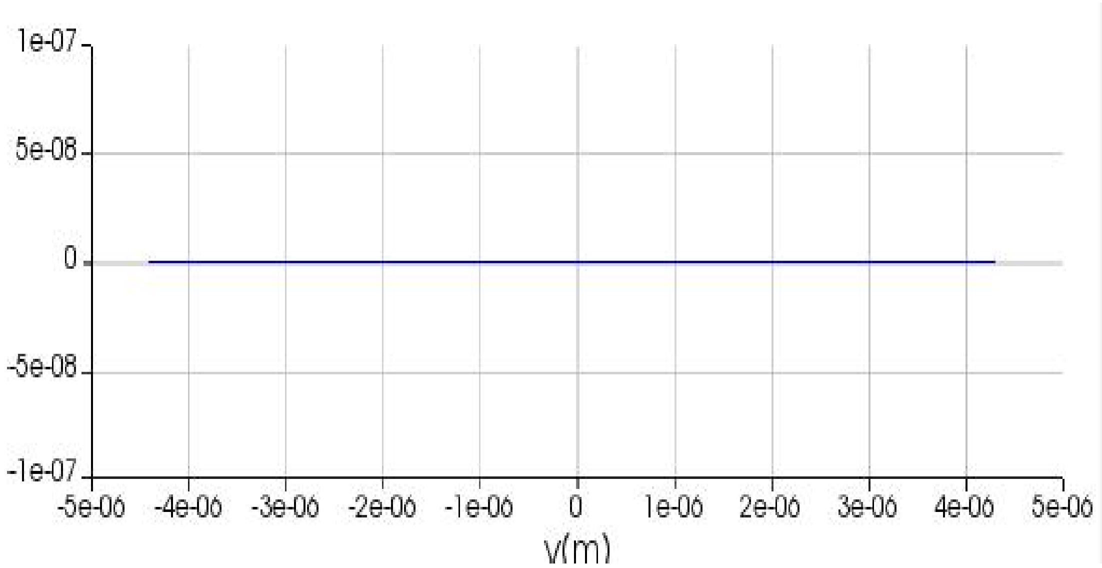


Fig 36. A =0, B=1

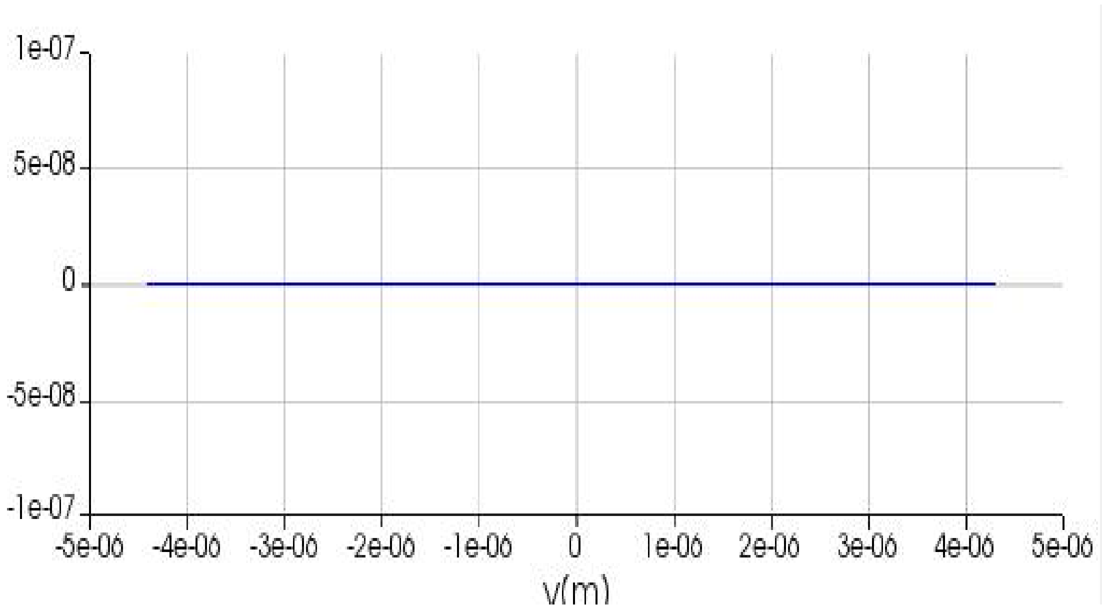


Fig 37. A =1, B=0

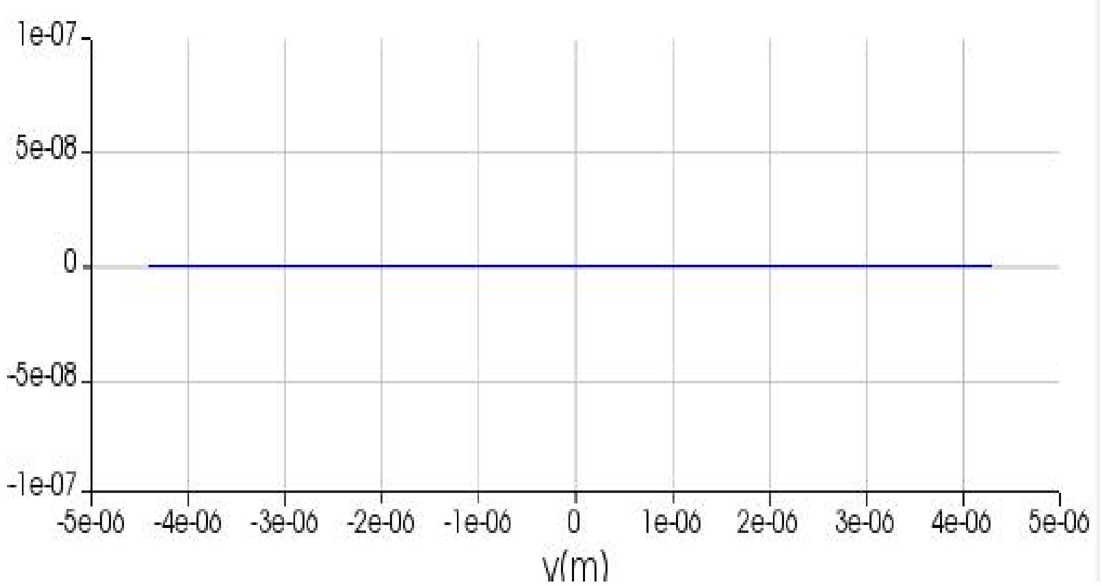


Fig 38. A =0, B=0

NOT GATE

NOT Gate gives output opposite to the input provided. So, the input port 2 is used as a control signal and only 1 input is sending signals.

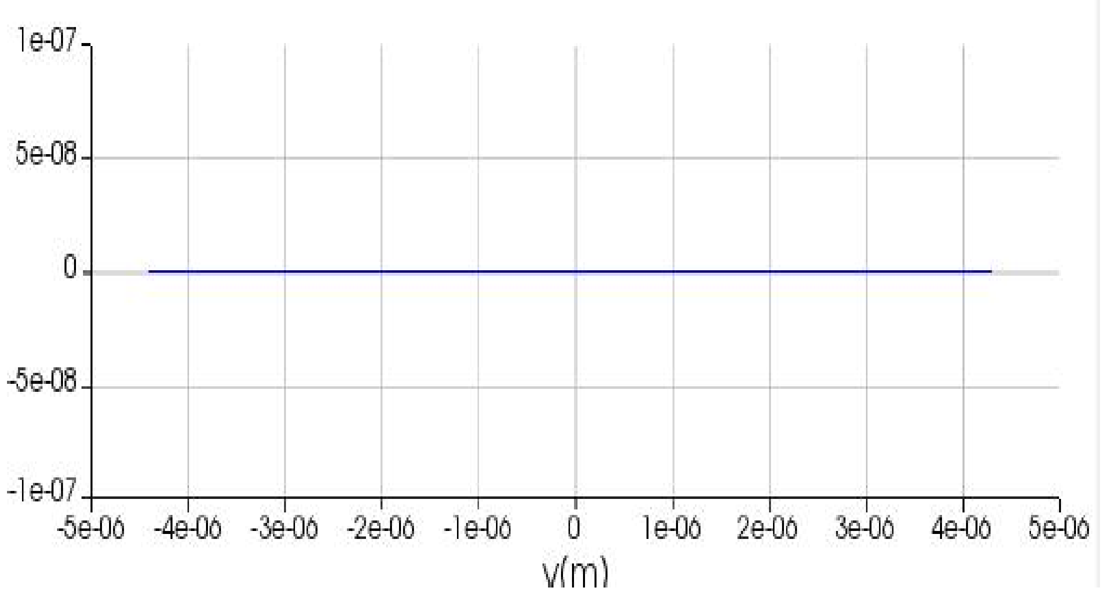


Fig 39. A =0

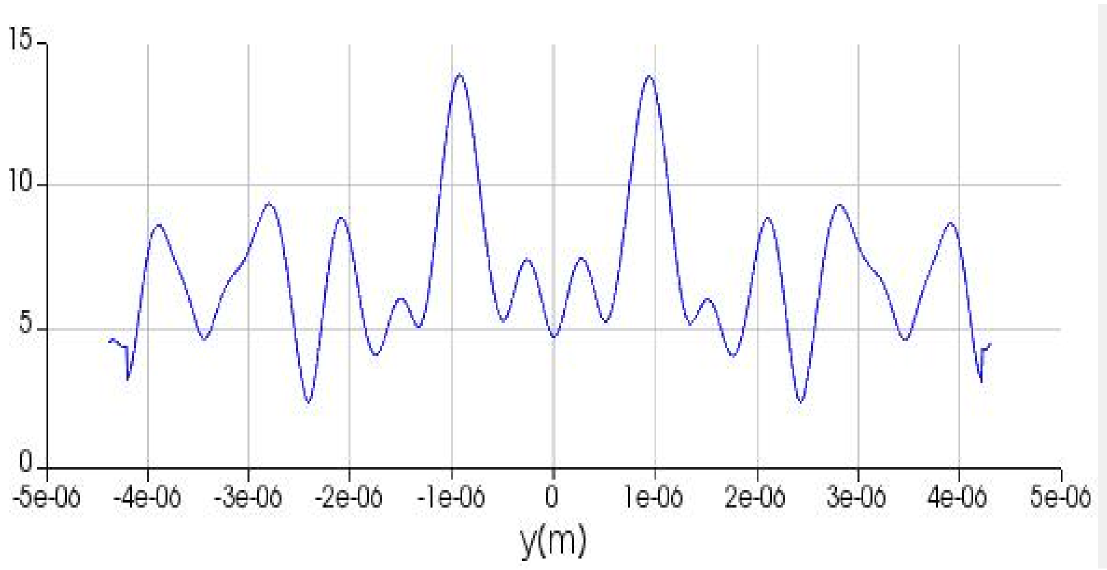


Fig 40. A = 1

CONCLUSION

After studying the gates above we are confident that the rest of the gates like NAND, NOR, XOR and XNOR can be also implemented using same method. In the future there is many more researches on this topic. By changing the value of input we have seen changes in our output also. The change in output is recorded. The result can be little different from the real result and as its in optical domain we can use it in various optical networks where we have to perform the logical operations. Further these logic gates can be fabricated and tested and the result can be compared to the simulation results.

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