REALISATION OF THE OFCC BASED INSTRUMENTATION AMPLIFIER

A DISSERTATION REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS

FOR THE AWARD OF THE DEGREE OF

MASTER OF TECHNOLOGY

IN

VLSI DESIGN & EMBEDDED SYSTEMS

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CANDIDATE'S DECLARATION

I, (Ayush Khare), Roll No. 2K17/VLS/06 student of MTech (VLSI design & Embedded systems), hereby declare that the project Dissertation titled "Realisation of the OFCC based Instrumentation Amplifier" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "Realisation of the OFCC based Instrumentation Amplifier" which is submitted by Ayush Khare 2K17/VLS/06, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

Nowadays, current mode devices are used as active elements at the circuits that work at high frequencies. A novel integrated CMOS based the operational floating current conveyor (OFCC) is used to develop Trans-admittance amplifier (TAM) and Trans-impedance amplifier (TIM) based Instrumentation Amplifier. OFCC is a five-port general purpose analog building block which combines all the features of different current mode devices such as the second-generation current conveyor (CCII), the current feedback operational amplifier (CFA), and the operational floating conveyor (OFC).

The OFFC is modelled and simulated using 0.5μm CMOS technology kit in Or-cad Capture tool and the supply voltage of the proposed OFCC is 1.5V.

Current mode (CM) blocks offers advantages over voltage mode (VM) blocks, such as performance improvement, low power consumption, controlled gain without feedback components, better linearity and improved bandwidth. This gives the motivation to use CM block to implement various ASP applications and to review already existing literatures available using CM blocks. Current conveyor is used as it is a high-performance active element and it ensures high accuracy, wide bandwidth and exceptionally high slew rates combined with low voltage and low power implementations under small or large signal conditions.

The main advantage of the proposed OFCC that it provides a wide bandwidth compared to other work. In addition, the applications based on OFCC shows good results compared to others.

The new topology of instrumentation amplifier (IA) using OFCC is proposed and analysed which is working in current mode (CM) and low output impedance, high differential mode gain and high CMRR.

ACKNOWLEDGEMENT

I express my deepest gratitude to my project guide **Dr. Deva Nand (**Assistant Professor), Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, whose encouragement, guidance and support from the initial to the final level enabled me to develop an understanding of the research work. His suggestions and ways of summarizing the things made me to go for independent studying and trying my best to get the maximum for my project, this made my circle of knowledge very vast. I am highly thankful to him for guiding me in this project.

I also express my profound sense of gratitude to **Prof. S. Indu** (H.O.D., ECE), for giving encouragement and opportunity to complete my project smoothly.

I also express my thanks to all staff of VLSI laboratory to provide me all facilities to complete this research.

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LIST OF ABBREVIATIONS AND SYMBOLS

ASP	:	Analog Signal Processing
SoC	:	System on a Chip
OTA	:	Operational Transconductance Amplifier
CM	:	Current Mode
VM	:	Voltage Mode
IC	:	Integrated Circuits
CMOS	:	Complementary Metal Oxide Semiconductor
BJT	:	Bipolar Junction Transistor
CC	:	Current Conveyor
CCI	:	First Generation Current Conveyor
CCII	:	Second Generation Current Conveyor
CCIII	:	Third Generation Current Conveyor
OFC	:	Operational Floating Conveyor
OFCC	:	Operational Floating Current Conveyor
CFA	:	Current Feedback Amplifier
VFA	:	Voltage Feedback Amplifier
CA	:	Current Amplifier
VA	:	Voltage Amplifier
IA	:	Instrumentation Amplifier
TAM	:	Trans-admittance Amplifier
TIM	:	Trans-impedance Amplifier
KCL	:	Kirchoff's Current Law
CMRR	:	Common Mode Rejection Ratio

CONTENTS

CHAPTER-1
INTRODUCTION

1.1 INTRODUCTION

Analog electronics has an immense assortment of uses, directly over the entire range of education industries, media communications, transportation, medical entertainment, industrial instrumentation and power supplies. Nonetheless, there are very few applications of electronics where analog techniques and circuits are not utilised in some piece of their framework.

Analog signal processing has played a very significant job in System on a chip (SoC) devices and correspondence frameworks. A framework on chip (SoC) is fundamentally an incorporated circuit or a chip which coordinates numerous circuits on a solitary chip and each chip is performing various activities. One of the most important pieces of SoC is the amplifier circuits. These circuits can be implemented utilising either voltage approach or current approach.

In voltage approach circuits, information is represented by voltage at nodes of the circuit whereas in current approach circuits, information is represented by the current flowing in various branches of the circuit.

With voltage mode circuits, huge output voltage swing can be achievable with minimal total power consumption in the device. But because of this it leads to high impedance at nodes of voltage mode circuits. With huge voltage swings, the parasitic capacitances present in the devices needs to be discharged and charged, thereby limiting the slew rate and speed of the voltage mode circuits. In voltage approach circuits, BJT's and MOSFET's in spite of being current devices are organised into voltage-arranged devices. The current signal is conveyed into voltage domain causing different consequences on the devices like it makes system bandwidth diminish, likewise the parasitic capacitance present in the high impedance node at voltage mode circuits create a dominant pole at lower frequencies. Accordingly, low power, low voltage and more extensive bandwidth capacities are hard to accomplish.

On the other hand, current mode circuits have developed as an option in contrast to voltage mode circuits since it offers a few preferences over voltage mode. As current mode circuits are low impedance node circuits improving framework execution regarding speed and slew

rate in terms of speed and slew rate. Current mode circuits offer wider bandwidths as the transistors used in current mode amplifiers are valuable up to their unity gain bandwidth. In integrated circuits, current mode has advantages offer voltage mode:

- Performance Development:
  - Low power consumption at high frequency.
  - High speed.
  - Low cross talk.
- Structural Advantage:
  - Easy schematic.
  - Simple architecture as addition and subtraction can be performed effectively.
- Specific Features:
  - Current switching techniques.
  - Well appropriate for low voltage and power applications.

As the devices are contracting on integrated circuits (IC's) and furthermore there is a continuous need of low power supply voltage these activities can be effectively taken care of in current domain as current mode circuits are designed for lower voltage swings.

There are different current block circuits which has brought about development of numerous analog building blocks that are utilized for the acknowledgment of various signal processing and generation circuits. Current conveyor (CC) is the most basic building block for realising analog circuits. It is both current and voltage circuits which is widely explored. The first-generation current conveyor (CCI) [1], second generation current conveyor (CCII)[2], third generation current conveyor (CCIII) [3], current feedback amplifier, operational floating current conveyor (OFCC) [4] are the different current block circuits in analog CMOS current mode signal processing.

The operational floating current conveyor (OFCC) [4] is another variant combining the features of both current feedback amplifier and second-generation current conveyors (CCII) [2]. It offers wide input voltage and current reaches, higher precision in voltage and current transfer, huge gain bandwidth product, ideally infinite open loop transimpedance gain, low input impedance and high output impedance.

OFCC is a current mode circuit which discounted the issues looked in voltage mode circuits [5].

CHAPTER-2
CURRENT MODE DEVICES

2.1 INTRODUCTION

In this section, a concise writing survey of the various sorts of current mode circuits like first generation current conveyor (CCI), second generation current conveyor (CCII), the current feedback amplifier (CFA), the operational floating conveyor (OFC), and the operational floating current conveyor (OFCC) is displayed. Furthermore, the difference between current mode (addressed by CFA) and voltage mode (addressed by VFA) circuits is discussed.

2.2 AMPLIFIER CIRCUITS

In this segment, we will present the most fundamental signal handling function, one that is utilized in some structure in pretty much every electronic framework, in particular, signal amplification which is the amplifier as a circuit building-block.

The power as well as amplitude of a signal is expanded utilizing the electronic amplifier by taking force from the DC power supply and controlling the yield or output to coordinate the information signal shape however with a larger amplitude

The gain of the amplifier circuit can be characterised as:

1. The proportional between the output and the input voltages.

2. Or the proportional between the output and the input power.

3. Or any other combination of current, voltage and power.

In the structure of an electronic system, the sign of interest—regardless of whether at the framework input, at the middle stage, or at the output—can be either a voltage or a current. For instance, a couple of transducers have high yield impedance and can be even more fittingly shown as current sources. In like manner, there are applications in which the yield current rather than the voltage is of interest. Thusly, disregarding the way that it is the most predominant, the voltage amplifier considered above is only one of four conceivable amplifier types. The further three are the current amplifier, the transconductance intensifier,

furthermore, the transimpedance amplifier. Table 2.1 demonstrates the four amplifier types and their ideal input and output impedance values.

Table 2-1: The four amplifier types and their Ideal Input and Output impedances values

AMPLIFIER CATEGORY	INPUT IMPEDANCE	OUTPUT IMPEDANCE
Trans-resistance amplifier	0	0
Trans-admittance amplifier	∞	∞
Voltage amplifier	∞	0
Current amplifier	0	∞

2.3 CURRENT MODE CIRCUITS

The voltage mode circuits experience the ill effects of having a consistent gain bandwidth product issue implying that when its gain starts to be increased, the bandwidth is diminished [6]. Current mode devices overcome the gain dependent bandwidth limitation so they have been utilised as the dynamic components at the circuits that work at high frequencies.

2.3.1 Current Conveyor

Current transports are a current mode of equivalent operational amplifiers. It is a three-terminal device (but can also have 4-6 terminals additionally) presented by Sedra and Smith in 1968[1]. It can perform numerous valuable simple signal processing applications when orchestrated with other electronic segments in explicit circuit arrangements relying upon the application. We can structure current conveyor circuits that work at levels near their anticipated hypothetical presentation which is a huge preferred position over the voltage mode circuits [7]. The structure of the current conveyors is predominant utilizing bipolar junction transistors (BJTs) and complementary MOS (CMOS).

2.3.1.1 First Generation Current Conveyor:

Smith and Sedra [1] presented an original circuit idea in 1968 called current conveyor on as indicated by which current is passed on between two ports at amazingly distinctive

impedance levels. The circuit building square exemplifying this idea was named originally as current conveyor, CCI. The block diagram is given in fig 2.1:

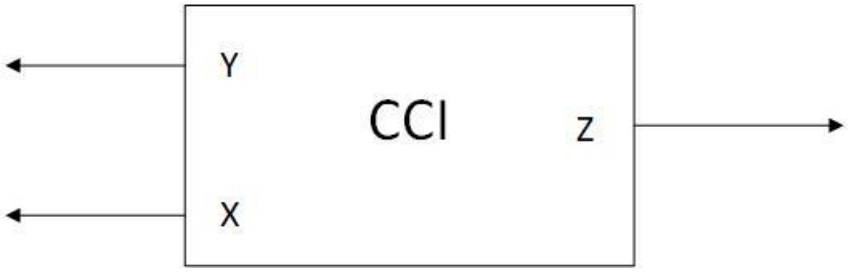

Fig 2.1 Block diagram of CCI [8]

From the block diagram, we can derive that if a voltage is connected on terminal Y, an identical voltage will appear on the terminal X. Correspondingly, an input current connected at terminal X will result into an identical measure of current streaming in terminal Y. The current I flowing in the terminal X will be passed to the output terminal Z such that terminal Z has the attributes like a high output impedance current source. The operation of CCI can be depicted by port matrix equation given below:

$$\begin{bmatrix} I_Y \\ V_X \\ I_Z \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & 1 & 0 \end{bmatrix} \begin{bmatrix} V_Y \\ I_X \\ V_Z \end{bmatrix} \quad (1)$$

Some application of CCI:

1) Negative impedance converter [9]
2) Useful in generating oscillators
3) Ideal voltage follower
4) Wideband Current measuring device [10]
5) High speed logic gate

2.3.1.2 Second Generation Current Conveyor:

It was published by Sedra in 1970 to improve the exhibition of the CCI. It has two forms: the primary is the positive second era current conveyor CCII+ [2] which copies the current from a low input impedance node to a high output impedance node having equivalent phase and magnitude. The subsequent one is the negative second era current conveyor CCII-which additionally duplicates the current from low impedance to a high impedance terminal but opposite in phase. The block diagram is given depicted in fig 2.2.

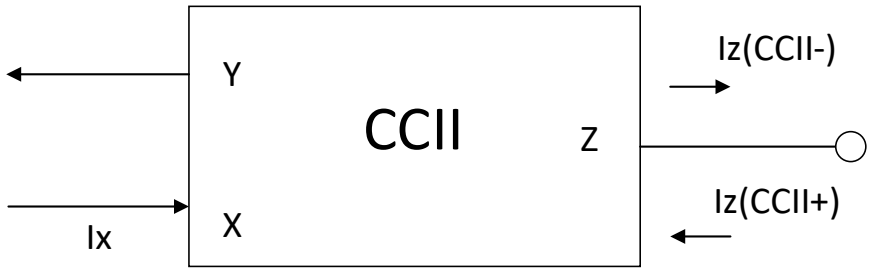

Fig 2.2 Block Diagram of CCII [11]

The terminal mapping equation matrix of second-generation current conveyor is given by:

$$\begin{pmatrix} I_Y \\ V_X \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ V_Z \end{pmatrix} \quad (2)$$

The input terminal Y has very high input resistance as the current flowing in this terminal is zero. However, voltage following activity exists at the input terminals Y and X for example the voltage connected at terminal Y is duplicated to terminal X. The current at input terminal X is taken to output terminal Z with the same magnitude but it can be in same phase (CCII+) or in the opposite phase (CCII-).

Some applications of CCII:

1) Simulation of inductors.
2) Realisation of immittance converters.
3) Filter realisations
4) Analog computation.

2.3.1.3 Current Feedback Amplifier (CFA):

Current feedback amplifier was originally proposed by David Nelson. It depended on CCII+ and structured by utilizing CCII+ circuit pursued by a buffer circuit as portrayed in fig. 2.3 [12] – [13].

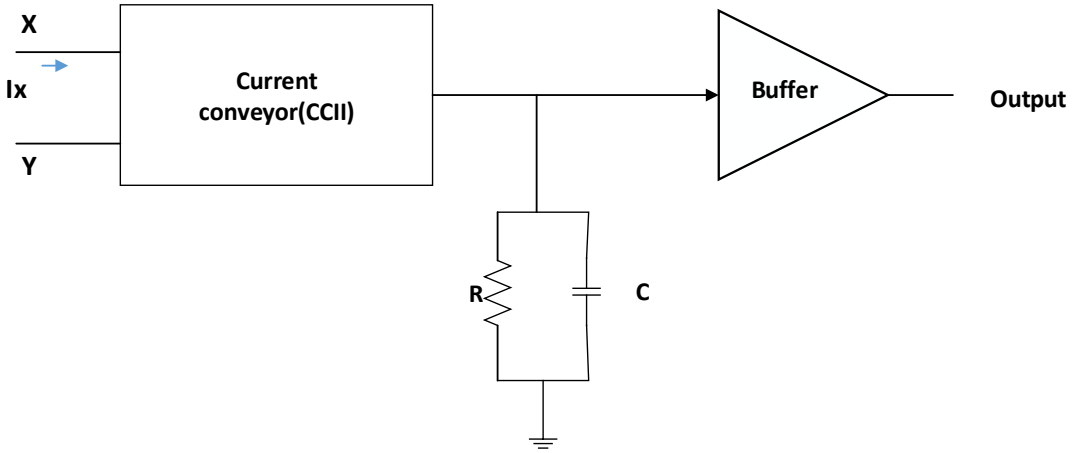

Fig 2.3 Block Diagram of CFA [12]

CFA circuit has two info ports. The first one being is the inverting input terminal (X) having low input resistance resulting in short circuit. And the subsequent one is the input (Y) in the noninverting form having very high input resistance resulting in the open circuit.

The CFA circuit has a voltage-following activity between its two info ports X and Y. The buffer is utilized to display the voltage-following between the two input ports of the CFA.

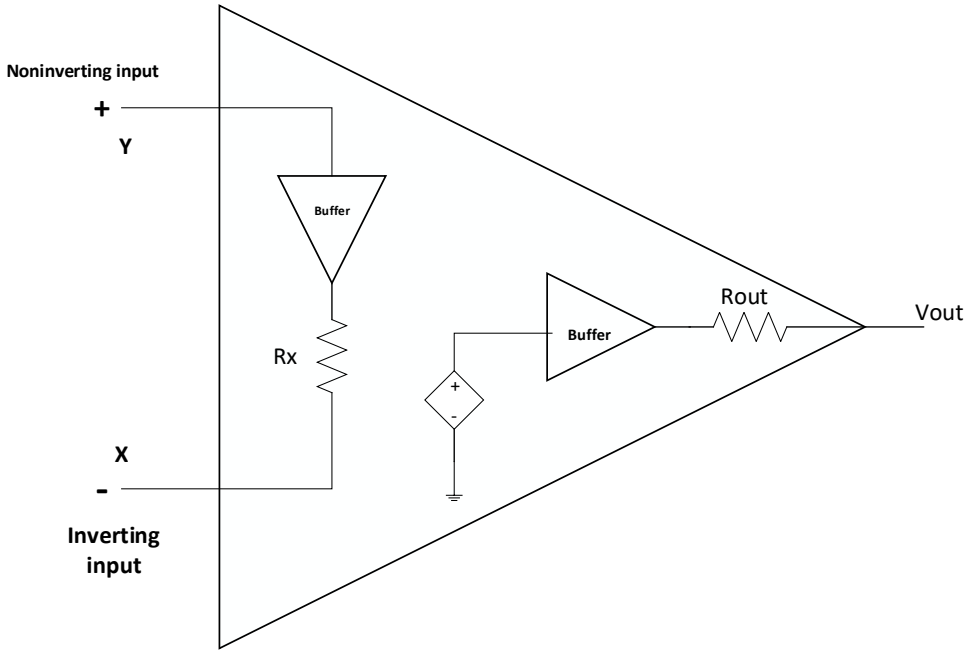

Fig 2.4 CFA equivalent circuit [14]

The CFA circuit can simply work fine in a closed loop manner. Likewise, the CFA circuit has an ideal criticism resistance which improves its steadiness and meanwhile it affects bandwidth [13].

2.3.1.4 Operational Floating Conveyor (OFC):

The operational floating conveyor (OFC) was originally introduced by Toumazou, Payne, and Lidgey in the year of 1991. It can be realised using a single CCII+ block, a non-inverting trans-impedance amplifier with gain Zt and a positive current follower as shown in fig 2.5 [4]

It can be seen that the output voltage at terminal W(V_W) equivalents to the total of the voltage at the input terminal of the trans-impedance amplifier and the input current at terminal X(I_x) multiplied by the trans-impedance amplifier gain (Z_t). Thusly, the input terminal of the trans-impedance amplifier of above realisation must be for all intents and purposes are virtually grounded so as to deliver an output voltage at terminal W(V_w) equivalents to the input current at terminal X(I_x) multiplied by the trans-impedance intensifier gain (Z_t) to give a legitimate realisation of the OFC block.

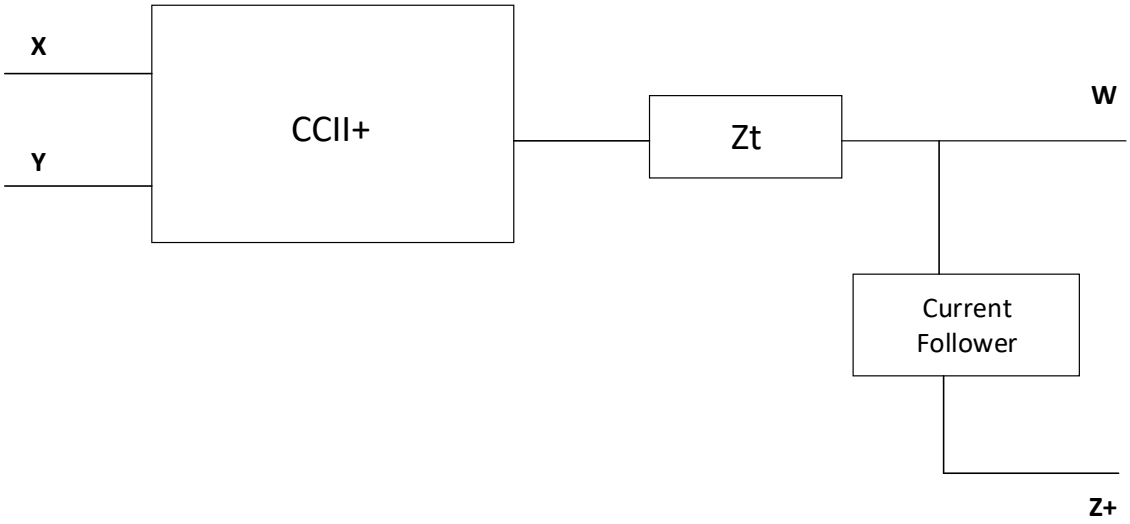

Fig 2.5 Block diagram of OFC using one CCII+ block and current follower [4]

It can be seen that the output voltage at terminal W(V_W) equivalents to the total of the voltage at the input terminal of the trans-impedance amplifier and the input current at terminal X(I_x) multiplied by the trans-impedance amplifier gain (Z_t). Thusly, the input terminal of the trans-impedance amplifier of above realisation must be for all intents and purposes are virtually grounded so as to deliver an output voltage at terminal W(V_w) equivalents to the input current at terminal X(I_x) multiplied by the trans-impedance intensifier gain (Z_t) to give a legitimate realisation of the OFC block.

Operation of OFC can be described using port matrix equation:

$$\begin{pmatrix} V_X \\ I_Y \\ V_W \\ I_Z \end{pmatrix} = \begin{pmatrix} 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 \\ Z_t & 0 & 0 & 0 \\ 0 & 0 & -1 & 0 \end{pmatrix} \begin{pmatrix} I_X \\ V_Y \\ I_W \\ V_Z \end{pmatrix} \tag{3}$$

2.4 Operational Floating Current Conveyor (OFCC):

OFCC is a versatile current mode analog block. OFCC has similar transmission properties as of OFC (operation floating conveyor) and current feedback amplifier (CFA). Generally, it is the five-port terminal analog building block. The symbol of OFCC [4] is shown in Fig

2.6[4]. The terminals X and Y are two info terminals and the port Y, Z+ and Z- are three output terminals.

Fig. 2.6 OFCC symbol [4]

Input terminal X is a low resistance current input port and the input terminal Y is a high input resistance voltage input port. Also, W terminal is the output voltage port and has low output resistance. Both Z+ and Z- are high resistance output current ports. The current delivered at terminal W is passed on to the two terminals Z+ and Z-with equivalent in magnitude yet inverse in phase (180◦ out of phase). OFCC has extra high output impedance terminal which makes the device having preferred adaptability over the CFA and OFC [15].

2.4.1 OFCC Operation:

The input current streaming at node X as it has very low input resistance (in a perfect way zero). It is multiplied by the open loop trans-impedance gain (Zt) to create an output voltage at node W. Hence, voltage following activity exists between the two input ports (X and Y). The voltage appearing at low input resistance node X is same as that appearing at the high input impedance node Y.

The output terminal W comprises of output signals which are of 2 types. The first is the voltage which is identical to the multiplication of input current of the input port X and open loop transimpedance gain (Zt) of the circuit. The subsequent one is the current produced at port W. This current is passed on to the node Z+ and Z- with the same extent but 180° out of phase. As Zt represents the very high open loop trans-impedance gain, therefore feedback loop among port X and port W is essential for developing any application.

Hence, from above operations we can deduce two types of tracking actions:

1) Voltage tracing action exists at the two info ports X and Y.
2) Current tracing action exists among output port W and Z+, Z- terminals.

The procedure of the OFFC can be defined by means of the resulting port matrix- equation:

$$\begin{pmatrix} I_Y \\ V_X \\ V_W \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ I_W \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \quad (4)$$

The above port matrix equation shows the ideal characteristics of OFCC. However, its behaviour may deviate from ideal to nonidealities of OFCC discussed below.

2.4.2 OFCC Nonidealities effect:

OFCC suffers from two types of nonidealities effect:

1) In terms of non-ideal current and voltage transfer between their respective ports and

2) Due to the finite transimpedance gain.

These two types of nonidealities are explained below in brief:

2.4.2.1 Finite Transimpedance gain effect:

Open loop transimpedance gain Z_t is ideally infinite. However, in reality this is not the case, in fact it is a frequency reliant on parameter of some determinate value. By using only pole method, the transimpedance gain Z_t can be given by:

$$Z_t(s) = \frac{Z_{to}}{1 + \frac{s}{\omega_{tc}}} \quad (5)$$

Where Z_{to} is the open loop trans-impedance gain and ω_t is the cut off frequency.

For very high frequency applications, Z_t can be expressed as:

$$Z_t(s) = \frac{1}{\frac{s}{Z_{t0}\omega_{tc}}}$$

$$Z_t(s) = \frac{1}{sC_p}$$

Where

$$C_p = \frac{1}{Z_{t0}\omega_{tc}}$$

C_p is the parasitic capacitance of OFCC.

2.4.2.2 Voltage and current tracking errors effect:

The port connection of OFCC practically speaking, differs since the condition in view of voltage and current following errors and is spoken to as:

$$\begin{pmatrix} I_Y \\ V_X \\ V_W \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ \beta & 0 & 0 & 0 & 0 \\ 0 & Z_T & 0 & 0 & 0 \\ 0 & 0 & \alpha & 0 & 0 \\ 0 & 0 & -\gamma & 0 & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ I_W \\ V_{Z+} \\ V_{Z-} \end{pmatrix} \quad (6)$$

Where $\beta = (1-\varepsilon_v)$ $\beta = (1-\varepsilon_{i+})$ $\beta = (1-\varepsilon_{i-})$ are errors in voltage transmission from Y to X port and error in current transmission from W port to Z+ and Z- ports respectively. Here ε_v signifies voltage following mistakes, whereas ε_{i+} and ε_{i+} are current following errors. The impact of following errors is unequivocally topology dependent, for instance, the voltage following mistakes does not influence the reaction if Y terminal of OFCC is put to zero voltage and the equivalent is valid for the current following errors if Z+ or Z-ports being not utilized.

2.5. Noise in Amplifier circuits:

An Amplifier, while intensifying just builds the quality of its information signal whether it contains data or some commotion alongside data. This noise or some unsettling influence is presented in the amplifiers on account of their solid inclination to acquaint murmur due with abrupt temperature changes or stray electric and magnetic fields.

The exhibition of an amplifier primarily relies upon this Noise. Noise is an undesirable sign that makes unsettling influence to the ideal signal substance in the framework. This can be an extra signal that is delivered inside the framework or can be some unsettling influence

went with the ideal data of the information signal. In any case, it is undesirable and must be expelled.

A decent framework is one in which the noise produced by the enhancer itself is little contrasted with noise from the approaching source.
Noise in electronic circuits is an arbitrary signal or irregular in nature. Noise sources must be portrayed by a probability density function (the most widely recognized probability density function is Gaussian,[16]) as they have amplitudes that change haphazardly with time, so it is regularly determined in root mean square worth (RMS).

Noise can either be overlaid on the circuit by outside sources or produced inside in the amplifier, from its related detached parts.

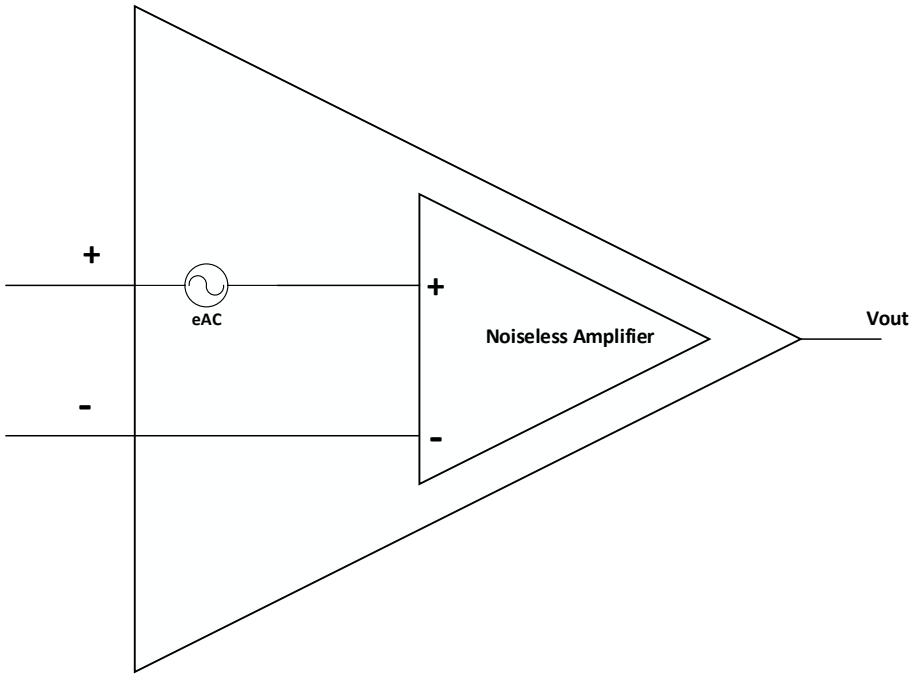

Figure 2.7: Noise model of CMOS amplifier circuit [16]

There are various sorts of noise in electronic circuits, for example, thermal noise, flicker noise, avalanche noise, white noise, and shot noise. Thermal noise is the most operative noise constraint in the CMOS electronic circuits as it dominates noise's value existing in the CMOS electronic circuit [17].

The input noise voltage hotspot for CMOS differential enhancer circuits overwhelms the noise impact as the input ports have genuine high input resistances (gate terminal of the MOSFETs). The noise model for this situation can be communicated by just a single voltage source at the noninverting input port of the amplifier as depicted in fig 2.7.

2.6 CONCLUSION:

The OFCC circuit is a capable current mode device in place of it consolidates the whole current mode device features. It provided the following advantages:

1) Wide input voltage and current ranges,

2) Huge precision in voltage and current transfer (unity gain and zero offset),

3) Extensive voltage and current transfer bandwidths,

4) Huge open loop trans-impedance gain (ideally infinite open loop trans-impedance gain and

5) Low power dissipation.

CHAPTER – 3

OPERATIONAL FLOATING CURRENT CONVEYOR

3.1 INTRODUCTION

In this chapter, operational floating current conveyor (OFCC) CMOS based implementation and characteristics are explained. The operational floating conveyor (OFCC) originally introduced by Toumazou, Payne, and Lidgey has three variants [4]. Here variant number two of [4] is realised and using that instrumentation amplifier is proposed.

3.2 OFCC (OPERATIONAL FLOATING CURRENT CONVEYOR):

One of the most versatile block is OFCC due to its availability of both high and low output and input impedance terminals. OFCC is a basically four terminal port block in addition one terminal is also provided. Input port X is low resistance port making it appropriate for current sensing purposes and input port Y is high resistance suitable for voltage applications. The output terminal Z+ is a high impedance current output terminal and the terminal marked as W is the low impedance output voltage. Voltage follower action persists at the input side i.e. ideally $V_x = V_y$ and current follower action exists at the output side i.e. ideally $I_z = I_w$. The port matrix equation is given below:

$$\begin{pmatrix} I_Y \\ V_X \\ V_W \\ I_{Z+} \\ I_{Z-} \end{pmatrix} = \begin{pmatrix} 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 0 \\ 0 & Z_t & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 \\ 0 & 0 & -1 & 0 & 0 \end{pmatrix} \begin{pmatrix} V_Y \\ I_X \\ I_W \\ V_{Z+} \\ V_{Z-} \end{pmatrix}$$

3.2.1 CMOS based implementation:

The CMOS based usage of OFCC are given in [4]. This subsection depicts the CMOS usage used to approve various proposition in the work. Reproductions are done utilizing usage plot [4] of fig. 3.2. It utilizes a positive type current transport (CCII+), a transimpedance amplifier circuit (Z_t) and a current follower. The CMOS schematic of OFCC [4] dependent on this implementation plan is delineated in Fig. 2.3. It uses coordinated or matched transistor sets (M1 and M2), (M3 and M4), (M10 and M15) and (M11, M12 and M14).

Seeing the saturation region of the considerable number of transistors, the working of the circuit might be explained as pursues. Port X pursues voltage of W port through transistors (M1 - M7) which structure CCII+. The cross coupled current mirror framed by transistors (M16 - M21) give negative current transfer from W port to Z-port. Voltage at port W is delivered by augmentation of current information at X port with transimpedance gain (Z_t) given by enhancer framed by transistors M8 - M13. The arrangement of transistors (M10, M12, M14 and M15) structures current follower and gives current action between ports W and Z+.

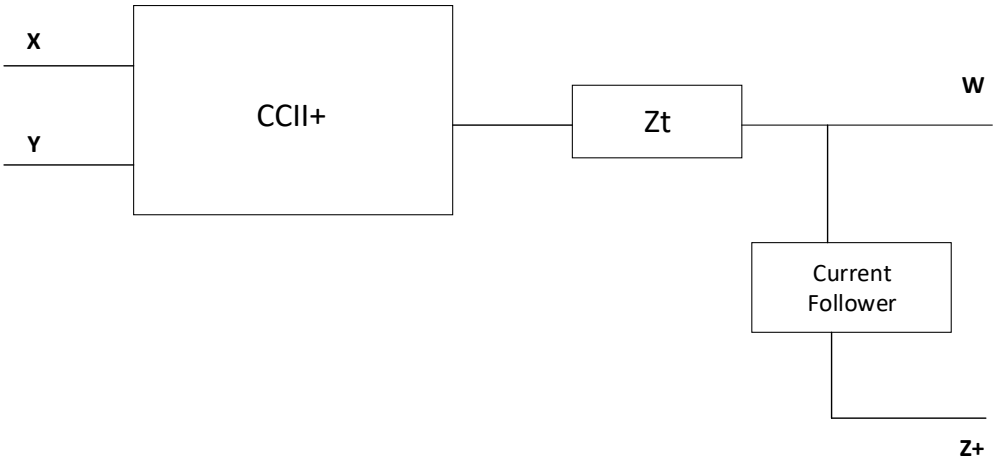

Fig 3.1 Block Diagram of OFCC with Current conveyor II and current follower

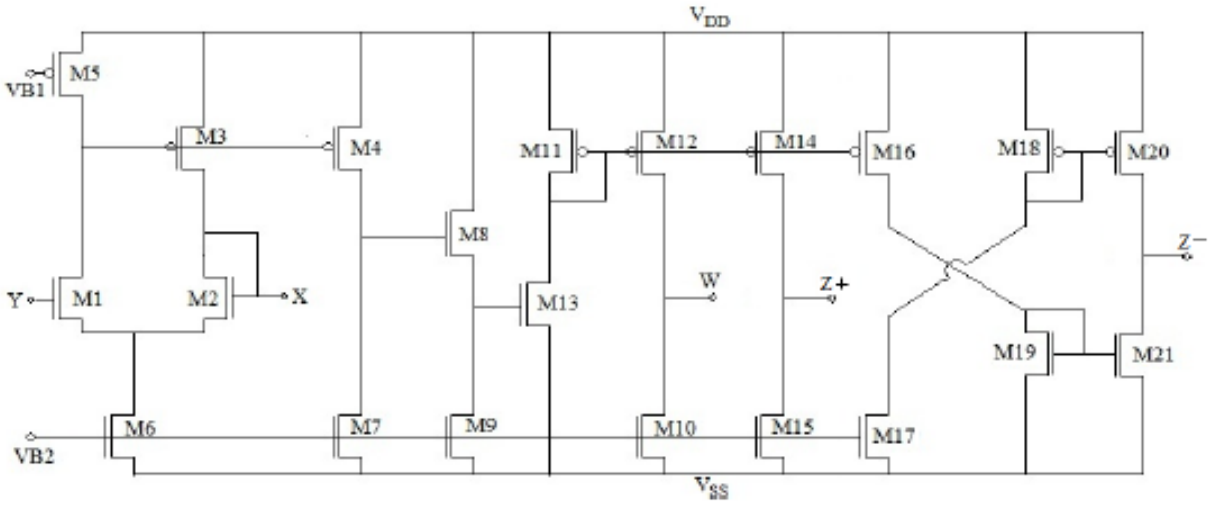

Fig 3.3 CMOS Implementation of OFCC [4]

For verification of CMOS based OFCC block, PSPICE simulations are carried out using the 0.5 μm CMOS technology node parameters. W/L parameters of PMOS and NMOS are given table. The power supplies used for this block are V_{DD} and V_{SS} as + 1.5 V and – 1.5 V. The biasing voltages applies are of bias voltage V_{B1} and V_{B2} of +0.8 V and -0.8 V.

Table 3.1 W/L parameters [4]

Transistors	**W/L (in μm)**
M1, M2	50/1
M3, M4, M11, M12, M14, M18, M16, M20	50/2.5
M5, M7, M10, M15, M17, M19, M21	20/2.5
M6, M8	40/2.5
M9, M13	100/2.5

3.2.2 SIMULATION RESULTS:

1) Voltage Transfer Plot:

The frequency response of the voltage transfer characteristics of OFCC is shown in fig 3.3. is simulated in PSPICE OR-Cad. The voltage transfer characteristics shows the voltage follower action exists between terminal Y and X. The voltage transfer value is around 0.99. This deviation from unity gain is due to the voltage tracking error (ε_V) discussed earlier**.**

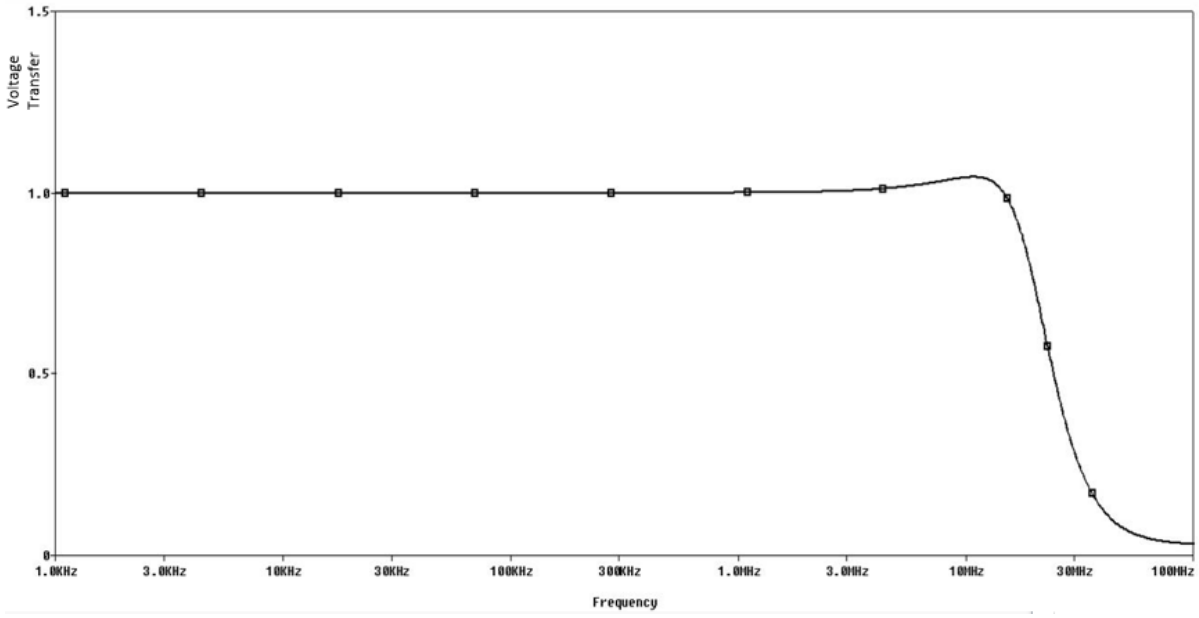

Fig3.3 Frequency response of Voltage Transfer Action of OFCC

2) Current Transfer Plot:

The frequency response of the current transfer characteristics of OFCC is shown in fig 3.4. is simulated in PSPICE OR-Cad. The current transfer characteristics demonstrate the current follower action between terminal W and Z. It is discovered that current transfer value is 0.99 which is less than unity due to the current tracking error (ε_i).

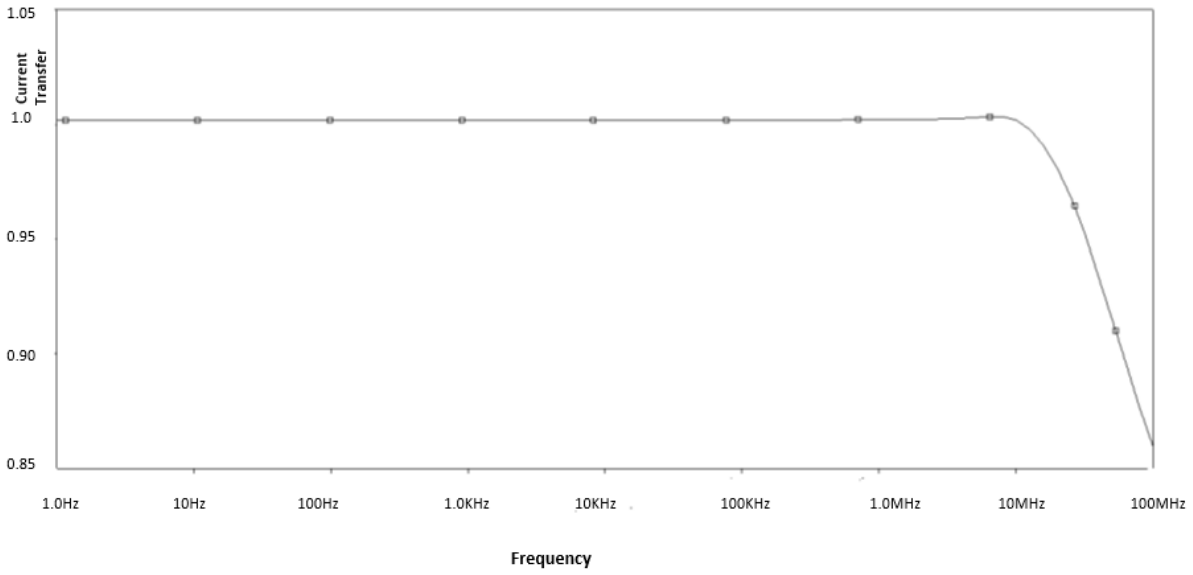

Fig 3.4 Frequency response of Current Transfer Action of OFCC

CHAPTER – 4

PROPOSED INSTRUMENTATION AMPLIFIERS

4.1 INSTRUMENTATION AMPLIFIER:

An instrumentation amplifier enables an engineer to modify the addition of an amplifier circuit without changing more than one resistor esteem. It is a superior circuit solving the low input resistance problem of the difference amplifier.

Instrumentation amplifier block diagram shown in fig 4.1 consists of two cascaded stages. In the first stage, two inputs are applied to the two current amplifier or voltage amplifier blocks and the output amplified by these blocks will be differenced and then applied to the second stage comprising of another current amplifier or voltage amplifier which gives the final output of instrumentation amplifier. The advantage is that it does not required input resistance matching making it ideal to use in many fields like biomedical [18], power sensor applications [19], automotive transducers etc. Also, it offers additional features like very high input resistance, less noise, very high CMRR (common mode rejection ratio) and high open loop gain. Instrumentation amplifier is a stable and controlled circuit can be simply adjusted by varying the gain value.

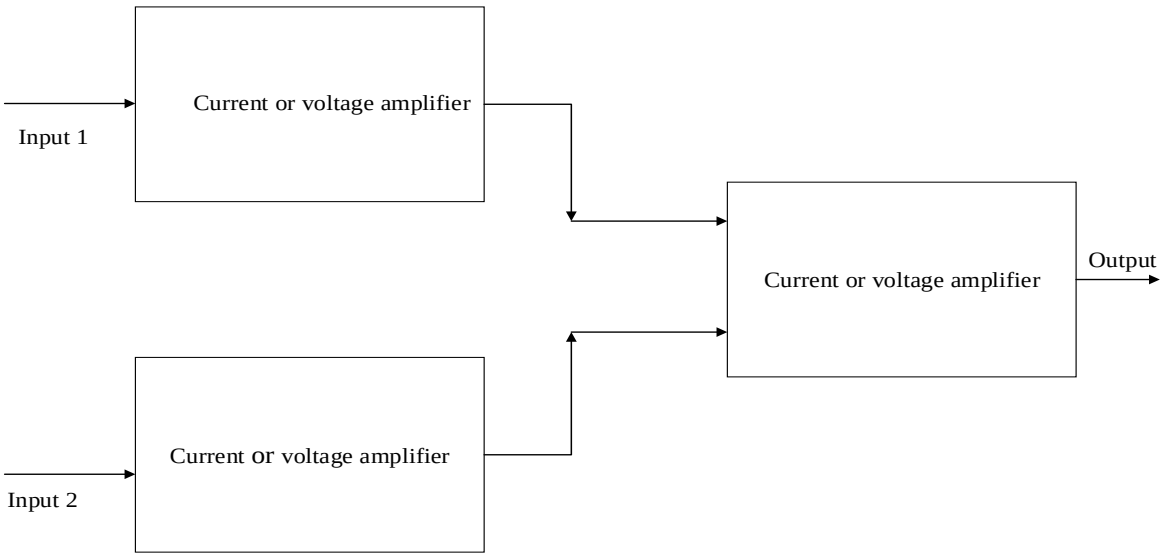

Fig 4.1 Block Diagram of Instrumentation Amplifier

4.2 PROPOSED INSTRUMENTATION AMPLIFIERS:

4.2.1 Proposed TAM Instrumentation Amplifier:

This section depicts the implementation of the proposed Trans-admittance Instrumentation Amplifier (TAM IA) using OFCC block. The OFCC used in the realisation of proposed TAM IA consists of two stages containing three OFCC blocks and three resistors. In the first stage there are two OFCC's shown in fig 4.2 and one resistor R1. The Z terminal of first OFCC is connected to X terminal of second OFCC to provide more control over current I_3. In the second stage a single OFCC (OFCC3) is used with two resistors R2 and R3. OFCC3 depicts the basic current amplifier topology and the output current produced is proportional to the current produced at the first stage.

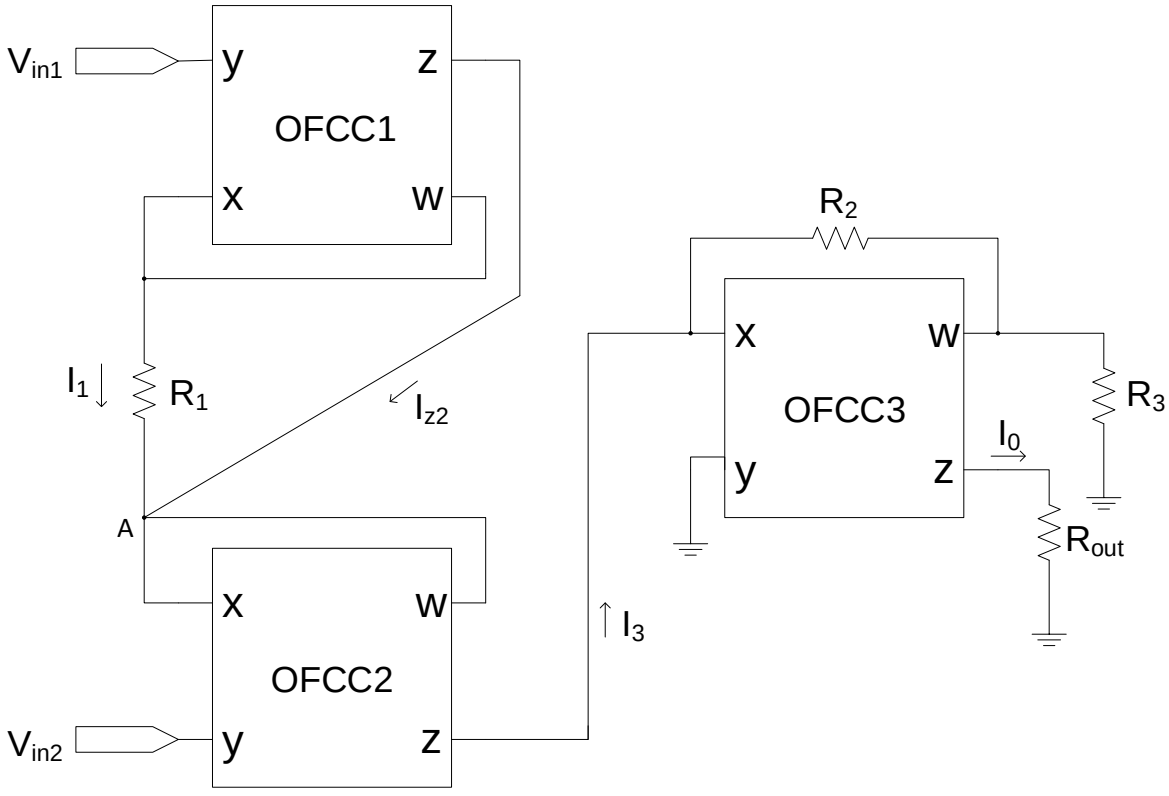

Fig 4.2 Proposed TAM Instrumentation Amplifier

4.2.1.1 Ideal Study of proposed circuit:

Let Vin1 and Vin2 are the two input voltage signals applied at the Y ports of both the OFCC1 and OFCC2 of first stage. From the port matrix of OFCC we know that Vx = Vy i.e. voltage follower action at the input terminals and Iz = Iw i.e. current follower action at the output terminals. Let the voltage produced at the terminals X1 of OFCC1 and X2 of OFCC2 are Vx1 and V_{x2} such that

$$V_{x1} = V_{in1}$$

$$V_{x2} = V_{in2}$$

By routine analysis, current through the resistor R_1 between two terminals of X_1 and X_2 can be given by:

$$\frac{I_1=(V_{in1}-V_{in2})}{R1} \quad (1)$$

At node A, applying KCL law,

$$I_{w2} = I_{z1} + I_1 \quad (2)$$

Also,

$$I_1 = I_{z1} \quad (3)$$

Now,

$$I_{w2} = 2I_1 \quad (4)$$

$$I_{z2} = I_{w2} \quad (5)$$

$$I_{z2} = 2*I_1$$

$$I_3 = 2\frac{(V_{in1}-V_{in2})}{R_1} \quad (6)$$

From second stage OFCC behaving as a current amplifier, the relationship between output and input is given by:

$$\frac{I_{w3}}{I_3} = \left(1 + \frac{R_2}{R_3}\right) \quad (7)$$

From equation (6) and (7)

The output current is given by:

$$I_{w3} = 2\left(\frac{V_{in1}-V_{in2}}{R_1}\right)\left(1+\frac{R_2}{R_3}\right) \quad (8)$$

Differential Amplifier ideally is given by:

$$A_d = \frac{I_0}{V_{in1}-V_{in2}} \quad (9)$$

$$A_d = \frac{2}{R_1}\left(1+\frac{R_2}{R_3}\right) \quad (10)$$

4.2.1.2 Non-Ideal Study of proposed circuit:

The proposed circuit response deviates from the original response due to nonidealities effects comprises of tracking errors and parasitic effects.

By considering tracking errors effects, we get

$V_{x1} = \beta_1 V_{in1}$

$V_{x2} = \beta_2 V_{in2}$

So current through the branch resistor R1 is given by nodal analysis:

$$I_1 = \frac{\beta_1 V_{in1}-\beta_2 V_{in2}}{R_1} \quad (11)$$

By considering parasitic effects, current at terminal Z_1 of OFCC is:

$$I_{Z2} = \alpha_1\left(\frac{\beta_1 V_{in1}-\beta_2 V_{in2}}{R_1}\right)\varepsilon_1(s) \quad (12)$$

Where,

$$\varepsilon_1(s) = \frac{1}{1+sC_{p1}R_1}$$

Similarly, Current output of first stage I_3 is:

$$I_3 = \alpha_2\,(I_1 + I_{z2})\varepsilon_2(s)$$

From equation (11) and (12)

$$I_3 = \alpha_2 \left[\frac{\left(\beta_1 V_{in1} - \beta_2 V_{in2}\right)}{R_1} + \alpha_1 \left(\frac{\beta_1 V_{in1} - \beta_2 V_{in2}}{R_1}\right)\varepsilon_1(s)\right]\varepsilon_2(s)$$

$$I_3 = \alpha_2 \left[\left(\frac{\beta_1 V_{in1} - \beta_2 V_{in2}}{R_1}\right)\{1 + \alpha_1\varepsilon_1(s)\}\right]\varepsilon_2(s)$$

$$I_3 = \frac{1}{R_1}\left[\left(\beta_1 V_{in1} - \beta_2 V_{in2}\right)\{\alpha_2 + \alpha_1\,\alpha_2\,\varepsilon_1(s)\}\right]\varepsilon_2(s) \qquad (13)$$

Now from second stage:

$$\frac{I_{w3}}{I_3} = \left(1 + \frac{R_2}{R_3}\right)\varepsilon_3(s)$$

Where

$$\varepsilon_2(s) = \frac{1}{1 + sC_{p2}R_1}$$

$$\varepsilon_3(s) = \frac{1}{1 + sC_{p3}R_2}$$

Also, tracking error of OFCC3 gives

$$I_0 = \alpha_3\, I_{w3}$$

$$I_0 = \alpha_3 I_3 \left(1 + \frac{R_2}{R_3}\right)\varepsilon_3(s) \qquad (14)$$

From eq (13) and (14)

$$I_0 = \frac{1}{R_1}\left(1 + \frac{R_2}{R_3}\right)\left[\left(\beta_1 V_{in1} - \beta_2 V_{in2}\right)\alpha_3\{\alpha_2 + \alpha_1\,\alpha_2\,\varepsilon_1(s)\}\right]\varepsilon_2(s) * \varepsilon_3(s)$$

(15)

If,

$$\alpha_1 = \alpha_2 = \alpha_3 = \beta_2 = \beta_1 = 1$$

Above equation becomes

$$I_0 = \frac{1}{R_1}\left(1 + \frac{R_2}{R_3}\right)\left[(V_{in1} - V_{in2})\{1 + \varepsilon_1(s)\}\right]\varepsilon_2(s)\,\varepsilon_3(s)$$

$$\frac{I_0}{(V_{in1} - V_{in2})} = \frac{1}{R_1}\left(1 + \frac{R_2}{R_3}\right)[\{1 + \varepsilon_1(s)\}]\varepsilon_2(s)\,\varepsilon_3(s)$$

(16)

Different parameters can be calculated to verify the proposed work are:

1) Common mode gain (A_{CM}):

   If Vin1 = Vcm and Vin2 = Vcm, then the common mode gain (A_{CM}) is computed as:

$$A_{CM} = \frac{I_0}{(V_{in1} - V_{in2})}$$

$$\frac{I_o}{V_{CM}} = \frac{1}{R_1}\left(1 + \frac{R_2}{R_3}\right)\left[\left(\beta_1 - \beta_2\right)\alpha_3\,\{\alpha_2 + \alpha_1\,\alpha_2\,\varepsilon_1(s)\}\right]\varepsilon_2(s)\,\varepsilon_3(s)$$

(17)

$$A_{CM} = \frac{1}{R_1}\left(1 + \frac{R_2}{R_3}\right)\left[\left(\beta_1 - \beta_2\right)\alpha_3\,\{\alpha_2 + \alpha_1\,\alpha_2\,\varepsilon_1(s)\}\right]\varepsilon_2(s)\,\varepsilon_3(s)$$

(18)

2) Differential mode gain (A_d):

   For calculating differential mode gain we can represent $V_{in1} = V_{CM} + \Delta$ and $V_{in2} = V_{CM} - \Delta$, where V_{CM} is common mode voltage and Δ is differential voltage. Differential mode gain (A_d) is computed as following:

$$A_d = \frac{I_0}{2\Delta}$$

$$I_o = \frac{1}{R_1}\left(1 + \frac{R_2}{R_3}\right)\left[\left(\beta_1 + \beta_2\right)\Delta + \underbrace{\beta_1 V_{CM} - \beta_2 V_{CM}}\right]\{\alpha_2 + \alpha_1\,\alpha_2\,\varepsilon_1(s)\}\,\alpha_3\,\varepsilon_2(s)\,\varepsilon_3(s)$$

Rejected for calculating A_d

$$I_o = \frac{1}{R_1}\left(1 + \frac{R_2}{R_3}\right)\left(\beta_1 + \beta_2\right)\{\alpha_2 + \alpha_1\,\alpha_2\,\varepsilon_1(s)\}\,\alpha_3\,\varepsilon_2(s)\,\varepsilon_3(s) * \Delta$$

$$\frac{I_o}{2\Delta} = \frac{1}{2R_1}\left(1 + \frac{R_2}{R_3}\right)\left(\beta_1 + \beta_2\right)\{\alpha_2 + \alpha_1\,\alpha_2\,\varepsilon_1(s)\}\,\alpha_3\,\varepsilon_2(s)\,\varepsilon_3(s)$$

(20)

3) Common Mode Rejection Ratio (CMRR):
   CMRR is computed as the ratio of differential gain (A_d) and common mode gain (A_{CM}):

$$CMRR = \frac{A_d}{A_{CM}}$$

$$CMRR = \frac{\beta_1 + \beta_2}{2(\beta_1 - \beta_2)} \quad (21)$$

4.2.1.3 Simulation Results:

4.2.1.3.1 Differential Gain plot for the proposed circuit:

The plot for the differential gain of the IA is shown in Figure 4.3. The plot is taken by applying the input value of 5mV at Y2 terminal of one OFCC block, and 0mV at the Y terminal of other OFCC block for different gains and corresponding resistance values are shown in the plot.

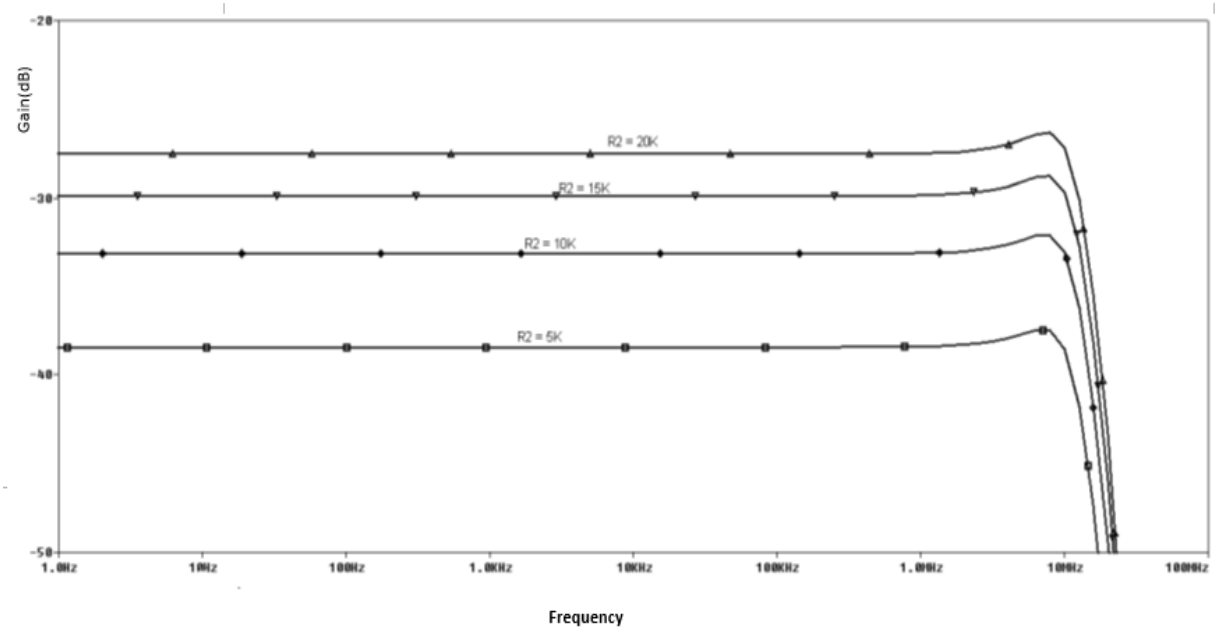

Fig 4.3 Differential Gain plot for the proposed circuit

The differential gain is plotted by varying the value of resistor R2 in fig 4.3.

4.2.1.3.2 CMRR plot for the proposed circuit:

The CMRR is plotted for output stage gains of 5,10,15 and 20 by varying the value of resistance R2 and resistance with value R1= 1k, R3 = 1k and Rout = 1k in Fig 4.4

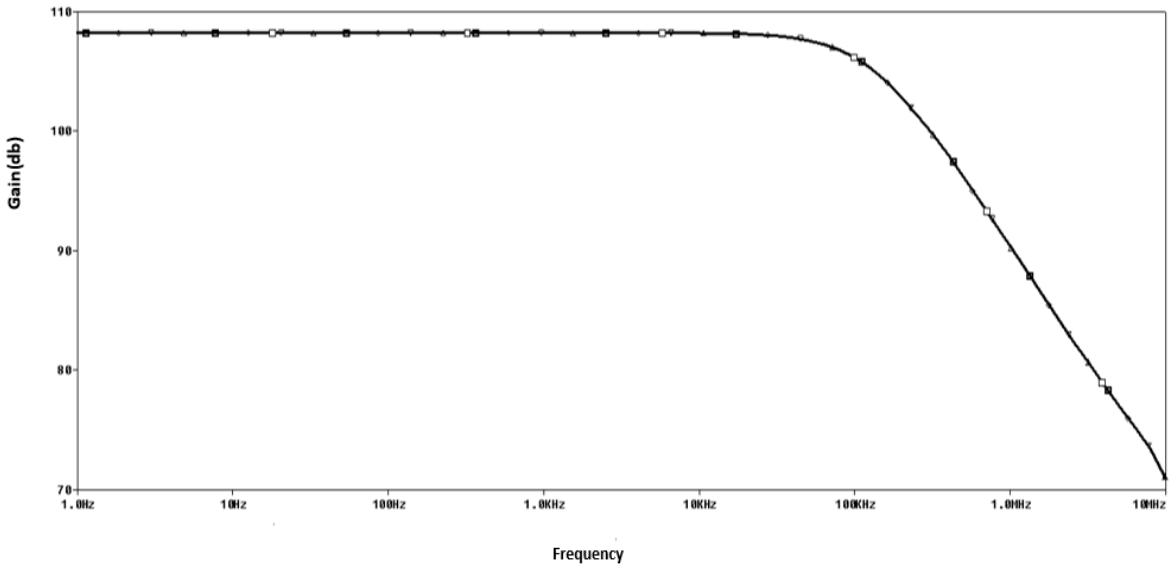

Fig 4.4 CMRR plot

The CMRR plot for a proposed circuit is given in fig 4.4. The CMRR value from the plot comes out to be 108.18 db.

4.2.2 Proposed Transimpedance Instrumentation Amplifier (TIM IA)

This section depicts the implementation of the proposed Transimpedance Instrumentation Amplifier (TIM IA) using OFCC block. The OFCC used in the realisation of proposed TIM IA consists of two stages containing three OFCC blocks and six resistors. In the first stage there are two OFCC's shown in fig 4.5 and with resistor R_1 connected between terminal W_1 and terminal X1, also between terminal W2 and terminal X2.

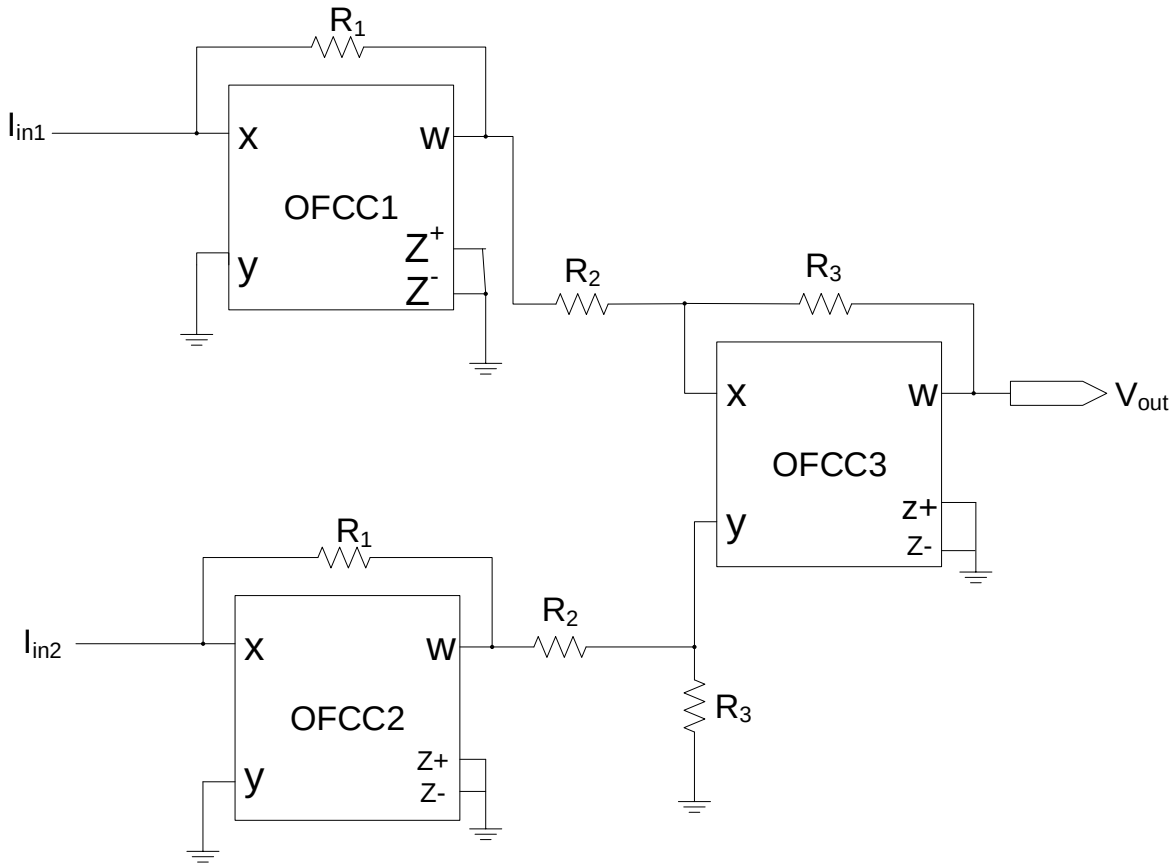

Fig 4.5 Proposed TIM Instrumentation Amplifier

The OFCC1 and OFCC2 both are transresistance amplifier providing voltages proportional to the input current. Now the 2nd stage OFCC3 works as the difference amplifier with the two inputs coming from the output of OFCC1 and OFCC2 blocks. The output voltage produced at the 2nd stage OFCC3 is proportional to the input current, thus depicting TIM mode IA.

4.2.2.1 Ideal Analysis of the proposed circuit:

Let Iin1 and Iin2 are the two input current signals applied at the X1 and X2 ports of both the OFCC1 and OFCC2 of first stage of fig4.5. From the port matrix equation of OFCC we know that $V_x = V_y$ i.e. voltage follower action at the input terminals and $I_z = I_w$ i.e. current follower action at the output terminals. The voltage produced at the terminals W1 of OFCC1 and W2 of OFCC2 are Vw1 and Vw2 such that these voltages are used as input of the difference amplifier OFCC3

From fig 4.5 the output voltage of OFCC1 and OFCC2 produced at Vw1 and Vw2 are:

$$V_{W1} = I_{in1}\, R_1 \tag{22}$$

$$V_{W2} = I_{in2}\, R_1 \tag{23}$$

Now using routine analysis,

The output voltage V_o of the difference amplifier OFCC3 is computed as:

$$V_{out} = \frac{R_3}{R_2}\, R_1\, (I_{in1} - I_{in2}) \tag{24}$$

Differential Gain A_d is given by:

$$A_d = \frac{V_{out}}{(I_{in1} - I_{in2})} \tag{25}$$

$$\frac{V_{out}}{(I_{in1} - I_{in2})} = \frac{R_3}{R_2}\, R_1 \tag{26}$$

4.2.2.2 Non-Ideal Analysis:

Non ideal analysis means considering the parasitic effects and tracking errors of OFCC block. Ideally OFCC has a very high open loop transimpedance gain but in general the impedance Z_t is a frequency reliant on parameter. Considering single pole model,

$$Z_t(s) = \frac{Z_{t0}}{1 + s/\omega_{tc}}$$

Taking into account the parasitic effects, voltages at different nodes can be computed as:

$$V_{W1} = I_{in1}\, R_1\, \varepsilon_1(s) \tag{27}$$

$$V_{W2} = I_{in2}\, R_1\, \varepsilon_2(s) \tag{28}$$

Where,

$$\varepsilon_1(s) = \frac{1}{1 + sC_1R_1}$$

$$\varepsilon_2(s) = \frac{1}{1 + sC_2R_2}$$

Also,

$$V_{out} = \frac{R_3}{R_2} R_1 (I_{in1} - I_{in2}) \varepsilon_3(s)$$

(30)

Where

$$\varepsilon_3(s) = \frac{1}{1 + sC_3R_3}$$

Considering tracking errors and parasitic effects,

$$V_{out} = \frac{R_3}{R_2} [\left(\beta_3 I_{in2} R_1 \varepsilon_2(s)\right) - I_{in1} R_1 \varepsilon_1(s)] \varepsilon_3(s)$$

$$V_{out} = \frac{R_3}{R_2} R_1 [\left(\beta_3 I_{in2} \varepsilon_2(s)\right) - I_{in1} \varepsilon_1(s)] \varepsilon_3(s)$$

Considering only tracking errors,

$$V_{out} = \frac{R_3}{R_2} (\beta_3 V_{W2} - V_{W1})$$

From eq (22) and (23)

$$V_{out} = \frac{R_3}{R_2} (\beta_3 I_{in2} R_1 - I_{in1} R_1)$$

$$V_{out} = \frac{R_3}{R_2} R_1 (\beta_3 I_{in2} - I_{in1})$$

(31)

Considering $\beta_3 = 1$ above equation will become:

$$V_{out} = \frac{R_3}{R_2} R_1 (I_{in2} - I_{in1})$$

$$\frac{V_{out}}{(I_{in1} - I_{in2})} = \frac{R_3}{R_2} R_1$$

Differential Gain, A_d is given by:

$$A_d = \frac{R_3}{R_2} R_1 \qquad (32)$$

Also, putting $I_{in1} = I_{cm} - \Delta$ and $I_{in2} = I_{cm} + \Delta$ in equation (31)

$$V_{out} = \frac{R_3}{R_2} R_1 \left(\beta_3 I_{CM} + \beta_3 \Delta - I_{CM} + \Delta\right)$$

$$V_{out} = \frac{R_3}{R_2} R_1 \left(\beta_3 I_{CM} - I_{CM} + \beta_3 \Delta + \Delta\right)$$

$$V_{out} = \frac{R_3}{R_2} R_1 \left(\beta_3 I_{CM} - I_{CM} + (\beta_3 + 1)\Delta\right)$$

Rejected for calculating A_d

$$V_{out} = \frac{R_3}{R_2} R_1 \left(\beta_3 + 1\right)\Delta$$

$$\frac{V_{out}}{\Delta} = \frac{R_3}{R_2} R_1 \left(\beta_3 + 1\right)$$

$$\frac{V_{out}}{2\Delta} = \frac{R_3}{2R_2} R_1 \left(\beta_3 + 1\right)$$

Differential gain (A_d) is also calculated as:

$$A_d = \frac{V_{out}}{2\Delta}$$

So,

$$A_d = \frac{R_3}{2R_2} R_1 \left(\beta_3 + 1\right) \quad (33)$$

And common gain A_{CM} can be computed as by considering:

$$I_{in1} = I_{in2} = I_{cm}$$

So, equation (31) becomes:

$$V_{out} = \frac{R_3}{R_2} \left(\beta_3 I_{CM} R_1 - I_{CM} R_1\right)$$

$$\frac{V_{out}}{I_{CM}} = \frac{R_3}{R_2} \left(\beta_3 R_1 - R_1\right) \quad (34)$$

Common gain A_{CM} can be computed as:

$$A_{CM} = \frac{V_{out}}{I_{CM}}$$

$$A_{CM} = \frac{R_3}{R_2}(\beta_3 R_1 - R_1)$$

$$A_{CM} = \frac{R_3}{R_2} R_1 (\beta_3 - 1) \quad (35)$$

CMRR is calculated as:

$$CMRR = \frac{A_d}{A_{CM}}$$

$$CMRR = \frac{(\beta_3 + 1)}{2(\beta_3 - 1)} \quad (36)$$

4.2.2.3 SIMULATION RESULTS:

4.2.2.3.1 Differential Gain plot for the proposed circuit:

The plot for the differential gain for the proposed TIM based IA is shown in Fig 4.6. The plot is taken by applying the input value of 1μA at X terminal of one OFCC block, and 0μA at the X terminal of other OFCC block for different gains and corresponding resistance values are shown in the plot.

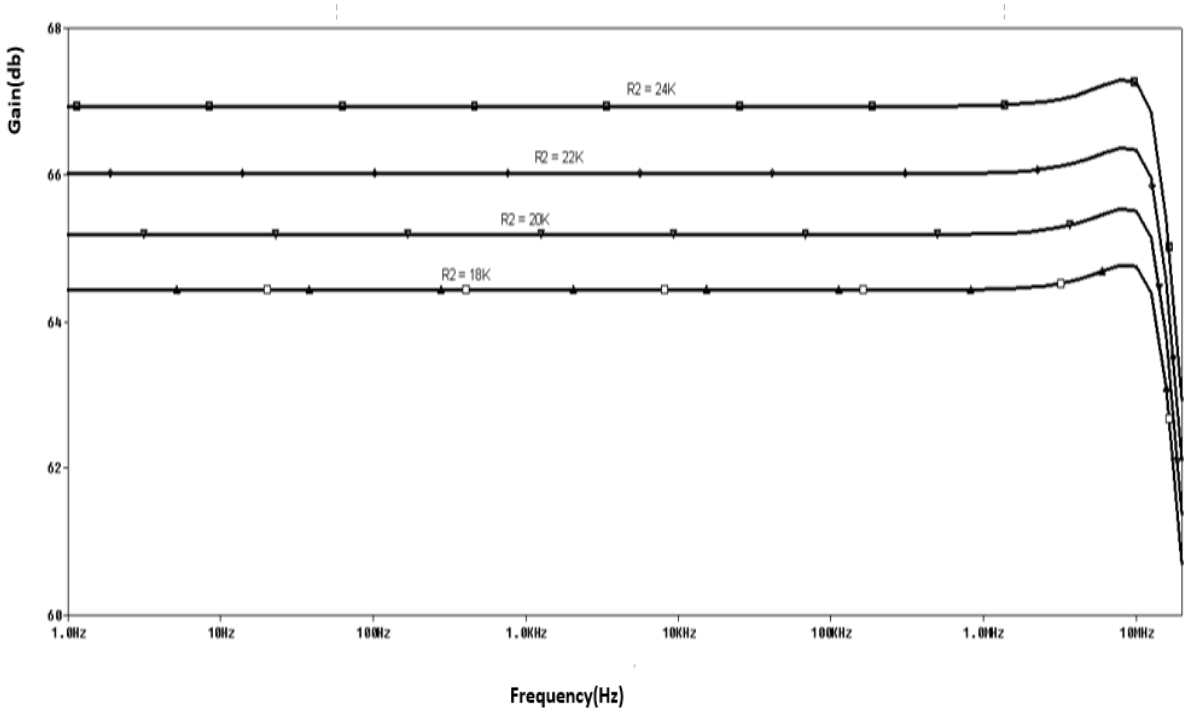

Fig 4.6 Differential Gain Plot for the proposed circuit

The different gain values observed at the different resistor R2 values of 18k, 20k,22k and 24k are 66.93db, 66.00db, 65.19db, 64.44db.

4.2.2.3.2 CMRR plot for the proposed circuit:

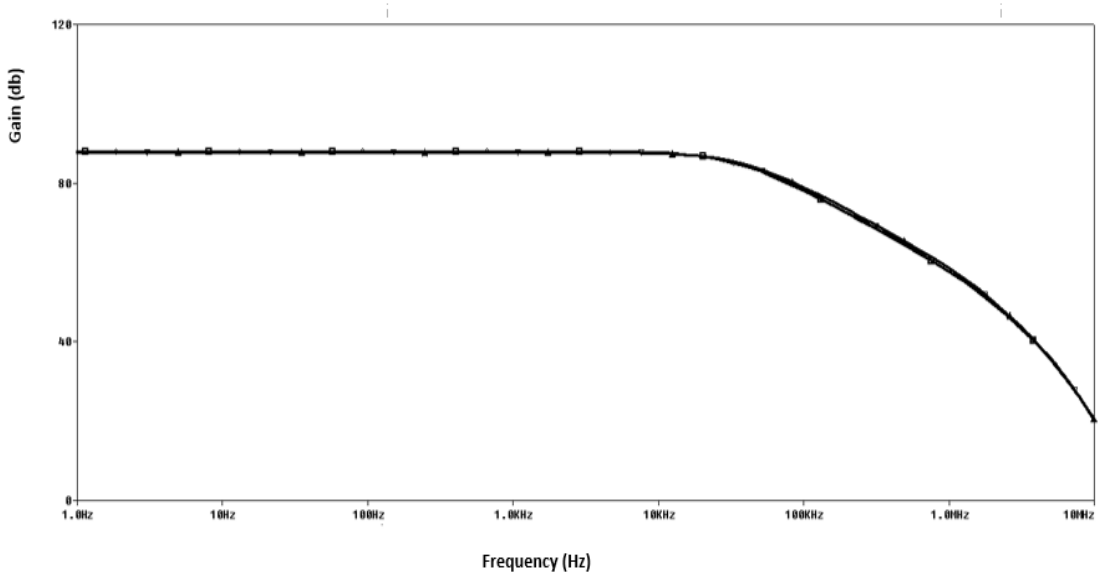

Fig 4.7 CMRR Plot

The CMRR is plotted with component values of R1 = 2k, R3 =2k and R2 = 18k, 20k, 22k, 24k in fig 4.7. The CMRR value from the plot comes out to be 88.04 db.

CHAPTER-5
CONCLUSION

5.1 CONCLUSION:

An integrated CMOS based OFCC has been modelled and simulated. The circuit architecture uses a low-drive CCII+ as a first gain stage, a transconductance amplifier as second gain stage, and a current follower as the output stages. The simulation results show that the proposed OFCC has the following advantage: it offers wide bandwidth with low power consumption.

Applications based on OFCC such as Instrumentation Amplifier is proposed. Two new topologies have been proposed, one is TAM based IA and the subsequent one is TIM based IA. It is simulated using Or-Cad Capture tool with 0.5μm CMOS technology. Hence, the responses are verified.

5.1 FUTURE SCOPE:

The IC usage of the exhibited circuits is the most normal future issue. The circuit exhibited in this Thesis depended on at least 0.5 μm CMOS technology. The circuit may further be overhauled utilizing nano meter CMOS innovation. This would make the dynamic components dependent on these structures appropriate for use in portable communication applications along these lines boundlessly expanding their adaptability and acknowledgment. The bandwidth of the proposed circuits can also be improved later on by utilizing bandwidth enhancement procedures.

To aggregate up, there is still a great deal of degree in analog signal processing to exploit the focal points of elite all active dynamic components in the up and coming advancements for further research.

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