DESIGN OF HIGH STATIC NOISE MARGIN TRANSMISSION GATE BASED SRAM CELL

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I, **TARTEEL OSMAN ABDELMOULA IBRAHIM, Roll No. 2K20/VLS/26** student of M.Tech. VLSI Design & Embedded System, hereby declare that the major project II titled DESIGN OF HIGH STATIC NOISE MARGIN TRANSMISSION GATE BASED SRAM CELL " which is submitted by me to **Prof. NEETA PANDEY**, Department of Electronics and Communication, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of degree of master of technology is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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I hereby certify that the Major project II Dissertation titled "DESIGN OF HIGH STATIC NOISE MARGIN TRANSMISSION GATE BASED SRAM CELL" is a bonafide record of work done by **TARTEEL OSMAN ABDELMOULA IBRAHIM, Roll No. 2K20/VLS/26** at Delhi Technological University, New Delhi for the award of the degree of Master of Technology. This project was carried out under my supervision and has not been submitted anywhere else, either in part or full, for the award of any other degree or diploma to the best of my knowledge and belief.

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Abstract

SRAM cell is the most commonly used embedded memory in System-On-Chip; it occupies the largest portion of the chip area and dominates the total chip power. Reducing the power consumption of the SRAM cell and enhancing the static noise margin is very important to improve system performance, efficiency and reliability.

The conventional 6T SRAM cell suffers from the read destruction problem. In this report a new 10T SRAM cell design based on transmission gates is represented. The proposed design uses a separate read path, thus no voltage division between the storage node and the bitline, the read stability is maintained as equal as the hold stability.

The conventional 6T SRAM cell has two bitlines for read and write operation, The proposed SRAM cell operates by charging / discharging of a single bit-line (BL) during read and write operations thus results in reduction of dynamic power consumption.

The proposed design has been simulated at 32 nm technology node using LTSPICE software tool. The effect of process corners on read and write access time have been studied. N-curve method is used to analyze the static stability and stability parameters like SINM, SVNM, WTI and WTV have been measured and the effect of variation of power supply and temperature on stability have been studied .

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List of symbols and abbreviations

SRAM	Static Random Access Memory
DRAM	Dynamic Random Access Memory
ICs	Integrated Circuits
CMOS	Complementary Metal Oxide Semiconductor
LSI	Large Scale Integration
SOC	System On Chip
T	Transistor
WL	Word Line
RL	Read Line
BL	Bit Line
BLB	Bit Line Bar
WWL	Write Word Line
RWL	Read Word Line
WBL	Write Bit Line
RBL	Read Bit Line
VTC	Voltage Transfer Characteristic
SA	Sense Amplifier
CR	Cell Ratio
PR	Pull Ratio
WAS	Write Assist Signal
WASB	Write Assist Signal Bar
RAS	Read Assist Signal
SNM	Static Noise Margin

RSNM	Read Static Noise Margin
WSNM	Write Static Noise Margin
SVNM	Static Voltage Noise Margin
SINM	Static Current Noise Margin
WTV	Write Trip Voltage
WTI	Write Trip Current
PVT	Process Voltage Temperature

Chapter 1

INTRODUCTION

Systems on Chip embed many complicated functions which necessitate an enhanced memory capacity. Static Random Access Memory SRAM is the commonly deployed when prime considerations are low power and/or bandwidth. The SRAM does not need periodically refreshing, unlike the DRAM, SRAM stores each bit by using a bistable latch circuit. The data stored in SRAM will be lost when the memory is not powered up therefore falls under volatile memory. Interfacing SRAM is easier and more truly random access than modern DRAM.

A significant portion of the entire chip area is captured by the On-chip cache memory also it shares a large percentage of power consumption which is increasing with advances technologies. The power consumption in the SRAM depends on the number of the cell accessing times, using the SRAM at high frequencies made the cell power hungry as DRAM, also at full bandwidth many watts are consumed by some ICs. The SRAM memory which is used in moderately clocked microprocessors, consumes lesser power and power consumption can be nearly negligible in idle state, typically in range of a little micro watts.

The SRAM has different modes of operation write, read, and hold. For SRAM to operate it should have read stability and write ability, in advanced technologies, these two conditions are difficult to satisfy because of variability in CMOS transistor parameters.

1.1History and trends of SRAM cell

The exemplary memory for logic LSI is the SRAM memory. Because it draws less power at hold mode and runs fast as logic circuits. One more benefit is that the manufacturing process is fully compatible with the basic CMOS process. So no additional processing cost is needed. These features cannot be obtained with other memories like Flash memories and DRAM.

Nowadays about 40% of the LSI area is taken by an array of SRAM memory cells, thus the characteristics of the SRAM array limits the parameters of the logic Large Scale Integration, these parameters like power supply, size of the chip, and operating speed. Therefore, a good SRAM cell design and good SRAM array

design is imperative to achieve little cost, less power, and reliable LSI circuits with high performance.

Many kinds of SRAM cell topologies are proposed, used, and developed.

The high-R cell which is illustrated in Fig. 1.1 was the first cell proposed as a low power 4K SRAM cell. In this cell, a poly-silicon layer with high-resistance has been used as the inverter load. The cell size was smaller because the bulk PMOS is not used, since the resistance of the poly-silicon layer is about 10^{12}, the cell current at standby mode was drastically reduced to 10^{-12} per cell. This cell has been used widely in low power LSI SRAM memory and high density from 4K to 4M bit. The drawback of this cell is that it works at low voltage. At low voltages of less than 1.5V, the voltage of the cell node must be charged to level equals to the supply voltage throughout the write operation. Because the resistance of the poly-silicon load is high, the required time for charging the high node to the supply voltage is quite large, the cell cannot work with supply voltage less than 1.5V.[1]

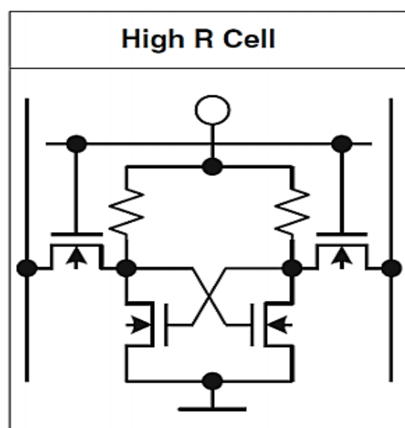


Fig. 1.1 High-R cell [1]

The six transistors 6T cell topology, also known as full CMOS cell which is illustrated in Fig. 1.2 was employed as logic LSIs memory rather than the high-R cell. The 6T cell is bigger than the high-R because it uses bulk PMOS transistors as inverter load; the 6T cell process is same as the logic process. In addition, in this cell the nodes voltages are pulled up fast by using the PMOS transistors, thus the cell works at lower power supply than the high R. Therefore, as technology advances reducing the voltage made the cell unavoidable for logic LSI.

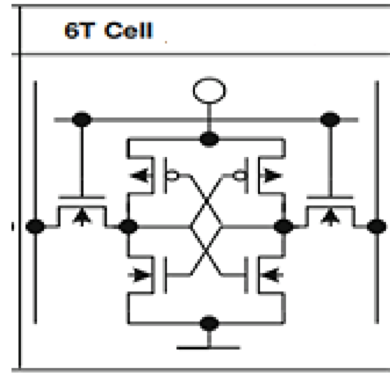


Fig. 1.2 The 6T cell [1]

Fig.1.3 illustrates the 7T SRAM cell topology which was proposed to enhance the cell stability by breaking the feedback between the back to back connected inverters. This cell is the 6T cell with addition of another pull down NMOS transistor, the added transistor turns OFF in the read mode thus prevents the pull down transistor to discharge to ground.

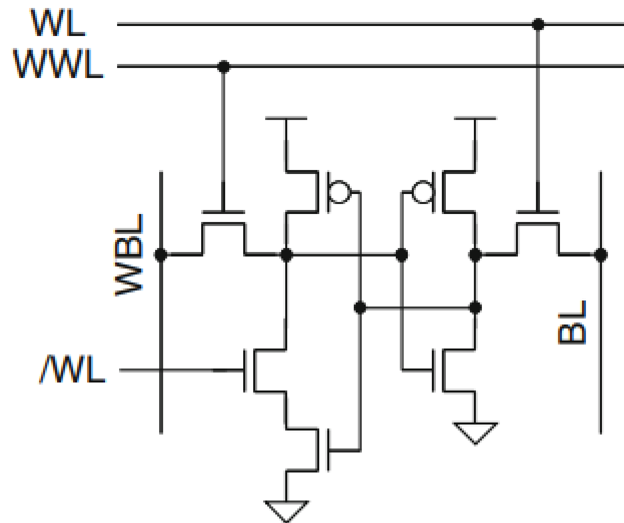


Fig. 1.3 The 7T SRAM cell [1]

Fig.1.4 illustrates the 8T SRAM cell topology which is used widely in advanced CMOS devices. It consist of the conventional 6T with addition of a pair of NMOS transistors which provides an isolated read port that has separate RWL and single RBL . The isolated read port doesn't allow the read current to flow through the cell thus improves the RSNM and make it as same as the hold SNM. This cell can be used as single and dual port cell.

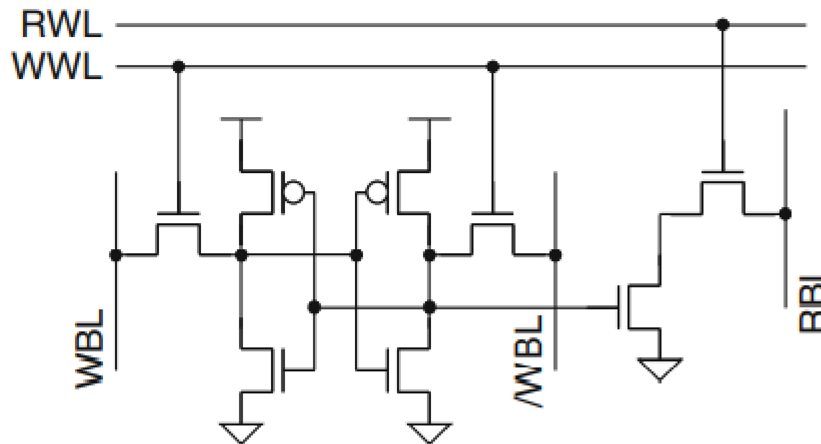


Fig. 1.4 The 8T SRAM cell [1]

Another SRAM cell topology is illustrated in Fig. 1.5, it consists of the conventional 6T cell with addition of four NMOS transistors. This cell uses differential write bitline and read bitline pairs and separate word line for read and write operations. This topology also can be used as single and dual port SRAM cell.

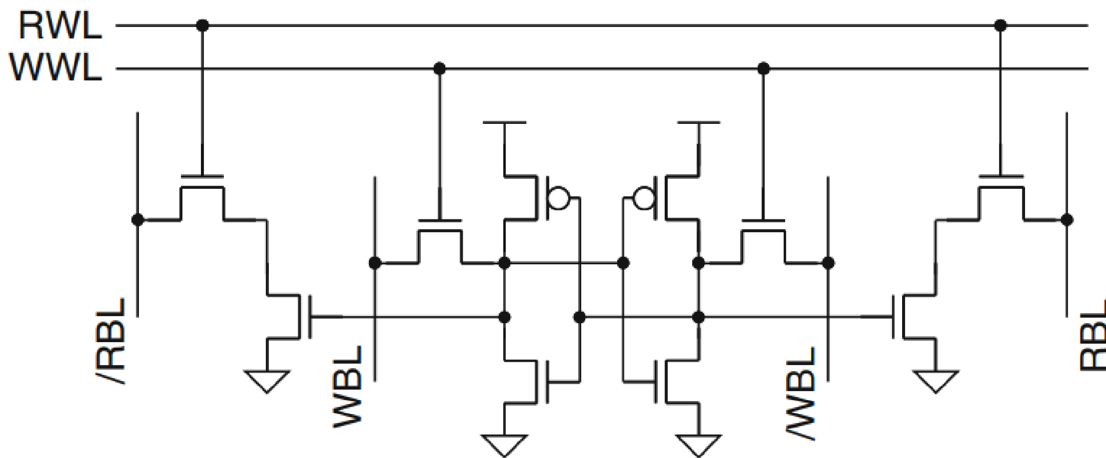


Fig. 1.5 The 10T SRAM cell [1]

The FINFET technology has been used in designing of SRAM cells, in this technology the gate of the device controls the device channel from back and front sides thus suppress the short channel effects , the channel in FINFET devices is fully depleted therefore the channel dopant fluctuation is reduced and the Vth variation is suppressed .

The FINFET SRAM provides high SNM, the worst value of static noise margin is better than the bulk transistor SRAM. [1].

1.2 Motivation

SRAM occupies a significant portion of the entire chip space in the modern processors and SOCs. Because of their faster performance than DRAM, SRAM blocks are commonly employed as cache memories in processors.

The CMOS continuous scaling affects the SRAM stability which results in read disturbs and write failure. Read destruction is the major challenge in designing SRAM cells, the 6T SRAM cell read destruction problem can be overcome by using the new 10 T SRAM that uses transmission gates instead of the NMOS access transistors. Here the data storage node and the bitline are separated throughout the read mode and thus improving the stability.

1.3 The Objective

The aim of the work is to design a reliable SRAM cell that enhances the read operation stability and eliminates the read disturbance, and attains read static noise margin same as hold static noise margin.

1.4 Organization of the report

The report has been organized into 4 chapters. Chapter 1 introduces the SRAM cell. It also includes the history and trends of SRAM cell, motivation and objective of the report. Chapter 2 represents the architecture of the 6 T SRAM cell, discuss the working principle of the cell and the concept of static stability analysis. In chapter 3 the architecture of the new 10T SRAM cell is demonstrated, it explains the cell operation also it represents the process, voltage and temperature variations and stability analysis of the new cell. Chapter 4 concludes the report.

Chapter 2
THE 6T SRAM CELL

The 6T cell is widely employed. This chapter describes the 6T SRAM cell operation and methods used to compute various parameters.

2.1. The Conventional 6T SRAM cell

2.1.1. Basic structure

The 6T SRAM cell that is illustrated in Fig. 2.1. The transistors of the 6T SRAM cell should be sized properly to allow read and write operations. The data is to be stored in 6T SRAM in cross coupled inverters (M1-M2; M3-M4) having '0' and '1' stable states. Apart from the two inverters it uses M5 and M6 transistors which are used to access the stored data and perform read/write operation. The WL enables the access transistors.

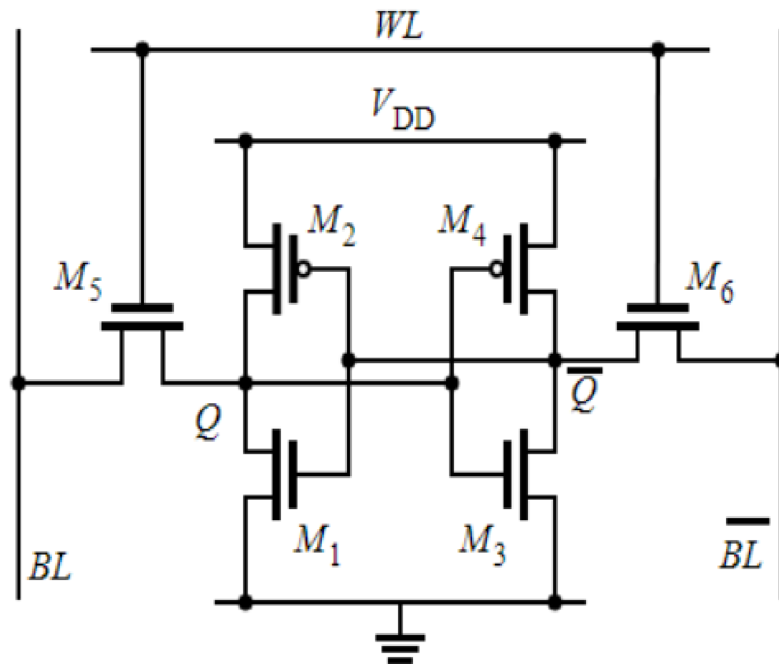


Fig. 2.1 The 6T SRAM cell [2]

2.1.2. Working of the 6T SRAM cell

There are three operation modes for the SRAM cell; the first one is standby, the second is read, and the third is write. In standby the cell holds the data, the data is read in read mode while the contents are updated in write mode. It is worth mention that the cell shall have “readability” and "write ability” features. The operation in these modes is described below [2, 3, 4]:

1. Standby mode:

In this mode WL is kept at low (0) which makes M5 and M6 off thus the cell is disconnected from the bit lines. As power supply remains on, the cross-coupled inverters will retain the data and the current drawn from power supply is known as standby or leakage current.

2. Read mode:

In this mode, both BL and BLB are pre-charged to VDD then the WL is enabled, one of the bitlines will discharge through the access and pull down transistors. The cell stores ‘0’ if the BL discharges and ‘1’ if the BLB discharges. The voltages of the bitlines potentials are sensed by a sense amplifier which generates the output. To avoid the read operation failure, the node which stores 0 must not rise above the second inverter trip point; this can be ensured by making the cell ratio to be large enough. In general, depending on the desired noise margin and application the cell ratio is between 1.25 and 2.5.

In equation (2.1) the discharging Current across M1 and M5 are equated.

SNM is related to the Cell Ratio (CR). The ratio of the drive and access transistors specifies the CR. Increasing CR results in increasing the SNM and thus the current increases [2]

$$\beta n, M5\{(VDD - VQB - Vtn)VDSATn - (V^2DSATn)/2\} = \beta n, M1\{(VDD - Vtn)VQB - (V^2QB)/2\} \quad (2.1)$$

Equation (2.1) can be simplified to equation (2.2)

$$VQB = VDSATn + CR(VDD - Vtn) - \sqrt{V^2DSATn + (1 + CR) + CR^2\,(VDD - Vtn)^2} \quad (2.2)$$

CR is known as β or cell ratio and is represented in equation (2.3)

$$Cell\ Ratio = \frac{\frac{W1}{L1}}{\frac{W5}{L5}} \quad (2.3)$$

3. Write mode:

In write mode, the data to be written is applied to the BL and its complement to the BLB then WL is enabled. The data is written , Q and QB nodes voltages are changed.

The ratio of load and access transistors defines the Pull Ratio PR. The PR value must be lower to ensure a successful write operation, generally it equals to ‘1’, lower PR value can be obtained by making the access transistor stronger but the read SNM will reduce if the access transistor width is increased. It is found that as the Pull Ratio increases the cell SNM will increase. Equation (2.4) equates the current flowing across M4 and M6 in for successful write operation. [2].

$$\beta n, M6\{(VDD - Vtn)VQ - (V^2Q)/2\} \; = \beta p, M4\{(VDD - Vtn)VDSATp - (V^2\,DSATp)/2\} \tag{2.4}$$

This equation (2.4) can be rewritten as follows:

$$VQ = VDD - Vtn - \sqrt{(VDD - Vtp)^2 \, 2\frac{\mu p}{\mu n} \, PR \;\; (VDD - Vtp)\, VDSATp - \frac{V^2VDSATp}{2}} \tag{2.5}$$

PR is called pull ratio and is represented as in equation (2.6)

$$Pull\,ratio(PR) = (\frac{W4}{L4})/(\frac{W6}{L6}) \tag{2.6}$$

2.2. Sizing of transistors of SRAM cell

For the cell to function properly, read and write stability must be ensured. For the read stability, the cell node between the two transistors M1 and M5 should not flipped , this can be guaranteed by making M1 transistor size greater than M5 When in the write operation, the cell will be overpowered with a new value. The inverters should not overpowered by the high bit lines throughout the read mode. This leads to making M2 transistor size weaker than M5.

2.3 SRAM static data stability

The characteristics of SRAM cell can be defined on the basis of following parameters:

2.5.1. Static Noise Margin SNM

SRAM works in the sub-threshold region reducing both the access energy and the leakage power. SRAM must be able to work at sub-threshold voltages compatible with the combinational logic sub-threshold. This scaling promises to be continuous, which leads to sub-threshold operation of SRAMs. When the cell holds the data, the word line is low. Thus disables the access transistors. For SRAM to properly retain its data, the cross-coupled inverters should keep a bistable operating points; SNM is the best measure for inverters ability to keep their states.

The SNM is the maximum noise voltage that can be entered at the inverters input without affecting the cell data. [5,6,7,8].

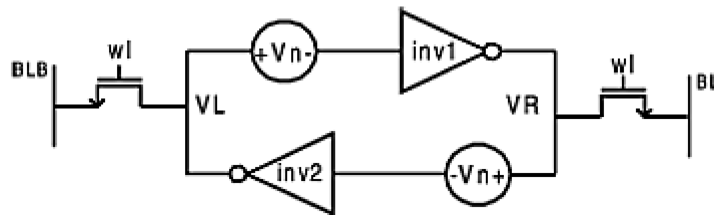


Fig. 2.2 Setup of the conventional 6T SRAM Cell for SNM [8]

Fig. 2.3 illustrates the widely used method to graphically represent the SNM of a cell holding data. Inverter 2 VTC and its inverse are plotted. The two-lobed curve is known as butterfly curve that is used in determination of the SNM.

The largest square side's length which can be included within the butterfly curve lobes defines The SNM [2,5]. Consider the case where two DC voltage noise sources V_N are given at the two internal nodes. When increasing the value of V_N from 0, VTC-1 of inverter1 moves downward and the VTC of inverter2 goes right. When the two curves moved by a value equals to the SNM they intersect at two points.

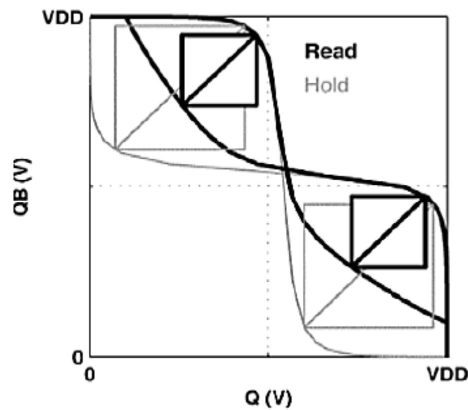


Fig 2.3 Butterfly curve for SNM [9]

CR, PR and, VDD values typically have significant roles in the SNM analysis. SNM value must be high to achieve high stability. For calculating the static noise margin, the current of the drain is considered and is defined in equation 2.7 and 2.8 [2,5]

$$ID = \frac{1}{2}\beta(VGS - VT)^2 \quad (2.7)$$

$$ID = \frac{1}{2}\beta\, VDS(VGS - VT - \frac{1}{2}VDS) \quad (2.8)$$

The static noise margin is calculated in saturation and linear region as follow:

$$SNM6T = VT - \left(\frac{1}{K+1}\right)\{\left(\frac{VDD - \frac{2r+1}{r+1}VT}{1 + \left(\frac{r}{k(r+1)}\right)} - \frac{VDD - 2VT}{1 + K\frac{r}{q} + \frac{\sqrt{r}}{q}\left(1 + 2K + \frac{r}{q}K^2\right)}\right)\} \quad (2.9)$$

$$r = ratio = \frac{\beta d}{\beta a} \quad (2.10)$$

$$q = \frac{\beta p}{\beta a} \quad (2.11)$$

$$K = \left(\frac{r}{r+1}\right)\{\sqrt{\frac{r+1}{r+1-\frac{V^2S}{V^2T}}} - 1 \quad (2.12)$$

$$Vs = VDD - VT \quad (2.13)$$

$$Vr = Vs - \left(\frac{r}{r+1}\right)VT \quad (2.14)$$

2.5.2. Read Noise Margin

The cell in the read mode should keep its state. For reading the data BL, BLB and WL are kept at VDD. For calculation of RSNM, the feedback between the two inverters must be broken. Then, the inverter VTC in half circuit is plotted as illustrated in fig 2.4 (V2 vs V1). Then, the butterfly curve is plotted by overlapping Fig. 2.4 VTC with its inverse as shown in Fig 2.5. SNM of the Read operation will be the maximum square side which is included in the butterfly curve. [2,5].

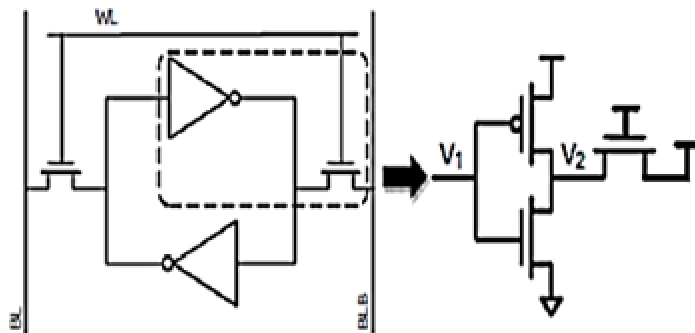


Fig. 2.4 SRAM setup to calculate RSNM

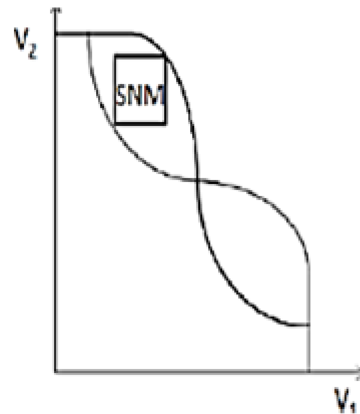


Fig. 2.5 Read butterfly plot [7]

During the read mode, if the Read-SNM reduces the cell will be vulnerable. And the reason for vulnerability is that the BL, BLB, and WL are precharged high when RSNM is calculated. Due to the effect of dividing the voltage between the access and drive transistors, the internal node which is representing zero is pulled up by the access transistor therefore degrades the static noise margin while the reading process happens. The cell state may be changed during the read mode

which leads to wrong data. Figure 2.5 illustrates the VTC plot of the RSNM characteristics and the RM is calculated according to this plot. The RM specifies the read stability.

The stability of SRAM cell decreases as the power supply is reduced thus the leakage current caused by technology scaling increases exponentially. Fig.2.6 compares between the leakage current and the read static noise margin of the 6T cell at different technology nodes.

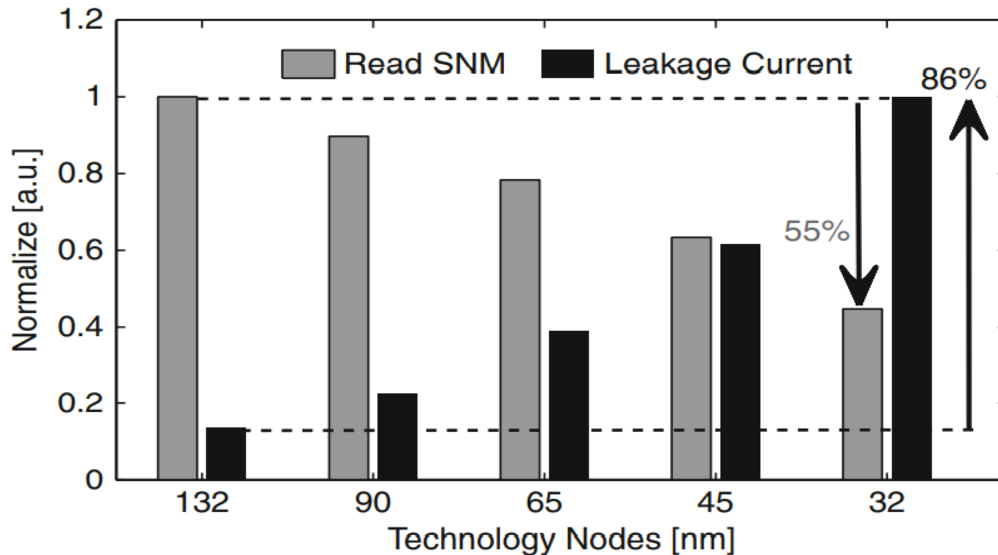


Fig. 2.6 Leakage current and read static noise margin at different technology nodes [10]

Increasing the SNM value increases the read stability. Therefore the cell has good read stability if the RSNM is high. [2, 5, 6].

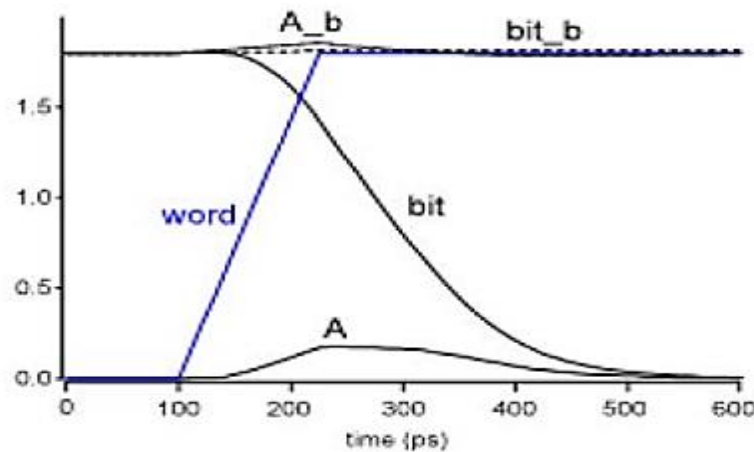


Fig. 2.7 Read Margin from SNM [5]

2.5.3. Write Noise Margin WNM

The nodes Q and QB are swept to obtain the WNM. For writing operation, WL is set at VDD. For calculation of WSNM, the two inverters feedback is broken. The inverters VTCs in half circuit as illustrated in Fig 2.8 are plotted as shown in Fig.2.9. There will be asymmetry in the VTCs because one of the bitlines is driven to VDD while the other to 0. WM measures the write ability and is specified as the minimum voltage in the bit-line that is applied for flipping the cell. The value of WNM relies on the cell design and is calculated from the butterfly curve that is shown in Fig. 2.9 as the largest square side that is included between the two curves. A SRAM cell with low WSNM has poor write ability. [2,10].

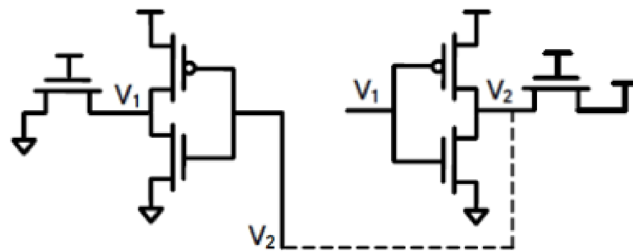


Fig. 2.8 SRAM setup for calculation of WSNM

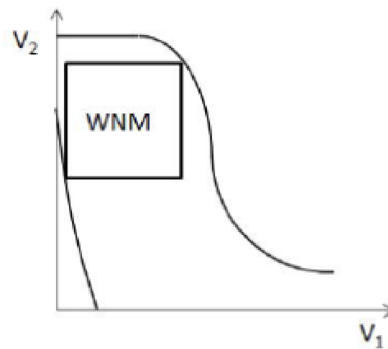


Fig. 2.9 write butterfly plot

The write trip point voltage is an alternative way to determine the write ability of the cell. The maximum voltage on the bitline which is required to change the cell contents is defined as the write trip point voltage and it is calculated from Fig. 2.10 as the difference in voltage between VDD and the largest voltage amount required on the bitline to change Q and QB nodes. Write trip point voltage is equal to WSNM.

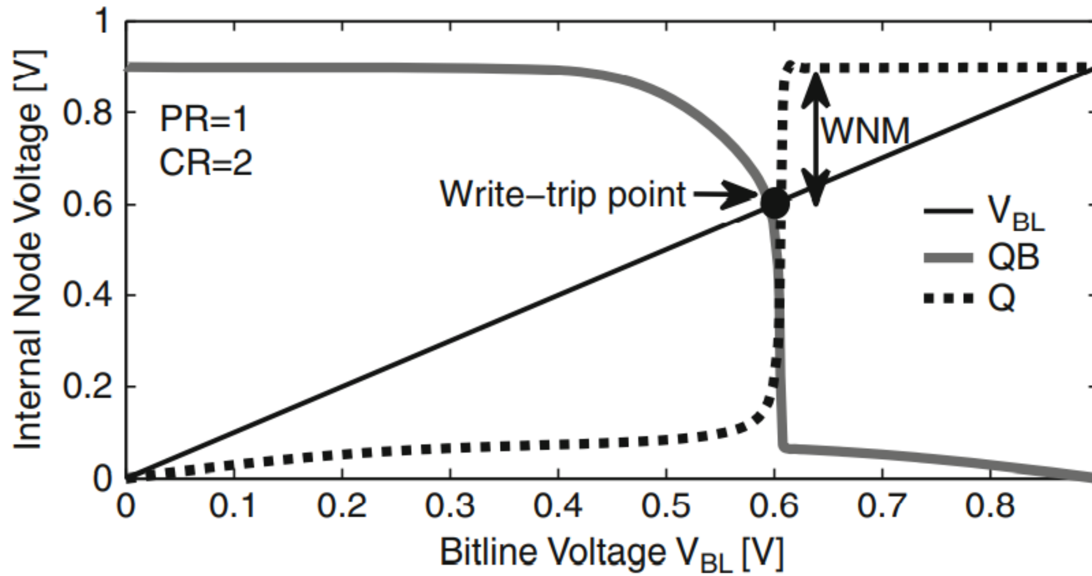


Fig. 2.10 the SRAM cell WNM as voltage trip point [10]

2.5.4. Data Retention Voltage (DRV)

During this mode, the NMOS access transistors are disabled and the supply voltage is lowered to a certain value – DRV to decrease static power consumption. The minimum supply voltage needed to keep the high node in the hold state is defined as DRV. The SRAM cell has two nodes Q and QB to store either 0 value or 1. Then the power supply must be reduced to a certain value that changes the SRAM cell state or keep the contents constant. The power supply is scaled down to DRV value, the VTC of the two inverters will be degraded to a level that the SNM of the cell is zero. DRV value must be larger than the threshold voltage. [6].

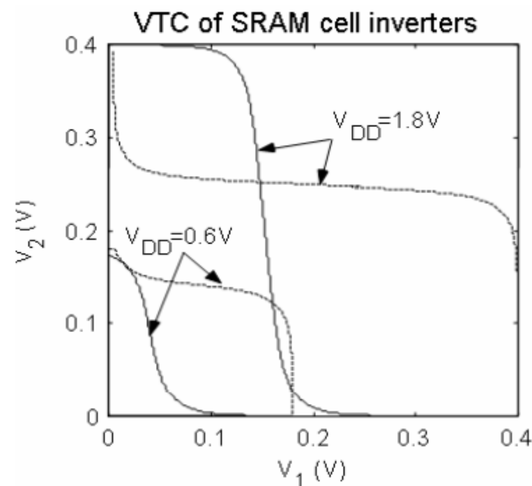


Fig. 2.11 VTC during Data Retention Voltage calculation [6]

2.6. N- CURVE

Several SNM analytical models are developed to improve the design of the cell, predict the influence of changing the parameters on the SNM and evaluate the effect of variations in the intrinsic parameter on the stability of the cell. To enhance the stability, authors proposed and developed several new designs of the SRAM cell. Because the butterfly curves define a maximum square side of the maximum; the cell stability is limited. Another disadvantage is that the automatic inline testers cannot be used to measure the SNM because the SNM must be derived from the butterfly curve by performing mathematical manipulations on the measured data. Also, for write and read stability measurement a separate analysis is needed for each of them, the butterfly curve doesn't give information about the flow of current that is necessary for the analysis of stability.

Static stability analysis can also be done using the N curve approach, this approach gives information about the write ability and the read stability thus allowing the cell to be analyzed completely, it directly gives the cell functional information thus the measured data does not need any mathematical manipulation. [5,6].

To extract the N Curve of the conventional 6T SRAM cell, the setup is illustrated in Fig. 2.11

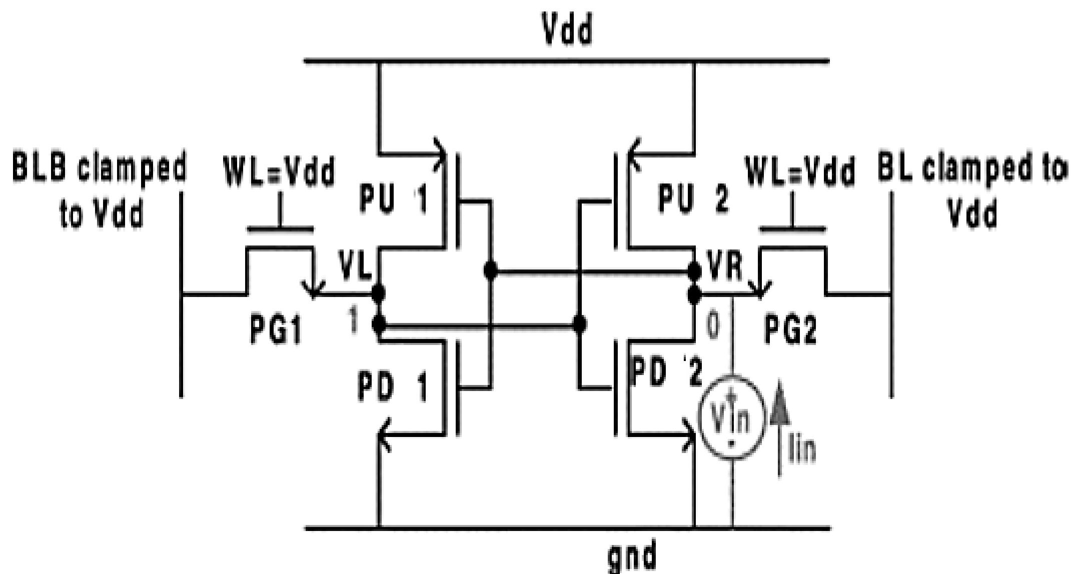


Fig 2.12 Set up for N curve analysis [8]

Assuming that the internal node VL stores 1 and the internal node VR stores 0. By Appling a voltage source Vin at the node VR and sweeping it from 0 to VDD, then the current of the applied source is measured and the relationship between

the Vin and Iin is plotted as illustrated in Fig. 2.12, at A, B, and C, the extracted N curve intersects three times. A and C are the butterfly curve stable points while B is the metastable point. At A, B, and C the current of the voltage source is zero.

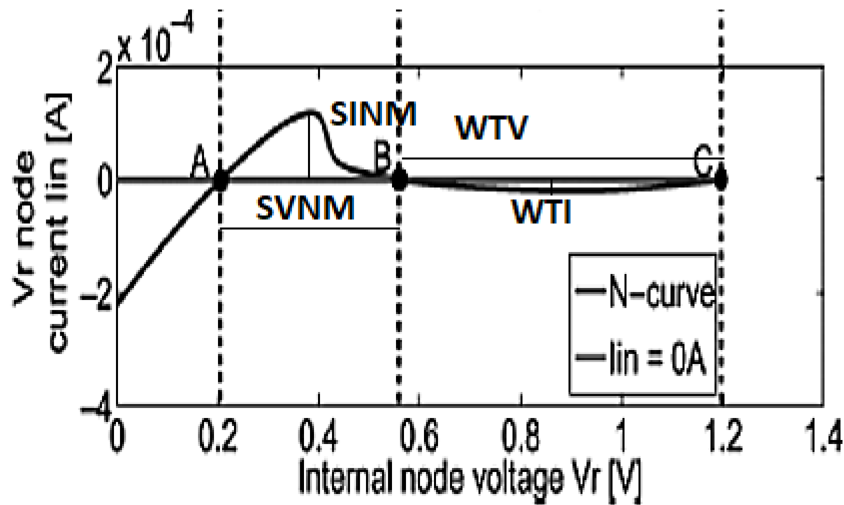


Fig. 2.13 N curve for 6T SRAM cell [8]

When Vin and node VR are at 0 V, the PG2 transistor operation region is saturation velocity and the PD2 is in linear region. The PG2 has drain current greater than the PD2 drain current and according to Kirchoff's current low the difference between the two drain currents enters the source to keep the voltage at node VR at 0 V. When the difference between the two currents equals 0 A (point A). The point A voltage is specified by the pull-down to access transistor ratio. Increasing Vin increases Iin and devices operation regions are remained unchanged up to SINM. The access transistor and pull-down to pull up ratio affect Point B voltage. The pull-down transistor PD2 moves to velocity saturation at SINM, the pull-up transistor PU2 is active and regions of operation of PG2, PD2, and PU2 changed to saturation between SINM and WTI. PG2 and PU2 are in the linear region while PD2 changes from the active to the cut-off region at WTI. The pull up to access transistor determines point C voltage. [10].

2.7. Static Current and Voltage Metrics

By using the N curve, the following parameters determine the cell read stability and write ability. [6].

1. Static voltage noise margin (SVNM)

It is defined as the largest amount of DC voltage noise that can be tolerated at the inverters input before the content of the cell changes and calculated from Fig. 2.12 as the difference in voltage between A and B.

2. Static current noise margin (SINM)

It is the largest amount of DC current injected into the cell before the stored data changes and is calculated from Fig. 2.12 throughout the read operation as the peak value of the sweep source current that is between A and B.

3. The Write Trip Voltage (WTV)

The required drop in voltage to change the cell high node with clamping the two bitlines at VDD is specified as WTV and is calculated from fig. 2.12 as the difference in voltage between B and C.

4. The Write Trip Current (WTI)

It is the required current to write the cell when clamping the two bitlines at VDD and is calculated from fig. 2.12 as the peak value of the sweep source current between B and C.

To attain improved read stability, amount of SVNM, SINM value, and thus the static power noise margin SPNM value must be larger.

To attain improved write ability, WTV amount, the absolute WTI magnitude, and thus WTP amount should be smaller.

Chapter 3

THE PROPOSED 10T SRAM CELL

3.1. Schematic diagram of the proposed cell

The proposed topology of the 10T SRAM cell is depicted in Fig. 3.1. It consists of two back to back connected CMOS inverters (M1, M2, M3, and M4). This connection ensures storing of the data. The cell uses write assist signal WAS and its complement WASB that controls the transmission gate T1 formed by the (M5 and M6) transistors. The access transistor of 6T SRAM cell is replaced by transmission gate T2 (M7 and M8). An isolated read port comprised of T2, M9, and M10 where M9 is controlled by the read assist signal RAS and M10 is controlled by the internal storage node QBAR.

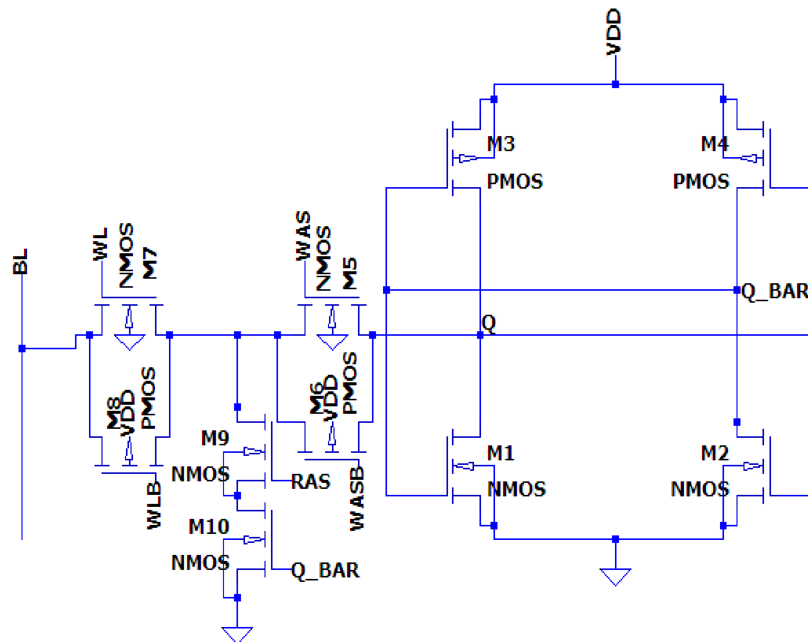


Fig. 3.1 The proposed 10T SRAM cell

3.2. Operation of The proposed 10T SRAM cell

1. Hold mode

During the hold mode the data is maintained as long as the cell is powered up. All control signals are kept low except WLB and WASB are kept high thus isolates

the bitline from the cross coupled inverter and the bitline remains precharged to VDD.

2. Read mode

In this case, WAS and WASB are connected to 0 V and VDD respectively which makes T1 OFF and isolates the storage node Q from the bitline, the read assist signal RAS is activated and the bitline is precharged to VDD followed by turning ON WL. If the stored value is 0, M10 is ON and the bitline will discharge to ground, if the stored value is 1, M10 is OFF and the bitline will remain precharged.

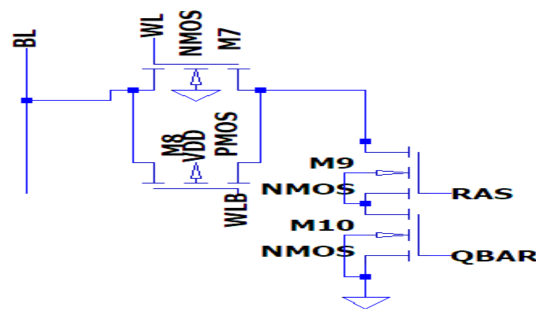


Fig. 3.2 The read path of the proposed cell

3. Write mode

Prior to the write process is performed, read assist signal (RAS) is disabled by setting it at logic low, thereby the transistor M9 is turned OFF, during the write operation BL is precharged to VDD or 0 V according to the data to be written, both the transmission gates T1 and T 2 are switched ON and connected to the BL by setting the control signals WL and WAS at VDD and WLB and WASB at logic low. The BL is charged or discharged.

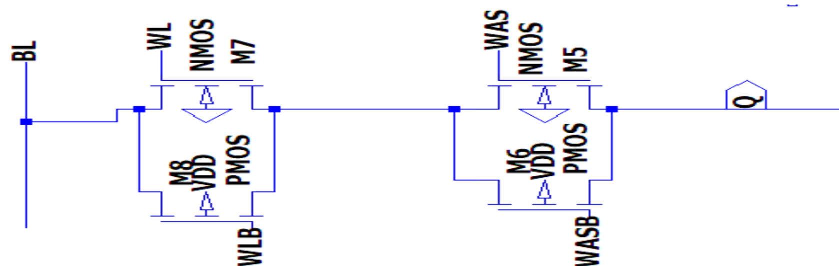


Fig. 3.3 The write path of the proposed cell

3.3. PVT Variations

During the simulation, the designer runs the design at different Process, Voltage, and Temperature corners to ensure that the design operates reliably under variations. These corners are as follow,

1. Temperature-- -40° as Low to 125°C as high,
2. Voltage – variation of ±10% from the nominal value
3. Process-- There are five process corners: FF, TT, FS, SF, and SS. Where T for Typical, S for Slow, F for Fast. The NMOS behavior is represented by the first letter and the PMOS behavior by the second letter. TT, SS, and FF are known as even corners; because the NMOS and PMOS are influenced evenly. In TT corner, the PMOS and NMOS are switched at a moderate speed while in SS the switching of the PMOS and NMOS is slower. In FF corner, the switching of PMOS and NMOS is faster. Scaling increases the process variations [12]. Fig. 3.4 illustrates the process corner

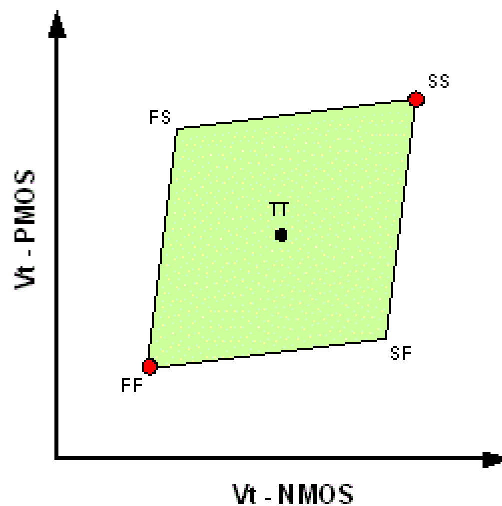


Fig. 3.4 process corners [12]

Running the design at different process corners is not enough; the impact of variability must be assessed through a simulation which is called Monte Carlo. In this simulation a group of simulation schemes are pre-defined and the transistor models physical parameters are set randomly. During each iteration the values of the parameters are changed. The value of a parameter P distribution is approximated as a Gaussian distribution of standard deviation σP and mean value μP. The designer uses these cell parameters representations to set the margins that meet the manufacturing yield target. [13].

3.4. The transient response of the new 10T SRAM cell

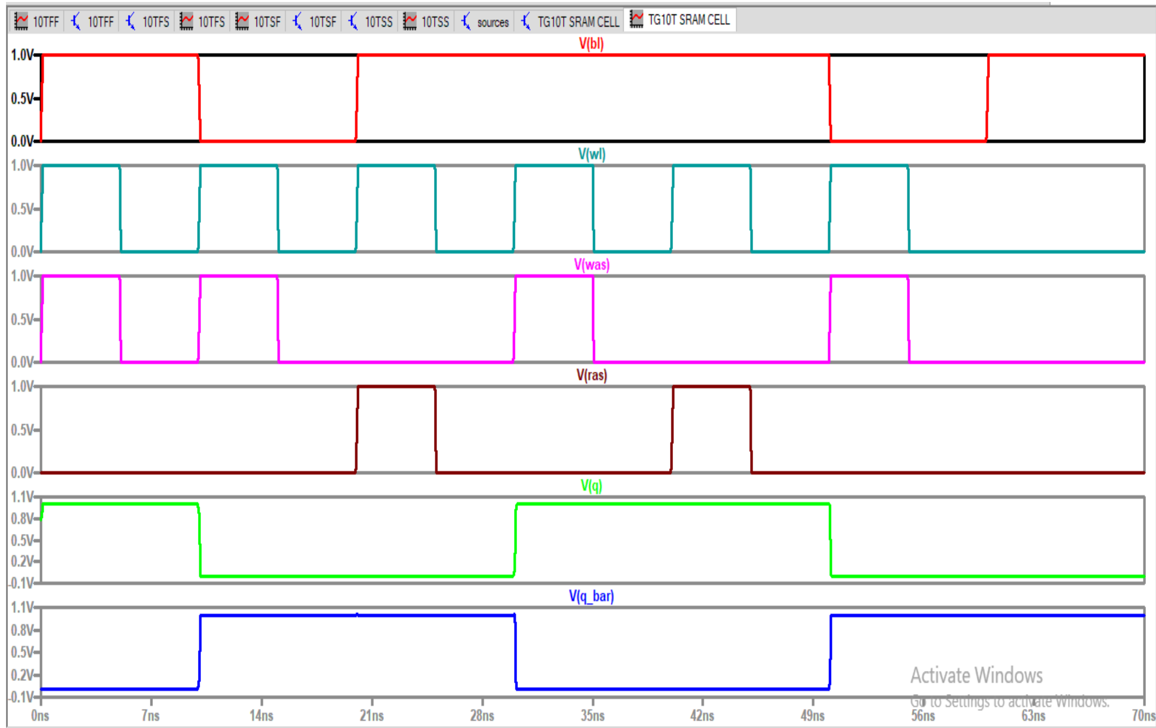


Fig. 3.5 The transient response of the new 10T SRAM cell

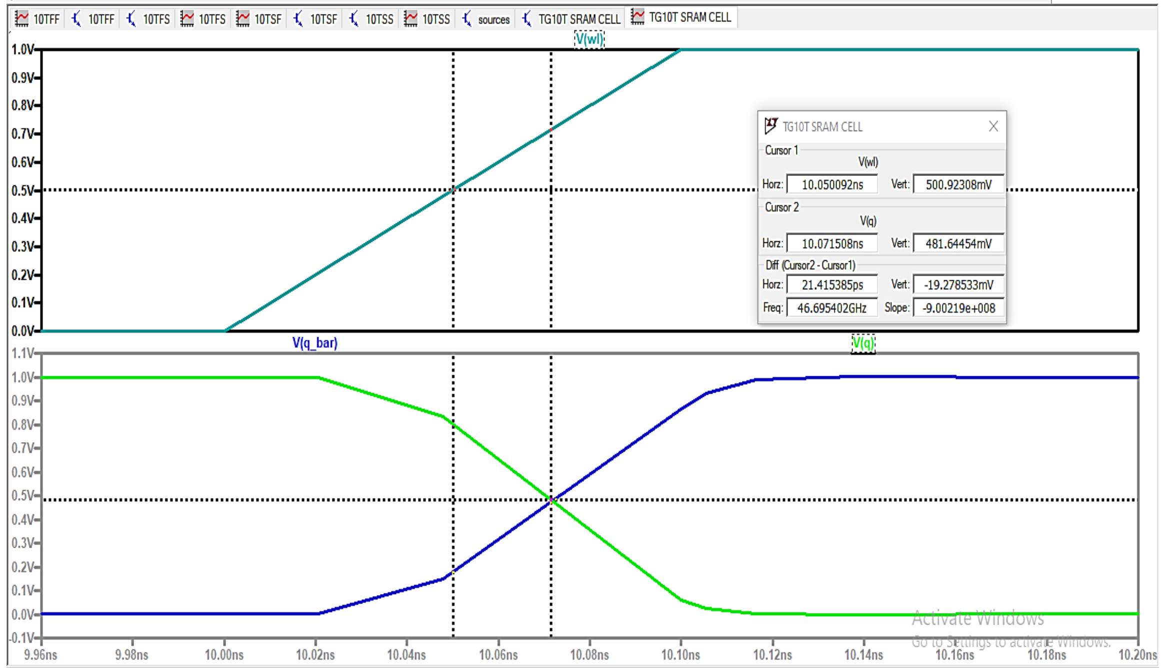
Fig. 3.5 represents the transient response of the transmission gate SRAM cell .when WL=0, WAS=0, and RAS =0, the cell holds the data. When WL=1, WAS=1, the cell contents are updated and when WL=1, and RAS =1, the read operation can be performed.

3.5. Access time

3.5.1 Write delay

It is specified as the time taken from the word line arriving VDD/2 to the time in which the voltage at the storage nodes become equal.

The effect of the process corners on write delay has been analyzed and the results are shown in fig. 3.11



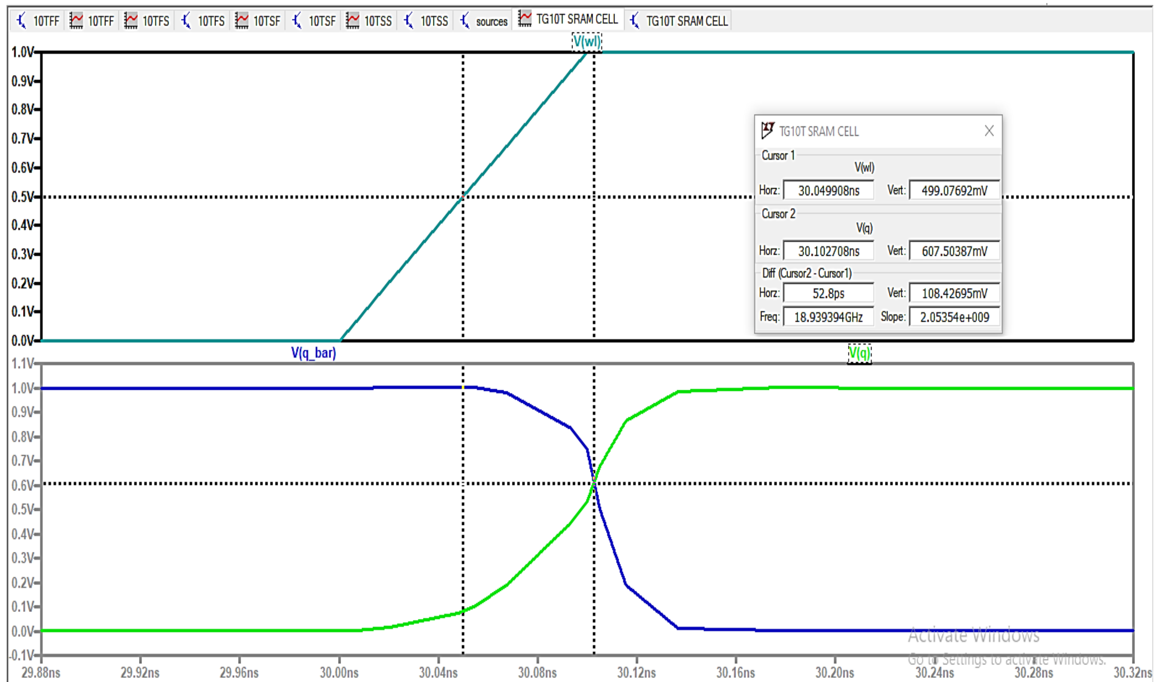
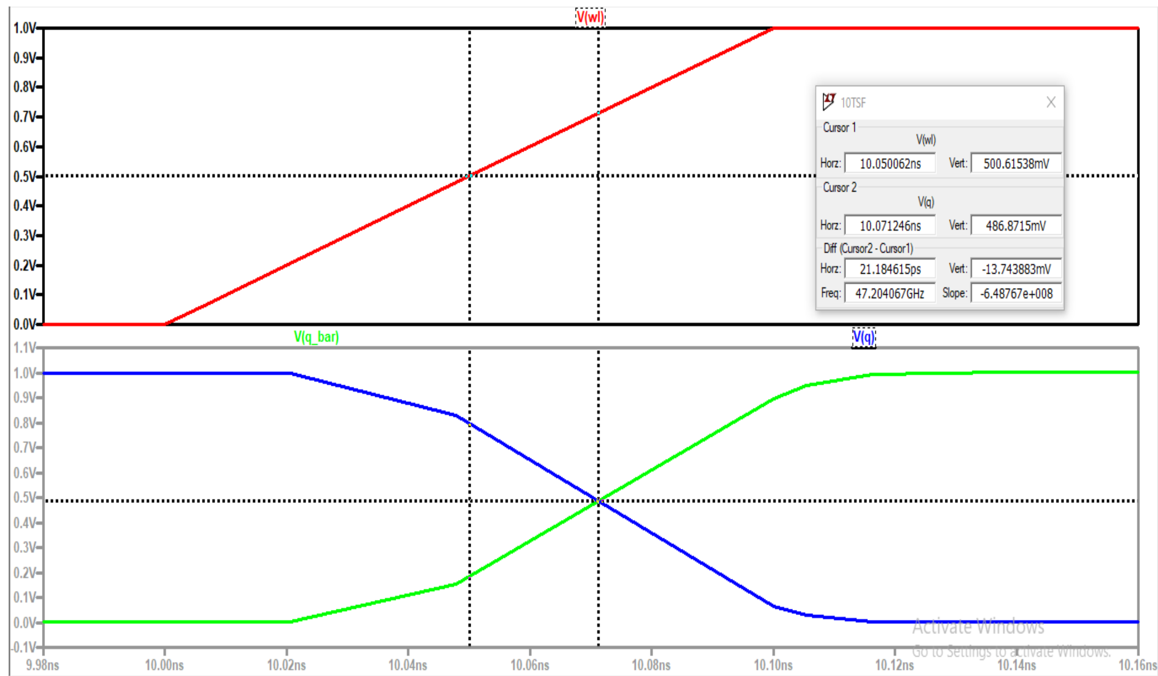


Fig. 3.6 Write delay measurement - TT corner



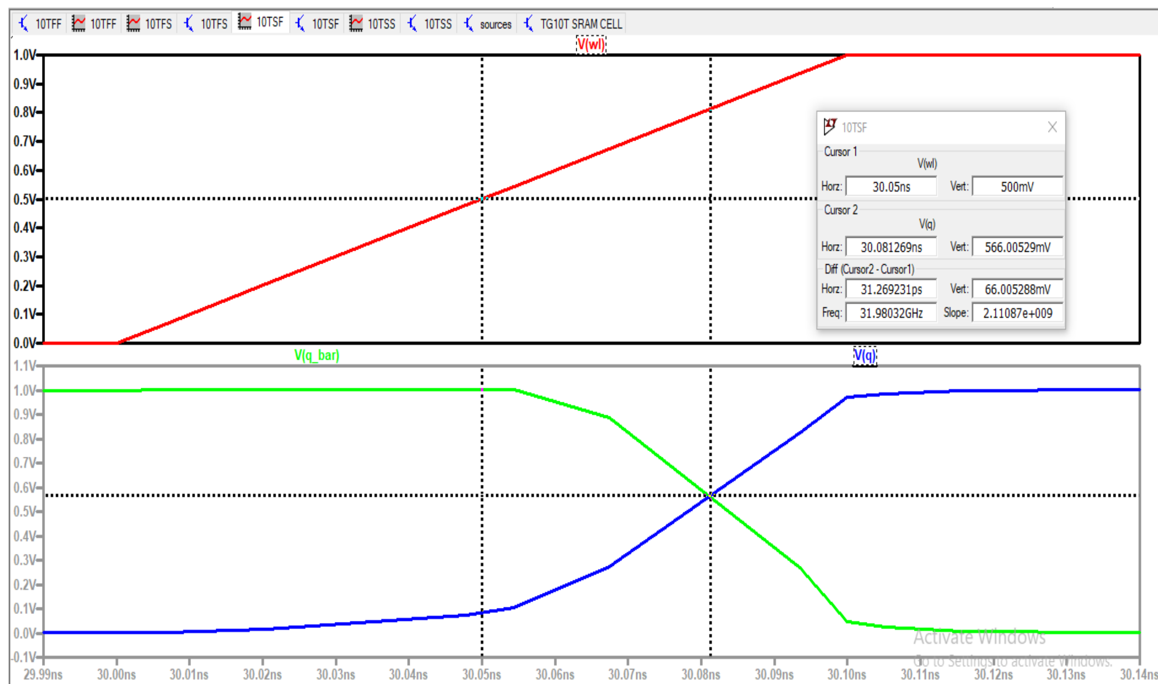


Fig. 3.7 Write delay measurement – SF corner

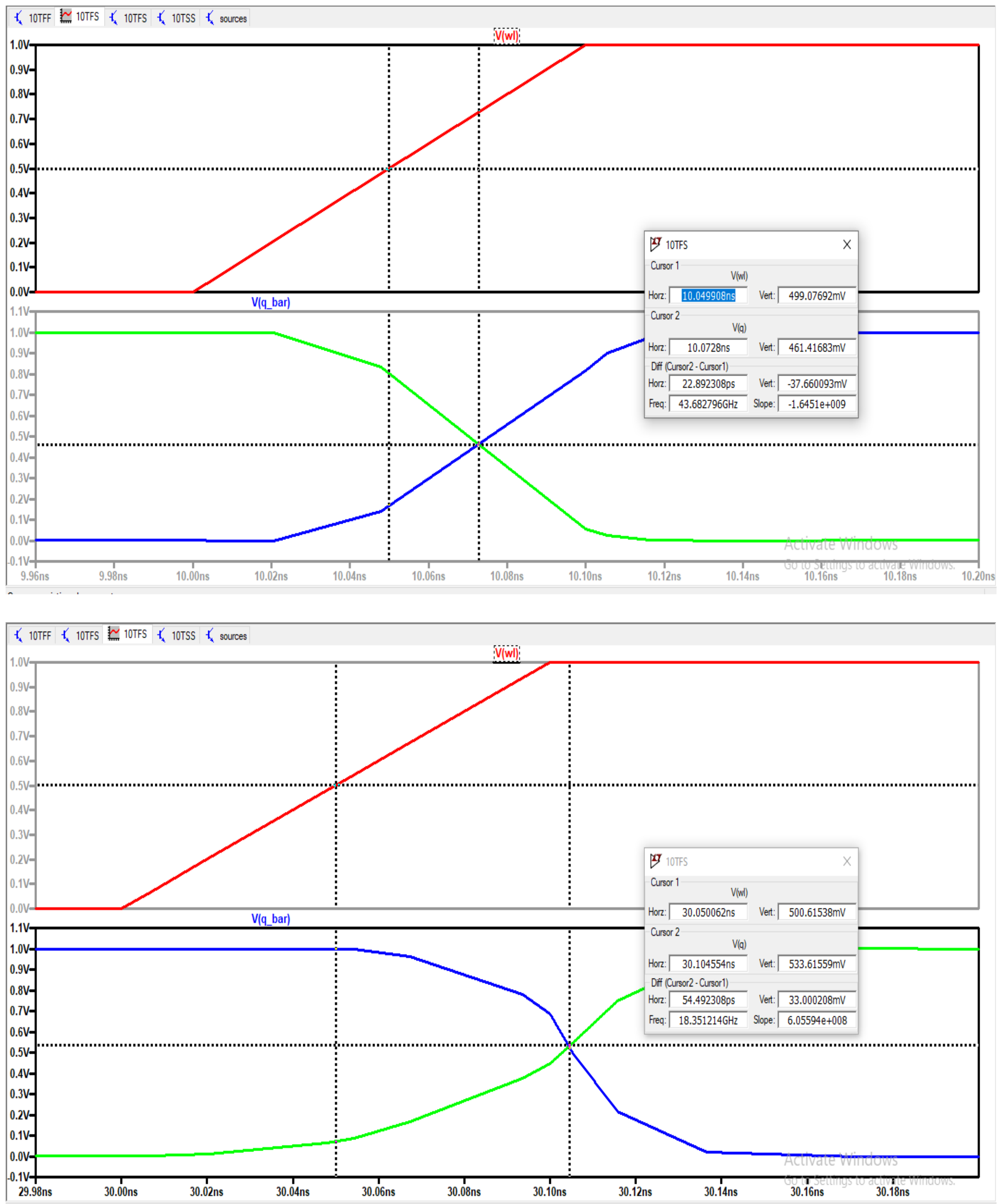


Fig. 3.8 Write delay measurement - FS corner

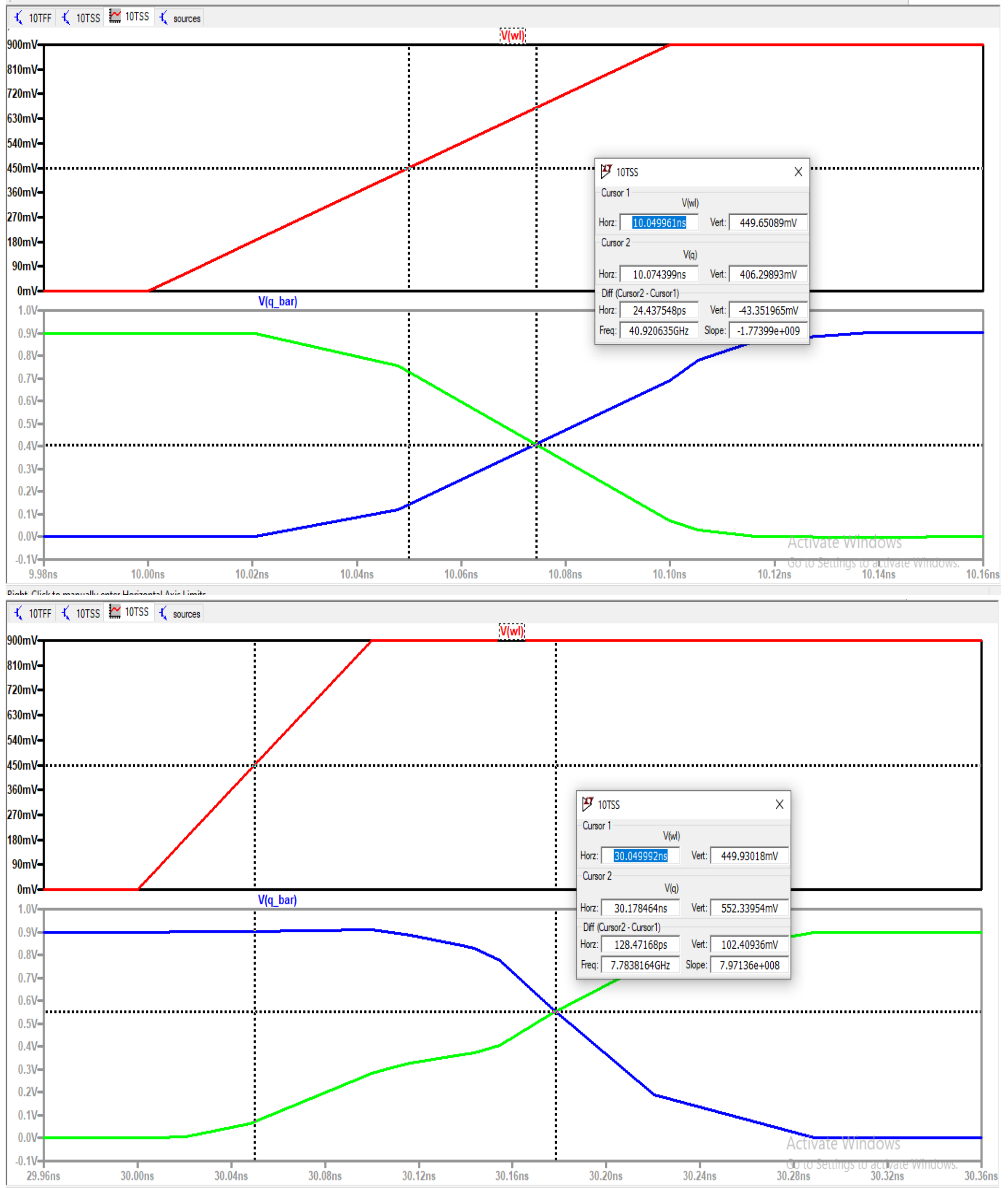
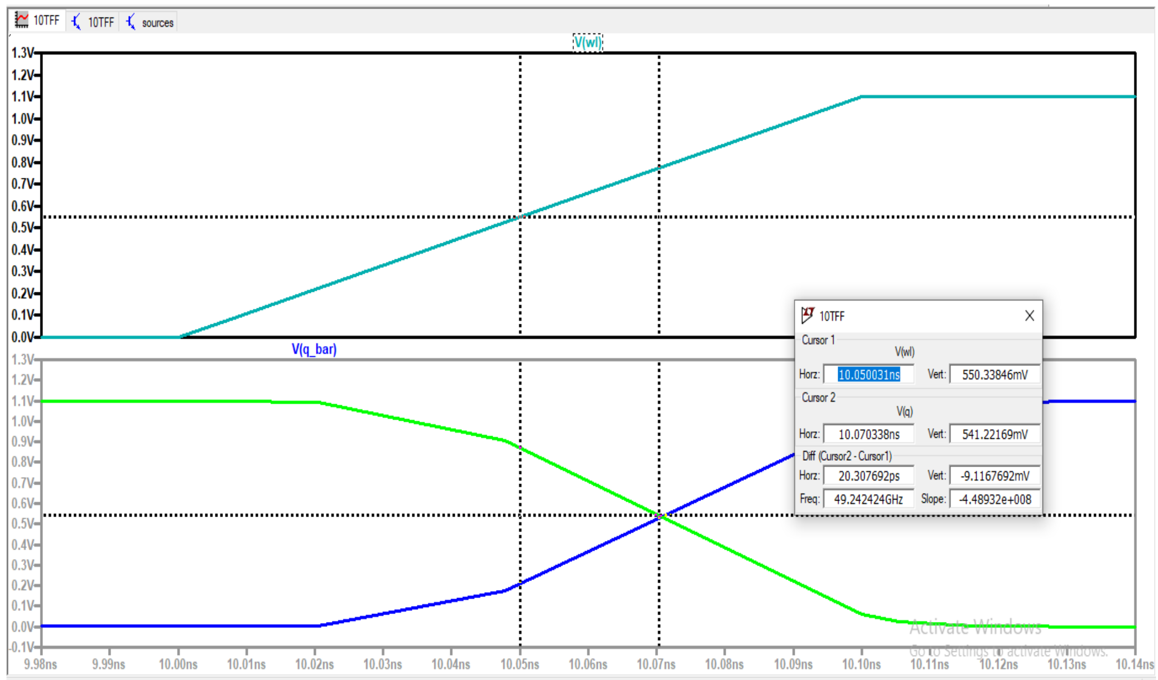


Fig. 3.9 Write delay measurement - SS corner



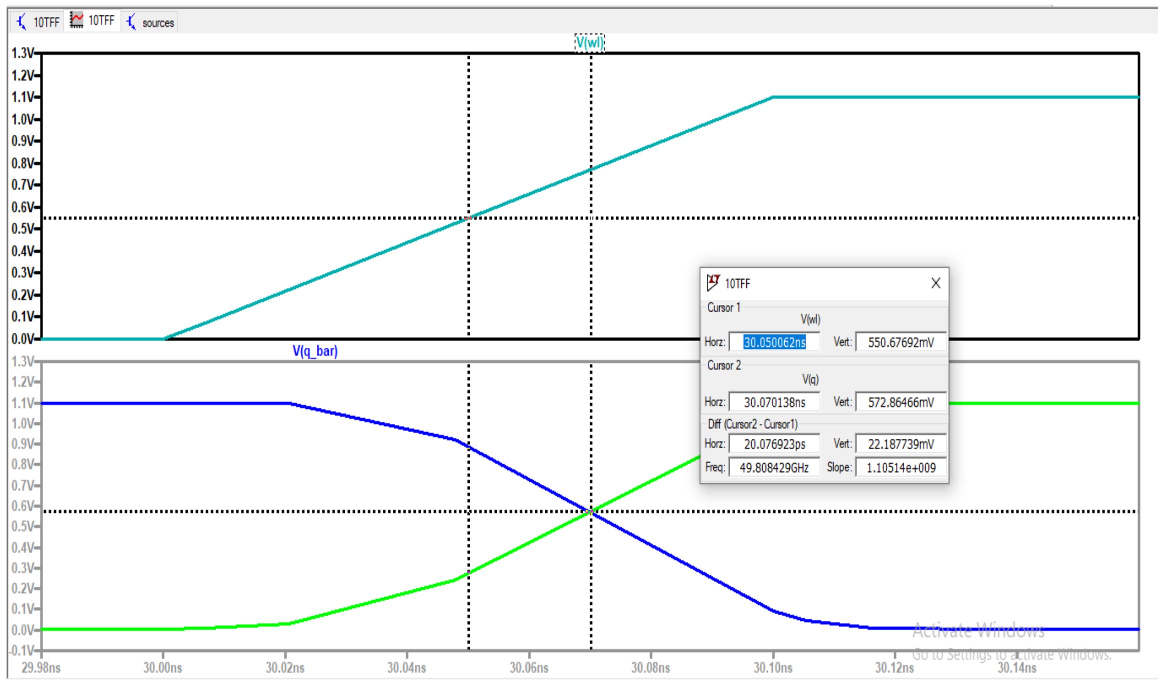
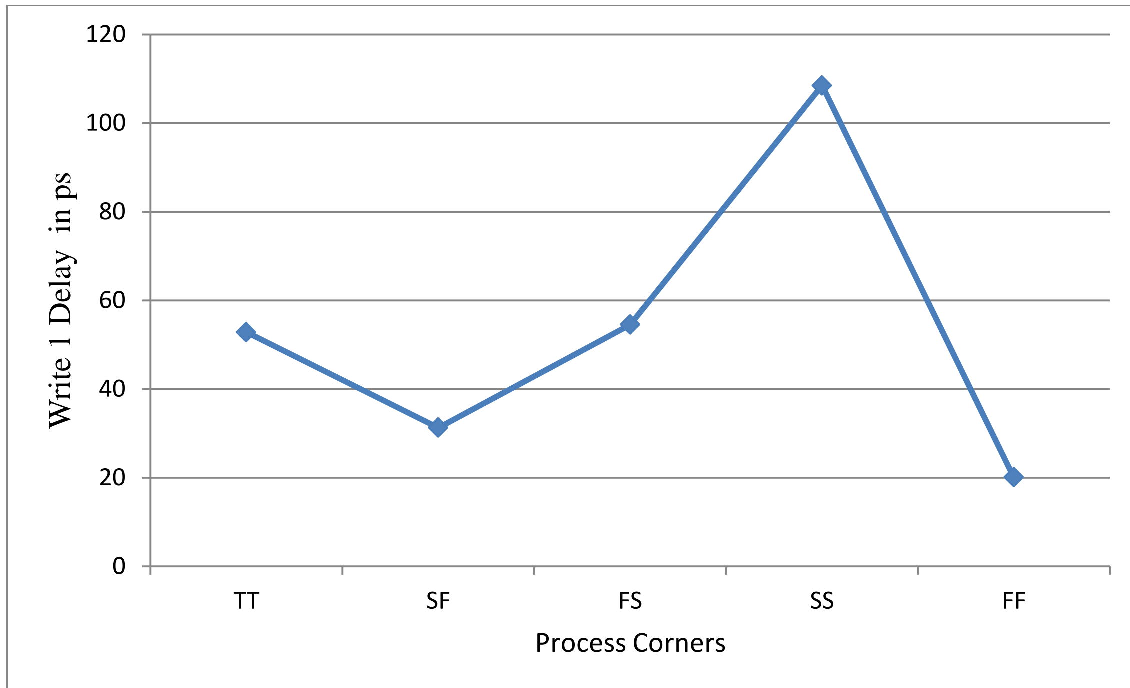


Fig. 3.10 Write delay measurement - FF corner



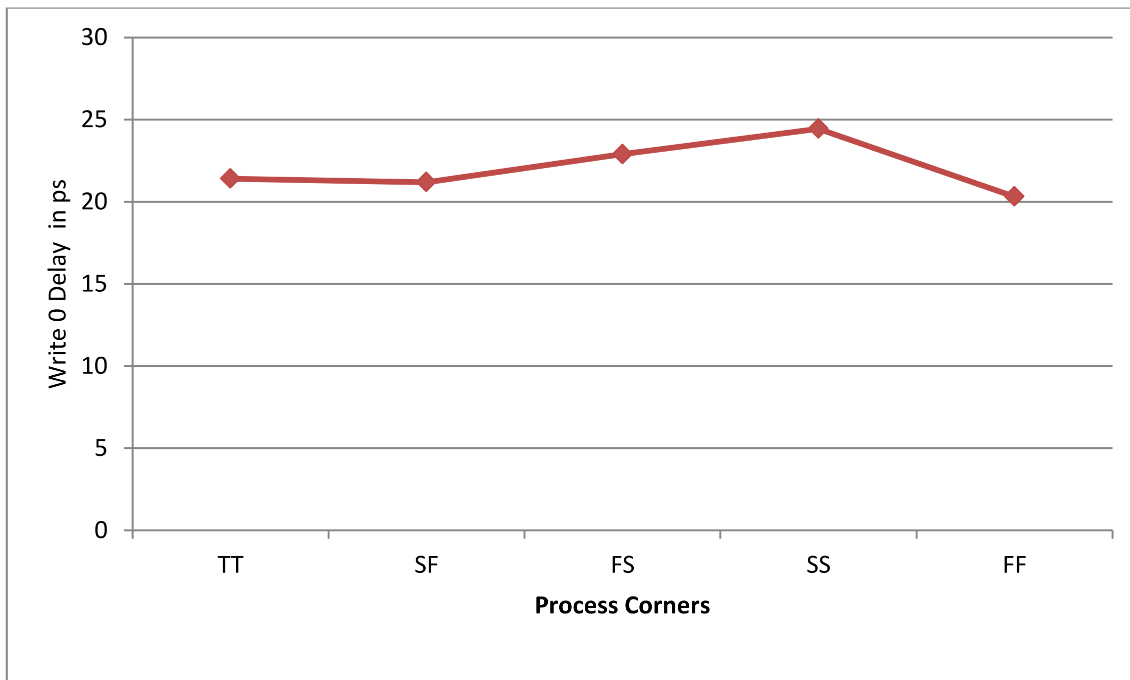


Fig. 3.11 process corners analysis of write delay of the new design

Fig. 3.11 illustrates the write delay of the transmission gate based 10T SRAM cell for various process corners. From Fig. 3.11, the FF corner has lower write delay and SS corner has higher write delay than other corners.

3.5.2. Read delay

It is determined as the time taken from the read word line arriving VDD/2 to the time when the voltage of the bitline reaches 10% of VDD. The effect of the process corners on read delay has been analyzed and the results are shown in fig. 3.12

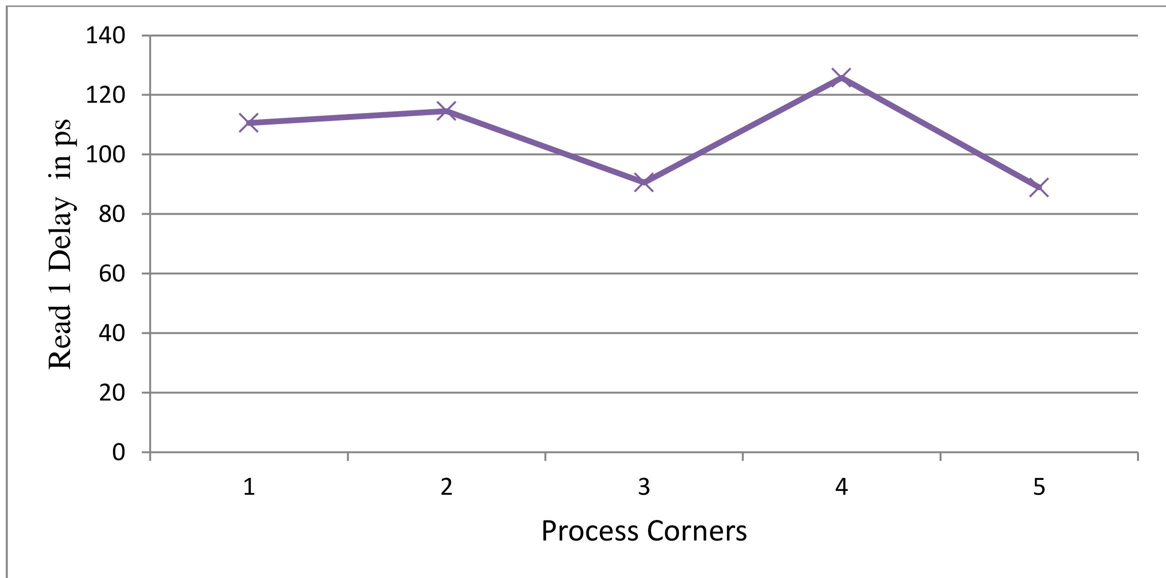


Fig. 3.12 process corners analysis of read delay of the new design

3.6. Stability analysis

Calculation of the noise margins is done by using the N-Curve approach and the setup for the proposed design is illustrated in Fig. 3.13. The bitline BL is clamped to VDD (1 V), M7, M8, and M9 are switched ON while M5 and M6 are switched OFF. A voltage source has been applied at node QBAR that stores zero then swept from 0 V to 1 V, the current of the applied source has been measured and plotted as illustrated in Fig. 3.14.

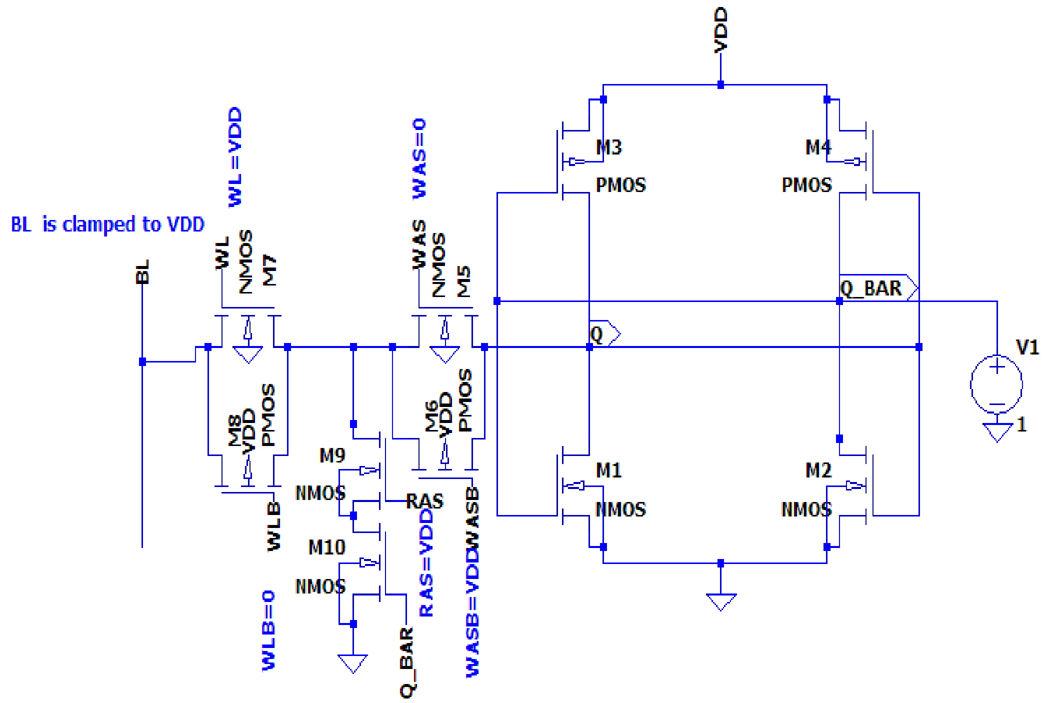
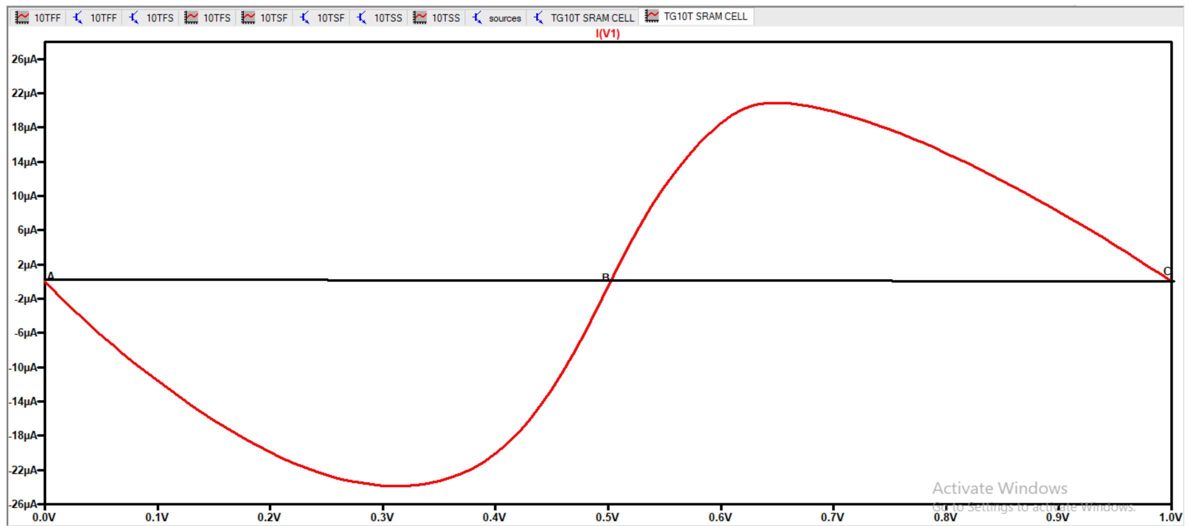


Fig. 3.13 Set up for N curve of the proposed design



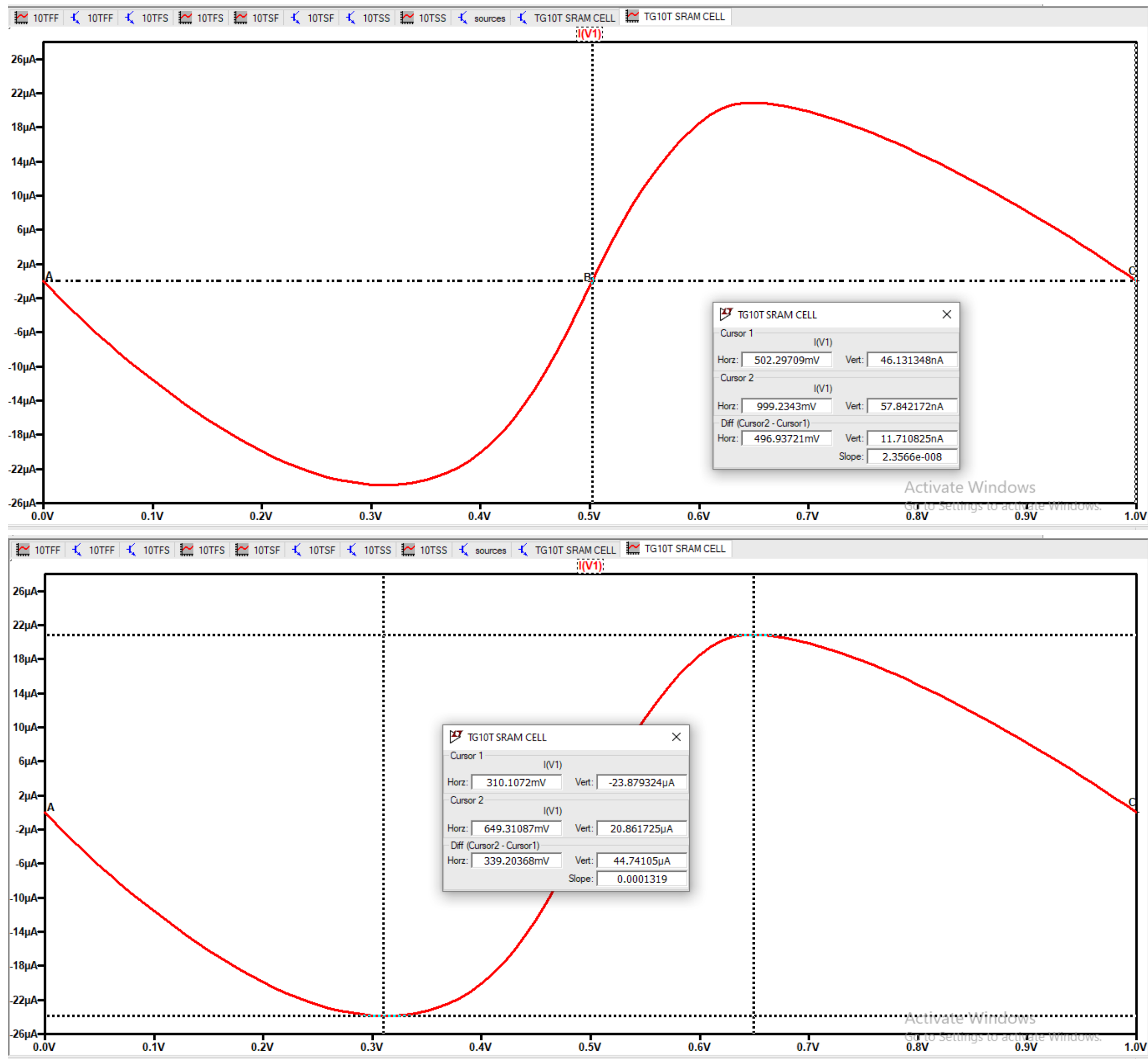


Fig. 3.14 N-curve of the new SRAM cell

The noise margins have been calculated from the simulated N curve and tabulated in table 1

Table 1 the Noise Margins

	The Proposed 10T SRAM
SVNM(mV)	502.297
SINM (µA)	-23.879
WTV (mV)	496.937
WTI (µA)	20.862

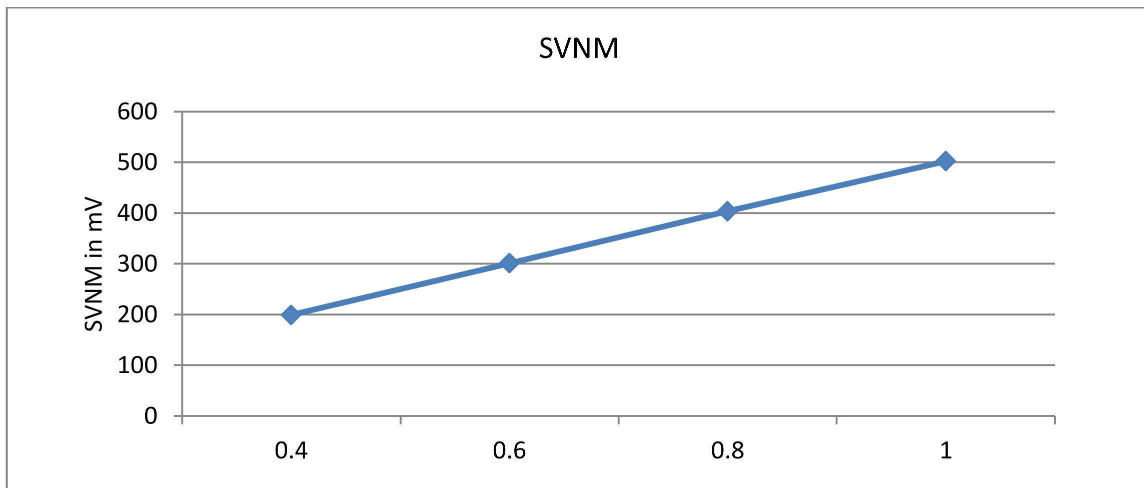
Thus it may be inferred that the proposed cell has read SNM greater than VDD/2.

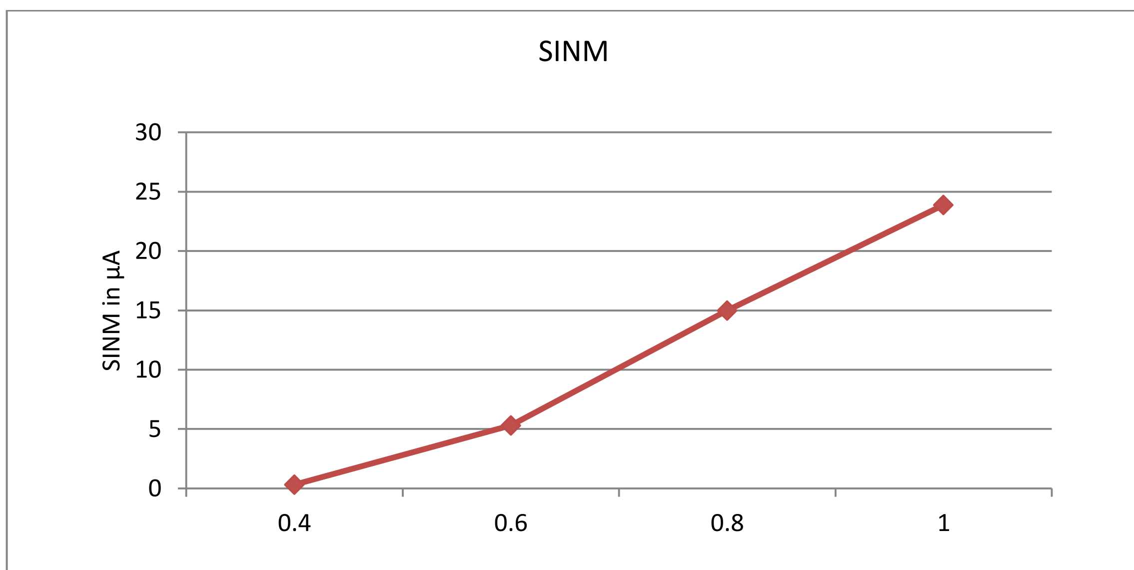
3.6.1. Effect of VDD on stability

To study the supply voltage influence on stability, the performance parameters SVNM, WTV, SINM, and WTI are observed at various supply voltages and the results are summarized in Table II and plotted in Fig. 3.15 for better visualization.

Table II Effect of VDD on stability

Supply voltage	SVNM	WTV	SINM	WTI
0.4	199.225	200.464	- 0.3119	0.26198
0.6	300.919	299.081	- 5.304	4.272
0.8	403.387	396.613	- 14.976	12.216
1	502.297	496.937	- 23.879	20.862





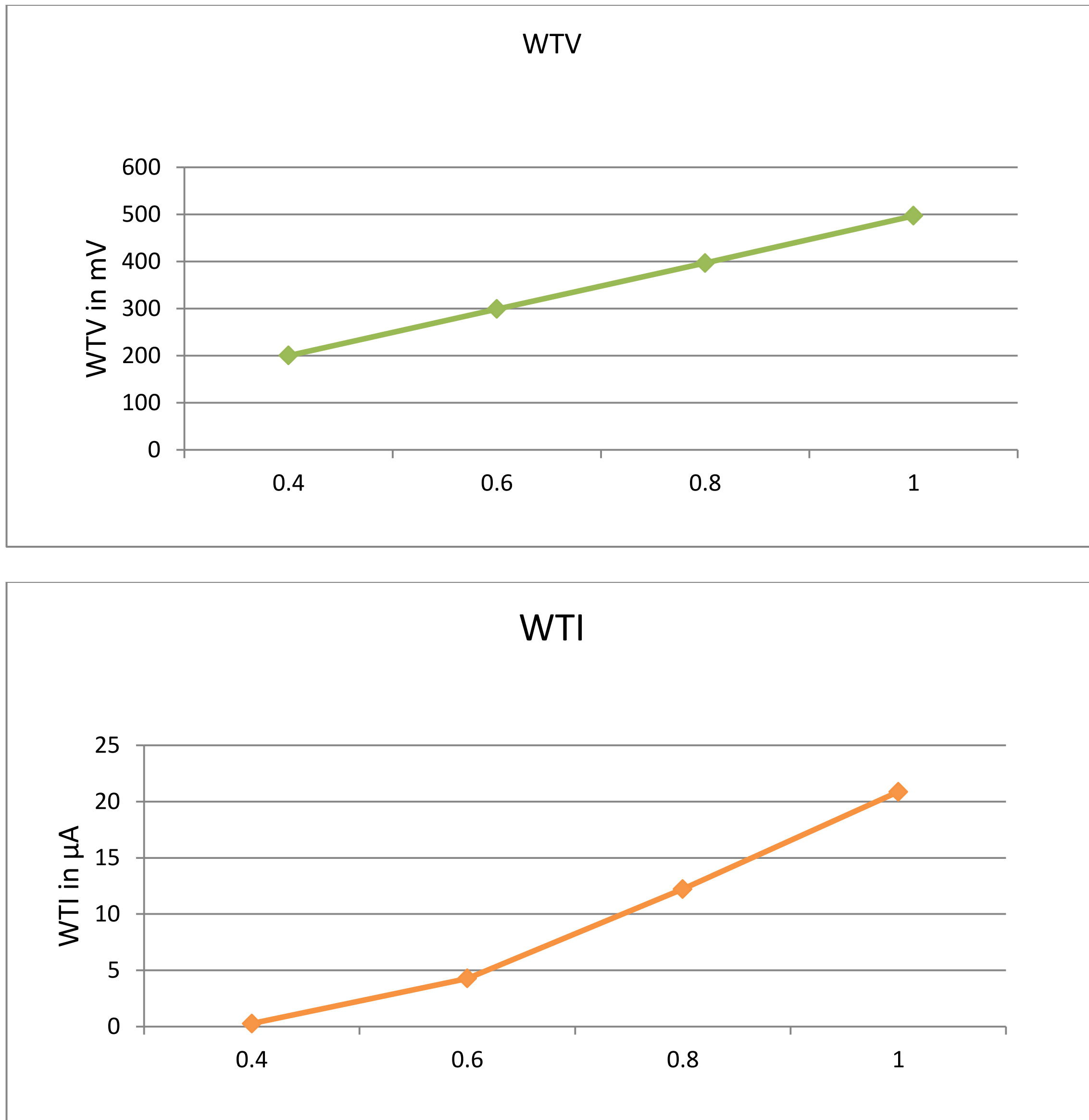


Fig. 3.15 Effect of VDD on stability

From Fig. 3.15, it may be noted that as the supply voltage increases, the cell stability increases.

3.6.2. Temperature effect on stability

The simulated N Curve of the new design at different temperatures is illustrated in Fig. 3.16

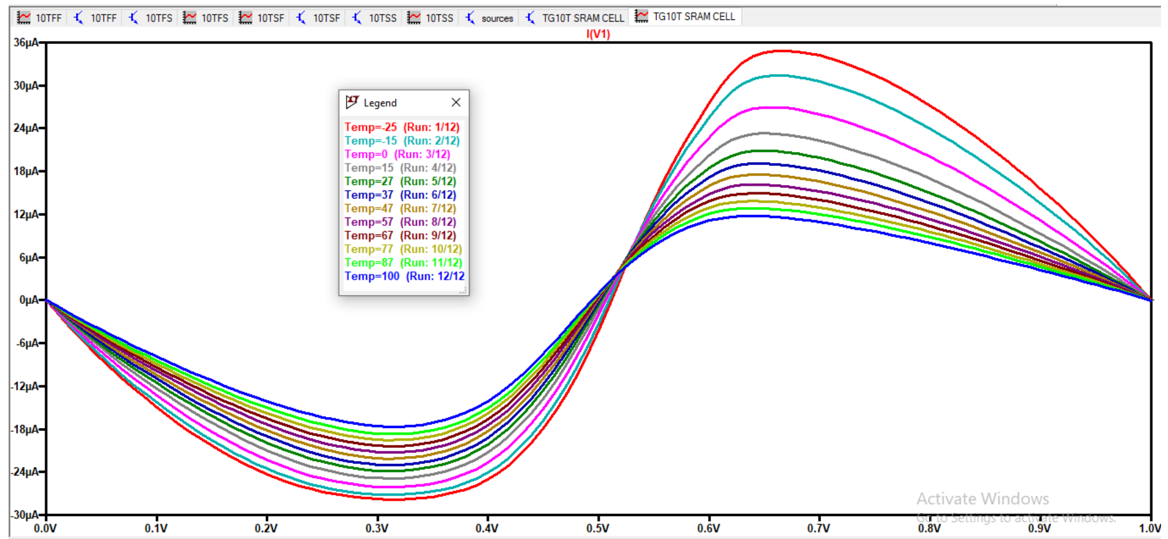
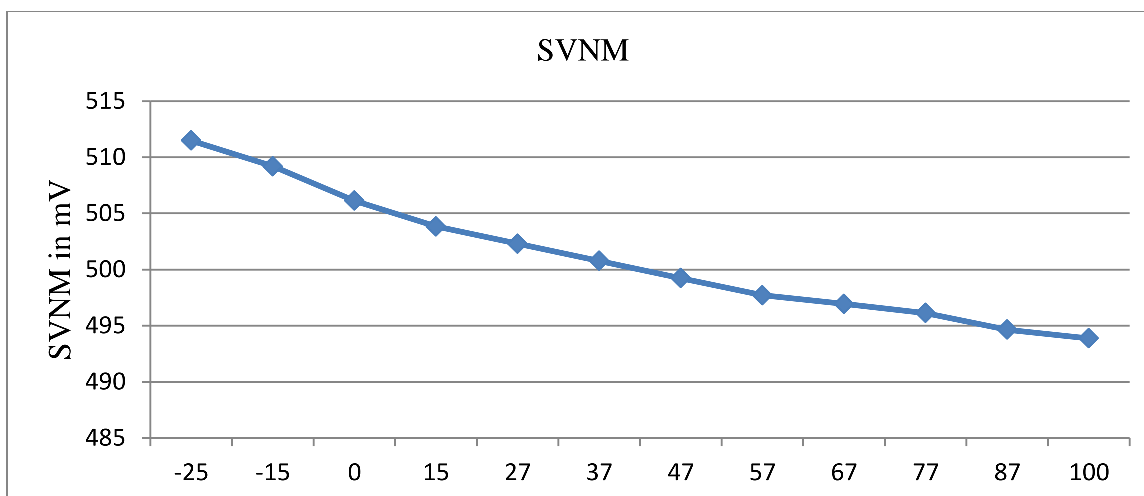


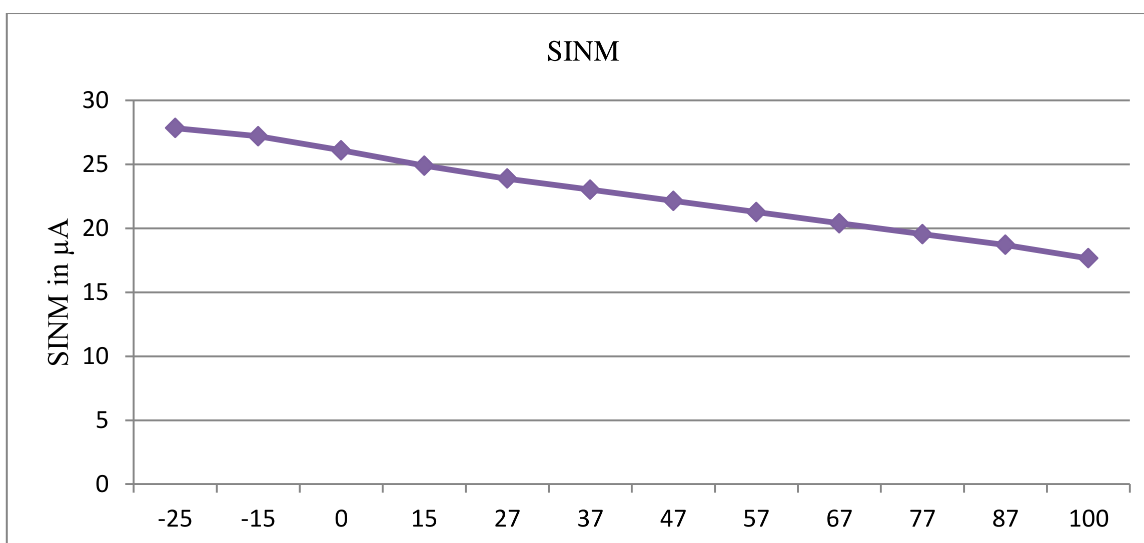
Fig. 3.16 N Curve of the new design at several temperatures

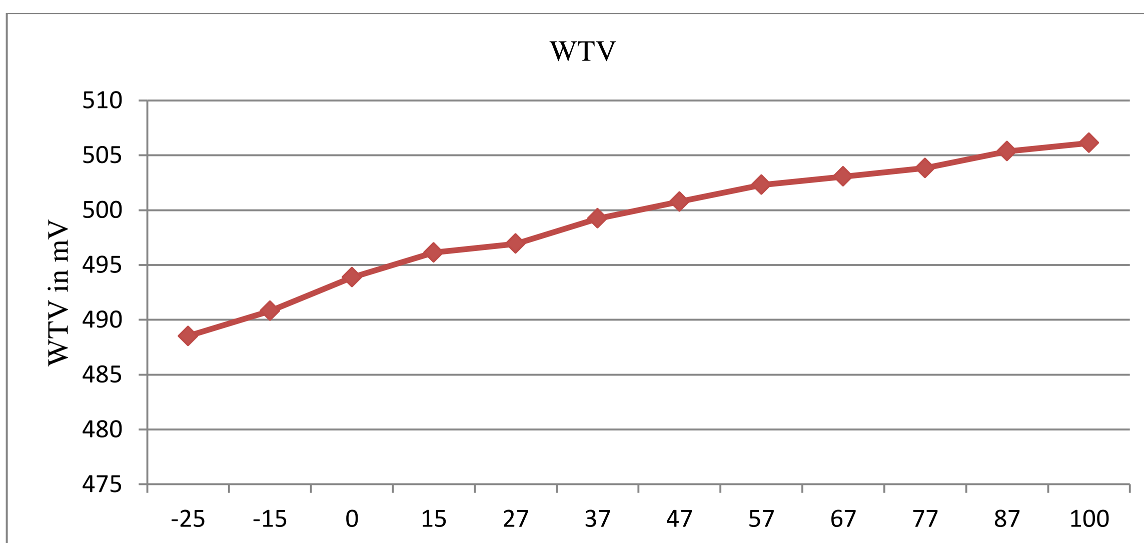
The results are summarized in Table III and plotted in Fig. 3.17 for better visualization.

Table III Effect of Temperature on stability

Temperature	SVNM	SINM	WTV	WTI
-25	511.485	-27.832	488.514	34.851
-15	509.188	-27.185	490.812	31.392
0	506.126	-26.094	493.874	26.944
15	503.828	-24.891	496.127	23.302
27	502.297	-23.879	496.937	20.861
37	500.766	-23.011	499.234	19.076
47	499.234	-22.137	500.766	17.533
57	497.703	-21.261	502.297	16.161
67	496.937	-20.393	503.063	14.941
77	496.127	-19.537	503.828	13.851
87	494.64	-18.702	505.359	12.872
100	493.874	-17.653	506.125	11.748


SVNM
SVNM in mV
515
510
505
500
495
490
485
-25
-15
0
15
27
37
47
57
67
77
87
100


SINM
SINM in µA
30
25
20
15
10
5
0
-25
-15
0
15
27
37
47
57
67
77
87
100


WTV
WTV in mV
510
505
500
495
490
485
480
475
-25
-15
0
15
27
37
47
57
67
77
87
100

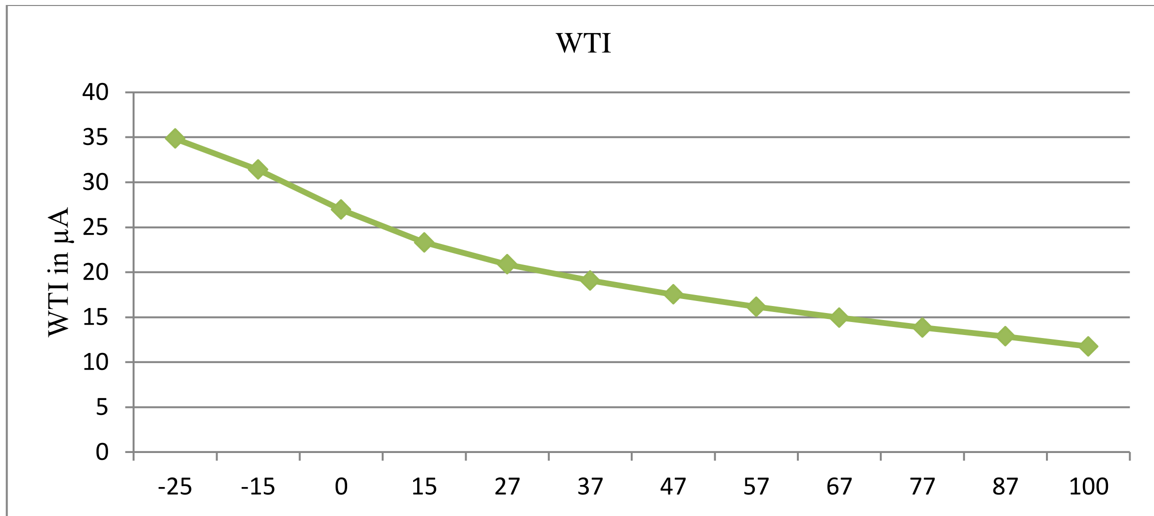
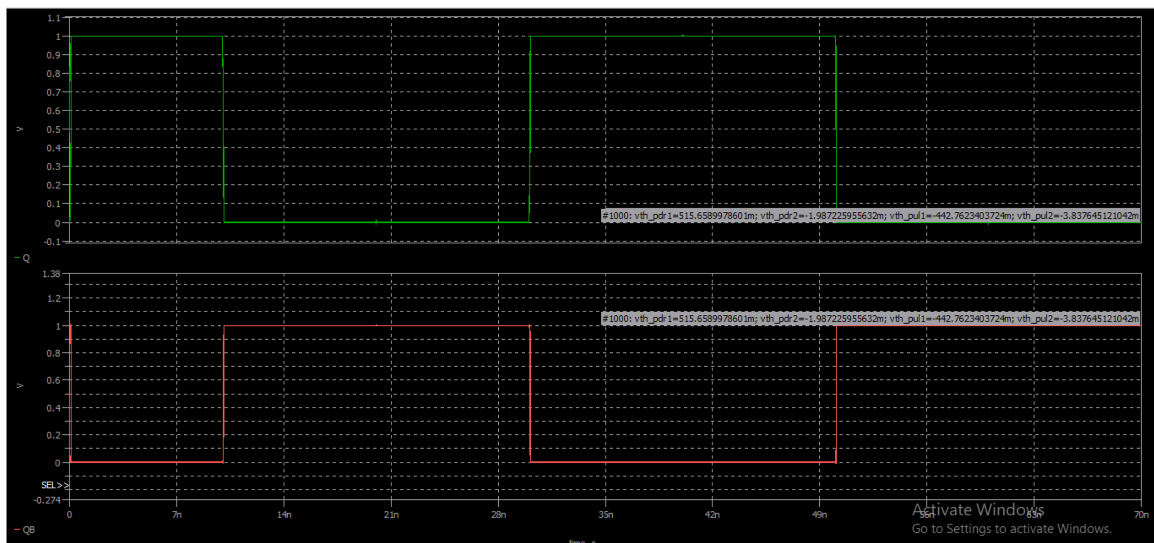


Fig. 3.17 Effect of Temperature on stability

As temperature varies from -25˚C to 100˚C, it has been noted that the SVNM, SINM, and WTI reduce with increasing temperature while WTV increases.

3.7. Monte_ Carlo analysis

The proposed design has been run in Monte Carlo simulation to ensure the cell reliability under different environmental parameters and process variations. The simulated 10T cell transient response for 1000 MC Simulation is shown in Fig. 3.18



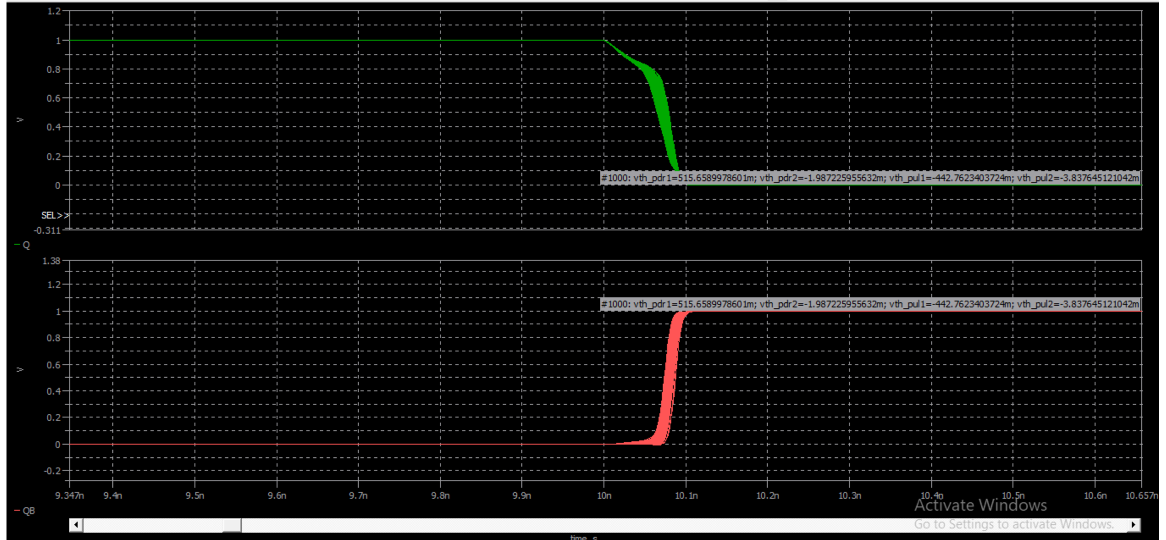


Fig. 3.18 1000 Monte_Carlo simulation of the new 10T SRAM Cell

Chapter 4

CONCLUSION AND FURTHUER WORK

4.1.Conclusion

In this report a new SRAM cell has been designed in 32 nm technology node, the proposed design overcomes the basic stability problem throughout the read mode of the 6T SRAM cell by using an isolated read port, thus isolating the cross-coupled inverter from the bitline and the read current never transits over the cell internal node, therefore the read stability becomes equal to the hold stability.

The difficulty of writing ‘1’ in single ended structures has been solved by using two transmission gates instead of the NMOS access transistor.

The effect of the process corners on write and read delay has been analyzed. The noise margins have been calculated by using the N-Curve method, the new 10T SRAM cell has read static noise margin greater than VDD/2 also the influence of the temperature and supply voltage on stability have been studied.

4.2. Further work

The new 10 T SRAM cell based on the transmission gates can be used to operate close to the subthreshold region and because at low voltages the leakage current will increase exponentially one of the common leakage current reduction techniques will be used to decrease the power consumption and the cell can be used for low power applications.

The 10 T SRAM cell can be used to build an SRAM array.

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