BLOCK LEVEL TIMING AND POWER OPTIMIZATION OF VLSI PHYSICAL DESIGN

A DISSERTATION REPORT

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR

THE AWARD OF THE DEGREE

OF

MASTER OF TECHNOLOGY

IN

VLSI DESIGN & EMBEDDED SYSTEMS

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MAY, 2022

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CANDIDATE'S DECLARATION

I, Sandeep Kumar Gupta, Roll No. 2K20/VLS/17 student of M. Tech (VLSI & Embedded systems), hereby declare that the project Dissertation titled **"Block level Timing and Power optimization of VLSI Physical Design"** which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship, or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled **"Block level Timing and Power optimization of VLSI Physical Design"** which is submitted by **Sandeep Kumar Gupta, 2K20/VLS/17**, to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the prerequisite for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place:

Date**:**

Dr. Prof. Manjeet Kumar
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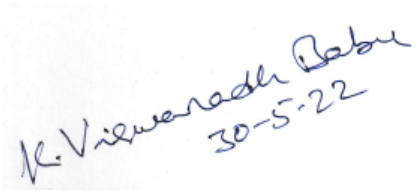
COMPANY CERTIFICATE

This is to Certify that the Project entitled **Block Level Timing and Power Optimization of VLSI physical design** was carried out by **Sandeep Kumar Gupta Emp ID 50032839** At **AMD RESEARCH AND DEVELOPMENT PVT. LTD. HYDERABAD** under my guidance during January, 2022 to May, 2022.



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ABSTRACT

This project analysed and implemented VLSI physical design for CMOS technology, which is an important step towards fabrication of an integrated circuit on a silicon wafer. The physical design is performed in two levels, PNR Flow and ECO Flow. At ECO (Engineering Change Order) timing violations are fixed. There may be constraints that were missed on specific nets. ECO is used to control the timing behaviour of the design.

The advancements in current day CMOS technology have resulted in shrinking feature size of the MOS devices and an increase in the potential packing density. This has enabled designers to offer increased computational powers to the end users on smaller and smaller devices which have resulted in a huge demand for portable devices such as PDAs, cellular phones, etc. But this trend in increasing logic complexities on a single chip has come with its own challenges. Apart from packing large functionalities on a single IC, consumer applications need to be designed to consume less power to reduce the package costs without compromising on the performance.

The results obtained indicated that design optimization times can be significantly reduced by enabling concurrent optimizations in all the important PVT corners for the design under consideration. Tools are used for better optimization of design, to see run-time, and better QoR results. This helped in closing the design with minimal timing and other electrical violations in a shorter time when compared to the earlier trend of having a sequential optimization cycle. These aspects make it possible to leverage the capabilities of present-day EDA tools to tape-out complex SoC designs in a competitive semiconductor market. Here we used the tool ICC compiler, Primetime, Calibre, Formality, and Redhawk.

ACKNOWLEDGMENTS

Foremost, I would like to express my sincere gratitude to my mentor **Dr. Manjeet Kumar** for helping me on each step of this research, due to her continuous help and support I completed this research. Her patience, motivation, enthusiasm, and vast knowledge helped me in all the time of this research and writing of this dissertation. Without her guidance, I could not have imagined completing this research. Her suggestions and the way of managing the work were the most important key points, which made my path clear. She helped me use my full potential because of that I tried my best to get the maximum for this project. I am extremely grateful for guiding me throughout the project. I am thankful to Electronics Department and faculty for helping me, and also thankful to my friends who helped me directly and indirectly in my research.

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LIST OF ABBREVIATIONS

ASIC- Application Specific Integrated Circuits

VLSI- Very Large Scale Integrated

PD- Physical Design

PnR/PNR- Place and Route

QoR- Quality of Report

RTL- Register Transistor Level

UPF- Unified Power Format

ECO- Engineering Change Order

PVT- Pressure Voltage Temperature

STA- Static Time Analysis

IC- Integrated Circuits

CPU- central Processing Unit

VHDL- Hardware Description Language

FPGA- Filled Programable Gate Array

SOC- System on Chip

DRC- Design Rule Check

DRV- Design Rule Verification

WNS- Wurst negative Slack

TNS- Total Negative Slack

NV- Number of Violating

CTS- Clock Tree Synthesis

DEF- Design Exchange Format

SPEF- Standard Parasitic Exchange Format

MOS- Metal Oxide Semiconductor

CMOS- Complementary Metal Oxide Semiconductor

FinFET- Fin Field Effect Transistor

LS- level Shifter

CHAPTER 1

INTRODUCTION

In prior ages of IC plan advances, the principal boundaries where timing concern with regained devices was intended to boost performance in that limiting region so utilization power concern a lesser, we have seen that CMOS (Complementary Metal oxide semiconductor) has viewed as a lower power innovation, which genuinely lower power utilization for somewhat frequency are low for a clock utilized that point, whether irrelevant spillage currents [1]. As of late, nonetheless, gadget densities and clock frequencies have expanded emphatically in CMOS gadgets, along these lines expanding the power utilization decisively. Simultaneously, supply voltages and semiconductor limit voltages have been brought down, making spillage current become a critical issue. Subsequently, power utilization levels have arrived at their satisfactory cut-off points, so power become significant for timing and region. Higher supply utilization could bring about unnecessarily temperatures are high during activity.

That implies costly artistic IC bundling should be utilized rather than complicated costly intensity cooling and sinks frameworks frequently expected for their item activity. High power utilization additionally lessens battery duration in versatile gadgets, for example, PCs, telephones, and individual hardware. As additional elements are added to an item, power utilization increments so as battery duration has diminished, required bigger battery so more limited duration for charges. Battery innovation behind lingered the expanded reefers to that power [2]. Actual union is a significant element of present-day VLSI strategies. The actual combination starts with a planned netlist created the by rationale blend. The netlist created after consistent combination portrays the intelligent associations of the parts like macros, input yield squares, and pins ant he'd actual combination creates a netlist which is upgraded and an actual format which gives a fundamental assessment the of situation and directing in execution instrument and actual mindful blend is the age of that floorplan by PnR that is [lace and route device so taking care of floorplan by def file to union instrument and consequently actual format assessment is utilized rather than wire load displaying assessment [1]. The time taken in number of cycles from combination PnR as well as the other way around decreases and timing improves bringing about a superior QoR. The Floor arranging step essentially

incorporate full-scale position, apportioning of configuration, input-yield ports arrangement, and power arranging. The plan boundaries, for example, power, region, timing and execution should be considered during floor arranging so these assessments are determined at each progression in light of the input from the execution group, IP proprietors, and RTL planners If there should arise an occurrence of progressive plans, the quantity of cycles increments as every one of the squares are connected at higher top-level [2].

To lower the power consumption of chips, designers are increasingly resorting to power reduction techniques such as multi-Vdd design partitioning, Dynamic voltage, and frequency scaling, state retention for power gating and substrate biased. Implementing such technique adds more complexity to the entire backend flow, especially during P&R, power analysis, reliability check, and timing signoff. In addition to this added complexity, verifying the correctness of the low power implementation is a challenge by itself.

1.1Motivation

Numerous ventures are moving towards lower innovation hubs because of expansion sought after for SOC speed and execution. The floor arranging influences the planning process duration the in whole plan stream from configuration intending to execution. A few difficulties, for example, enormous plan sizes, expand full-scalable count, timing/power assessments, district for, timing and pin task, predefined arrangement areas, large scale directions and pin positions, synchronous standard cell and large-scale situation, blockage and timing-driven arrangement, diminishing process duration, elite execute, on and low power targets are expanding for a floorplan fashioner [4]. At times, the macros should be authorized to the outskirts of the plan to give e most extreme region to the standard cell situation [1].

The Unified Power Format (UPF) alongside creative procedures empowers power-mindful confirmation at the register move level, utilizing customary RTL configuration styles and reusable blocks. The outcome is a multi-instrument arrangement that can be utilized all through the RTL to GDSII stream, applying predictable semantics for both check and execution [1].

1.2Objective

The basic objective of this project is to implement the complete Place and Route flow for Lower technology, for a given design by incorporating the best leakage optimization technique which depends on the design block and the instance count in the block. The optimized flow methodology is arrived at by analysing QoR (Quality of Results) of multiple experimental runs for the different methods employed to reduce the leakage power, thus achieving reduced power consumption and desired timing closure.

This includes two important flows PNR and ECO (Engineering change Order) so In PnR flow multiple experimental runs are conducted with different floorplans. The best one of them is picked for the final ECO flow. Most of the violations are resolved PnR flow only. The violations left after complete PNR flow are resolved at ECO flow by adding manual corrections to the design After completion of the PNRw in parallel with resolving violations, some experiments are conducted to increase the performance of the design.

1.3 Organization of Thesis

In this thesis physical implementation of a power, gated design is discussed and also techniques used for reducing leakage power are presented. The current thesis is organized in the following manner.

Chapter-1 Today challenges and needs for the project objective are discussed and literature survey is briefly discussed.

Chapter-2 ASIC design flow is discussed.

Chapter-3 Place and Route are discussed.

Chapter-4 Low Power design and Technique and ECO are discussed.

Chapter-5 Result of project and simulation are done.

Chapter-6 includes the conclusion and future scope of the project is described.

1.4 Literature Review

we centre around the foundation of nano meter plan strategies utilized in the business and the difficulties looked as innovation hubs advance with time. “The component size of incorporated circuits has been forcefully decreased chasing after better speed, power, silicon region and cost attributes. Semiconductor innovations with highlight sizes of a several nano meters are right now being developed” [1].

Representing the impacts of cycle, supply voltage, and temperature (PVT) minor departure from circuit execution is an essential necessity in present day chip configuration streams. Ordinarily, PVT varieties are partitioned into two gatherings chip-to-chip varieties and on-chip varieties, which are varieties seen across a solitary chip on-chip varieties are viewed as less serious than chip-to-chip varieties and are dealt with utilizing derates, or edges, in static timing Analysis (STA) runs [5]. Then again, chip-to-chip varieties can cover altogether more extensive cut-off points inside the working reach, and accordingly it isn't functional to apply margining strategies to this sort of varieties. All things considered, fashioners utilize corner examination, where STA runs are performed at various PVT settings, alluded to as corners. By doing this, it becomes conceivable to catch a circuit's most pessimistic scenario conduct in the PVT space without the extreme negativity of margining. Obviously, this comes at the runtime cost of playing out numerous STA runs. A couple of these varieties influencing the circuit execution are talked about in the succeeding areas.

1.4.1 Scaling Technology and Increased need for sophisticated designs

Moore's Law sees that over the historical backdrop of processing equipment, the quantity of semiconductors on incorporated circuits pairs around like clockwork so for as CMOS innovation ceaselessly downsizes to more modest calculations and the thickness of plan coordination typically and mercilessly increases as per Moore's Law, IC plan efficiency should increment at a similar rate so a lot bigger chips are planned inside similar worker hours financial plan [4].

“This expansion in plan efficiency should come from new innovative plan philosophies and high-level EDA apparatuses since the actual design and mental ability of the human cerebrum has been basically unaltered for the beyond countless years we have seen that light of authentic proof to date, plan efficiency has stayed aware of innovation and plan thickness scaling well overall, particularly in the front-end plan region so be that as it may, there are indications of stoppage in back-end efficiency” [6].

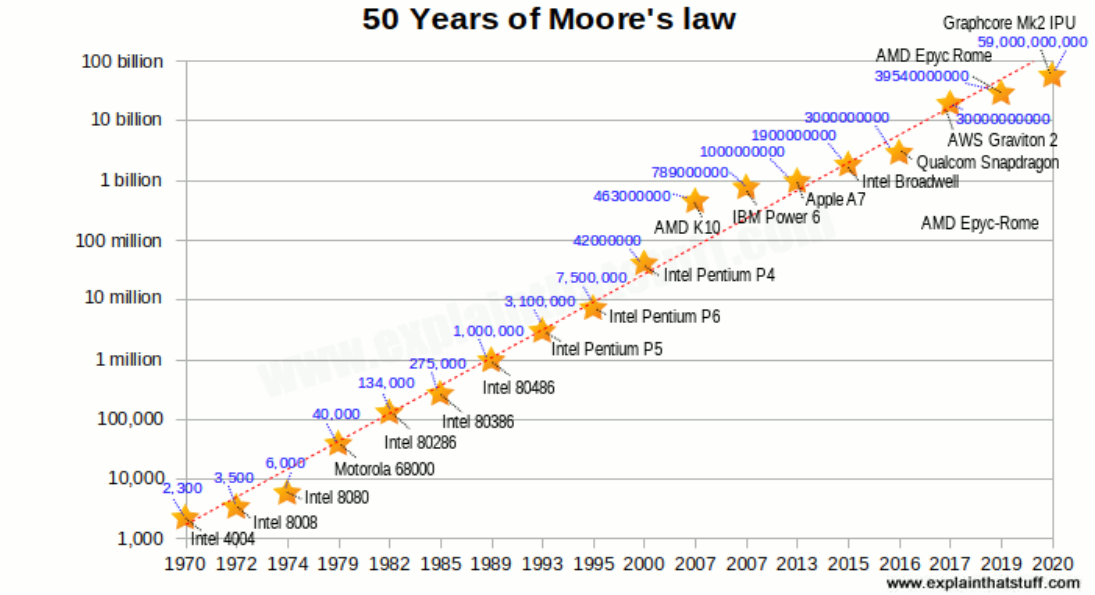

Figure 1.1- Moore's Law circuit level in per year. [26]

As displayed in Figure 2.1, the diagram portrays Moore's regulation with number of semiconductors on the y-hub and the time in years on x-hub. Chart covers processors from Intel and Advance Micro devices.

Evidently, this development is harder on actual plan so it's on frontend partner. Other than that, plan factors in sizing, the challenges there are actual plan system because of their caused connected with assembling advancements, like gadget and interconnect parasitic, physical and electrical plan rules, gadget dependability, and interaction variety.

1.4.2 Speed (Timing Closure)

The test of timing conclusion is caused fundamentally on that interconnect the metal from the parasitic of capacitance done and we have to see in cycles of 0.25 miniature meter and underneath, interconnect wire postpone begins to overwhelm the entryway defer on chip timing ways. Nonetheless, the deferral brought about by wire parasitic is obscure at the rationale amalgamation stage. Previously, this issue was managed by the wire-load model which appraisals wire parasitic in light of a cell's fan-out and configuration size. Their methodology, that time rationale combination, the door not fixing the size customary methodology so All things being equal, the timing spending plan, or capacitance load spending plan, for each not entirely settled, while the entryway floting in the size. there following technique, that die size are changed in further actual plan stage in light of genuine wire parasitic when they are free [26]. This approach gives a superior opportunity

to timing terminations with quicker times required to circle back and more modest in general chip sizes.

1.4.3 Need of Low-Power Designs

Scaling of innovation hub increments power-thickness more than anticipated. CMOS innovation past 15nm hub addresses a genuine test for any kind of voltage and recurrence scaling Starting from 180nm hub, each new interaction has intrinsically higher dynamic and spillage current thickness with insignificant improvement in speed. Between 90nm to 15nm the unique power scattering is practically same while there is ~8% higher spillage/mm2 so we have to care this Low cost generally keeps on driving more significant levels of incorporation, though minimal expense innovative forward leaps to monitor power are getting exceptionally scant [7].

1.4.4 Power Dissipation constraints

Power dissemination is the primary compel with regards to Portability so therefore cell phone customer requested more element so expanded duration. Top 3G prerequisite for administrators is power proficiency Clients need more modest and sleeker cell phones [7]. This requires elevated degrees of Silicon coordination in cutting edge processes, yet high level cycles have innately higher spillage current.

1.4.5 Related technology and library files

“Technology files contain information or commands that are used to configure structures, parameters (such as physical design rules and parasitic extractions), and limits of an ASIC design targeted to specific process technology” [8].

1.5 Tool set used

ICC Compiler- Used for Place and Route and ECO methodologies.
PrimeTime- Signoff Timing verification check.
Calibre- Signoff Physical verification check.
Formality- Signoff Logical equivalence check.
Redhawk- Signoff IR drop analysis.

CHAPTER 2

ASIC FLOW

2.1 Introduction to ASIC flow

Incorporated Circuits are produced using silicon wafer, with every wafer holding many bite the dust an application specific IC. An Integrated Circuit planned is known an ASIC (Application Specific Integrated circuits) assuming plan known as application specific IC for the particular objective. Instances of application specific IC incorporate, chip planned as a connection point among memory and CPU and so forth. Instances of integrated circuits which are not known as application specific IC incorporate Memories, Microprocessors and so on [9]. As shown in figure 2.1, the general ASIC is explained in detailed. ASIC Flow is generally divided into two phases Front End and Back End.

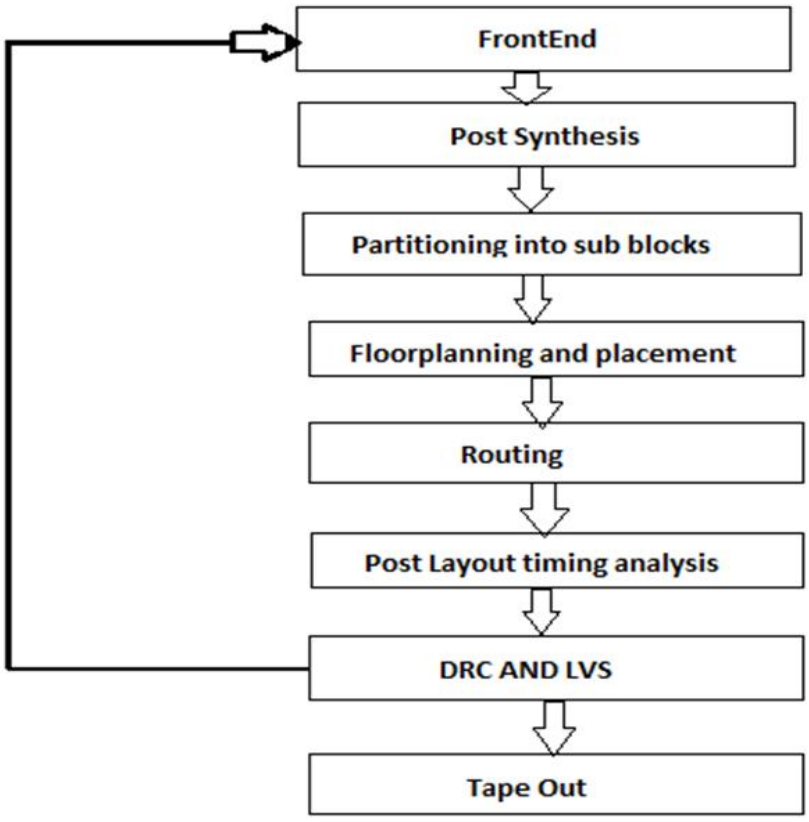

Figure 2.1 ASIC flow chart.

2.1.1 Front End

The initial process thought their chip's that concocted that designation as should visible from Figure. Details are only Performance seen they're in terms power, speed and Technology requirements like space and size, fabrication innovation and plan methods.

That following stage in the stream are concocted functional and structural Description. It really intends now one should choose sort of engineering need to plan, ALU(Address Latch Enable), pipelining and so on [8]. To make it more straightforward to plan a perplexing framework it is regularly separated into a few sub frameworks. The usefulness of these subsystems ought to match the details.

Now, the connection between various sub frameworks high level framework is additionally characterized. That sub part frameworks, high levelled frameworks once characterized, should be executed. It is executed utilizing rationale portrayal limited state machines, Combinatorial, Sequential Logic, Schematics and so on [8]. Fundamentally, the RTL portrays the few sub frameworks. It ought to match the practical depiction. RTL is communicated normally in Verilog or VHDL (Verilog Hardware Description language) [8].

"When Functional Verification is finished, the Register transistor level is changed over into an advanced GLN this progression is called Register transistor logic blend and this is finished by Synthesis tools like blast create, design compiler, register transistor level compiler and so on, a combination apparatus takes a register transistor level equipment depiction and a standard cell library as information and produces a door level netlist as result" [9].

2.1.2 Back End

Physical design is most important step in ASIC/FPGA/SOC design cycle, which mainly aims at manufacturability of the chip with less effort at the Foundry/FAB. The dependency of the Physical design flow on automation has become indispensable. VLSI actual plan incorporates every one of the undertakings expected to construct a silicon chip from configuration net rundown to last GDSII design.

Contrasted with configuration catch, re-enactment, and rationale blend which are called front-end exercises, actual plan is alluded to as back-end work. At the end of the day, actual plan covers the assignments important to divert the plan from a rationale element

into an actual substance [8]. It begins from the net rundown, which is created from the rationale amalgamation Notwithstanding, the actual plan can likewise incorporate the undertaking of RTL rationale amalgamation since there is a consistently expanding tie between the rationale combination and the actual design [9].

The challenges of a VLSI physical designer are good floor plan, good placement of standard cells, well-built clock tree with good insertion delay factor, routing the design with less congestion, timing closure and taping out the chip by following the DRC specifications by the Foundry. Though the tasks are done by tools, making the tools work towards the intended results and extracting the best performance from the tools lies in the expertise and skill of a designer.

2.1.3 Physical Design Flow

"In facilitated circuit plan, genuine arrangement is a phase in the standard arrangement cycle which drags along the circuit plan. At this movement, circuit depictions of the parts of the arrangement are changed over into numerical depictions of shapes which, when delivered in the relating layers of materials, will ensure the normal working of the parts. This numerical depiction is called consolidated circuit design. This movement is ordinarily separated into a couple of sub-steps, which consolidate both arrangement and affirmation and endorsement of the plan" [8].

2.2 Place and Route (PnR)

2.2.1 Introduction to Physical Design (PD) Flow

PD is an important step towards fabrication of an integrated circuit on a silicon wafer. The physical design is performed in two levels. They are PNR Flow and ECO Flow. PNR flow is the most important flow of the physical design where all optimizations like CTS optimization and Routing optimization will be done with the help of tools. The ECO flow is different from PNR where manual corrections are added to the design. These manual corrections can be resolving violations like timing violations or DRC violation fixes.

2.2.2 Place and Route (PNR) Flow

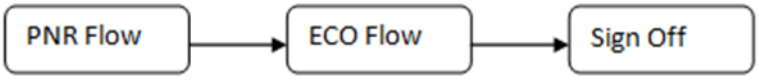

Figure 2.2 Physical design flow chart.

The physical design starts with PNR flow and end at ECO. It involves following sequential steps are

1. Floor planning
2. Placement and Placement optimization
3. CTS and CTS Optimization.
4. Routing and Route Optimization
5. ECO for timing closure

2.2.3 Goals of PNR flow

1. To finalize the Floorplan.
2. CTS optimization.
3. To bring the insertion delay less than or equal to target value.
4. To give best input run to ECO flow with less violations.

CHAPTER 3

PLACE AND ROUTE

3.1 Floorplan

Floor Planning is the principal significant stage in actual plan is that he vital undertakings in this progression incorporate dissecting the bite the dust size, choosing the bundle, putting the I/Os, setting the full-scale cells as memory Cells, simple cells, and exceptional capacity Cells, arranging appropriation force that tickers, apportioning the order [12]. Bite the dust size assessment frequently begins from the door count of the net rundown accessible from the rationale amalgamation process in addition to the actual size of the I/Os and macros. The fundamental prerequisites of a decent floorplan are meeting the predefined use region, painstakingly dissected Macro situation and very much constructed power lattice [13].

3.1.1 Inputs and Outputs of Floorplan

For doing floorplan some basic inputs are required which includes Verilog netlist, partition information from full-chip team, constraints file for checking pre-timing, libraries. The output after floorplan stage is Verilog netlist and def. Figure 3.1 shows the inputs and outputs of floorplan.

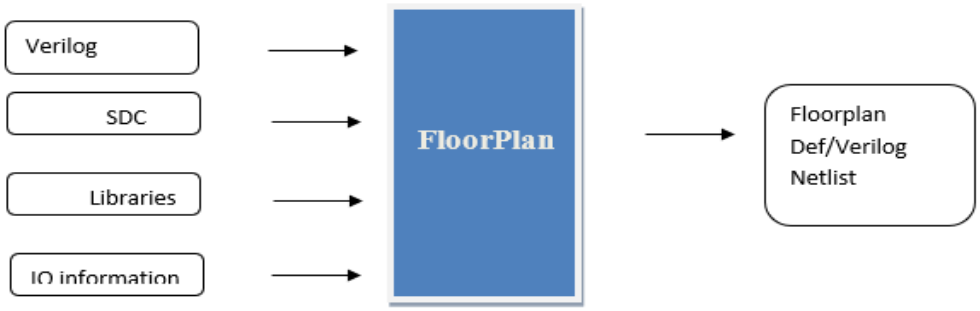

Figure 3.1 Inputs and output of floorplan.

Inputs required-

Parameters of floorplan, physical information of design, pad/io pins position, netlist of logic design.

3.1.2 Utilization

Floorplan utilization are characterized as the proportion of the area of standard cells, macros, and the cushion cells to the region of the chip less the region of the sub floorplan. Contingent on the utilizable region of the plan block the macros and the recollections are set to meet fundamental floorplan objectives (like least clog for standard cells situation). A terrible floor plan will prompt wastage of kick the bucket region and steering blockage. Improving the plan for least region permits the plan to utilize less assets, yet in addition permits the segments of the plan to be nearer together [9].

Aspect ratio (AR): it is the ratio of length to width of macro.

AR=1 that is square.

AR not equal to 1 that is rectangular shape.

Utilization = ratio of standard cell area and macros cell area to total core area.

If utilization of 0.6 means that 60% of the area is available for placement of cells, whereas 40% is left free for routing.

3.1.3 Power Grid

All the cells in the design require power to operate. To distribute power throughout the area Power and ground structure is created. Such a structure is designed to take in power from IO pads and supply it to the core logic and macros present in the design with minimal IR drop (power loss).

These vertical and level fragments are associated through a suitable by means of cut so Interior centre power and ground transport comprises of a couple of sets of wires or strips that rehash at customary stretches across the canter rationale, or determined district, inside the plan [11]. Every one of these power and ground strips run upward, on a level plane, or in the two headings. As such strips run both in an upward direction and on a level plane at customary stretches, this style is known as cross section. Consequently, the construction is known as a Power Mesh. A model should be visible in figure 3.2 and figure 3.3.

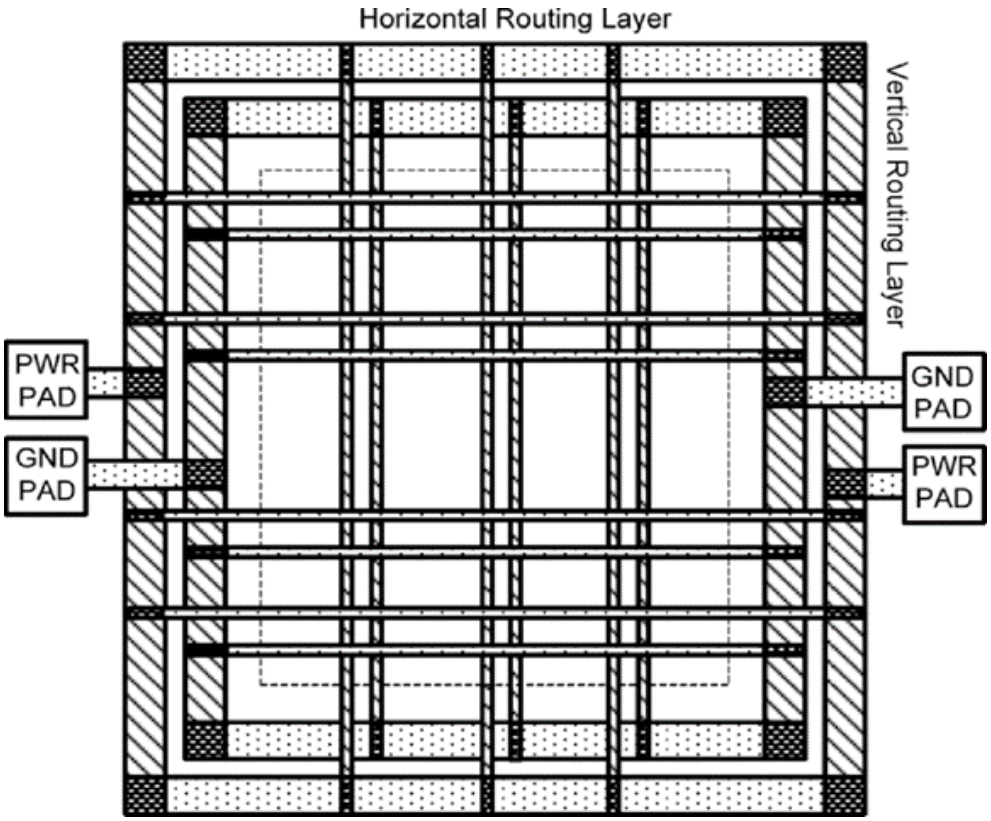

Figure 3.2 Power Mesh horizontal and vertical grid. [11]

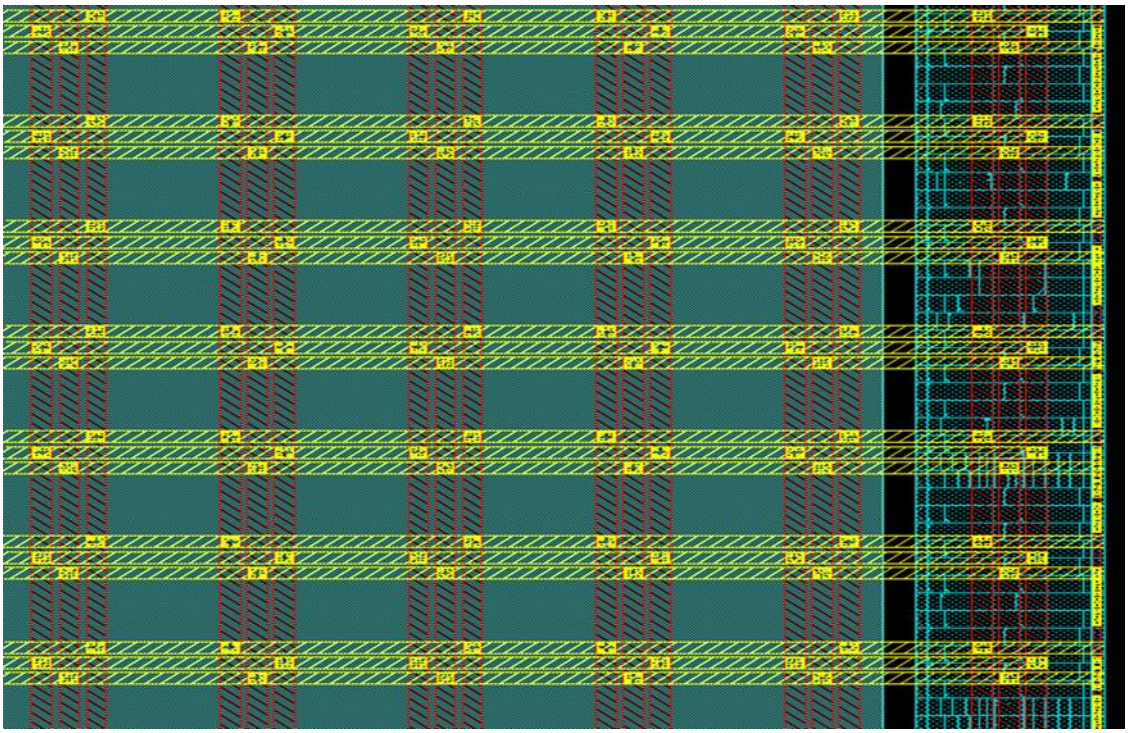

Figure 3.3 Power Mesh creation of block.

3.1.4 Macro Placement

These standard cells are part of modules from the netlist. When module splitting, i.e., cells from the same module are placed apart then floorplan must be reviewed and changed if necessary. Manual macro placement was carried out with available macros. Macro placement requires basic rules to be followed as shown in below figures.

While doing floorplan it is recommended not to leave any isolated pockets. More isolated pockets lead to wastage in core area. So, it is required to follow guidelines given by foundry for better core area. The foundry guidelines include the distance between tile edge and macro, distance between macros, distance between abutting macros, macro channel width etc. Figure 3.4 shows the difference between two different floorplans with and without isolated pockets.

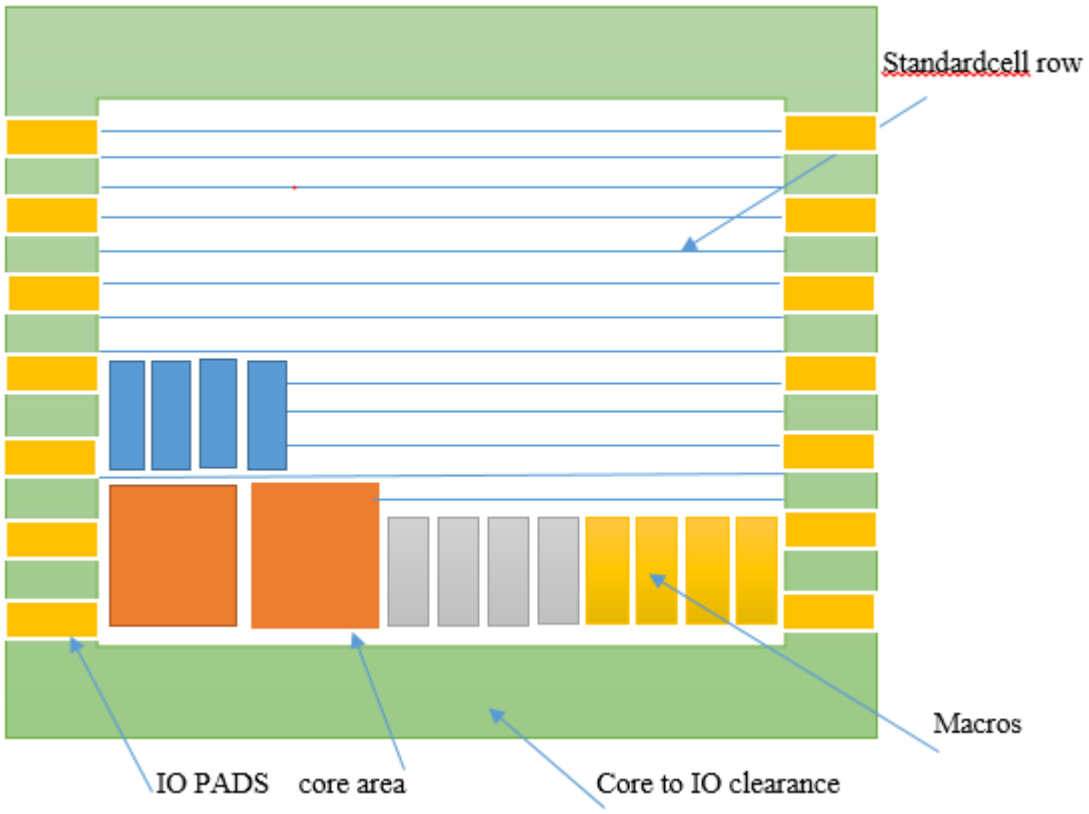

Figure 3.4 Macro's and io placement. [27]

The second important step is to check for module communication shown in Figure 3.5, so Generally, communication between modules is checked by using flight lines. It is mandatory to avoid and overlapping lines in the communication.

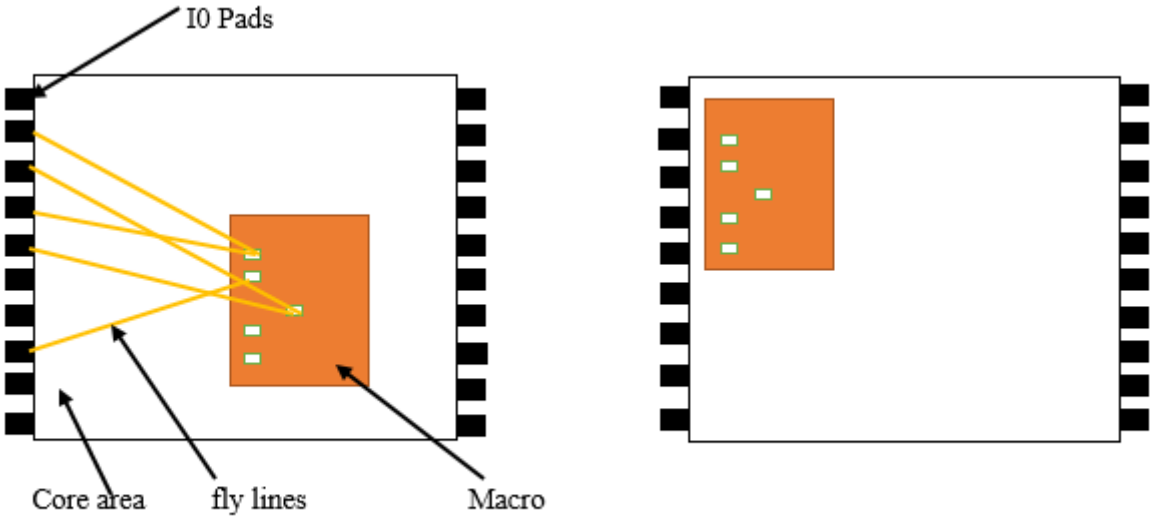

Figure 3.5 Macro and Module communication. [27]

3.2 Physical Cell Insertion

3.2.1 Well (Tap) Cells

Creates and Places TAPCELL's at regular pitch (~30um) on each row. Figure 3.6 shows the tap cell arrangement in core area. It is used for removing latch up issues in design. It creates resistance path between supply to ground.

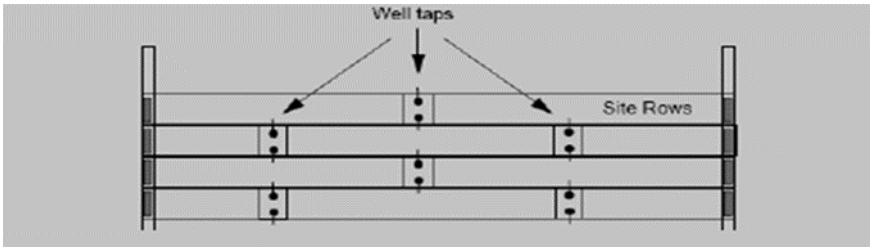

Figure 3.6 well cells creation. [27]

3.2.2 Boundary (End Cap) Cells

Creates and Places ENDCAP cells on every row both ends. Figure 3.7 shows the endcap cells placed in a chip. It is Boundary cell and help restrict design flow of macros.

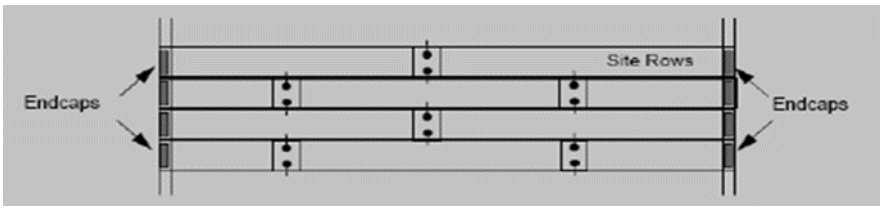

Figure 3.7 Boundary cells creation. [27]

3.3 Placement stage

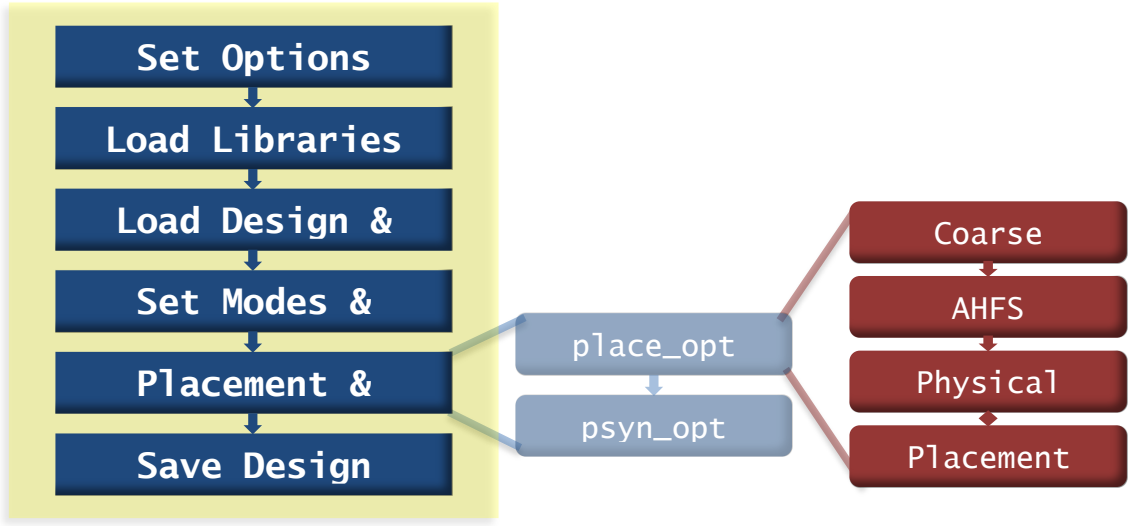

Figure 3.8 Placement flow. [15]

Showing the Arrangement and fundamental stage in electronic plan computerization of CTS shown in Figure 3.8. The objective of standard cell arrangement is to plan application specific integrated circuit parts, onto places of the application specific IC centre region, or standard cell situation district, which is characterized by columns" [15]. The standard cells should be set in the allocated district with the end goal that the ASIC can be directed productively and the general timing prerequisites can be fulfilled.

3.3.1 Total wire-length at placement stage

"Limiting the complete interconnect length, and amount of interconnection the relative multitude in the plan, is the essential target of most existing placers. This not just limits chip size, and subsequently cost, yet additionally limits power and postponement, which are corresponding to the wire length" [21].

3.3.2 Timing Violation

The timing violation are occurred in data path, clock path on depending on arrival and required time with respect to the setup violation and hold violation of the logic path [18].

3.3.3 Congestion check

“While it is important that limit the absolute wire length to meet the all-out directing assets, it is additionally important to meet the steering assets inside different neighbourhood districts of the chip's centre region a blocked locale could prompt over the top directing diversions, or make it difficult to finish all courses” [16].

3.3.4 Power analysis

Power minimization ordinarily includes disseminating the areas of cell parts in order to decrease the general power utilization, mitigate problem areas, and smooth temperature inclinations. An auxiliary goal is arrangement runtime minimization Placement Tool does the undertaking in two phases [17].

3.3.5 Inputs and outputs of placement stage

Arrangement stage requires floorplan DEF, netlist, innovation documents, and imperatives as information sources. Furthermore, it will give yield DEF and Verilog. It will likewise produce a few timing reports and blockage reports. Figure 3.9 gives a concise view about arrangement information sources and results.

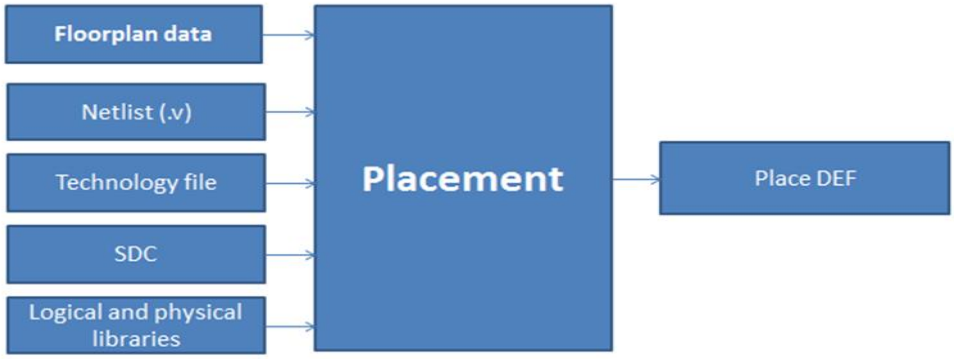

Figure 3.9 Inputs to the placement stage.

Inputs required:

Constrain file in term of timing, and information of power in upf file and floorplan file.

Outputs:

Output is different report like timing, congestion and legalization of placement.

3.3.6 Post Placement

In this stage, standard cells are placed on the basis of communicating logic and these are not placed in fixed and legal locations. The main goal of this placement is to ensure that the cells are placed in approximate initial locations on the die. It is important to carry out this step first because knowing the location of cells is critical to estimate timing and congestion or buffering requirements [16].

3.3.7 Detail Placement

During the global placement stage, there are possibilities of cells overlapping and cells not being placed on the standard cell placement grid. These issues are taken care of in the Detail placement stage. In this process the tool finds the nearby available legal locations for the cells to be placed. The detail placement is done on the basis of timing driven or congestion driven placement [16]. During Placement, tool will optimize DRVs (design rule violations) and Setup and we will have ideal clock.

3.3.8 Path Grouping

“The timing ways of the plan are coordinated into bunches called way bunches of course, there is one way bunch for each clock in the plan and all timing way timed by a given clock at the way endpoint have a place with that clock's way bunch” [20]. A plan that has just a solitary clock has just a single timed way bunch, so completely timed ways in the plan have a place with that gathering.

3.4 Clock Tree Synthesis

It is the way of inserting buffer/inverter to minimise the skew and insertion delay of design along the clock paths and optimizing the clock network [30].

3.4.1 Inputs & Outputs of CTS

As shown in Figure 3.10 the basic inputs to the CTS stage are placement stage DEF and technology library, constraints, cts spec file where in all the stop pins, exclude pins and some exceptions are defined.

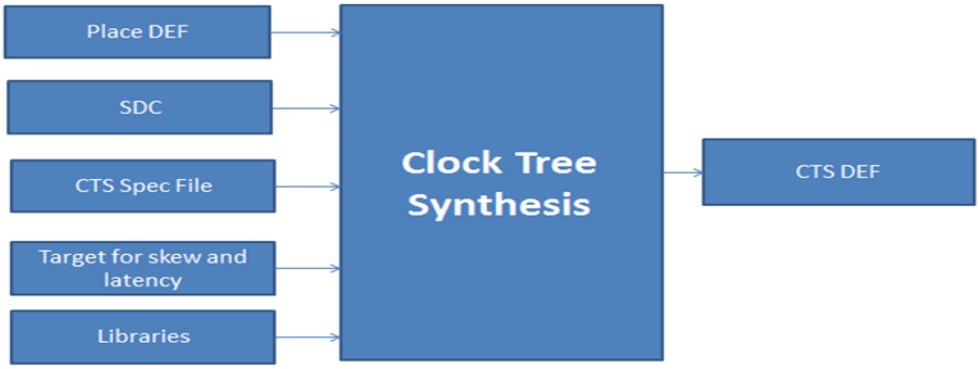

Figure 3.10 Inputs to the CTS stage.

3.4.2 Timing Analysis

Timing investigation is indispensable piece of application specific IC configuration stream. Whatever else can be compromised however not timing. Timing investigation is the calculated examination of a computerized circuit to decide whether the timing requirements forced by parts or points of interaction are met [25]. Ordinarily, this implies that checking whether all setup and hold timing are met or not.

3.4.3 Two Types of Timing are analysed

1. Static Timing Analysis: The time which are analysed any logic path so does not apply any input or functionality syntax.

2. Dynamic Timing Analysis: It analysed the path where the functionality or input of path given.

3.4.4 Path of timing

There are basically following way path to analysed are clock path, data path and Asynchronous path and clock gating path.

Checking Data path – they have following way analysed timing are Input pin to flip flop D pin, input pin to output pin, CLK pin flop to D pin flop and CLK pin of flop to output pin. Here we check WNS (Wurst Negative Slack), TNS (Total Negative Slack) and NV (Number of Violating) of each path.

Different paths are explained in figure 3.11 which shown below

Path 1- Input port to Register.

Path 2- Register to Register.

Path 3- Register to Output port.

Path 4- Input port to Output port.

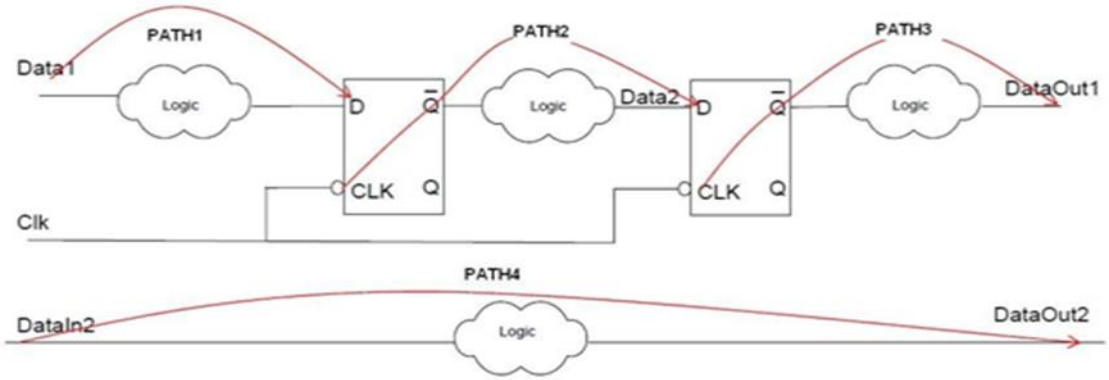

Figure 3.11 four types of data paths. [25]

Checking clock path

Source Point: CLK pin port

Sink Point: CLK pin of the flip-flop/memory of sequential cell

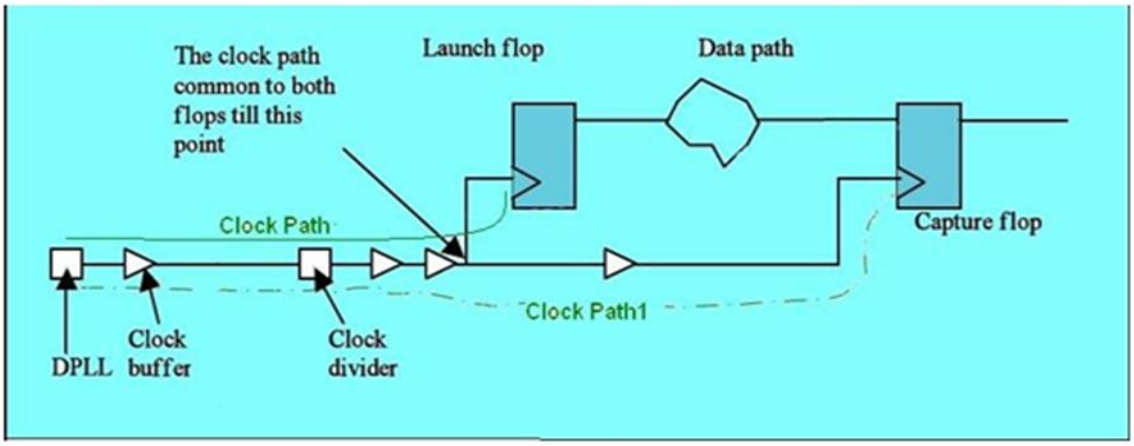

Figure 3.12 Clock Path. [27]

In the above fig 3.12 obviously clk way the beginnings from the information pin/port of the plan which is explicit for the clk input and the sink point is the clock pin of a consecutive component in the middle of between the Source point and sink point there might be bunches of inverter or buffer or clk divider [27].

Checking Clock Gating path

Source Point: Input port of the design.

Sink Point: Input port of clock-gating element.

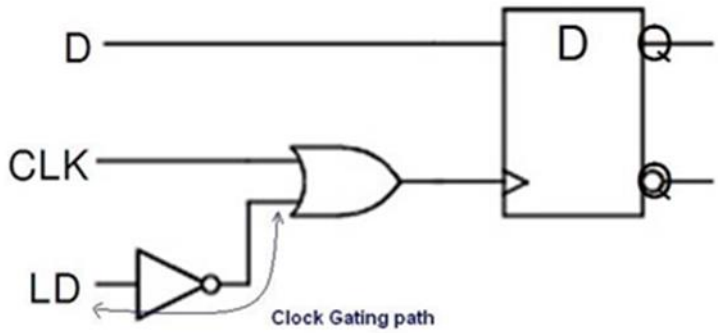

Figure 3.13 Clock gating Path. [27]

“As in the above fig 3.13 input given to inverter are LD pin isn't a piece of any clk however it is utilizing for gating the first CLK signal. Such sorts of ways are neither a piece of Clock way nor of data path in light of the fact that according to the source Point and sink Point meaning of these ways, it's unique Along these lines, such kind of ways is essential for Clock gating way” [27].

Checking asynchronous path

Source Point: Input Port of the design.

Sink Point: Set/Reset/Clear pin of the flip-flop/latch/memory of sequential cell.

A way from an information port to a nonconcurrent set or clear pin of a consecutive component. See the accompanying fig 3.14 for seeing obviously as the usefulness of set/reset pin is autonomous from the clock edge its level set off pins and can begin working whenever of information [27].

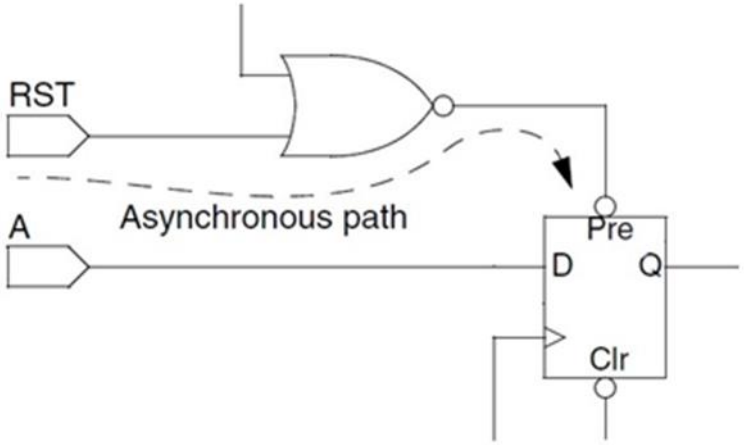

Figure 3.14 Asynchronous path. [27]

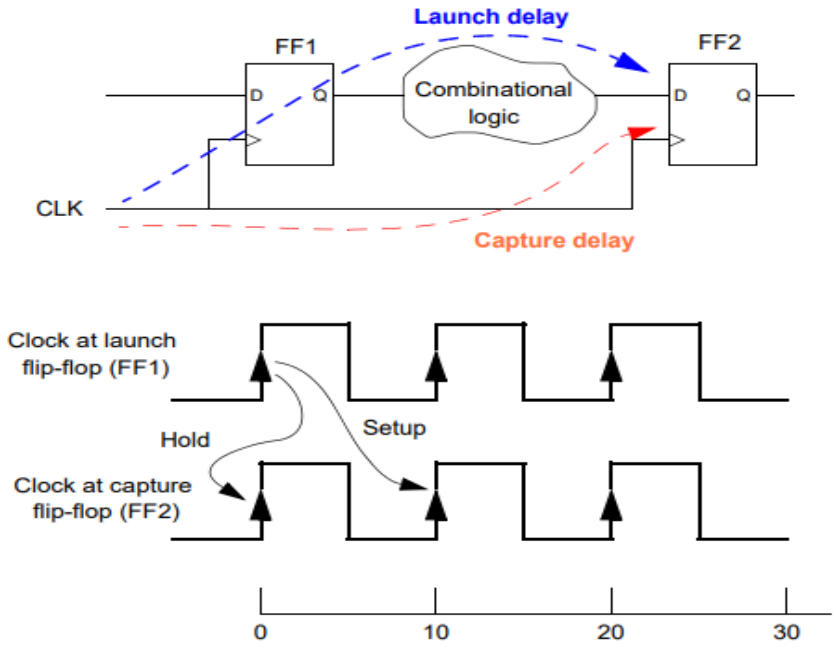

Figure 3.15 Setup and Hold Analysis for the Same Launch and Capture Clock.

Setup Timing: Minimum time interval for which the input signal must be stable before the active edge of clock. For no set up violation it must be follow the equation (i).

Tclk-q+Tcomb. <= Tclk-Tsetup+Tsetup uncertainty ……. (i)

Hold Time: Minimum time interval for which the input signal must be stable after the active edge of clock. For no hold violation it must follow the equation (ii).

Tclk-q+Tcomb.>= Thold+Thold uncertainty ……(ii)

3.4.5 OptCTS: The OptCts (post-CTS) is the step where the setup, hold, DRVs are optimized with propagated Clock.

3.5 Routing

After the clock tree is built, precise regions pins and cells are fixed and the ensuing stage is to really complete the interconnections described in the netlist this recommends using metals wire to communicate the associated terminals inside each net the strategy engaged with find out numerical plans for the nets is known as routing an essential, the nets are coordinated inside a limited area [23]. Furthermore, nets should not be short-circuited. At the end of the day, the nets should not electrically converge one another. The target of the directing system relies upon the idea of the plan. “While worldwide directing analyses the format in the extent of whole chip, point by point steering thinks about only each district in turn in this stream, there are four stages of directing activities are Track Assignment, Global Routing, Detail Routing and Search and Repair” [24].

3.5.1 Global Routing

Worldwide directing is the disintegration of application specific IC plan interconnections into net fragments and the task of these net portions to districts without determining their genuine formats [24]. These directing districts are ordinarily called Global Routing Cells.

3.5.2 Track Assignment

Track Assignment relegates each net to a particular track and genuine metal follows are set somewhere around it so it attempts to make long, straight follows to stay away from enormous number of vias of DRC (Design Rule Check) isn't continued in Track assisment stage [24].

3.5.3 Detailed Routing

The target of detail directing is to follow the worldwide steering and play out the genuine interconnections of application specific IC plan so along these lines, the detail switch puts the genuine wire fragments inside the district characterized by the worldwide switch to finish the necessary associations between the ports [24].

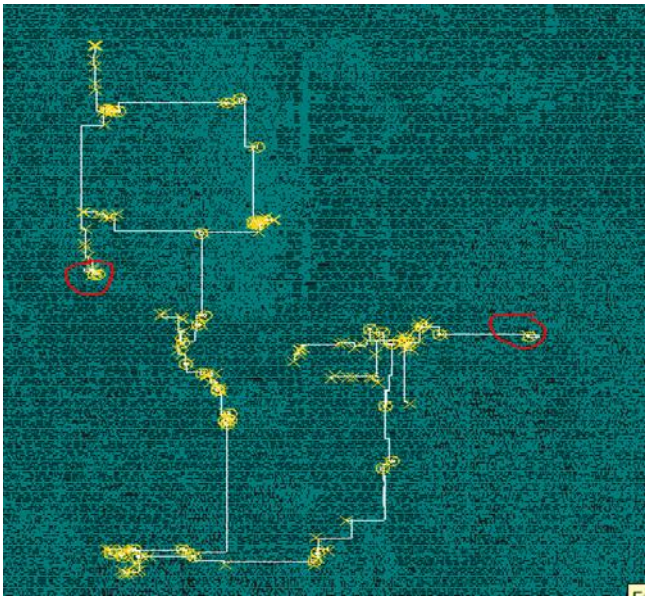

Figure 3.16 Tracks and Detail routing using grids.

Detail switches utilize both level and vertical directing frameworks for genuine steering. The tracks and frameworks for point-by-point directing are displayed in the above figure 3.16.

3.5.4 Inputs & Output of Routing

For routing it is required to have CTS DEF, Verilog, and tluplus file, constraints, and routing algorithms information, physical libraries shown in Figure 3.17.

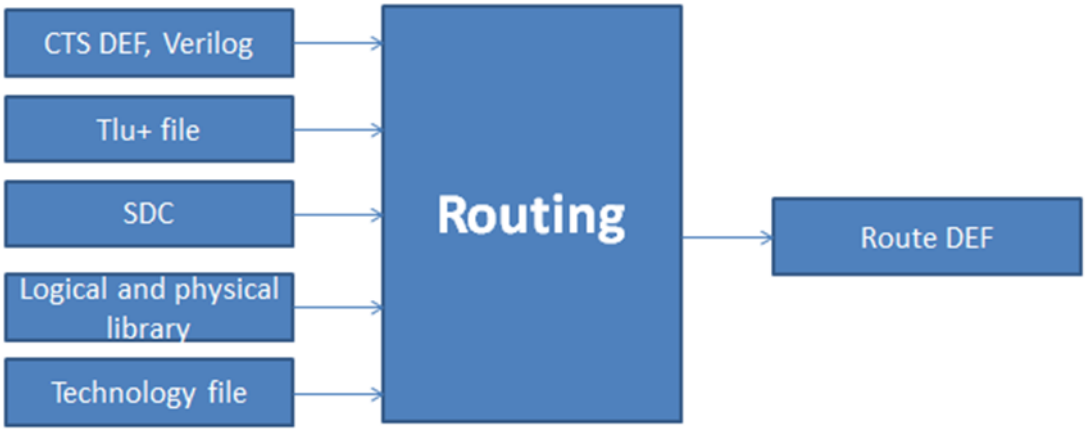

Figure 3.17 Inputs and output to routing stage.

3.5.5 OptRoute: At this stage., both timing and the Routing DRCs are optimized. It will try to reduce cross talk interference, shorts, DRCs, antenna etc.

3.6 Extraction

"Parasitic extraction is the computation of all directed net capacitances and protections with the end goal of postpone estimation, static timing investigation, circuit reproduction, and sign trustworthiness examination" [20].

3.6.1 Capacitance and Resistance values from Foundry

To extricate capacitance wires and obstruction, the from designer give the value of capacitance and their position of RC value and opposition values for different electrical boundaries capacitance coefficient and sheet obstruction depend on estimations performed utilizing test-keys from genuine silicon information for best, ostensible, and most horrendously terrible interaction conditions or corners [20].

3.6.2 Standard Parasitic Extraction Format (SPEF)

Quite possibly the most ordinarily utilized design take value of RC commodity appropriated RC parasitic capacitance and obstruction values extricated per net in light of their genuine calculation and layer width and dispersing data, SPEF for determining chip parasitic. Subsequently many apparatuses support import/commodity of SPEF for communicating with other parasitic extraction motors and different instruments [27].

3.7 Routing Issues

Routing issues arise because of bad inputs from its previous stage, which includes bad Floorplanning and congested module placement. Some of the routing issues include long nets, detouring nets, design rule violations, signal integrity violations like glitches, double switches etc.

3.7.1 Long Nets and Detouring Nets

Long nets and bypassing nets are available in the plan since terrible directing done by the instrument. For the most part, this issue emerges as a result of deficiency in directing assets. Rerouting nets are dispensed with by eliminating the current endlessly directing the net again physically or by giving it to the instrument. Long nets are made short by adding supports to the net.

3.7.2 Signal Integrity Violations

"Signal trustworthiness is the capacity of an electrical sign to convey data dependably and oppose the impacts of high-recurrence electromagnetic obstruction from neighbouring signs so Crosstalk commotion is frequently instigated in lengthy interconnects running lined up with one another now there emerges a need to limit the impact of these crosstalk commotion in order to keep up with the sign trustworthiness in interconnects" [28].

3.8 Physical Verification

Once the entire place and route flow is done, in correctness of the layout design is to be checked which is done in the Physical Verification stage. Physical Verification step involves three types of checks. They are

3.8.1 Design Rule Checking (DRC)

This rule check ensures the manufacturability of the design. It involves many checks provided by the fabrication unit. These checks vary according to the foundries and include parameters such as spacing between the geometries, density of the metals, minimum area rules etc.

3.8.2 Layout vs. Schematic (LVS)

LVS is the process where it is including the Comparisons and Extraction of schematics and layout netlist. So, there are common issues in layout vs schematics are-

- Component Missing
- Shorts
- Global net connects missing
- open

3.8.3 Electrical Rule Checking (ERC)

ERC includes checks a plan for all signal associations that are thought of as hazardous for the working of the IC so for this could incorporate checking for well and substrate regions for appropriate contacts and dispersing along these lines guaranteeing right power and ground associations, detached inputs or shorted results and entryways associated straightforwardly to provisions [26].

3.8.4 Antenna Rule Checking

In that we will check the antenna violation occurred when huge amount of charge flow through metal interconnect which connected to Gate of transistor when plasma etching caused the oxide gate are damaged [26]. Different way to prevent antenna violation are

- Using Antenna Diode
- Using floating gate are attached
- Using Metal Hopping

CHAPTER 4

LOW POWER DESIGN AND TECHNIQUES AND ECO

4.1 Global Power View

System on Chip (SoC) architects are design of Block need an early and accurate global view of chip power consumption that guides decisions on the selection of the fabrication process and the configuration of the Silicon Intellectual Property (Silicon IP) that is embedded into the IC in the form of compiled memories, soft IP blocks, hard IP blocks and high speed I/Os. As the continually growing array of process variants and IP options becomes unwieldy, the design team needs a common view of the conflicting and interrelated requirements that link power to other chip metrics such as area, speed and cost.

The below figure 4.1 shows how power is distributed to different parts of a SOC, where most of the power is consumed by logic. Again, the logic power is divided into two major components as static and dynamic power. The detailed explanation of power consumption is presented in below sections [24].

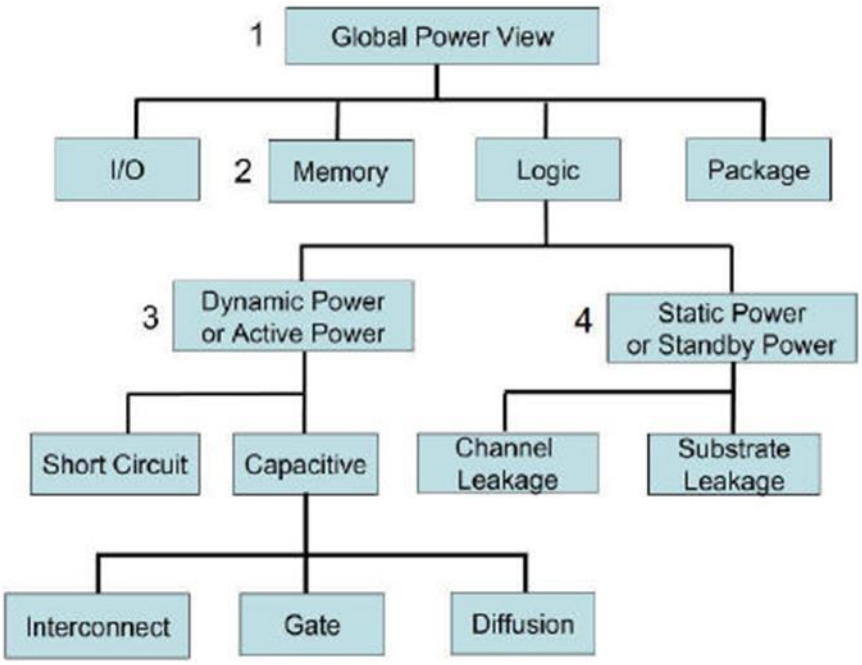

Figure 4.1 Global View of Chip Power. [27]

4.1.1 Defining Static Power

Static power is the power disseminated by an entryway when it isn't exchanging, that is to say, when it is dormant or static. Static power is disseminated in more ways than one. The biggest level of static power results from source-to-deplete subthreshold spillage, which is brought about by diminished limit voltages that keep the entryway from totally switching off [23].

4.1.2 Gate Tunneling leakage (Igate)

The spillage part IGIDL is Gate Induced Drain Leakage current. Since the semiconductor is switched off, there is voltage distinction between the entryway and the channel terminals [24]. This electric field makes some flow stream from the channel into the substrate. IGIDL increments as TOX becomes slenderer and it additionally increments with temperature. The last part is the opposite predisposition diode spillage from the channel into the substrate. It additionally increments dramatically with temperature [24] and the behaviour shown in Figure 4.2.

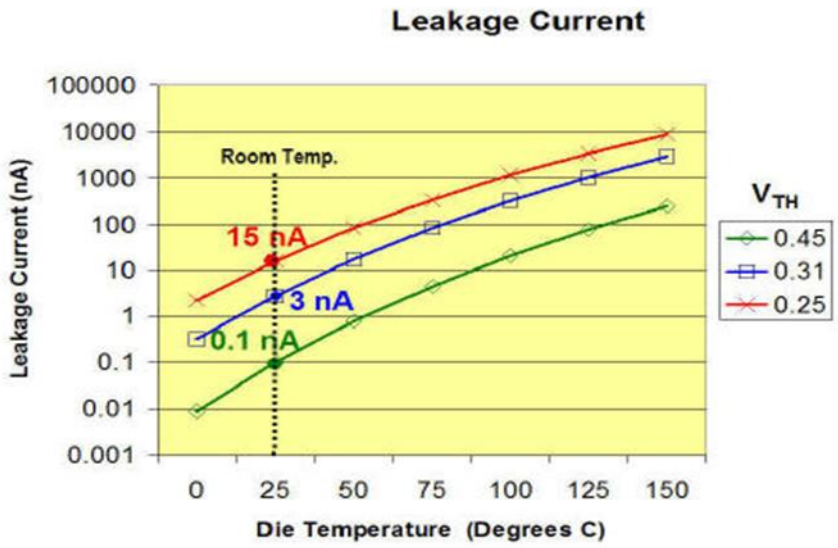

Figure 4.2: Leakage Current with V_th and Temperature. [24]

4.1.3 Dynamic power

“Dynamic power is the power disseminated when the circuit is dynamic that is a circuit is dynamic whenever the voltage on net changes because of some improvement applied to the circuit Since voltage on an information net can change without fundamentally bringing about rationale progress on the result, dynamic power can be disseminated in any event, when a result net doesn't change its rationale state” [24]. Consequently, most

low power design flows centre their implementation strategy on reducing dynamic power. Following figure shows the design parameters for dynamic power.

P_D= (C_Diffusion+C_Fanout+ C_wire)*∝*F*V_DD^2

Were,

P_D=Dynamic Power

C_Diffusion=capacitance of output transistors

C_Fanout=Capacitance of input transistors of the next stage

C_Wire=Capacitance of the interconnect wires

∝ =How often,on average,do signals switch

F = Applied clock frequency

V_DD^2=Applied Voltage

4.1.4 Switching Power

The exchanging force of a driving cell is the power disseminated by the charging and releasing of the heap capacitance at the result of the cell. The absolute burden capacitance at the result of a driving cell is the amount of the net and entryway capacitances on the driving result. Since such charging and releasing are the consequence of the rationale advances at the result of the cell, exchanging power increments as rationale changes increment [24]. Along these lines, the exchanging force of a cell is a component of both the complete burden capacitance at the cell yield and the pace of rationale advances and how the transition take place shown in Figure 4.3.

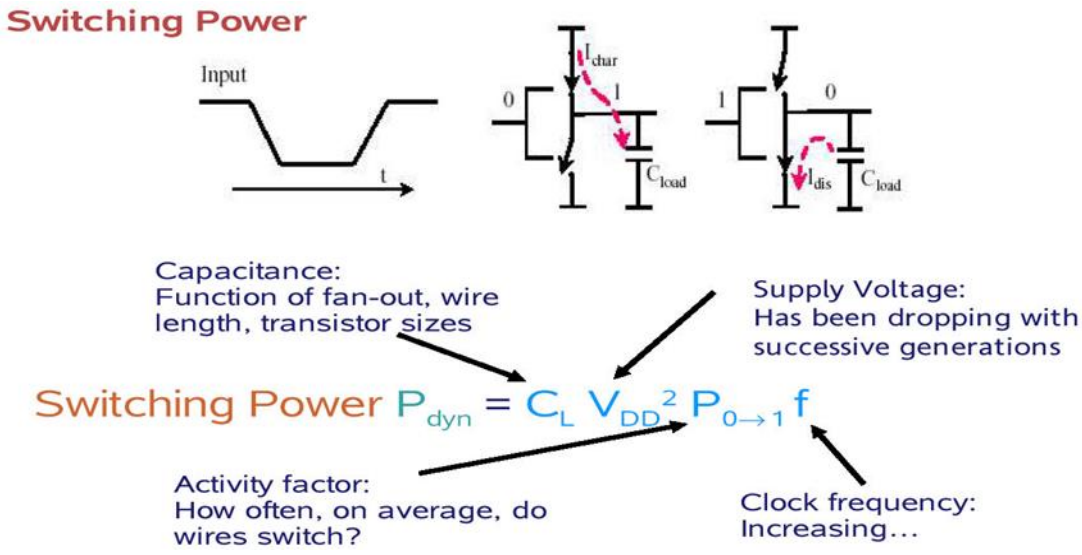

Figure 4.3 Switching Power behaviour shown. [30]

4.1.5 Internal Power

As shown in the following figure 4.5 when the input to a gate is driven by an undersized driver, the input transition time increases and excess short circuit current flows as the ISC current spike becomes wider [26].

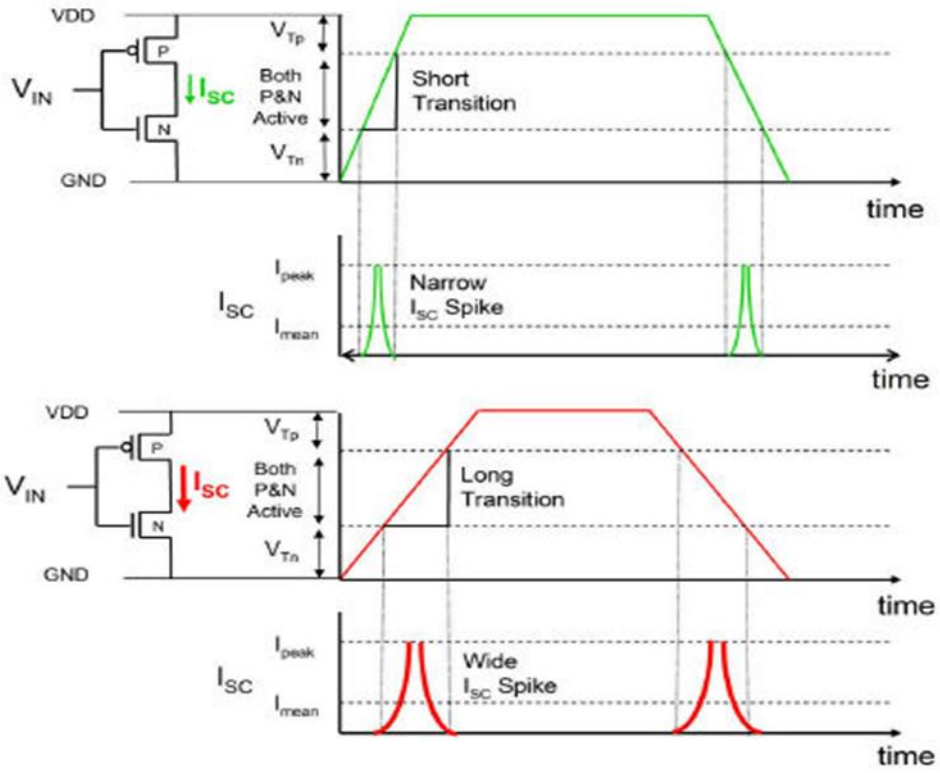

Figure 4.4 Long transition times on a logic gate's input leads to excess short circuit current. [30]

Sizing a logic gate so that its input and output transition times are about equal, can reduce the short-circuit power dissipation. Static Timing Analysis (STA) checks for long transition times and In Place Optimization (IPO) is used to resize the drivers to exactly match the gate size to the load.

In modern ASIC libraries, a wide variety of gate sizes from ½X to 16X drive strength are offered for all of the common logic gates. In addition, an inverting input is offered for all the basic gates and there are 48 driver strengths for inverters shown in Figure 4.4. This wide selection of gates offers the ability to match the input and output transition times reducing short circuit power dissipation. Note that gate resizing optimization in terms of minimizing PSC usually leads to a different gate size than would be selected for propagation delay minimization.

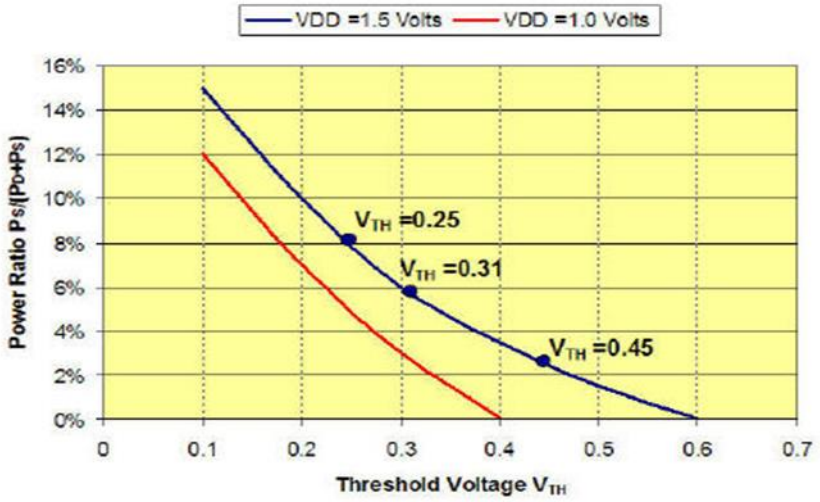

Figure 4.5 Short circuit power < 10% of total power. [30]

As gate length decreased to 90 nanometres, up to half the power consumption can be caused by static leakage, as shown in the figure 4.5 and Behaviour of dynamic power, leakage power are shown in Figure 4.6.

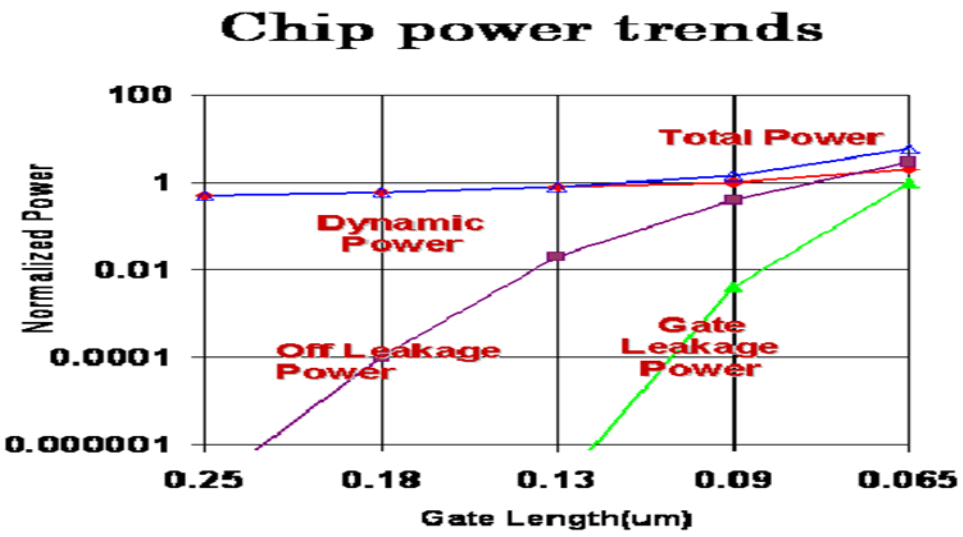

Figure 4.6 Chip power Trends. [30]

4.2 Low Power Design Technique

There are a few different RTL and entryway level plan methodologies for diminishing power dissemination in CMOS circuit plan so there is a few strategies, for example, clock gating, have been utilized generally and effectively for a long time. Others, for example, dynamic voltage and recurrence scaling, have not been involved much in that frame of mind due to the troublesomely of carrying out them. As power turns out to be progressively significant in trend setting innovations, more techniques are being taken

advantage of to accomplish the plan prerequisites a couple of these strategies are talked about in the succeeding segments.

4.2.1 Clock Gating

The Clock tree power in a circuit is mainly design dependent and can amount to approximately 40%-50% of the total power dissipation in a chip. The most effective method to reduce the clock dynamic power is by gating the clock signals for chosen register banks during times when the put away rationale values are not evolving One potential execution of clock gating is displayed in Figure 4.8 [24].

4.2.2 Multiple-Vt Library Cells

Some CMOS advancements support the manufacture of semiconductors with various limit voltages (Vt values) All things considered, the cell library can offer at least two distinct cells to carry out every rationale work, each utilizing an alternate semiconductor limit voltage [25]. Spillage power effect can be significant diminished by utilizing such multi-limit gadgets are low-Vt Transistors (LVT), standard-Vt semiconductors (SVT) and high-Vt semiconductors (HVT).

4.2.3 Multi-Voltage Design

In down to earth situations, the speed prerequisites fluctuate across a chip. For instance, the CPU and RAM squares could should be quicker than a fringe block.

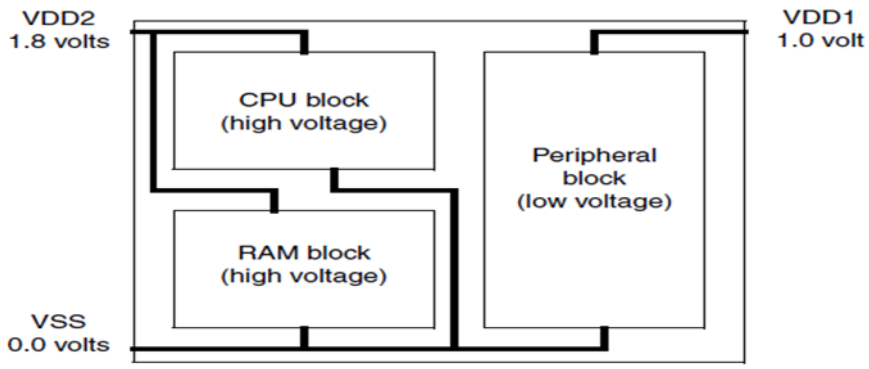

Figure 4.7 Multi-voltage chip Design.

As referenced before, a lower supply voltage diminishes power utilization as well as decreases speed. To receive the rewards of both speed and power, the CPU and RAM can be worked at a higher inventory voltage while the fringe block works at a lower voltage, as displayed in Figure 4.7.

This leads to two effects are

Extra gadget pins are expected to supply the ideal chip voltages, and the power framework should be intended to disseminate every one of the voltages supplies independently to the suitable squares. At the places where a rationale signal leaves one power space and enters another, on the off chance that the voltages are fundamentally unique, a level-shifter cell is important to produce a sign with the appropriate voltage swing which are shown in figure 4.8.

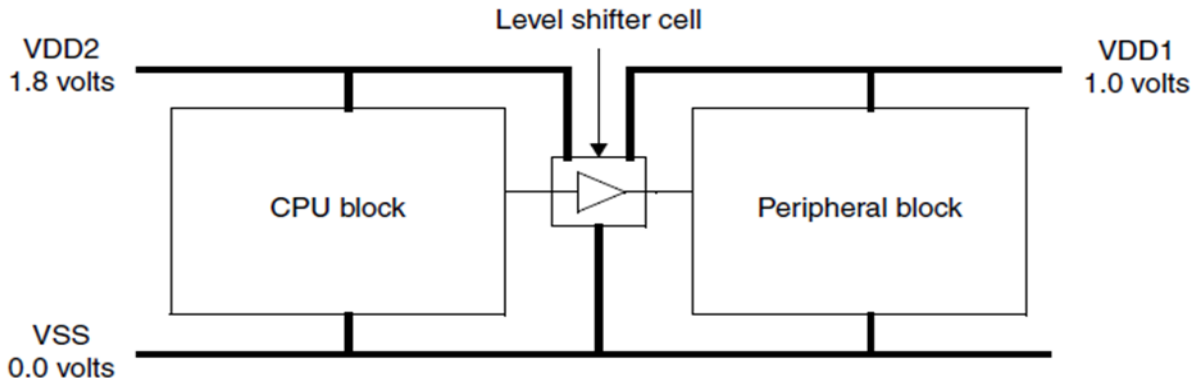

Figure 4.8 Level Shifter

4.2.4 Power Switching

"At Power changing gives the capacity to decrease the general power utilization significantly in light of the fact that it brings down spillage power as well as exchanging power and it likewise presents a few extra difficulties, including the requirement for a power regulator, a power-exchanging network, disengagement cells, and maintenance registers" [28]. To limit spillage, High-Vt semiconductors from a Multiple-Threshold CMOS (MTCMOS) innovation are utilized for the power switches and furthermore in light of the fact that their exchanging speed isn't basic so PMOS header switches can be put among Vdd and the square power supply pins, or NMOS footer switches can be put among Vss and the square ground pins, as displayed in Figure 4.9 and inserting isolation between two voltage domain shown in Figure 4.10 and retention register shown in Figure 4.11. During top power utilization in the square, to give satisfactory voltage drop, the number, the drive strength, and arrangement of switches ought to be selected cautiously [25].

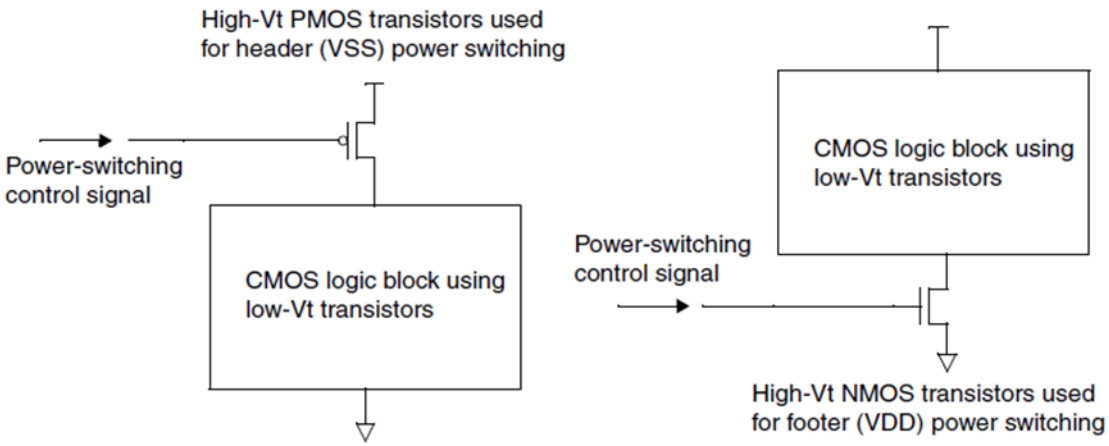

Figure 4.9 Power Switching Network Transistors.

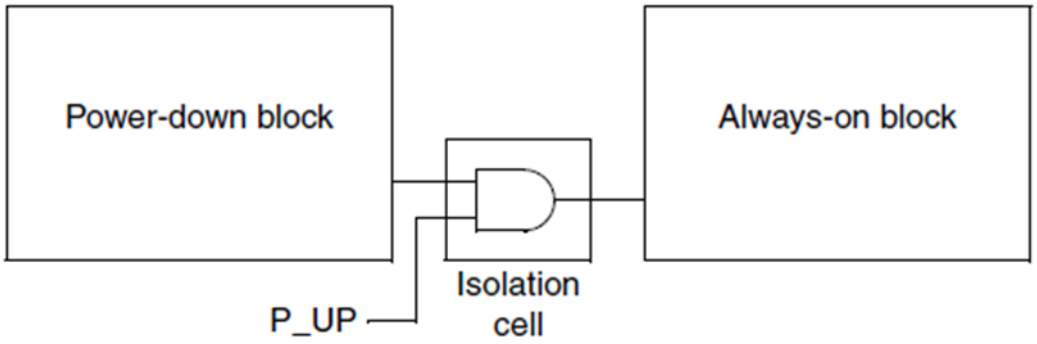

Figure 4.10 inserting isolation cell between two domains.

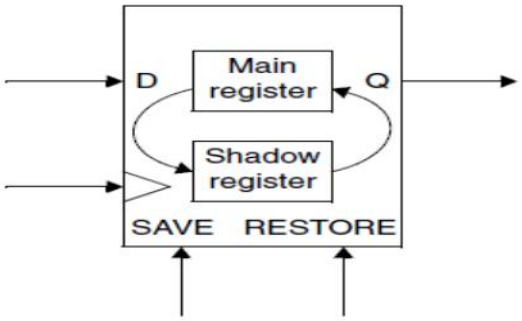

Figure 4.11 Retention Register.

4.3 HVT cells without leakage optimization flow

After the synthesized netlist in which all the cells are RVT cells, in this flow methodology the initial netlist is hacked and all the RVT cells are changed to HVT cells and is pushed down to the place and route flow stages. In this flow the leakage power optimization is not enabled. Inputs & Output of Routing is optimization resulted in congestion critical

and area critical design as only HVT cells were used. These cells added degraded timing to a greater extent due to which a greater number of inverters and buffers were added by the tool at optimization stages, resulting in a huge increase in the total instance count of the design. No significant power savings were seen in this case [25].

4.4 HVT cells with leakage optimization flow

The netlist used for the flow consists of only HVT cells. In this flow method leakage optimization is enabled during all the optimization. It is observed that this method resulted in better power savings compared to the flow methodology of HVT cells and without leakage optimization flow. Also, it is observed that there was increase in the area utilization without much timing degradation.

4.5 Engineering Change Order (ECO)

ECO is the most common way of altering the PNR Netlist to meet timing prerequisites. For example, assuming there's an arrangement infringement in the plan, it suggests that a combinational way has enormous postponement than required. For this situation, we want to diminish the postponement by levelling up cell, which decreases opposition, thusly, lessens RC deferral of the way [9].

CHAPTER 5

RESULTS

5.1 Floorplan

Floorplanning guidelines for placing Macro's are

1. Macro Groupings as per modules.
2. Macro Placement considering IO ports.
3. Macro Placement considering Feedthrough's.
4. Recommended to Place Macros on the Tile edges.
5. Allow Spacing between Macros and Tile edges.
6. Macro pins connections and Orientation.
7. Macro Pins should face towards core-area.
8. Aim for Contiguous Modules.

Goals:

• Minimum congestion

• Meet the timing

Below Figure 5.1 and Figure 5.2 shows two stages of floorplans, Figure 5.1 is initial floorplan of dcn_opp_t block we get some bad results then we trying too many floorplans to achieve our goals, fig 5.2 is taping of power grid floorplan we get good results respectively fig 5.1. The main difference between two stages floorplans is the module placement, connectivity and clock_mesh_cts_root buffers moved to middle of the block, to reduce source latency.

Placing Macro's

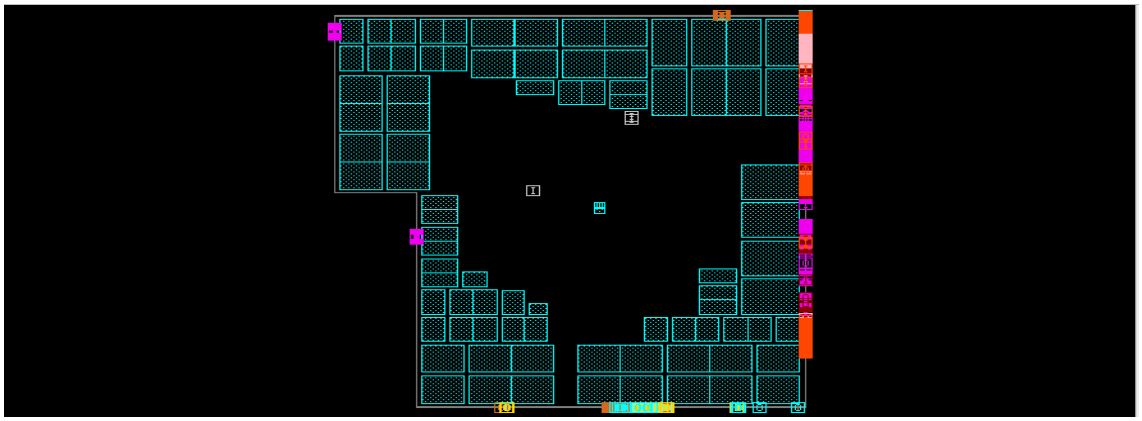

Figure 5.1 Macros Placement this experiment.

• Macro and IO-pin placement

• Internal power grid creation

• Physical cell insertion

• Power gaters insertion

• Insert clock mesh cts buffers

• Taping of power gaters

• Macro power hook-up

• power ground ring creation

Physical cells around the macro

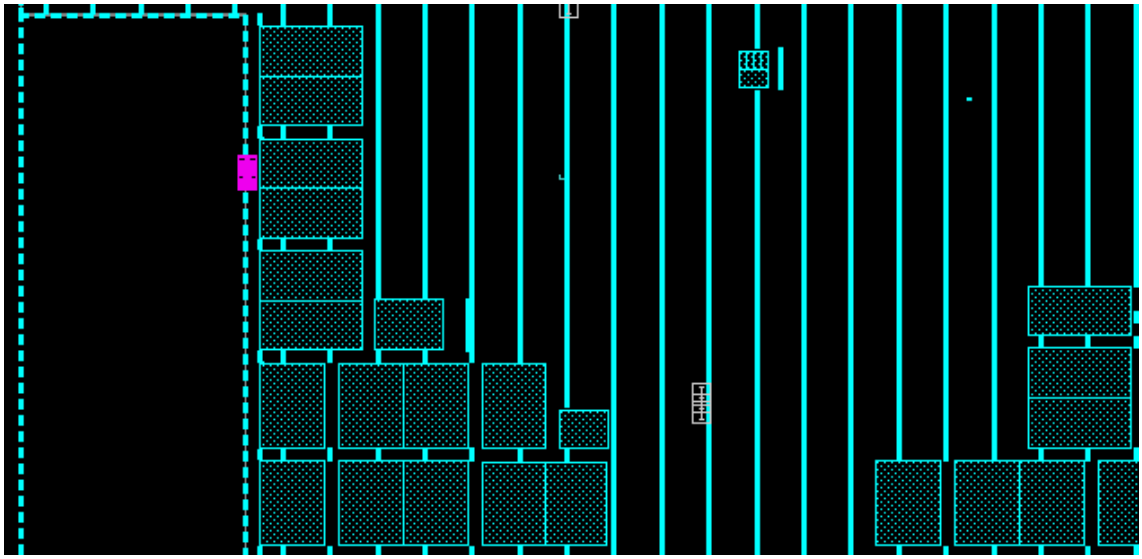

Figure 5.2 Floorplan where the Tap cell and Endcap cells are formed.

Multi-Voltage Regions

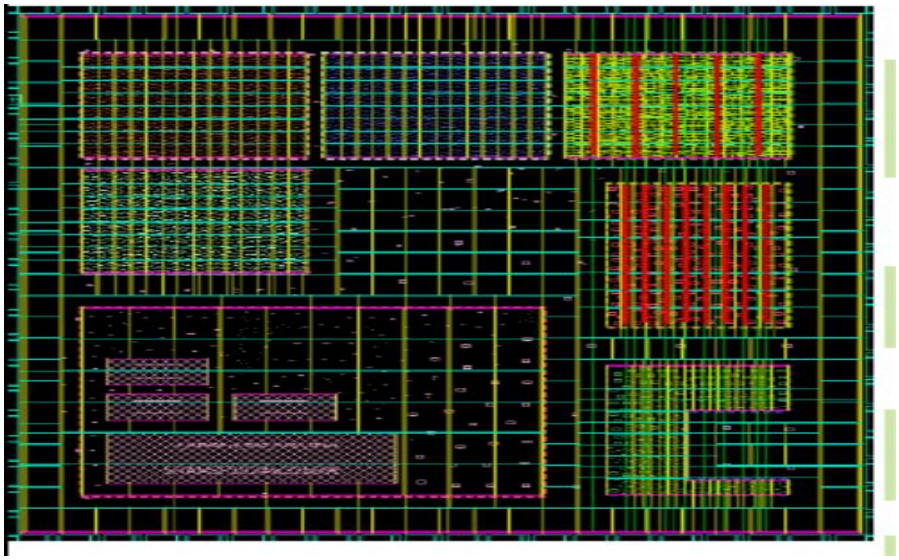

Figure 5.3 Multi voltage region are formed.

Switch Cells Insertion

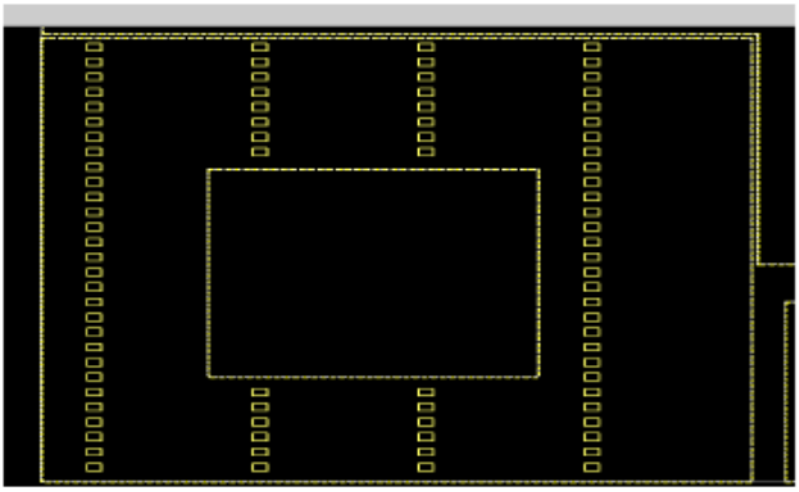

Figure 5.4 Switch cells inserted is formed.

5.1.1 Blockage at Floor Plan

The hard blockage is added at the macro channels in order to prevent the placement of logic cells and flops in the macro channels.

Command used: finish Floorplan -fill Blockage Hard 19 create_placement_blockage -name soft_1 -type soft -bbox {-4609.8 -3490.923 -4307.5 -3489.8}

5.2 Standard Cell Placement

Standard cells are placed according to the module communication. The main aim of the placement is to get uniformity in the module placement. There should not be any spitted module because these split modules can cause bad timing.

As shown in figure 5.6 There is no module splitting in the shown placement diagram. And modules which are near to the macros will communicate with respective macros.

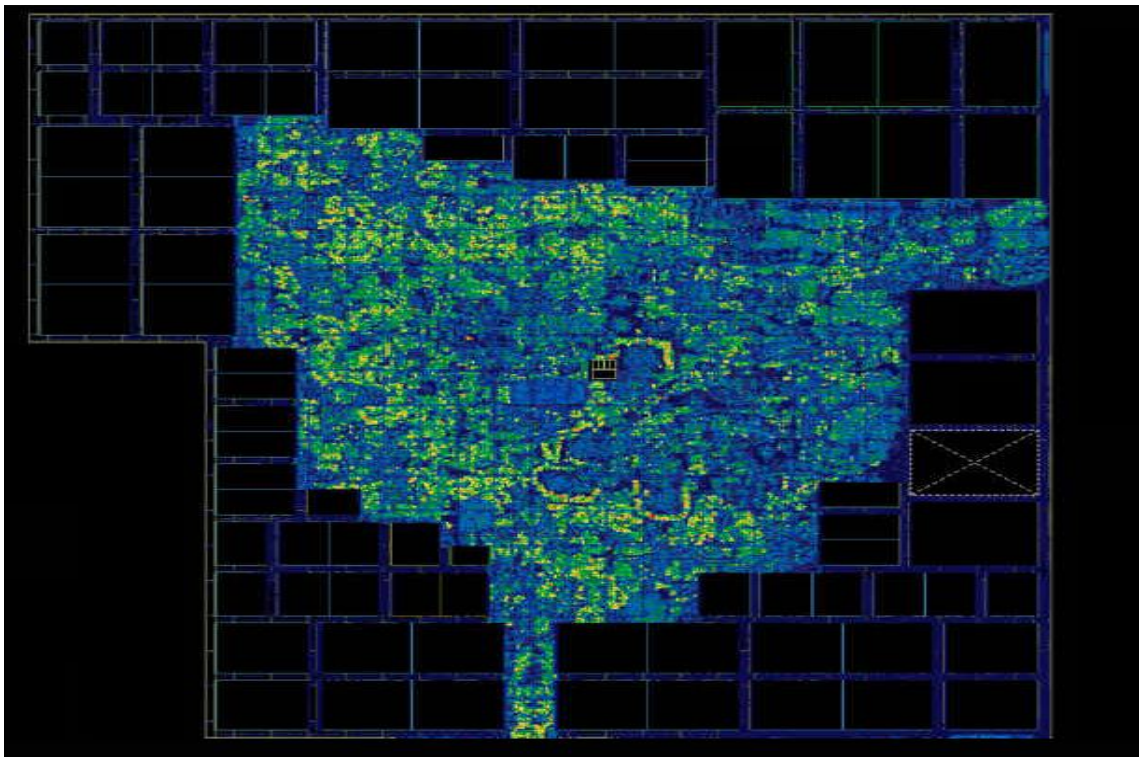

Figure 5.5 Module Placement for block.

5.2.1 Congestion Reduction experiment at Placement

Congestion is said to be high when the placement density of standard cells is high in a particular region. A very high degree of congestion may make the design un-routable and, hence, inhibit design convergence. Congestion issues create one of the most difficult.

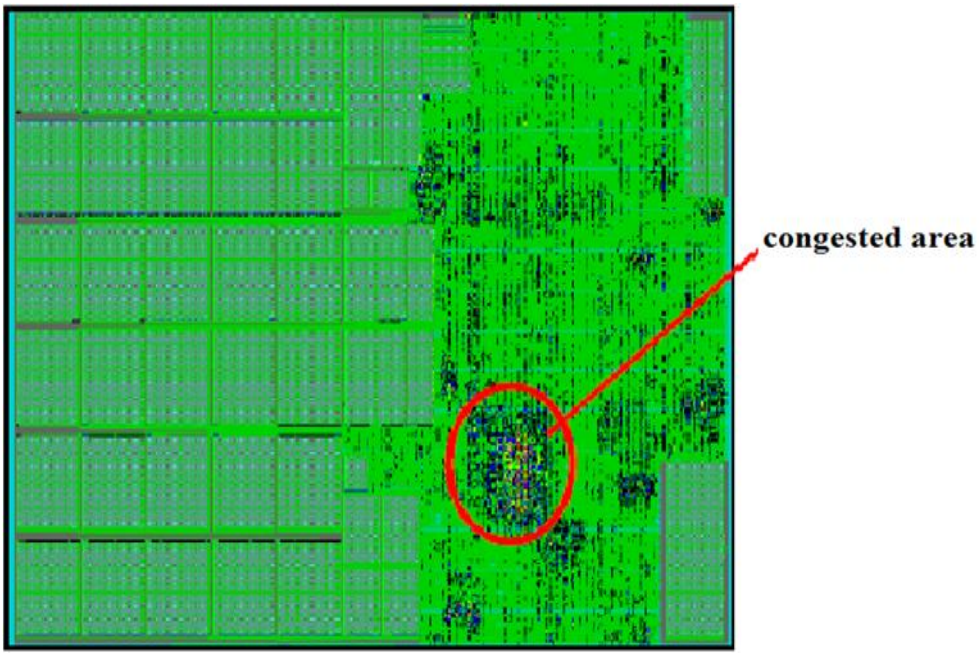

Figure 5.6 congestion showing for block.

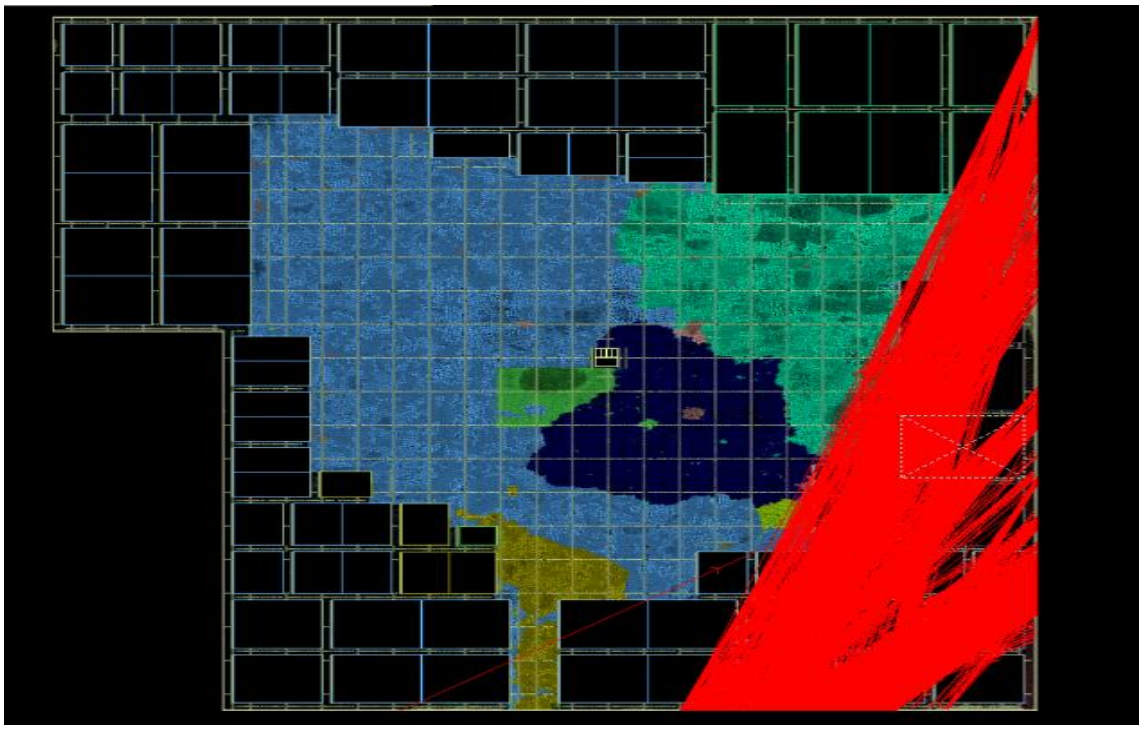

Figure 5.7 feed Pin congestion of the module.

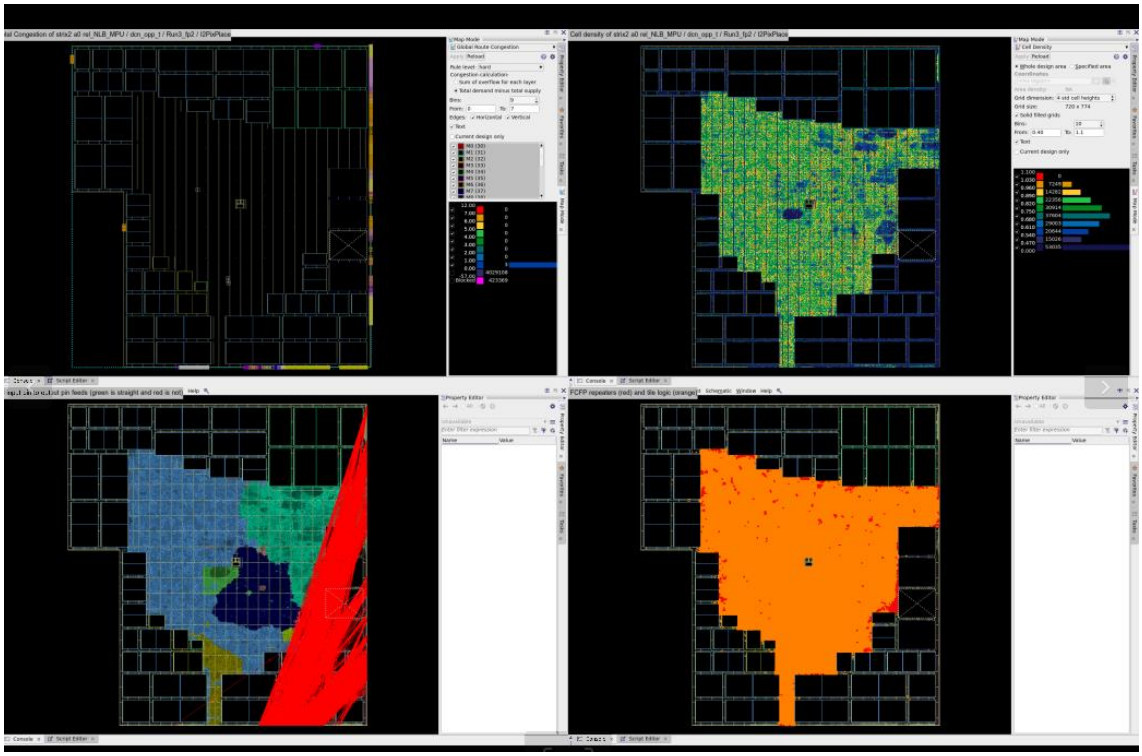

Figure 5.8 Congestion, placement density Module placement and feed placements.

Step1: To avoid the congestion at macro channel and block boundaries blockage is added before placement of the standard cells. With that the blocked place is not used for the cell's placement. There the congestion is controlled. During placement the cells are placed with non-uniform density i.e., Placement density is different at different locations. The placement density high region creates the congestion. To make the placement density uniform we have to enable the tool which takes the control of placement density to given value.

Step2: By applying cell padding to high pin density cells. Generally, AOI & OAI cells will have more pins and may need more routing resource

Command used

set_keepout_margin -type hard -outer {0.27 0.0 0.27 0.0} \ [get_cells "*" -hier -filter "ref_name =~ *AOI*"]

Step3: By applying density screens at the highly congested areas. An IC Compiler command is used to set the utilization to a fixed value for the specified region.

Command Used

set_congestion_options max_util 0.5 coordinate {-284.67 -281.664 -59.85 -117.504}

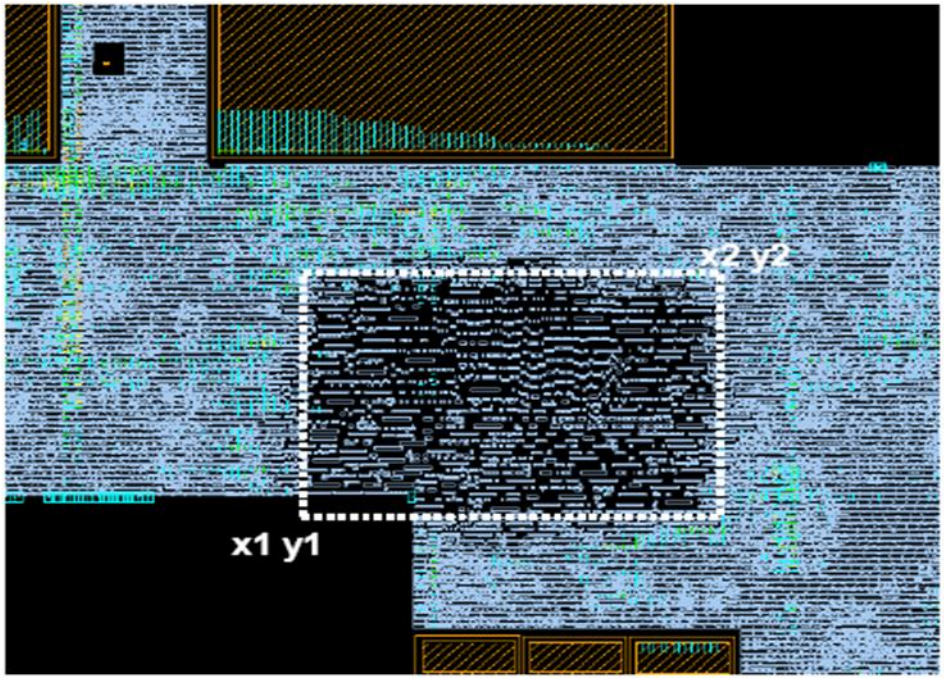

Figure 5.9 Coordinate to represent of some area.

Result of the Experiment: Congestion is reduced from 1.63% to 0.75%

Note: The experiment for congestion has a negative impact on timing.

5.2.2 Path Grouping and Bounding

Path grouping is a slack reduction experiment where, all the violating paths are given highest priority. So, after applying path grouping critical paths are routed first.

group_path -name crit_start_points -from [get_cells $startpoints] -weight 10.0 -critical_range 100.0

group_path -name crit_end_points -to [get_cells $endpoints] -weight 10.0 -critical_range 100.0

Parameter	Without Path Grouping	With Path Grouping at Place	With Path Grouping at Route
WNS (ns)	-208	-0.155	-0.155
TNS (ns)	-193.7	-105	-55
NV	2055	1050	997

Table 5.1 Path grouping of experiment result.

Bound:

create_bounds -name DBUS_repeater_bound1 -coordinate {1413.367 430.253 1462.401 481.031} -type soft $.....p1_cells

5.2.3 Area Optimization Experiment

This experiment is done to reduce the area occupied by the standard cells. In this experiment, the cells which are in the non-critical path are downsized (drive strength is decreased) to decrease the area of the cells. This is also called standard cell utilization area reduction. The width of the cell with drive strength 8ur is 1.5 units as shown below figure. When it is downsized to 4ur its size is reduced to 1unit. Like this all the cells are down sized to reduce the standard cell utilization Area. As the drive strength increases the transition delay of the cell increases. With this the timing violations will be reported. These timing violation slack can be recovered easily by upsizing the cells which are violating the time.

Figure 5.10 standard cell before and after downsizing.

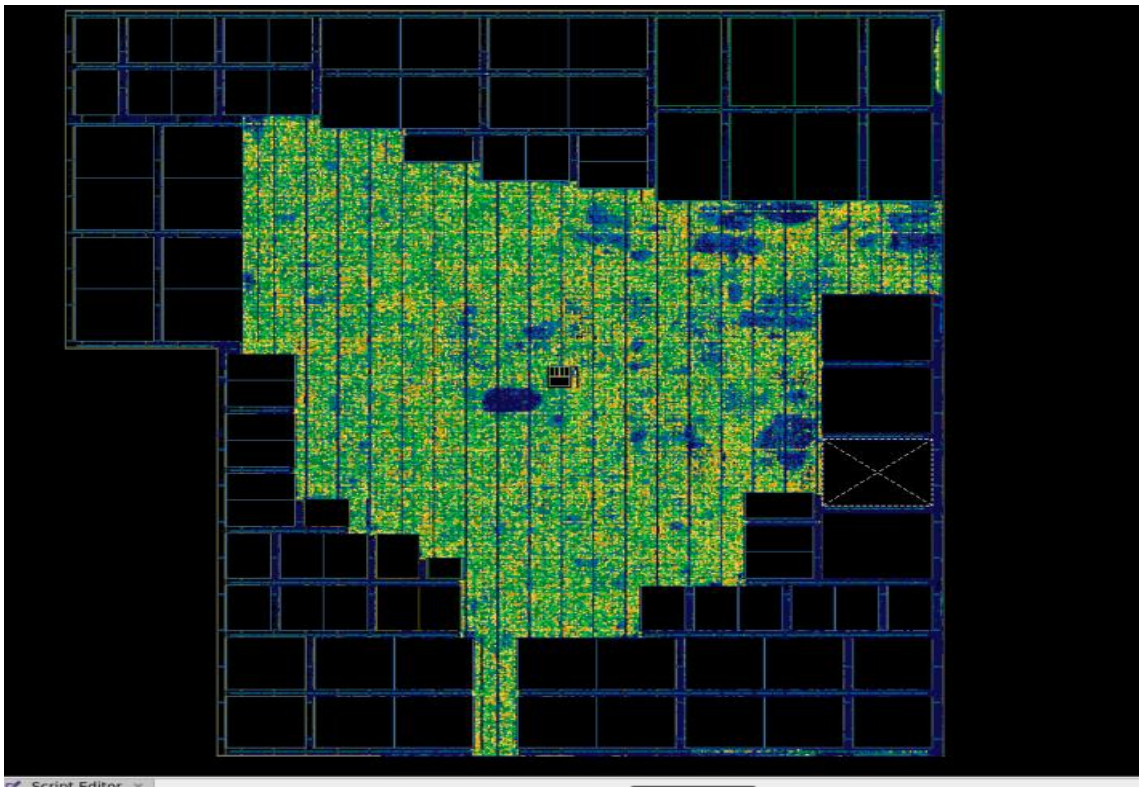

Figure 5.11 Standard Cell utilization view.

	Floorplan Stage	Route Stage
Total tile area(µm2)	355651.1040	355651.1040
Total cell area(µm2)	258679.4939	291833.7435
Standard cell area(µm2)	89194.6364	120738.7245
Logic cell area(µm2)	89194.6364	105450.0057
Standard cell utilization	48.42%	67.22%
Logic cell utilization	48.42%	61.44%
Design utilization	72.73%	81.60%

Table 5.2 shows the number of cells and utilization in the floorplan and route stage.

Result

The standard cell utilization area before the experiment is 48.42%

The standard cell utilization area after the experiment is 67.22%

So, utilization ratio is 0.6068.

5.3 Clock Tree Synthesis

Figure 5.12 shows the location of clock root buffers. Since the block has multi-point CTS there will be multiple roots. These multiple roots are arranged in mesh type structure. It is observed that all the roots lie on the same grid line.

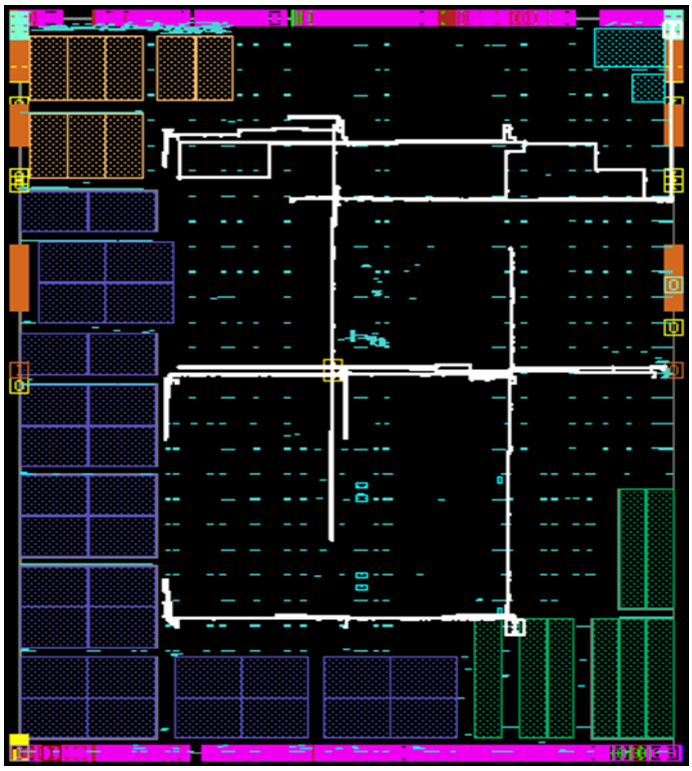

Figure 5.12 Clock Tree Synthesis for Experiment.

5.3.1 Insertion delay reduction experiment

This Experiment is performed after CTS. After CTS if the Insertion delay is more than the required value, it must be reduced in order to avoid timing violations. There are many techniques to reduce clock insertion delay.

Methods to Reduce Insertion delay are

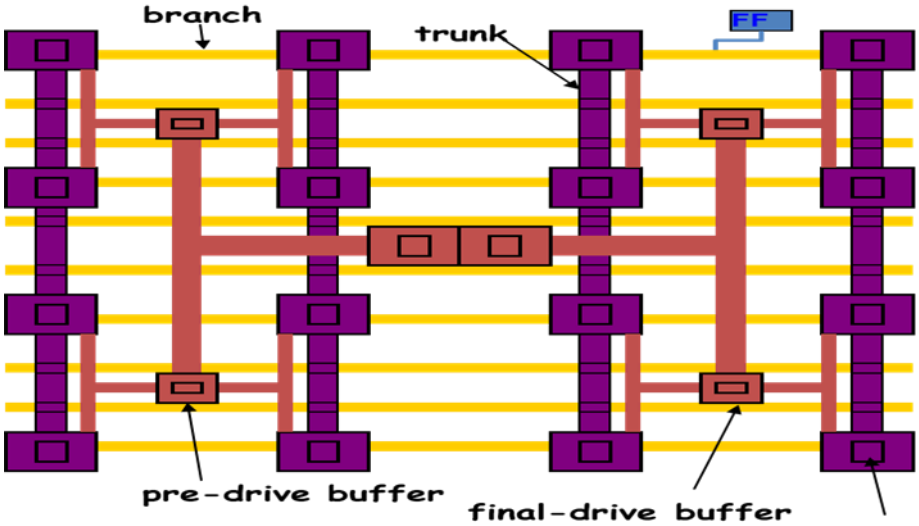

Figure 5.13 Clock Tree synthesis with insertion of the buffer.

Clock	Clock Skew(ps)	Insertion Delay(ps)
Clk1	65	308
Clk2	60	350
Clk3	45	340

Table 5.3 It show Clock skew and insertion delay of clocks of design.

• Placing the far sitting clock gaters near to the root.

• By increasing the skew limit.

• Changing clock gating cells to better drive strength before cts.

• Create bound for the 1st & 2nd level clock gaters.

• Moving PDLY Cell to center of the tile.

• Improving input transition by adding a big root buffer.

• Sink/buffer tran relaxing to 10% of clock period.

In this technique the clock buffers which are near to the main clock buffers are placed near to the main clock buffers to reduce the transition delay between those two buffers. The figure.5.14 shows the clock tree structure. clkbf represents the main clock buffer and ckbf1, ckbuf2, ckbf6 represents the inserted clock buffers to feed clock to all the cells in the design block. The secondary buffers are ckbf2, ckbf2, ckbf3 which are directly connected to main clock buffers are moved closer to the main clock buffer to reduce the insertion delay.

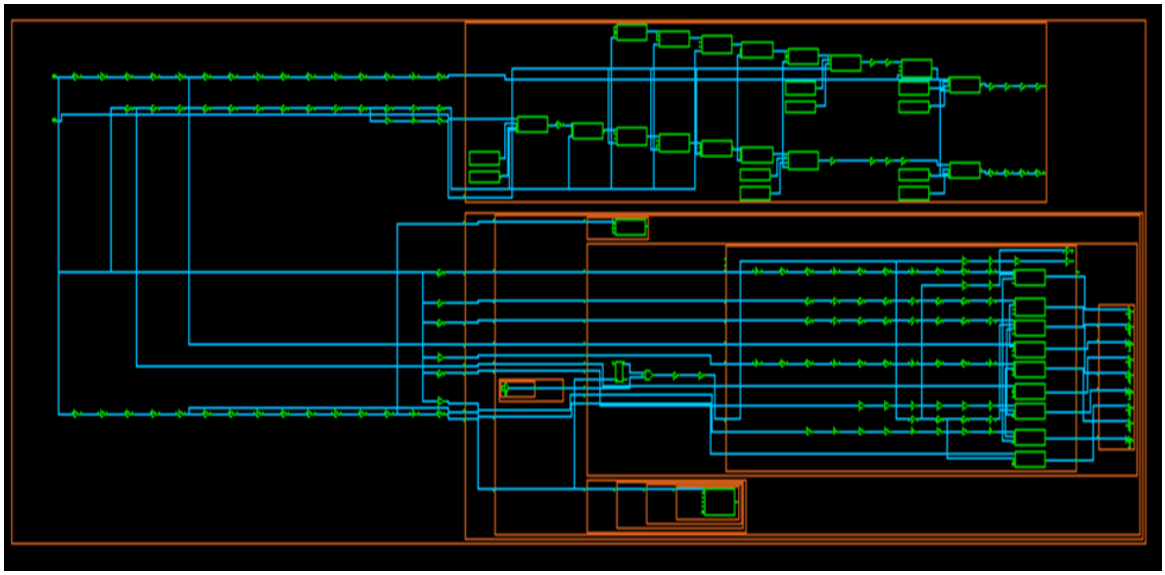

Figure 5.14 Clock Gating for Experiment.

Number of Clock gating elements	8865
Number of Tool-Inserted Clock gates	4 (0.05%)
Number of Pre-Existing Clock gates	8861 (99.95%)
Number of Gated registers	59765 (93.71%)
Number of Tool-Inserted Gated registers	2534 (3.97%)
Number of Tool-Inserted Gated registers	59764 (93.71%)
Total number of registers	63774

Table 5.4 shows the Clock gating Summary.

5.4 Routing

In routing some nets were not routed properly. Nets with long lengths are observed. Because of those violations got increased.

Long net buffering experiment

The aim of this experiment is to add buffers to the nets having lengths greater than 400um. As the length of the net increases the strength of the signal carried by those net decreases, to avoid this, the buffers are added while routing to regenerate the signal. Usually, the net length should not exceed 400um. If the net length is greater than 400um the buffers should be added.

Number of Max. Transition violation	1014
Number of Max. capacitance violation	1185
Number of Max. Fanout violation	o
Number of violations	15519
Total number of nets	1353561
Total number of open nets	4
Total number of excluded ports	0
Total number of DRCs	194
Total number of Antenna violation	1
Number of Shorts	33

Table 5.5 It shows DRV at the Route stage for a particular Mode and Corner.

The syntax to add buffer to the net in ICC tool is

add_buffer_on_route -no_legalize -first_distance 80 -repeater_distance 200 -cell_prefix _data_trans_fix_09_apr_ [get_nets -of_objects IcPlace_719/CLK] ……6ur

Depending up on the length of the net the buffer strength is taken.

The nets reported with lengths greater than 850um are 150.

5.5 Main Commands in ECO flow [ICC format]

Size_cell: Relinks leaf cells to a new library cell that has the required drive strength (or other properties).

Ex: size_cell dbus_REPEATER2_usblk_vceb/U26 ……...2ur

Insert_buffer: Inserts buffer cells on specified nets or nets connected to specified ports or pins.

Ex: insert_buffer e1/Z ……s4ur

Add_buffer_on_route: Adds buffers along the route of the specified nets.

Ex: add_buffer_on_route -no_legalize -first_distance 80 -repeater_distance 20cell_prefix _data_trans_fix_09_apr_ [get_nets -of_objects IcPlace_719/CLK] …..r

Set_cell_location /move_object: Specifies the physical location, orientation, and is fixed status for leaf cells

Ex: set_cell_location -coordinates {100 100} INST_1

Remove_buffer: Removes the buffer cells at a specified driver pin or net on a mapped design

Ex: remove_buffer cell2

Remove_net_routing: Removes all routing (vias and segments) for specific nets.

Ex: remove_net_routing {sig1 sig2}

5.6 QOR report

Once we have the design synthesized or placed/routed or clock tree synthesized, at every step, the one thing which you want to know quickly and accurately is the QOR of your design. This ICC and ICC2 command give an initial performance picture of your design. From a very high-level point of view, the below information should be good enough as the QOR of your design.

After Final Place and Route Stage

Clock Period	1.052ns
No. of Violating paths	21717
Worst Negative Slack	-21864.77
Total Negative Slack	-10924190.81

Table 5.6 Clock report of Setup after P&R stage.

Worst Negative Slack	-396.39
Total Negative Slack	-353494.43
No. of Violating paths	7213

Table 5.7 Clock report of hold after P&R stage.

After Engineering Change Order Stage

No of Violating paths	0
Worst Negative Slack	0
Total Negative Slack	0

Table 5.8 Clock report for setup and hold after ECO.

	Before experiment	**After experiment**	**Solution**
Setup violation	WNS=-45ps TNS=-5.7ns NV=397	WNS=0 TNS=0 NV=0	0paths Upsizing standard cells in data path/skewing in the clock path
Hold violation	WNS=-90ps TNS=-40ns NV=700	WNS=0 TNS=0 NV=0	0 paths Downsizing standard cells in data path /Adding Delay cell/skewing in the data path
Insertion delay	350ps	300ps	Pulling clock gaters towards root clock buffer
Double Switch	250	0	Clearing setup violations
Data Tran violations	400	0	Buffer insertion / Increasing driver strength
Glitches	90	0	Upsizing driver strength

Table 5.9 Results summary after doing all the experiments.

5.7 Vt Swap Experiment Results

Name of cells	Leakage(nw) in Typical Corner	Area(um2)	Delays(ps) in all corner
…. ss1ul	186.38	0.351	60
…. ss1ur	36.09	0.351	100
…. ss1urd	20.24	0.351	160
…. ss1uh	12.78	0.351	200
…. Ss1uhd	6.81	0.351	270

Table 5.10 It shows the Voltage Vt comparison.

Parameter	Total cells	Total leakage power saving (%)	Total area(µm2)
Total stdvt cells	438320	98.05	496154.18
-normal svt	437045	97.77	49484.69
-normal svt	1275	00.29	1305.49
Total hivt cells	8568	01.92	10521.11
-normal hvt	6608	01.48	6271.90
-wimpy hvt	1960	00.44	4249.21
Total lvt cells	141	00.03	1371.01
-normal lvt	141	00.03	1371.01
-wimpy lvt	0	00.00	0.00
Fill/DCAP cells	0	--	0.00
TIEH/TIEL cells	6313	--	1477.24
Other cells	9307	--	33108.31
Macros	10	--	38624.76
Total	462659	--	581256.60

Table 5.11 It show the power leakage percentage and area of higher technology result.

Parameter	Total cells	Total leakage power saving (%)	Total area(µm2)
Total stdvt cells	516199	62.55	231008.81
-normal svt	466103	56.05	216320.05
-normal svt	53529	08.40	15588.76
Total hivt cells	309042	37.54	76302.26
-normal hvt	30541	05.70	9196.94
-wimpy hvt	278541	33.75	67105.31
Total lvt cells	55	00.01	164.48
-normal lvt	55	00.01	164.48
-wimpy lvt	0	00.00	0.00
Fill/DCAP cells	908326`	--	145412.71

TIEH/TIEL cells	2780	--	374.70
Other cells	14879	--	14147.06
Macros	56	--	184724.84
Total	1751337	--	653034.86

Table 5.12 Vt Swap Initial Experiments report Power of lower technology.

Parameter	**Total cells**	**Total leakage power saving (%)**	**Total area(µm2)**
Total stdvt cells	244261	30.38	92940.67
-normal svt	101120	12.57	42789.25
-wimpy svt	143141	17.80	50151.42
Total hivt cells	559471	69.57	210593
-normal hvt	24717	03.97	8091.13
-wimpy hvt	534754	66.50	202502
Total lvt cells	417	00.05	400.04
-normal lvt	404	00.05	391.82
-wimpy lvt	13	00.00	8.22
Fill/DCAP cells	932484	--	149854.38
TIEH/TIEL cells	2781	--	374.83
Other cells	14879	--	14147.06
Macros	56	--	185724.84
Total	1754349	--	653034.84

Table 5.13 Vt Swap final Experiments report Power of lower technology.

Parameter	Before Experiment	After experiment
Leakage power/per. µm2	81mw	40mw
Dynamic Power/per. µm2	151mw	120mw
Total Power/per. µm2	232mw	160mw

Table 5.14 It show Power Result in design.

5.8 Summary

From the above tables it is clear that the increase in high Vt cell count will reduce the leakage power in the design. From Table 5,12 and 5.13 it is clear that leakage power per area(mm2) is reduced by 45% and area also reduced by 10 % also it seen in Table 5.14 the total power is reduce as technology are reduces.

CHAPTER 6

CONCLUSION & FUTURE SCOPE

Evaluation of different techniques for low power design for power-based designs to obtain minimal power consumption, desired timing closure and prototyping the appropriate method for design for power optimization flow. Implemented default place and route flow on power gated design block. Performed multiple trials on design blocks to optimize the design for lower power consumption and select the best method among them. Analysed the results obtained and prototyped the flow providing the best QoR.

Studied the default design for power implementation and adopted it in a suitable manner to further obtain better leakage power optimization. Participated in ECO implementation to obtain design closure for tape out. This could be nevertheless overcome to a certain extent by using power switches in different blocks at larger spacing than at very close intervals of distance. With this method, it was also seen that the power consumption of the design also came down to a certain extent.

Few of the timing critical paths in dense designs require use of LVT cells. Identify such paths earlier on in the design and do suitable floorplan changes or placement changes to make sure use of LVT cells are limited. This technique can be applied after completion of place and route flow to save area and instance count for better leakage optimization.

In future the flows can be further improvised by identifying all the non-critical timing paths and optimizing only those paths by swapping HVT cells. This helps in achieving design closure in a smaller number of iterations and with lower power numbers when compared to generic default flow methodologies.

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