POWER FACTOR CORRECTION OF VARIOUS CONVERTERS FOR EV CHARGING APPLICATIONS

DISSERTATION/THESIS

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Submitted by:

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DECLARATION

I, **Rishita Shukla**, Roll No. 2K20/PES/17 student of M.Tech (Power Electronics and Systems), hereby declare that the project Dissertation titled **"Power Factor Correction of DC-DC Converters for EV Charging Applications"** which is submitted by me to the Department of Electrical Engineering Department, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously submitted for the award of any Degree, Diploma.

The matter presented in this report has not been submitted by me for the award of any other degree of this or any other Institute/University. The work has been accepted and presented in peer reviewed Scopus indexed conference with the following details:

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SUPERVISOR'S CERTIFICATE

This is to certify that the work presented in this dissertation "**Power Factor Correction of Various Converter for EV Battery Charging Applications**" by Rishita Shukla, Roll No. 2K20/PES/17, is a record of original research carried out by her under my supervision and guidance in partial fulfilment of the requirements for the degree of Master of Technology (Power Electronics and Systems Engineering). Neither this dissertation nor any part of it has been submitted earlier for any degree or diploma to any institute or university in India or abroad.

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ABSTRACT

This work presents the modelling and design of two different EV Chargers. The proposed EV chargers consists of two-stage power conversion. Initially, DBR (Diode Bridge Rectifier) is connected for AC-DC Conversion which is followed by LC Filter to damp out the third order harmonics. The first stage consists of Power factor correction circuit using various DC-DC converters like boost, buck and buck-boost derived converter and the second stage consist of DC-DC stage for providing isolation of the grid and the charging port. Total research is done into two sections as mentioned below.

The first section consists of power factor correction using SI-SEPIC Converter cascaded with Flyback converter. It comprises of two stage EV Charger where initial stage consists of SI-SEPIC converter, which inherently provides the power factor correction of the EV charger at the source, and the later consists of Flyback converter. Collective combination of these two converters for the EV charger results for the operation of converter at reduced duty ratio resulting which efficiency of the converter is increased. This work mainly focuses on designing the components of the converter and power factor correction using PWM and SPWM controller techniques in MATLAB environment. The SEPIC Converter has a disadvantage of having more ripple in the output current so, modified Zeta converter is used which provides better dynamic response in DCM and it also provides less ripple in the output current.

The second section comprises of power factor correction using modified zeta converter cascaded with HB-LLC Resonant Converter. The Modified Zeta Converter operates in Discontinuous Conduction mode (DCM) and LLC Resonant Converter is used to transfer the DC-Link power to the battery. Collective combination of these two converters for the EV charger results in smooth operation, reduced voltage stress across the PFC devices and Modified efficiency of the converters. This work mainly focuses on designing the components of the converter and comparison of the Modified and Conventional Zeta Converter fed HB-LLC Resonant Converter in MATLAB/Simulink environment.

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NOMENCLATURE

PQ	Power Quality
THD	Total Harmonic Distortion
EV	Electric Vehicle
PFC	Power Factor Correction
DBR	Diode Bridge Rectifier
UPS	Uninterrupted Power Supply
PF	Power Factor
CC-CV	Constant Current-Constant Voltage
DCM	Discontinuous Conduction Mode
SI-SEPIC	Switched Inductor-Single Ended Primary Inductance Converter
PWM	Pulse Width Modulation
SPWM	Sinusoidal Pulse Width Modulation
HB-LLC	Half Bridge-Inductor-Inductor-Capacitance
EMI	Electromagnetic Interference
DPF	Displacement Power Factor
CF	Crest Factor
BEV	Battery Electric Vehicle
PFM	Pulse Frequency Modulation
SOC	State of Charge
HFT	High Frequency Transformer

CHAPTER 1

INTRODUCTION

1.1 Background of Project

In current scenario, electric vehicle is gaining more popularity as they do not produce hazardous carbon emission [1]. In addition, the price of fuel is increasing every day, which lead people to adopt Electric Vehicle. EVs have several advantages over conventional vehicles as fuel is reserved which causes the reduction in air pollution [2]. There are three levels of EV Charging which includes Level 1, Level 2 and Level 3 Charging respectively. The final Level of charging which is the Level 3 is further classified into Supercharging and DC Fast Charging. Each level is characterised by its speed of charging the electric vehicle which is different at each level. So, at higher charging levels speed of charging increases and the provided power is also increased [3].

Battery charger is an important component of the electric vehicle, which not only affects the life of the battery but it also affects the performance of all the electrical apparatus which are connected to the grid which may result a polluted electrical supply at the grid. For this reason, a reliable EV charger must be constructed which should operate at unity power factor and low input current distortion [4]. Line current should exactly follow line voltage, line power factor should be unity, and line current THD should be less than 5%, according to IEC 61000-3-2 which is shown in Table I and IEEE 519 standards. [5].

TABLE I. IEC 61000-3-2 MAXIMUM PERMISSIBLE HARMONIC CURRENTS FOR CLASS D EQUIPMENT [6]

n (harmonics order)	3	5	7	9	11	13	15 to 19
Max I_n (harmonics Current in Amp)	2.3	1.14	0.77	0.40	0.33	0.21	0.15 – 0.15/n

An off-board EV charger must have better Power Quality (PQ) characteristics in addition to a small form factor and high-power density, so that energy utilisation density is maximised during charging. However, the line THD (Total Harmonic Distortion) of traditional EV chargers is in the range of 50-70% having Full Bridge Rectifiers at the front end [7]. In this type of EV charging, highly distorted current is drawn from the AC mains. As a result, losses

in traditional EV chargers are quite high, and different Power Quality indices such as power factor (PF), displacement power factor (DPF), and total harmonic distortion (THD) are extremely low. Also, the requirement of reactive power rises significantly, low power factor results in depreciation for the availability of active power from the utility grid whereas a rise in harmonic content is the outcome. High harmonic distortion in the line produces EMI issues and cross-interferences across all the different components connected to the same grid via the line impedance. [8].

The conventional EV charger without power factor correction increases the content of harmonic into the supply current which results in poor input power quality (PQ) indices such as PF (Power Factor), DPF (displacement power factor) and CF (crest factor). The power factor value lies between 0 and 1 for lagging load, but to have significant PQ indices it should be near to unity i.e. 0.95-0.99 or 1. For lagging load, When the load power demand is reactive (for inductive load) the value of true PF is 0 as active power demand becomes zero.

Displacement Power Factor represents the power factor which occurs because of phase difference between input current and input voltage at fundamental line frequency. The value of true PF is considered with respect to harmonic current whereas DPF is taken into account at fundamental frequency. The value of PF and DPF is same for sinusoidal current having less distortion in its waveform and the value becomes unity. Therefore, to overcome the problem of PQ indices and to improve the converter efficiency, a front-end Power Factor Correction converter is designed to meet the requirements of EV charger for this reason, single stage and double stage EV charger comes into literature.

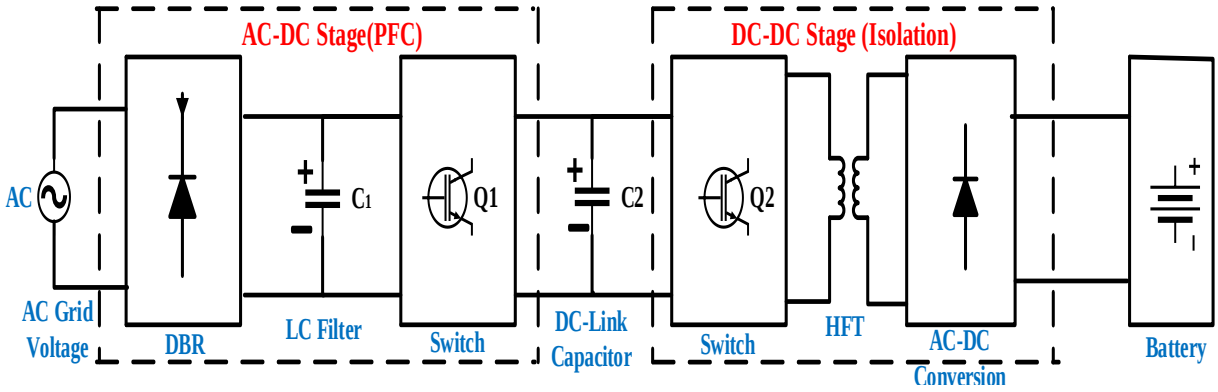


Fig.1.1 A General Structure of two-stage on-board EV Charger

The conventional Electric Vehicle charger consists of Diode Bridge Rectifier (DBR) for AC-DC conversion. Due to the presence of DBR, these chargers suffer from several Power Quality issues i.e. it draws non-sinusoidal and peaky current from the mains, resulting in a very

large amount of THD which badly affects the life of distributed transformer and various other elements, that are present in the charger [9]. Due to the bad effects of harmonics and large amount of THD present in the line, the addition of UPF (Unity Power Factor) based converter is required between the DBR and the DC-Link Capacitor. The charger added can be either a single-stage or double-stage EV charger based on the requirements.

As Diode Bridge Rectifier (DBR) is present at the input stage for AC-DC conversion, several problems are observed such as,

a. It draws peak input current from the mains
b. Produces high level of harmonics
c. Poor Input power factor
d. High THD
e. Increase in harmonic content into the supply

To mitigate these problems, PFC is essential for every AC-DC Converter. A General structure for PFC in an onboard EV Charger is shown in Fig 1.1 where for PFC different converters are used such as boost converter, buck converter, buck-boost converter, SEPIC converter, Cuk converter, Zeta converter etc. PFC is necessary to reduce the harmonics, improve the THD and power factor of the converter, effective utilization of active power which makes the grid more stable [10]

1.2 Importance of Power Factor

Nowadays, due to the modernization and electrification in the industries, the power quality requirements have been increased drastically among people. All the electronic gadgets such as computers, mobile phones, laptops etc have basic requirement of power quality. If the power quality is bad, then these electronic devices will not work adequately. Power factor is one of the most significant factors for power quality which directly impacts the PQ (Power Quality) [11] and effective utilization of active power.

When the power factor is poor, it has various negative impacts on the grid such as waveform distortion, large phase distortion between current and voltage and increased losses on the line which in turn reduces the service time of the power devices. AC-DC conversion circuit is also known as rectifier circuit which is used to convert alternating current to direct current and these circuits are widely used in the industries nowadays in various stages of power conversion. One of the applications of rectifier circuit is UPS (Uninterrupted Power Supply) [12]. Rectifier circuit acts as an interface between grid and power electronics devices, by

providing regulated DC power supply, it supplies good quality power for power electronics devices in the subsequent stages for power conversion.

Switching devices are widely used in different power conversion devices due to the large application of power electronic devices into the power industry. Because of the presence of switching devices, the device efficiency can be improved effectively but several problems like harmonics and low power factor are subsequently introduced which are considered as PQ issues. To mitigate such PQ issues i.e. elimination of harmonics and improvement in the power factor, power factor correction is being utilised effectively [13].

1.3 Disadvantage due to the presence of harmonic current in the grid

Due to the presence of harmonic component of current phase shift between current and voltage increases, thus power factor becomes poor. The impulse shaped waveform of input current contains a numerous number of odd ordered harmonic components of current which pollutes the grid [14]. Harmonics in the electric power system are present because of the presence of non-linear electric loads such as rectifiers. The current will be produced at different frequency levels rather from its original, i.e. fundamental frequency. Following are the disadvantages due to the presence of harmonic current component into the power grid:

1. When the harmonic current passes through the load, the phase difference between voltage and current is increased resulting which it distorts the effective voltage of the power grid, causing overvoltage and overcurrent into the grid. This is also known as “secondary effect” of the harmonic current.
2. Due to the presence of harmonic current components, losses will be more in the circuit and thereby decreasing the efficiency of equipment.
3. Abnormal operation of Power devices such as capacitors, transformers and electric motors, relay protection, automatic devices and computer system will be observed due to the presence of harmonic current component.
4. Improper calibration and measurement of quantities from the measuring instruments will be observed.

1.4 Power Factor Correction of two stage EV Charger

To overcome above disadvantages and to minimize the presence of harmonic components, also to improve the PQ indices present on AC mains, an additional Power Factor Correction stage is added in conventional EV charger. The addition of PFC stage improves the efficiency of charger on the cost of increase in the cost and size of the charger.

A single stage and double stage charger are used for the power factor correction. Generally, a double-staged AC-DC converter is chosen for improved Power Quality-based EV chargers as it offers the advantage for the low value of DC-Link capacitor, high reliability and reduced voltage stress across PFC device.

Single-stage PFC converter have high value of voltage stress and current stress across the PFC device, due to this reason it is generally not used [15]. A general configuration of two-stage EV charger is shown in Fig 1.2.

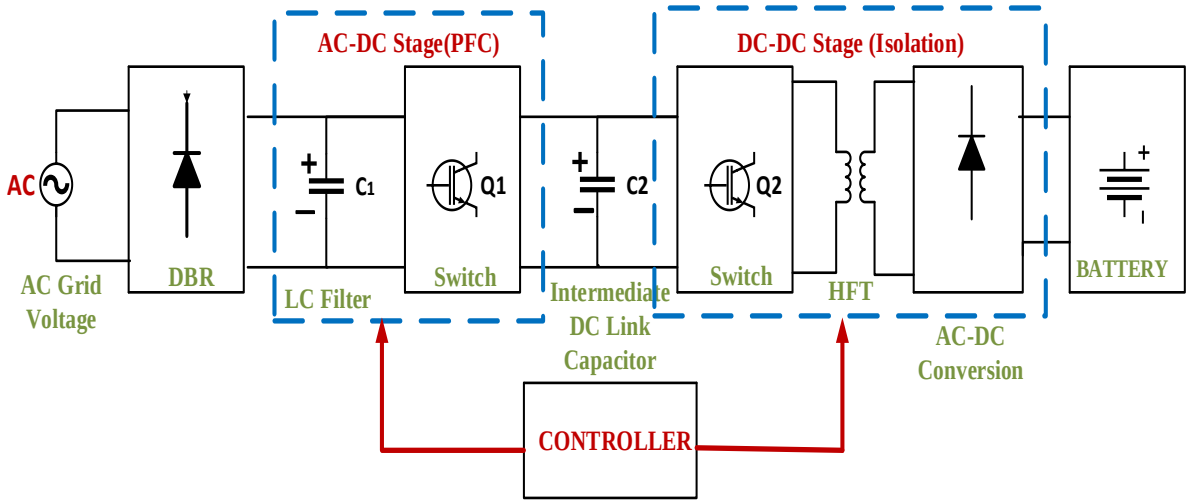


Fig. 1.2 *A General Structure of two-stage on-board EV Charger*

The high-performance BEV (Battery Electric Vehicle) charger circuit includes, DBR for AC-DC Conversion, but it injects a huge amount of harmonic current into the circuit which affects the efficiency and the performance of the charger. To mitigate the adverse effects of DBR, LC filter is connected which reduces the amount of third order harmonics in the charger. The LC Filter is followed by a Power Factor Correction (PFC) circuit at the front end.

The PFC circuit at the front end is used to obtain high power factor and reduce the harmonic current injected into the grid. Then it is cascaded with DC-DC converter with isolation from the main grid. It will provide higher efficiency, high power density and economical PFC based AC-DC Converter [16]. HFT (High Frequency Transformer) is used to provide isolation between the grid and the charging port.

Various DC-DC converters that are used for providing isolation are Flyback Converter, Forward Converter, Push-Pull Converter, Half-Bridge LLC Resonant Converter and Full-Bridge LLC Resonant Converter [17]. Then Battery is connected for charging the electric vehicle. Various ratings of battery can be connected for charging the EV, in this work 48 V and 100 Ah battery is used for charging the BEV.

1.5 Main Objective of Research

The main objective of this work includes:

1. ***Design and Modelling of the EV Charger*.** The EV Charger consists of two stages. First stage consists of DC-DC converter used for power factor correction and the later stage consist of DC-DC converter for providing isolation between main grid and charging port. Initially, we learn to compute various converter parameters and implement the model of EV charger.
2. ***Modes of Operation of EV Charger*.** In this work we will see the operation of converter in three different modes of operation with its applicability.
3. ***Control of EV Charger.*** After designing various components, we will learn about the control methods of EV charger with different controller techniques for controlling various parameters and increasing the efficiency of the chargers which will be discussed in the later chapters.
4. ***MATLAB-Simulink Implementation.*** With the help of design parameters that are calculated using the design equations and the control strategy of the EV Charger, the implementation of converter is done on MATLAB-Simulink environment and results obtained are discussed.

1.6 Outline of dissertation

The dissertation consists of the following chapters:

Chapter 1: In this chapter the importance of power factor correction for electric vehicle along with the problems arises due to the presence of DBR in the charger is discussed. Also, various methods are observed to mitigate the PQ issues present in the grid.

Chapter 2: This chapter includes the literature survey of the project "Power Factor Correction of DC-DC Converter for EV Battery Charging Applications". This chapter gives the basic understanding of various DC-DC Converters which are used for power factor correction along with their advantages and disadvantages.

Chapter 3: This chapter presents the first work which includes "Power Factor Correction of SI-SEPIC converter cascaded with Fly back Converter for EV Battery Charging Application". It includes the modelling and design of the proposed EV charger along with the control of EV charger using PWM and SPWM controller techniques.

Chapter 4: This chapter presents second work which includes "Power Factor Correction of Modified Zeta Converter Fed with Half Bridge-LLC Resonant Converter for EV

Charging Applications". In this chapter a comparison between conventional and modified Zeta converter is also discussed along with the design and modelling of Modified Zeta Converter and its control using dual loop controller technique.

Chapter 5: In this chapter, the MATLAB-Simulink Model of both the EV Chargers are presented and the results are discussed.

Chapter 6: This chapter summarizes the results obtained through the MATLAB-Simulink Model of the Proposed Converter and also acknowledge the future work that can be done.

CHAPTER 2

LITERATURE REVIEW

2.1 Introduction

In this chapter, various DC-DC Converters that are being used for providing PFC (Power Factor Correction) are reviewed along with a comparison table which shows the advantages and disadvantages of various DC-DC converter present in literature. Also, Research papers related to Power Factor Correction of DC-DC converter for Electric Vehicle charging applications are discussed.

2.2 Overview of Various DC-DC Converters

Various DC-DC converters can be used for PFC converters like buck converter, boost converter, buck-boost converter, Cuk converter, zeta converter etc and DC-DC converter for isolation stage like Flyback converter, Forward converter, Push-Pull converter, half and full bridge converter etc. Every converter has its own advantage and disadvantages like buck and boost converter have discontinuous input and output current respectively, high input voltage ripple and high electric stress across the device but it requires lesser number of components so the cost of converter is reduced [18]-[19]. In Buck-Boost configuration [20], output voltage is negative and input voltage ripple is more.

Another converter is Cuk converter [21], the output voltage is inverting but continuous and reduced current flows at input and output terminals. Some demerits of this topology include increased number of passive components, large size of inductors and higher electrical stress across the PFC device. In SEPIC converter [22], the polarity of output voltage is same as input voltage and the voltage stress is less as compared to Cuk converter, but the input inductor and output capacitor are large in size and also the output current is discontinuous. Among all these configurations, Zeta converter provides good voltage regulations, better dynamic response in DCM, positive output voltage and less ripple in output voltage [23].

The DC-DC converter for isolation stage includes Flyback converter which is used for isolated conversion. It is simple to design with lesser cost. In flyback converter [24], high voltage can be obtained at the output but voltage stress across the devices is high and has lower efficiency.

Another one is Forward converter [25], where one of the switches is replaced by a diode which causes the reduction in cost of the converter. Push-Pull converter is used in high power application but it has a demerit that its duty ratio cannot be exceeded more than 50% [26].

The demerits of conventional buck-boost PFC converters include [27]:

a) Increased size of magnetic components due to higher current and voltage ratings.
b) Increased voltage stress across switch during operations.
c) high parasitic losses due to operation of conventional converter at higher duty ratio.

To overcome these disadvantages high gain PFC converters are used. Table II shows various DC-DC converters with the relation between the output and input voltage along with advantages and disadvantages.

TABLE II. COMPARISION OF VARIOUS DC-DC CONVERTERS [28]

CONVERTER	OUTPUT	ADVANTAGE	DIS-ADVANTAGES
Buck	$Vo = Vs * D$	Lesser number of components	Discontinuous input current, high input voltage ripple, high stress across device.
Boost	$Vo = \frac{Vs}{1 - D}$	Lesser number of components	Discontinuous output current, high ripple in input voltage, high stress across device.
Buck-Boost	$Vo = \frac{Vs * D}{1 - D}$	Lesser number of components	High ripple in input voltage, high stress across device, negative output voltage
Cuk	$Vo = \frac{Vs * D}{1 - D}$	Continuous current present at input and output, reduction in input and output current.	Large number of passive components, large inductor size, high stress across device, inverting output voltage.

SEPIC	$Vo = \frac{Vs * D}{1 - D}$	Voltage stress is less than cuk converter	Large input inductor and large output capacitor, discontinuous output current.
Zeta	$Vo = \frac{Vs * D}{1 - D}$	Output current ripple is less	Large input inductor and large output capacitor, output current is discontinuous.
Luo	$Vo = \frac{Vs * D}{1 - D}$	Output current ripple is less	Large input inductor and large output capacitor, output current is discontinuous.
Flyback	$Vo = Vs \frac{D}{1 - D} (\frac{Ns}{Np})$	Simple and inexpensive, high voltage can be obtained easily.	High voltage stress and lower efficiency
Forward	$Vo = VsD(\frac{Ns}{Np})$	Cost is less	
Push-Pull	$Vo = 2VsD(\frac{Ns}{Np})$	Used in high power application	Duty ratio cannot be more than 50%
Half-Bridge	$Vo = VsD(\frac{Ns}{Np})$	Fewer component, lower cost, simple control	High electric stress, discontinuous output current
Full-Bridge	$Vo = 2VsD(\frac{Ns}{Np})$	Lower electrical stress, high conversion ratio and power level.	More components are present, control is complex, higher cost.

* V_o = Output Voltage
* V_s = Input Voltage
* D = Duty Ratio
* N_s and N_p = Secondary and Primary turns ratio of high frequency transformer for providing isolation respectively

2.3 Overview of Power Factor Corrected DC-DC Converter in Literature

A survey of comparison of various topologies which are used for front-end PFC Converter are reported in [29]. All the EV Chargers are designed based on on-board and off-board charger configurations. Various on-board EV charger configurations with single-stage are discussed in [30]-[31]. But on-board EV Chargers have the disadvantage of heavy vehicle weight and charging at high power ratings is not possible, which makes off-board EV charger configurations to be more promising.

For providing built in PFC in EV Chargers, the conventional boost converter fed with DBR is the foremost choice but it has various disadvantage like, at high power ratings, boost converter involves some severe problems like degradation in efficiency, increased bridge losses, increased size of inductor [32]. For buck converter, discontinuous input current, high input voltage ripple, high electric stress across the device are present. So, buck and boost converters are not preferred for providing good power factor correction as the duty cycle is restricted and the quality of wave shaping becomes poor.

The buck-boost configuration provides the advantage of stepping up and stepping down the wide range of input voltage. For providing high efficiency and increased power density, the full bridge LLC (Inductor-Inductor-Capacitor) Resonant converter appears to be a good solution. But due to the presence of four driver circuit, the cost of the converter is increased and the complexity of the topology also increases. An LLC Resonant converter-based EV Charger also provides the additional advantage of low EMI (Electromagnetic Interference) noise along with improved efficiency and increased power density over wide range of input voltage. Hence, EV Chargers need some specific topology of converters for providing reliable charging applications [33].

All the buck-boost derived topologies such as Cuk, Zeta, SEPIC etc are more attractive solution for providing power factor correction due to the availability of wide range of duty cycle, with or without the presence of isolating transformer. SEPIC converter has the ability to improve thermal utilization of switches as the conduction losses are less. It also has less input current ripple and provides better efficiency at low level of input voltage. Also, the switch voltage stress is less in SEPIC converters. Zeta converter provides better dynamic response in discontinuous conduction mode (DCM) [34]. It also provides good voltage regulation, less ripple in output current and positive output voltage. Also, the voltage stress across the devices is quiet low in case of Zeta converter as compared to SEPIC converter.

In this research, a detailed discussion is done on power factor correction using SI (Switched Inductor)-SEPIC converter cascaded with flyback converter which works on lower duty ratio, provides better efficiency, reduces the THD, reduce the third order harmonics and reduces the voltage stress across the power factor correction devices. Also, power factor correction using Modified Zeta converter fed with HB-LLC (Half Bridge-Inductor Inductor Capacitor) Resonant Converter is discussed in detail, which improves the efficiency of EV charger, reduces the third order harmonics, reduces the Total Harmonic Distortion (THD), improves the power factor and reduces the voltage stress across the devices. Also, the modified Zeta converter is compared with the conventional Zeta converter and the obtained results are discussed in detail.

2.4 Active Power Factor Correction

For a linear circuit, $cos\varphi$ is used to express the power factor, where φ is the phase difference between the sinusoidal voltage and sinusoidal current. In rectifier circuit diode is non-linear, despite the fact that the input voltage is sinusoidal, the rectified current has a non-sinusoidal shape to it. So, finally it was found that power factor calculation is invalid for AC-DC converter.

The ratio of active power to perceived power is known as the power factor. So, its formula can be written as:

$$PF = \frac{P}{V * I} \qquad (2.1)$$

were, PF=Power Factor, P= Active Power

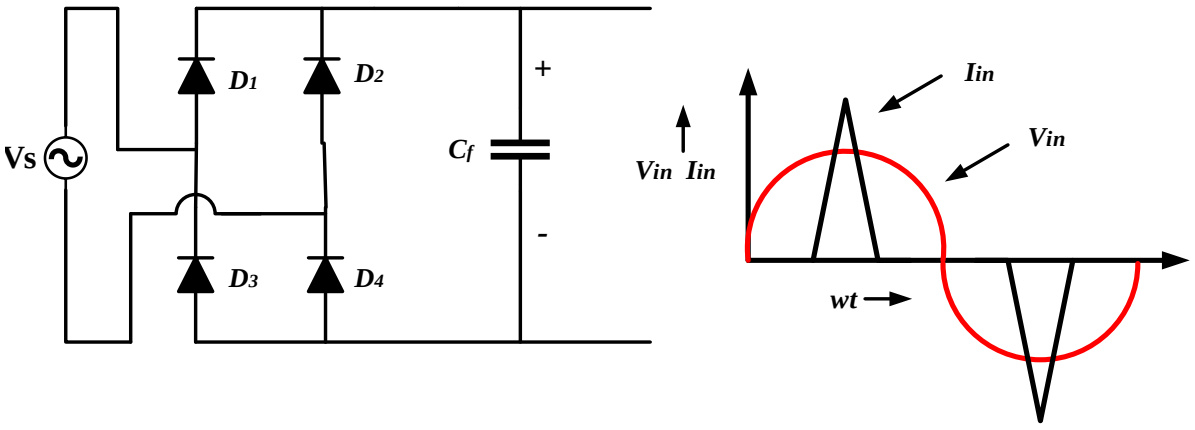


Fig 2.1 Rectifier Circuit for AC-DC Conversion and its Input Voltage and Current waveforms

The rms voltage and current are represented by V and I respectively in the above motioned equation. If the input voltage Vi (where the rms value is V) is sinusoidal but the input current is not, the rms of current is as follows:

$$I = \sqrt{I_1^2 + I_2^2 + \cdots + I_N^2 + ..} \qquad (2.2)$$

In this equation, I_1, I_2, ..., I_n are respectively the fundamental component, second harmonic, …, and N^{th} harmonic.

The power factor definition used in linear systems is no longer available in switching power systems due to the input current's severe distortion and phase change. We suppose that I_1 is behind V_i in terms of phase angle α, as indicated in the diagram below:

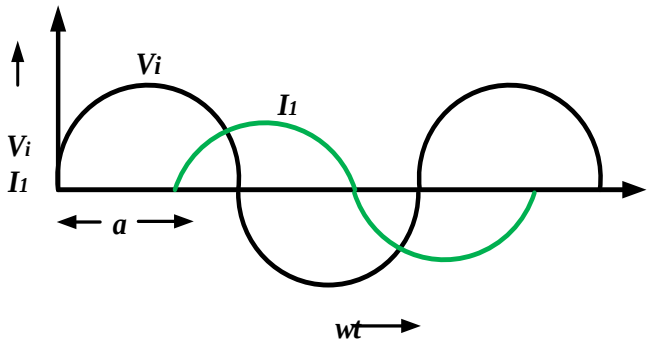


Fig 2.2 Waveforms of Input Voltage (V_i) and Fundamental Component of Current (I_1)

$$P = VI\cos\alpha \qquad (2.3)$$

where, the angle between input voltage V_i and fundamental component of current I_1 is the phase difference and is denoted by α. The power factor is calculated as,

$$PF = \frac{VI_1\cos\alpha}{VI} = \frac{I_1\cos\alpha}{I} \qquad (2.4)$$

The ratio of fundamental component of current to the rms current is calculated as,

$$\frac{I_1}{I} = \frac{I_1}{\sqrt{I_1^2 + I_2^2 + \cdots + I_N^2 + ..}} \qquad (2.5)$$

where, I_1, I_2, ..., I_n are rms value of the fundamental component, second harmonic, …, and N^{th} harmonic. The equation above describes the relative magnitude of the fundamental current, which is called distortion factor. And cosα is called displacement factor, and the power factor equals the distortion factor times the displacement factor.

When α=0, then power factor is given as:

$$PF = \frac{I_1}{I} \qquad (2.6)$$

Total harmonic distortion (THD) is defined as the measure of harmonic content in the signal [34]. The amplitude of harmonic content in a current signal is characterized as THD and is calculated as,

$$THD = \frac{I_h}{I_1} = \sqrt{\frac{(I_1^2 + I_2^2 + \cdots + I_N^2 + ..)}{I_1^2}} \qquad (2.7)$$

where, I_h is the rms value of all the harmonic component of current. THD considers all the fundamental frequency present on the line. It can be related to either current harmonic or voltage harmonics.

The equation of distortion factor is calculated as:

$$\frac{I_1}{I} = \frac{1}{\sqrt{1 + THD^2}} \qquad (2.8)$$

And when $\alpha = 0$,

$$PF = \frac{I_1}{I} = \frac{1}{\sqrt{1 + THD^2}} \qquad (2.9)$$

Equation 2.9 gives the relationship between the power factor (PF) and Total Harmonic Distortion (THD), it will help us to find the THD and PF of proposed DC-DC Converter. From the equation it is clear that THD and PF are inversely proportional to each other which means lower THD, results in improved power factor, which leads to lower peak currents and increasing the efficiency.

2.5 Conclusion

The literature review is done for the power factor correction stage in EV Charger is presented in this chapter in the relevant area for work presented in "Power Factor Correction of DC-DC Converter for EV Battery Charging Applications" in detail. The literature review is carried out to analyse all the different DC-DC converters topologies which are used for providing power factor correction along with their advantages and disadvantages. Among all the converters, SEPIC converter provides the advantage of less input current ripple and provide better efficiency at low level of input voltage. Also, the switch voltage stress is less in SEPIC converters. In discontinuous conduction mode (DCM), the ZETA converter provides a better dynamic response. It also improves the voltage regulation and lowers the ripple in output current. In the next chapters, design for the power factor correction using SEPIC and Zeta Converters are discussed.

CHAPTER 3

DESIGN AND SIMULATION OF SI-SEPIC CONVERTER CASCADED WITH FLYBACK CONVERTER

3.1 Introduction

In this chapter, Power Factor Correction of SI-SEPIC Converter cascaded with Flyback converter for EV Battery charging applications is presented. Initially, there will be a comparison between the traditional SEPIC converters and SI-SEPIC converters. Along with this the modeling and the three modes of operations of the proposed SI-SEPIC converter cascaded with Flyback converter will be discussed. The charger operates is Discontinuous Conduction Mode. Also, various parameters of the converter are calculated and the controller of the charger is designed using PWM and SPWM controller techniques.

3.2 Modeling of SI-SEPIC Converter cascaded with Flyback Converter

Due to the addition of an intermediate capacitor, the SEPIC converter does not have inrush current issues, and the regulated DC link voltage is not affected by the AC voltage peak, unlike boost converters. In discontinuous conduction mode (DCM), the control algorithm of the SEPIC converter and bridgeless SEPIC converter for inductor current is completed. Although it simplifies the PFC control technique, it has large input current peaks, which leads to overdesigned input filters. [35-36]. As a result, these converters can only be used for low-power applications. [37-38] investigates several variants of SEPIC converters and digital control of such converters; nevertheless, the component count is larger, resulting in increased cost and complexity.

The traditional SEPIC converter has step-up and step-down capabilities with positive voltage polarity [39]. A lower current ripple is obtained at the converter's input, as a high current ripple will distort the supply current, affecting the converter's performance. The sum of the input voltage and the DC-link voltage is the voltage across the device in the SEPIC converter [40]-[42]. Fig 3.1 represents the EV battery charger with conventional SEPIC converter. This configuration suffers from high voltage stress and less efficiency as compared

to high gain SEPIC converters [43]. To reduce the voltage stress across the device, the PFC converter is operated at lower input voltage with same DC-Link voltage and same power rating.

As a result, to reduce voltage stress across the devices, the standard SEPIC converter is substituted with a high step-up gain converter. We may be able to get the same DC-Link voltage with a lower input voltage due to the decreased duty cycle of these high step-up gain converters. [44]. Using a connected inductor is another technique to reduce voltage stress across the device. However, despite the inductor's simple design, voltage spikes develop across the devices when employing linked inductors.

A number of single stage single switch topologies based on integrated SEPIC with LLC converter, flyback converter, and valley fill circuit that are useful for EV chargers are discussed in the literature [45–46]. However, through the PFC device, all of these single-stage solutions are subjected to significant voltage and current stress. As a result, two-stage EV chargers are becoming increasingly common in order to ensure high dependability and low switch voltage stress on front-end PFC converter devices using high gain PFC converters.

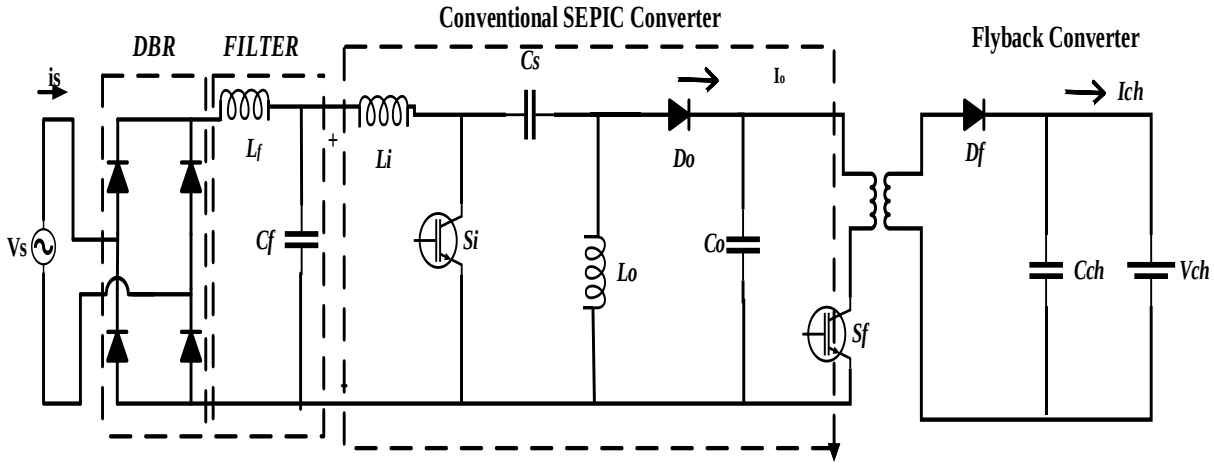


Fig 3.1 EV battery charger with conventional SEPIC Converter cascaded with Flyback converter

This work presents a two-stage EV charger with Switched Inductor (SI)-SEPIC converter cascaded with Flyback Converter for providing high-frequency isolation as shown in Fig 3.2, with reduced Duty Ratio (D) operation, providing lesser voltage stress across the switch. The converter consists of switched inductors L_m and L_a at stage-I along with two switches S_m and S_a with auxiliary components like C_a and D_{oa}, used to provide high gain to the converter. The main advantage of operating at reduced duty ratio is that efficiency of the

converter is improved as compared to conventional battery charger [47]-[48]; also, it provides the viability to increase the range of EV charger.

The advantages of the proposed converter over conventional SEPIC converter are:

1. The gain in voltage of SI-SEPIC converter is calculated as,

$$Gain = \frac{(3D + 1)}{(1 - D)}$$

where, D is the duty ratio of the proposed converter.

2. Reduced voltage stress across the PFC device.
3. Lower voltage stress leads to increase in voltage blocking capability of the switch, also reduces the on-state resistance.
4. High gain converter.
5. Efficiency of converter is improved.
6. Simple control topology.

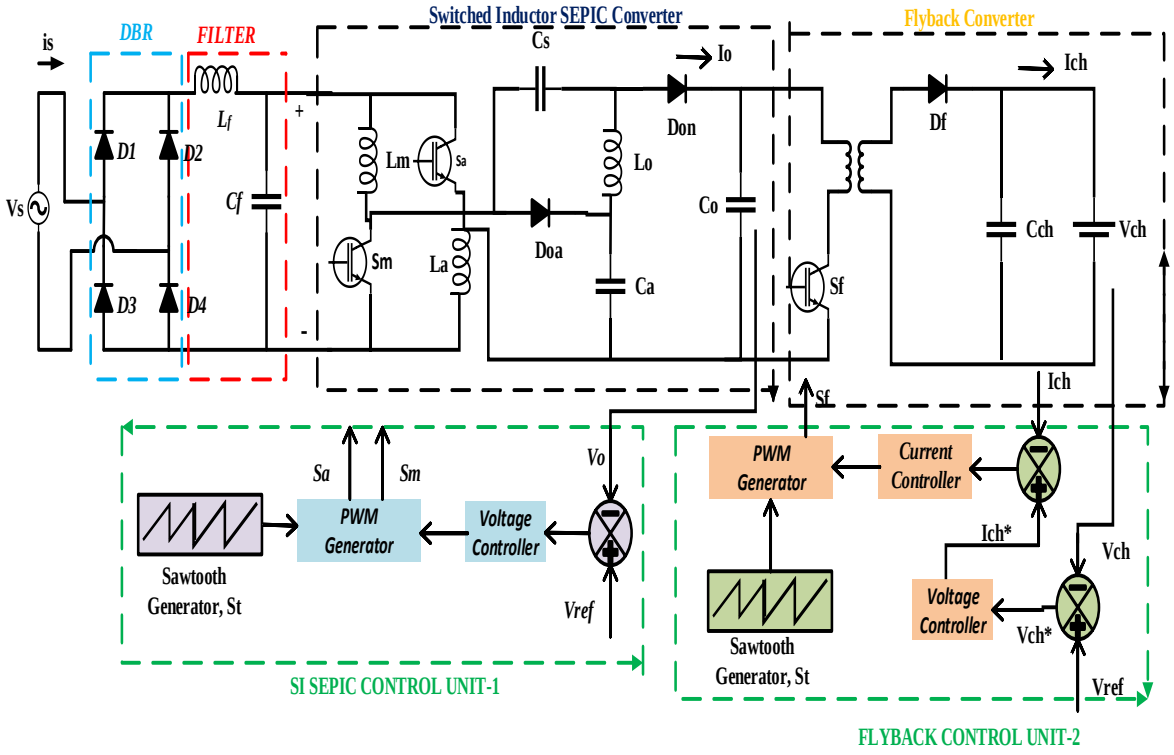


Fig 3.2 Proposed EV battery charger with SI-SEPIC Converter cascaded with flyback converter

Both the converters are designed to operate in Discontinuous Conduction Mode (DCM), to achieve zero voltage and zero current switching. A 220V AC is used at the source voltage then this AC voltage is converted to DC by connecting a DBR. A constant DC voltage

of 300V is achieved at the output of SI-SEPIC converter, this voltage is provided as the input of flyback converter and a voltage of 65V and 11A current is achieved across the battery at a power rating of 700W. The flyback converter is operated in CC-CV regions. The SI-SEPIC converter is operated using PWM and SPWM voltage control techniques individually; results of both of the controllers are compared. Simultaneously voltage stress across the devices is reduced and power factor is corrected.

3.3 Modes of Operations of Proposed SI-SEPIC Converter

The converter consists of switched inductors L_m and L_a at stage-I along with two switches S_m and S_a with auxiliary components like C_a and D_{oa}, used to provide high gain to the converter. The inductance L_o is designed for DCM operation. Different modes of this converter are explained below:

MODE 1*:* Both the switches S_m and S_a are turned on simultaneously, Fig 3.3(a). The current through the inductance L_m and L_a starts increasing linearly as in Fig 3.4. Both of the diodes i.e. D_{oa} and D_{on} remains reverse bias in this mode. Capacitors C_a and C_s starts to discharge in this mode through S_m and S_a.

In this topology we are considering L_m=L_a=L, using this expression we can calculate the expressions of voltage across switched inductors (V_{Lm}, V_{La}) and inductor voltage (V_{Lo}):

$$V_{Lm} = V_{La} = V_{sm} = L\frac{di_L}{dt} \qquad (3.1)$$

$$V_{Lo} = L_o\frac{di_{Lo}}{dt} = V_{ca}+V_{sm}-V_{cs} \qquad (3.2)$$

where, V_{sm} is the peak input voltage and i_L is current through inductor L_m and L_a.

MODE 2: Both the switches S_m and S_a are turned off simultaneously, Fig 3.3(b). The stored energy in inductor L_m and L_a is given to load via diode D_{on} and capacitor Cs. The auxiliary diode D_a is used to transfer the energy to the auxiliary capacitor C_a. The energy, which was present in L_O, is released through the diode D_{on}. The expressions of voltage across L_m, L_a and L_o is:

$$V_{Lm} = V_{La} = \frac{V_{sm} + V_{cs} - V_0}{2} = L\frac{di_L}{dt} \qquad (3.3)$$

$$V_o = L_o\frac{d_{iLo}}{dt} = -V_{cs} \qquad (3.4)$$

where, V_o is the output voltage of SI-SEPIC converter across the C_o DC-link capacitor.

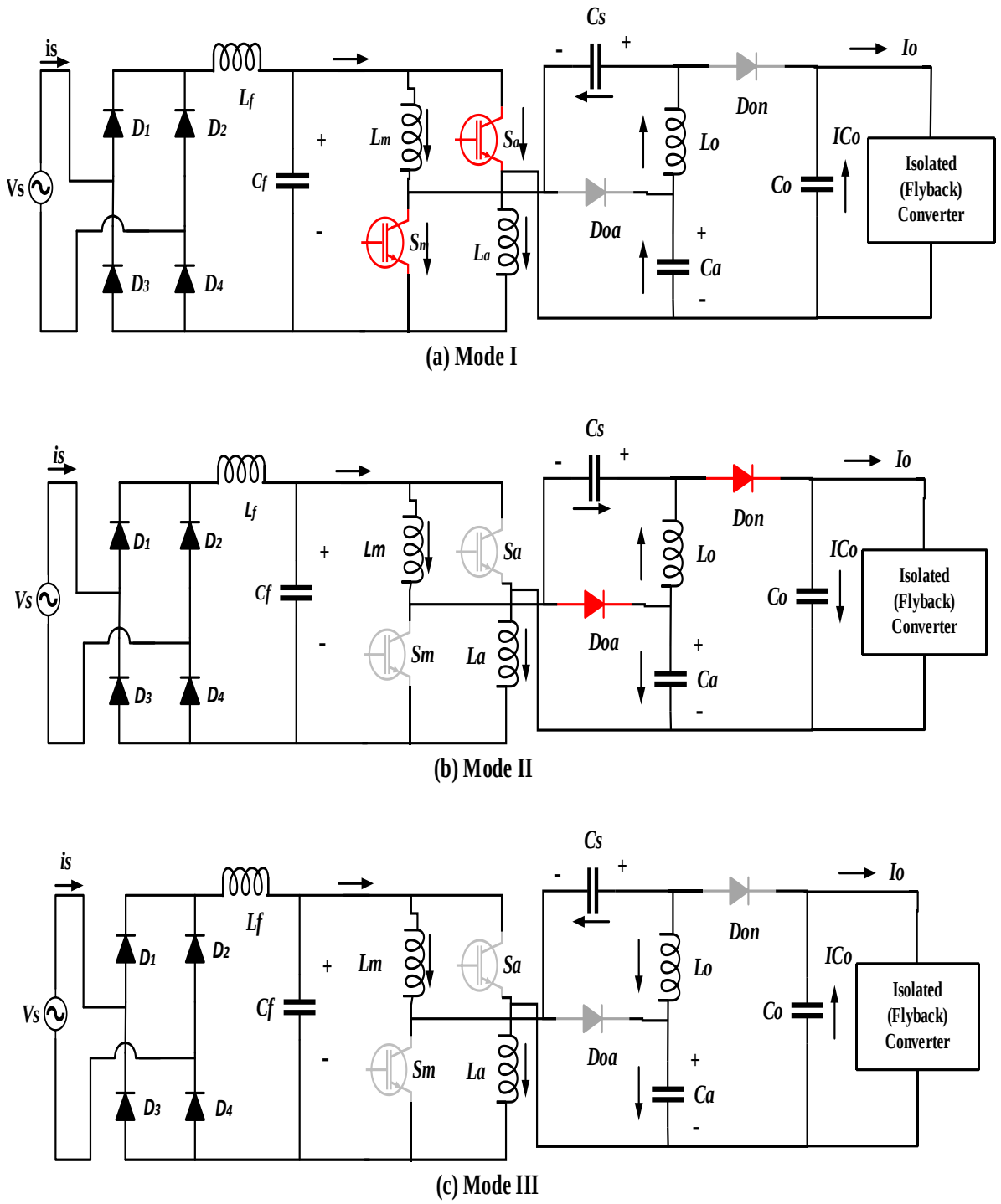


Fig 3.3 Modes of Operation of SI-SEPIC converter cascaded with Flyback converter.

(a) Mode-1, (b) Mode-2, (c) Mode-3

MODE 3: Both the diodes D_{on} and D_{oa} and the switches S_m and S_a remains turned off, thus this mode is called freewheeling period or DCM period, Fig 3.3(c). The current through the diodes D_{oa} and D_{on} is zero since both of them are non-conducting in this region, therefore

current i_{Lm}, i_{La} and i_{Lo} freewheels through the path shown. Using KVL in the closed path, the expressions of voltage is:

$$V_{Lm} + V_{La} + V_{ca} = V_{sm} + V_{cs} + V_{Lo} \quad (3.5)$$

Voltages V_{Lm}, V_{La} and V_{Lo} are considered zero during the steady state. Therefore, equation (3.5) becomes,

$$V_{ca} = V_{sm} + V_{cs} \quad (3.6)$$

The input and output voltage over one switching cycle is:

$$\frac{1}{T_s}\left(\int_0^{DT_s} V_{sm}dt + \int_{DT_s}^{T_s} \frac{V_{sm} - V_o + V_{cs}}{2} dt\right) = 0 \quad (3.7)$$

$$\frac{1}{T_s}\left(\int_0^{DT_s} (V_{sm} + V_{ca} - V_{cs})dt + \int_{DT_s}^{T_s} -V_{cs}dt\right) = 0 \quad (3.8)$$

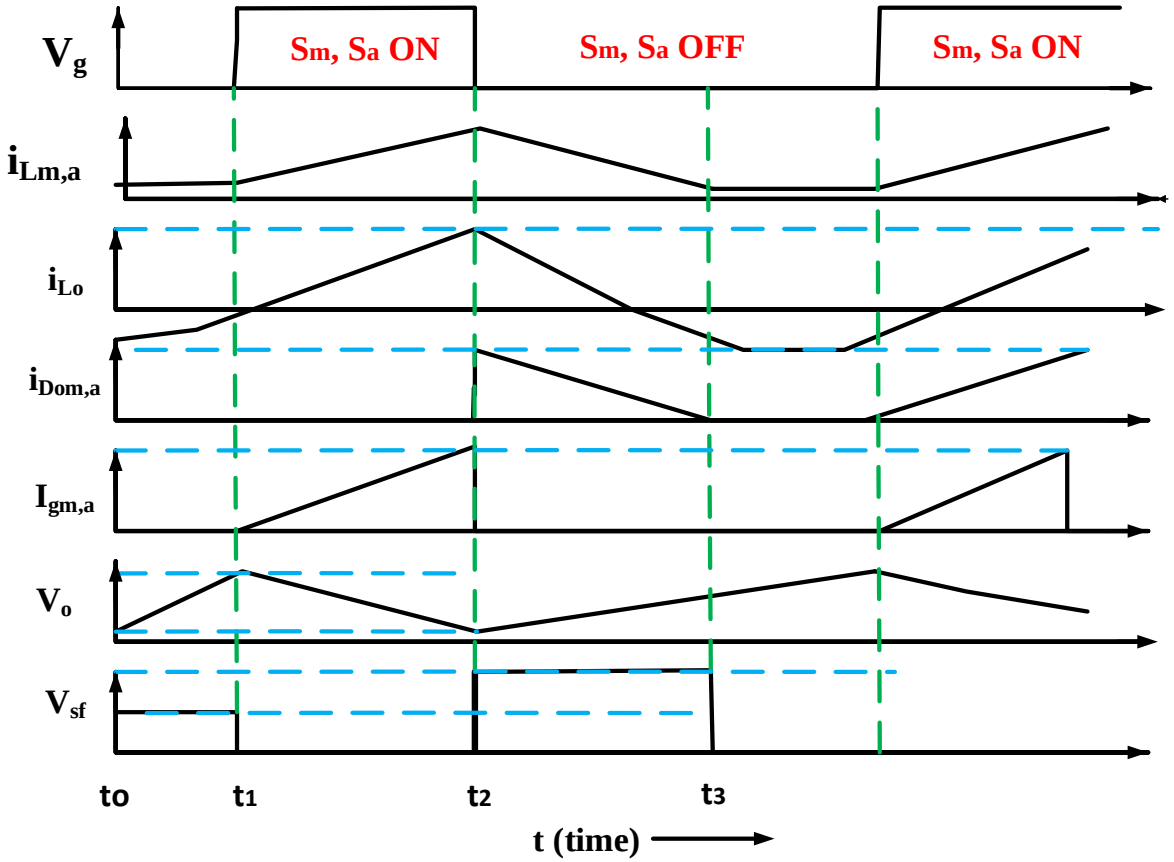


Fig 3.4 Switching waveforms of SI-SEPIC Converter cascaded with Flyback converter

The voltage across capacitors C_a and C_s can be calculated by using the equations (3.5), (3.6), (3.7) and (3.8)

$$V_{cs} = \frac{2D}{1-D} V_{sm} \quad (3.9)$$

$$V_{ca} = \frac{3D+1}{1-D} V_{sm} \quad (3.10)$$

Using above equations, the voltage gain across the SI-SEPIC converter is given as:

$$M_H = \frac{V_O}{V_{sm}} = \frac{3D+1}{1-D} \qquad (3.11)$$

From equation (3.11) shows that the voltage gain of the proposed SI-SEPIC converter is greater than the conventional SEPIC converter.

The flyback converter operates in constant current and constant voltage regions to facilitate the battery current. The magnetizing inductance is designed for DCM operation. The output current is provided to the battery by the capacitor C_{ch}. The operation of flyback converter can be explained as follows:

In Mode 1, the switch S_f is turned ON. During this mode the energy is stored in the inductance L_f, as the magnetizing current rises linearly. The diode D_f is in OFF state which means there is no transfer of energy between primary and secondary.

In Mode 2, S_f is turned OFF. The voltage across the primary reduces and positive voltage is applied to diode D_f, making it forward biased.

In Mode 3, both the switch and the diode are in OFF state and the converter operates in DCM. During this instant, the energy stored in L_m is completely reduced and the battery current is facilitated through the output capacitor C_{ch}.

3.4 Design Considerations of SI-SEPIC Converter

The instantaneous source voltage is,

$$V_s(t) = V_s\sqrt{2}\sin(2\pi ft) \qquad (3.12)$$

where, V_s is the source voltage which is taken to be 220V and f is the supply frequency. Using equation (3.11), the relation between DC Voltage V_o and peak input voltage V_{sm} can be given as,

$$V_o = \frac{3D+1}{1-D}\, V_{sm} \qquad (3.13)$$

The Duty Ratio of the proposed converter is,

$$D = \frac{V_o - V_{sm}}{V_o + 3V_{sm}} \qquad (3.14)$$

The above equation shows that the value of D (duty ratio) of this converter is less as compared to the conventional SEPIC converter

$$D = \frac{V_o - V_{sm}}{V_o + V_{sm}} \qquad (3.15)$$

which reduces the conduction losses of the converter and improves the efficiency.

The switching inductances L_m and L_a can be calculated using the equation,

$$L_m = L_a = \frac{V_{sm}D}{\sigma i L_m f_s} \quad (3.16)$$

where, σ is the permissible ripple in input current and f_s is the switching frequency SI-SEPIC converter.

The value of transfer capacitor C_s and auxiliary capacitor C_a are considered same and can be calculated from the equation given below,

$$C_s = C_a = \frac{P_i}{\rho\sqrt{2}V_{sm}fs\left(\sqrt{2}V_{sm} + V_o\right)} \quad (3.17)$$

where, P_i is the input Power and ρ is the permissible ripple in voltage. The inductance L_o in DCM can be expressed as,

$$L_o = \left(\frac{V_{sm}^2}{P_i}\right)\frac{1}{fs}\frac{V_o - V_{sm}}{V_o + 3V_{sm}} \quad (3.18)$$

The value of output capacitor C_o is designed in such a way that the battery current remains uniform at the output. The expression of C_o is,

$$C_o = \frac{I_o}{2\omega\Delta V_o} \quad (3.19)$$

where, Δ is the permissible voltage ripple in output and ω is angular frequency of supply voltage. The rating of the battery is taken to be 48V, 100 Ah and to provide CC-CV charging the output of the flyback converter is controlled at 65V. The transformation ratio of the Flyback converter is taken to be 1:3. The relation between V_o, Duty cycle C_o and V_{ch} can be given as,

$$V_{ch} = \frac{nD_o}{1 - D_o}V_o \quad (3.20)$$

where, V_{ch} is the output voltage of charger and V_o is the output voltage of SI-SEPIC converter, acts as the input of Flyback converter. The capacitor C_{ch} is used to provide rated output voltage in CC-CV mode and value of this capacitor is given as,

$$C_{ch} = \frac{D_o V_{ch}}{f_{sw}\left(\frac{V_{ch}^2}{P_i}\right)\Delta\varepsilon V_{ch}} \quad (3.21)$$

The magnetising inductance is given as,

$$L_{mg} \leq \frac{(V_o D_o)^2}{2V_{ch}I_{ch}f_{sw}} \quad (3.22)$$

LC filter is used after DBR to limit the reflection of high frequency harmonics and thereby reducing the THD of input current. The design equation of filter capacitance is,

$$C_{fmax} = \frac{I_m}{\omega V_m}\tan\theta \quad (3.23)$$

where, θ is the angle of displacement between the measured source current and fundamental component of supply voltage. f_c is defined as filter cut off frequency which chosen to be $1/10^{th}$ of switching frequency for eliminating higher order switching harmonics. The expression of filter inductance is given as,

$$L_f = \frac{1}{4\pi^2 f_c^2 C_f} \qquad (3.24)$$

Table III shows the parameters of the proposed converter used for the design of converter.

TABLE III. SPECIFICATIONS OF PROPOSED CONVERTER

S.No.	SPECIFICATIONS	VALUES
1.	Supply Voltage (V_s)	220V
2.	Output Voltage (SI-SEPIC)	300V
3.	Output Current (SI-SEPIC)	2A
4.	Switching Frequency (SI-SEPIC)	20kHz
5.	Output Power (SI-SEPIC)	600W
6.	Input Voltage (Flyback)	300V
7.	Output Voltage (Flyback)	65V
8.	Output Current (Flyback)	11A
9.	Switching Frequency (Flyback)	50kHz
10.	Battery Rating	48V, 100Ah
11.	Ripple Current in L_m (σ)	10%
12.	Ripple Voltage across C_s (ρ)	10%
13.	Ripple Voltage across C_o (Δ)	3%
14.	Ripple Voltage across C_{ch} (ε)	0.1%
15.	Input Inductance (L_m, L_a)	0.16mH
16.	Transfer Capacitance (C_s)	$5\mu F$
17.	Auxiliary Capacitance (C_a)	$5\mu F$
18	Output Inductance (L_o)	$3.57\mu H$
19.	Filter Capacitance (C_f)	$900\mu F$
20.	Filter Inductance (L_f)	1mH
21.	DC-Link Capacitance (C_o)	$250\mu F$
22.	Magnetic Inductance (L_{mg})	$240\mu H$
23.	Output Capacitance (C_{ch})	$1000\mu F$

3.5 CONTROL OF EV CHARGER

The control methodology of proposed EV charger can be explained in two stages:

(a) Control of SI-SEPIC converter

(b) Control of Flyback converter.

3.5.1 Control of SI-SEPIC converter

The multi-loop control is used for the control of SI-SEPIC converter. For the generation of reference source current and switching signals (G_s) the outer and inner PI controller is used respectively. Initially, Voltage error signal is generated on comparing V_{dc} with V_{dc_ref} as,

$$V_{oe}(k) = V_{dc_{ref}}(k) - V_{dc}(k) \qquad (3.25)$$

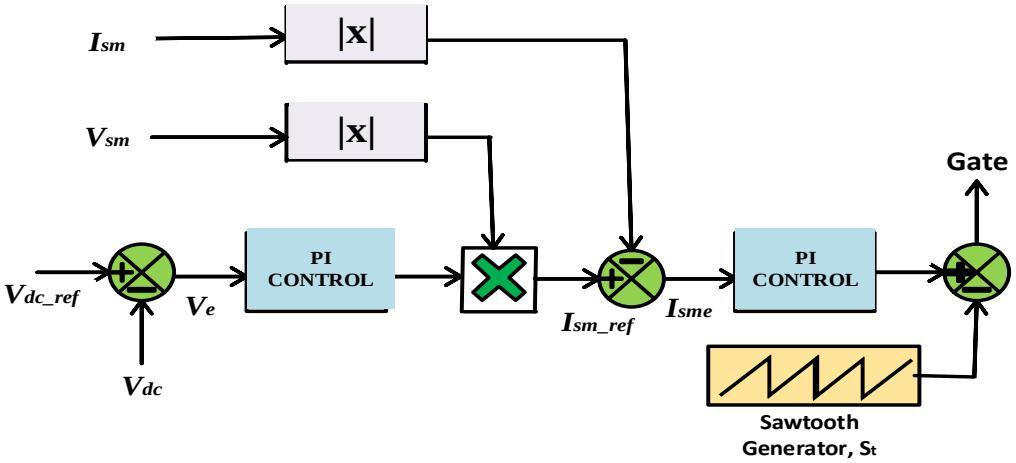


Fig 3.5 Controller design of SI-SEPIC converter

The outer voltage loop is used to control DC Link voltage of SI-SEPIC converter and the inner current loop control is used to control the output current of SI-SEPIC Converter. The DC-Link voltage (V_{dc}) is compared with the reference voltage (V_{dc_ref}) to generate error in voltage (V_e) and is provided to PI-Voltage Controller.

This voltage error signal is multiplied with the source voltage, V_{sm} to generate the reference source current. Both, reference source current and source current are then compared and the generated current error is given to PI controller. The PI Controller is used to control the current. The output of PI based current controller is compared with saw-tooth carrier waveform to generate the switching pulsed which are given to switches S_m, S_a of the SI-SEPIC Converter. Fig 3.5 represents the control methodology of SI-SEPIC converter by the help of dual loop controller technique.

3.5.2 Control of Flyback converter

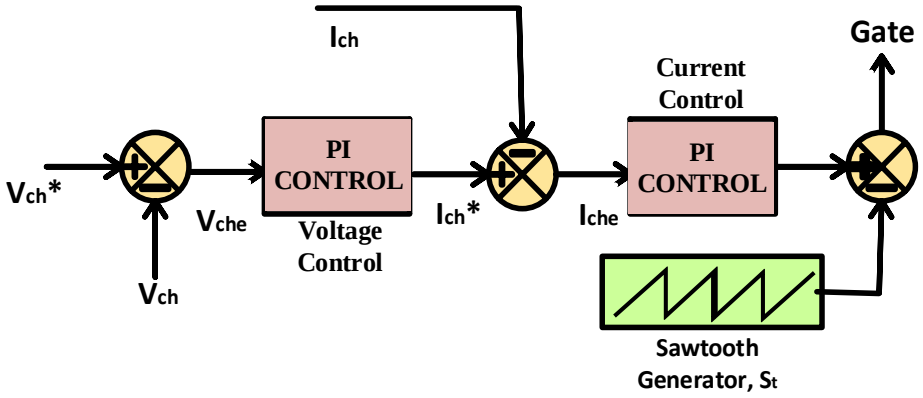


Fig 3.6 Controller design of flyback converter

The controller of flyback converter consists of cascaded PI controller. PI controlled current and voltage signals are utilised to provide CC-CV charging. During CC charging, the battery current I_{ch} and reference battery current I_{ch}^{*} are compared and an error signal I_{che} is generated,

$$I_{che}(k) = I_{ch}^{*}(k) - I_{ch}(k) \qquad (3.26)$$

During CV charging, the current PI controller remains inactive. The sensed battery voltage (V_{ch}) and reference battery voltage (V_{ch}^{*}) are compared and an error signal (V_{che}) is generated,

$$V_{che}(k) = V_{ch}^{*}(k) - V_{ch}(k) \qquad (3.27)$$

The output of PI controller is then obtained after processing through the voltage controller. Fig 3.6 represents the controller design of flyback converter.

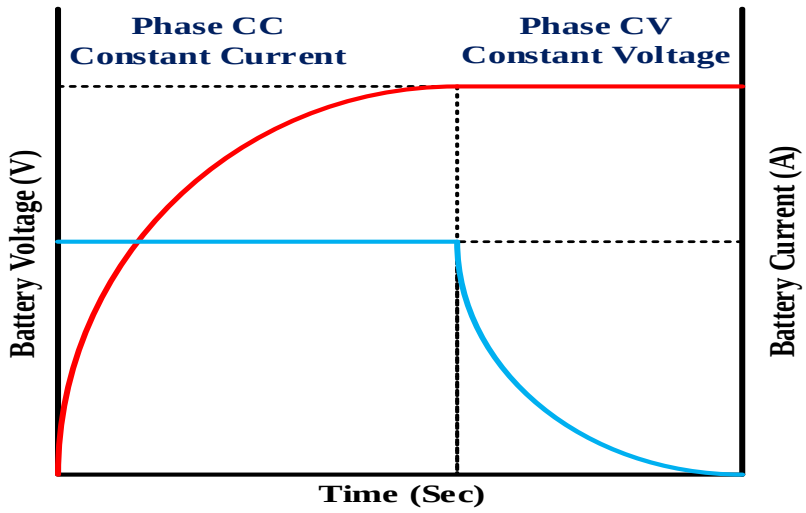


Fig 3.7 Battery Charger profile in CC-CV mode

Fig 3.7 shows battery charger profile in CC-CV mode in Flyback converter. It shows the conventional charging profile of a typical Li-ion battery employing the constant current (CC) and constant voltage (CV) with respect to charging time line. The charger switches to CV mode when the battery voltage reaches a pre-set level. This mechanism is normally applied to charge different kinds of batteries. For this converter, in constant current region, the battery voltage increases and the current remains constant i.e. 10.83 A. Similarly, in CV region, battery voltage remains constant i.e. 65 V and the current starts decreasing till it reaches zero.

3.6 Conclusion

In this chapter, the Power Factor Correction of SI-SEPIC Converter cascaded with Flyback converter for EV Battery charging applications is studied. Initially modelling and modes of operations were discussed. Also, the parameters of the converter are calculated and the controller of the charger is designed using PWM and SPWM controller techniques. The SEPIC Converter has a disadvantage of having more ripple in the output current, which will be seen in chapter 5. So, we will discuss about modified Zeta converter in the next chapter which provides better dynamic response in DCM and it also provides less ripple in the output current.

CHAPTER 4
DESIGN AND SIMULATION OF MODIFIED ZETA CONVERTER FED WITH LLC RESONANT CONVERTER

4.1 Introduction

In this chapter the power factor correction using modified zeta converter cascaded with HB-LLC Resonant converter is discussed. Initially, a comparison is made between conventional Zeta converter and modified Zeta converter and the advantages and applications of modified zeta converter are shown. Along with this, the modelling and the modes of operations of modified zeta converter cascaded with HB-LLC Resonant converter will be learnt. The design equations are calculated for proper operation of Zeta converter. The controller of the Modified Zeta converter is designed using dual loop controller and the controller of HB-LLC Resonant converter is designed using PFM (Pulse Frequency Modulator).

4.2 Modeling of Modified Zeta Converter cascaded with HB-LLC Resonant Converter

The dynamic response of Zeta converter is better than Cuk and SEPIC Converter in discontinuous Conduction Mode (DCM). It also provides good voltage regulation and low ripple in output current. All these advantages make the Zeta converter more appealing for providing improve power quality operation of BEV (Battery Electric Vehicle) based charger. But at higher power rating and in Discontinuous Conduction Mode, the stress in voltage across the device is quiet high in Zeta converter, which is equal to ($V_s = V_{in} + V_{dc}$, where V_{dc} is the DC-Link voltage of Zeta converter and V_{in} is the input side voltage of the converter). Several topologies come into literature for providing less voltage stress, one among them is by providing soft-switching techniques [49], but it adds more resonance components in the converter. Many switch voltage reduction techniques are present in literature using high gain converters [50]- [51]. All the mentioned high gain converters provide rated DC-Link voltage at duty ratio less than the conventional converter. With the help of such high gain converters voltage stress is lowered up to some extent but due to the presence of additional switches, diodes, capacitors and inductors, the power density of the converter is compromised [52].

Therefore, without using additional inductor and capacitor this work presents modified non- isolated Zeta converter fed with half bridge LLC Resonant converter with reduced voltage stress for improving the Power Quality indices of the EV charger. The modification in Zeta converter is achieved by providing some changes in the input side of the converter, which reduces voltage across the PFC devices at input side of the converter. By using this charger smaller devices are used at the power factor correction stage of the charger which reduces the losses across the device and provides improved efficiency as compared with charger based on Zeta converter in the literature.

The configuration of charger with Conventional and Modified Zeta converter is shown in Fig 4.1 and Fig 4.2 respectively. The Modified zeta converter is analogous to normal conventional zeta converter except for the addition of two clamping diodes (D_5, D_6) which are being added at the input and one switch S_2. By the help of clamping diodes, the voltage stress across the devices by clamping the voltage across the switches at input voltage V_{in}, which is half as compared with conventional Zeta Converter ($V_{in} + V_{dc}$). This reduces the losses across the device and improves converter efficiency. The value of DC-Link voltage is maintained at 300V by the help of input inductor (L_i), output inductor (L_o) and series capacitor (C_i).

The main application of this work includes:

1. A unique technique is adopted to increase the efficiency of the battery charger by operating near the resonance frequency.
2. This configuration is suitable for a wide range of battery voltage ranging from 48V-80V.
3. This battery charger has the ability to perform at universal AC mains supply (170V-300V).
4. The voltage stress at peak across devices in the modified zeta converter is less ($V_{s1} = V_{s2} = V_{in}$) in comparison with the conventional Zeta converter ($V_{s1,s2} = V_{in} + V_{dc}$) because of the use of clamping diodes (D_5, D_6).

This configuration is being used as it reduces the voltage stress due to the presence of two switches at the input voltage, which is $1/2$ $(half)$ as compared to Conventional converter. The DC link voltage is maintained at 300V. The modified non-isolated zeta converter is then followed by HB-LLC Resonant converter. Both Zeta and HB-LLC Resonant Converters operate in DCM, which reduces the diode reverse recovery time and provides zero current switching (ZCS).

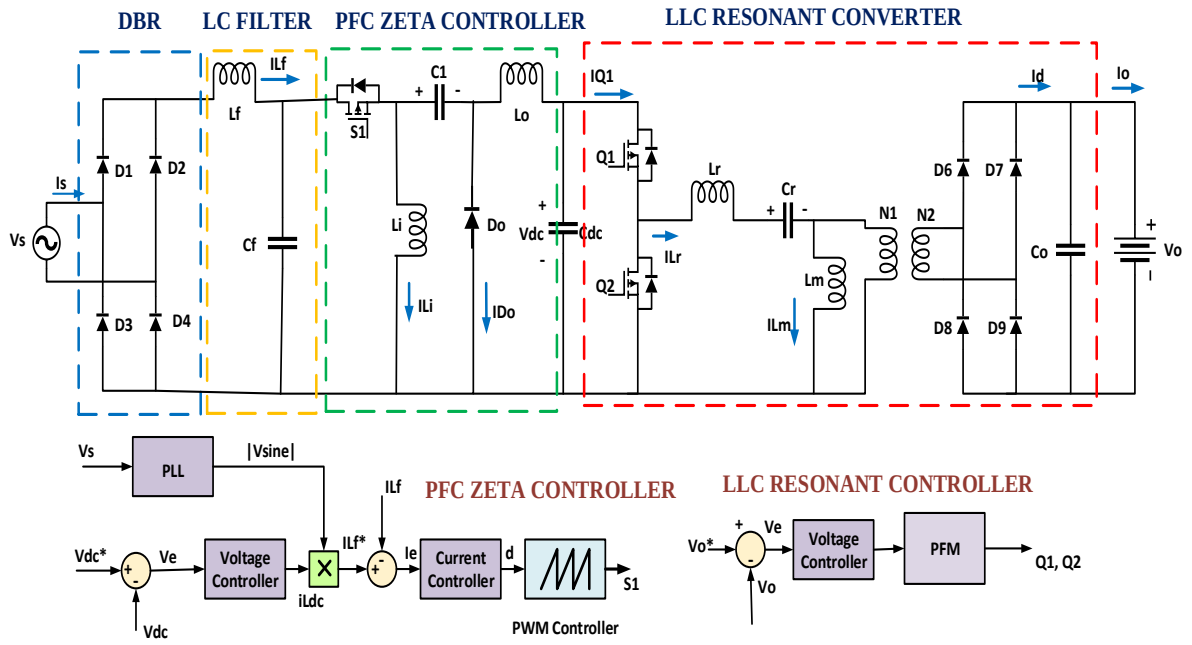


Fig. 4.1 Battery Charger with Conventional Zeta Converter fed LLC Resonant Converter

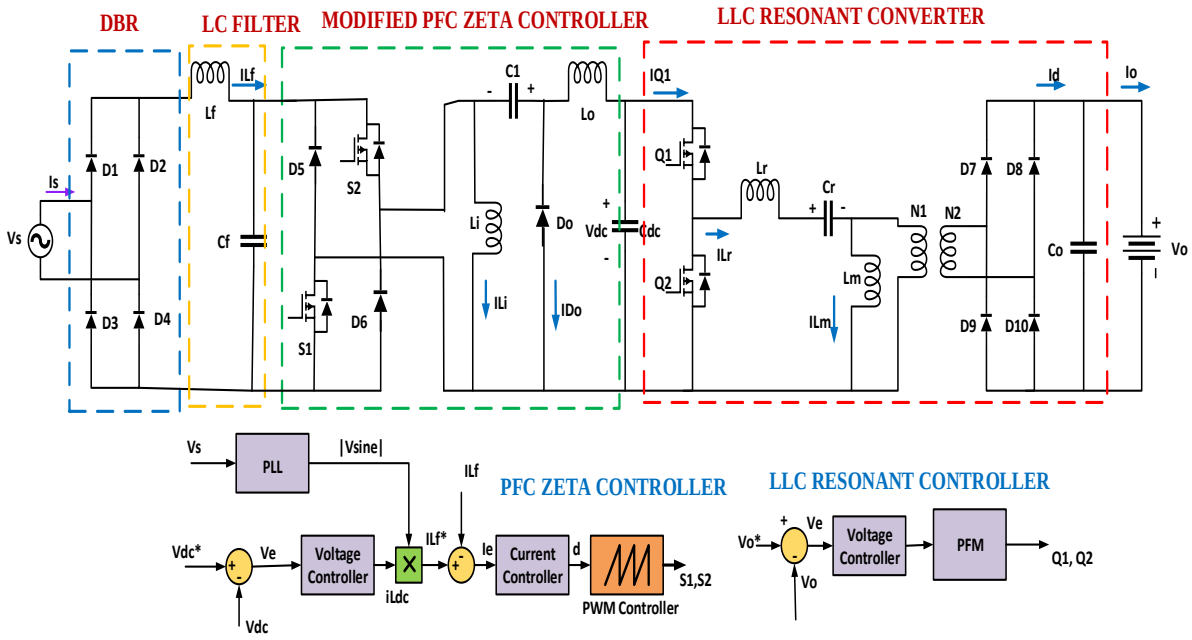


Fig. 4.2 Battery Charger with Modified non-isolated Zeta Converter fed LLC Resonant Converter

There are various advantages of the Modified Zeta Converter which includes:

a. The peak voltage stress across the modified zeta converter is ($V_{s1} = V_{s2} = V_{in}$) whereas conventional Zeta converter voltage stress is given as ($V_{s1,s2} = V_{in} + V_{dc}$) , it implies that the voltage stress across the device in modified Zeta converter is half in comparison

with conventional Zeta Converter and this is because of the use of clamping diodes (D_5, D_6).

b. This charger works on wide range of input AC voltage.

c. The efficiency of battery charger is high. For off-board charger, minimum distortions will be there on the grid which will lead to grid stability and installation of multiple chargers on the single station can be done easily. For on-board charger, the possibility to pollute the grid will be minimum and the charger is easy to plug in.

d. Input current Harmonics are less

e. THD is improved

4.3 Modes of Operations of Modified Zeta converter

The operating principle of Modified zeta converter is explained below. Fig 4.3 shows the operating waveforms and Fig 4.4 (a)-(c) shows various modes of operations of front-end Modified Zeta Converter cascaded with HB-LLC Resonant Converter, which can be explained as:

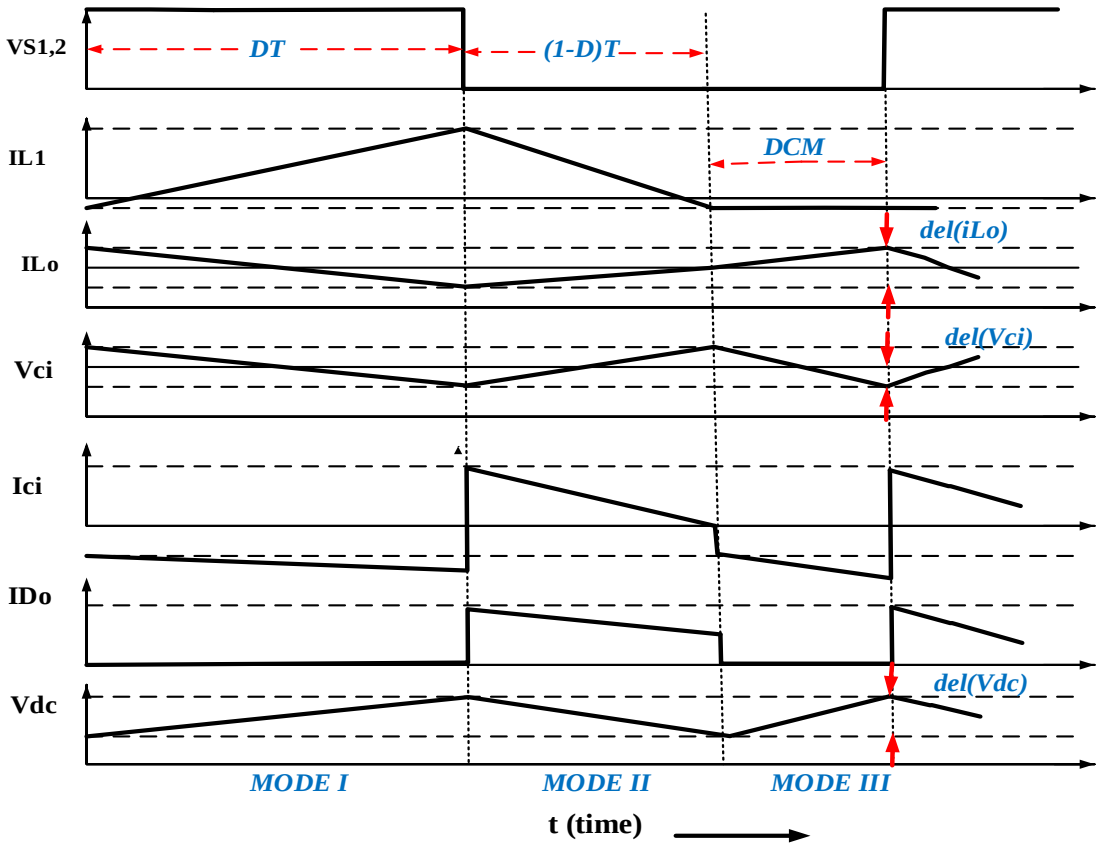
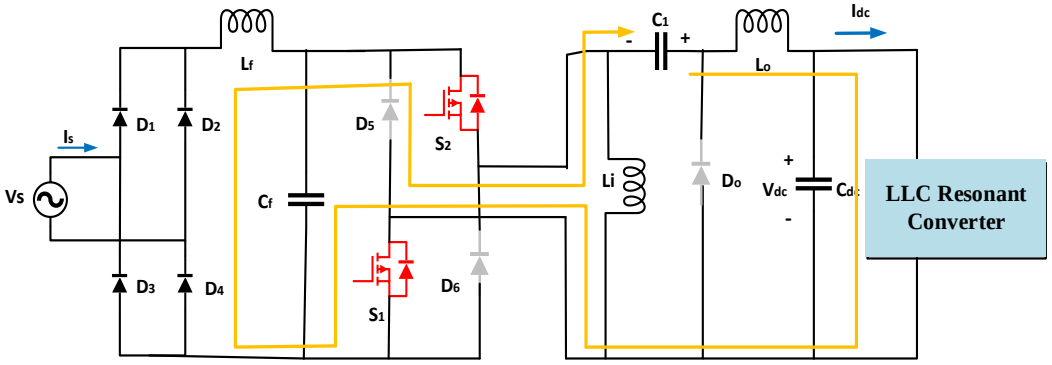
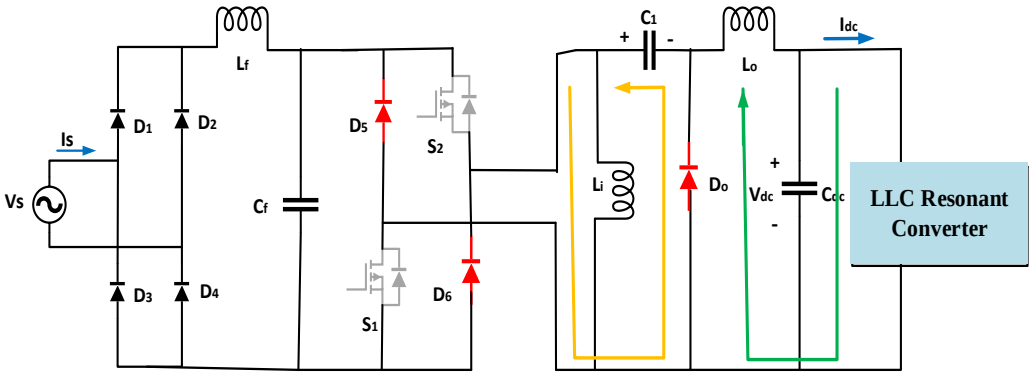


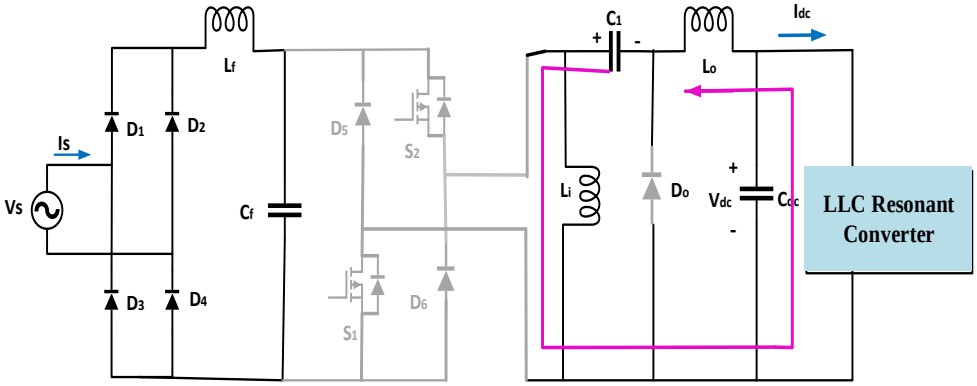
Fig. 4.3 Operating waveforms of Modified Zeta Converter fed half bridge LLC Resonant Converter



(a) Mode I



(b) Mode II



(c) Mode III

Fig. 4.4 Modes of Operations of Modified Zeta Converter fed HB-LLC Resonant Converter, (a) Mode-I Operation, (b) Mode-II Operation, (c) Mode-III Operation.

Mode-I: In this mode, gating signals are provided to both switches S_1 *and* S_2. As it can be seen in Fig 4.3 and 4.4 (a), the inductance L_i starts charging from supply as shown in the waveforms. Since the inductance L_o starts to store the energy, the voltage of the transfer

capacitance C_i began to reduce. At this instant, the diode D_o does not conduct as it will be reverse biased.

Mode-II: Both switches S_1, S_2 are turned OFF i.e., both switches are in OFF state. The clamping diodes D_5 and D_6 and D_o (Output Diode) are forward biased as given in Fig 4.3 and Fig 4.4 (b). During this period, inductance L_i starts discharging via the diodes D_5 and D_6. Transfer capacitance C_i starts charging by making D_o as forward biased. The output inductance L_o supplies to the next stage by the help of diode D_o and the DC-Link capacitor C_{dc}.

Mode-III: In this mode, switches S_1, S_2 and the clamping diodes (D_5, D_6) remains OFF. The Zeta converter enters in DCM mode, also known as Freewheeling period and can be observed in Fig 4.3 and Fig 4.4 (c). The current starts flowing from inductance L_i and L_o in such a way that the diode current (I_{do}) is reduced to zero which can be observed in the waveforms of I_{Li}, I_{Lo} and I_{do} shown in the Fig 4.3. The capacitance C_1 (transfer capacitance) helps to provide sufficient energy to the load by the help of inductance L_o and DC-Link Capacitance C_{dc}.

The peak voltage stress across the device (switches or diodes) is,

$$V_{s1} = V_{s2} = V_{in} \qquad (4.1)$$

whereas, conventional Zeta converter voltage stress is given as

$$V_{s1,s2} = V_{in} + V_{dc} \qquad (4.2)$$

It implies that the voltage stress of the modified Zeta converter is half as compared to conventional Zeta Converter and this is because of the use of clamping diodes (D_5, D_6).

4.4 DESIGN CONSIDERATIONS OF MODIFIED ZETA CONVERTER

The design of the Modified Zeta with HB-LLC Converter is shown in this section. The voltage across DC-Link of modified zeta converter is maintained at 300V and LLC Resonant output voltage is controlled at 65V. The design considerations can be divided into two sections:

4.4.1 Design of Modified Zeta Converter

The instantaneous duty cycle of Modified Zeta converter is calculated as,

$$D(t) = \frac{V_{dc}}{v_i(t) + V_{dc}} = \frac{V_{dc}}{v_s\sqrt{2} + V_{dc}} = 0.49 \qquad (4.3)$$

where, $v_i(t)$ is the instantaneous line voltage for DCM operation of Zeta converter. The switching frequency is taken as 20KHz.

The critical input inductance (L_i) is calculated as,

$$L_i = \left(\frac{{V_s}^2}{P}\right).\frac{T_s}{2}.\frac{V_{dc}}{V_S\sqrt{2}+V_{dc}} = 0.71mH \quad (4.4)$$

Where, P is the output Power, V_{dc} is DC-Link voltage of Zeta Converter. The critical series Capacitance (C_i) is calculated as,

$$C_i = \frac{P}{\delta f_s \left(V_S\sqrt{2}+V_{dc}\right)^2} = 0.94\mu F \quad (4.5)$$

where, δ is the voltage ripple considered for series capacitance and is taken as 12%. The critical output inductor (L_o) is given as,

$$L_o = \left(\frac{{V_s}^2}{P}\right).\frac{1}{\varepsilon f_s}.\left(\frac{V_{dc}}{V_S\sqrt{2}+V_{dc}}\right) = 5.58mH \quad (4.6)$$

where, ε is permissible ripple in the current of output inductor and is taken as 25%. The DC-Link capacitance (C_{dc}) of the modified zeta converter is calculated as,

$$C_{dc} = \frac{I_{dc}}{2\times 2\pi f \partial V_{dc}} = \frac{P}{2\times 2\pi f \lambda V_{dc}} = 600\mu F \quad (4.7)$$

∂ is voltage ripple considered for output capacitance and λ is voltage ripple considered for DC-Link capacitance and are taken as 0.2% and 2.5% respectively.

The filter capacitance (C_f) and filter inductance (L_f) is calculated as,

$$C_f = \frac{P.\tan(\theta)}{(2\pi f V_s)^2} = 895nF \quad (4.8)$$

$$L_f = \left[\frac{1}{4\pi^2 {f_c}^2 C_f}\right] - \left[\frac{0.04\times {V_S}^2}{2\pi f.P}\right] = 6.96mH \quad (4.9)$$

where, f_c is the critical frequency and is equal to 1/10th of the switching frequency f_s. So, the value of f_c is taken to be 2kHz.

4.4.2 Design of HB-LLC Resonant Converter

The controlled DC-Link voltage of modified zeta converter is provided to HB-LLC Resonant Converter for charging EV battery. The resonant frequency is taken as 50kHz to give the output voltage of 65V and output current of 13.07A. The turn ratio (T) of the transformer is calculated as,

$$T = \frac{V_{dc}}{2V_o} = \frac{300}{2\times 65} = 2.307 \quad (4.10)$$

The peak current of the resonant tank (I_{LR}) is determined as,

$$I_{LR} = \frac{2\pi P_o}{2V_{dc}}$$

$$I_{LR} = \frac{2 \times 3.14 \times 850}{2 \times 300} = 8.89A \quad (4.11)$$

where Po is the output Power and taking resonant frequency (f_r) to be equal to 50kHz, the Resonant Capacitor (C_r) can be calculated as,

$$C_r = \frac{I_{LR}}{2\pi f_r \left({}^{V_{dc}}/_{2}\right)}$$

$$C_r = \frac{8.89}{2 \times 3.14 \times \left({}^{300}/_{2}\right) \times 50 \times 10^{-3}} = 188.74nF \quad (4.12)$$

To provide a voltage gain, the ratio of the magnetizing inductance (L_m) and resonant inductor (L_r) is chosen 6. These inductances can be calculated as,

$$L_r = \frac{1}{(2\pi f_r)^2 \times C_r}$$

$$L_r = \frac{1}{(2 \times 3.14 \times 50 \times 10^{-3})^2 \times 188.74 \times 10^{-9}} = 53.73\mu H \quad (4.13)$$

$$L_m = 6L_r = 6 \times 53.73\mu H = 321.75\mu H \quad (4.14)$$

Table IV and Table V shows the specifications of the parameters used to design the modified Zeta converter respectively.

TABLE IV. SPECIFICATIONS OF MODIFIED ZETA CONVERTER

S.NO.	SPECIFICATIONS	VALUES
1.	Input Voltage,V_s (Modified Zeta)	220V
2.	Output Voltage/ Current (V_{dc}/I_{dc}) (Modified Zeta)	300V/4.23A
3.	Switching Frequency f_s (Modified Zeta)	20 kHz
4.	Input Voltage,V_s (LLC Resonant)	300V DC
5.	Output Voltage/ Current (V_{dc}/I_{dc}) (LLC Resonant)	65V/ 13.07A
6.	Resonant Frequency f_r (LLC Resonant)	50 kHz
7.	Power (P)	850 W
8.	Voltage ripple taken for series capacitance C_i (δ)	12%
9.	Current ripple taken for L_o output inductor (ε)	25%
10.	Voltage ripple taken for output capacitance (∂)	0.2%
11.	Voltage ripple taken for DC-Link capacitance (λ)	2.5%

TABLE V. DESIGN PARAMETERS OF MODIFIED ZETA CONVERTER

S.No.	DESIGN VARIABLES	VALUES
1.	Critical Input Inductor (L_i)	$0.71mH$
2.	Critical Series Capacitor (C_i)	$0.94\mu F$
3.	Critical Output Inductor (L_o)	$5.58mH$
4.	DC-Link Capacitance (C_{dc})	$600\mu F$
5.	Filter Capacitance (C_f)	$895nF$
6.	Filter Inductance (L_f)	$6.96mH$
7.	Resonant Capacitor (C_r)	$188.74nF$
8.	Magnetizing Inductance (L_m)	$53.73\mu H$
9.	Resonant Inductor (L_r)	$321.75\mu H$

4.5 CONTROL OF EV CHARGER

The EV battery charger of modified Zeta converter cascaded with HB-LLC (Half Bridge Inductor-Inductor-Capacitor) Resonant Converter controller can be classified into two sections:

a) Control of Modified Zeta Converter

b) Control of HB-LLC Resonant Converter.

4.5.1 Control of Modified Zeta Converter

In this work, the power factor correction is done using dual-loop control technique shown in Fig. 4.5. The outer voltage loop is used to control DC Link voltage of zeta converter and the inner current loop control is used to control the output current of Zeta Converter.

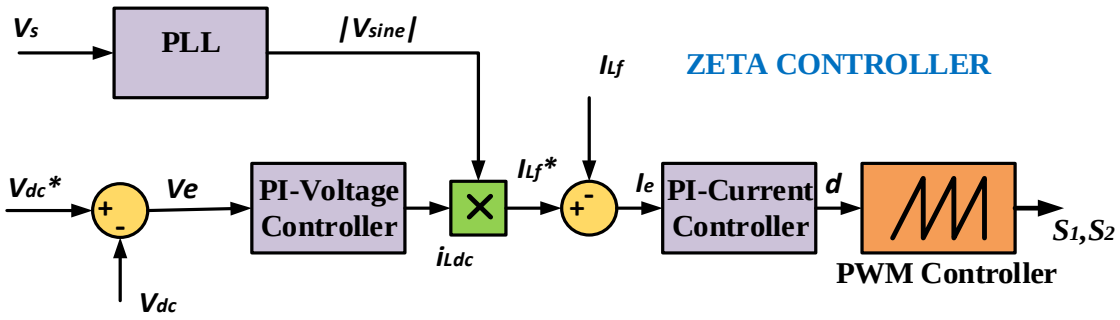


Fig. 4.5 Controller of Modified Zeta Converter

The DC-Link voltage (V_{dc}) is compared to the reference voltage ($V_{dc}{}^{*}$) which generates error in voltage (V_e) and that error is provided to PI-Voltage Controller. This output is the

modulating current signal (I_{Ldc}) and is multiplied by unit template of AC mains voltage to generate reference current for the primary inductor current ($I_{Lf}{}^{*}$). The current error (I_e) is calculated by comparing the reference current ($I_{Lf}{}^{*}$) to the primary inductor current (I_{Lf}) using the PI-Current controller. The output of PI based current controller is compared with saw-tooth carrier waveform to generate the switching pulsed which are given to switches S_1, S_2 of the modified Zeta Converter.

4.5.2 Control of HB-LLC Resonant Converter

The HB-LLC resonant converter is connected in second stage of PFC circuit. The DC-link voltage is given to HB-LLC resonant converter and its output voltage is controlled using PI-voltage controller as shown in Fig.4.6. The resultant frequency signal is processed by the Pulse Frequency Modulation (PFM) which generate the switching pulses for HB-LLC resonant converter.

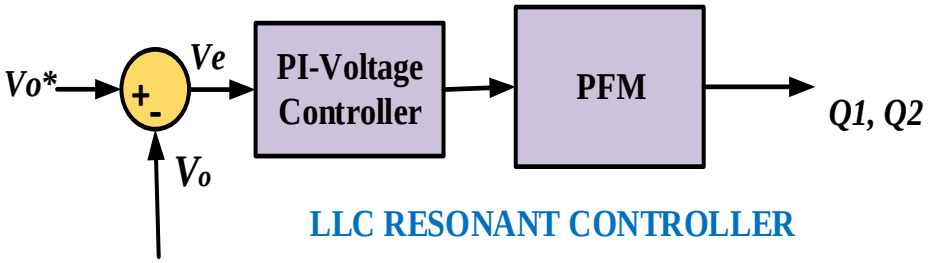


Fig.4.6 Controller of HB-LLC Resonant Converter

Pulse Frequency Modulation is a modulation method which is used to represent any analog signal using only two levels i.e. 0 or 1. PFM is similar to Pulse Width Modulation (PWM), which converts the magnitude of an analogue signal into a square wave that represents the converter's duty cycle. In PFM, the width of square pulses is fixed while the frequency is varied whereas in PWM the width of square pulse is varied at constant frequency. In Pulse Frequency Modulation, the width and amplitude of the pulses are kept constant.

The main advantages of using PFM are switching losses are reduced to some extent, thereby improves the efficiency under light loads. Other benefits of PFM include higher low-power conversion efficiency, lower total cost, and a simplified converter topology that eliminates the need for a control-loop-compensation network.

The block diagram of PFM (Pulse Frequency Modulation) can be seen in Fig.4.7 and is used in simulation to generate gate pulses for Q1 and Q2. The frequency is changed by the PFM for fixed duty cycle of 50 %.

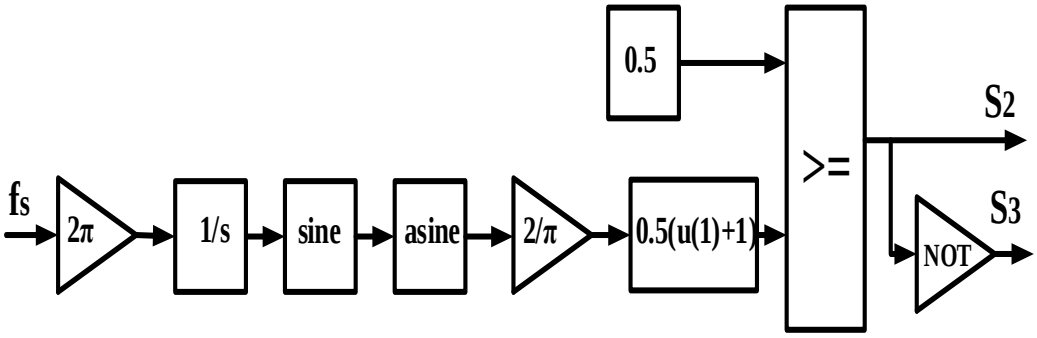


Fig. 4.7 Block Diagram of PFM (Pulse Frequency Modulation)

For the control of Modified Zeta Converter, the voltage error (V_e) generated on comparison with reference DC-link voltage is processed by Proportional-Integral (PI) controller and its resultant is given by the help of equation,

$$i_{Ldc}(n) = i_{Ldc}(n-1) + G_{pv}\{v_e(n) - v_e(n-1)\} + G_{pi}v_e(n) \quad (4.15)$$

Where G_{pv} and G_{pi} are proportional gain and integral gain for the voltage controller.

The input voltage sine template is multiplied with voltage loop output to generate reference primary inductor current is given as,

$$I_{Lf}{}^{*}(n) = I_{Ldc}(n) \times v_{\sin e}(n) \quad (4.16)$$

The current error (I_e) is passed through the PI controller and resultant is expressed as,

$$d(n) = d(n-1) + G_{pi}\{I_e(n) - I_e(n-1)\} + G_{ii}I_e(n) \quad (4.17)$$

Where G_{pi} and G_{ii} are proportional gain and integral gain for the current controller.

The second stage is formed by LLC resonant converter which uses Pulse Frequency Modulation (PFM) and voltage controller. The voltage error (V_e) generated on comparing reference output voltage and battery voltage is processed by the PI controller and output is given as,

$$f(n) = f(n-1) + G_{pllc}\{V_e(n) - V_e(n-1)\} + G_{illc}V_e(n) \quad (4.18)$$

Where G_{pllc} is the proportional gain and G_{illc} is the integral gain of Half-Bridge LLC resonant converter.

4.5 Conclusion

In this chapter, the Power Factor Correction of Modified Zeta Converter cascaded with Half Bridge LLC Resonant converter for EV Battery charging applications is studied.

Initially modelling and modes of operations were discussed. Also, the parameters of the converter are calculated and the controller of the charger is designed using dual loop controller techniques for modified Zeta converter and LLC resonant converter is designed using PFM Controller. The modified zeta converter provides the advantage of low voltage stress across the device also the output current ripple is less in case of zeta converter.

CHAPTER 5

RESULTS AND DISCUSSION

5.1 Introduction

In this chapter, the results of the proposed EV chargers will be discussed. This chapter is divided into two sections where first section includes the result of SI-SEPIC Converter cascaded with Flyback Converter and the obtained results are compared for PWM (Pulse Width Modulation) and SPWM (Sinusoidal Pulse Width Modulation) controller. The advantages of using SPWM Controller is discussed in detail. The second section includes the result of Modified Zeta converter Fed with HB-LLC Resonant Converter for EV Battery charging applications, which includes the comparison of Conventional and Modified Zeta converter. Also, the advantages of Modified Zeta Converter are discussed in detail.

5.2 MATLAB Simulation Results of SI-SEPIC Converter fed with Flyback Converter

In this section, the results of SI-SEPIC Converter cascaded with Flyback Converter based EV charger is shown, and is simulated in MATLAB-SIMULINK environment with a battery pack of 48 V, 100 Ah. Fig 5.1 represents the proposed EV Charger with SI-SEPIC converter cascaded with Flyback Converter and Fig 5.2 represents the MATLAB Simulink model of the proposed converter.

This work presents a two-stage EV charger with Switched Inductor (SI)-SEPIC converter cascaded with Flyback Converter for providing high-frequency isolation. The main advantage of this work includes:

a) Reduced Duty Ratio (D) operation,
b) Provides lesser voltage stress across the switch.
c) The converter consists of switched inductors L_m and L_a at stage-I along with two switches S_m and S_a with auxiliary components like C_a and D_{oa} used to provide high gain to the converter.
d) Improved efficiency
e) Reduction in THD (Total Harmonic Distortion)

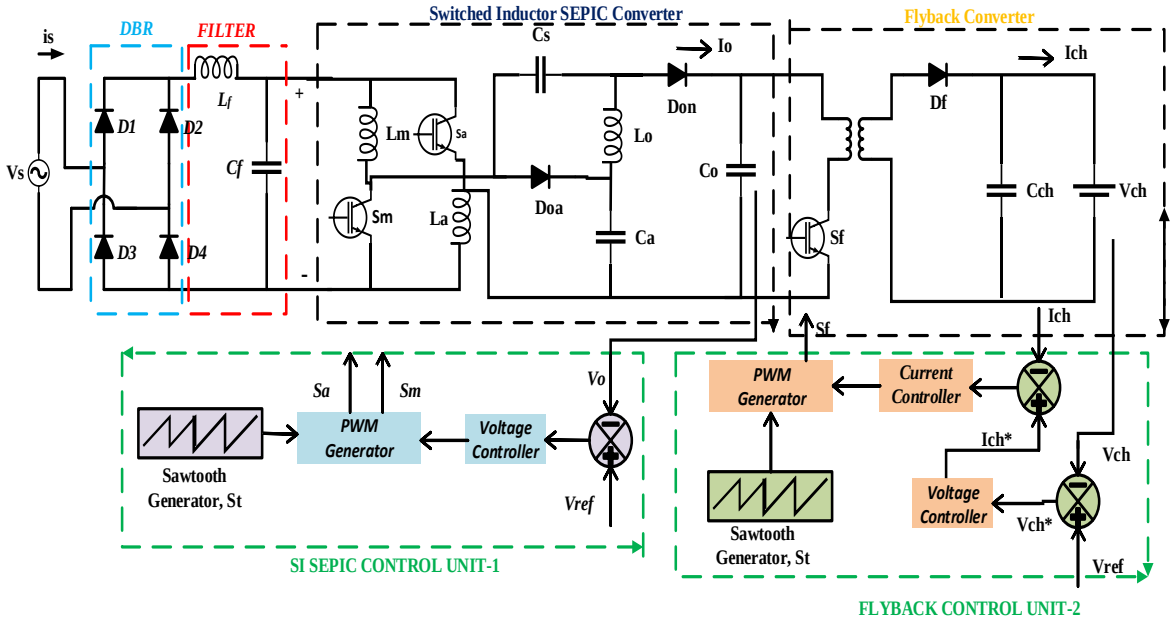


Fig 5.1 Proposed EV battery charger with SI-SEPIC Converter cascaded with flyback converter

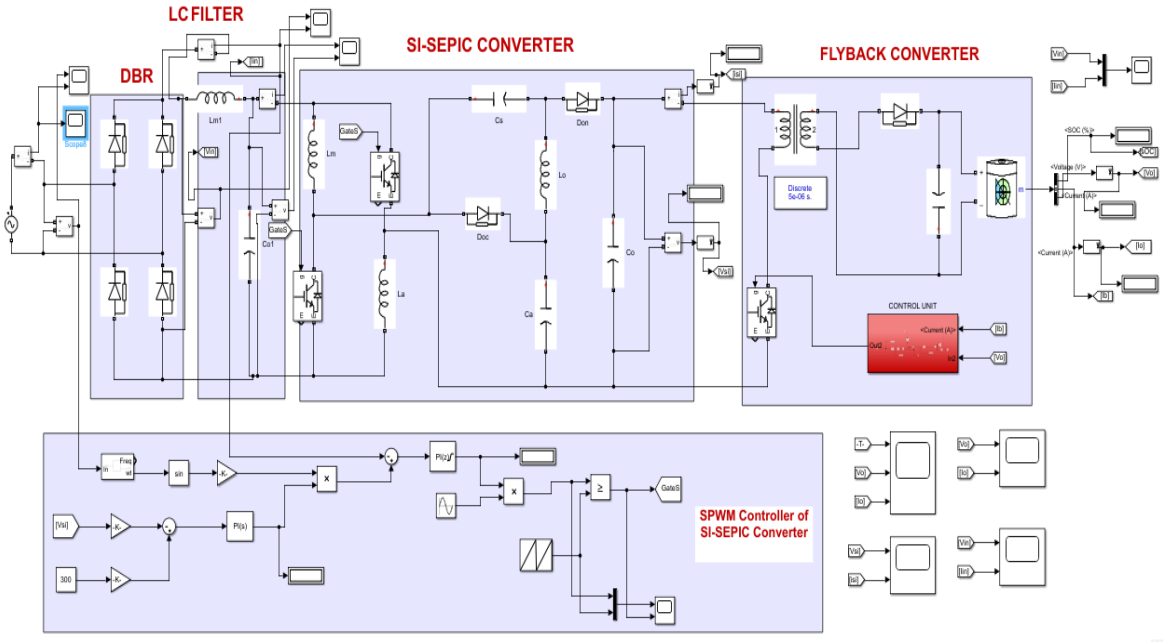


Fig. 5.2 MATLAB Simulation Model of SI-SEPIC Converter cascaded with Flyback Converter

5.2.1 LC Filter Bode Plot

Given bode plot of LC filter in Fig 5.3 demonstrates that damping factor (ζ) operates at nearly 0.02 which means that resistive nature of the damping factor sacrificing its phase plot which is approaching its asymptotic plot. It sacrifices its phase plot for improving the efficiency and achieving high Quality factor of the filter.

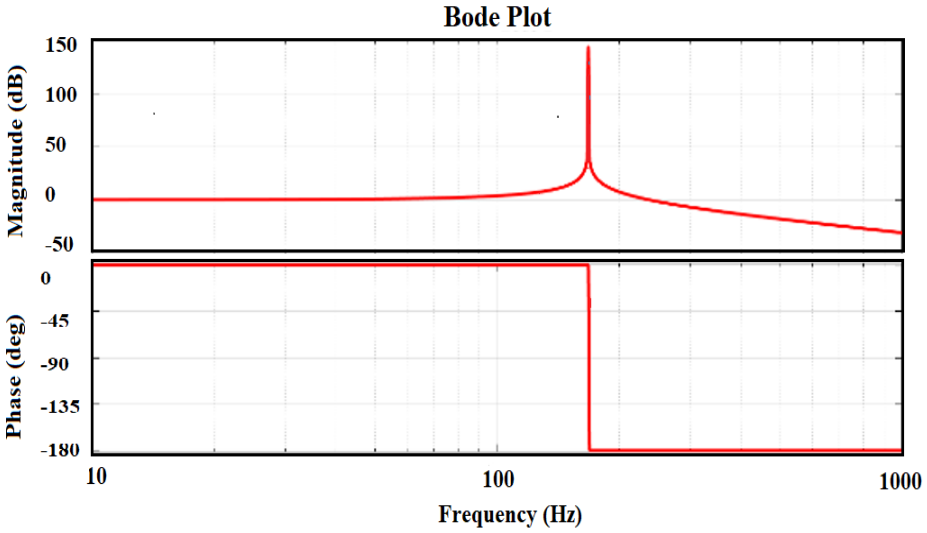


Fig 5.3 Bode plot for LC filter

5.2.2 PWM (Pulse Width Modulation) Controller

Fig 5.4 shows the input voltage and current of SI-SEPIC converter. It shows that the input current does not have the peaky components which depicts that harmonic contents are eliminated from the input current. The waveforms show that the input current exactly follows the input voltage depicting the power factor correction of the converter is done properly and the harmonics are eliminated from the input current.

Fig 5.5 shows the output voltage and current across the DBR (Diode Bridge Rectifier), depicting that both the voltage and current are almost in phase with each other, i.e, the charger is approaching unity power factor (UPF) operation.

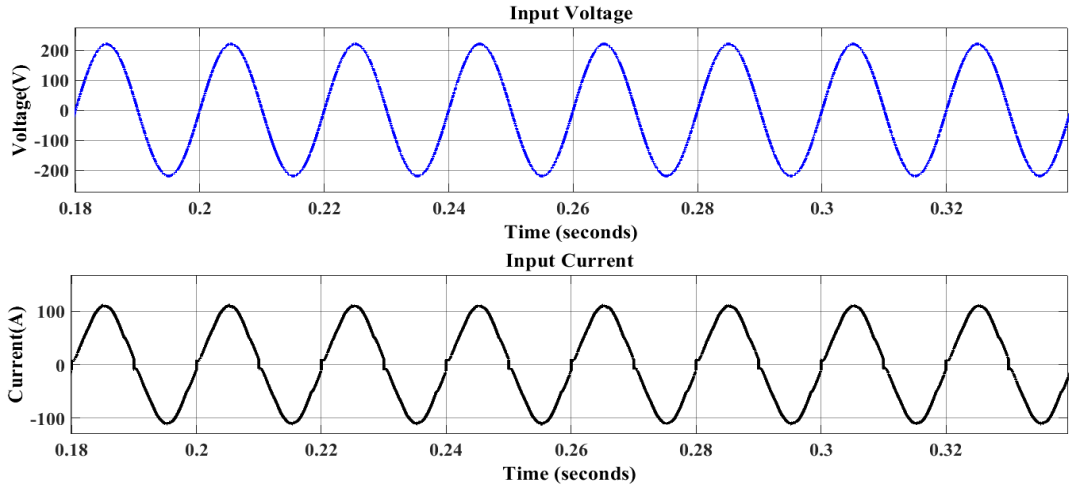


Fig. 5.4 Input Voltage and Current for SI-SEPIC converter

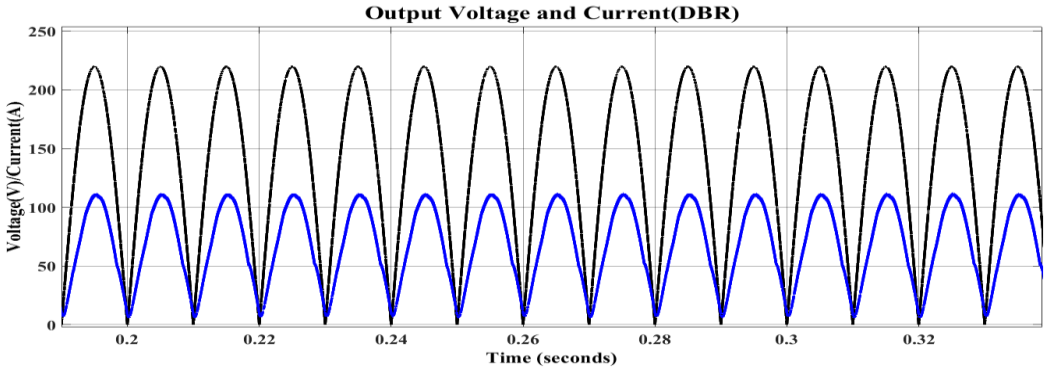


Fig. 5.5 Output Voltage and Current (across DBR)

In Fig 5.6, The outer voltage across SI-SEPIC converter is equal to 300V with a ripple of 1% in the output voltage and the current is maintained at 2.5A with a small ripple of 0.05A. The magnified view of output voltage and currents are observed in this figure which tells about the amount of ripple present in the output voltage and current. PWM (Pulse width Modulation) controller is used to maintain the voltage at 300V of SI-SEPIC converter.

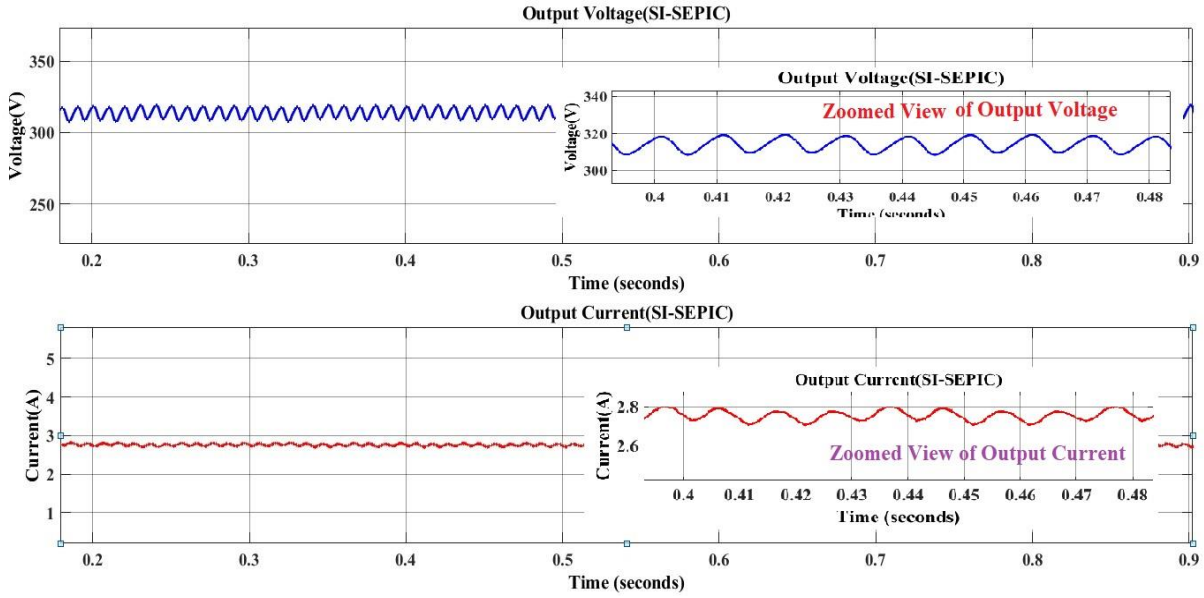


Fig. 5.6 Output Voltage and Current (across SI-SEPIC converter)

The SOC (%), voltage and current of the battery can be observed in Fig 5.7. SOC is defined as the state of charge of the battery and is a measurement of the amount of energy available in a battery at a specific point in time. It is expressed as a percentage (%).

The increasing SOC means that the battery is in charging mode. A constant current of 10.9A can be seen with current ripple of 0.15A for a 48V, 100Ah battery pack. From the fig 5.7, the battery voltage is observed to be 48V.

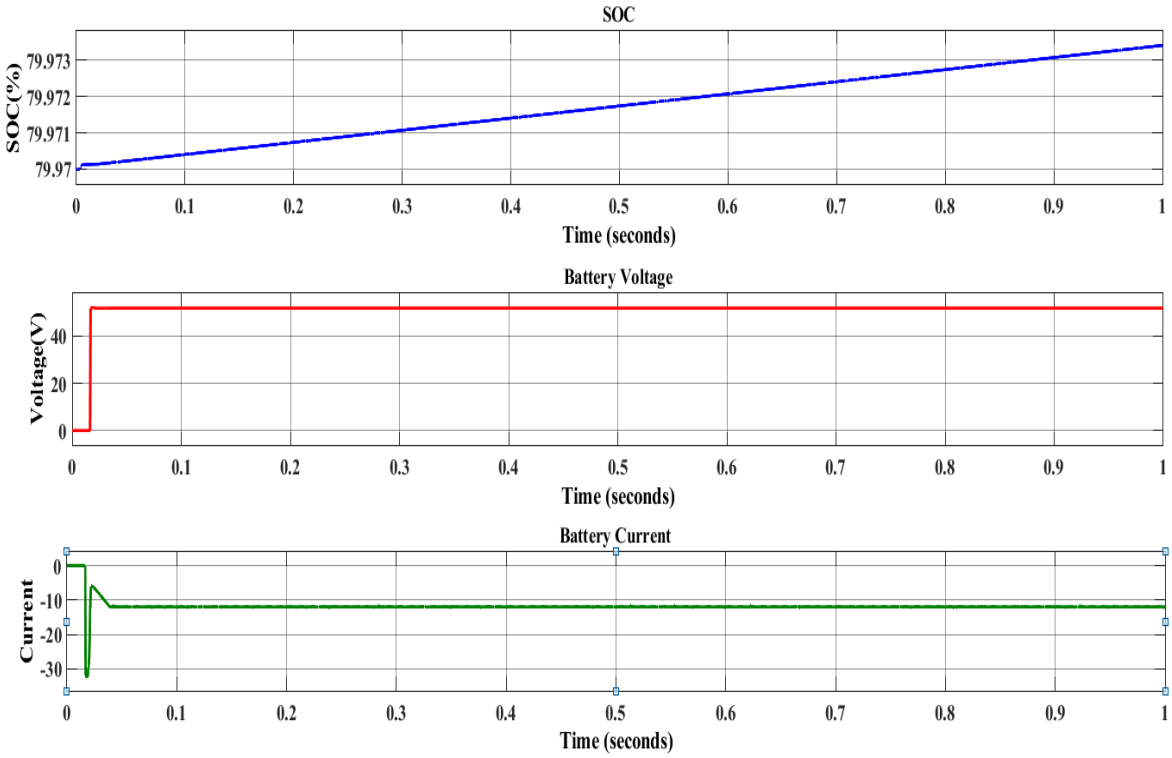


Fig 5.7 Battery SOC, Battery Voltage and Battery Current

In Fig 5.8, Total Harmonic Distortion (THD) in input current of the proposed SI-SEPIC converter cascaded with Flyback converter is observed to be 4.81%, which yields to the power factor of 0.92.

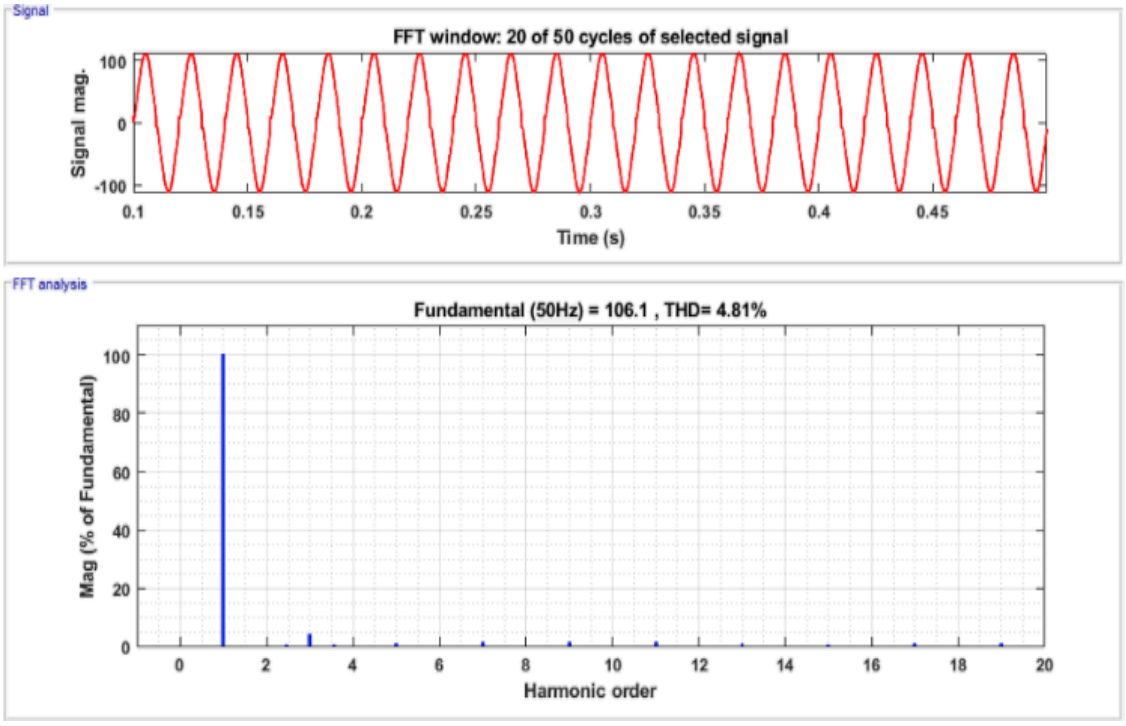


Fig. 5.8 THD (%) in input current using PWM controller

5.2.3 SPWM (Sinusoidal Pulse Width Modulation) Controller

Fig 5.9 shows the SPWM (Sinusoidal Pulse Width Modulation) comparator where the triangular pulses (S_t) and the sinusoidal pulses are compared and the switching signals are given to switches S_m and S_a.

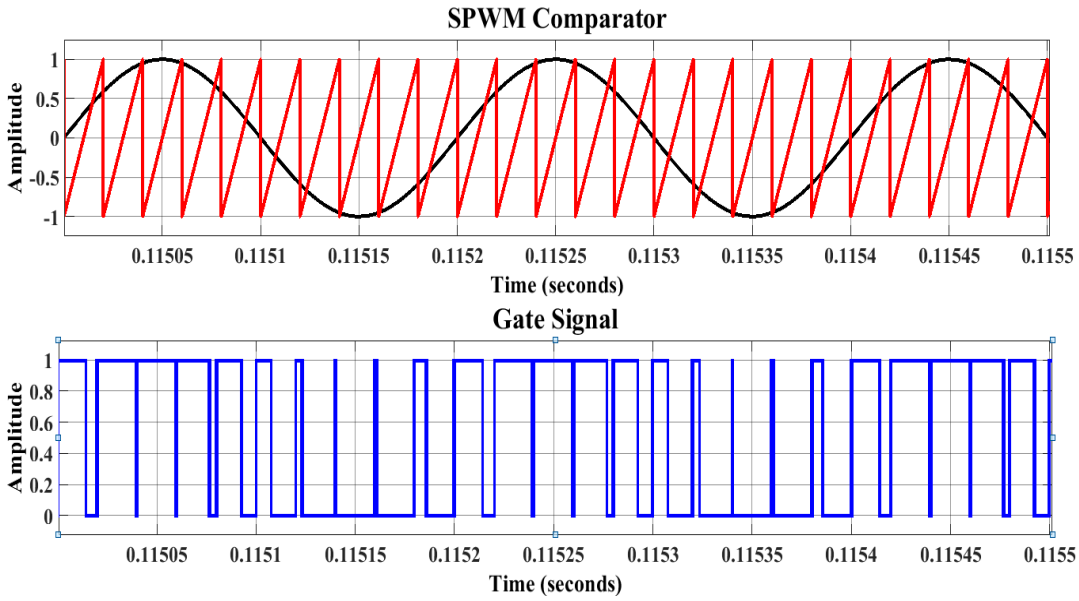


Fig 5.9 SPWM comparator and Switching signals given to S_a and S_m

In Fig 5.10, the input voltage (V_{in}) and Input current (I_{in}) can be observed. The input voltage of 220V is given to the SI-SEPIC converter which generates sinusoidal mains current using LC filter and SPWM controller.

The output voltage and current across the DBR can be seen in Fig 5.11 where both current and voltage are in phase with each other which demonstrates the UPF (Unity Power Factor) operation of the EV charger.

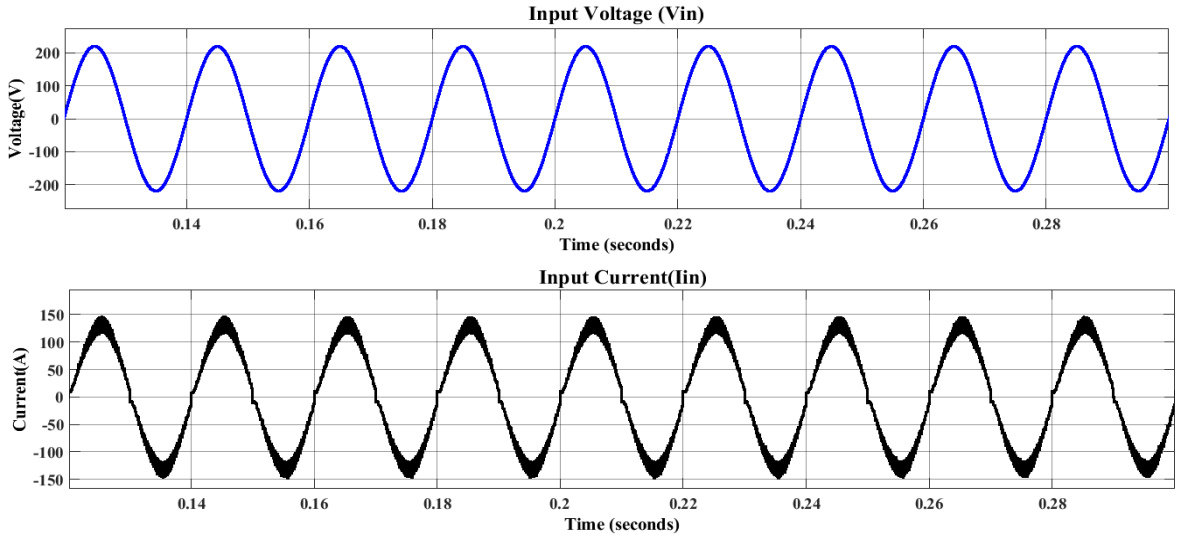


Fig. 5.10 V_{in} and I_{in} of SI-SEPIC converter

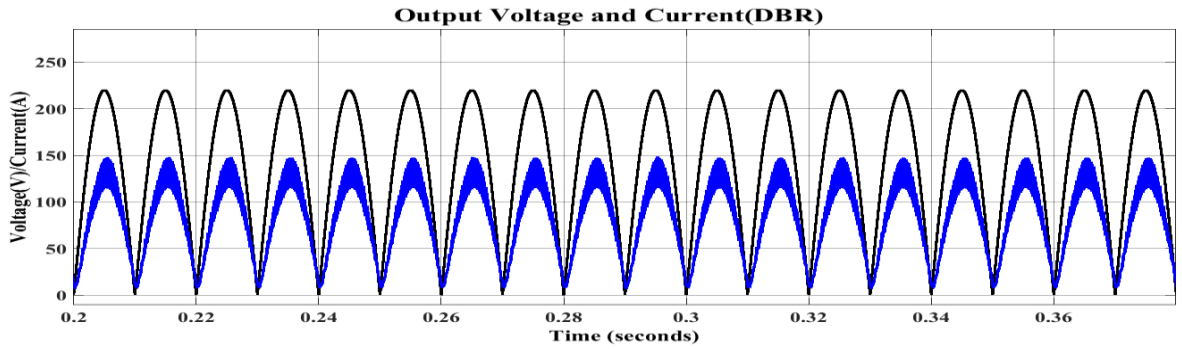


Fig. 5.11 Output Voltage and Current (across DBR)

The SOC, voltage and current of 48V, 100Ah battery can be seen in Fig 5.12. For CC-CV mode of charging, the reference voltage is taken to be 65V and output current of 10.83A can be observed across the battery having 0.04A ripple current.

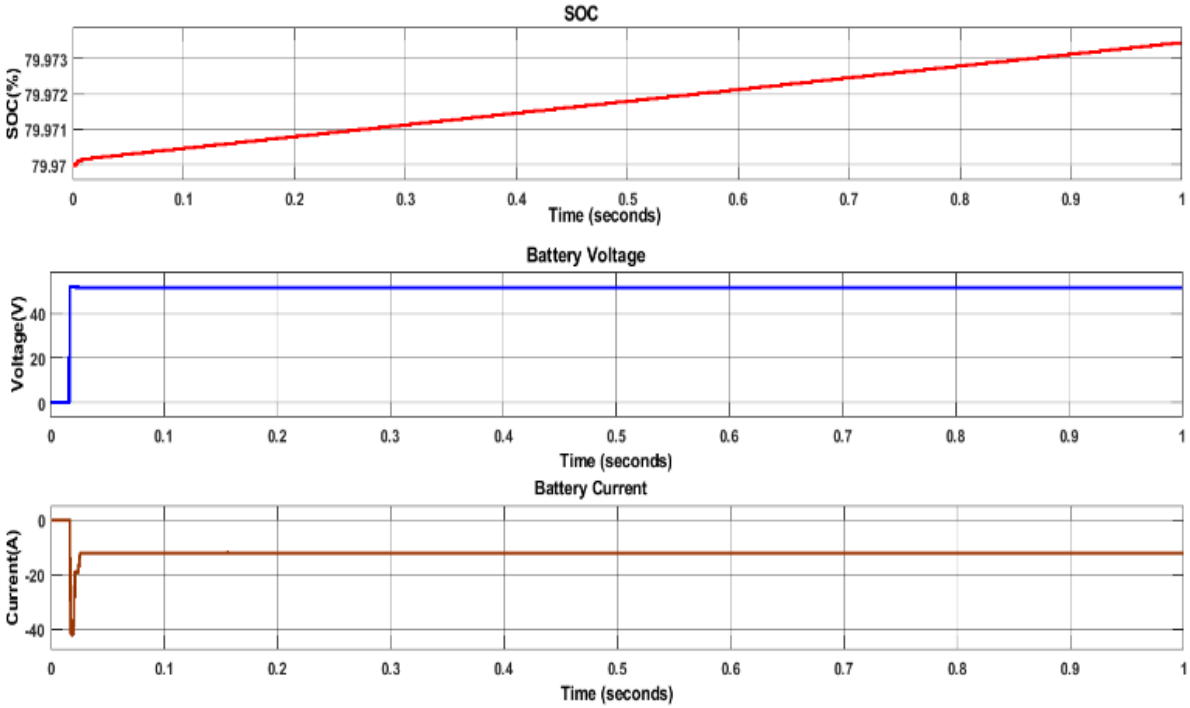


Fig 5.12 Battery SOC, Battery Voltage and Battery Current

Harmonic power factor is related to total harmonic distortion (THD), which can be calculated by the help of given equation

$$Power\ Factor = \frac{1}{\sqrt{1 + THD^2}} \qquad (5.1)$$

where, THD is the total harmonic distortion which can be calculated by,

$$THD = \frac{I_h}{I_1} = \sqrt{\frac{(I_1^2 + I_2^2 + \cdots + I_N^2 + ..)}{I_1^2}} \qquad (5.2)$$

where, I_1, I_2, ..., I_n are rms value of current the fundamental component, second harmonic, …, and N^{th} harmonic and I_h is the rms value of all the harmonic component of current.

Fig 5.13 shows the Total Harmonic Distortion of the SI-SEPIC converter using SPWM control as 3.66%, yielding to a power factor of 0.94.

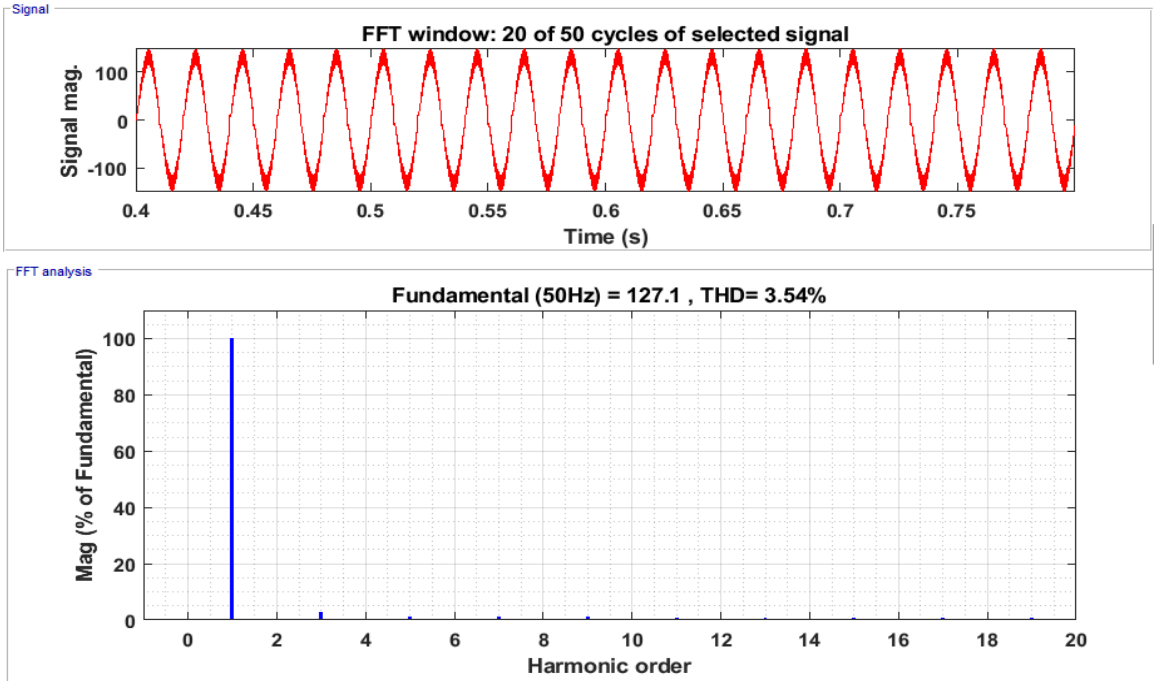


Fig 5.13 THD (%) in input current using SPWM controller

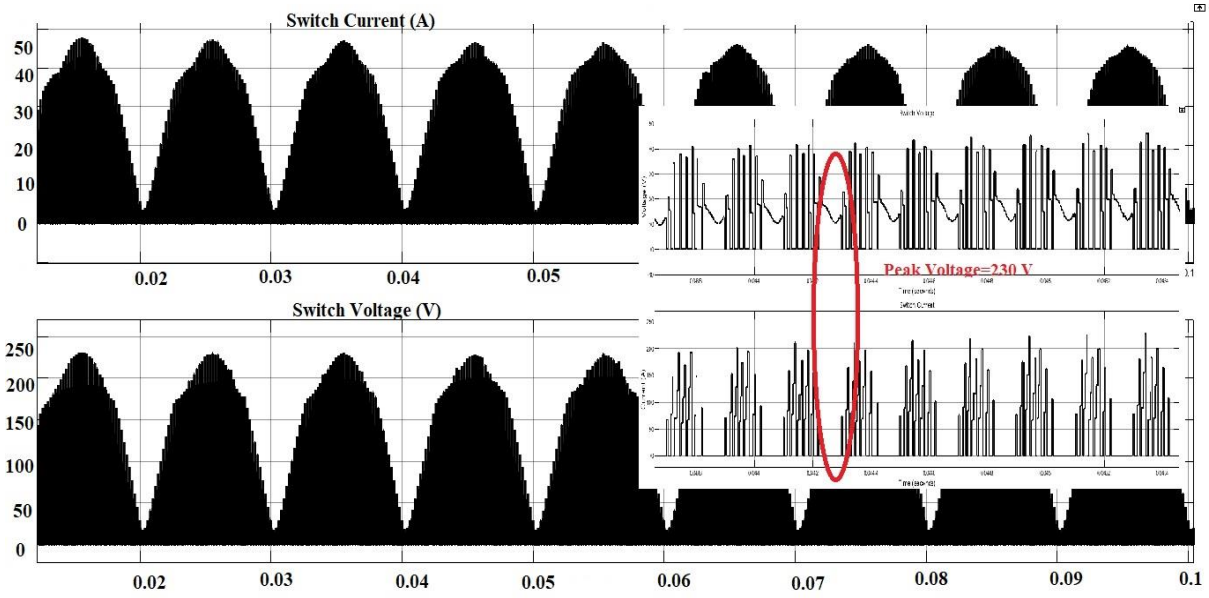


Fig. 5.14 Voltage and Current across auxiliary switches S_a and S_m

The voltage and current across the switches S_a *and* S_m can be seen in Fig 5.14. In the zoomed view it can be observed that a peak voltage tress of approx. 230 V can be observed

across the switches. Table VI shows the comparison of SI-SEPIC converter using PWM and SPWM controller techniques.

TABLE VI. COMPARISION OF CONTROLLER

Parameters	PWM Control Technique	SPWM Control Technique
Power Factor	0.92	0.94
Efficiency (%)	90%	92.8%
THD (%)	4.81%	3.66%
3rd harmonic component (%)	3.6%	2.9%
Output Current Ripple (ΔI_o)	0.15A	0.04A
Output Voltage Ripple (ΔV_o)	0.01V	0.005V

5.3 MATLAB Simulation Results of Modified Zeta Converter Fed with Half Bridge LLC Resonant Converter

In this section, the results of Modified zeta converter cascaded with HB-LLC Resonant converter are shown and is simulated in MATLAB-SIMULINK platform. Fig 5.15 shows the Battery Charger with Conventional Zeta Converter fed LLC Resonant Converter and Fig 5.16 shows the MATLAB Simulink model of Conventional Zeta Converter fed with HB-LLC Resonant Converter. Fig 5.17 shows the Battery Charger with Modified non-isolated Zeta Converter fed LLC Resonant Converter and Fig 5.18 shows the MATLAB Simulink model of Modified Zeta Converter fed with HB-LLC Resonant Converter.

The Modified non-isolated zeta converter is analogous to normal conventional zeta converter except for the addition of two clamping diodes (D_5, D_6) which are being added at the input and one switch S_2. By the help of clamping diodes, the voltage stress across the devices by clamping the voltage across the switches at input voltage V_{in}, which is half as compared to conventional Zeta Converter ($V_{in} + V_{dc}$). This reduces the losses across the device and improves the efficiency of the converter. The value of DC-Link voltage is maintained at 300V by the help of input inductor (L_i), output inductor (L_o) and series capacitor (C_i).

This configuration is being used as it reduces the voltage stress due to the presence of two switches at the input voltage, which is $1/2$ $(half)$ as compared to Conventional converter. The DC link voltage is 300V. The modified zeta converter is then followed by half bridge LLC Resonant converter. Both Zeta and HB-LLC Resonant Converters operate in DCM

(Discontinuous Conduction Mode), which reduces the diode reverse recovery time and zero current switching (ZCS).

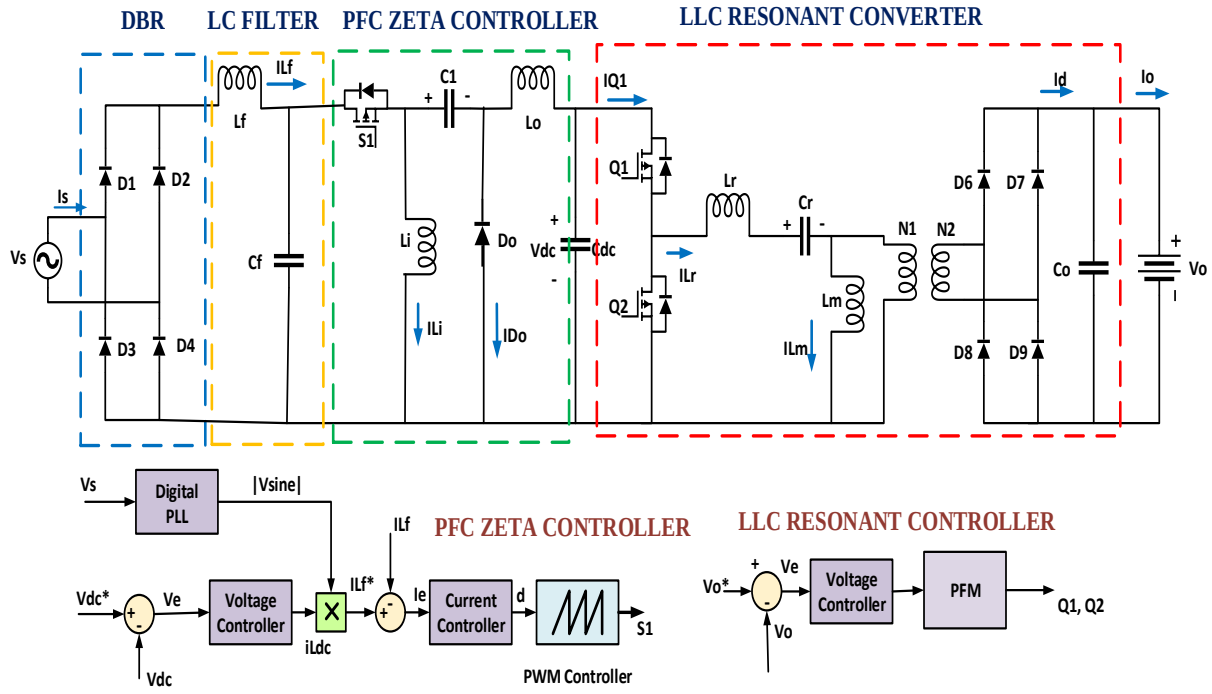


Fig. 5.15 Battery Charger with Conventional Zeta Converter fed HB-LLC Resonant Converter

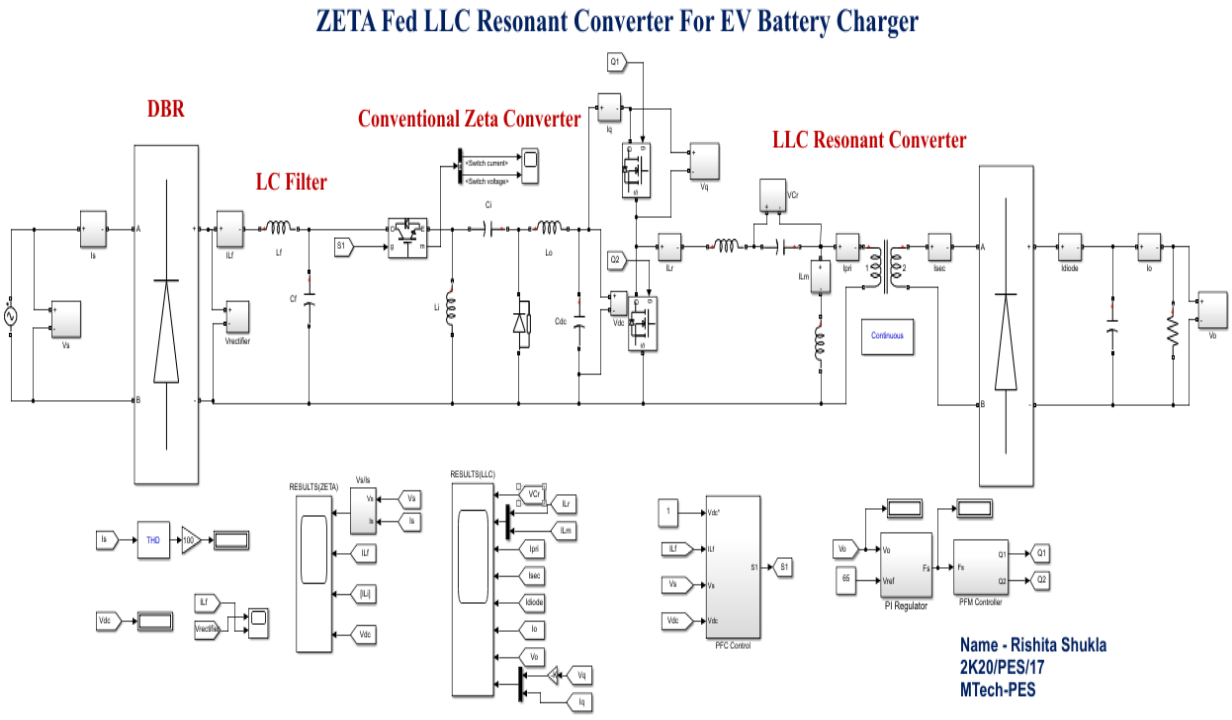


Fig 5.16 MATLAB Simulink model of Conventional Zeta Converter fed with HB-LLC Resonant Converter

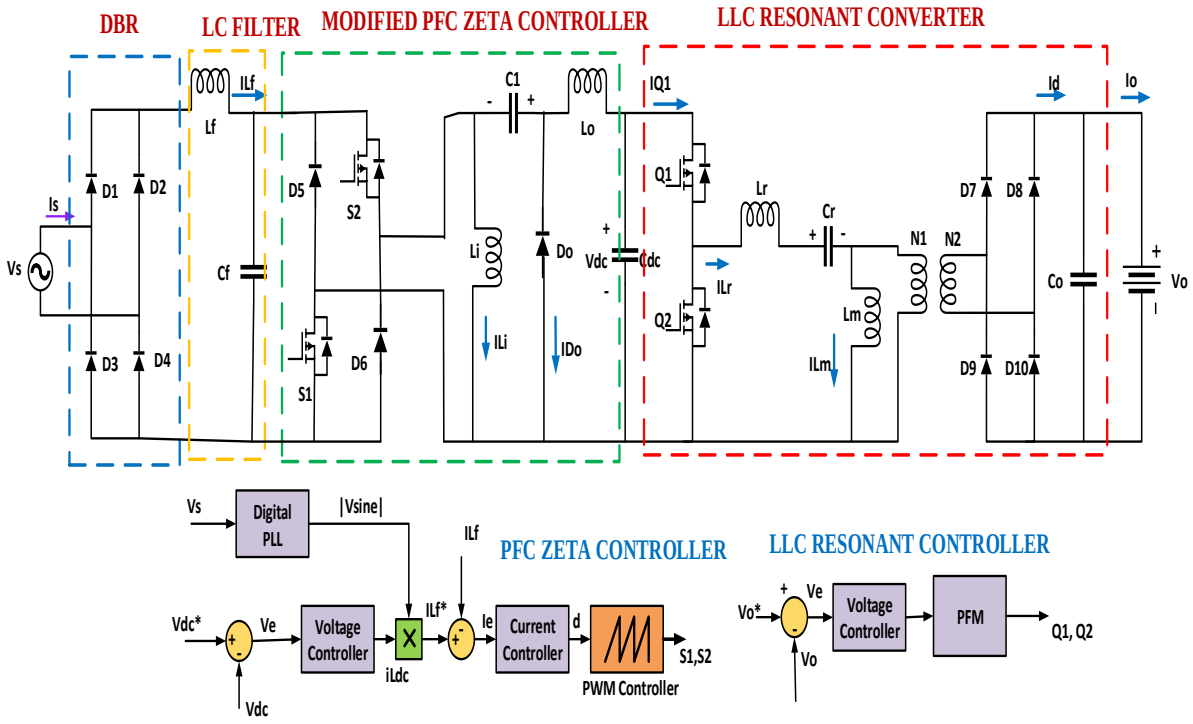


Fig 5.17 Battery Charger with Modified non-isolated Zeta Converter fed HB-LLC Resonant Converter

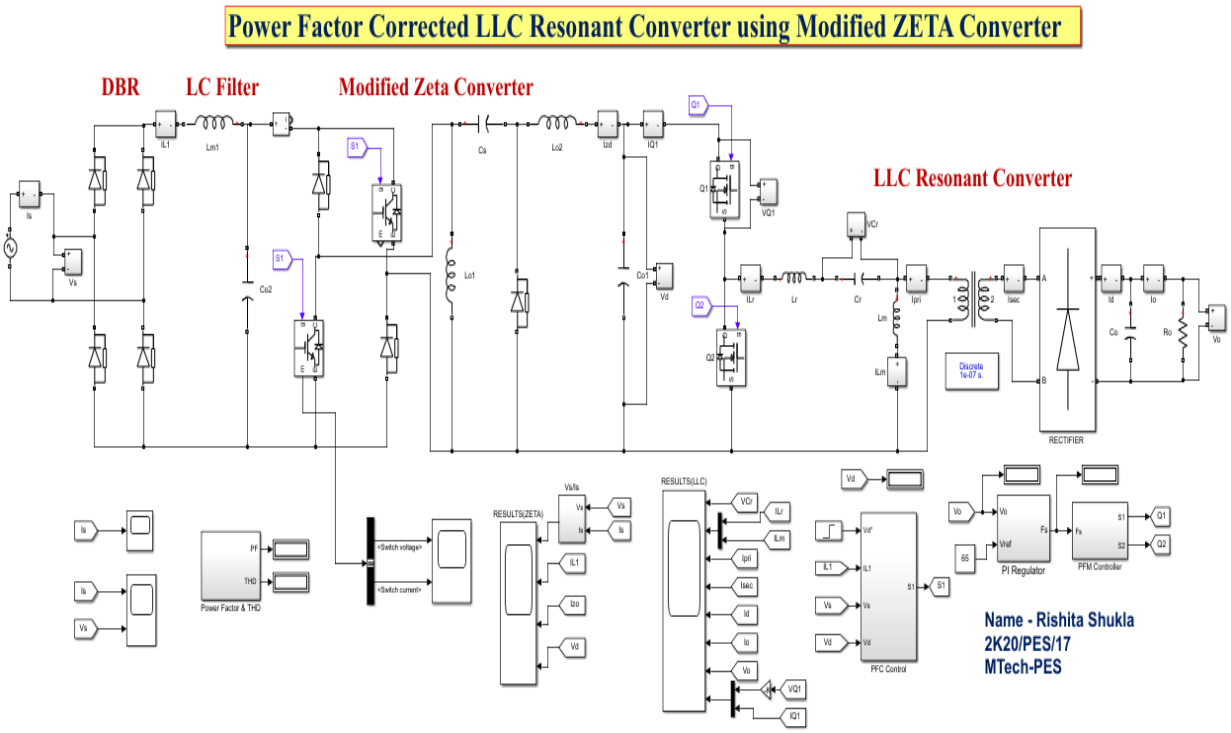


Fig 5.18 MATLAB Simulink model of Modified Zeta Converter fed with HB-LLC Resonant Converter

5.3.1 Steady State performance of the charger

The output waveforms of Modified Zeta converter fed LLC resonant converter at steady state are demonstrated in this section. This section is further divided into two subsections which shows the output waveforms of Modified Zeta converter and HB-LLC Resonant Converter for steady state performance of the charger.

5.3.1.1 Output waveforms of Modified Zeta Converter

Fig 5.19 shows input current and input voltage and both current and voltage are in phase with each other which represents the Unity Power Factor (UPF) operation of the Modified Zeta converter.

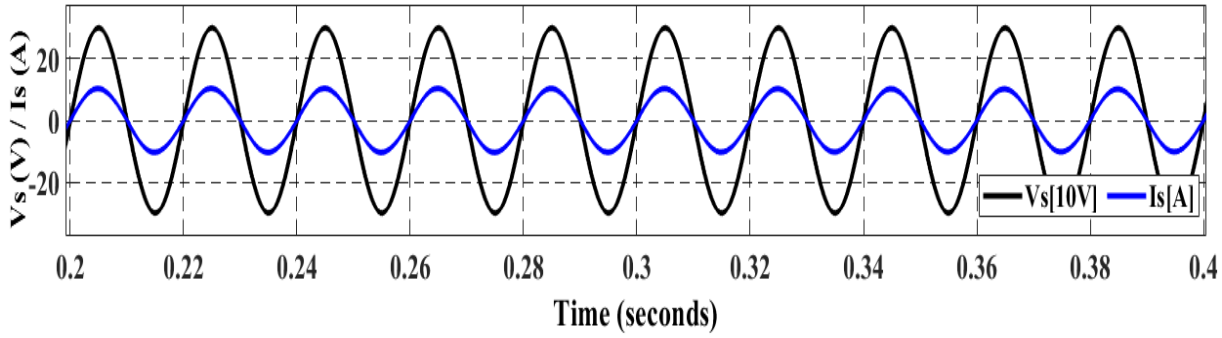


Fig. 5.19 Input Voltage and Current of Modified Zeta Converter

Fig 5.20 and 5.21 shows the current of output and input inductor respectively and Fig. 5.22 shows the DC-Link voltage of Modified Zeta converter.

The DC-Link voltage is 300V for 65V battery voltage. The magnified view of DC-Link voltage is observed in this figure which tells about the amount of ripple present in the DC-link voltage. The amount of ripple in DC-Link Voltage is 2% i.e., ripple voltage is 6V.

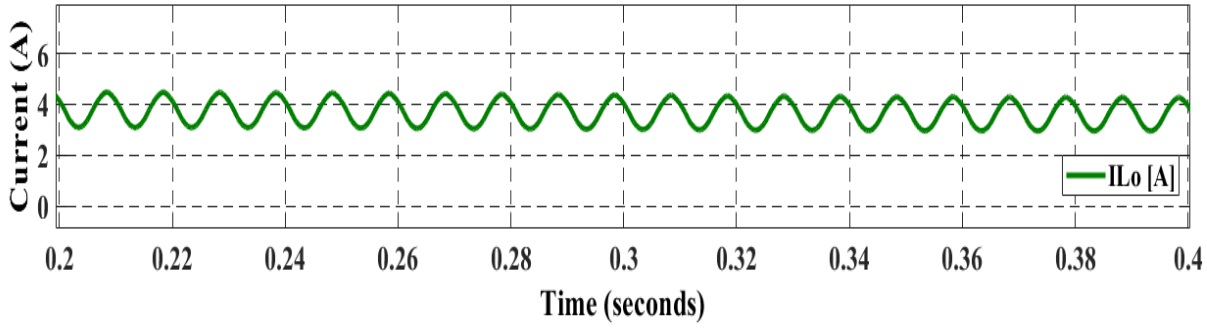


Fig. 5.20 Output Inductor Current of Modified Zeta Converter

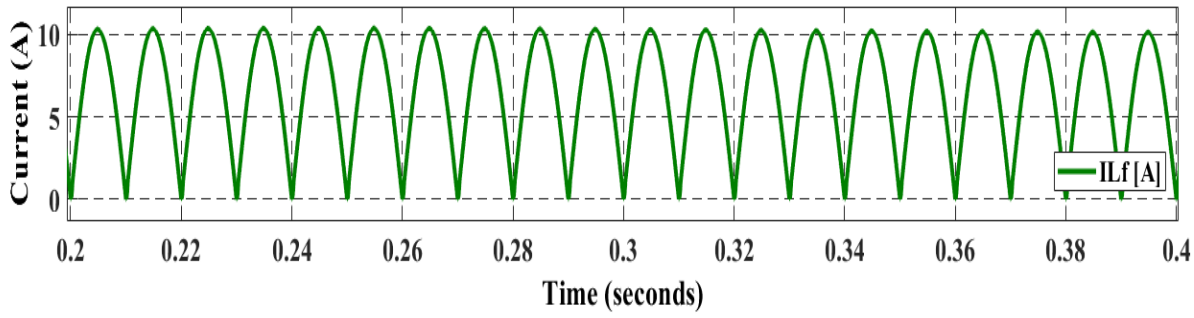


Fig. 5.21 Input Inductor Current of Modified Zeta Converter

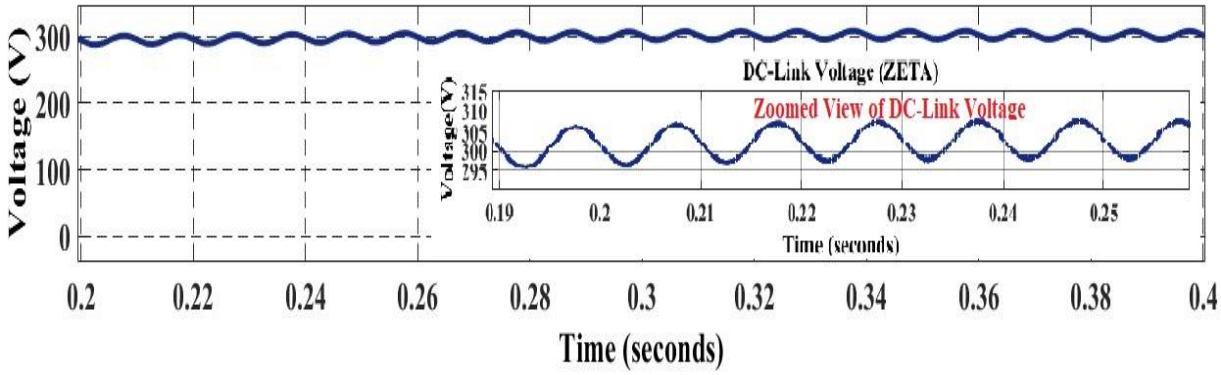


Fig. 5.22 DC-Link Voltage of Modified Zeta Converter

5.3.1.1 Output waveforms of HB-LLC Resonant converter

The output waveforms of HB-LLC Resonant converter are shown in the Fig. 5.23-5.27. Fig. 5.23 shows that the peak voltage of C_r and the voltage is observed to be 320V and in Fig 5.24 the current waveforms of L_r *and* L_m which shows that the converter is operating near resonant frequency (f_r). The peak amplitude of resonant current is 11.56 A and peak amplitude of magnetizing current is 2.87A.

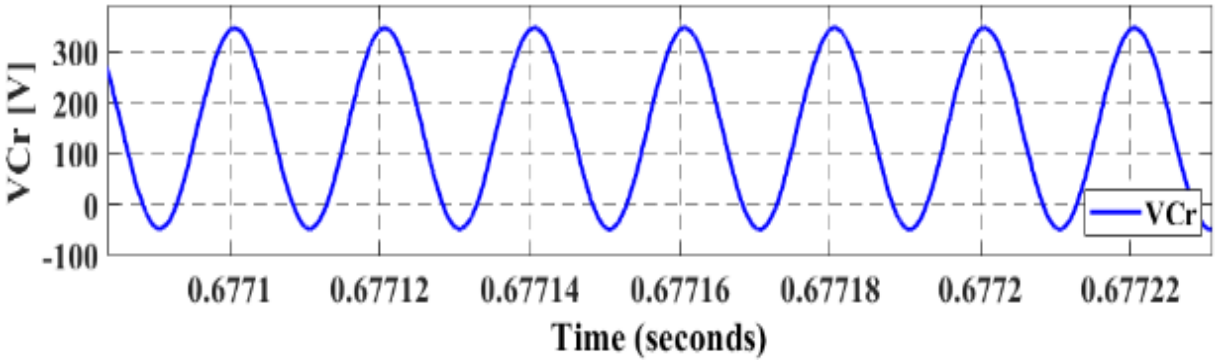


Fig. 5.23 Voltage across resonant capacitance (V_{Cr})

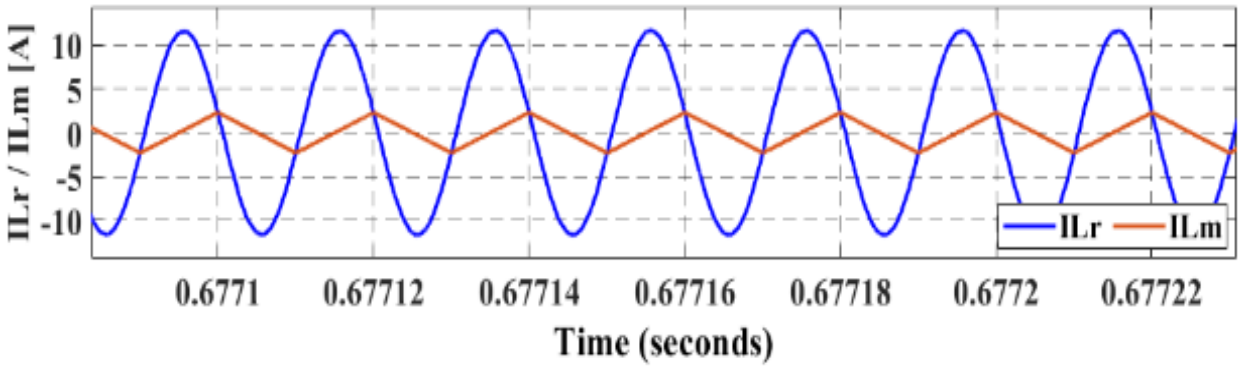


Fig. 5.24 Magnetizing inductance and resonant inductance Current waveform (I_{Lr} and I_{Lm})

The diode current (I_d) of the HB-LLC converter can be seen in Fig 5.25. Fig. 5.26 shows the voltage and current across the MOSFET which demonstrates Zero Voltage Switching (ZVS) is achieved. The voltage across the switch (V_{Q1}) and current flowing the switch (I_{Q1}) is shown in Fig 5.26. The current start rising when voltage reaches to zero. There is no overlap of current and voltage is observed.

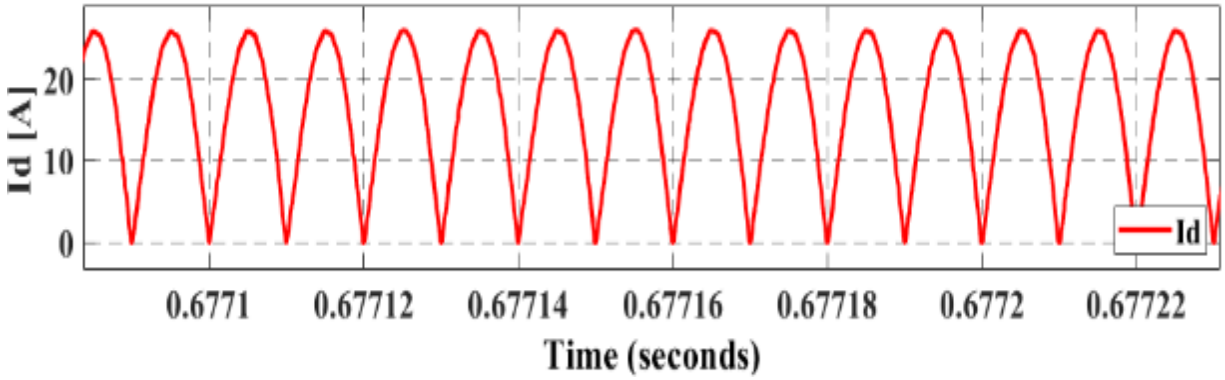


Fig. 5.25 Diode Current (I_d) of LLC Resonant Converter

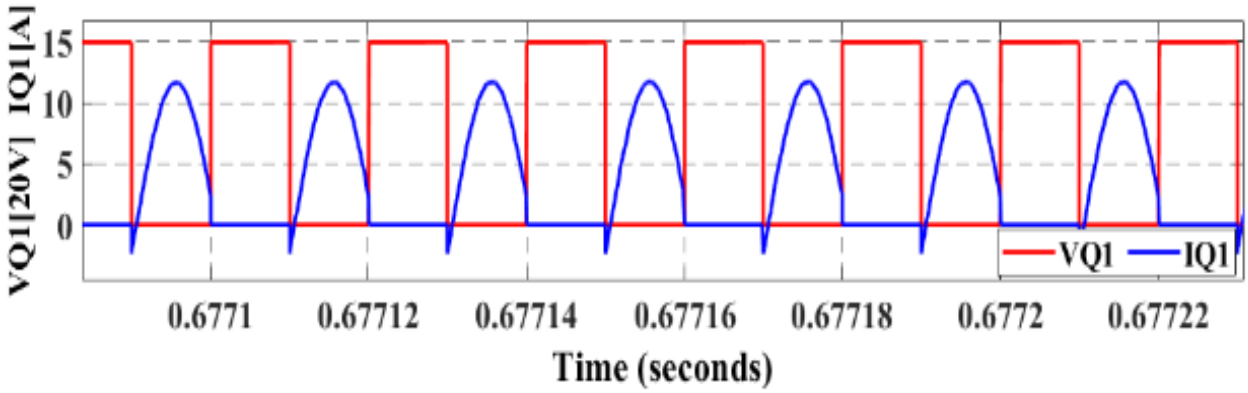


Fig. 5.26 Voltage and Current across the MOSFET Q1

As observed in Fig 5.27, a peak output current of 13.07A is observed across the battery with a ripple of 0.95% which can be observed in the magnified image of output current (I_o). From Fig 5.28, it is observed that the DC-Link voltage is 65V with a ripple voltage of 0.6V as

seen from the magnified image of output voltage (V_o) of the Half Bridge-LLC Resonant converter.

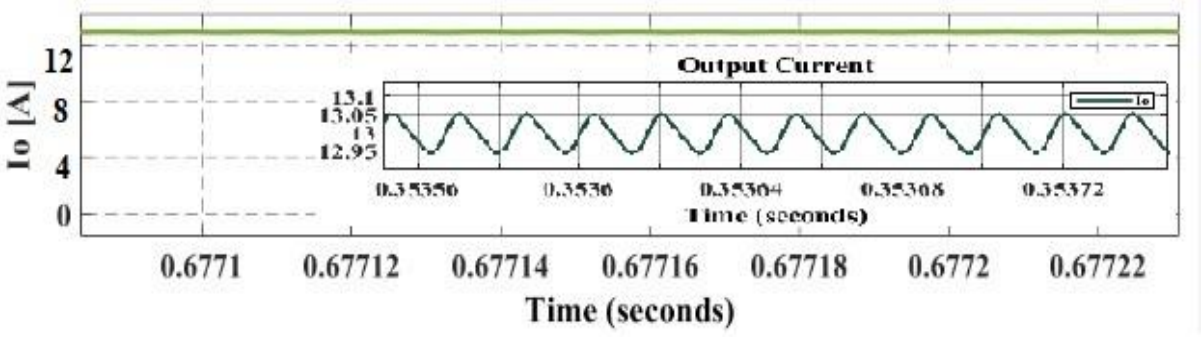


Fig. 5.27 Output Current (A) waveform of HB-LLC Resonant Converter

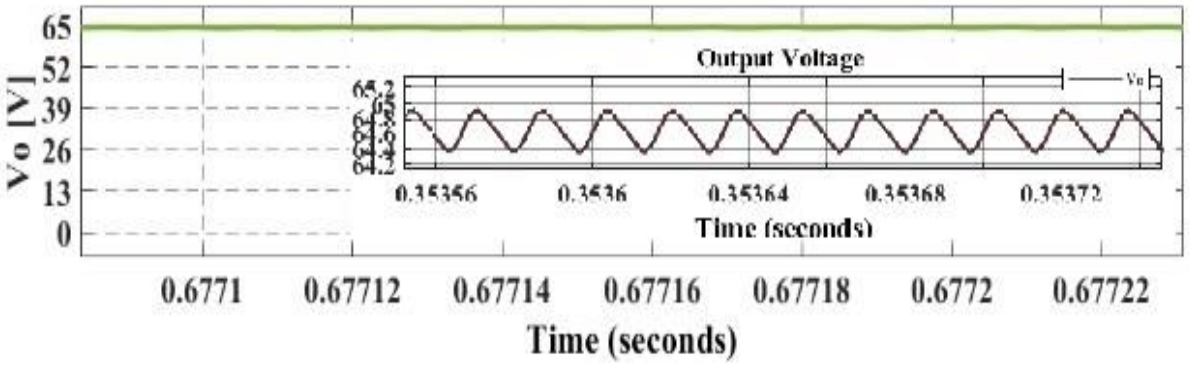


Fig. 5.28 Output Voltage (V) waveform of HB-LLC Resonant Converter

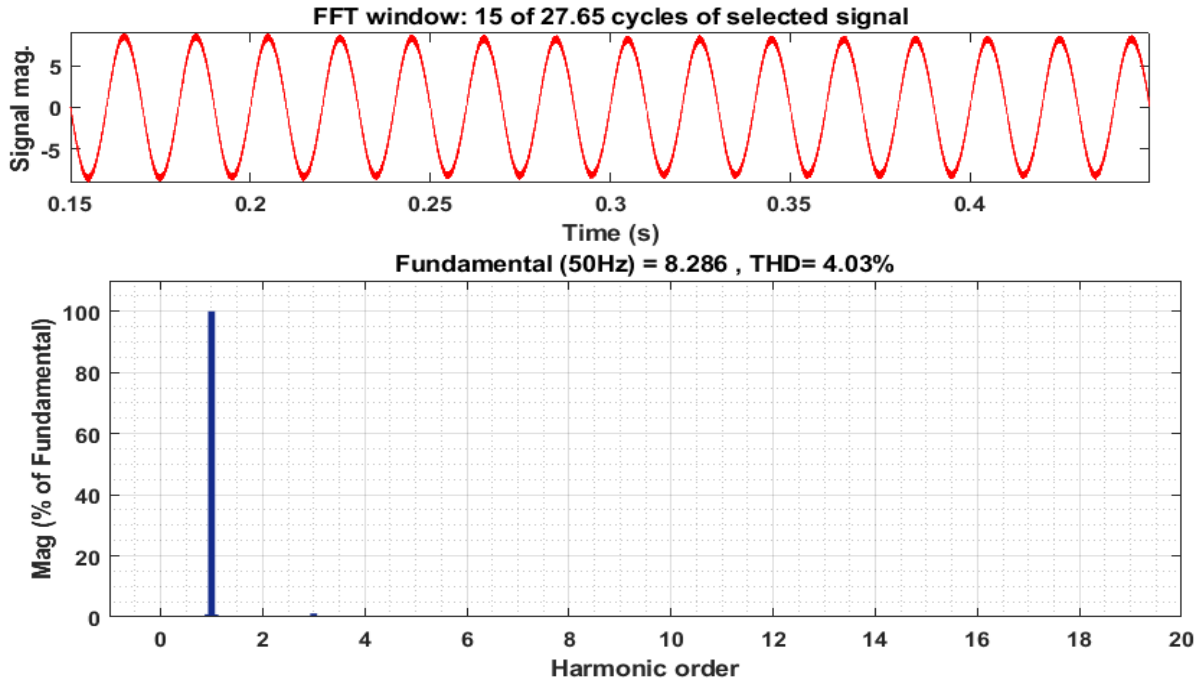


Fig. 5.29 Total Harmonic Distortion (THD) of Conventional Zeta Converter

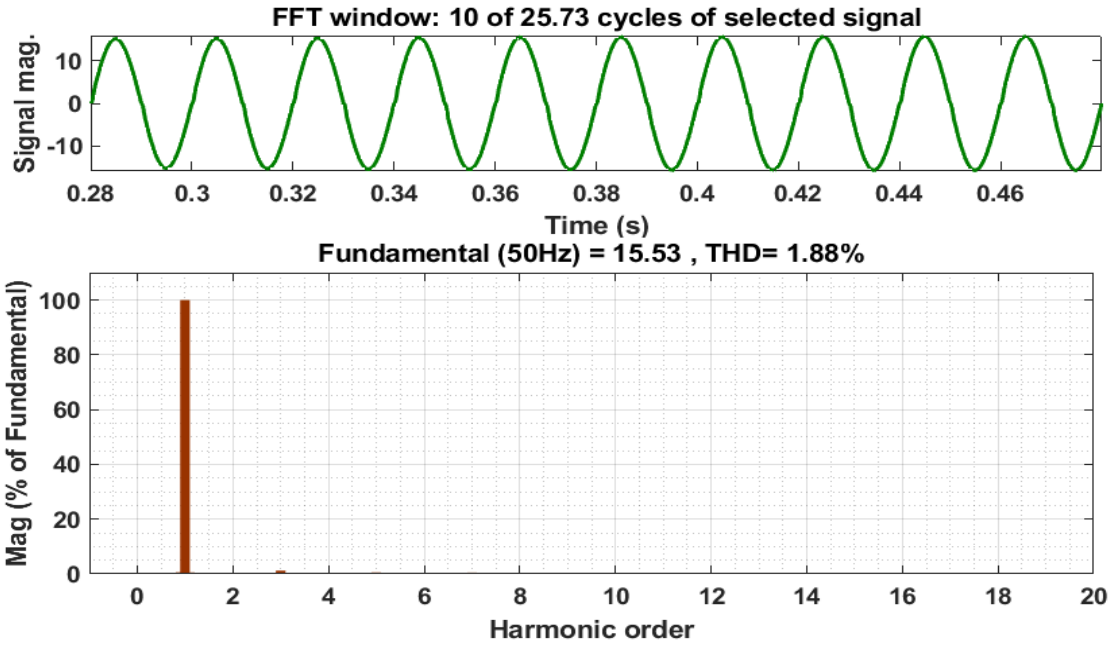


Fig. 5.30 Total Harmonic Distortion (THD) of Modified Zeta Converter

Fig 5.29 and Fig 5.30 shows the THD of conventional and Modified zeta converter which is 4.03% and 1.88% respectively giving the power factor of 0.92 and 0.98, respectively. The third harmonic component in conventional Zeta converter is 4.5% whereas in modified Zeta converter the third harmonic component is 2.03%.

5.3.2 Performance of the charger over different supply voltage

Fig. 5.31 shows the performance of charger over different supply voltage (Vs) ranging from 170V to 300V. The battery voltage remains constant at 65V through the entire variation of supply voltage. The performance of source current is excellent with THD less than 2% for the entire range.

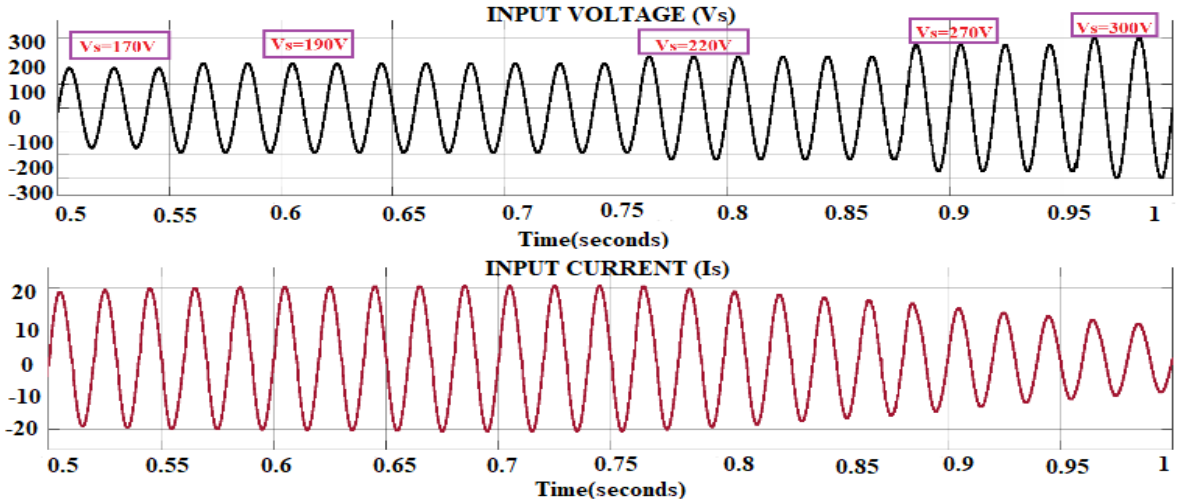
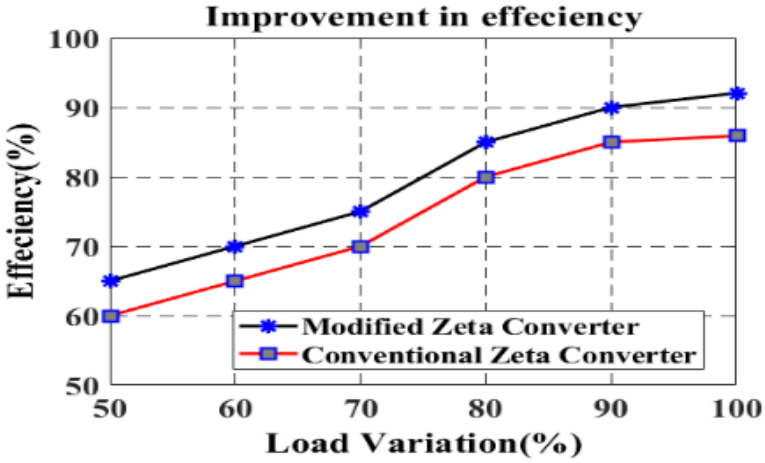
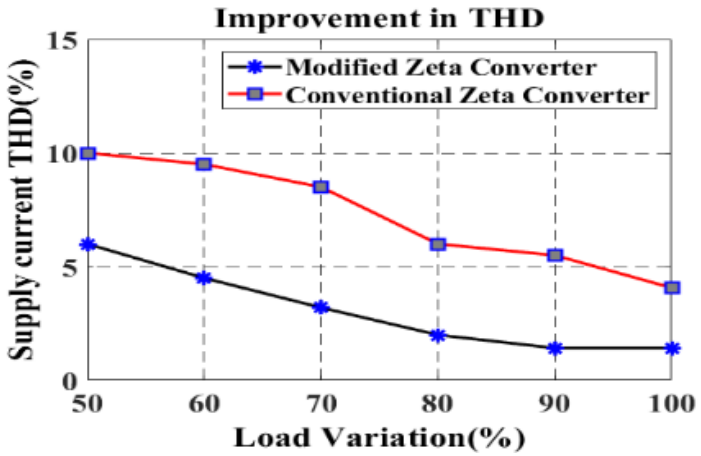


Fig. 5.31 Waveform of voltage (V) and current (I) over different supply voltage (Vs)

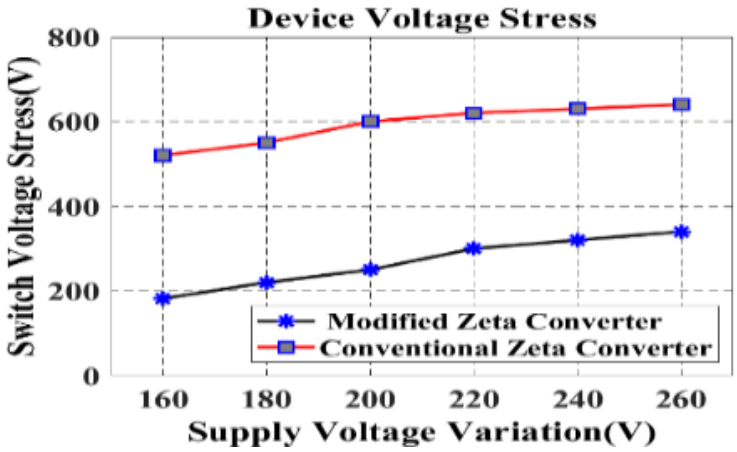
5.3.3 Comparison of Modified Zeta with Conventional Zeta Converter



(a) Efficiency (η)



(b) Total Harmonic Distortion



(c) Voltage Stress across device

Fig. 5.32 Comparison in (a) Efficiency (η), (b) Total Harmonic Distortion, (c) Voltage Stress across device of Modified Zeta Converter and Conventional Zeta Converter

In this section, the comparison of efficiency (η), THD and device voltage stress are discussed and is shown in Fig 5.32 (a)-(c). From Fig 5.32 (a), it is clear that the full load efficiency of this charger is 92.5% which shows a hike of 3-4% in comparison with the conventional zeta converter-based EV charger.

From Fig 5.29-5.30 and Fig 5.32 (b), the improvement in THD can be seen, it shows that the THD of Modified zeta converter is 1.88% which yields a power factor of 0.98 whereas the THD of conventional zeta converter is 4.03% which gives a power factor of 0.92. In Fig 5.32 (c), the improvement in device voltage stress can be seen. The modified zeta converter shows lesser device voltage stress in comparison with conventional zeta converter-based EV charger as shown in Table VII.

In conventional charger, the device voltage stress is the addition of input voltage (V_{in}) and the DC-Link voltage(V_{dc}). So, for a conventional converter the voltage stress is:

$$V_{s1,s2} = V_{in} + V_{dc} \qquad (5.3)$$

But voltage stress of Modified zeta converter-based EV charger is:

$$V_{s1} = V_{s2} = V_{in} \qquad (5.4)$$

which is quite low as compared to conventional counterpart, which is because of the use of the clamping diodes D_1, D_2. In Fig 5.32 (c), at input voltage of 220V, the device voltage stress is approx. 250V for Modified EV charger whereas 610V for conventional EV charger. Table VII shows the comparison of conventional ad modified zeta converter based EV charger.

TABLE VII. COMPARISION OF CONVENTIONAL AND MODIFIED ZETA CONVERTER BASED EV CHARGER

Parameters	Conventional Zeta Converter based EV charger	Modified Zeta Converter based EV charger
Power Factor	0.92	0.98
Efficiency (%)	89%	92.5%
THD (%)	4.02%	1.88%
3^{rd} Harmonic Component (%)	4.5%	2.03%
Device Voltage Stress (V)	610V	250V

5.4 Conclusion

In this chapters the results of SI-SEPIC converter cascaded with Flyback converter were shown and the charger is compared for two different controller topologies i.e., PWM and SPWM controller topology. SPWM controller provides better performance by improving the power factor, reducing the THD and 3rd order current harmonic and thereby improves the overall efficiency of the EV Charger. Also, the results of Modified Zeta Converter fed with HB-LLC Resonant converter were discussed. A comparison is done between conventional and Modified Zeta Converter which showed that modified Zeta converter improves the efficiency of the charger and voltage stress across the device is reduced to half in case of Modified Zeta converter.

CHAPTER 6
CONCLUSION AND FUTURE SCOPE

6.1 Conclusion

In this work various DC-DC Converters are discussed which are used for power factor correction of the EV Charger and thereby improving the THD of the input current, increasing the efficiency of the chargers and reducing the voltage stress. The work is basically divided into two sections where two different EV Chargers are designed and implemented in MATLAB environment.

Initially, the literature review is carried out to analyse all the different DC-DC converters which are used for providing power factor correction along with their advantages and disadvantages. Among all the converters, SEPIC converter provides the advantage of less input current ripple and provide better efficiency at low level of input voltage. Also, the switch voltage stress is less in SEPIC converters. Zeta converter provides better dynamic response in discontinuous conduction mode (DCM). It also improves the voltage regulation and lowers the ripple in output current.

- The first work includes the cascaded SI-SEPIC and flyback converter which is designed for EV application. Due to SI-SEPIC configuration at the input, high voltage gain is achieved as compared to conventional SEPIC converter.
- It also operates at reduced duty ratio to achieve an output voltage of 300V. This leads to low THD as per IEC standard, and thereby improving the PF (Power Factor) and efficiency of the converter.
- Two control techniques i.e. PWM and SPWM controller techniques are designed for the adequate performance of the converter and the obtained results are compared.
- SPWM controller provides better performance by improving the power factor, reducing the THD and 3^{rd} order current harmonic and thereby improves the overall efficiency of the EV Charger.
- As a way forward the proposed converter can be used for multiple battery rating, variable load and can be used with different sort of motor used in EV application.

- The SEPIC Converter has a disadvantage of having more ripple in the output current. So, modified Zeta converter was introduced which provides better dynamic response in DCM and it also provides less ripple in the output current.
- The second work includes a Modified Zeta Converter fed HB-LLC Resonant converter-based EV charger with reduced device voltage stress, improved efficiency and lower THD. The reduction in voltage stress is achieved by adding clamping diodes (D_5, D_6) at the input of conventional zeta converter without adding extra inductor and capacitor.
- The design parameters of Modified zeta converter and HB-LLC Resonant converter are also discussed. Also, the conventional and Modified zeta converter-based EV charger are compared in the last section.
- A comparison is done between conventional and Modified Zeta Converter which showed that modified Zeta converter improves the efficiency of the charger and voltage stress across the device is reduced to half in case of Modified Zeta converter.
- As a way forward, the design parameters and techniques discussed in this work can be used for experimental model.

6.2 Future Scope

This work basically comprises of two EV Chargers for power factor correction (PFC).

- First charger consists of high-gain SI-SEPIC Converter which works at reduced duty ratio (D) and thereby increases the efficiency of converter.
- Using the design parameters and techniques used in this work, the hardware implementation of this work can be done.
- As a way forward the proposed converter can be used for multiple battery rating, variable load and can be used with different sort of motor used in EV application.
- But due to the greater number of components present in this work, the cost and the size of the converter increases, in that field some research is needed to be done.
- Also, the SI-SEPIC Converter has a disadvantage of having more ripple in the output current, so modified Zeta converter-based EV charger is designed which provides better dynamic response in DCM (Discontinuous Conduction Mode) and provides less ripple in the output current.
- The second work includes a Modified Zeta Converter fed HB-LLC Resonant converter-based EV charger with reduced device voltage stress, improved efficiency and lower THD.
- The reduction in voltage stress is achieved by adding clamping diodes (D_5, D_6) at the input of conventional zeta converter without adding extra inductor and capacitor.
- Using the design parameters and techniques used in this work, the hardware implementation of this work can be done.
- As a way forward the proposed converter can be used for multiple battery rating, variable load and can be used with different sort of motor used in EV application.

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PUBLICATIONS

The work has been accepted and presented into the following publications:

1.	**Title of the Paper:**	**PFC of SI-SEPIC and Flyback Converter for EV Applications**
	Author names:	[1]Rishita Shukla and [2]Mr. Krishna Dutt
	Name of Conference:	7th International Conference for Convergence in Technology (I2CT)
	Name of Organizer:	Global Institute of Business Management & Decision Sciences (GIBDS), Pune, India IEEE Bombay Section
	Conference Date with Venue:	April 7th – April 9th, 2022 Virtual Mode
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2.	**Title of the Paper:**	**A Modified Zeta Converter Fed with HB-LLC Resonant Converter for Power Factor Correction**
	Author names:	[1]Rishita Shukla and [2]Mr. Krishna Dutt
	Name of Conference:	IEEE Region 10 Symposium (TENSYMP)
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APPENDIX I

A. IEC Standard 61000-3-2

EC 61000-3-2 Electromagnetic compatibility (EMC) – Part 3-2: Limits – Limits for harmonic current emissions (equipment input current ≤ 16 A per phase) is an international standard that limits mains voltage distortion by prescribing the maximum value for harmonic currents from the second harmonic up to and including the 40th harmonic current. IEC 61000-3-2 applies to equipment with a rated current up to 16 A.

Table 1. IEC 61000-3-2 Current harmonic limits

Harmonics [n]	Class-A [A]	Class-B [A]	Class-C [%]	Class-D [mA/W]
Odd Harmonics				
3	2.3	3.45	30xλ*	3.4
5	1.14	1.71	10	1.9
7	0.77	1.155	7	1.0
9	0.40	0.60	5	0.5
11	0.33	0.495	3	0.35
13	0.21	0.315	3	3.85/13
15≤n≤39	0.15*15/n	0.225x15/n	3	3.85/n
Even Harmonics				
2	1.08	1.62	2	-
4	0.43	0.645	-	-
6	0.30	0.45	-	-
8≤n≤40	0.23*8/n	0.345*8/n	-	-

***λ** is the circuit power factor

B. IEC Standard 519

The IEEE 519-2014 standard defines the voltage and current harmonics distortion criteria for the design of electrical systems. Goals for designing electrical systems that contain both linear and non-linear loads are established in this standard.

Important terminologies related to IEC Standard 519 are listed below:

- **Maximum demand load current:** This current value is enacted at the point of common coupling (PCC) and calculates as the average of the currents corresponding to the peak demand during the previous 12 months.
- **Notch:** A condition, lasting less than ½ cycle, in which the magnitude of the voltage waveform reversed its normal polarity.
- **Point of common coupling (PCC):** the point on a public power supply system, electrically closest to a specific load, in which other loads are, or maybe connected. The PCC is a point located upstream of the regarded installation.
- **Short-circuit ratio:** in a specific location, the rate of the available short-circuit current, to the load current, in amperes.
- **Total demand distortion (TDD):** The ratio of the root mean square of the harmonic content, including the harmonic components up-to the 50th order. Expressed as a percent of the maximum demand current. Inter-harmonics are specifically excluded. Higher frequencies (harmonics greater than 50) may be added when required.
- **Total harmonic distortion (THD):** The ratio of the root mean square of the harmonic content, including the harmonic components, up-to the 50th order. Expressed as a percent of the fundamental. Inter-harmonics are specifically excluded. Higher frequencies (harmonics greater than 50) may be added when required.

Voltage distortion limits

Table 2 (IEEE 519)

	Weekly 95th percentile short time		Daily 99th percentile short time	
Bus voltage V at PCC	Individual harmonic (%)	THD (%)	Individual harmonic (%)	THD (%)
$V \leq 1.0$ kV	5.0	8.0	7.5	12
1 kV < V ≤ 69 kV	3.0	5.0	4.5	7.5
69 kV < V ≤ 161 kV	1.5	2.5	2.25	3.75

Current Distortion Limits

Table 3 (IEEE 519)
Current distortion limits for systems rated 120 V – 69 kV

I_{SC}/I_L	**Individual harmonic limits (Odd harmonics) [a,b]** **Harmonics values are in % of maximum demand load current**					**TDD**
	3 ≤ h < 11	11 ≤ h < 17	17 ≤ h < 23	23 ≤ h < 35	35 ≤ h ≤ 50	
<20c	4.0	2.0	1.5	0.6	0.3	5.0
20<50	7.0	3.5	2.5	1.0	0.5	8.0
50<100	10.0	4.5	4.0	1.5	0.7	12.0
100<1000	12.0	5.5	5.0	2.0	1.0	15.0
>1000	15.0	7.0	6.0	2.5	1.4	20.0

Table 4 (IEEE 519)

Current distortion limits for systems rated 69 kV – 161 kV

I_{SC}/I_L	Individual harmonic limits (Odd harmonics) [a,b] Harmonics values are in % of maximum demand load current					TDD
	3 ≤ h < 11	11 ≤ h < 17	11 ≤ h < 17	23 ≤ h < 35	35 ≤ h ≤ 50	
<20[c]	2.0	1.0	0.75	0.3	0.15	2.5
20<50	3.5	1.75	1.25	0.5	0.25	4.0
50<100	5.0	2.25	2.0	0.75	0.35	6.0
100<1000	6.0	2.75	2.5	1.0	0.5	7.5
>1000	7.5	3.5	3.0	1.25	0.7	10.0

- Daily 99th percentile very short time (3 s) harmonic currents should be less than 2.0 times the values given in the tables below.
- Weekly 99th percentile short time (10 min) harmonic currents should be less than 1.5 times the values given in tables below.
- Weekly 95th percentile short time (10 min) harmonic currents should be less than the values given in tables below.

Table 4 (IEEE 519-2014)

Current distortion limits for systems rated > 161 kV[a]

I_{SC}/I_L	Individual harmonic limits (Odd harmonics) [a,b] Harmonics values are in % of maximum demand load current					TDD
	3 ≤ h < 11	11 ≤ h < 17	17 ≤ h < 23	23 ≤ h < 35	23 ≤ h ≤ 50	
<25[c]	1.0	0.5	0.38	0.15	0.1	1.5
20<50	2.0	1.0	0.75	0.3	0.15	2.5
≥50	3.0	1.5	1.15	0.45	0.22	3.75

- [a] Even harmonics are limited to 25% of the odd harmonic limits above
- [b] Current distortions that result in a dc offset, e.g., half-wave converters, are not allowed
- [c] All power generation equipment is limited to these vales of current distortion, regardless of actual I_{SC}/I_L
- I_{SC} = maximum short circuit current at PCC
- I_L = maximum demand load current (fundamental frequency component) at PCC

C. Understanding Power Factor (PF), Displacement Power Factor (DPF) and Crest Factor (CCF)

Power factor is the ratio of true power to apparent power in a circuit or distribution system. Any AC circuit consists of real, reactive, harmonic, and apparent (total) power. True power is the power, in W or kW, used by motors, lights, and other devices to produce useful work. Reactive power is the power, in VAR or kVAR, stored and released by inductors and capacitors. Reactive power shows up as a phase displacement between the current and voltage waveforms. Harmonic power is power, in VA or kVA, lost to harmonic distortion. Apparent power is the power, in VA or kVA, that is the vector sum of true power, reactive power, and harmonic power. Apparent power is not a simple summation but a vector summation.

The displacement power factor is the ratio of true power to apparent power due to the phase displacement between the current and voltage. Capacitors can usually be added to a circuit or distribution system to correct the displacement power factor. The displacement power factor is calculated as follows:

$$PF = \cos(\emptyset) \qquad (A.1)$$

Where,

PF = displacement power factor

$\emptyset$ = Difference between the phase of the voltage and the phase of the current (phase displacement) in degrees.

The distortion power factor is the ratio of true power to apparent power due to THD. Capacitors cannot be added to a circuit to compensate for the distortion power factor. The impedance of capacitors decreases with frequency. Therefore, a capacitor can become a sink for high-frequency harmonics. Special types of transformers or tuned harmonic filters consisting of capacitors and inductors are used to correct distortion power factor. The distortion power factor is calculated as follows:

$$PF_{THD} = \sqrt{\frac{1}{1 + THD^2}} \qquad (A.2)$$

where,

PF_{THD}= distortion power factor

THD = total harmonic distortion

The total power factor is the product of the displacement power factor and the

distortion power factor and is calculated as follows:

$$PF_{Tot} = PF * PF_{THD} \qquad (A.3)$$

where,

PF_{Tot} = total power factor

PF = displacement power factor

PF_{THD} = distortion power factor

The current crest factor is the peak value of a waveform divided by the rms value of the waveform. The purpose of a current crest factor is to give an idea of how much distortion is occurring in a waveform. The current crest factor is calculated as follows:

$$CCF = \frac{I_{peak}}{I_{rms}} \qquad (A.4)$$

where

CCF = current crest factor

I_{peak} = peak value of current (in A)

I_{rms}= root mean square value of current (in A)