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INVESTIGATION OF BRIDGELESS PFC CONVERTER

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I, Prathmesh Tandon, 2K20/PES/15, student of M.Tech Power Electronics and Systems, hereby declare that the project dissertation title "Investigation on Bridgeless PFC" which is submitted by me to the department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled “Investigation on Bridgeless PFC Converter” which is submitted by Prathmesh Tandon, 2K20/PES/15, Department of Electrical Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carrier out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date:

PROF. Vishal Verma

PROFESSOR

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ABSTRACT

This Project brings forward the design and modeling of buck-boost common ground bridgeless power factor corrector worthy enough to use in application which requires to deriving a *DC* power from *AC* power. The introduction of common ground between input and output side of the *AC-DC* converter wipes out *EMI* issues along with the reduction of undesired output voltage ripples. It converts the grid ac voltage into a wide range of voltage output all happening in a single-stage circuit. Since it is in a bridgeless structure so it is simple in design. Detailed study about power factor correction followed by its different approaches has documented. Bridgeless topologies are gaining a lot of attention, therefore different types are discussed. High power factor, low *THD*, desired constant output voltage are also achieved. The proposed topology is closed loop controlled via hysteresis controller. The proposed buck-boost topology is compared with the simulation of bridgeless boost PFC converter. The design and modeling of both converters is done on the MATLAB-simulation. Experimental results of modified buck-boost converter are presented for a 1.75 kW, operating from 220 V_{rms} input to 96 V_{dc} output. The modified buck-boost *PFC* result exhibits the potential for step-down ac to dc conversion with a significant efficiency respectively suitable to charge a 96V/15A EV battery.

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LIST OF ABBREVIATIONS

AC	Alternating Current
CCM	Continuous Conduction Mode
DC	Direct Current
DBR	Diode Bridge Rectifier
DCM	Discontinuous Conduction Mode
DF	Distortion Factor
DPF	Displacement Power Factor
DSP	Digital Signal Processor
EMI	Electromagnetic Interference
HF	High Frequency
HFT	High Frequency Transformer
HVDC	High Voltage Direct Current
IGBT	Insulated Gate Bipolar Transistor
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
MOSMPS	Multiple Output Switched Mode Power Supply
PC	Personal Computer
PF	Power Factor
PFC	Power Factor Correction
PI	Proportional Integral
PID	Proportional Integral and Derivative
PQ	Power Quality
PWM	Pulse Width Modulation

RMS	Root Mean Square
SMPS	Switched Mode Power Supply
THD	Total Harmonic Distortion
UPS	Uninterruptible Power Supply
BL	Bridgeless

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Power supplies can transform one type of power to another with a different variety of attributes in order to meet goals. The prominent feature of power supply is the conversion of uncontrolled input power into regulated voltage/current for the electrical equipment functioning. During power conversion process, reduced power loss, higher efficiency, compact size, and cheap cost are all important elements to consider. AC to DC conversion is commonly used in power utilities, where their principal function is to convert high alternating current voltage to low direct current voltage, such as in battery charger systems, LED drivers, dc motor drivers, and other similar industrial and domestic applications. Because of its varied collection of power uses, power factor correction (PFC) is an unavoidable requirement to minimize grid voltage harmonics [1]. Two-stage design is adopted in grid connected power converter to offer power conversion in between low voltage DC at input and sinusoidal AC at output. The dual-stage configuration is simple and widely used, with the front-end rectifier correcting the power factor and the rear end dc to dc converter stepping down the rectified voltage to the low output voltage. Furthermore, after the rectifier stage, dc-dc converter is used to align the AC current and maintain constant DC with minimum ripple [2]. Switch Mode Power Supply (SMPS) without an active Power Factor Correction (PFC) circuit, on the other hand, due to the diode bridge configuration and capacitor at the front end, the load is quasi. As a result, the diode bridge gives significant distortion of source current coming from AC supply raising Total Harmonic Distortion while lowering power factor, dissipation factor, and displacement power factor. Due to the conventional diode bridge configuration, the system experiences high conduction losses resulting in the restriction of overall efficiency thereby generating unusual power losses. In addition, the discontinuous current in the input induces harmonic issues in the grid and induces different mode noises in the system [3]. Consequently, a bulky input filter is required as a supplement. Therefore, to restrict the amount of current distortion allowed into it, the utility imposes specific norms and rules. IEC/61000/3 is a protocol limiting harmonic contents produce by rectifier. It is recommended that the rectifier with modest power ratings receive sinusoidal current from the input AC mains that copies exactly the AC voltage. The diode bridge formation has indeed a lot of constrain, therefore various bridgeless topologies have been introduced with low THD and high efficiency. Bridgeless topology helps in reduction of the number of components when comparing to the diode bridge topology and is more efficient, have smaller size, and maintain good quality [4]. Nevertheless, dc-dc converters are integrated with the bridgeless configuration to design a modified bridgeless PFC converter with different topologies discussed in the third chapter of the project. The numbers of semiconductors are less but a

high rectified buck-boost current is required when relating with the single-stage topology that leads to the high conduction loss [3]. Possible researches are going on improving power quality converters to alleviate power quality issues, increase efficiency, and reducing the number of components to make it more economical. To obtain a substantial improvement in power quality, PFC circuits are connected with the SMPS [13]. Even with variable input voltage and load circumstances, PFC circuits achieve high PF and low THD input currents.

1.2 MATLAB/Simulink

MATLAB stands for Matrix Laboratory, and it is a computer programming language. MATLAB was developed to put things easy by using the LINPACK (linear system package) and EISPACK (Eigen system package) projects' matrix software. MATLAB is a high-performance technical computing language. It incorporates arithmetic, graphics, and a programming environment into one application. Furthermore, MATLAB (Fig.1.1) is a splitting programming environment. The software programmer has been a staple tool at most institutions and businesses throughout the world since its original release in 1984. It has a set of reliable built-in algorithms that enable a wide variety of computations. It also supports basic graphics instructions for quickly displaying findings. The tools are organized into toolbox packages. Toolboxes are used in signal processing, symbolic computation, control theory, simulation, optimization, and a variety of other applied scientific and engineering areas.

Simulink is a graphical extension of MATLAB that enables user to model and simulate systems. Simulink presents systems as block diagrams on the screen shown in Fig.1.2. Many block diagram elements, like as transfer functions, summing junctions, and virtual input and output devices including function generators andoscilloscopes, are available which is shown in Fig.1.3. These virtual devices will allow users to simulate the models you'll be creating. Simulink and MATLAB are tightly connected, and data may be easily shared between the both. We can use Simulink to apply to examples of modeled systems, then design controllers and simulate the systems.

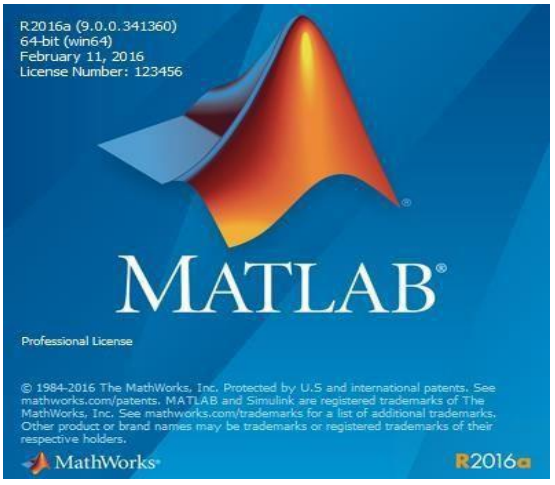


Fig.1.1 MATLAB software

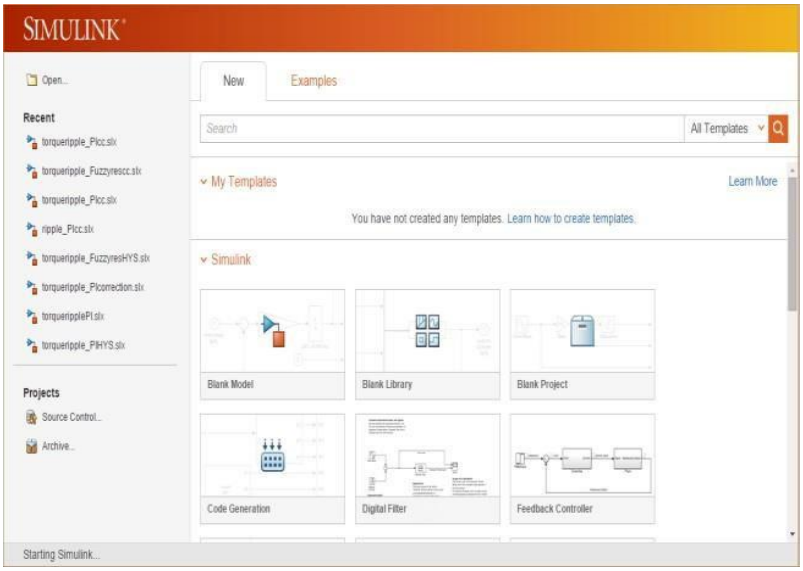
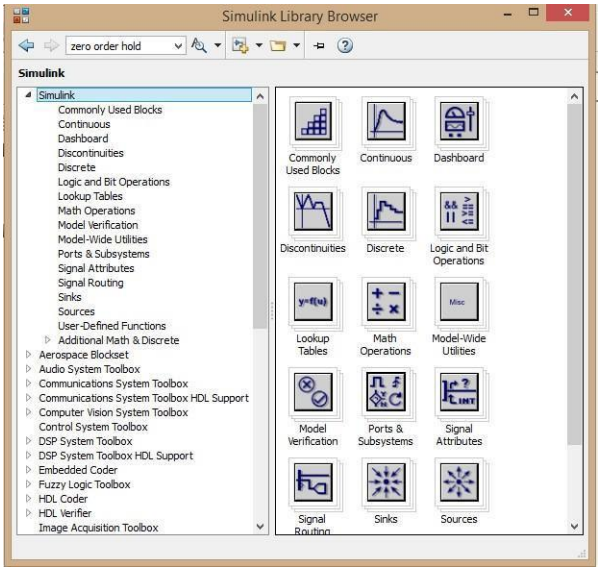


Fig. 1.2 Simulation page for implementation



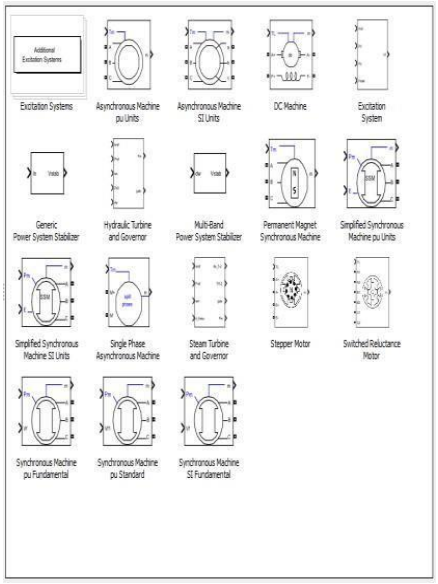


Fig.1.3 Simulink toolbox

1.3 MOTIVATION

These days the switch mode power supply (SMPS) is getting compatible with single or three phase ac source supply for devices like electronic equipment, PCs, mobile phones, and other similar

uses. At the front end of most of these power supplies are AC/DC converters. Earlier diode bridge rectifiers were used in ac to dc conversions. Even though it consists of non linear features, these rectifiers create large harmonics and low power factor that result to poor power quality in the system. The objective is to provide a good quality of sinusoidal input current. It should be unaffected by any load variations, input or output voltage, highly efficient with considerable power density capable of meeting with the international protocols. Therefore, the demand for high switching converter is increasing exponentially. it aids in the reduction of converter size but at a cost of impacting efficiency and generating switching losses. Active PFC converters with appropriate controllers can be used at the SMPS's front end to overcome such issues. The usage of soft switching is another promising way to reduce switching losses. In terms of control approach, even a simple current mode control with proper switching logic as giving pulse to the gate signal alternatively in every cycle could lead to the improvement in THD. The electromagnetic interference issue is one of the grey areas to be looked upon. Different topologies can be implemented on front end as well as back end of active PFC to see for the improvements. Hence, there is a lot of scope in an advancement of PFC for industrial and residential purposes. Reviewing the performance measures is the key area of the motivation for this thesis.

1.4 OBJECTIVES

The following are the research objectives of this project:

(1) To study about various converter designs that have a capability to enhance the power quality by improving THD at input side, produce regulated voltage output and maintain a unity power factor.
(2) To implement the intended converter architecture in order to avoid common mode electromagnetic interference.
(3) To evaluate the capability of the common ground bridgeless PFC against conventional bridgeless PFC.
(4) To review the performance benchmark of different bridgeless topology based PFC’s.

(5) To analyze current control method and implementation of it respectively.

1.5 ORGANISATION OF THESIS

1. The notion of power converters for SMPS applications which requires mandatory PFC circuit for low THD and improved power factor is introduced in **Chapter 1**.

2 **Chapter 2** completes the literature assessment as well as the problem's foundation following that, the thesis' aims and outline are outlined.

3 In **Chapter 3**, the topology of the various bridgeless PFC taken into consideration. This chapter delves into the system setup, and performance of the proposed two-stage converters.

4 In **Chapter 4**, the common ground bridgeless PFC controller along with different current control strategy is discussed

5 In **Chapter 5**, In this section the working principle, design consideration of passive elements, and development of modified bridgeless is compared. Common ground bridgeless formation is presented.

6 Conclusions are drawn in **Chapter 6** based on the opinions and findings of the study project. This chapter also suggests some future research directions in the field of improvisation of switching cycle.

CHAPTER 2

Literature Review

2.1 INTRODUCTION

Lots of devices such as phones, laptop, and similar electronics appliances still operate on traditional uncontrolled rectifiers, which draw distortion, are causing issues in the system.

As a result, device system's performance suffers, and the rated capacity of device is wasted. There are two basic approaches to attain PFC that is categorized as passive PFC and Active PFC. although, passive filters are cheaper and highly efficient but it includes large and heavy filter components that are not easy to operate in closed loop system. On the other hand, active power factor correction is of two types: single stage and two stage. As the name suggest, in two stage PFC, two converters are employed, where the role of the second converter is to match the input current at the front end for such a scenario, two different controllers are regulated to improve the output voltage and input current waveforms. Active power factor correction gives high power factor, reduced harmonic contents, and regulated dc back-end design. Hence, this approach is used but at a slightly high costing because of extra switching and controller involved. The benefits of a single stage system are economical and compatible size which is the opposite of a two stage. The active single stage power factor correction is an amalgamation of front end and back end. The front end consists of ac to dc conversion, while back end consists of dc-dc conversion. There is a capacitor present in between both the ends that stores the energy and discharges according to the harmonic content of the input current. The history of *PFC* was brought out to the market by Texas Instruments *(TI)* in 1980's made a huge contribution by developing different PFC techniques. Indeed, it is still leading the market trend wise as well as innovation wise [16-17]. Average Current Mode Control is a *PFC* converter idea that has been frequently used. All other conventional approaches, such as peak-current-mode control [21], were superseded by the *ACMC.* They were the main creators and makers of *PFC* converter control integrated circuits. The active PFC control technique may be used in *SMPSs* with a variety of topologies that is discussed in chapter 3. Power flow may be configured in either a unidirectional or bidirectional manner for all converter topologies. Because of its rapid switching speed and low conduction losses, the Metal Oxide Semiconductor Field Effect Transistor *(MOSFET)* is favored over other switching devices in low-power applications. IGBTs, on the other hand, are recommended in high and medium power applications and can operate at a switching frequency of around 30 kHz. *PFC*

converter control relies heavily on digital signal processors [19-20]. The input current is made to follow the reference value via the hysteresis controller. The ACMC performs better, but the controller design is more difficult. Sliding mode control is known for its robustness and tracking mechanism. It is gaining a lot of attention also. However, the hysteresis controller has been implemented discussed and simulated respectively.

2.1 Power factor correction (PFC)

The power factor (PF) indicates the performance of the load of using the power from utility grid. The following relationship explains it:

$$PF = \frac{Pav}{Vrms.Irms} = k_{distortion}.k_{displacement} \quad (1.1)$$

As in the equation 1.1, P_{av} is the average power getting divided by the RMS value of current and voltage accordingly. Power factor is also the product of distortion and displacement factor respectively. The closer its value to unity is the better the system efficiency would be.

$$k_{distortion} = \frac{1}{\sqrt{1+(THD)^2}} \quad (1.2)$$

THD: Total Harmonic Distortion

The power factor has a value between 0 and 1. Line current harmonics connected to the utility mains are regulated by international regulations.

2.2.1 PASSIVE - ACTIVE PFC

The importance of *PFC* is rising because a greater number of power semiconductor devices are finding inquisitive ways to couple with the grid. The interlink of *PFC* with *SMPS* is an emerging state in terms of designing and meeting the needs. The *PFC* can be achieved via two different ways either active or through passive. In case of passive PFC, the use of passive elements such as *LC* filter is employed to reduce the harmonic of input current. It is installed just after the AC source and right behind the bridge rectifier, as shown in Fig.2.1. This kind of *PFC* is use in case of low power application by keeping the value of inductor and capacitor relatively small while maintaining the power factor to 0.9 or less. The good side of this approach is its simple design, economical, stability, and lack of unwanted electromagnetic interference [24-25]. Since only one *LC* filter is sufficient to suppress a single harmonic frequency, so in case of removing large number of harmonics, passive power factor correction becomes unduly huge and expensive.

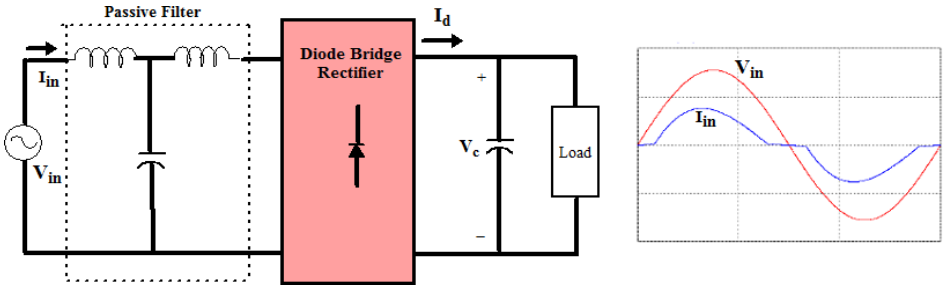


Fig.2.1 Passive PFC with input waveform

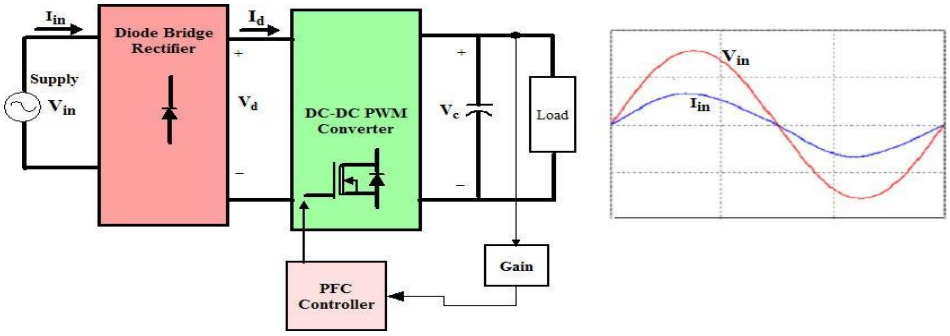


Fig.2.2 Active PFC with input waveform

Because of the better performance and small size, active PFC has gotten a lot of interest. In active power factor correction, the input current should be ideally sinusoidal and in phase with the input AC voltage by putting a DC-DC converter in the complete circuit and operating it at high frequency. Figure 2.2 depicts the active PFC technique's block diagram. Buck-Boost, SEPIC and CUK are the most frequent DC-DC converter designs in active PFC [26-29]. A power factor close to unity may be produced with this PFC approach, and the AC-DC converter imitates a pure resistor [29]. In the SMPS, a boost converter arrangement is typically selected as a PFC pre regulator [25]. Active PFC has several advantages over passive PFC, including less size and weight, lower harmonics, and a higher power factor. As a result, the focus of the research is more on the side of active PFC converters utilized in SMPS.

2.2.2 Single Stage Active PFC

As the use of AC-DC converters grows, researchers are focusing on developing single-stage converters that alleviate PQ issues, enhance efficiency, and lower the total cost of the system by employing fewer components. Figure 2.3 shows a block schematic of the single-stage active PFC approach. Single stage active PFC is an acceptable choice especially for

light load condition to deal with low frequency harmonics. There is only one control loop,

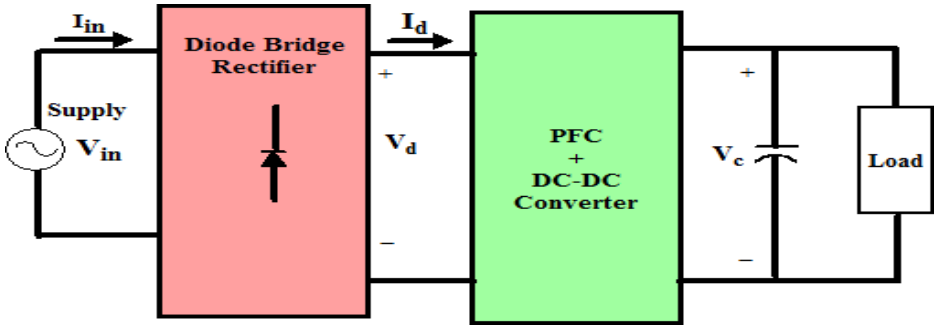


Fig.2.3. Single- stage active PFC

and the energy is only handled once. Because of its easy design and inexpensive cost, it is ideal for low-power applications [20-21]. An input EMI filter filters the AC supply before it reaches the diode bridge rectifier. With the assistance of an EMI filter, the line current becomes ripples free and virtually sinusoidal. A single-stage PFC is effective at low power levels and costs less.

2.2.3 Two- stage active PFC

The electrical components of a single- stage SMPS are put under a lot of stress. The output side capacitors employed to reduce second harmonic content are extremely large.

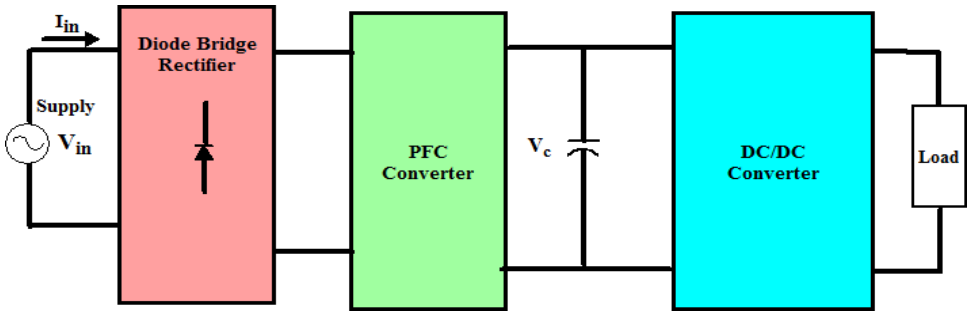


Fig.2.4. Dual-stage active PFC

A two-stage PFC system is preferred to alleviate these limitations. Fig.2.4 shows a block schematic of the two-stage active PFC approach. A PFC stage and a DC-DC conversion stage are included [32-33]. The PFC step transforms the utility line voltage to a high-power factor constant DC voltage. The corrected output of the DBR feeds this initial

stage, which aids in PFC. Using a separate control, the DC-DC conversion transforms the constant voltage to a specified value with precise output voltage regulation. For the mentioned purposes, the double stage PFC approach is best suited for high power applications: The sinusoidal source current obtained from the grid meets power quality criteria, two stages can be ideally constructed since they work separately, amount of time a power supply is able to maintain the output at regular voltage levels may be simply calculated, and a common line voltage can be used. Due to the fact that power is handled twice, two-stage PFC has a low efficiency [34-35].

2.3 Review of BL-PFC Converter

Buck-Boost, CUK, and SEPIC Converters are used to design an efficient PFC converter with less number of semiconductor switches [35, 36]. Boost and Flyback Converters are the most self-PFC capable of these converters. Boost Converters are the best choice for power factor correction because Flyback Converters require high frequency transformers. However, due to the conventional diode bridge configuration, the system experiences high conduction losses resulting in the restriction of overall efficiency thereby generating unusual power losses. Therefore, different bridgeless PFC topologies have arrived. Firstly, Bridgeless PFC rectifiers reduce the number of power semiconductor devices are much efficient in terms of performance, size, quality [4]. The numbers of semiconductors are less but a high rectified buck-boost current is required when relating with the single-stage topology that leads to the high conduction loss [3]. There have been various single stage topologies derived from SEPIC, CUK, converters that are further extracted from buck-boost converter thereby are feasible to operate in step-up and step-down voltage making a PFC converter more suitable for flexible dc output voltages but there are wide areas that can be improvised. The number of sensors, components and balancing of control can be rectified. Furthermore, discontinuous current requires an additional input filter-making these topologies fixed for certain applications only. The active switching of PFC circuits leads to common mode electromagnetic interference (EMI). To overcome this, EMI filters are required that trouble the system efficiency,

generate unnecessary ripples, and increase the overall cost of the system [7]. The common-mode noise or common-mode current ($i_{cm)}$ begins from noise coupling through the parasitic capacitor. Normally, the switching voltage can be reduced by reducing the size and bandwidth to minimize common-mode noise. The negative output of a traditional boost PFC converter is always connected to the input side through the presence of diode in the bridge rectifier, resulting in common-mode noise in the input lines. This does not occur in active clamped bridgeless PFC rectifiers in [10], [11], which contribute to a high value of common-mode noise and thus necessitate a bulky filter. To improve EMI performance, four distinct ways are illustrated in fig 2.5 for maintaining the grid voltage to the output of the bridgeless rectifiers DC to improve EMI performance. Conclusively, in all different approaches the capacitor filter, split C circuit method, and inductor filter have been emphasized and modified accordingly to improve the magnitude and frequency of switching voltage ripple although these lead to a decrease in performance in terms of phase current and weaken the quality of dc voltage which is not a good compensation for the reduction of dv/dt by filters [12], [13]. After retrospection of all these variants, it is evident that the existing structures of buck-boost bridgeless PFC converter, the mitigation of EMI common-mode noise with the low number of components and less conduction path are still the improvisation area.

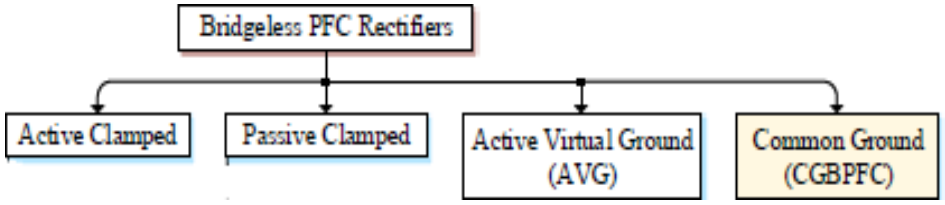


Fig.2.5 Different types to achieve bridgeless topology

The circuit proposed in this project offers such improvements. The direct connection between ac supplies to the negative terminal of dc output is the most pick out way to mitigate EMI common-mode noise and reduce the output dc voltage ripples. In addition,

the continuous current is getting achieved which removes the need for bulky filters and avoid the use of MOSFETs body diode conduction in continuous conduction mode as well as reverse recovery power losses of body diodes making an overall circuit simple and effective.

2.4 Common Mode Noise Analysis

Active switching PFC circuit design often leads to the generation of electromagnetic interference. The current arises because of the presence of capacitor as shown in fig 2.6 circulates between the switching part of the circuit and ground. This unreservedness can be eliminated by minimizing the frequency and magnitude of the switching side voltage ripple or $\frac{dv}{dt}$ changes. So, these types of converters suffer from high common mode noise on the input lines. Due to this reason, larger filter is required. As shown in fig 2.5 different types of approaches can be used to clamp the ac to the dc side. It can help to improve EMI performance. Consecutively, for the passive clamped [9],[11] and active virtual ground [16],[17] the magnitude and frequency of voltage switching ripple is getting reduced through the capacitive filter. The converter in [17] uses a split C method to avoid the short circuit possibility on the grid side. In order to minimize the high effect of Dv/D_t changes from the converter, isolation transformers and large sized filters such as Y-capacitor or common mode chokes are widely used [19]. These methods are costly, bulky, and may invite inrush current in the circuit. Moreover, they cannot completely eliminate the voltage switching ripples.

According to this review, it can be inferred that the elimination of common mode noise completely with low component count in conduction path, reduced size, and cost effective is bit challenging. The circuit proposed in this project where there is a provision of common ground is provided in dual stage active bridgeless PFC. This converter offers the mitigation of common mode noise along with less component count and improved efficiency. The best part is that there is no additional filter is added to combat the stated issue. The detailed analysis is presented in other chapters.

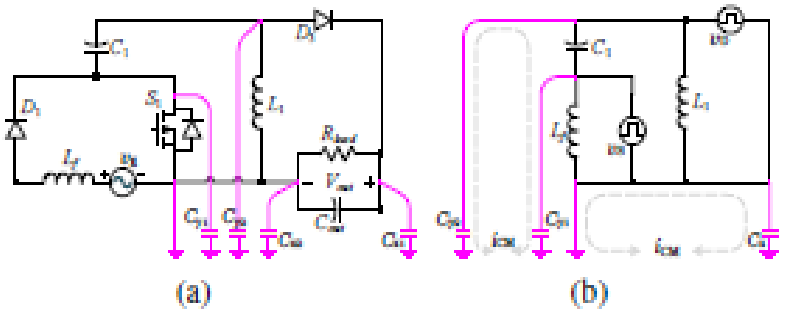


Fig 2.6 (a) Pink line depicting parasitic capacitors, (b) high frequency circuit.

In fig 2.6(a), the parasitic capacitor is shown as C_{x1} and C_{x2} are formed between the positive dc bus and the ground, negative dc bus and ground respectively. Cy_1 is the parasitic capacitor between the drain of the MOSFET and ground, C_{y2} is the parasitic capacitor between the anode of the diode and ground. The technique in [13], shows the high frequency equivalent circuit that can be formed by taking the ac source and the dc bus as short circuited, and the switching MOSFET and diodes as sources with voltages V_s and V_D. The grey dashed line is the common mode noise current path in fig 2.6(b) as C_x (sum of x_1 and x_2), C_{y1} and $C_{y2.}$ The common mode noise voltage appears in $C_{x,}$ C_{y1}, and $C_{y2.}$ Conclusively, C_x is short circuited and therefore the D_v/D_t across C_x is totally removed. In addition, V_s and V_d change in complimentary manner. It results in reduction of switching voltage ripple in C_{y1} and C_{y2}. Finally, it can be seen that without the need of extra C filter, the common mode noise can be eliminated.

2.5 Conclusion

This chapter displays many literatures on PFC-related converters, bridgeless topology, and the proper method for the suggested research's effective plan. By forming the core of the suggested models, these chapters figure out the virtues and potential drawbacks of earlier study effort.

CHAPTER 3

BRIDGELESS PFC TOPOLOGIES

3.1 Introduction

This chapter introduces some generic measures to derive single phase bridgeless power factor correction topologies followed by the configuration of different basic types of dc cells. The study has been done on some already existing topologies with intent to review for possible scope of work in future. The performance benchmarking of these PFC topologies in terms of conversion, component size, and cost is presented. Bridgeless boost PFC topology is used as example to show the performance, which include theoretical and experimental results. Lastly, some comparison is noted between bridgeless topology and conventional diode bridge configuration. Active power factor correction converters are commonly employed as the front-end in AC-DC converter with an aim to achieve non distorted input current [1]. Figure 1 depicts the operation modes of the inductor in continuous mode. The boost PFC is the most popular topology [2]. It can be observed well from the mentioned figure that the current is always conducting across three power semiconductors. Since there are always two conduction paths involved in the diode bridge configuration. The conduction losses can be minimized by avoiding diode bridges and instead looks for more efficient PFC converter. As a result, the bridgeless topology has gained a lot of popularity these days [2], [10].

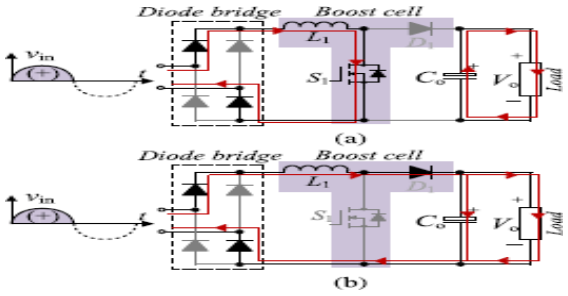


Fig 3.1 Boost PFC positive cycle (a) S: on, (b) S: off

3.2 Theoretical ways to form BL Topology

Many of the bridgeless PFC has started gaining attention over conventional PFC such as boost topology based. The bridgeless topologies are very effective in high power applications. Even though their primary aim is to reduce the conduction losses, they enhance the performance and efficiency of the device. Bridgeless buck boost PFC is widely used in electronics appliances. Different bridgeless PFC converters like ZVS soft switching resonant, interleaved boost or buck-boost based are significant area of research. In case of single converter cell as shown in Fig 3.1 they can take one input ac voltage. Because of that, Diode Bridge is used to convert positive input voltage from the ac input voltage so that single converter can perform since it will take positive or negative only. Now to get the bridgeless topology, one way is to use two converter cells with each cell operating with the positive or negative input voltage consecutively. Therefore, each cell is responsible to take one polarity from the ac side. The formation of two converter cell in parallel input (IP) with either series or parallel output (OS/OP) leads to the two combination. These are IPOS and IPOP formations of dual converter cells. Since there is a presence of two converter cell that leads to more number of components because one converter will operate in one cycle and other in another cycle. The components use in these topologies would incur lower thermal stresses than conventional topologies. Alternatively, The second way to get bridgeless topology is by using one converter cell with bidirectional switch [18],[27]. Resonant circuit instead of freewheeling diode would be required to design these kinds of single converter cells. However, the main focus is to attain bridgeless using dual converter cells. The combinations discussed above can be implemented by removing diodes from the diode bridge. Fig 3.2 presents three formations along with the flow of current. It can be seen that IPOP can have two types of configuration. Converter cells in Fig 3.2 (b) are using the diode in lower legs of the bridge only, whereas in Fig 3.2 (c) shows the converter cells configuration by eliminating the lower legs of diode from diode bridge. The last part of fig 3.2 shows the formation of diode in one side of the leg of bridge.

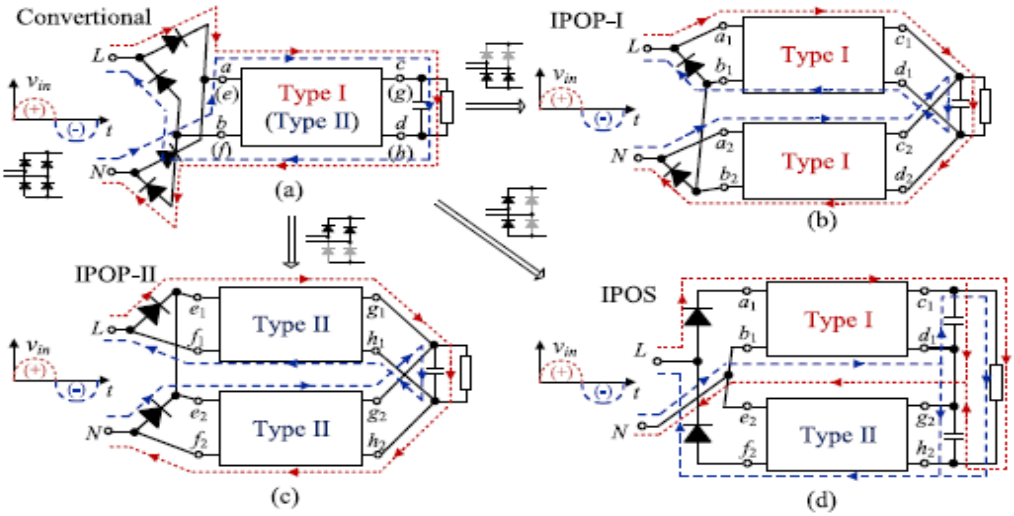


Fig 3.2 Ways to achieve "Bridgeless"

3.3 DUAL CONVERTER BASED PFC CONFIGURATIONS

As discussed above, input parallel with output series or parallel could yield different bridgeless PFC topology that can form by using two converter cells as shown in Fig 3.3.

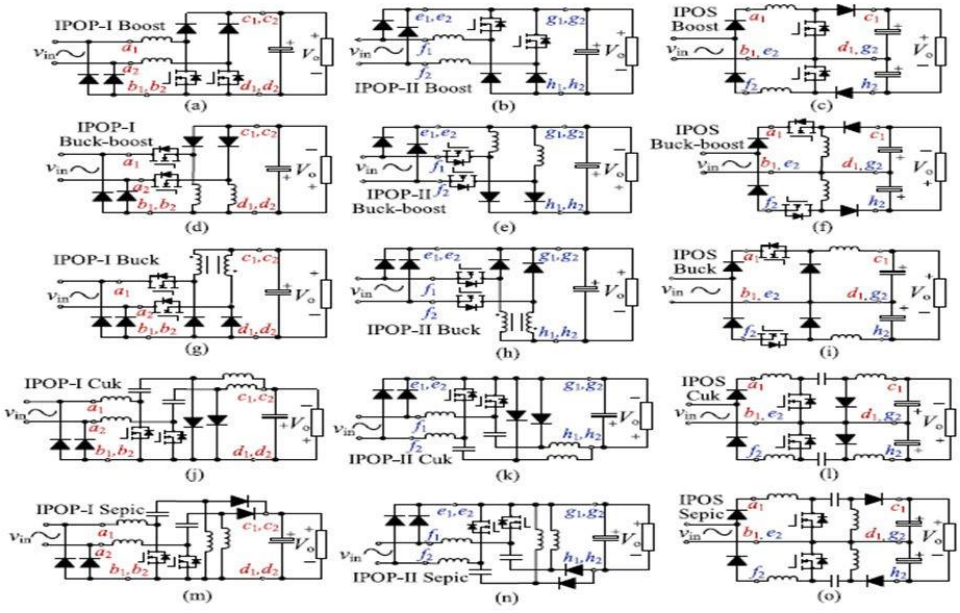


Fig 3.3 Formation of bridgeless PFC using different converter cells.

Different existing topologies of bridgeless PFC as shown in Fig 3.3 are reviewed and mentioned below.

BOOST TOPOLOGY: Three variety of boost topology is shown in Fig 3.3. The IPOS boost in fig 3.3 (c) is the oldest topology proposed in 1995. It is also called as dc split converter as it gives the final voltage double of each converter cell. However, this topology did not gain much attention due to the limiting of input voltage to maximum 135 ac voltage. Since the boost voltage ratio limitation is $\sqrt{2}\ V_{in} < 0.5\ V_o$. Nevertheless, the inductor present at input side can be modified into single working in both polarities. Fig 3.3 (a) illustrates the IPOP-1 boost configuration. It was presented in [29] and an electromagnetic compatibility upgraded version of earlier boost type consisting of extra diodes. Despite of such modifications, more can be done such as the very popular totem-pole topology is implemented as IPOS boost topology but the demerit is it has two different switch driving signals [33].

BUCK-BOOST TOPOLOGY: IPOP-1 topology presented in fig 3.3 (d) is widely recognized for dc motor drive, LED drivers and has better power factor performance than its conventional topology. The major area of concern in case of buck-boost is the high voltage stress across power semiconductors. The modified version is proposed in [35]. The other topology of this converter is fig 3.3 (f) i.e., IPOS buck-boost topology which have lower stresses to improve the efficiency in light load conditions but this topology has high conduction losses at the output diodes than conventional topology.

CUK and SEPIC: The IPOP-1 Cuk or Sepic topology presented in Fig 3.3(j) and (m) is proposed with a significant efficiency improvement. They have the ability to bring down the THD and achieve close to unity power factor. The use of two active switches on one side of bridge can be integrated to ease the drive circuit. Overall, they have lower stresses and lower switching losses. The IPOP configuration has gained a lot of attention which means IPOS type topologies can be look upon or further research such as achieving soft switching [33]. Hence two different converter cells can be merged to improve the

power factor.

3.4 WORKING PRINCIPLE OF BL-PFC

3.4.1 ACTIVE PFC DUAL CONVERTER

Active power factor correction (PFC) converters are typically employed as the front-end to avoid distorted ac input current, followed by a boost converter for low dc output voltage. The most common topology is the boost PFC converter. However, because two diodes are conducting and working at the same time, unexpected power losses occur, reducing the converter's overall efficiency. Furthermore, discontinuous current results at the input cause harmonic difficulties in the grid as well as common mode noise is an additional problem. As a result, several bridgeless boost PFC converters have already been discussed.

1. Bridgeless Buck Boost PFC Converter

In the wide input voltage range of adjustable electronic devices, especially in high voltage input conditions, a boost PFC converter creates a large voltage stress (>1000V). As a result, selecting components and an energy storage capacitor for a later-stage isolated converter is extremely challenging [1]. PFC converters with the capacity to provide both step-up and step-down topologies have been proposed to acquire adequate bus voltage. In a Buck-Boost PFC converter, the maximum device voltage stress is always lower than in a Boost PFC converter. In addition, the Buck-Boost PFC converter avoids the inrush current issue that arises with boost PFCs at starting [2-5]. As illustrated in Fig. 3.4, a bridgeless buck-boost PFC converter is presented. Bridgeless buck-boost PFC converters use three conduction semiconductors at all times without the input rectifier bridge, which improves efficiency greatly. Although, the common mode noise of a bridgeless buck-boost PFC converter is the same as that of a Bridge Buck-Boost PFC converter. By modifying the AC input line current waveform to match to the AC input line voltage, the control approach achieves near unity power factor. Average current mode control provides a

constant, low-distortion sinusoidal line current without requiring slope compensation, has a fixed switching frequency, and is suitable for high-power applications.

Operating & Design of Converter:

Two power semiconductor switches, S1 and S2, in the converter are triggered alternatively during each half cycle. The converter runs in boost mode when the AC input voltage V_s is less than the output voltage V_o. The converter runs in buck mode when the AC input voltage V_s is greater than the output voltage V_o.

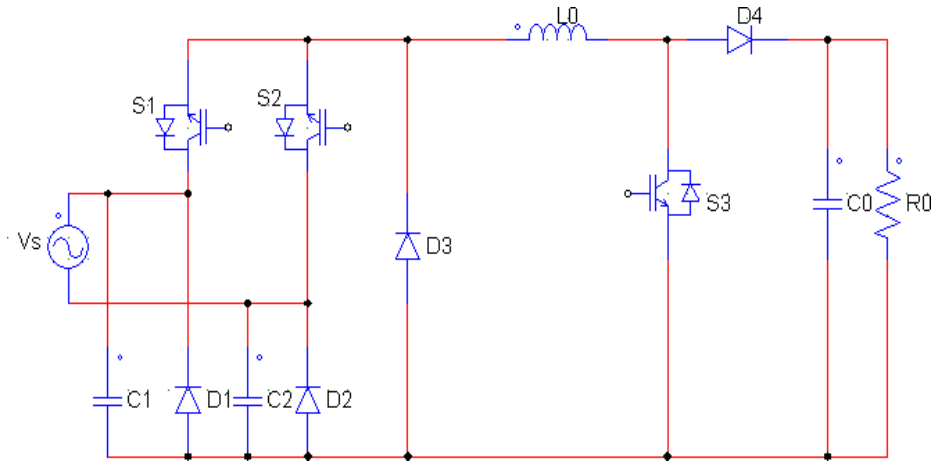


Fig 3.4 Bridgeless Buck-Boost PFC converter

Boost Mode 1: The switches S1 and S3 are conducting at this time. Inductor Lo stores energy from the input voltage. Furthermore, the energy is transferred from capacitor Co to the load.

Boost Mode 2: S3 has been switched off. The load is powered by the input voltage and Lo and the amount of energy stored in Lo decreases.

Buck Mode 3: S1 is turned on. C1 capacitor has been discharged. The load and inductor are powered by the input voltage.

Buck Mode 4: Diode D3 conducts when switch S1 is turned off. The load is powered by Lo. Capacitor C1 is charged at this point. The procedures performed during the negative half cycle are identical to those performed during the positive half cycle.

(a) Selection of Inductor

During the ON state of the switch S, the inductor value may be computed as

$$Li = \frac{D.Ts.Vd}{\Delta i} \qquad (4.1)$$

Taking inductor current ripple as 5%, while input current is 1 A, the unregulated rectified voltage is 198V with a duty cycle of 50% and 50 kHz switching frequency, on solving eq 4.1, the inductor value is calculated as 39.6 mH.

(b) Selection of Capacitor

In order to decrease THD in the supply current, a second order low-pass filter is employed to filter out higher order harmonics in the input current. The capacitance of the ripple filter is calculated as

$$Ci = \frac{Ip.tan\theta}{2.\pi.f.Vp} \qquad (4.2)$$

Here, taking the peak input voltage as 311 V along with RMS input current of 1.27A. The supply frequency is line frequency that is 50 Hz. For power factor adjustment, the value is 1 The computed capacitance is 200 nF.

2. Bridgeless Cuk PFC Converter

In PFC applications, the CUK converter has a number of advantages, including simple transformer isolation, natural protection against current ingress, which happens at the early stage or overload current, and lower input current ripple. The CUK converter is a buck boost converter with a common terminal that produces a negative polarity regulated output voltage. Nonetheless, unlike the inductor in the buck boost converter, the capacitor acts as primary energy storage and transfers between the input and output. Because of the large capacitor in the CUK converter, the input current and the current feeding the output stage were nearly ripple-free. The CUK converter, unlike the SEPIC converter, has constant input

and output currents with reduced current ripple. In the nature of PFC converter topologies, the CUK converter looks to be a suitable contender for applications requiring minimal current ripple at the converter's input and output ports. Figure 3.5 depicts the planned PFC BL-CUK converter. It has evaded DBR to some extent. The BL-CUK converter is made by connecting two DC–DC CUK converters, one for the positive half-line period of the input voltage and the other for the negative half-line period, according to Nahavandi et al (2015). Figure 2.4 also shows one rail of the output voltage bus, which is connected to the input AC line through slow-recovery diodes (Dp) and (Dn). Due to the high common-mode electromagnetic interference noise emission (EMI) concerns, the BL-CUK converter performs better than conventional converter. The voltage follower technique is used by the BL-CUK converter in DCM, which means that the current flowing in either as an input or output inductor (L1, L2, and L0) or the voltage across the intermediate capacitor (C1 and C2) causes the switching period to become irregular. For AC side PFC and output voltage regulation, DCM, on the other hand, requires an independent voltage sensor. However, the same control signal (V) may handle the two power switches, allowing the circuitry to be managed more easily.

Operating Principle

The analysis assumes that the converter operates in a stable condition and makes the following assumptions: pure sinusoidal input voltage, perfect lossless components, and a large capacitor with small switching voltage ripples at the sample switching period. Furthermore, the output capacitor (C0) has a large capacitance, ensuring that the voltage remains consistent during the line period. The initial DC–DC CUK circuit, L1 Q1 C1 L0 D0, will be active throughout the positive half-line cycle because of diode Dp, which connects the input AC source to the output. The second DC–DC CUK circuit, L2 Q2 C2 L0 D0, will be active during the negative half-line cycle through the diode Dn, which connects the AC source to the output. This produces the average voltage across capacitor C1 during the line cycle, which is indicated as follows:

$$V_{C1}(t) = \begin{cases} V_{ac}(t) + V_{OUT}, \text{ during positive cycle} \\ V_{out}, \text{ during negative cycle} \end{cases} \quad (4.3)$$

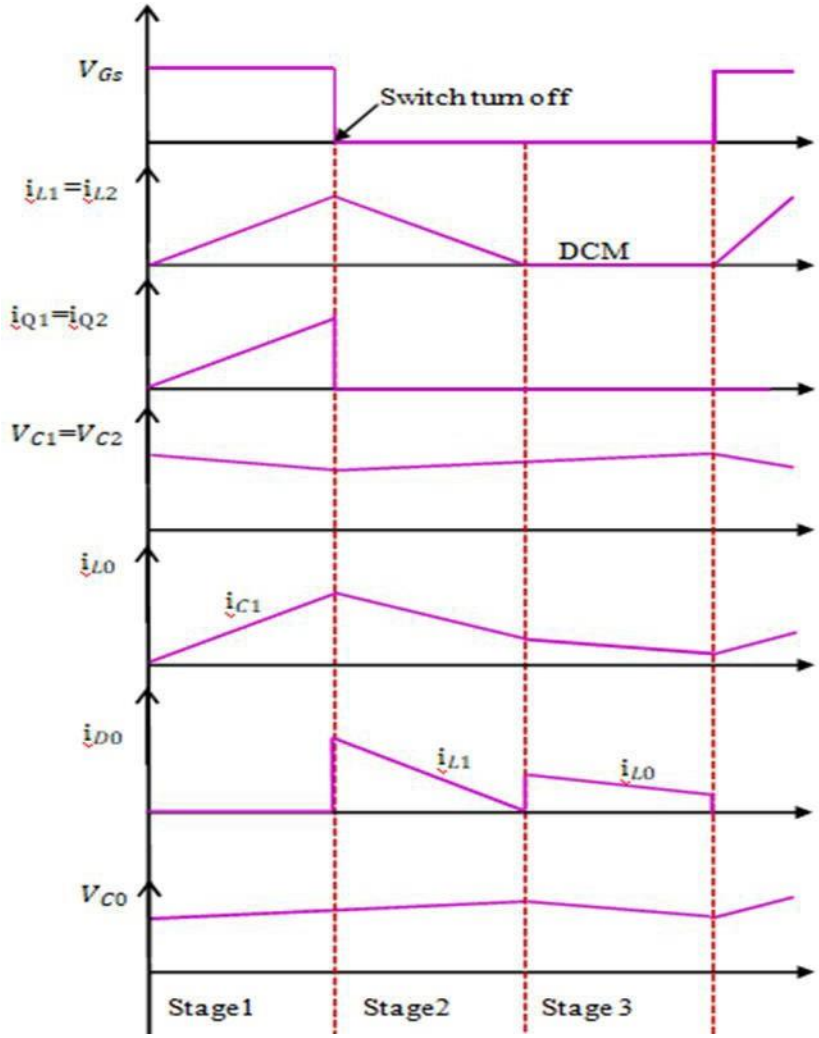


Figure 3.6 Theoretical waveforms during one switching period.

Because of the symmetry of the circuit, it is critical to analyze it during the positive half cycle of the input voltage. Thus, the diode (D_p) switched on and off continuously throughout the positive half line voltage switching time, and the average voltage across (C2) is equal to the output voltage (Vout). Because of the present flow through (C2 and L0), the output is minimal. As a result, the current flow through (L2) during the positive half cycle of the input voltage is equal to the negative current flow through Q2's body diode. The current is normally sent via the body diode of the static switch (Q2) during the positive half cycle of the input voltage. This is due to the input inductors' (L1 and L2) low

impedance at line frequency. As a result, the input diode (Dp) and the body diode of (Q2) seem to be connected in parallel to share the return current. The diode, which has a lower voltage drop, will carry a large percentage of the return current. In addition, the functioning of the proposed BL-CUK converter will be discussed in terms of the three DCM inductors. Many merits will be acquired by using it. The power switches were shifted about ON at zero current, and the output diodes (D0) were switched OFF at zero current, resulting in a natural near-unity power factor. As a result, losses at the time of turn-on switching and the opposite recovery of the output diodes might be reduced. The theoretical DCM waveforms during one switching cycle at the positive half cycle of the input voltage are shown in Figure 3.6. The BL-CUK converter circuit operates in DCM, which allows it to be divided into six independent operational phases during complete switching periods.

Positive half line voltage operation

Stage 1 [t_0, t_1]: When the switch (Q_1) is turned on. The inductor current (i_{L1}) forward biases the diode (Dp). The result is that the diode (Dn) is biased in the opposite direction by the reverse voltage (Vac + V_O). The current flowing through the inductors (L_1 and L_0) will be raised linearly with the input voltage at this stage.

Stage 2 [t_1, t_2]: This stage starts when the switch (Q_1) is switched off and the diode (D_O) is turned on at the same time, creating a channel for the inductor currents (i_{L1}) and (i_{L0}). The diode (Dp) continues to conduct to provide a channel for (i_{L1}). When (i_{D0}) reaches zero and (D_0) becomes oppositely bias, this interval is complete. The diode (D_0) is turned off when the current is zero.

Stage 3 [t_2, t_3]: Only the diode (D_O) conducts throughout the interval to provide a route for (i_{LO}). As a result, the inductors in this range serve as steady current sources. As a result, the voltage across the two inductors is 0V. The inductor current (i_{L0}) charges the capacitor (C_O). When (Q_1) is switched on, this period ends.

Negative half line voltage operation

Stage 4: When the switch (Q_2) is turned on, this stage begins. The inductor current (i_{L2}) forward biases the diode (Dn). The input voltage will cause the output diode (Dp) to become oppositely biased. The reverse voltage (Vac + V_O) will make the output diode (D_O)

oppositely biased. The current goes via the inductors (L_2 and L_O and is boosted linearly as the input voltage increases.

Stage 5: This stage starts when the switch (Q_2) is switched off and the diode (D_O) is turned on at the same time, creating a channel for the inductor currents (i_{L2}) and (I_{LO}). The diode (Dn) continues to conduct to provide a channel for (i_{L2}). When (i_{DO}) reaches zero and (D_O) becomes biased, this interval ends. The diode (D_O) is turned off when the current is zero.

Stage 6: Only the diode (D_O) conducts during this interval to provide the route for (i_{LO}). As a result, the inductors in this range operate as constant current sources. As a result, there is no voltage across the two inductors. The inductor current (i_{LO}) will be used to charge the capacitor (C_O). When (Q_2) is switched on, this period ends.

Voltage Gain and Capacitor Selection of BL CUK Converter

The power balancing theory will be used to determine the voltage conversion ratio (M) in terms of the converter factors. The following is how the average input power will be expressed:

$$<P_{in}(t)>_{T/2} = \frac{2}{T}\int_0^{T/2} Vac(t) <i_{ac}(t)> T_s\, dt \qquad (4.4)$$

where $<.>_x$ signifies the average value during the interval (x), (T) denotes every half line, (Ts) means the switching period, then period, (T) denotes the entire period of the whole line voltage, and (Vac and i_{ac}) represent the input line voltage and current, respectively. The input current is similar to the inductor current (L_1) in the positive halfof the line cycle. Over a switching time, the average input current is provided by

$$<i_{ac}(t)>_{Ts} = <i_{L1}(t)>_{Ts} = \frac{Vac(t)}{Re} \qquad (4.5)$$

Where (Re) is the modeled input resistance of the converter and is given by

$$Re = \frac{2Le}{D^2} . \frac{1}{Ts} \qquad (4.6)$$

where (D) is the duty cycle of the switch, and (Le) is the parallel combination of inductors (L1 and L0). The allowable voltage conversion ratio is computed by multiplying (2.5) by (2.6) and enforcing the power balance between the input and output ports.

$$M = \frac{Vout}{Vma} \qquad (4.7)$$

Where (Vma) is the peak AC line voltage input. However, because the values of the capacitors (C1) and (C2) alter the fundamental nature of the input line current, they were significant parts in the suggested BL-CUK converter. It should be selected such that their steady-state voltages have the structure of the rectified input ac line voltage waveform, as well as an output voltage with minimal switching voltage ripple in its potential. Furthermore, the converter inductors should not oscillate at low frequencies due to the values of (C1) and (C2). The energy transformation of the capacitor will be resolved according to the values of the inductors (L1 and L0) (by assuming that L1 = L2) in this scheme, such that the resonant frequency (fr) at the DCM stage will be higher than the line frequency (f_L) and considerably below the switching frequency (fsw).

Thus, $f_L < f_r < f_{sw}$ (4.8) $f_r = \frac{1}{2\pi\sqrt{C1(L1+Lo)}}$ (4.9)

In contrast to this design, the output capacitor (C0) requires a large amount of energy to retain the less energy necessary for equalizing the differences between the time-varying input power and the constant load power. The output voltage ripple at low frequencies is given as,

$$\Delta V_{OUT} = \frac{1}{Co}\int_{Ts/8}^{3Ts/8}[\in i_{LO} - i_{OUT}]\, dt \qquad (4.10)$$

In contrast to this design, the output capacitor (C0) requires a large amount of energy to retain the less energy necessary for equalizing the differences between the time varying input power and the constant load power. The output voltage ripple at low frequencies is given as,

$$\in i_{LO} = \frac{V2}{Re.Vout} \qquad (4.11)$$

The capacitor ripple equation is obtained by substituting (4.11) to (4.10) and calculating

$$\Delta V_{OUT} = \frac{Vout}{\omega \times RL \times Co} \qquad (4.12)$$

Where (R_L) indicates the corresponding load resistance value and (ω) represents the angular frequency.

3. Bridgeless SEPIC PFC Converter

Figure 4.5 represents the proposed bridgeless SEPIC converter. The bridgeless SEPIC converter is a more sophisticated variant of the bridge SEPIC converter. On the supply side,

the bridgeless SEPIC converter simulates a resistor while maintaining a well-controlled output voltage. The converter draws a sinusoidal current from the utility in this case. An appropriate sinusoidal reference is normally required for this, and one is provided, with the control purpose being to push the input current as near to zero as feasible. The PFC bridgeless SEPIC converter is a straightforward circuit that converts a single-phase AC source voltage to a chosen dc output voltage while maintaining a high power factor. Sepic is a dc-dc converter that can alter a variety of dc voltages while maintaining a constant output voltage. To fulfill harmonics regulation and standards, active power correction techniques for power supply and power charger are increasingly important [7]. Boost type converters have been employed in the past, but they have several drawbacks [4]. Those disadvantages are overcome in a bridgeless Sepic converter by using the PWM approach to force the current [8] to be in phase with the input voltage as much as possible. A unit power factor is produced when the voltage is in phase with the current, which is particularly desirable for increased power quality [2].

Operating Principle

The procedure is completed when MOSFET switch 1 operates in the positive half cycle and MOSFET switch 2 operates in the negative half cycle.

Mode 1: During the first mode of operation of the bridgeless SEPIC converter both switches are turned on in this mode. Because D_1 is a forward conduction diode (F.B.), so it facilitates the completion of the initial mode of operation. In this mode of operation, both the inductors L_1 and L_2 play a role. In this mode of functioning, L_1 magnetizes while L_2 demagnetizes.

Mode 2: Only one switch is active in this mode of operation (S1: off, S2: on). Because switch S1 is in the off position, the mode of operation is altered. Through the diode D_3, inductor L_2 demagnetizes. In this mode of operation, diode D_2 has no effect. V_O obtained as output voltage.

Mode 3: This is the bridgeless SEPIC converter capacitor's third mode of operation. C_1 begins to charge, and the inductor L_2 begins to magnetize; in this state, D_3 is reverse biased (R.B.). S1 is in the off state, S2 is in the on state, and D_1 is in the on state.

DESIGN PROCEDURE

Input Current

The following equation may be obtained from the converter's output power and efficiency:

$$I_{nput} = I_1 \sin(\omega t) = \frac{2Pout}{mV1} \sin(\omega t) \qquad (4.13)$$

And the mode II duration may be used to derive the equation for ΔI_L (current ripple):

$$\Delta I_L = \frac{Vin(to)d}{L1.fsw} \qquad (4.14)$$

Inductor (L2 *and* L_2)

L1 and L2 inductors may be determined using the maximum ΔI_L specification (as derived in Eq. 4.14):

$$L_1 = L_2 = \frac{Vin(to)d}{\Delta Iripple.fsw} \qquad (4.15)$$

Capacitor (C_O)

Because the output voltage ripple is greater, the Co (output capacitor) must be large enough to mitigate the effect. As a result, the resulting equation is:

$$C_O = \frac{Po}{4.f1.Vo.\Delta Vo} \qquad (4.16)$$

Capacitor (C_1)

Because it is continuous in one switching period and follows the input line voltage, it has a significant influence on input current. As we all know, resonance frequency is crucial in capacitor (C_1) design. To avoid current oscillation, the resonant frequency should be higher than the line frequency; similarly, the resonant frequency should be lower than the switching frequency. The following is the equation derived from the aforementioned assumptions:

$$C_1 = \frac{1}{4.\pi(L1+L2).fr^2} \qquad (4.17)$$

CONCLUSION

Different types of PIPO and PISO configurations are studied. Input parallel output parallel topologies; a lot of research has been done for example in case of Cuk PFC converter. On the other hand, PISO opens up a lot of area from research point of view i.e., soft switching, zero voltage or zero current switching across the switches. Two different cells can be

merged to form a converter. The subsequent chapter illustrates one of those types of converter. Moreover, the bridgeless converters are feasible for different output capacitor arrangements that can reduce switching frequency ripple significantly.

CHAPTER 4

CONTROL OF THE PROPOSED SYSTEM

4.1 Introduction

Optimization of system reliability at the input terminal and management of the power supply under steady and transient states are determined by the control method chosen. The controllers are intended to increase the converter's performance. The controller's primary needs are: I) fast dynamic reaction II) faster computing time; III) excellent signal detection and computation accuracy. Under variable source and load situations, the typical controller's performance is one of the deciding factors to get the desired results. This chapter discusses the current control approaches for single-phase systems. For PFC buck-boost converter topologies, hysteresis-based control technique has been proposed. Even with significant changes and advancements, there are multiple kinds of distortion. The input side filter is used to ensure that the ripple current created by switching does not reach the line conductor. Nevertheless, the filter attenuation is not infinite, and some ripple does affect it, leading the line voltage waveform to be further distorted. The current-loop is the second source of distortion. The role of the control system would be to maintain the inductor current so that its low frequency value (free of switching noise) is equal to the reference value. A few controller types, however, are not sufficient of precise current control. Odd harmonics of common mode arc have been recorded in the literature, resulting in exceptionally high THD. The only option is to use a high switching frequency (40-100 kHz) such that the regulator's flaws are in the frequency region where the reference signal is small or non-existent. The output voltage-loop signal is the third source of distortion [4]. At double the line frequency, the regulator is unable to eliminate the fundamental output voltage ripple. As a result, the second harmonic sync with the reference signal of current results in additional distortion of the input current. Lastly, operating a load that is less than normal cause’s distortions. Although, this does not affect

much the control of switching However, certain controllers have trouble maintaining the inductor current in continuous conduction mode at low loads, resulting with extra distortions [3]. All the four types of distortions are different from one another, but their combined impact can cause THD to surpass the specified amount. With correct design and traditional approaches, THD may be reduced to the absolute minimum at an uncompetitive price. As a result, new approaches for reducing the unique impacts of each source should be devised. The current-mode controller is the most typically preferred for loads over than 1KW. It'll be implemented as an integrated circuit, and it's reasonably priced. If low harmonics are to be avoided, it must be utilized with a high switching frequency. However, due to magnetic and semiconductor losses, working at 50 kHz or higher at very high loads is not favorable in case of current-mode control. Significant commutation at high voltages and currents also produces electromagnetic compatibility issues. As a result, working at a "low" switching frequency can be a boon. Surely, filtering the ripple is the main. This study proposes a unique way for properly controlling the input current at low switching frequencies, with aim to filter odd harmonics of the line frequency and switching ripple than with standard average current-mode. The two types of current mode control are presented in the next section.

4.2 Current mode control technique

The current control strategies are used to regulate PFC converter such as peak current mode control and hysteresis current mode control strategies are explored in this part to allow the input current to be synced with the fundamental component of the input voltage. Input voltage, current, and output voltage are the parameters utilized in controllers to create the gate signals for the switches. In the, there are two loops. The inner loop is in charge of managing the inductor current's form, while the outer loop is in charge of controlling the output voltage and keeping it constant at the reference value. The output voltage level is clamped and compared with the reference of the outer loop. The PI controller's input is determined by the error acquired from this comparison. This controller's output is the scaling factor, which is used to calculate the current reference. The reference current, i_{ref}, is calculated by multiplying the voltage controller's output by the rectified input

voltage. The inductor current is compared to the reference current in the inner loop. The separate current controllers that will be employed to create the gate signals for the switches will handle the inaccuracy of this comparison.

4.2.1 Peak current mode control

Peak Current Control mode is a well-known power conversion control method. It has been widely used in PFC pre-regulator converters. The inductor current is used as the programming variable in this control setup, and it is compared to the reference current to create the switching signal. A clock signal turns on the switch, which is switched off when the total the inductor current approaches the reference current. The inductor current builds while the switch is on, and when it hits reference, the switches are switched off, prompting the inductor current to push down until the next clock. The PCMC's benefits are outlined as follows. The switching frequency is constant. For industrial purposes, the switch current can be separately sensed by current transformer; thereby the losses due to sensing resistor can be avoided. Also, there is no need of current error amplifier and compensation. Limiting switch current at the time of need is also possible. Alternatively, the demerits are the availability of sub-harmonic oscillations at duty cycles as a result the compensation ramp is needed. Moreover, the input current distortion gets increased at peak voltage and the increased sensitivity to commutation noises are the negative traits [9-11].

4.2.2 Hysteresis current mode control

Because it reacts rapidly, the hysteresis control technique gives outstanding dynamic performance. There is also an inbuilt peak limiting capability. This sort of control generates two sinusoidal current references which correspond to the maximum and minimum boundary limits. A narrow hysteresis band is intended to achieve reduced ripple in the input current. The greater the switching frequency, the smaller the hysteresis band is. In a constant frequency operation, it is also feasible to enhance the hysteresis control, although this generally increases the control circuit's complexity. The switch is switched on when the inductor current falls below the lower reference and off when the inductor current rises over the higher reference in this control mechanism, resulting in variable frequency control. It can be opposite also depending on the signal connection and

arrangement. The control mechanism used in this technique is extremely basic and straightforward to implement. The selected control method is depicted in block diagram format in Fig. V_{O*} is the intended reference voltage at the converter's output, while V_O is the converter's actual output. The voltage controller takes the error in the output voltage. The error is processed by the voltage controller (PI controller) and generates a current signal that is adequate (IS). The input signal (IS) is multiplied by a unit sinusoidal template that is created via phase locked loop (PLL) generating I_S sinωt. The load current I_L is subtracted from the I_S sinωt to get the reference signal I_S*. Since the inductor current cannot change, the circuit gives the absolute value of the reference signal that is I_C*. The actual signal and the reference are connected to the current controller to generate a proper gating signal.

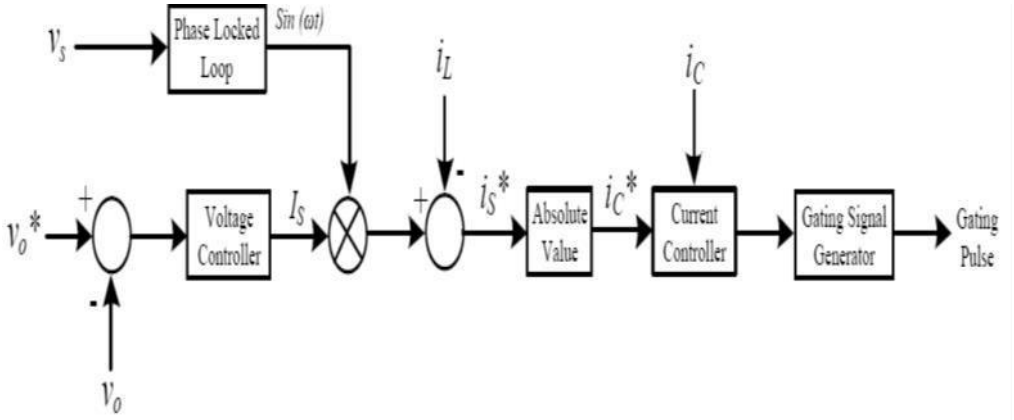


Fig.4.1 Adopted modulation scheme for the proposed converter

The current controller is hysteresis controller where the upper and lower band is created by adding and subtracting a constant with I_{C*}. The input current is entitled to adjust itself within the band created. So, when the current goes above or below the band, the pulses to the switch connect or disconnect accordingly. This is one of the ways to track the reference current and resultant current to obtain the proper switching as near to sinusoidal with low harmonic content and low THD. Due to this the power factor also improved.

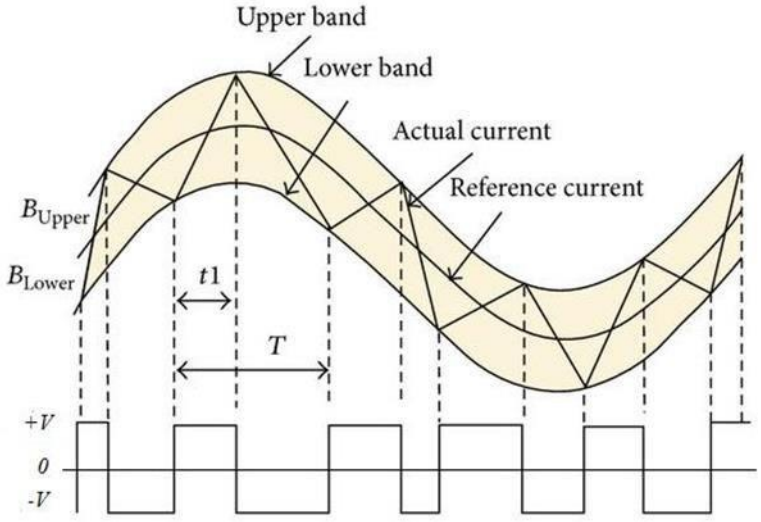


Fig 4.2 Hysteresis controller two levels

4.3 Control of Parallel Input Series Output PFC Converter

In the bridgeless PFC converter, the current mode hysteresis control approach has been implemented keeping in the mind of its robustness and ease of operating at high frequency. Since the bridgeless contains two active switches instead of diode bridge formation, so the gating to both the switching is given through the hysteresis controller. The input voltage with the unit template is multiplied with constant value taken as reference current as stated in the previous section. The output of that is compared with the actual input current to produce the gating signal passing from the relay block in MATLAB subjecting to the upper and lower band. When the input sinusoidal voltage goes above zero that is positive side, the band is subjected to give pulses to the one switch. Similarly, when voltage goes below zero, the pulse would be given to another switch. In this way both the switch gets turn on simultaneously in each cycle. In fig 5.3, the demonstration is shown that is implemented through Matlab/Simulink software. The Power Factor of converters with open loop control has been shown to be quite low as compare to the closed loop due to the hysteresis controller implementations.

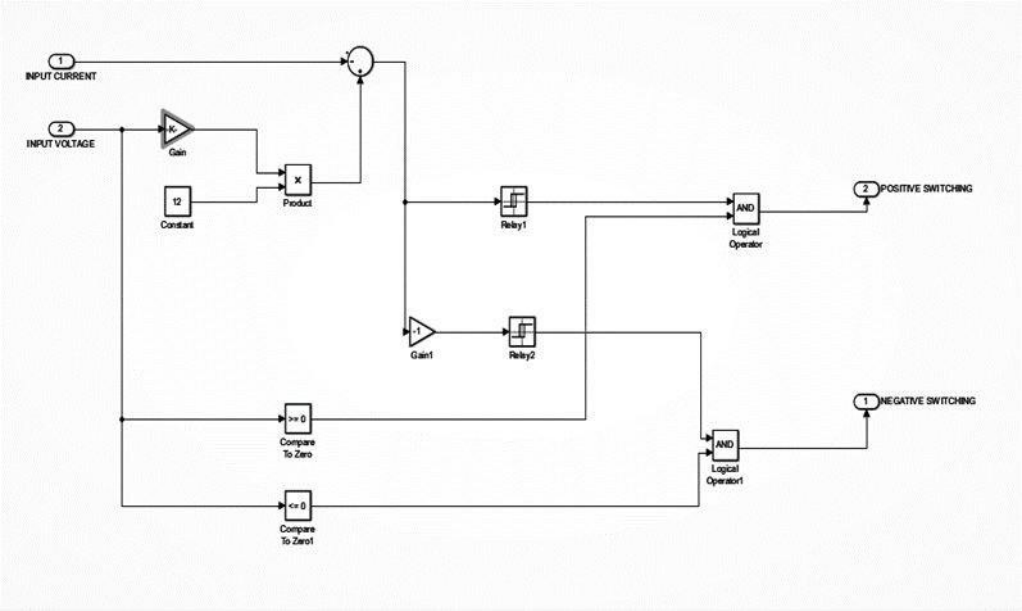


Fig 4.3 Control of proposed bridgeless converters.

As shown in the fig 4.4, the gate signals, $S_A$and S_B are pulsated through the polarity detecter to synchronize the gate signals and grid voltage. Fig 4.4 shows the simplified gate signals for the proposed topology. The gate signals are synchronized with the line frequency. The switches are getting turn on alternatively in each cycle to shape the input inductor current.

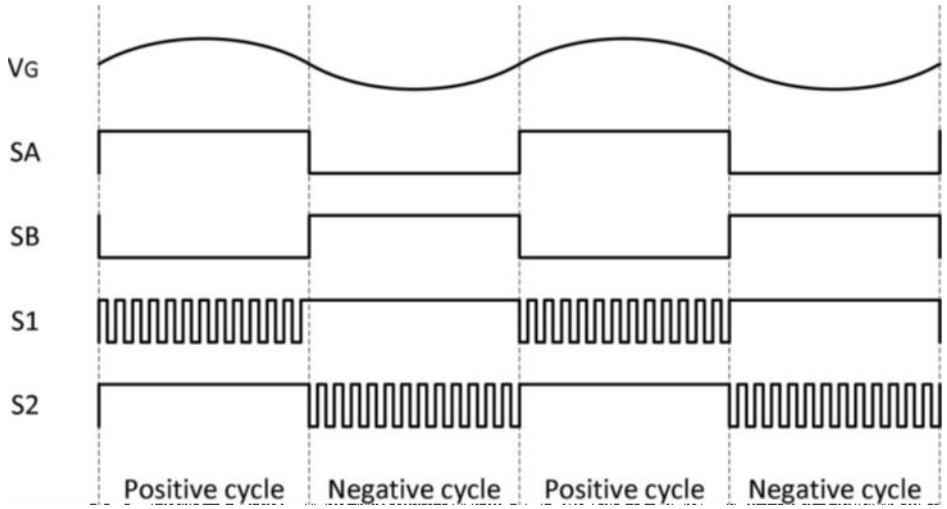


Fig 4.4 High level view of gate signal for proposed bridgeless converter.

The modulation strategy can help in reducing the semiconductor losses in following ways:

1) There is only single pair of switching unit with high frequency switching at any one moment. Since turning on of both switches at same time leads to more losses.

2) Conduction losses: when the main switch is not set to high frequency switching, it is switched on to allow the reverse current to flow via the channel rather than through the body diode. A channel of a MOSFET has a smaller voltage drop than a MOSFET's body diode [21{AVG}]. The basic PFC current component does not flow via the circuit. Only the high ripple current is carried by the circuit. Input Inductor ripple current has a low root-mean-square value, which means that conduction losses are low.

3) Switching losses: The switches are trying to switch at grid voltage zero crossings. In theory, it's also the grid current's zero crossing places, therefore zero current switching can be observed. Furthermore, the line frequency, such as 50 Hz, is the switching frequency. As a result, the switches' switching losses may be ignored.

4.4 Conclusion

In this section, two well-known current control strategies for single-phase PFC converters were discussed, and the results are compared to get a better knowledge of PFC topology control techniques. Peak current mode control and hysteresis current mode control are two of the control approaches available. The Matlab/Simulink application was used to conduct the converter simulation. The advantages, drawbacks, control strategy, and THD of input current are emphasized for each control approach. The findings reveal that, while the PFC values for these control approaches are virtually identical, the THD values differ. The peak current mode mode control approach is less noise sensitive than the hysteresis current mode control technique, and has fixed switching frequency as compared to hysteresis current control technique. One converter can be utilized to reduce the harmonic current created by the other non-linear load without the need for a separate converter. With the use of a simulation analysis, it has been shown that this arrangement eliminates practically all lower order harmonics, allowing us to obtain a power factor closer to unity and a THD of less than 15%. This approach, however, is confined to applications in which the non-linear load (pulsating) current is low and constant. In addition, the literature study was created to investigate various modulation schemes of power factor

correction strategies. The tracking of signal and comparing with actual is the real point of observation. The major drawback of this control is poor efficiency in case of non-linear outputs. The sliding mode control approach can be implemented in that case since due to its robustness it can be more efficient under suck situations.

CHAPTER 5

STEP BY STEP DEVELOPMENT OF BRIDGELESS PFC

5.1 INTRODUCTION

The purpose of the project work is to investigate the complete bridgeless structure employed as PFC along with back-end DC-DC system. Various single-stage and two-stage PFC converter are offered to improve the SMPS's input power quality. The suggested single-stage and two-stage converters' system setup, working principle, and analysis of boost bridgeless PFC and Bridgeless buck-boost with a direct connection of input and output connected through ground wire is compared based on dynamic loading are presented in this chapter. As shown in Figure 4.1. MOSMPS is the abbreviation of multiple output switch mode power supply.

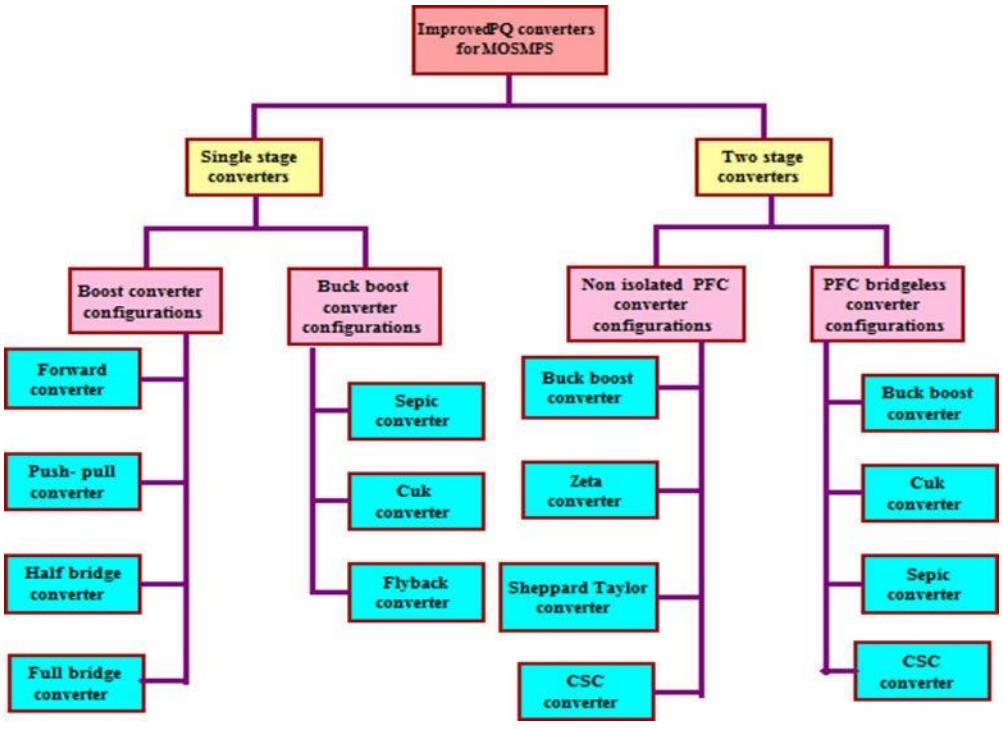


Figure 5.1 various converter configurations for Multiple Output Switched Mode Power Supply (MOSMPS)

5.2 ANALYSIS OF BL-BOOST PFC CONVERTER

In this section, the operating modes of IPOS boost topology is reviewed and shall be compared with advanced bridgeless buck-boost PFC for performance evaluation. The design specifications are mentioned in Table 1. The operating modes of IPOS boost converter are shown in the Fig 5.1.

TABLE 1

IPOS BOOST SPECIFICATIONS

Parameters	Value
Switching frequency	65kHz
Line frequency	50 Hz
RMS input Voltage	220 V
Output Voltage	400 V
Output Power	3.6 kW`
Inductor	254e-6 H
Capacitor	1500e-6 F

The operating modes of the conventional boost PFC is introduced in [35]. The boost IPOS modes are discussed. Certain assumptions such as considering all components as ideal, large output capacitor to attain V_O as constant are considered. Due to the similar positive and negative line cycle, the positive cycle is mentioned.

Switch On: The current starts flowing through inductor, rectified diode and switch. Inductor current rises linearly. During this phase the input voltage would be equal to the inductor voltage, while the capacitor handles the load side.

Switch Off: Now the energy stored in inductor will find a path to transfer it to load, whereas the capacitor will discharge continuously and resulting to the drop in voltage. During this period the voltage across inductor is $Vin - \frac{1}{2}Vo$. The voltage conversion ratio of IPOS boost PFC converter is $\frac{Vo}{Vin} = \frac{2}{1-D}$

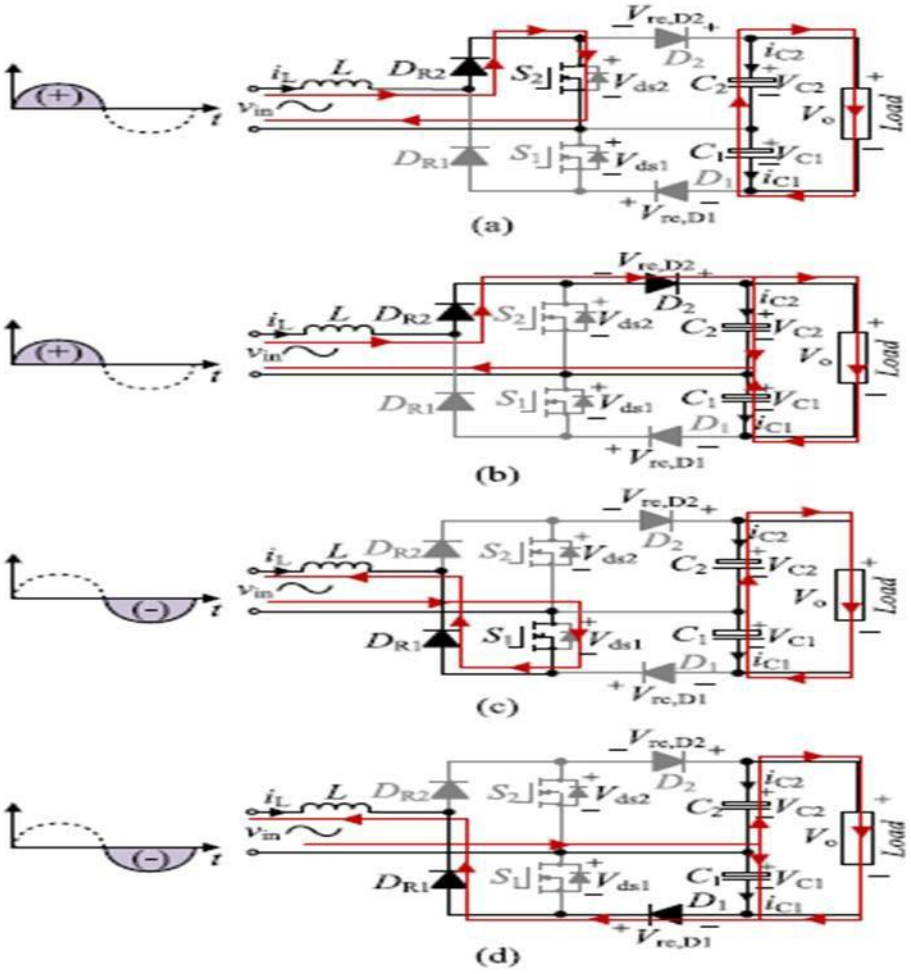


Fig 5.2 Operating modes of IPOS Boost.

This type of configuration has lower switching losses, but high conduction losses because of output diodes. Overall, the voltage stress across switch and output is only half of that in conventional PFC converter. Fig 5.3 shows the input and output waveforms. It can be inferred that the THD has significantly improved compared with conventional boost PFC. Fig 5.4 shows the total harmonic distortion. However, the second harmonics are the inherent nature of this topology as a result it is always challenging to bring input current in phase with output voltage. In addition; the voltage stress across semiconductors in IPOS boost converter is 200V, which is half of conventional converter. The performance is analyzed under dynamic loading changing from half load to full load as shown in Fig 5.5. It can be observed that from the current waveform under load variation, it is pulling

sinusoidal from the utility.

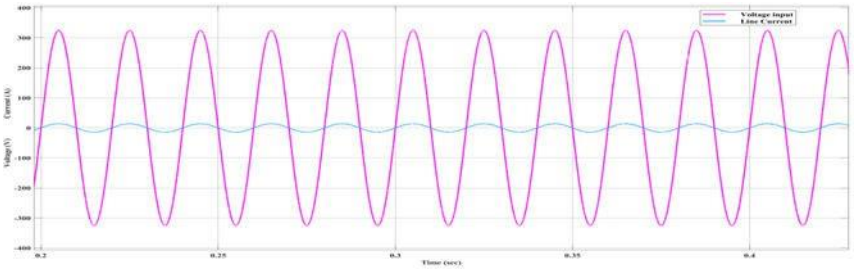


Fig 5.3 Input voltage current waveform under rated (steady state).

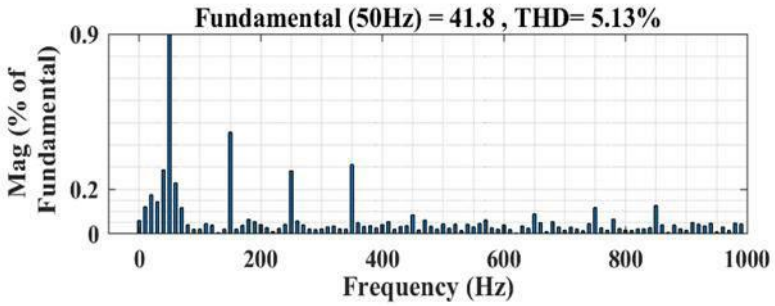


Fig.5.4 THD in PFC boost

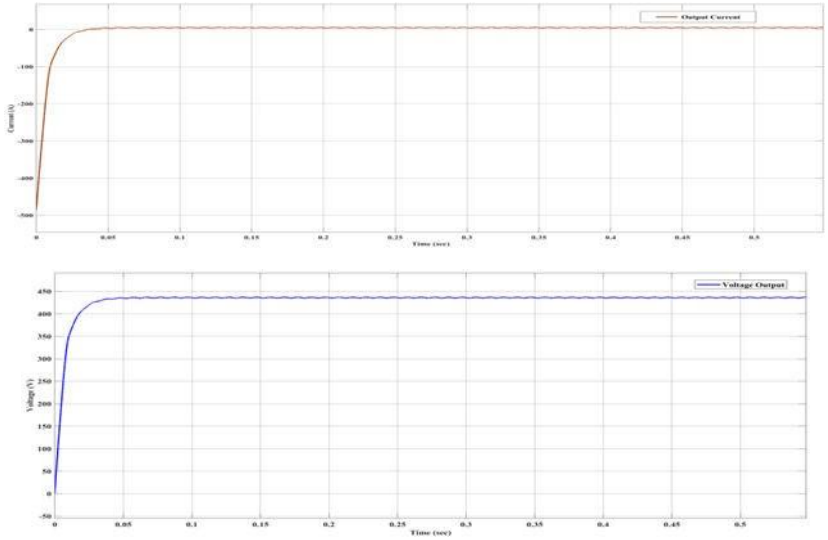


Fig 5.5 Output voltage and Current waveform.

It can be seen from fig 5.6 that under the dynamic performance, the output is maintained at desired range. The battery has been employed in the converter. Dynamic performances are observed by varying the load condition.

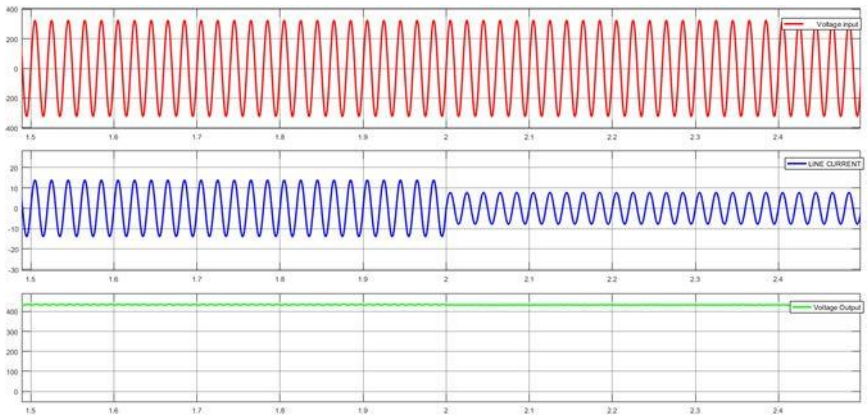


Fig 5.6 Transition of Current under dynamic

5.3 Bridgeless Common Ground Buck-Boost PFC Converter (CGBPFC)

This section proposes bridgeless PFC stage in input cascaded with dc/dc converter in output. There is the direct connection between ac supply ground to the negative terminal of the dc output as shown in Fig 5.6. This direct connection releases the drawbacks faced by bridgeless PFC rectifiers such as subjected to high value of common ground noise on the input lines. The bridgeless buck-boost circuit is made up of two identical switches on one leg and two diodes on the other, with one switch active during the positive half cycle and the other during the negative half cycle. The PFC stage converts the full-wave rectifier's high-crest-factor current into a perfectly sinusoidal waveform that is in phase with the line voltage [3]. Furthermore, the second stage is divided as the SEPIC configuration operates during the positive half cycle of the proposed converter as illustrated in Fig. 5.7, while the Cuk configuration operates during the negative half cycle as shown in Fig. 5.8. The Cuk and SEPIC topologies outperform the ZETA and Flyback PFC topologies in total harmonic distortion (THD), natural protection against inrush current, efficiency, and power factor correction [9]. As a result, for low output-voltage applications, a combination of SEPIC and Cuk is proposed that can work in discontinuous conduction mode. The roles of inductors L1 and L2 are switched throughout each half-cycle. L1 operates as a converter side inductor to manage power conversion during the positive half-line cycle. In the proposed converter, L2 operates as a converter side inductor during the negative half cycle. Because L1 and L2 are not active at the same time, they can be placed on distinct limbs of

the same magnetic core, increasing power density. The peak value of the input ac voltage is expected to be equal to the maximum capacitor voltage. As the loading resistance decreases, the grid side current increases rapidly in a relatively short period of time. It is observed in results section that the THD is significantly improved because of common grounding as compared to the PFC boost.

OPERATION ANALYSIS

Figure 5.6 illustrates the proposed CGBPFC rectifiers. The proposed CGBPFC converters uses two active toggles S1 and S2, four diodes D1, D2, D3, and D4, three inductors Lf, L1, and L2, and three capacitors C1, C2, and Cout. This section describes an operation states during CCM in each switching period (Ts). During the positive half cycle of CGBPFC, diodes D_2 and D_4 are reversed biased, the switches S_1 is hysteresis controlled and S_2 is turned off. Thus, the components S_1, D_1, D_3, L_f , L_1, C_1 and C_{out}, participate in conduction to supply the dc side load during the states outlined below. Similarly, during the negative half cycle, D_1 and D_3, are reversed biased, S_1 is turned off and S_2 is hysteresis controlled. In this case S_2, D_2, D_4, L_f , L_2, C_2 and C_{out} participate in the operation

State 1 $|0 - t_1|$: In this interval at the positive half cycle, S_1 is turned on. As a result, the input filter inductor L_f, is charged by the input ac source, V_g with a slope of V_g=$L_{f.}$ The capacitor C_1 is discharged through the inductor L_1 and dc output, thus, L_1 is charged linearly with a slope of V_{c1} = L_1. The diode D_3 is reverse biased, and the stored energy of C_{out} supplies the dc resistance load i.e. R_{load}.

State 2 $|t_1 - Ts|$: Contrary to state 1, in this interval the switch S_1 is turned off and the diode D_3 is forward biased. Hence, the current path is provided to discharge the energy of L_f and L_1 with slope of (Vg – V_{C1} - V_{OUT}) / L_f and –Vout = L_1 ((Vg + V_{C2}) / L_f), respectively.The procedures carried out during the negative half of the cycle are the same as those carried out during the positive half.

Design Consideration

Semiconductors rating By applying KVL in Fig. 3, the voltage across the semiconductor devices in the proposed CGBPFCs are obtained as follows:

$$V_{S1} = V_{C1} + V_{out},\ V_{S2} = V_{C2} \qquad (2.18)$$

$$V_{D1} = V_{C1},\quad V_{D2} = V_{C2} - V_{out} \qquad (2.19)$$

$$V_{D3} = V_{C1} + V_{out},\quad V_{D4} = V_{C2} \qquad (2.20)$$

By applying KCL in Fig. 3, the peak current of $L_{1,2}$ and the semiconductor devices are obtained as follows

$$IL_{1,2} = (1/L_f + 1/L_{1,2})DT_S.V_g - I_g \qquad (2.21)$$

$$IS_{1,2} = ID_{3,4} = IL_{1,2} + I_g \qquad (2.22)$$

Passive Components Design

The input filter inductor is designed according to the ac source voltage and the desired maximum input current ripple,

Δi_{Lf} as: $L_f = DV_m / (\Delta i_{Lf} * f_s)$ (2.23)

The value of inductors L_1 and L_2 can be determined to the boundary condition considering in DCM mode.

$$L_1 = L_2 \geq \left(\frac{\frac{2fs}{Rt}}{1-D^2} - \frac{1}{Lf}\right)^{-1} \qquad (2.24)$$

The voltage of C_1 should be a constant value within a switching period. Therefore, the resonant frequency created by elements L_f, C_1 and L_1 i.e. f_r, must be much higher than the grid frequency, f_g and lower than the switching frequency, f_s. Now, C_1 (or C_2) can be expressed as

$$C_{1,2} = \frac{1}{(2.\pi.fr)^2} * \frac{1}{Lf+L1,2} \ ;\ fg < fr < f_s. \qquad (2.25)$$

The output capacitor filter is designed based on output power, P_{out} and the tolerable ripple of the output dc voltage, i.e. ΔV_{out},

$$C_{out} = \frac{Pout}{2\pi\Delta VoutVout^2} \qquad (2.26)$$

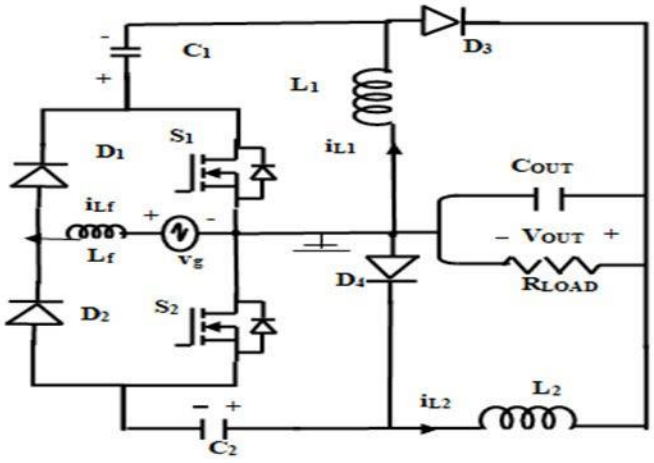


Figure 5.7 Bridgeless Common Ground PFC Circuit

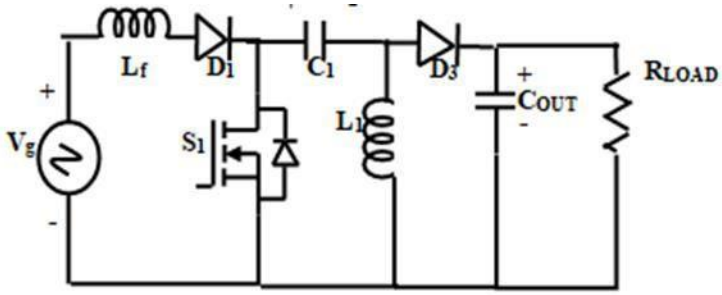


Figure 5.8 SEPIC (operating (during positive half

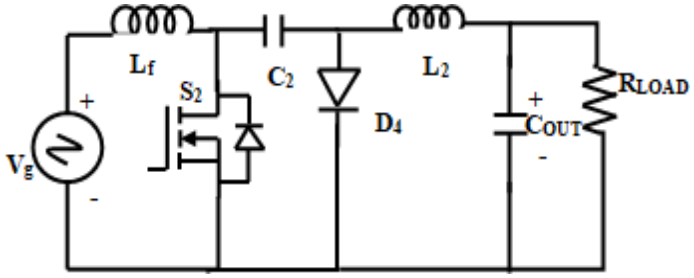


Figure 5.9 CUK (operating during negative cycle)

TABLE 2: SPECIFICATIONS

Parameters	**Values**
Rated power	1.6 [KW]
Switching Frequency (f_s)	50 [kHz]
Grid voltage (V_g)	220 [V] and 50 [Hz]
DC voltage (V_{out})	92-96 [V]
Inductors L_1, L_2	0.2 [mH]
Inductor L_f	1.5 [mH]
Capacitors C_1, C_2	2.2 [uF]
Capacitor C_{out}	20000 [uF]

The simulation is done on a verified platform with a rated power of 1.6 KW. Table 2 shows the specs of the converters as well as the component characteristics. The measured data from the CGBPFCs simulation are examined in this section. The roles of inductors L1 and L2 are switched throughout each half-cycle. L1 operates as a converter side inductor to manage power conversion during the positive half-line cycle. In the proposed converter, L2 operates as a converter side inductor during the negative half cycle. Because L1 and L2 are not active at the same time, they can be placed on distinct limbs of the same magnetic core, increasing power density. The peak value of the input ac voltage is expected to be equal to the maximum capacitor voltage. As the loading resistance decreases, the grid side current increases rapidly in a relatively short period of time. The experimental input and output voltage and current waveforms are shown below. The figures suggest the CGBPFCs' steady-state performance under various system settings. The platforms have been tested using a 220 Vrms input and 96 Vdc output.

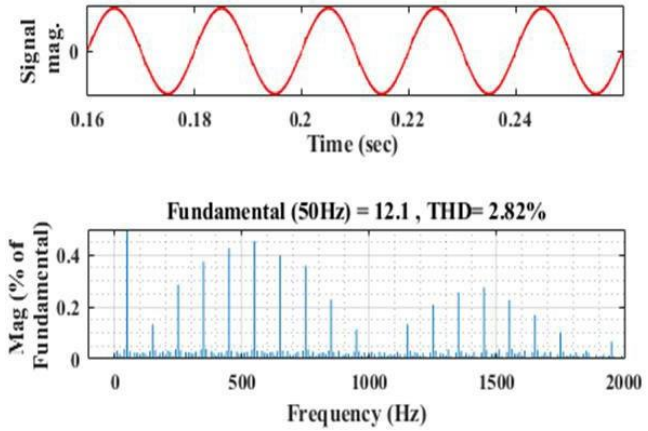


Fig.5.10. Total Harmonic Distortion

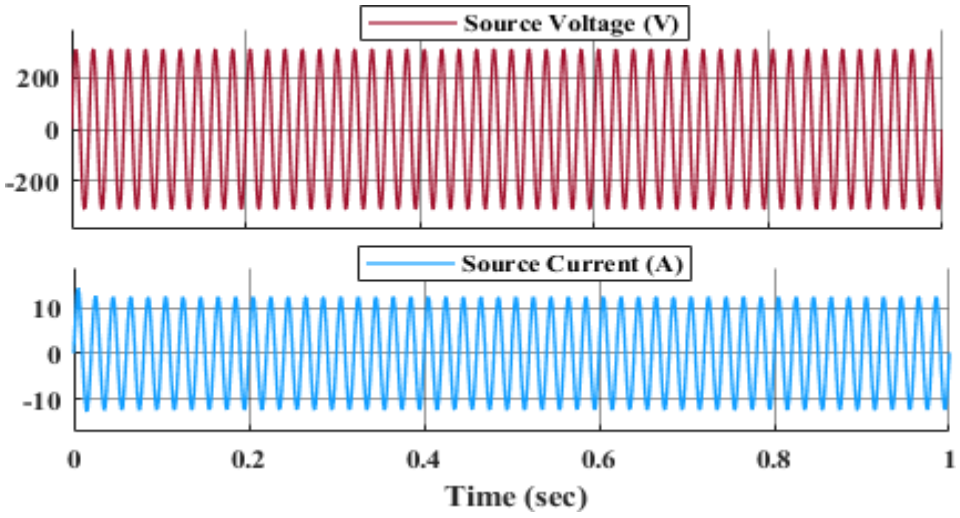


Fig 5.11. Input Voltage in phase with current

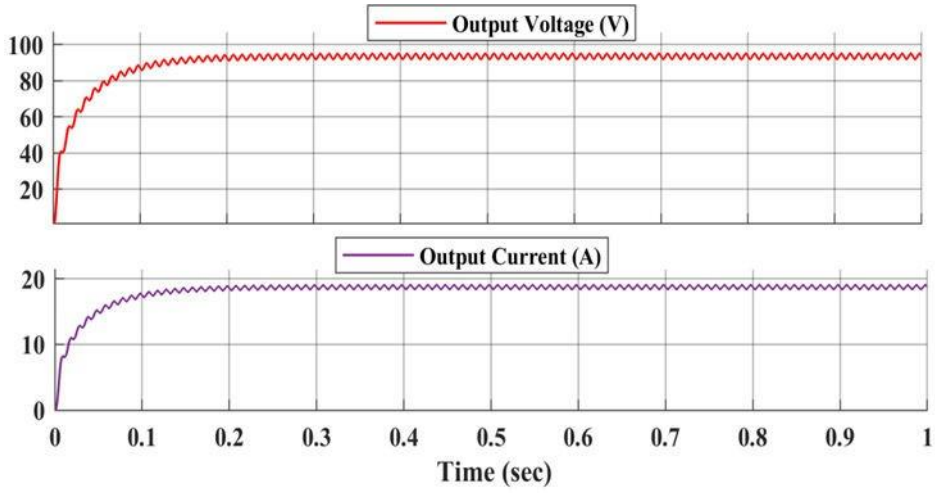


Fig.5.12 Output Voltage and current

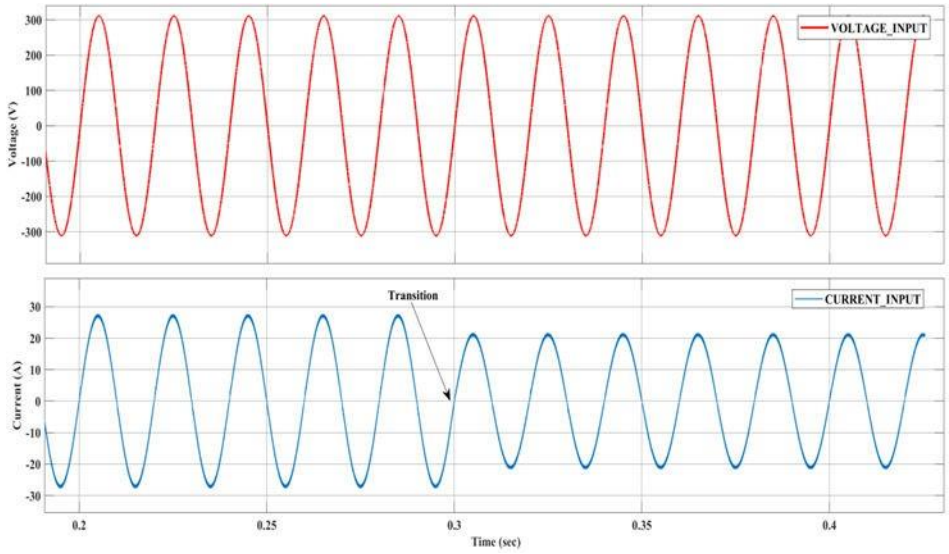


Fig 5.13 Input current under transient changing

At steady-state conditions, all of the figures show consistent performance. The output voltage is regulated to 96 V as shown in fig with a voltage ripple of 2% by automatically altering the duty cycle using the suggested hysteresis current controller,

while a sinusoidal current is received from the ac grid. The input line current is in phase with the grid voltage, as shown in fig 5.10 with a slight harmonic distortion of grid current and output dc voltage ripple. Dynamic performance is shown in fig. The output is maintained at rated capacity here due to the provision of common ground; the circulating current is getting eliminated as explained in literature review under common mode noise analysis.

5.4 Performance evaluation of proposed converter

Table 3 compares some essential elements of the proposed CGBPFC converters to the primary buck-boost bridgeless PFC rectifiers. None of these cutting-edge converter topologies have the proposed CGBPFC's common ground characteristic. The converters in the table are classified according to the four ways utilised for clamping the ac side's ground terminal to the dc side, namely active clamping, passive clamping, active virtual ground, and common ground (which is suggested in this study). The active clamped rectifier suffer from high frequency changes of dv/dt, while the passive clamped converter can mitigate that issue but it requires an external filter to mitigate common mode noise. However, the active virtual ground is based on the hybrid clamped method that uses LCL circuit but addition of extra components is drawback. In contrast to these, the common ground bridgeless PFC are the only with direct connection between ac grid side ground and the terminal of the dc load. It can be inferred from the table that CGBPFC has lowest component count with no dv/dt issue.

Due to the common ground feature, it is eliminating circulating current of the system. Indeed, the THD increases as the load changes due to the sudden change and transients. However, the buck-boost topology along with the common ground provision proves to be efficient and economical since low numbers of semiconductor devices are used.

Performance analysis of buck-boost and boost bridgeless PFC is carried out. Interestingly, both of them are provided with the direct connection of input side to the output side rather than passive or active clamping. Both are treated under 50% load and full load to see the input source current distortions. Buck-boost outperforms boost since the

second harmonics are always carried along in case of boost PFC.

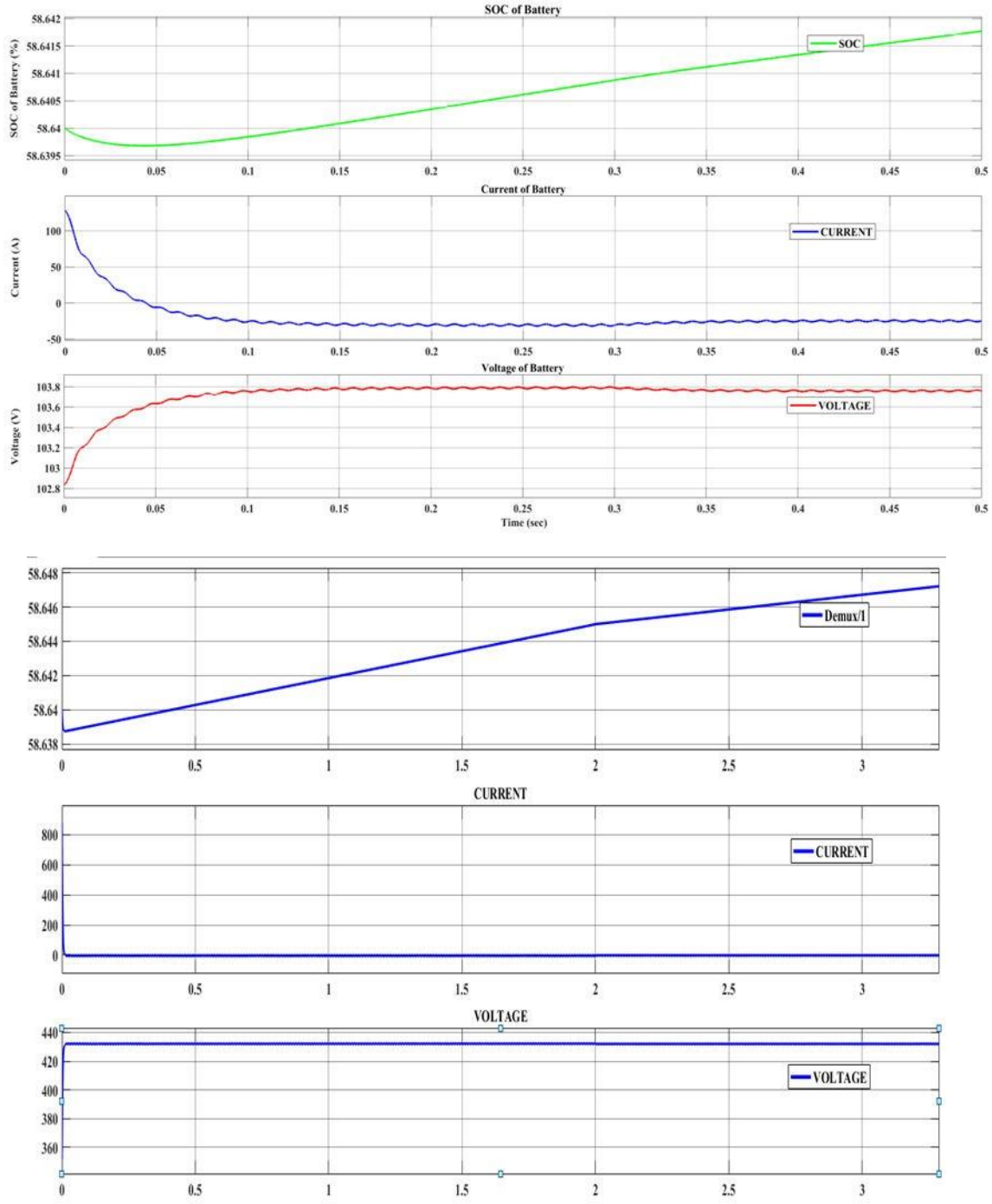


Fig 5.14-15 Comparison of BL-Boost and Buck-Boost charging

TABLE 3: Comparison among main buck-boost BPFC rectifiers

Type of clamping	**No. of Elements**	**No. of state**	**Results**
Active Clamping [10]	2S,2BD,2SD,1FD, 2L,2C	3	THD: 2% $180V_{ac}$ to $150V_{dc}$
Passive Clamping [11]	2S,0BD,2SD,2FD, 3L,4C	2	THD: 2% $110V_{ac}$ to $48V_{dc}$
Active Virtual Ground [17]	4S,2BD,0SD,2FD, 2L,2C	3	THD: 3% $120V_{ac}$ to $48V_{dc}$
Common Ground (Buck-boost)	2S,0BD,2SD,2FD, 3L,3C	2	THD: 2.8% $220V_{ac}$ to $96V_{dc}$
Common Ground (Boost)	2S,0BD,2SD,2FD, 1L,2C	2	THD: 5.13% $220V_{ac}$ to $400V_{dc}$

S: switch, BD: body diode, SD: slow diode, FD: fast diode, L: inductor, C: capacitor

5.4 CONCLUSION

A comparison of two bridgeless converters has been carried out after the explanation of bridgeless topologies. The comparison was mainly on the basis of performance by operating the converter under different load conditions. The performance specifications are tabulated in Table 1 and Tale 2 respectively, whereas the overall comparison is tabulated in table 3. It shows the significant advantage of grounding provision between input and output. Both the boost and buck-boost are modified with this feature. It has been observed even though buck-boost performs better in terms of reliability but common ground indeed brings the advantage such as lesser number of components as well as decent efficiency. The main feature of it is to diminish the circulating current without even the cost of extra passive element.

CHAPTER 6

CONCLUSION

6.1 CONCLUSION

The proposed converter shows exceptional results since it is achieving common ground between input and output by eliminating all the possibilities of parasitic capacitors. Moreover, it yields the results with high efficiency and less number of semiconductor devices. The key observation is the bridgeless configuration, the switches are used on the second line of the bridge that are responsible for shaping the input current as well as providing simultaneous switching to both the converter cells.

Another key point is the converter is not using the body diode to discharge the residue. Both the topologies involved are providing the relevant output. In comparison to the active virtual ground kind of converter, the common ground is accomplished at the expense of one more capacitor and two more discrete diodes. This is a legitimate trade-off to obtain the benefits of common ground. A hysteresis controller was used in the suggested converters to ensure smooth and accurate regulation of the grid side current. Output dc voltage regulation has been successfully demonstrated for both types using the prototype. The proposed rectifiers have a maximum efficiency of 94% at Vdc = 96 V, Vrms =220 V, Pout =1.6 kW, and fs =50 kHz.

The prototype's observed waveforms validated the analysis and operation of the converters. When compared to previously published converters, the advantages of the converters in terms of common grounding, minimizing the dv=dt issue and eliminating the need for the common mode noise filter make them a practical and adaptable architecture.

6.2 SCOPE OF WORK

The future area of work will be to focus on achieving the soft switching zvs condition, since the negative half CUK topology and positive half SEPIC topology in case of modified buck boost bridgeless PFC explained in chapter 5 can both be replaced with ZVS configuration. As a result, the converter's total efficiency improves.

REFERENCES

[1] International Standard, “Electromagnetic compatibility (EMC)-part 3-2: Limits-limits for harmonic current emissions (equipment input current ≤16 a per phase),” IEC Std 61000-3-2:2018, pp. 1–73, 2018.

[2] M. C. Kisacikoglu, M. Kesler, and L. M. Tolbert, “Single-phase on-board bidirectional PEV charger for V2G reactive power operation,” *IEEE Trans. Smart Grid*, vol. 6, no. 2, pp. 767–775, Oct. 2014.

[3] K. K. M. Siu and C. N. M. Ho, "Manitoba Rectifier—Bridgeless Buck–Boost PFC," in IEEE Transactions on Power Electronics, vol. 35, no. 1, pp. 403-414, Jan. 2020, doi: 10.1109/TPEL.2019.2910489.

[4] C. N. M. Ho, R. T. Li and K. K. Siu, "Active Virtual Ground—Bridgeless PFC Topology," in IEEE Transactions on Power Electronics, vol. 32, no. 8, pp. 6206-6218, Aug. 2017, doi: 10.1109/TPEL.2016.2620974.

[5] Z. Chen, P. Davari and H. Wang, "Single-Phase Bridgeless PFC Topology Derivation and Performance Benchmarking," in IEEE Transactions on Power Electronics, vol. 35, no. 9, pp. 9238-9250, Sept. 2020, doi: 10.1109/TPEL.2020.2970005.

[6] K. M. Siu, “Single-phase Single-stage Grid-connected Converters using High Frequency Virtually Grounded Technique,” Ph.D. thesis, University of Manitoba, 2019.

[7] K. M. Siu, “Single-phase single-stage grid-connected converters using high frequency virtually grounded technique,” Ph.D. dissertation, University of Manitoba, Department of Electrical and Computer Engineering,Sept. 2019.

[8] A. A. Fardoun, E. H. Ismail, A. J. Sabzali, and M. A. Al-Saffar, “New efficient bridgeless Cuk rectifiers for PFC applications,” IEEE Trans. Power Electron., vol. 27, no. 7, pp. 3292–3301, Jul. 2012.

[9] M. R. Sahid, A. H. M. Yatim, and T. Taufik, “A new AC-DC converter using bridgeless SEPIC,” in IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society, pp. 286–290, 2010.

[10] M. Mahdavi and H. Farzanehfard, “Bridgeless SEPIC PFC rectifier with reduced

components and conduction losses," IEEE Trans. Ind. Electron. vol. 58, no. 9, pp. 4153–4160, Sept. 2011.

[11] Y.-D. Lee, D. Kim, S.-H. Choi, G.-W. Moon, and C.-E. Kim, "New bridgeless power factor correction converter with simple gate driving circuit and high efficiency for server power applications," IEEE Trans.Power Electron., vol. 35, no. 12, pp. 13 148–13 156, Dec. 2020.

[12] J.-H. Jung, S.-I. Hwang, and J.-M. Kim, "A common-mode voltage reduction method using an active power filter for a three-phase three level NPC PWM converter," IEEE Trans. Ind. Appl., vol. 57, no. 4, pp.3787–3800, 2021.

[13] B. Singh, Sanjeev Singh, A. Chandra and K. Al-Haddad, ―Comprehensive study of single-phase AC-DC power factor corrected converters with high frequency isolation‖, IEEE Transactions on Industrial Informatics, November 2011, Vol. 7, No. 7, pp. 540–556.

[14] M. J. Kosher and R. L. Steigerwald, ―An AC to DC converter with high quality input waveforms‖, in Proc. IEEE Power Electronics Specialists Conference, 1982, pp. 63-75.

[15] J. B. Williams, ―Design of feedback loop in unity power factor AC to DC converter‖, in Proc. IEEE Power Electronics Specialists Conference, 1989, pp. 959-967.

[16] L. H. Dixon, ―High power factor switching preregulator design optimization‖, Unitrode Power Supply Design Seminar Manual, SEM-700, 1990.

[17] L. H. Dixon, ―Average current mode control of switching power supplies‖, Unitrode Power Supply Design Seminar Manual, SEM-700, 1990.

[18] J. P. Noon, ―Designing high-power factor off-line power supplies‖, Unitrode Design Seminar Manual, SEM-1500, Texas Instruments, 2003.

[19] M. O. Eissa, S. B. Leeb, G. C. Verghese and A. M. Stankovic, ―Fast controller for a unity-power-factor PWM rectifier‖, IEEE Transactions on Power Electronics, January 1996, Vol. 11, pp. 1-6.

[20] S. Buso, P. Mattavelli, L. Rossetto and G. Spiazzi, ―Simple digital control improving dynamic performance of power factor preregulators‖, IEEE Transactions on Power Electronics, September 1998, Vol. 13, pp. 814-823.

[21] C. Zhou and M. Jovanovic, ―Design trade-offs in continuous current-mode controlled boost power-factor correction circuits‖, in Proc. High-Frequency Power Conversion Conf., 1992, pp. 209-219.

[22] C. Zhou, R. B. Ridley and F. C. Lee, ―Design and analysis of a hysteretic boost power factor correction circuit‖, in Proc. IEEE Power Electronics Specialists Conference, 1990, pp. 800-807.

[23] Limits for Harmonic Current Emissions (Equipment Input Current ≤ 16 A per Phase), International Electro Technical Commission Standard, 61000-3-2, 2004.

[24] N. Mohan, Power Electronics: A First Course, Wiley, New York, NY, USA, 2011.

[25] Y. Zaohong and P. C. Sen, ―Recent developments in high power factor switch-mode converters‖, in Proc. IEEE-Elect. & Computer Engg., Conf., 1998, Vol. 2, pp. 477-480.

[26] W. Huai, I. Batarseh, ―Comparison of basic converter topologies for power factor correction‖, in Proc. IEEE- SECON'98, 1998, pp. 348-353.

[27] K. Rustom and I. Batarseh, ―Recent advances in single-stage power factor correction‖, in Proc. Intl. Conf. on Indl. Technology (ICIT'03), 2003, Vol. 2, pp. 1089-1095.

[28] C. Qiao, and K. M. Smedley, ―A topology survey on single-stage power factor corrector with a boost type input-current-shaper‖, IEEE Transactions on Power Electronics, May 2001, Vol. 16, No. 3, pp. 360-368.

[29] O. Garcia, J. A. Cobos, R. Prieto, P. Alou and J. Uceda, ―Single phase power factor correction: A survey‖, IEEE Transactions on Power Electronics, May 2003, Vol. 18, No. 3, pp. 749-755.

[30] O. Garcia, J. A. Cobos, P. Alou, R. Prieto, J. Uceda and S. Ollero, ―A new family of single stage AC/DC power factor correction converters with fast output voltage regulation‖, in Proc. IEEE Power Electronics Specialist Conference, 1997, pp. 536-542.

[31] Robert Erickson, Michael Madigan and Sigmund Singer, ―Design of a simple high-power-factor rectifier based on the flyback converter‖, in Proc. IEEE Applied Power Electronics Conference, 1990, pp. 792-801.

[32] Abraham I. Pressman, ―Switching power supply design‖, McGraw-Hill Companies Inc., Second Edition, 1998.

[33] I. Barbi and J. L. Freitas Vieiras, ―A high power factor PWM-ZVS single stage power supply‖, in Proc. HPFC'93 Conf., May 1995, pp. 209-219.

[34] D. S. L. Simonetti, J. Sebastian and J. Uceda, ―The discontinuous conduction mode Sepic and Cuk power factor preregulators: Analysis and design‖, IEEE Transactions on Industrial Electronics, October 1997, Vol. 44, No. 5, pp. 630–637.