HIGH PERFERMENCE ENERGY EFFICIENT CMOS VOLTAGE LEVEL SHIFTERS

A DESSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

MASTERS OF TECHNOLOGY

IN

CONTROL & INSTRUMENTATION

Submitted by:

RAVI NANDAN RAY

Roll No. 2K20/C&I/08

UNDER THE SUPERVISION OF

Dr. Madan Mohan Tripathi

and

Dr. Chaudhry Indra Kumar

ELECTRICAL ENGINEERING DEPARTMENT

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

MAY 2022

ELECTRICAL ENGINEERING DEPARTMENT
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of
Engineering) Bawana Road, Delhi-
110042

CANDIDATE'S DECLARATION

I, Ravi Nandan Ray, Roll No. 2K20/C&I/08, an M.Tech (Control & Instrumentation) student, hereby declare that the MAJOR PROJECT titled **"High performance energy efficient CMOS voltage level shifters"** is submitted by me to the Department of Electrical Engineering, Delhi Technological University, Delhi for the partial fulfillment of the requirements for the award of the degree of Master of Technology, and that this submission is original and not copied from any source without proper citation. This work has never been used to give a degree, diploma associate ship, fellowship, or any other equivalent title or recognition.

Place: Delhi

Date: May, 2022

RAVI NANDAN RAY

ELECTRICAL ENGINEERING DEPARTMENT
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the MAJOR PROJECT titled **"High performance energy efficient CMOS voltage level shifter"** submitted by Ravi Nandan Ray, 2K20/C&I/08 [Electrical Engineering Department], Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of a Master of Technology degree is a record of the project work completed by the student under my supervision. To the best of my knowledge, this work has never been submitted in part or in whole for any degree or diploma at this university or anywhere else.

Date; May, 2022

Place: Delhi

Chaudhry Indra Kumar

Dr. Madan Mohan Tripathi
(Professor)
Electrical Engineering Department
Delhi Technological University
Formerly DCE

Dr. Chaudhary Indra Kumar
(Assistant Professor)
Electrical Engineering Department
Delhi Technological University
Formerly DCE

ACKNOWLEDGEMENT

In this Major Project - II, I have put forth effort. It would not have been feasible without the generous support and assistance of many people and organization. I'd want to express my heartfelt gratitude to each and every one of them. Professor **Dr. Madan Mohan Tripathi** and Assistant Professor **Dr. Chaudhary Indra Kumar** deserve special thanks for their advice and constant supervision, as well as for providing vital project information and for their assistance in completing the project. I'd want to convey my gratitude to my parents and members of Delhi Technological University for their support and encouragement in helping me complete the project.

ABSTRACT

In today's ICs and SOCs, voltage level Shifter (VLS) circuits are commonly employed as interfaces for several voltage domains (SOCs). The major design considerations for high performance level shifters are low power dissipation and low latency. In this dissertation we propose two voltage level shifter designs. The first being, an energy efficient voltage CMOS voltage level shifter. The main purpose of this voltage level shifter is to convert the voltage level from one level to another. We verified our voltage level shifter in ASAP7 7nm Fin-Fet technology. The proposed voltage level shifter is based on differential cascade voltage switch logic, which takes an input voltage in the range of 0.25V to 0.6V and provides an output of 0.7V. Our voltage level shifter improves propagation delay and power dissipation with 48% and 43%, respectively, with recently reported Wilson current mirror voltage level shifter with zero-Vth design. The proposed design technique comes up with significantly lower power consumption and drastically reduced propagation delay over a wide range of temperatures (-25 to 25 degree Celsius), as compared to existing technologies. The secondly proposed design is based on select signal (Vin) voltage switch logic, which takes an input voltage in the range of 0.3V to 0.6V and provides an output pulse of 1.2 to 0.6V peak to peak. We verified our voltage level shifter in ASAP7 7nm Fin-Fet technology. Our voltage level shifter improves propagation delay and power dissipation with 42.76% and 39.6% respectively with recently reported Wilson current mirror voltage level shifter with Zero-Vt design. The proposed design topology comes up with significantly lower power consumption and drastically reduced propagation delay.

CONTENTS

LIST OF TABLES AND FIGURES

List of Tables

List of Figures

CHAPTER – 1
INTRODCUCTION

INTRODUCTION TO CONVENTIONAL VOLTAGE LEVEL SHIFTER

1.1 NEED OF VOLTAGE LEVEL SHIFTER IN VLSI CIRCUITS?

Low power consumption is one of the most important challenges in today's SoC designs in the era of complementary metal-oxide-semiconductor (CMOS) technology. Low power and low output delay are in high demand, especially for mobile devices such as cell phones and tablets. CMOS technology is widely employed in microelectronics circuit systems to address the growing demand for low power consumption and minimal delay operation. With the evolution of CMOS technology, a significant drop in chip size (less than 1 mm2) has been achievable, lowering production costs significantly. The level shifter is an important circuit component in multi-voltage systems, and it is typically utilized between the core circuit and the input/output (I/O) circuit Level shifters are used to change the voltage level of an input signal at the output node to a different voltage level. Power dissipation is the product of voltage and current, as we all know.

$$P = V * I.$$

When we replace I=V/R, this becomes

$$P=V\text{^}2/\ R.$$

We can see that power dissipation in any circuit is directly proportional to the square of the voltage at which that circuit is operating.

The basic solution for this is to reduce the voltage level before doing any logical operation and when once the logical operation is done the voltage can be shifted up to the required range.

1.2 COMPLEMENTARY METAL OXIDE SEMICONDUCTOR (CMOS)

A CMOS is termed as complementary metal oxide semiconductor, there are two kinds of MOS transistors NMOS and PMOS. They are the most popular technology in the world of modern electronics.

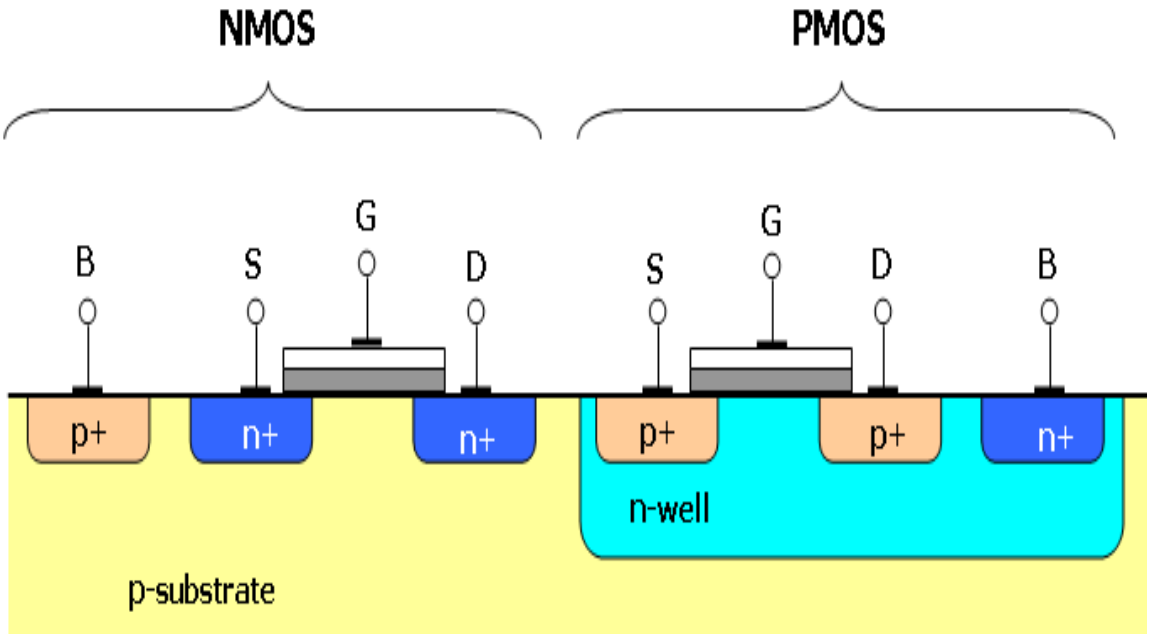

Figure – 1.1 Structure of NMOS and PMOS

The Fig 1.1 shows the internal design and doping of the NMOS and PMOS respectively. The substrates and the doping of the materials are shown here.

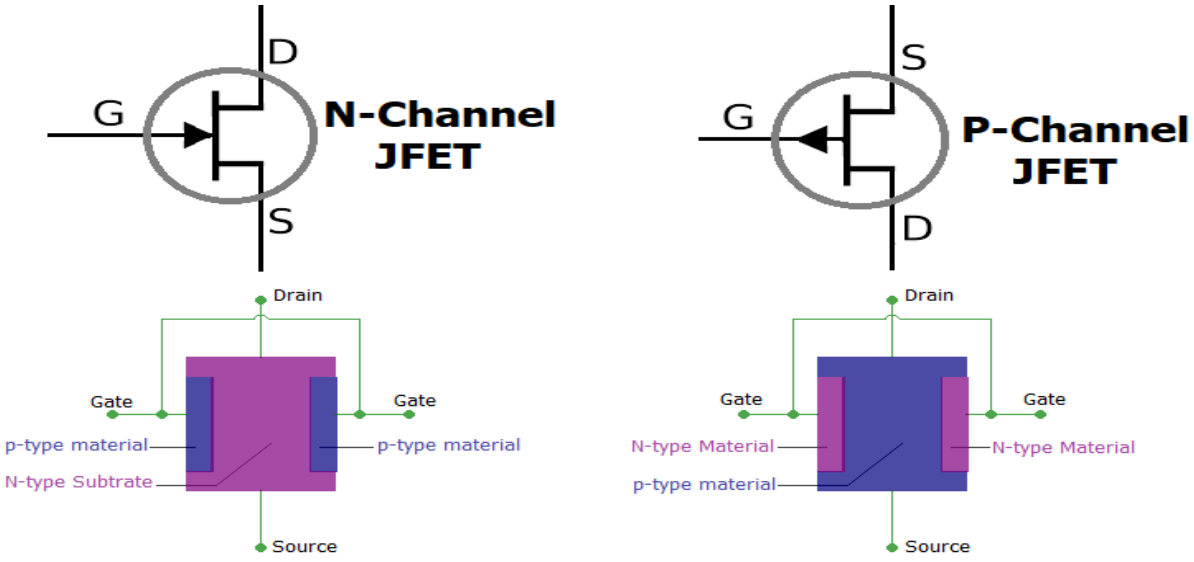

Figure – 1.2 Symbolic representation of NMOS and PMOS

In Fig. 1.2 the symbolic diagram of N-channel and P-channel MOs are shown. This figure also makes us clear with how is the direction of drain current in each of the NMOS and PMOS.

1.3 WORKING OF CMOS INVERTER

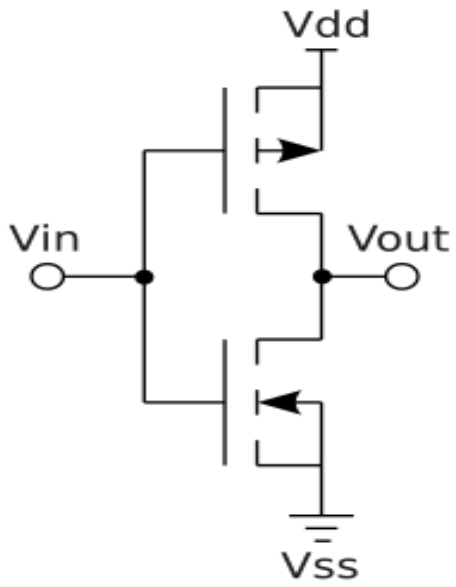

Figure – 1.3 CMOS voltage inverter

The Fig. 1.3 shows us the schematic circuit diagram of a CMOS voltage inverter. In NMOS the channel formed is of electrons whereas in PMOS the channel formed is of holes. The substrate in NMOS is made up of P-type material, whereas the substrate in PMOS is made of N-type material. In NMOS drain current flows from drain to source whereas in PMOS the drain current flows from source to drain. The working of CMOS inverter is as follows:-

1. When the input voltage Vin is kept low (i.e. 0V) both the gate terminals of each of the NMOS and PMOS are exposed to low voltage, which turns ON the PMOS, and hence the output terminal gets shorted with VDD. As a result the obtained output is VDD, i.e. high voltage.
2. When the input terminal is provided with high voltage (1V) both the gate terminals of NOMS and PMOS are exposed to higher voltages, which turns ON the NMOS and the ground terminal is sorted with output terminal. As a result the voltage received at output terminal is low i.e. 0V.

This can be easily seen that the CMOS circuit gives output voltage as 0V when the input is high, and the output voltage is 1V when the input is low. That is where the name comes from. It inverts the input signal given to its input terminal. The output waveform of the CMOS voltage inverter is shown here.

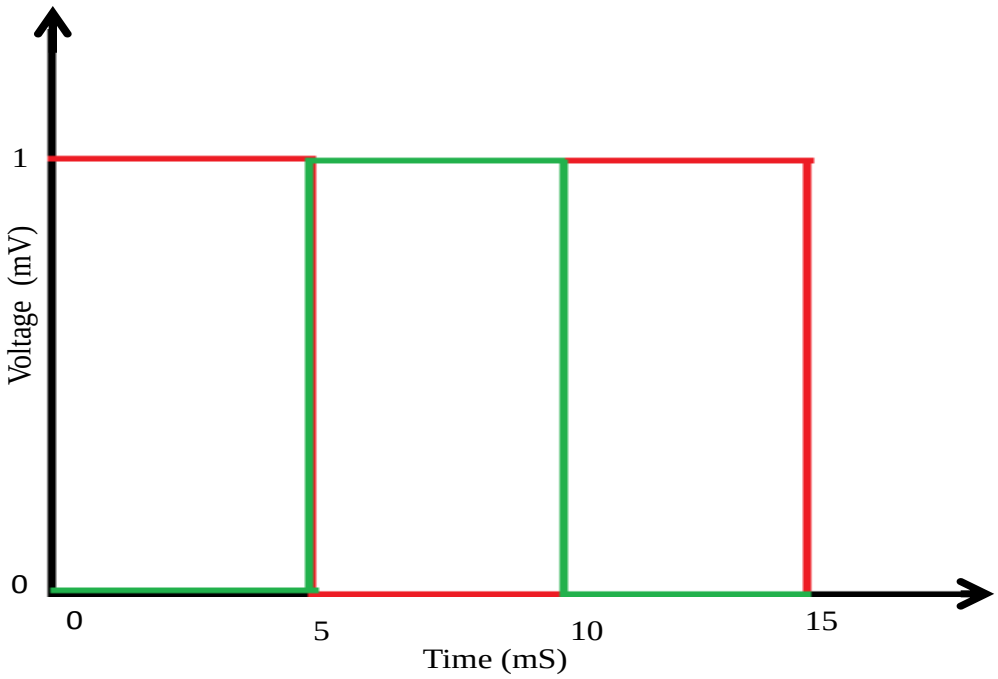

Figure – 1.4 Output waveform for CMOS inverter

The Fig 1.4 shows the output waveform of the CMOS voltage inverter.

1.4 CONCEPT OF VOLTAGE LEVEL SHIFTER

A voltage level shifter cell shifts the voltage range of a signal from one voltage domain to another. When a chip operates in various voltage domains, this is essential. The voltage range of a signal in one voltage domain may differ from that of a signal in another voltage domain. The variation in voltage range could cause the destination domain to malfunction. Hence, in the voltage domain crossings, level shifter cells are used.

A level shifter translates logic signals from one level to another. Usually, this shift takes place between 5V and 3.3V, but you can use other voltages as needed, such as 2.5V or 1.8V. Important specs to look for include:

1. How much the shift may introduce time delay?

2. What voltages are available?
3. Whether shifts take place in one direction or are bi-directional, allowing signals to travel back and forth as needed.

There are two possible situations, one where the source signal voltage is low compared to the sink voltage domain, second one is vice versa. But there can be also situations where dynamic voltage scaling is used and the voltage relation between the source and destination might change over time of operation. In that case we need level shifter which is capable of shifting both low to high and high to low. Accordingly the three types of level shifters are:-

1. Low to High Level Shifters can be realized using a buffer or a pair of inverters. The gate voltage of a MOS transistor can be driven up to its breakdown voltage. Breakdown voltage is the voltage beyond which the dielectric gets damaged irreversibly and no longer exhibits the desired dielectric characteristics. This breakdown voltage is typically much higher than the supply voltage. This means the input of the MOS transistor can be driven with an higher voltage than the supply voltage (provided gate voltage is bellow its breakdown voltage).
2. High to low level shifting can be realized using two CMOS inverters and should be operating on required supply voltages. The CMOS inverters which can be used are similar to those, which are shown in this literature beforehand.

Low to High Level shifter requires a careful transistor sizing. A low voltage signal may not even reach the threshold voltage of the logic cell in the High voltage domain. In this case the level shifter circuit is built by choosing the transistor sizing to bring the threshold voltage down so that the low voltage signal can turn it ON. Also they may increase the GATE thickness to help accumulate the charge better. Traditional Low to High Level Shifter circuit used a cross coupled transistor to amplify the low voltage signal. It consumes more power and introduces more delay. However the designers have come up with many different and efficient ways to implement the Low to High Level Shifter. The circuit implementation of a typical Low to High Level Sifter is show in the picture below.

1.5 CONVENTIONAL CMOS VOLTAGE LEVEL SHIFTER

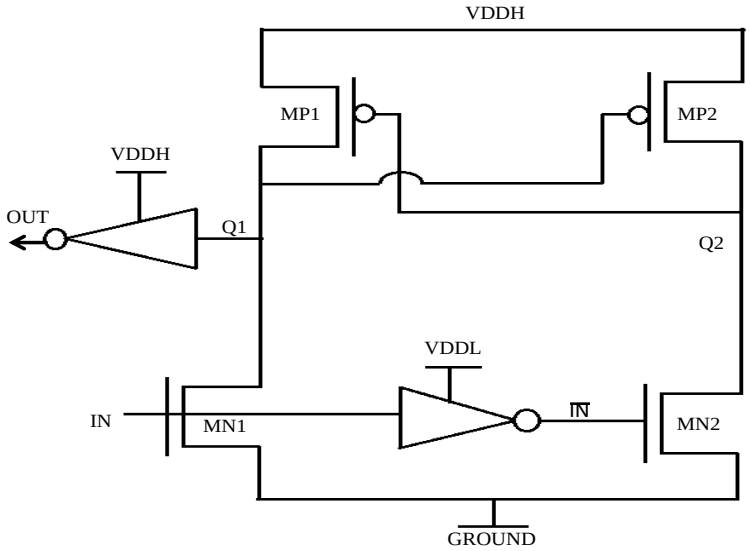

Figure – 1.5 (Conventional voltage up shifter)

As we all know an N-MOS turns on when the voltage at gate is high, where as a PMOS turns on when the gate voltage is low. We will follow this thought the detailed working of voltage level shifters.

1. When the voltage Vin is low the P-MOS Mp1 will be turned on, which means Vinb is now Vddi, when this vddi is given at the gate of Mn1 it turns on, and at the same time vddi turns on Mn3 so the voltage at the gate terminal of Mn4 is low, hence it remains in off state. But turning on of Mn1 turns on Mp4 as the ground is now directly connected to the gate terminal of Mp4 which makes. This process shorts the nodes Vddo with the output node and hence the Vout becomes equal to Vddo.
2. Now considering the second case, when Vin is high, it directly turns on Mn2 making Vinb go low, which turns off Mn1 and Vinb being low turns on Mp2, which makes the voltage at the gate terminal of Mn4 go high and equal to Vddi. Which turns on Mn4 and so the output voltage goes to 0V.

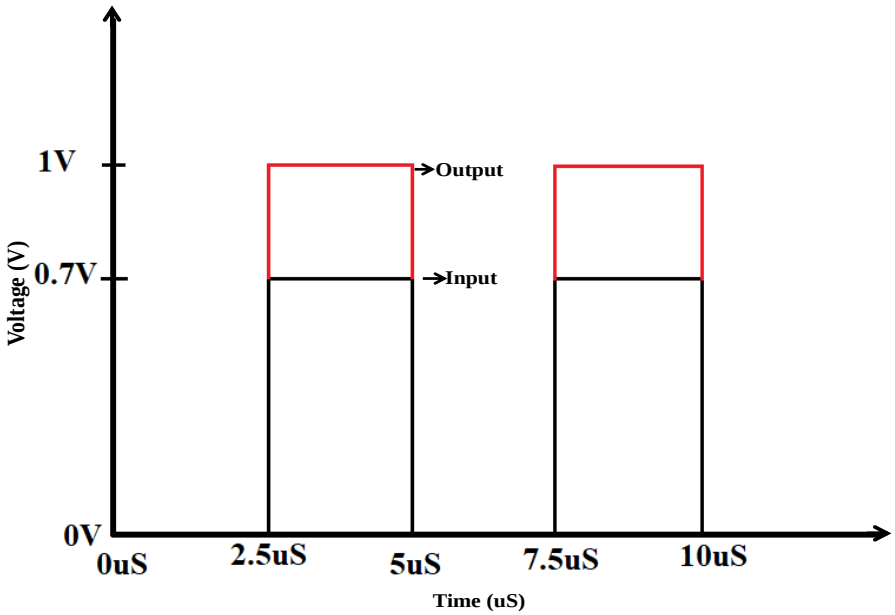

Figure – 1.6 (Output of conventional level up shifter)

1.6 CONVENTIONAL VOLTAGE LEVEL DOWN SHIFTER USING CMOS

1. When VIN is low MP1 turns on which makes MN2 turn on and the output voltage becomes 0V.
2. When VIN is high MN1 turns on which makes MP2 turn on and the output voltage becomes VDDL.

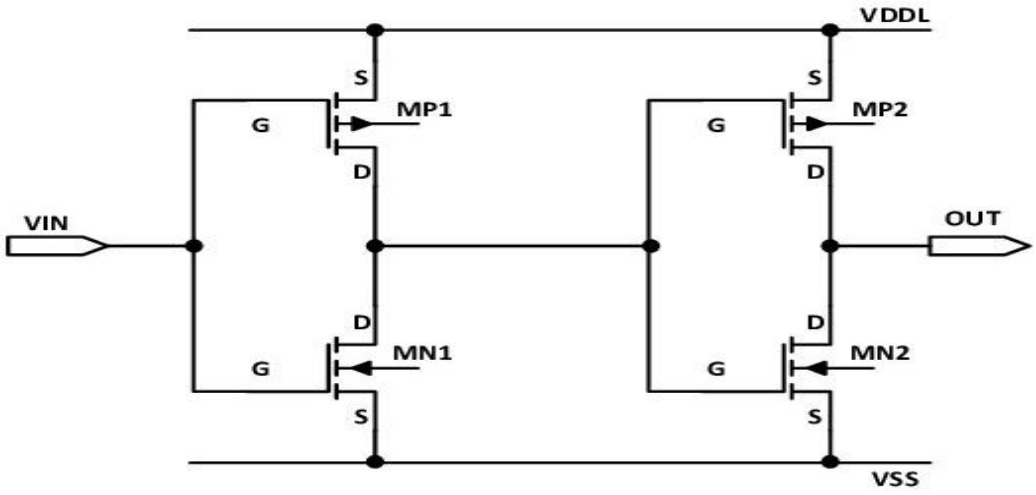

Figure – 1.7 (Conventional voltage down shifter)

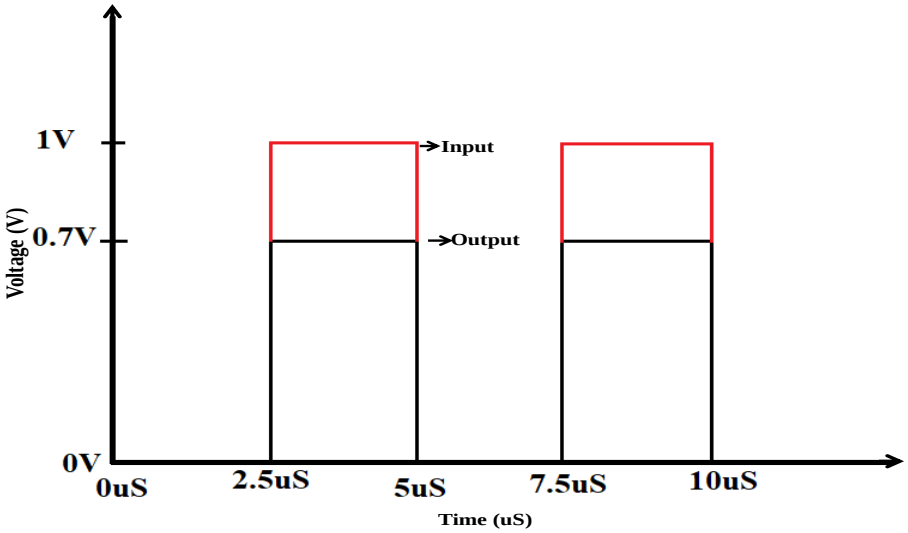

Figure – 1.8 (Output of convention down shifter)

As we know the conventional voltage level up shifter shifts the input voltage to the provided or designed level, when given a high voltage. Similarly a CMOS voltage down shifter shifts the input voltage to a desired level lower than the input voltage when it is provided with an input of 1V. Hence seeing the operation and various output waveforms of conventional level shifter, what we can easily say is a level shifter translates logical signals from one voltage level to another, and you are going to read various designs of CMOS voltage level shifter, which are more power as well as delay efficient than the conventional ones.

CHAPTER – 2

LITERATURE REVIEW

2.1 INTRODUCTION

For interfacing between two chips, we use a voltage level shifter. Nowadays electronic gadgets require a power efficient operation, for this requirement, improvement and optimization in the operation of system on chips (SOCs) is needed, especially considering reduction in propagation delay and power dissipation as the significant optimization parameters. Hence, the use of power efficient and minimized delay voltage level shifters is required now days. In literature various techniques are used to design a power efficient voltage level shifter.

2.2 LITERATURES

In **[1]** a CMOS voltage level shifter is presented, which uses a multiple-threshold voltage technique. In **[2]** the back gate of transistors can also be taken into use to reduce the threshold voltage of the transistor, to reduce the static power consumption. In **[3]** the supply voltage can be scaled down and the whole circuit can be operated in near threshold voltage regime. In **[4]** the input supply voltage can be used as select signal and a multiplexer can be added in the conventional design for further optimizations. A regulated cross coupled structure in the pull up region can be utilized for further reduction in static power consumption is presented in **[5].**

In **[6]** the design of conventional voltage level shifter using six, eight, ten transistor configuration is further used in optimization regards. The circuit diagram of the conventional voltage level shifter **[7]**. The combination of multiple - threshold CMOS technique with novel topological modification can be made to operate on wide range of voltages. In **[8]** Further optimization in circuital operations is done keeping in mind the circuit area of the device. In **[9]** The voltage level shifter can be made more energy efficient by combining the various circuital topologies to make the shifter more robust. In **[10]** a single supply voltage level shifter is modified using N-MOS to reduce the power dissipation. In **[11]** a reflected output Wilson current mirror topology with extremely high sizing ratio has been used for optimization of level shifter. In **[12]** a conventional level shifter design topology combined with multi threshold CMOS technology can also be used for voltage shifting process optimization.

In **[13]** this voltage level architecture is based on the single stage differential cascode voltage switch scheme which also makes use of the self-adapting pull up network for operational optimization of the voltage shifter. Two deferentially switched cascoded transistor ladder topology is presented in **[14].**

In **[15]** analog circuit technique has been used with standard zero-Vt NMOS transistor for reducing the power consumption.

In **[16]** a high voltage driver has been designed on basis of stacked-standard low-voltage C-MOS, the designed circuit uses a 65nm TSMC technology. The nominal voltage is 2.5V without any passive elements. The design proposed in **[17]** is based on DC-DC buck converter. All the technologies are based on 55nm technology.

In **[18]** a passive phase shifter has been proposed based on 130nm C-MOS technology. The fabrication matrix includes 12 transistors, which are controlled by different gate voltage levels. A novel red-hard design has been proposed for ultra-low power operations, which is immune over wide range of input voltages **[19].** In **[20]** a novel wave modulator has been proposed which works on the principle of single pole double throw (SPDT).

In **[21]** a novel phase shifting topology has been proposed based on 180nm TSMC technology. A compact and optimized fabrication size can be achieved using this design topology. In **[22]** bias temperature instability (BTI) aging has been evaluated to optimize the propagation delay as the major parameter in the phase as well as level shifting model. In **[23]** an analog to digital converter along with split-capacitor switching has been designed, and a level shifter which consumes less energy and is more power efficient has been proposed.

In **[24]** a level shifter circuit has been proposed which can handle extremely low supply voltages. The circuit design is based on the logic error generation, which is obtained by comparing the input and output voltages. In **[25]** a passive level shifter has been proposed, which makes use of diode-based voltage clamping technique. In **[26]** a bio-signal sensor based on motion artifact reduction is proposed for a modern sleep monitoring system. Adaptive DC control level (ADLC) has been taken in to use for adjusting the DC signal levels for prevention of signal saturation due to enlarged motion artifacts.

In **[27]** Multi dynamic input voltage has been used for dynamic power reduction in integrated circuits. A novel design for level shifter has been proposed which turns off the idle level shifter and gives an alternate path for the current to flow for optimized performance of

voltage level shifter. In **[29]** a phase shifter based on 40nm CMOS technology has been proposed for phase array applications. This takes in to use quadrature signals available to us from the I/Q mixers.

In **[30]** a modification has been done on conventional level shifter to extend its operational range down to sub threshold regime. Transistor stacking and channel stretching has been used to reduce the leakage current.

In **[31]** the proposed level shifter topology optimizes various parameters such as propagation delay as well as power delay product (PDP). The design takes into use IBM 130nm CMOS technology. The working principle along with the schematic circuit has been shown below.

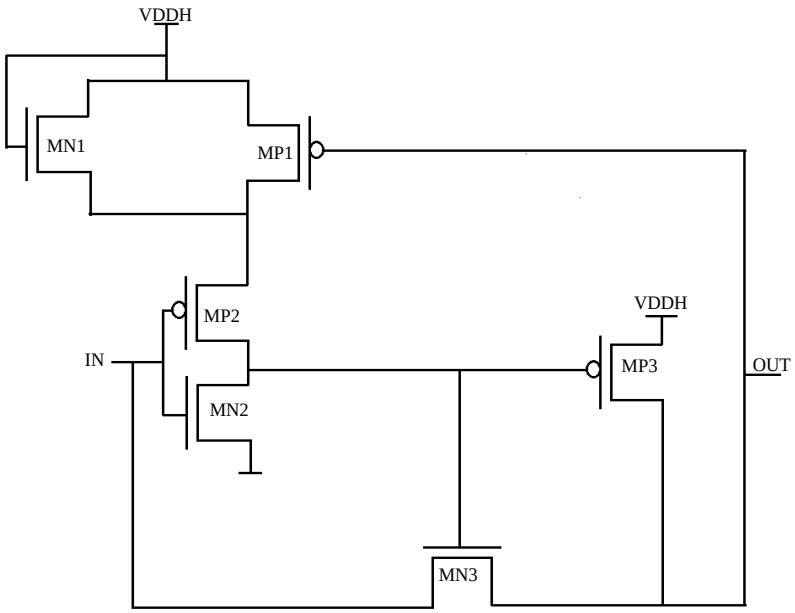

Figure – 2.1 (Energy efficient level shifter)

The Fig.2.1 shows the schematic circuit diagram of energy efficient voltage level shifter. The MP2 and MN2 input level inverters are used to create a virtual VDDL, and hence the proposed level shifter is also based on a single voltage level supply. The PMOS transistor MP3 is used here as a pull up transistor

.In **[32]** this paper introduces us to capacitive floating level shifter. All the transistor simulation makes use of 65nm CMOS technology process. In **[34]** a simple approach for implementation of rail-to-rail operational amplifiers has been shown, which makes use of switch voltage followers. All the simulations are based on 0.5um CMOS technology process. In **[35]** a new and optimized inverter has been proposed based on level shifter. All the processes are based

on 0.18um CMOS technology. In **[36]** a novel level shifter circuit topology has been implemented using 0.35um CMOS technology. To reduce various parameters like propagation delay and power consumption a closed loop negative feedback technique has been employed. In **[37]** thin gate-oxide devices have been employed to derive a novel level shifter topology which is based on 65nm CMOS technology. The proposed topology is operational at 800MHZ and has low static power consumption. In **[38]** low voltage architecture for level shifter has been proposed, which works on 130nm CMOS bulk process, an assist circuit has also been proposed to make the operation furthermore optimized. In **[39]** a two-level driver circuit is proposed to drive ultrasonic transducers, which is based on 0.18 um HV SOI CMOS technological process. In **[40]** a high-voltage driver chip has been proposed for micro pixelated LED display, the simulations are based on 0.18um CMOS technological processes. In **[41]** a dual supply voltage level shifter has been proposed based on Wilson current mirror concept. The proposed level shifter design works in two stages i.e., input and output stage. This design has been used for comparison to our proposed model, hence its brief explanation is necessary. The design along with its working, operation and schematic diagram is explained here.

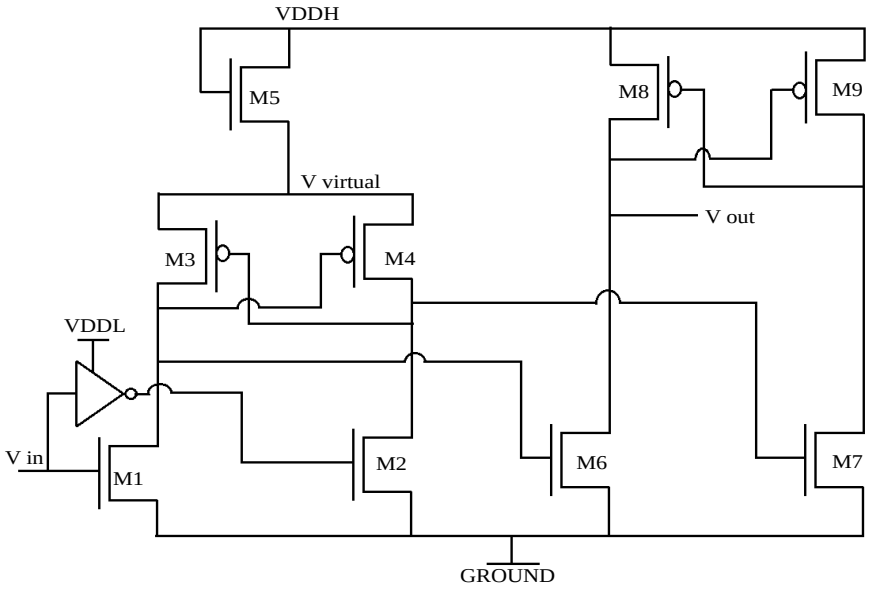

Figure – 2.2 (Dual supply model)

The Figure-2.2 shows the circuital diagram of dual supply voltage level shifter. This design works in two different stages, the first stage is a cross-coupled latch along with diode connected N- MOS M5, which is used to make drop of threshold potential Vt from source voltage to cross-coupled differential latch circuit. The sole purpose of the second stage is to

convert the output of the first stage to full swing output. This kind of circuit design brings in the use of diode-connected N-MOS to create a high threshold potential pull-up P-MOS in order to increase the strength of the input stage N-MOS for input signal conversion. So, the numbers of transistors required are large, hence decreasing the speed of operation of the overall circuit. Two supply voltages are also required further increasing the overall cost of the system.

In [42] a single or mono supply voltage level shifter is proposed. The voltage drop across the gate-drain terminal of an NMOS transistor is used to obtain VDDL from VDDH. The brief explanation and working of the proposed design is shown below, along with its schematic design.

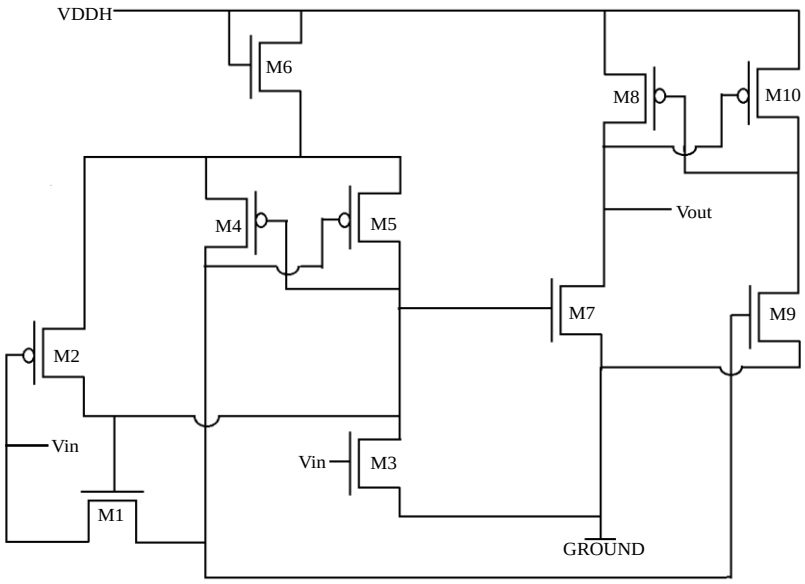

Figure – 2.3 Mono supply model

The Figure – 2.3 shows the schematic circuit diagram of a mono (single) supply voltage level shifter. The V_{DDH} is one and only supply voltage used for the voltage shifting process. The threshold voltage drop across N-MOS M1 is used to provide VDDL to the input stage inverter. Its implementation leads to reduction in terms of pin count and the overall cost of building the system, but this model does lacks in optimizing the parameters like propagation delay and power dissipation.

In **[43]** a high speed voltage level shifter is proposed, which makes use of feedback loops and thick gate-oxide layers for various devices for optimization of the proposed model. The working and operation of the model along with the schematic diagram is shown here.

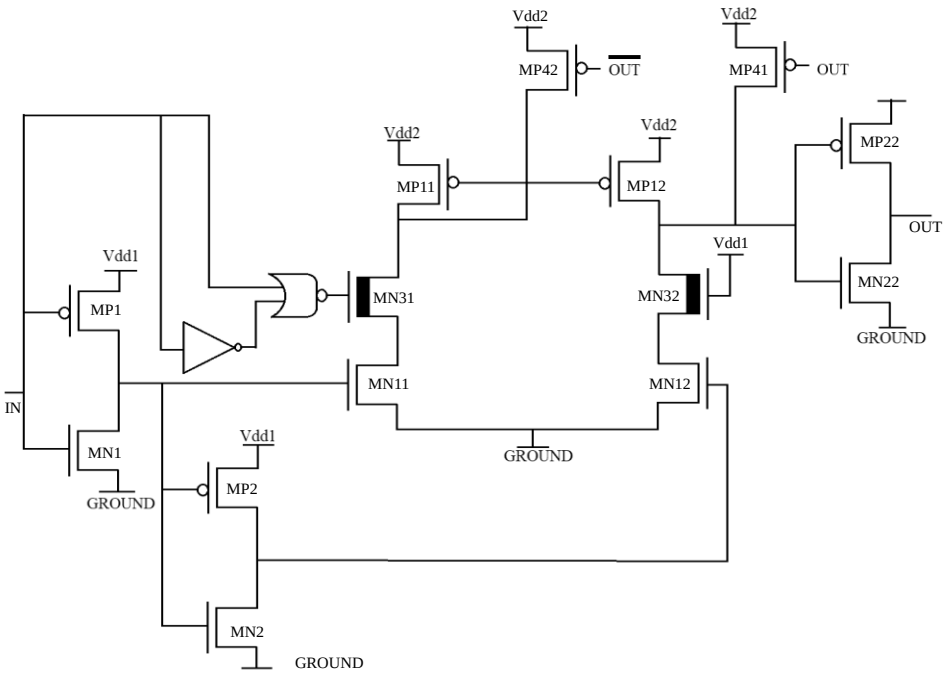

Figure – 2.4 High speed model

The circuit design of high-speed voltage level shifter is shown in Fig. 2.4, which can operate on core voltages, even lower than 1V. Thin gate-oxide layer transistors are used at the input stage. MN31 and MN32 are thick gate-oxide layer zero-Vth transistors. When input voltage is high, MN11 turns OFF and MN12 turns ON and MP11, MP12 are turned OFF, the node D is discharged, and the inverted output Y is VDD2. Whereas, when input voltage is low, MN11 turns ON and MN12 turns OFF, as a result node C is discharged, which in return turns ON MP12, as a result the node D is charged to a potential of VDD2, and the inverted output Y is 0V. But this circuit design is not area efficient, and also requires the implementation of logic gates, which makes the layout furthermore complex. The high-speed design of the level shifter shown in previous designs does not work for the input voltages less than or equal to 0.6 volts, due to thick gate-oxide layers being used. So, it's comparison with the proposed level shifting design is not possible, either considering power dissipation or even the propagation delay as the comparison parameters. Thus, all the comparisons involved in this paper do not consider the high-speed level shifting model.

In **[44]** the proposed design is called dual current limiter voltage level shifter, it is based on stacked Wilson current mirror. The schematic along with its working is shown below, as it has been used to compare it with our proposed design. Fig – 2.5, shows the schematic circuit diagram of dual current limiter voltage level shifter design. When input is low (0V), MN5 will

be in OFF stage, and MN6 will turn ON, which leads to turning ON of MP1. Consequently, VDDH is pulled to the gate terminals of MN1 and MN2, which turn them ON, resulting in the provision of VDDH provided at the input of output stage inverter which gives low (0V) output. Whereas, when input is high (1V), MN5 turns ON, and the input terminal of the output stage inverter gets provided with 0V and gives an output of VDDH. The design is complex and requires large number of transistors, further making the fabrication area large.

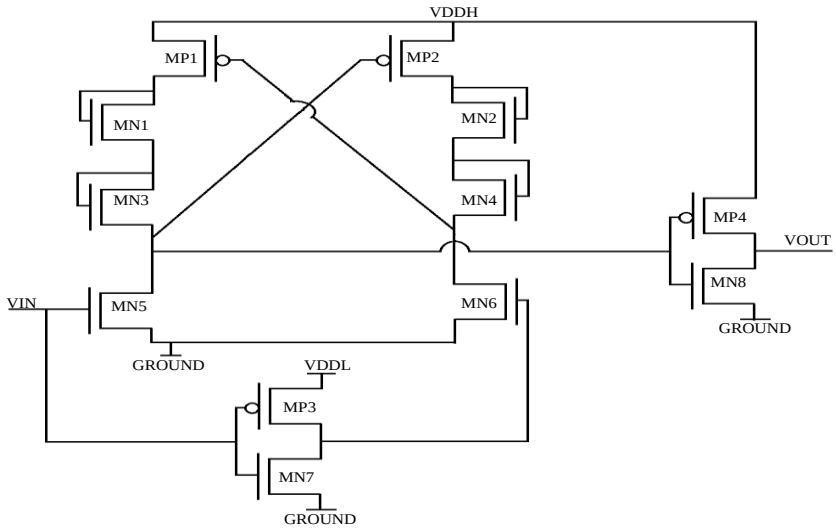

Figure – 2.5 Dual current limiter model

In **[45]** a low power operational level shifter has been proposed, this design has also been used to make comparisons with our proposed design. The design along with its schematics and its working has been explained below.

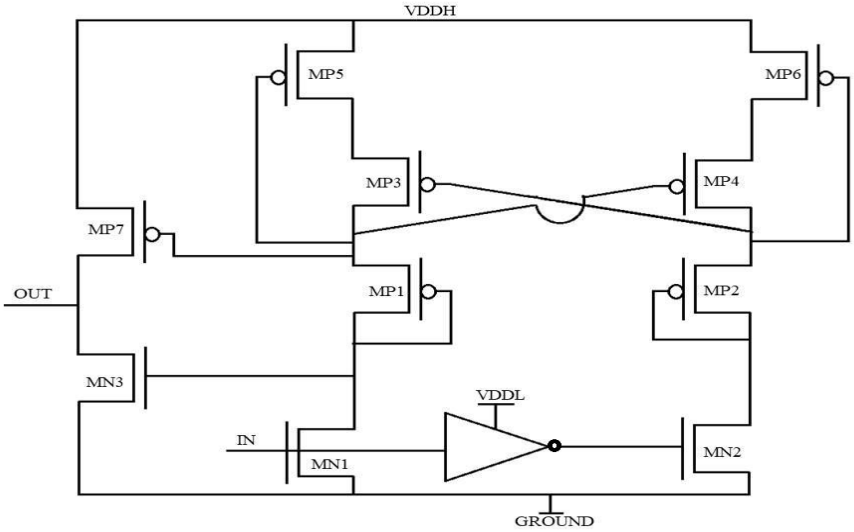

Figure – 2.6 Low power voltage level shifter

The Fig.2.6 shows the circuital diagram of low power design of voltage level shifter. If input voltage is high (1V), NMOS and PMOS transistors MN1 and MP1 turn on respectively. As a result, the voltage at the gate terminal of MP7 is low, which turns ON MP7 and the output voltage obtained is VDDH. Whereas, if the input applied voltage is low (0V) MN2 turns ON, which turns ON MP2, as a result MP3 is turned ON. MP5 also turns ON, because the gate terminal of MP5 was discharged to 0V in the last peak of the input voltage. Hence turning On of MP5, MP1and MP3 transistors pull VDDH tothe gate terminal of MN3, hence MP3 transistor turns ON and the output obtained is low (0V).

In **[46]** a select signal input voltage level shifter has been proposed, which is mainly consisting of two parts. The working along with the schematic circuit diagram of the proposed voltage level shifter. The Fig.2.7 shows the circuital diagram of the level shifter under discussion. When Vin is low (0V), MN2 turns ON. As a result ground voltage 0V is pulled to output terminal Vout. Whereas when Vin is high (1V), MN1 turns ON, which turns ON MP2. Vin being 1V, MN4 is in ON state, which makes VDD equal to VDDL. As MP2 is turned ON the VDD being VDDL is pulled to the output terminal and Vout becomes VDDL.

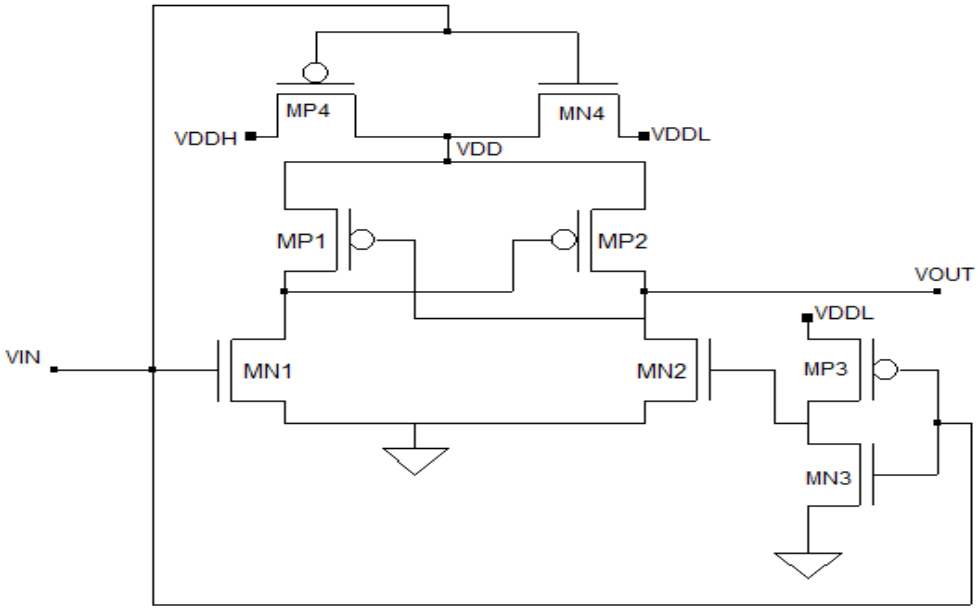

Figure – 2.7 Select signal voltage level shifter

CHAPTER – 3

CROSS COUPLED LEVEL SHIFTER

3.1 HIGH PERFORMANCE ENERGY EFFICIENT CMOS VOLTAGE LEVEL SHIFTER

The schematic diagram of the proposed voltage level shifter is shown in Fig3.1. The proposed design is based on the differential voltage cross - coupled C-MOS load. In our design we have used only single supply voltage (VDDH). Consequently, our design eliminates the drawback of dual supply voltage as compare the existing design techniques.

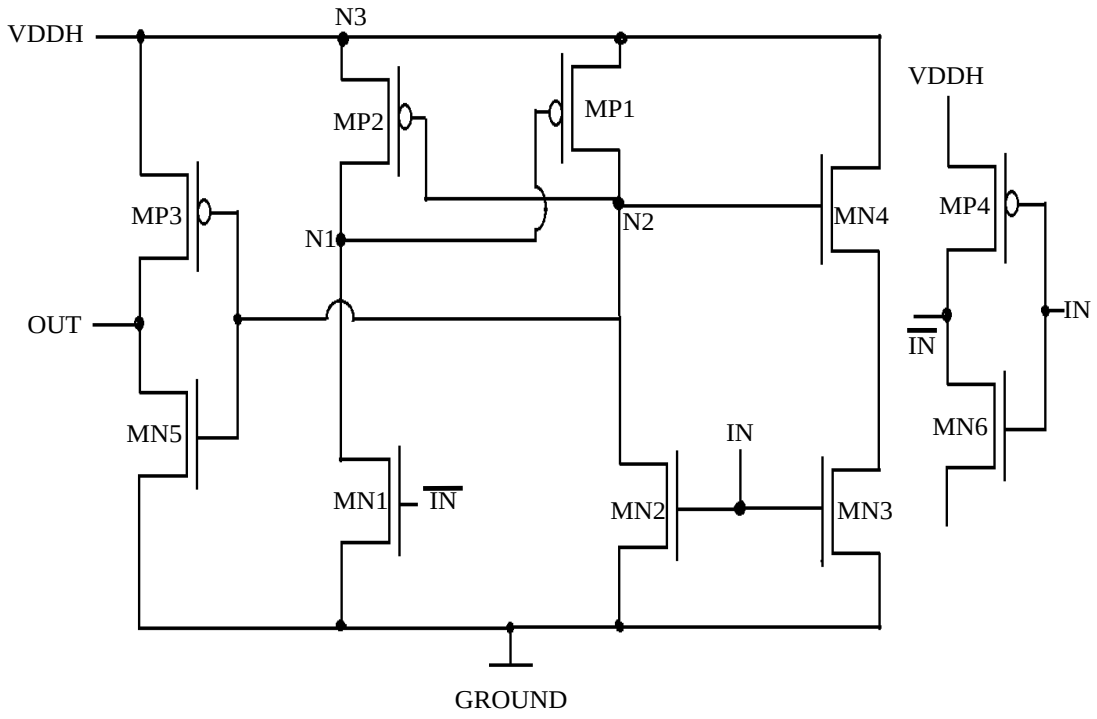

Figure – 3.1 Proposed CMOS voltage level shifter design

In our design, we have used 10 MOSFETs, MN1-MN6 transistors are NMOS and MP1-MP4 transistors are PMOS. The MN6 and MP4 transistor employ an inverter which is used to provide the inverted input signal (IN bar) to our design. Now, we will discuss the operation of proposed voltage level shifter. When the input voltage (IN) is low i.e. (0V) MN2 and MN3 transistors are in OFF state, while MN1 transistor turns ON, as a result Node N1node is discharged, hence MP1 transistor turns ON. Consequently, N2 node starts charging through

transistor MP1. Now N2 node is at logic 1 (VDDH) which is capable to turn ON transistor MN5, as a result, we get a zero potential at output terminal. Which in turn charges node N2, which is attached as the supply voltage to the output stage CMOS inverter. The charged node N2 turns ON MN5, and as a result the output potential obtained is 0V. When the input voltage is high (i.e., VDD), both MN2 and MN3 transistors are turned ON, while and MN1 transistor turns OFF. Consequently, N2 node discharges which results MP2 transistor turns ON, Node N1 starts charging because MP2 turns ON as a result MP1 transistor turned OFF. Due to MP1 transistor turning OFF, N2 node discharges completely as a result MP3 transistor turns ON. Consequently, we got a high logic (i.e., VDDH) at output node.

3.2 SIMULATION AND RESULTS

Cadence Virtuoso tool is used for circuit performance and validation. In Cadence simulations, we have used ASAP7 7nm Fin-Fet technology. We have verified the proposed level shifter at different voltage levels (0.25 to 0.5V). Fig.3.2. shows the simulated waveforms of the proposed level shifter for different voltage levels. In simulations, we verified our voltage level shifter at different voltage levels, which range from 0.25V to 0.5V with a step size of 0.05V.

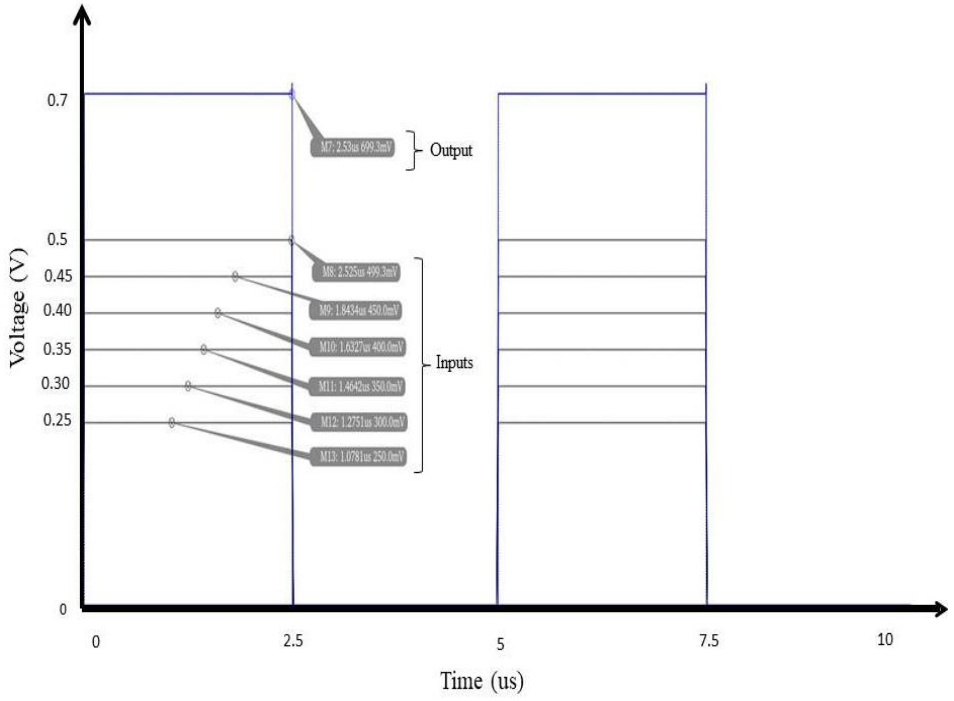

Figure – 3.2 Output waveform of the proposed voltage level shifter design under various input voltages

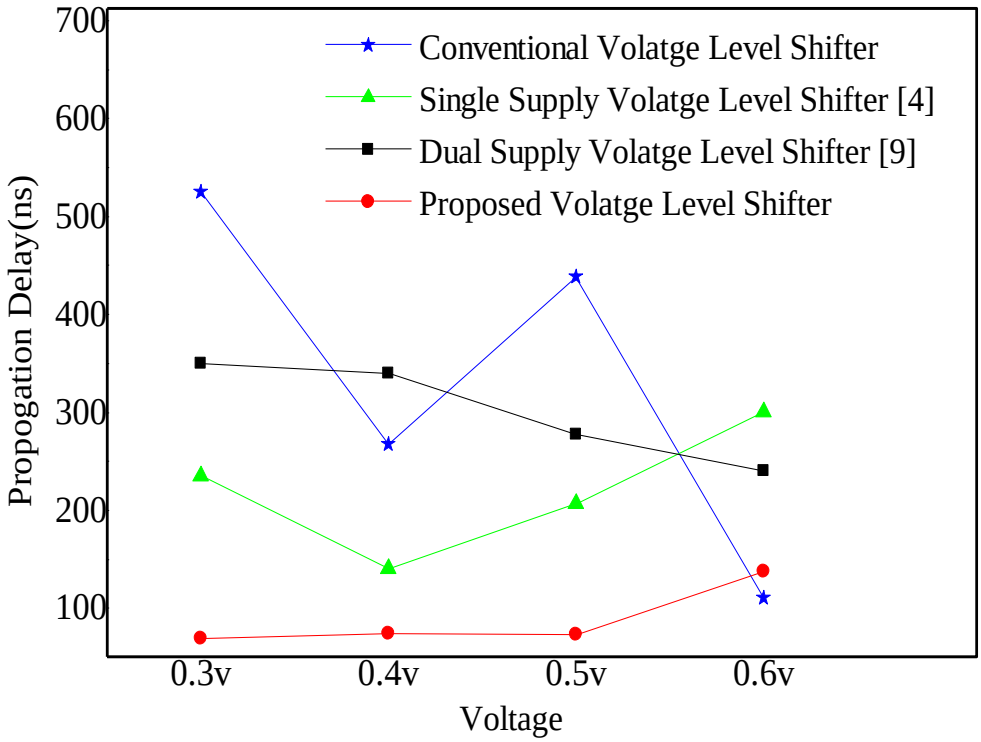

Figure – 3.3 Propagation delay comparison of different voltage level shifter at different power supply voltages

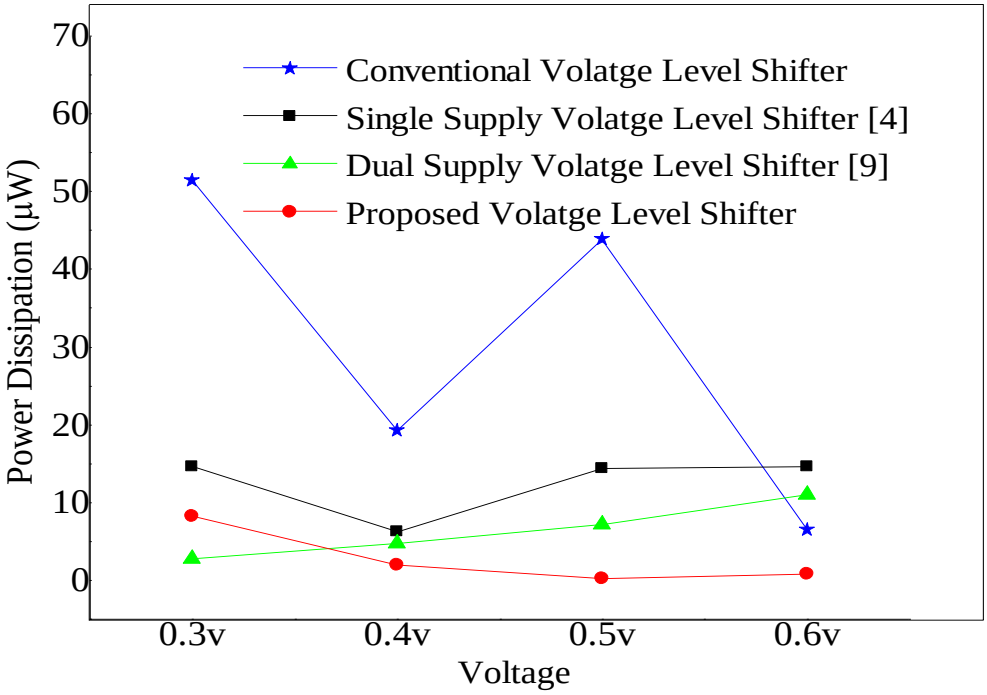

Figure – 3.4 Power dissipation comparison of different voltage level shifter at different power supply voltages

The comparison of propagation delay at different voltage levels of the proposed level shifter with the reported level shifters is shown in Fig.14. From the simulation results, it is observed that, at all voltage levels (0.3 to 0.6V) the proposed voltage level shifter design shows less propagation delay, in comparison to existing voltage level shifter designs.

Fig.3.4 contains the power dissipation curve of the proposed level shifter design. The power dissipation in ON and OFF states are 1.98uW and 917.15pW respectively, which is comparatively lesser than the previous level shifter designs, at the supply voltage equal to 0.4V. From Fig.8, it is observed that, at all voltage levels (0.25 to 0.5V) the proposed voltage level shifter design shows minimum power dissipation, as compared to reported voltage level shifter designs.

Fig.3. shows the graphical comparison of the propagation delay of proposed voltage level shifter with existing designs at different temperature ranges. From Fig.3.5 we can see that the delay provided by the proposed design is much lesser than the existing designs of voltage level shifter.

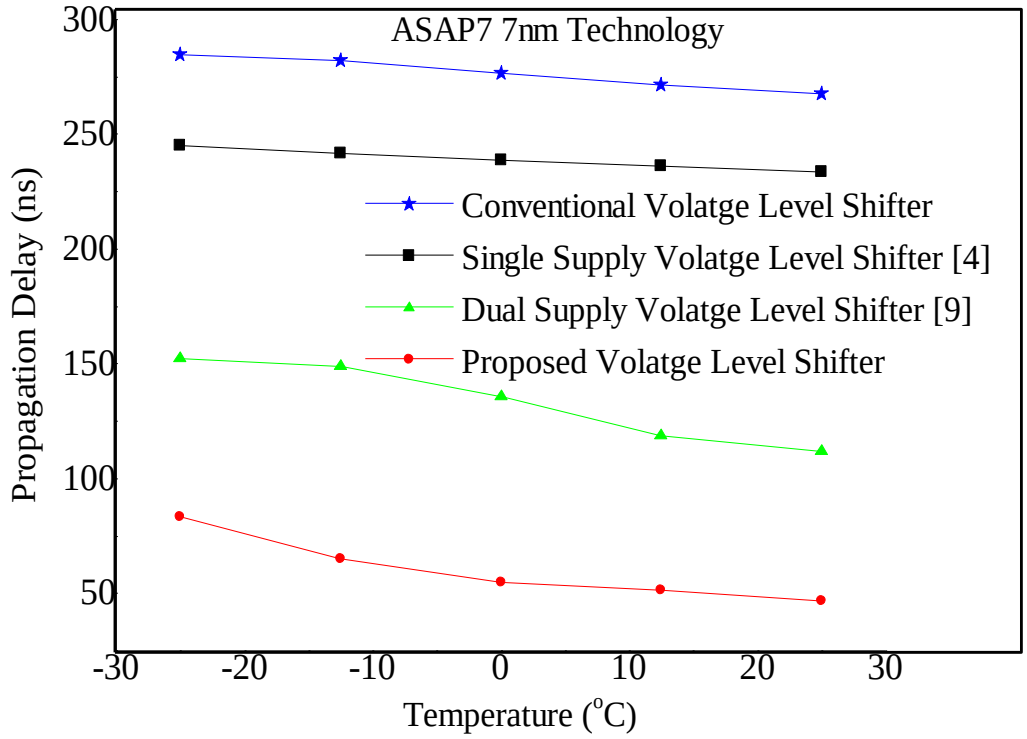

Figure – 3.5 Propagation delay comparison of different voltage level shifter at different temperatures

Fig.3.6 shows the power dissipation of various voltage level shifter designs over a wide range of temperature i.e., from -25 to 25 degree centigrade, when the input voltage provided, is

0.4V. It can be seen clearly in the graphical representation that proposed voltage level shifter design consumes lesser power in comparison to already existing voltage level shifter designs.

After comparison we say that the proposed design is much more power efficient as well as involves significantly lesser propagation delay in different voltages and temperatures.

The peak power consumed by conventional level shifting model is 19.29uW, and the power consumed by single supply voltage level shifter is 6.24uW, the dual supply model consumes 4.81uW power and provides a delay of 339.48uS, whereas our model consumes only 1.98uW in ON stage and even lesser in OFF stage.

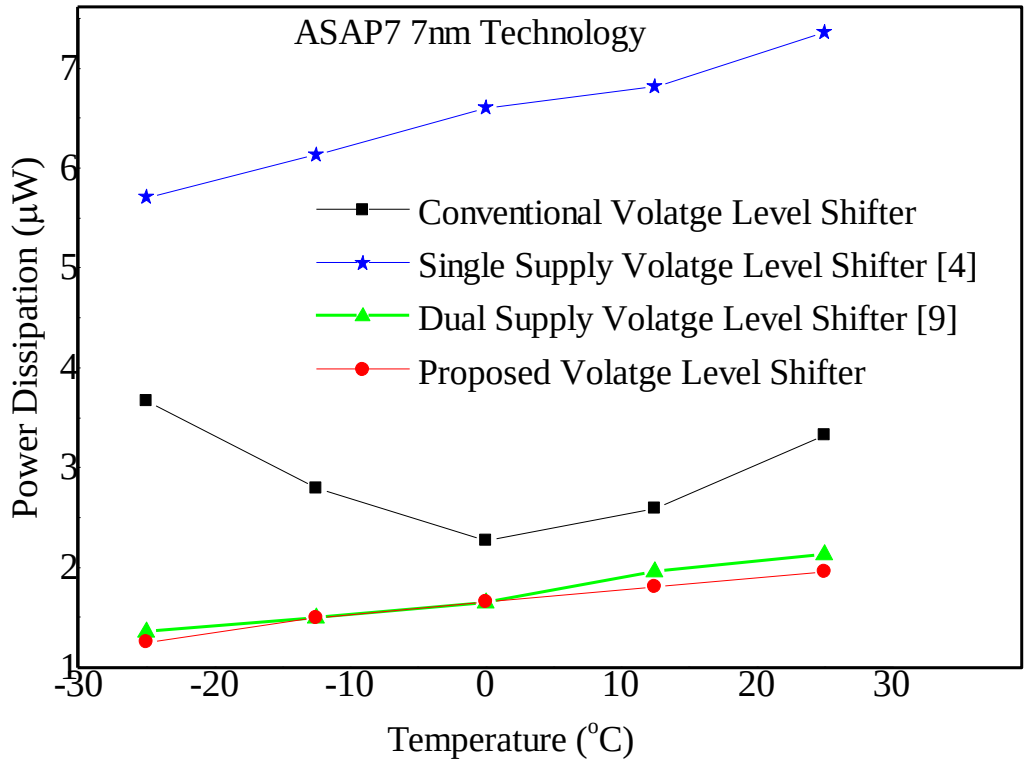

Figure – 3.6 Power analysis comparison of different voltage level shifter at different temperatures

An optimized and power efficient design of voltage level shifter has been proposed for low core voltage operations. The optimization is especially done keeping in mind two major parameters, propagation delay and power consumption respectively. Also, the proposed voltage level shifter design requires only a single power supply for its operation, which adds on to the reduction of overall cost of the system and gives us an edge over dual supply level shifter

design. The proposed design is designed properly, and the results have been verified using transistors based on ASAP7 7nm technology. All the simulations are performed in cadence virtuoso tool at various input voltages, and the results have been verified. The performance of the proposed level shifting design is optimized as well as power efficient in comparison to older versions of voltage level shifting designs.

3.3 OUTCOMES OF THE RESEARCH

An optimized and power efficient design of voltage level shifter has been proposed for low core voltage operations. The optimization is especially done keeping in mind two major parameters, propagation delay and power consumption respectively. Also the proposed voltage level shifter design requires only a single power supply for its operation, which adds on to the reduction of overall cost of the system, and gives us an edge over dual supply level shifter design. The proposed design is designed properly and the results have been verified using transistors based on ASAP7 7nm technology. All the simulations are performed in cadence virtuoso tool at various input voltages, and the results have been verified. The performance of the proposed level shifting design is optimized as well as power efficient in comparison to older versions of voltage level shifting designs.

CHAPTER – 4

DUAL SUPPLY SELECT SIGNAL DESIGN

4.1 A NOVEL OPTIMIZED SELECT SIGNAL CMOS VOLTAGE LEVEL SHIFTER

The schematic diagram of the proposed voltage level shifteris shown in Fig.4.1. The proposed voltage level shifter can perform both the operations of shifting the voltage up as well as down, as the shifting operation depends on the selected input voltage signal. Two voltage sources have been takenin to use i.e., VDDH and VDDL. The two voltages signals, VDDH and VDDL are at 1.2V and 0.6V respectively. For up and down shifting VDDH and VDDL are respectively selected dependingon the input voltage signal Vin. Hence, the output voltage level either comes out to be VDDH or VDDL.

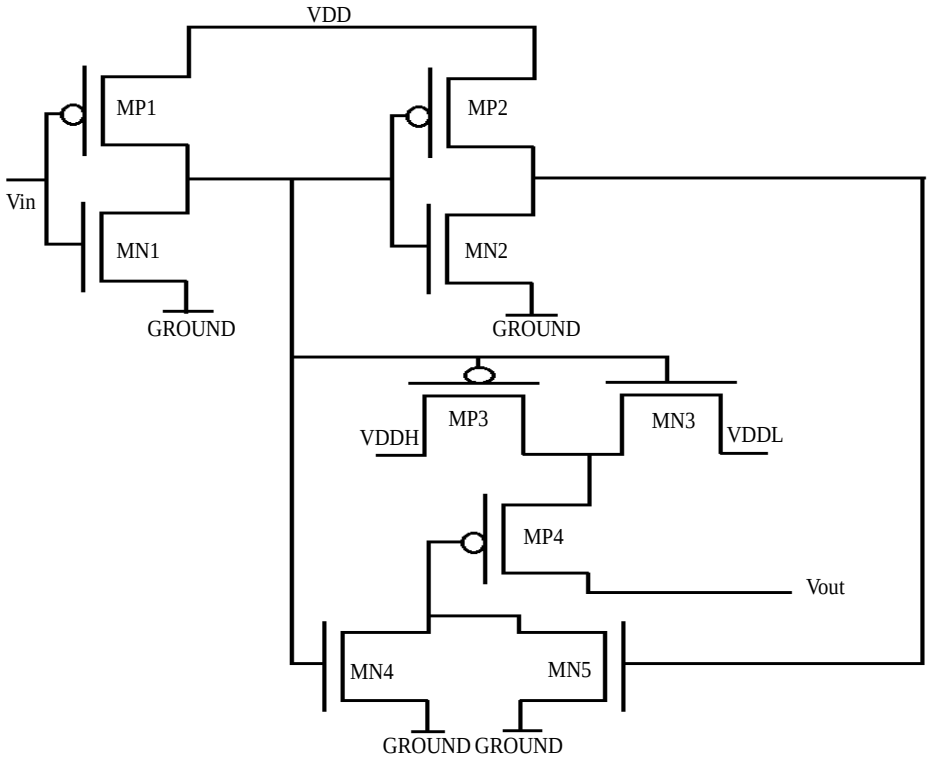

Figure – 4.1 Proposed C-MOS voltage level shifter model

Let us understand the working of the proposed voltage level shifter design. When input voltage Vin is low (0V), MP1 transistor turns ON, which in return turns ON MN3 and MN4

transistors. The transistor MP4 is now provided with 0V at its gate terminal, which turns it ON. At this time MN3 and Mp4 transistors are ON and provide direct path from VDDL to output terminal (Vout become VDDL). This is the operation for level down shift. Now we consider the scenario when Vin is high (i.e., Vin = 1). In this case, MN1 turns ON, which in return puts MP2 and MP3 in ON state. Now, the gate terminal of MN5 now gets provided with high voltage, which turns ON MP4 and hence, the obtained output is VDDH i.e., 1.2V. This is called as level up shift. The transistor network MP3 and MN3 are working as 2 X 1 multiplexer. Either VDDH or VDDL will be selected on the basis of input select signal Vin. Hence, Vin is acting as selecting signal to transfer the operation from up shift to downshift and vice versa.

4.1 SIMULATION AND RESULTS

Cadence Virtuoso is used for circuit performance and validation. In cadence simulations, we have used ASAP7 7nm Fin-Fet technology. We verified the proposed level shifter at different voltage levels (0.3 to 0.6V).

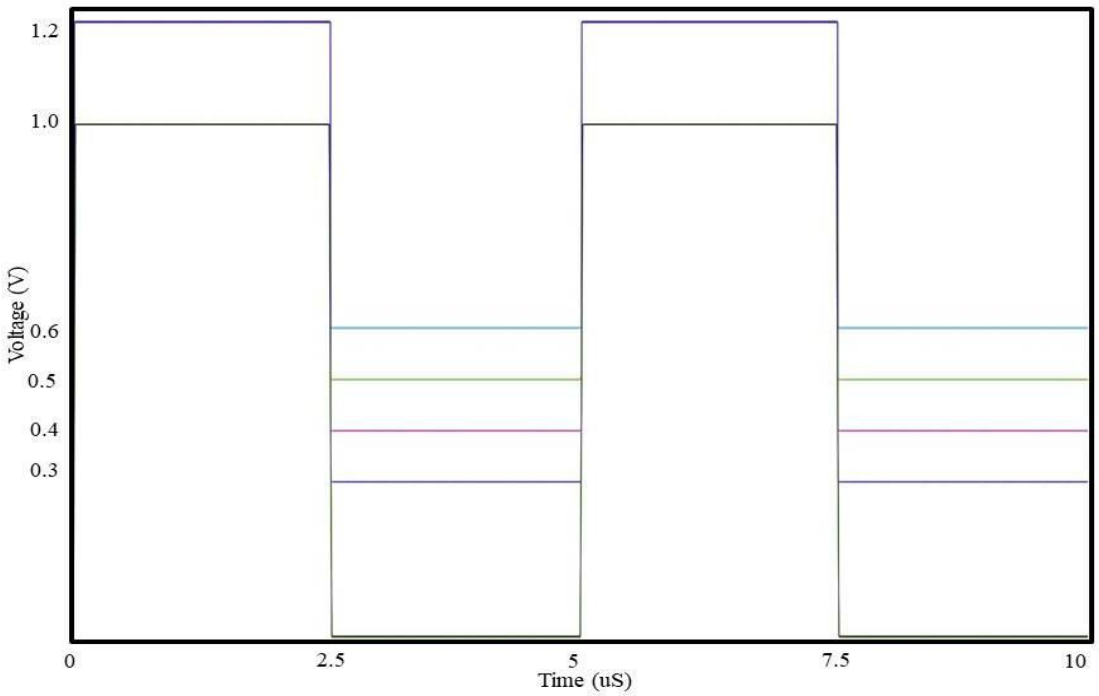

Figure – 4.2 Output waveform of the proposed circuital model under various input voltages

Fig.4.2. shows the simulated output waveforms of the proposed level shifter for different voltage levels. In simulations we apply different voltage levels, the VDDL ranges from 0.3V to 0.6V with a step size of 0.1V, and VDDH remain to be 1.2V. The comparison of propagation delay at

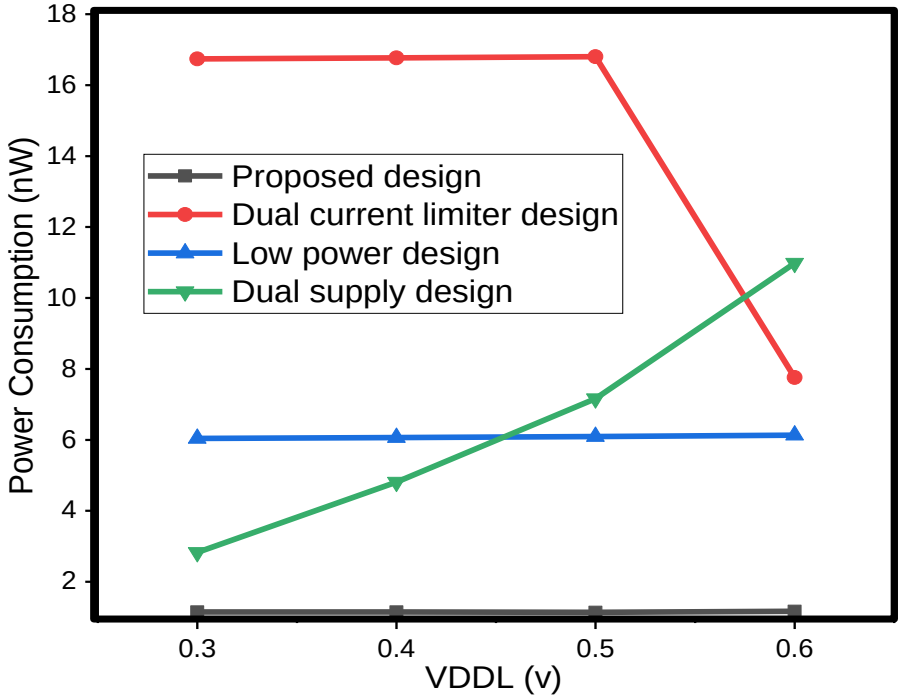

Figure – 4.3 Power dissipation comparison with other models

different voltage levels (VDDL) of the proposed level shifter with the reported level shifters is shown in Fig.4.4. From the simulation results, it can be easily observed that, at all voltages (VDDL ranges from 0.3 to 0.6V) the proposed voltage level shifter shows less propagation delay as compared with existing voltage level shifter.

Fig.4.3 shows the power dissipation curve of the proposed level shifter model. The power dissipation of the proposed level shifter model is comparatively lesser than the previous level shifter models at the provided similar voltage range of 0.3V to 0.6V. Only the VDDL has been changed to obtain the results, VDDH remains same as 1.2V for each simulation.

If we compare this design with previous level shifting models, we arrive to a conclusion that the proposed design is much more power efficient as well as, involves lesser propagation delays. The power dissipated by low power level shifter model, dual supply level shifter model, dual current limiter level shifter model is 6.065nW, 4.81nW and 16.77nW respectively, whereas the proposed select signal level shifter model consumes only 1.15nW power at VDDL 0.4V and VDDH 1.2V.

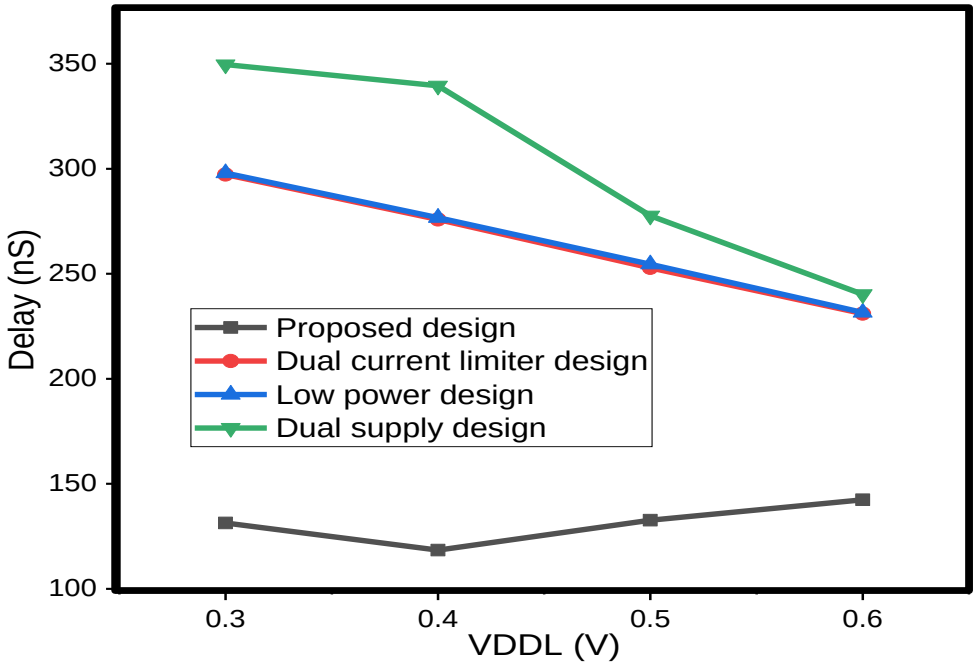

Figure – 4.4 Propagation delay comparison with older versions

Table.3 compares the propagation delay and power consumption of proposed design with existing level shifter designs. It can be easily observed that our design has better performance as compared to the existing design, at VDDL range from 0.3V to 0.6V and VDDH remains at 1.2V, with ASAP7 7nm Fin-Fet design model. The model can also be used as a up shifter as well as a down shifter simultaneously.

Table – 3 Power and delay analysis of various models

VERSIONS	**POWER DISSIPATION (nW)**	**PROPOGATION DELAY (nS)**
Low Power model	6.065	276.75
Dual supply Model	4.81	339.48
Dual current limiter model	16.77	275.87
Proposed Model	1.15	118.42

An optimized and power efficient model of voltage level shifter has been proposed for low core voltage operations. The optimization is especially done keeping in mind two major parameters, propagation delay and power consumption respectively. The proposed model is designed properly, and the results have been verified using transistors based on ASAP7 7nm technology. All the simulations are performed in cadence virtuoso tool at various input voltages, and the results have been verified. The performance of the proposed level shifting model is optimized as well as power efficient in comparison to older versions of voltage level shifting models. Along with all these advantages, the proposed voltage level shifter adds one feature to the design, that a single model can be used for both up shift and down shift at the same time, making Vin as the select signal.

4.3 OUTCOMES OF THE RESEARCH

An optimized and power efficient model of voltage level shifter has been proposed for low core voltage operations. The optimization is especially done keeping in mind two major parameters, propagation delay and power consumption respectively. The proposed model is designed properly and the results have been verified using transistors based on ASAP7 7nm technology. All the simulations are performed in cadence virtuoso tool at various input voltages, and the results have been verified. The performance of the proposed level shifting model is optimized as well as power efficient in comparison to older versions of voltage level shifting models. Along with all these advantages, the proposed voltage level shifter adds one feature to the design, that a single model can be used for both up shift and down shift at the same time, making Vin as the select signal.

CHAPTER – 5

CONCLUSION

A voltage level shifter in modern days should be energy efficient and more reliable for industrial use. The first proposed methodology presents an optimized and power efficient design of voltage level shifter for low core voltage operations. The optimization is especially done keeping in mind two major parameters, propagation delay and power consumption respectively. Also, the proposed voltage level shifter design requires only a single power supply for its operation, which adds on to the reduction of overall cost of the system and gives us an edge over dual supply level shifter design. The proposed design is designed properly, and the results have been verified using transistors based on ASAP7 7nm technology. All the simulations are performed in cadence virtuoso tool at various input voltages, and the results have been verified. The performance of the proposed level shifting design is optimized as well as power efficient in comparison to older versions of voltage level shifting designs. The second proposed methodology gives us an optimized and power efficient model of voltage level shifter has been proposed for low core voltage operations. The optimization is especially done keeping in mind two major parameters, propagation delay and power consumption respectively. The proposed model is designed properly, and the results have been verified using transistors based on ASAP7 7nm technology. All the simulations are performed in cadence virtuoso tool at various input voltages, and the results have been verified. The performance of the proposed level shifting model is optimized as well as power efficient in comparison to older versions of voltage level shifting models. Along with all these advantages, the proposed voltage level shifter adds one feature to the design, that a single model can be used for both up shift and down shift at the same time, making Vin as the select signal.

REFERENCES

1. M. Alioto, "Ultra-low power VLSI circuit design demystified and explained: A tutorial," IEEE Transactions on Circuits and Systems I: Regular Papers, vol. 59, pp. 3-29, 2012.
2. K. Usami, M. Igarashi, F. Minami, T. Ishikawa, M. Kanzawa, M. Ichida, et al., "Automated low-power technique exploiting multiple supply voltages applied to a media processor," IEEE Journal of Solid-State Circuits, vol. 33, pp. 463-472, 1998.
3. https://whatis.techtarget.com/definition/CMOS-complementary-metal-oxide-semiconductor
4. https://pediaa.com/difference-between-nmos-and-pmos/
5. M. Lanuzza, P. Corsonello, and S. Perri, "Fast and wide range voltage conversion in multisupply voltage designs," IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 23, pp. 388-391, 2015
6. VanLoi Le, Student, and Tony Tae-Hyoung Kim, ―An Area and Energy Efficient Ultra-Low Voltage Level Shifter with Pass Transistor and Reduced-Swing Output Buffer in 65-nm CMOS,‖ TCAS-II-02776- 2018
7. Kabirpour, S., Jalali, M.: A power-delay and area efficient voltage level shifter based on a reflected-output Wilson current mirror level shifter. IEEE Trans. Circuits Syst. II: Exp. Briefs 67(2), 250–254 (2020)
8. Le, V.L., Kim, T.T.-H.: An area and energy efficient ultra-low voltage level shifter with pass transistor and reduced-swing output buffer in 65nm CMOS. IEEE Trans. Circuits Syst. II: Exp. Briefs 65(5), 607–611 (2018)
9. Kabirpour S. and M. Jalali, ―A Power-Delay and Area Efficient Voltage Level Shifter Based on a Reflected-Output Wilson Current Mirror Level Shifter,‖ IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS— II: Express Briefs 2018.
10. A.P.Chandrakasan, S. Sheng, and R. W. Brodersen,(1992) ―Low- power CMOS digital design,‖ IEEE J. Solid-State Circuits, vol. 27,no.4, pp. 473–484.

11. Marco Lanuzza, Pasquale Corsonello, and StefaniaPerri, ―Fast and Wide Range Voltage Conversion in Multisupply Voltage Designs,‖ IEEE TRANSACTIONS ON VERY LARGE-SCALE INTEGRATION (VLSI) SYSTEMS.
12. R. Lotfi, M. Saberi, S. R. Hosseini, A. R. Ahmadi-Mehr, and R. B. Staszewski, "Energy-Efficient Wide-Range Voltage Level Shifters Reaching 4.2 fJ/Transition," IEEE Solid-State Circuits Letters, vol. 1, pp. 34-37, 2018.
13. T. T.-H. Kim, "An Area and Energy Efficient Ultra-Low Voltage Level Shifter With Pass Transistor and Reduced-Swing Output Buffer in 65-nm CMOS," IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 65, pp. 607-611, 2018.
14. H. Kawaguchi, K. Kanda, K. Nose, S. Hattori, D. D. Antono, D.Yamada, T. Miyazaki, K. Inagaki, T. Hiramoto, and T. Sakurai, “A 0.5-V, 400-MHz, VDD-Hopping Processor with Zero-VTH FDSOI Technology,” ISSCC, Feb. 2003, pp. 106-107.
15. Tran, C.Q. Kawaguchi, H. Sakurai, T., “Low-power highspeed level shifter design for block-level dynamic voltage scaling environment”, ICICDT 2005, 9-11 May 2005, pp. 229- 232.
16. S. Pashmineh and D. Killat, "Self-biasing high-voltage driver based on standard CMOS with an adapted level shifter for a wide range of supply voltages," 2015 Nordic Circuits and Systems Conference (NORCAS): NORCHIP & International Symposium on System-on-Chip (SoC), 2015, pp. 1-4, doi: 10.1109/NORCHIP.2015.7364405.
17. X. Hao, F. Yang, M. He, Y. Zheng, Y. Guo and H. Liao, "A 93.7% peak efficiency DC-DC buck converter with all-pass network based passive level shifter in 55 nm CMOS," 2016 IEEE International Symposium on Circuits and Systems (ISCAS), 2016, pp. 445-448, doi: 10.1109/ISCAS.2016.7527266.
18. S. Londhe and E. Socher, "28–38-GHz 6-bit Compact Passive Phase Shifter in 130-nm CMOS," in IEEE Microwave and Wireless Components Letters, vol. 31, no. 12, pp. 1311-1314, Dec. 2021, doi: 10.1109/LMWC.2021.3112689.
19. P. Palakurthi, J. Martinez and E. MacDonald, "Radiation hardened level shifter

for sub to superthreshold voltage translation," 2012 IEEE Subthreshold Microelectronics Conference (SubVT), 2012, pp. 1-3, doi: 10.1109/SubVT.2012.6404302.

20. D. d. Rio, C. -J. Liang, C. -W. Chiang, R. Berenguer, M. -C. F. Chang and Y. -C. Kuan, "A Simultaneous Phase Shifter and Up-Converter for the 28/38/60-GHz Bands in 28-nm CMOS," 2020 IEEE Asia-Pacific Microwave Conference (APMC), 2020, pp. 1012-1014, doi: 10.1109/APMC47863.2020.9331563.
21. E. Atasoy, F. Piri and B. S. Yarman, "Symmetric lattice 45°, 90° and 180° digital phase shifter at 3–6 GHz for LTE, WIFI, Radar applications," 2015 International Symposium on Signals, Circuits and Systems (ISSCS), 2015, pp. 1-4, doi: 10.1109/ISSCS.2015.7203994.
22. J. Cai, B. Halak and D. Rossi, "Analysis of BTI aging of level shifters," 2016 IEEE 22nd International Symposium on On-Line Testing and Robust System Design (IOLTS), 2016, pp. 17-18, doi: 10.1109/IOLTS.2016.7604662.
23. K. L. Chan, A. A. Lee, X. Yuan, K. R. Krishna and M. Je, "A 8.9-ENOB 2.5-εW 150-KS/s non-binary redundant successive approximation ADC in 0.18-μm CMOS for bio-implanted devices," 2010 Annual International Conference of the IEEE Engineering in Medicine and Biology, 2010, pp. 650-653, doi: 10.1109/IEMBS.2010.5627231.
24. Y. Osaki, T. Hirose, N. Kuroki and M. Numa, "A Low-Power Level Shifter With Logic Error Correction for Extremely Low-Voltage Digital CMOS LSIs," in IEEE Journal of Solid-State Circuits, vol. 47, no. 7, pp. 1776-1783, July 2012, doi: 10.1109/JSSC.2012.2191320.
25. X. Lai and F. Yuan, "Passive voltage level shifters for analog signaling," 10th IEEE International NEWCAS Conference, 2012, pp. 481-484, doi: 10.1109/NEWCAS.2012.6329061.
26. S. Hong, S. Lee, T. Roh and H. Yoo, "A 46 μW motion artifact reduction bio-signal sensor with ICA based adaptive DC level control for sleep monitoring system," Proceedings of the IEEE 2012 Custom Integrated Circuits Conference, 2012, pp. 1-4, doi: 10.1109/CICC.2012.6330602.

27. M. Terres, C. Meinhardt, G. Bontorin and R. Reis, "A novel approach to reduce power consumption in level shifter for Multiple Dynamic Supply Voltage," 2013 IEEE 20th International Conference on Electronics, Circuits, and Systems (ICECS), 2013, pp. 715-718, doi: 10.1109/ICECS.2013.6815514.

28. P. S. Swain, M. Shrivastava, H. Gossner and M. S. Baghini, "Device–Circuit Co-design for Beyond 1 GHz 5 V Level Shifter Using DeMOS Transistors," in IEEE Transactions on Electron Devices, vol. 60, no. 11, pp. 3827-3834, Nov. 2013, doi: 10.1109/TED.2013.2283421.

29. C. Lu et al., "A scalable baseband phase shifter with 12 GHz I/Q Mixers in 40-nm CMOS for 60 GHz applications," 2014 IEEE International Symposium on Circuits and Systems (ISCAS), 2014, pp. 2708-2711, doi: 10.1109/ISCAS.2014.6865732.

30. B. Mohammadi and J. N. Rodrigues, "A 65 nm single stage 28 fJ/cycle 0.12 to 1.2V level-shifter," 2014 IEEE International Symposium on Circuits and Systems (ISCAS), 2014, pp. 990-993, doi: 10.1109/ISCAS.2014.6865304.

31. R. Llanos, D. Sousa, M. Terres, G. Bontorin, R. Reis and M. Johann, "Energy-efficient Level Shifter topology," 2015 25th International Workshop on Power and Timing Modeling, Optimization and Simulation (PATMOS), 2015, pp. 148-151, doi: 10.1109/PATMOS.2015.7347600.

32. Wen-Ming Zheng et al., "Capacitive floating level shifter: Modeling and design," TENCON 2015 - 2015 IEEE Region 10 Conference, 2015, pp. 1-6, doi: 10.1109/TENCON.2015.7373013.

33. M. Moghaddam, M. H. Moaiyeri and M. Eshghi, "A low-voltage level shifter based on double-gate MOSFET," 2015 18th CSI International Symposium on Computer Architecture and Digital Systems (CADS), 2015, pp. 1-5, doi: 10.1109/CADS.2015.7377778.

34. M. R. Valero, A. López-Martín, A. Román-Loera, J. Ramírez-Angulo and R. G. Carvajal, "Constant gm rail-to-rail CMOS OpAmp with only one differential pair and switched level shifters," 2015 IEEE International Symposium on Circuits and Systems (ISCAS), 2015, pp. 2461-2464, doi: 10.1109/ISCAS.2015.7169183.

35. H. -W. Lin and T. -H. Lin, "A 0.3V, 625Mbps LVDS Driver in 0.18um CMOS Technology," 2020 IEEE International Conference on Semiconductor Electronics (ICSE), 2020, pp. 65-68, doi: 10.1109/ICSE49846.2020.9166860.

36. M. Karimi et al., "A 1.99-ns 0.5-pJ Wide Frequency Range Level Shifter With Closed-Loop Negative Feedback," 2020 18th IEEE International New Circuits and Systems Conference (NEWCAS), 2020, pp. 174-177, doi: 10.1109/NEWCAS49341.2020.9159830.

37. P. Shukla, P. Singh, T. Maheshwari, A. Grover and V. Rana, "A 800MHz, 0.21pJ, 1.2V to 6V Level Shifter Using Thin Gate Oxide Devices in 65nm LSTP," 2020 27th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2020, pp. 1-4, doi: 10.1109/ICECS49266.2020.9294984.

38. E. Låte, T. Ytterdal and S. Aunet, "An Energy Efficient Level Shifter Capable of Logic Conversion From Sub-15 mV to 1.2 V," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 67, no. 11, pp. 2687-2691, Nov. 2020, doi: 10.1109/TCSII.2020.2966654.

39. P. K. Poongodan, F. Vanselow and L. Maurer, "A Two-Level, High Voltage Driver Circuit with Nanosecond Delay for Ultrasonic Transducers," 2020 9th International Conference on Modern Circuits and Systems Technologies (MOCAST), 2020, pp. 1-4, doi: 10.1109/MOCAST49295.2020.9200247.

40. H. -C. Lee et al., "A High Voltage Driving Chiplet in Standard 0.18-μm CMOS for Micro-Pixelated LED Displays Integrated with LTPS TFTs," in IEEE Transactions on Circuits and Systems for Video Technology, doi: 10.1109/TCSVT.2022.3168051.

41. S. N. Wooters, B. H. Calhoun and T. N. Blalock “An Energy-Efficient Sub-threshold Level Converter in 130-nm CMOS,” IEEE Trans. Circuits Syst. II, Exp. Briefs, vol. 57, pp. 290–294, April 2010.

42. Q. A. Khan, S. K. Wadhwa and K. Misri, "A single supply level shifter for multi-voltage systems," 19th International Conference on VLSI Design held jointly with 5th International Conference on Embedded Systems Design (VLSID'06), 2006, pp. 4 pp.-, doi: 10.1109/VLSID.2006.24.

43. Manoj, Kumar & Arya, Sandeep & Pandey, Sujata. (2010). Level Shifter Design for Low Power Applications. International Journal of Computer Science & Information Technology. 2. 10.5121/ijcsit.2010.2509.

44. S. Gundala, M. M. Basha and S. Vijayakumar, "Double Current Limiter High Performance Voltage Level Shifter for IoT Applications," 2020 5th International Conference on Communication and Electronics Systems (ICCES), 2020, pp. 285-288, doi: 10.1109/ICCES48766.2020.9137901.

45. S. Kabirpour and M. Jalali, "A Low-Power and High-Speed Voltage Level Shifter Based on a Regulated Cross-Coupled Pull-Up Network," in IEEE Transactions on Circuits and Systems II: Express Briefs, vol. 66, no. 6, pp. 909-913, June 2019, doi: 10.1109/TCSII.2018.2872814.

46. P. K. Machiraju and D. Y. Pushpamithra, "A novel energy efficient voltage level shifter," 2014 International Conference on Science Engineering and Management Research (ICSEMR), 2014, pp. 1-4, doi: 10.1109/ICSEMR.2014.7043658.

CHAPTER – 6

PUBLICATIONS

LIST OF PUBLICATIONS

6.1 PUBLICATION TABLE

SERIAL NO	HEADING OF THE PAPER	PUBLICATION	SCOPES (Yes/No)	AUTHOURS
1.	High performance energy efficient CMOS voltage level shifter.	IEEE 2nd CONIT 2022 (Accepted)	Yes	**1.**Ravi Nandan Ray, **2.**Dr. Madan Mohan Tripathi, **3.**Dr. Chaudhary Indra Kumar
2.	A novel optimized select signal CMOS voltage level shifter.	IEEE VDAT 2022 (communicated)	Yes	**1.**Ravi Nandan Ray, **2.**Dr. Madan Mohan Tripathi, **3.**Dr. Chaudhary Indra Kumar