A Project Report

On

**Design and Analysis of Low Power SRAM**

Submitted in the Partial Fulfilment of the Requirement for the Award of the Degree of

**Master of Technology**

In

**VLSI & Embedded Systems**


Submitted By:

**Kundan Kumar Das**

**(2K20/VLS/09)**

Under the Supervision of:

**Mr. Sachin Dhariwal**

**(Asst. Professor)**




Department of Electronics & Communication Engineering

Delhi Technological University, Delhi

(Formerly Delhi College of Engineering) Bawana Road, Delhi- 110042

# DECLARATION

We declare that the work presented in this project titled **"Design and Analysis of Low Power SRAM"**, submitted to the **Department of Electronics & Communication Engineering, Delhi Technological University, Delhi** for the award of the **Master of Technology** degree in **VLSI & Embedded Systems** is our original work. We have not plagiarized or submitted the same work for the award of any other degree. In case this undertaking is found incorrect, I accept that our degree may be unconditionally withdrawn.

Date – 31st May 2022 Kundan Kumar Das

Place – Delhi 2K20/VLS/09

# CERTIFICATE

This is to certify that the work contained in the project titled "**Design and analysis Low Power SRAM**", submitted by **Kundan Kumar Das** in the partial fulfilment of the requirement for the award of Master of Technology in VLSI & Embedded Systems to the Electronics & Communication Engineering Department, Delhi Technological University, Delhi, is a record of the project work carried out by the student under my supervision.

Date – 31st May 2022
Place – Delhi

Mr. Sachin Dhariwal
Asst. Professor
ECE Department
DTU Delhi

# Abstract

In the present scenario the portable operated battery devices has significant demand in low power IC design. In modern SOCs, embedded SRAM has an important part and traditional SRAM designs are not good in performance and also consume more power.

In this project the working of SRAM has been discussed, and analyzed the power consumption by the static random access memory (SRAM). There are different strategies to reduce the different power loss in memory cell, but here our main focus on to reduce the leakage power. Because the transistors are growing in SRAM unit, it leads to increase the leakage current. Now transistors are scaling down it made leakage current more crucial in term of power loss. So reduce the power loss from the memory cell stacked technique has been used. In stacked technique N type transistor is used. In this technique the NMOS transistor is placed in between the cell and ground. First analysis has done with only one transistor and second time the analysis has done with the help of two NMOS transistor. After that a comparison has been done among traditional 6T SRAM cell and proposed design of low power SRAM cell. The stacked designed techniques-based SRAM cell has better performance with respect to power consumption compare to traditional SRAM cell.

# ACKNOWLEDGEMENT

It gives us immense pleasure to present this innovative work for the partial fulfillment for the award of M.Tech degree in VLSI & Embedded Systems. We owe special debt of gratitude to our supervisor **Mr. Sachin Dhariwal**, Asst. Professor Department of Electronics and Communication Engineering, Delhi Technological University, Delhi for their constant support and guidance throughout the course of our work. Their sincerity, thoroughness and perseverance have been a constant source of inspiration for us.

We would also like to thank all other faculty members of Electronics and Communication Engineering Department for their valuable suggestions and co-operation at every step in this project. We would also like to thank our parents and batch mates for their constant motivation throughout this work. Last but not the least we would like to thank Almighty for His invisible presence and constant support.

Date – 31st May 2022 Place – Delhi

Kundan Kumar Das
2K20/VLS/09

# CONTENTS

# LIST OF TABLE

# LIST OF FIGURES

# ABBREVIATIONS

RAM - Random Access Memory

SRAM - Static Random Access Memory

DRAM - Dynamic Random Access Memory

ASIC - Application Specific Integrated Circuit

VTC - Voltage Transfer Characteristics

SNM - Static Noise Margin

SOC - System on Chip

CMOS - Complementary Metal-Oxide Semiconductor

BL - Bit-Line

BLB - Bit-Line-Bar

SA - Sense Amplifier

# CHAPTER 1

# INTRODUCTION AND MOTIVATION

## 1.1 INTRODUCTION

In current time the demand of high-speed processors which are operated in very less power and required lesser area, is increasing exponentially with time. A perfect memory is reliable, space efficient and quick with consuming minimum power. Almost all VLSI chips now include fast low power SRAM as a vital component, and it's particularly true for all the processors, where cache memory sizes are increasing on the SOCs with generation to overcome the performance gap between the memory and the processors [1, 2].Furthermore due to greater integration, running speed and the exponential expansion of battery operated product, power dissipation has become an essential problem [3]. The design of SRAM investigated in this thesis, with an emphasis on optimizing latency and power, but scaling of supply [6, 11] and the process [4, 5] will always be most important factor. This thesis looks at certain approaches that will be utilised in certain combinations with scaling to produce fast low-power operation.

As there is a demand in battery-operated portable devices increasing, low power and compact size design becoming a crucial factor and most favourable area of research for researchers. To design a fast processor, fast sampling of data is one of the major constraints, and SRAM plays this crucial role. SRAM works as mediator between processor and main memory which are interfaced with other slower peripheral. RAM work as cache memory in a processor. SRAM or cache memory consists of instruction data temporarily, which are frequently in use by the processor. SRAM is $2^{nd}$ fastest memory in memory organization. It comes after the register type memory. With passing of time as the demand of high-speed operation is increasing, size of cache memory is also increasing proportionally. Since larger size of SRAM memory provides a wider operational bandwidth, which implies larger size of data can be received or can send to destination. Bandwidth is directly related to the speed of operation of processor. i.e., as bandwidth increases speed of operation will also improve. However, as the size of SRAM on System

on Chip increases, it becomes a greater area consumer on SOC board. On an average it consumes about 50% of the total area on a SOC board. This is a major concern. In this project, we will try to optimize our SRAM cell design at block level so that the requirement of area can be minimized. The next work will upon low power techniques at block level and at transistor level to minimize the power dissipation.

Some features of SRAM are like it does not require data refreshing after certain period of interval. These properties of SRAM cell eliminate the requirement of complex and area taking peripherals. It implies that SRAM can retain the data until unless power is not removing, so SRAM need to be connected to the power supply when it is in use. As SRAM is a mediator between processor and other peripherals and memories, it has wide application in many areas for example in wireless communication, in DSPs, in portable devices etc.

SRAM cell generally designed using only MOSFETs. 6T SRAM is a most used design in SRAM cell design. Many other designs is also proposed by the researchers, which have an edge in terms operational speed, data stability, reduced read and write cycle time, but still 6T SRAM cell is the first choice of memory manufacturing industry. Since SRAM cell already consumes about 50% area of the total SOC board which is a major constraint. With passing of time much advancement is also proposes by the researcher in 6T SRAM cell design and it is highly compatible with other SRAM design. In this project the work will upon designing of a low power 6T SRAM cell, and using this cell we design a SRAM memory using the concept of memory banking. The design should be low power and high-speed peripherals of SRAM memory.

## 1.2 MOTIVATION

In modern era the demand of battery operated and a portable mobile device is increasing explosively. Surge in battery operated devices gives birth for the low power design and motivates researchers to research and design low power devices with optimizing area and speed trade-off as well. Since SRAM is a one of the most essential part of a SOC and it consumes larger area of a SOC. This constraint motivates me to work upon this topic and try to find an optimum solution which can minimize the speed, power, and area trade off.

SRAM is one of the most essential parts of a SOC. it has a wider range of application. It is using in field of wireless communication, in DSPs, in field of bio medical equipment and devices, in portable devices, in multimedia devices, in smart phones and in various high-speed processor. This is also one the reason to decide to work upon this topic. As the size and demand of Low power and high-speed processors is increasing. So, to find out an optimum solution at transistor level, at block level, and at architectural level, so that the power dissipation, area requirement can be reduced, and operational speed can be increased is the main motivation behind doing this project. In emerging sub-100 nm design technologies, leakage power is a major concern. Because most cells of SRAM are inactive and it cannot be accessed, and these cells will have little dynamic activity, it becomes more critical for on-chip SRAM. In terms of leakage, they are on and use static electricity. With the widespread use of battery-powered electronic devices, integrated circuit power consumption is becoming increasingly essential, and because if number of transistor will be more then the leakage power will be more. So it can be said that leakage power is directly related to the how many number of transistors are included. This can be a significant source of leakage power in the design. Through this work, I tried to look at different ways to reduce SRAM's leakage (static) power and develop SRAM cells that can do so without compromising the reliability of the cell and performance.

### 1.3 OBJECTIVE

To work on this thesis various investigation done and investigate several strategies and different techniques for lowering the SRAM’s leakage power design using CMOS technology. Stacked SRAM are proposed here, in order to lowering the leakage power without compromising the performance of the SRAM. It is also investigated the effect of different temperature on SRAM circuits.

# CHAPTER 2

## LITERATURE REVIEW

- Shokoufeh Naghizadeh, Mohammad Gholami **[1**], explained about the importance of SRAM. In present days there is increase in demand of portable device like mobile laptops, tablets and many more. These device provide limitless functionality, to provide limitless functionality they limitless power. But the battery technology is not developed at that speed. Due to this reason the portable device runs on battery, the battery should not drain too fast. So, for lowering the leakage power consumption of the battery operated device. They show different techniques. RAM is most important device for the electronic circuit. It is used in the many integrated chip or SOCs due to its speed. It is used for the fetching the data and instruction from the main memory.
- Debasis Mukherjee, Hemanta Kr.Mondal [2], Explained how to compute the static noise margin, read static noise margin, and write static noise margin of a 6T SRAM cell using the butterfly approach. Also explained the pull up ratio and cell ratio, how is it calculated and how it affect the stability of memory cells through his paper. In the conventional 6T SRAM cell for stability during reading process the size of pull down or NMOS transistor must be greater than the pull up transistor and the access transistor. The size of access transistor must be lesser to reduce the bit line capacitances. In other hand for write operation the size of access transistor should be highland it must have good current capability. The read stability and the write ability of the cell have conflicting design requirements. To solve this problem, separate path for read and write.
- Jan M. Rabaey, Anantha Chandrakasan B. Nikolic [3], Proposed SRAM design and also explained the design of memory using the SRAM cells, also explain about the other peripheral like row and tree decoder, pre-charge, sense amplifier and the connection between them for memory creation.
- Sung M. Kang and Y. Leblebici [4], explained SRAM cell design and its reading writing and hold operation. Also explain that how a cell is connected to create memory cell, all the cell are connected together in array fashion. That the alternation of stored data is not permitted in reading process. In his book DRAM is also introduced. ITRS

predicted that the SRAM take 90% area of the chip and consume massive power it's about 50% of total power. So, we require the SRAM which will take less power and give high performance. Most of time SRAM is idle and it take power to store data. In other hand the passive does not required power to store the data. But we use SRAM because of its high speed. It helps to enhance the speed of the operation of the processor.

- K. Yamaguchi, H. Nambu [5], proposed the 64KB CMOS In which ECL are the word line drivers. He uses combination of ECL work line, cell array of CMOS SRAM and some write circuit. The ECL word line drivers and write circuit drive the CMOS SRAM Cell arrays without the use of an intermediate voltage level converter.
- Rakesh Dayaramji Chandankhede [6], Proposed a decoupled latch sense amplifier which is a current control that reduces power consumption while improving performance. When the enable signal is logic low, the bit line logic and Bit-line Bar logic grows on the latch output, i.e. differential voltage. Whenever the pull down NMOS transistor in SRAM is off, the logic on bit - line and logic on bit-line bar does not expand, and the enable signal remains high. When the EN signal is high, the low-voltage line will go to ground.
- Sreerama Reddy G M, P Chnadra sekhara Reddy [7], Proposed an 8KB SRAM which consume less power than congenital 6T SRAM, also introduce memory banking approach which works at 800MHz. This 8KB low power SRAM was based on 180 nm technology. They also addressed the reduction in power dissipation and clock latency here.
- Harekrishna Kumar, V. K. Tomar, [8], proposed the various type of leakage power in SRAM through this paper and explains it. In present use of the portable devices has increased exponentially. And it is increasing day by day. SRAM is major part of embedded memory and SOC. As technology size decrease the leakage power of devices has become the major issue. It also degrades the power supply. We need to develop the device that consume less power, and gives high performance. Here a comparison has been done and the analysis of 6T, 7T, 8T, 9T, and 10T SRAM. Then give the different idea to reduce it, introduced many schematic diagrams to reduce the leakage power and current.

- Pavan kumar Bikki and Pitchai Karuppanan, [9], present a paper, in this paper they give a detail review of SRAM also give information about the different leakage power explain it and at the end gave the idea for reduction for those leakage power, In present scenario the devices used in the world are small and almost each one is operated on the battery. SRAM is heart of chip, to make single chip millions of SRAM are required. So, designing the circuit that get embedded into these devices in such a way that it will consume less power or energy is major challenge in present day. Because the leakage power is one third of total power consumption. It can affect the stored data or information in memory.

.

# CHAPTER 3

# OVERVIEW OF SRAM

Over time, improvements are happened in SRAM array organisation in memory and circuit design that leads to lower the delay and power of practical SRAMs. This chapter is going to explores about both of these subjects as well as the concerns that this thesis addresses. In Section 3.1, The different strategy like partitioning strategies before highlighting the key circuit solutions which were published in the literature to make certain improvements in speed and power.

## 3.1 PARTITIONING OF SRAM

In huge SRAMs, partitioning arrays of cell into smaller sub units as in cell arrays, instead having a single monolithic array as depicted in Figure 3.1, can result in significant gains in delay and power. A big array is typically made into several no. of same sized sub arrays (usually known as macros), each of which holds a portion of the accessible word, termed the sub word, and all of which are triggered at the same time to access the entire word [10,12]. Low-power SRAMs normally have only one macro, whereas high-performance SRAMs can have up to 16 macros. Except for sharing sections of the decoder, the macros can be regarded of as independent RAMs.

The basic structure of every macro is the same as the one shown in below Figure 3.1. Word line plays an important role while access to a row, it enables all of the cells in particular row, and the column multiplexers access the requested sub word. For macros with a large set of columns, this layout has two drawbacks: The RC latency on the WL increases as the row's square and number of cells. The number of columns increases the bit-line power linearly. Both of these flaws can be addressed by subdividing into small – small pieces units of cells by using approach. The DWL approach divides a typical array's lengthy word line into k pieces, which doesn’t depend to any circuit, and triggered separately, lowering the word line length by k and hence the RC delay by K2. Figure 3.2 depicts the DWL design, which divides a 256-column are divided in two into four blocks, each with 64 columns. The row choosing is now done in two stages. The word line which is enabling

first which is global, and then a block select signal is sent into the appropriate block to enable the specified local word line. The local word line has a reduced RC latency since it is smaller (just 64 columns long). Despite the fact that the global

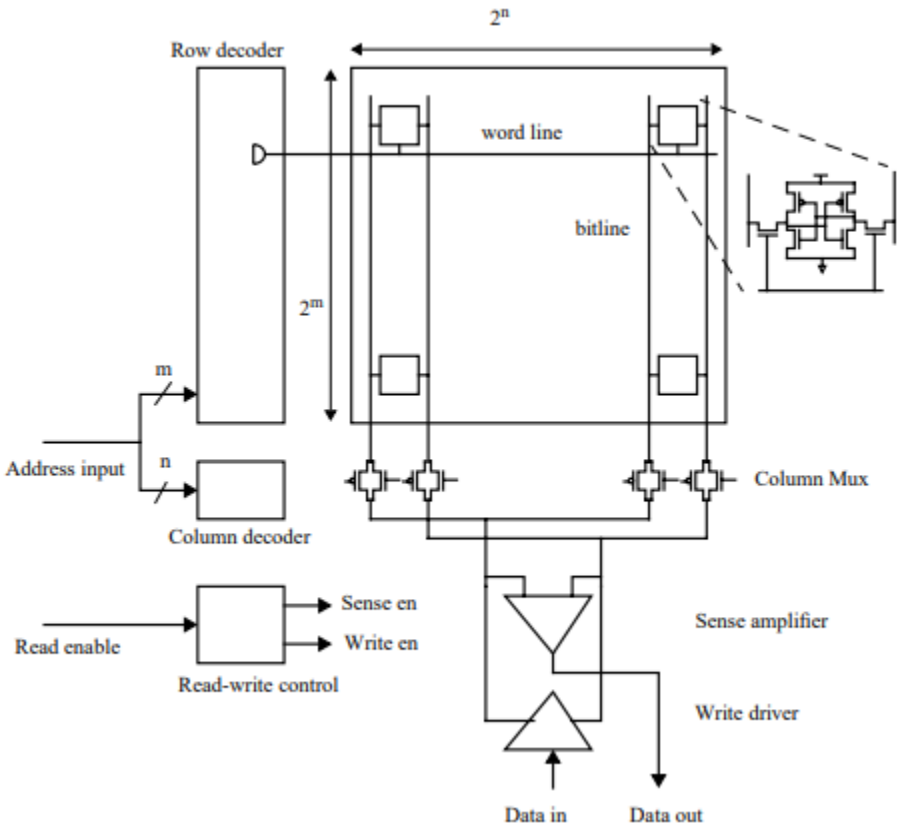


Fig. 3.1: Cell design framework using SRAM [10].

The macro's width and word line are nearly same; it will possess lesser RC latency than a whole word line due to its reduced loading capacitance. Despite the fact that the main word lines are almost similar to the macro's width, it has a very less RC latency than a whole word line due to its relatively low load capacitance. Rather than seeing the loading of all 256 cells, the four word line drivers can be seen input loading. Furthermore, because it is used bigger wires on an advanced level metal layer, its resistance may be lower. By retaining the word drivers at the middle of the word line segments and halving the length of the each section, the word line RC latency is decreased by another factor of four. The column current is also lowered by a factor of four because among 256 cells first 64 cells are activated in the undivided array. The Hierarchical Decoding (HWD) method [14] is based on the idea of partitioning the word line recursively on the Main word line (and the

blocking select line) for large RAMs. Partitioning can also be used to minimise bit-line heights, as explained in the following section.

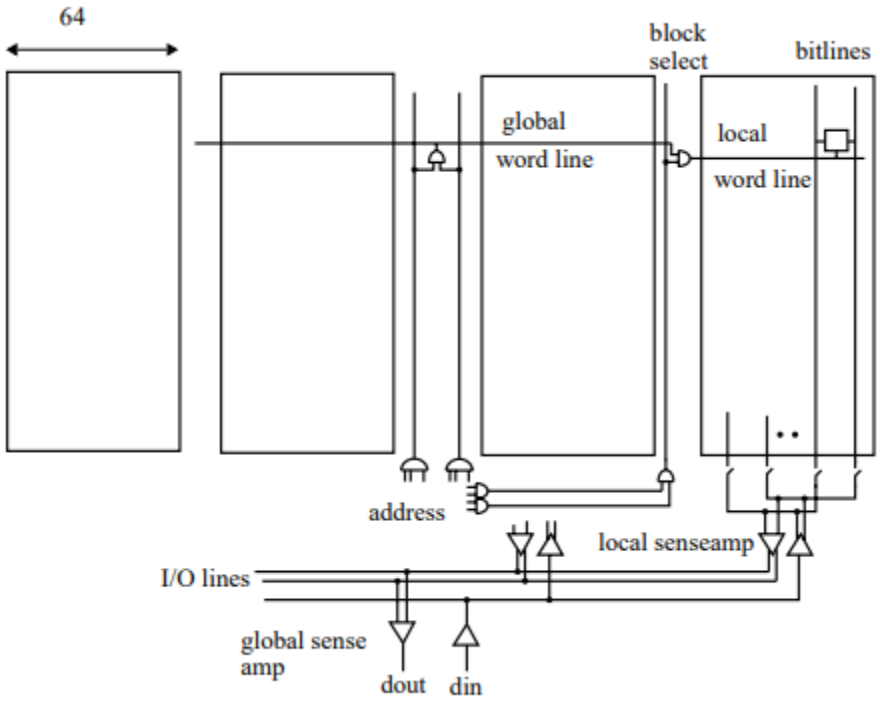


Fig. 3.2: Architecture of Divided Word Line (DWL) [10].

RAM partitioning results in area overhead at the partition boundaries. A partition that deconstructs the word lines, for illustration, necessitates the deployment of word line drivers at the boundaries. Because the area of RAM defines the decoder's main wires length and the data channel, it has a direct impact on their latency and energy. Just look at the Adjustment in latency, area and energy achieved through the dividing.

### 3.2 CIRCUIT METHOD IN SRAM

The data path the decoder and are two components that make up the SRAM access path. The address input circuit to the word line are included in the decoder. The circuits make cells to the input and output ports and make up the data path.

The logic function of decoder is similar to n-input AND gates, with a level arrangement of the more fan-in AND operation. Figure 3.3 depicts the architecture of a two-level 8 to 256 converter. The pre-decoder is the first level, where among the four address inputs two groups and the complement of (A0, A0, A1, A1,...) are decoded active first of its 16 pre-

decoder o/p the wires, resulting in partially decoded products (A0A1A2A3, A0A1A2A3, ...).

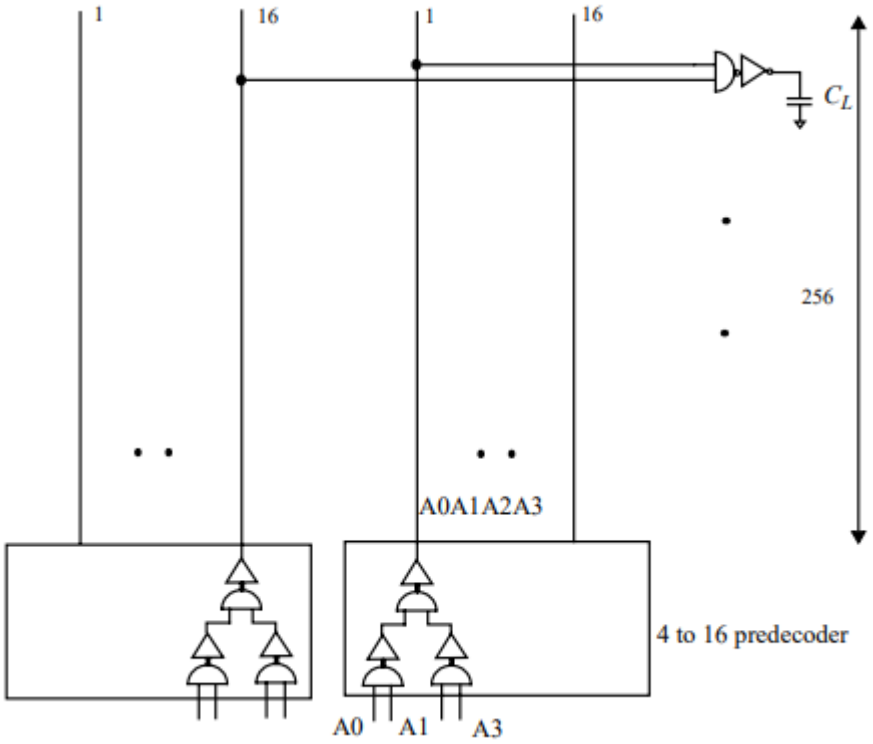


Fig. 3.3: Diagram of decoders [9].

To enabling the word line, the pre-decoder o/p is merged at the other stage. The gate latency along path (crucial), as well as interconnection delays of the word line and pre-decoder and wires, makes up the decoder's latency.

In large SRAMs, the latencies of wire in the structure, particularly of the word line, become critical as the RC latency generate due to the wire length. The size of the gates which are available in the decoder provides always a trade-offs in between the consumption of power and latency. A lot of researchers have looked into transistor size for both fast speed and low power. Because of the presence of intermediary link from the pre-decode wires, the decoder sizing problem is slightly difficult. We look at this issue and propose lower bounds on latency. We also look at some simple scaling strategies for achieving high speed and minimal power. By optimising the circuit style utilised to design the decoder gates, the decoder delay can be considerably reduced. Designs in old days very simple use in

combinational method using static CMOS circuits to implement the decode logic function (Figure 3.4a) [20, 22]. Its 2m lines (word) would be functioning randomly in this design.

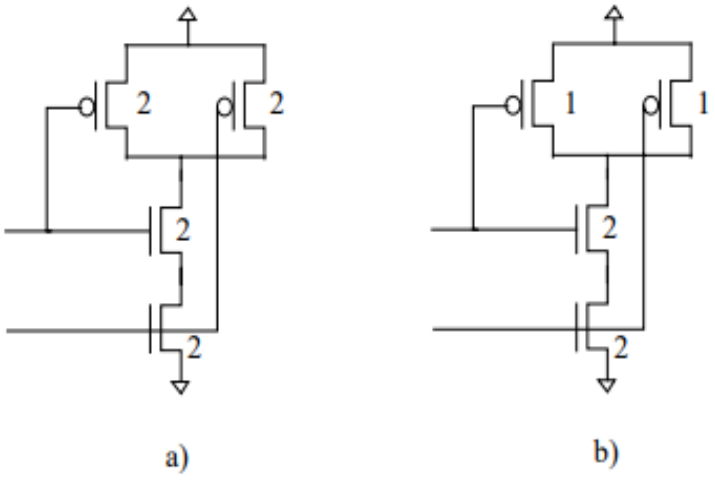


Fig. 3.4: a) NAND gate (conventional) b) NAND gate by Namura [11].

The maximum latency to the old line(word) and the time to insert a new line(word) is therefore the decoder latency of gate in such a design, and its reduced when each gate available in the decoder will be designed in such a way so that it has equal timing of rising and falling. Using pulsed circuit approaches, where the word line is a pulse that stays active for a given minimum length before shutting off, then the latency of gate can will be minimal. As a result, all of the before any accessing, the word lines which are disabled, and the decoder only needs to reactivate them for the updated row address. Because the decoder logic chain only requires transmitting one type of transition, the sizes of transistor plays an important role to increase the speed and reduce the latency and delay timing. Diagram 3.4(b) illustrates this method, in which the size of enhancement P type transistor is half in the NAND gates Structure. The size of PMOS can be lowered further by a half in the pulsed design while maintaining the same rising latency since both inputs are guaranteed to de-assert, decreasing the load of the first stage hence the entire decoder's latency.

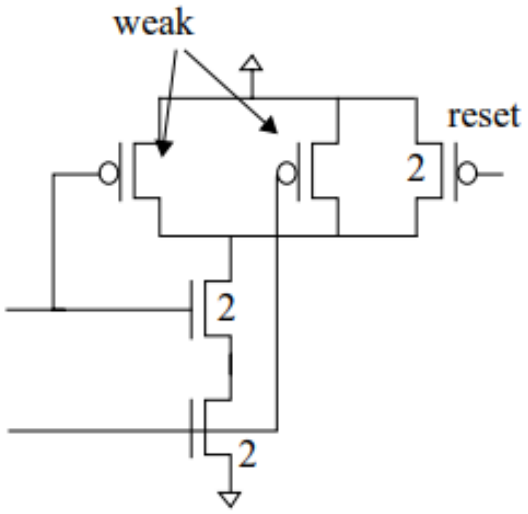


Fig. 3.5: Skew NAND gate [11].

In low-power design there are more other ways like a pulsed decoder can be used is by lowering the power of the bit-line path, which we'll go into momentarily.

For reads, the data in SRAM route a multiplexor can be implemented (and to writes, a de-multiplexer). The multiplexor alone has two phases in the simplest implementation. A limited amount of bit-lines are multiplexed first by column pass transistors at the next level. When the bit-line height is particularly large, additional layers of metal can be used to partition it into multi-level bit-line hierarchy. The multiplexor structure can be built in a variety of ways in particular. Figure 3.6 depicts two different designs for a 512-row block. Only the N-mosfet pass gates are shown in the schematic for the true multiplexor would use Complementary MOS pass gates for differential bit-lines to allow for reads and writes, while the single-ended bit-line was used to decrease the complexity in the figure. Figure 3.6 (a) depicts a single level multiplexer architecture in which two adjacent columns of 512 cells are multiplexed into a single sensing amplifier.

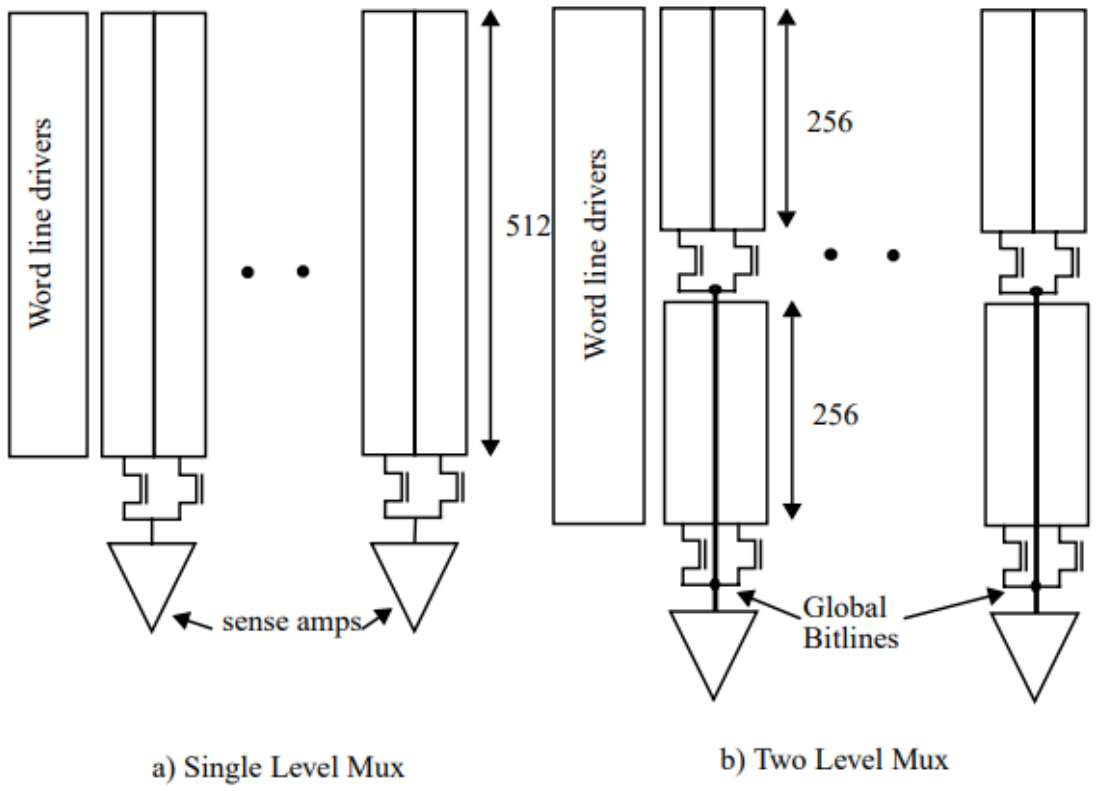


Fig. 3.6: Bit-line MUX architecture [11].

Figure 3.6b depicts a two-level structure. In the above two level structure first level multiplexes the two 256high column. The above output can be multiplexed in second level to generate the global bit-lines, which feed into the sense amplifier. The I/O lines, which will be connected to the output of every other SA to the I/O ports, can also be used for hierarchical MUX .A memory cell is highly weak due to its small size, which limits the bit-line slew rate when read is done. As a result, SA's are employed to magnify the bit-line signal in order to detect signals as low as 100mV. In a traditional architecture, the sense amplifiers continue to slew after sensing the bi-tines, subsequently resulting in a significant voltage difference. Because the bit-lines have a high capacitance, this results in severe power waste. We can control the amount of the charge pushed down by the bit-lines and so reduce pd by restricting the word line pulse width. We suggest a strategy in this thesis to manage the word line pulse width has to just be wide enough. For the sense amplifiers to consistently sense and block the bit-lines from slewing even more over a wide variety of operating circumstances.

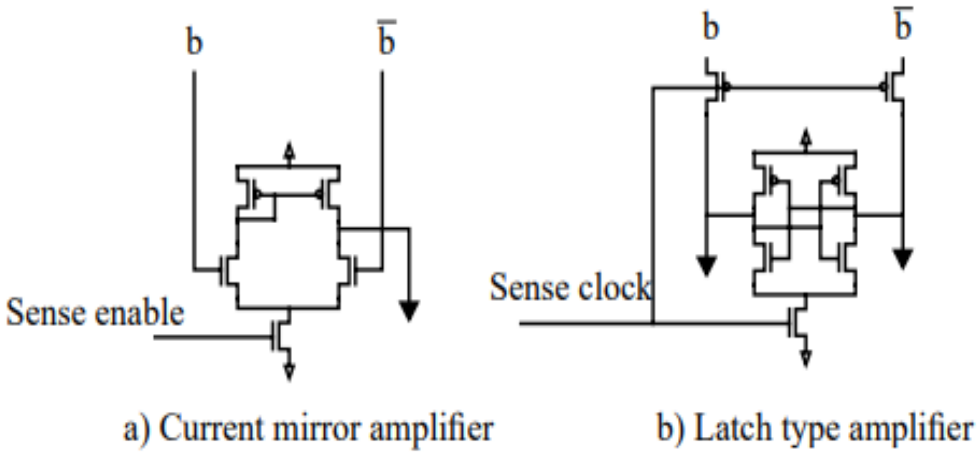


Fig.3.7: Two different type of sense Amplifier a) Current mirror type b) Latch type [11].

There have been a variety of SA circuits presented in the past, but generally they fall into two categories: linear amplifiers and latch amplifiers [10]. A simple prototype of each class is shown in Figure 3.7. The linear amplifier type (Figure 3.7a) requires a DC bias current is to set it up in high gain area before the bit line signal arrives.

There are several levels of amplification necessary to change the little swing bit line signal to a full swing Complementary MOS signal. These Amplifiers are commonly seen in high-end designs. Low Voltage and low power designs are not recommended since they take the biasing power and will operate over a limited supply voltage. The latch type designs are generally used in these designs (Figure 3.7b).

Due to the extra timing margins, the sense clock timing is typically modified for a worst case operating as well as process conditions, which bring it down under, average situations.

The outputs of SA's are connected to the I/O lines in big SRAMs, adding another level to data flow hierarchy (Figure 3.2). The signal is transported between Memory blocks and RAM I/O ports through the I/O lines. Because the power consumption of these lines can be severe in high access width SRAMs, signalling on these lines is also done via tiny swings. We'll use the low swing bit-line technique to lower the power of the I/O lines as well.

# CHAPTER 4

## SRAM DESIGN PRINCIPAL AND PARAMETER

A memory is one of the biggest inventions for the device which is used for storing the data or information. It is a very essential electronic component which is used in the computation field and many more. It is also used for transferring the data from one system to another system for example flash memory.

Similarly, a semiconductor memory is also very essential part for computer processing technology. Basically, it is the main memory element for the processor or any system on chip (SOC). We all know this is the era of system on chip, and this system of chip having to perform many complex tasks for many systems. For this it needs a high-speed memory inside it which can take the instruction and from the main memory for the system on chip (SOC). If we talk about the semiconductor memory then it is very much capable to do this. It has very fast in compare to normal memory system.

Semiconductor memory are also classified same as ordinary memory. ROM, PROM, EPROM, SRAM and DRAM are the different type of semiconductor memory. The semiconductor memories are fabricated using the transistor. Mainly CMOS technology used to fabricate this kind storing element. Among the all the different types of semiconductors some of them is going to describe only RAM, because RAM is the most used semiconductor memory.

The semiconductor memory is mainly classified into two types that is RAM and ROM, and RAM further classified into two types

- DRAM
- SRAM

### 4.1 DRAM

DRAM is the type of memory which is frequently utilized in computer systems. The acronym DRAM refers to "dynamic random access memory.” Its cell structure is shown in the figure given below. The DRAM cell diagram contains one bit line and one word line.

One capacitor is connected followed by NMOS pass transistor. The information store in the DRAM in the form of charge and by the charging and discharging the data stored in the DRAM cell that can be find out. To store the data, we have to charge the capacitor and to read the data from the DRAM we have to discharge the capacitor.

For read or write we have to give address line high because here pass transistor is N type, and we all know that NMOS is on only when we give high to its input. So, for read and write NMOS must be on. And if NMOS is on then we should give the data to the bit line whatever data we want to store. And the data will store in the capacitor through the NMOS.

Similarly, if we want to read the data then at that time NMOS must be on then we can access the data. But in this case capacitor will discharge and it will lose the data.

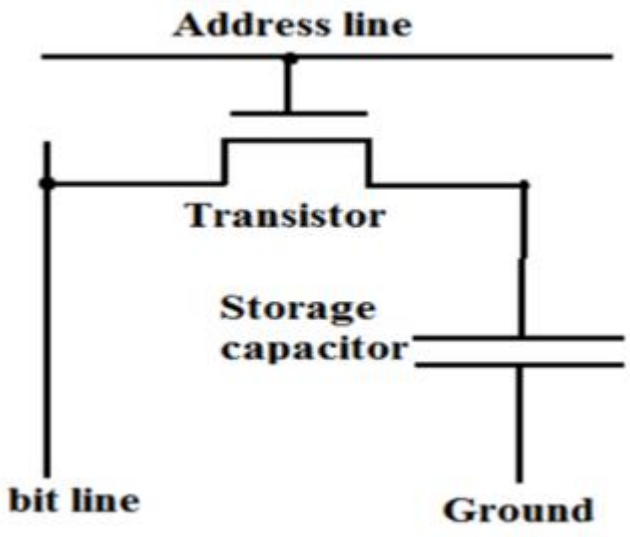


Fig. 4.1: Schematic of dynamic RAM [9].

We have already discussed that when we read the data from the DRAM then the capacitor will lose its data, because during read operation it will discharge. That's why we need to refresh it periodically. Due to this reason, it is known as dynamic RAM.

### 4.2 SRAM

The SRAM contain two couple inverter, which is used as storing element. SRAM stands for static random-access memory. Before understand its work, it's better to understand the diagram first it give the proper idea. The outline of SRAM can be seen in figure given

below. This is the conventional 6T SRAM, we can see that the SRAM contain only 6 transistors.

To make this conventional SRAM we need 4 N enhancement type and 2 P enhancement type transistors. Here N3 and N4 are the pass transistor which is N-type. Other 4 transistor are used for making cross couple inverter. Two-bit line is available in both right and left side, which is connected to NMOS from side. One word line is there.

### 4.2.1 IMPORTANCE OF SRAM

There are different level of memory grading which have been added in the primary memory of any processor to narrow the gap between the CPU's performance and the other storage speed (typically dynamic Memory) [35]. This hierarchy ranges from on-chip, low-speed memories to external, high-speed memory like DRAM and hard drives. Processors aim to keep commonly

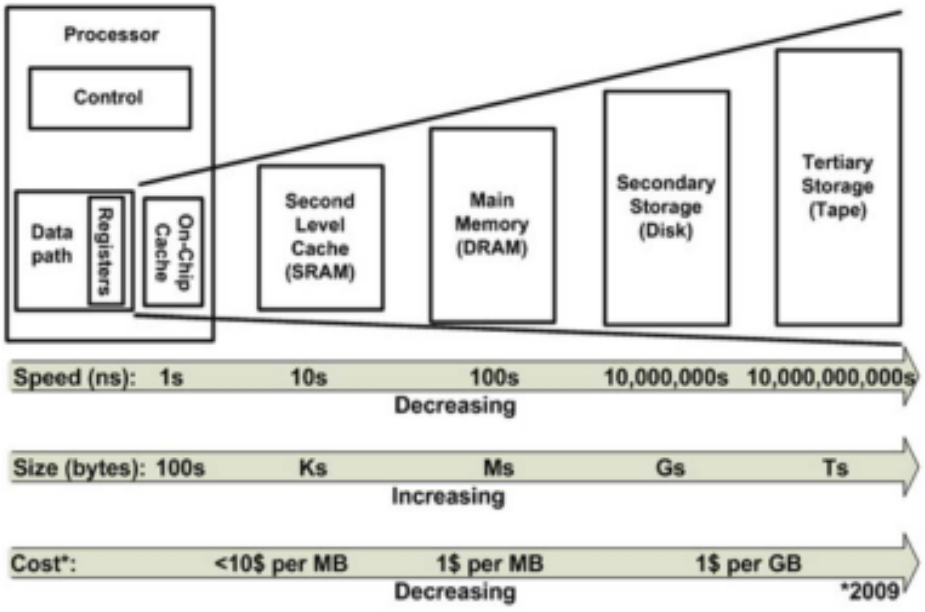


Fig. 4.2: Hierarchy of memory [11].

Used instructions and data close to themselves in fast on-chip memory known as cache (data speed is superfast) or scratchpad (it is quickest method) memories. A typical memory hierarchy of a modern computer system is shown in diagram 4.2.

On-chip cache memory is classified into three levels: L1, L2, and L3 cache memories, each with a different capacity and speed. The storage capacity of a lower-level cache is lesser, but it is much faster than the other memories . While the cache memories are managed by hardware and are hidden from view by the main processor, certain processors use memory allocator memories. CPU is controlling the all Scratchpad storage device, and software can determine whether data or instructions require storage in scratchpad memories. SRAM is used to develop both scratchpad and cache memory. To satisfy the demands, CPU which has highest performance and system on chip (SOC) is demanding additional on-chip memory, Actually SOC are application specific and it increase the performance it increases the operational speed. However, because to space and cost constraints, huge amounts of SRAM cannot be integrated into the chip.

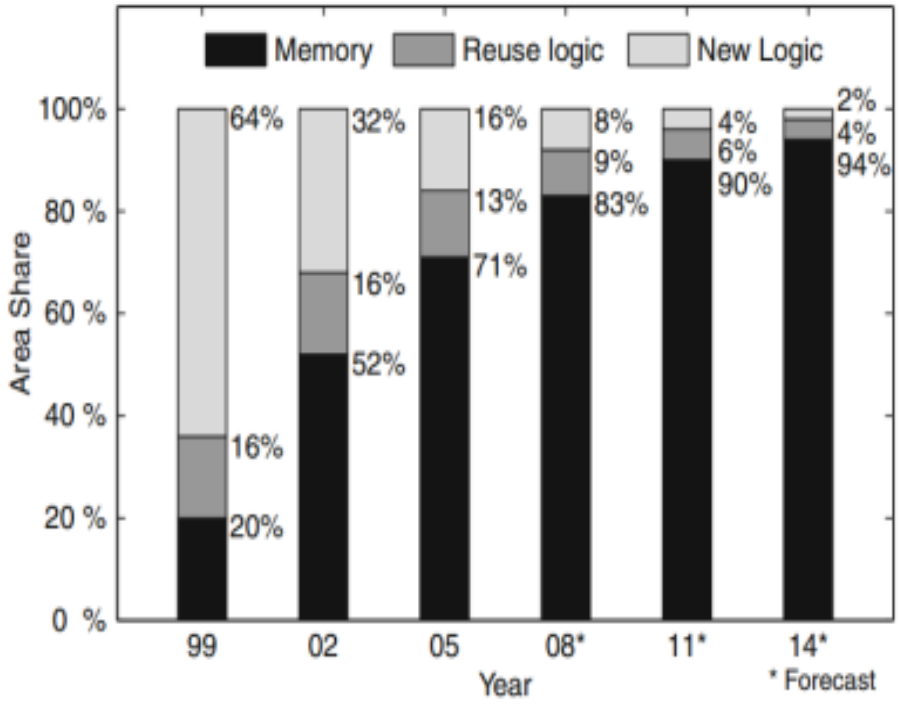


Fig. 4.3: Trend and area of memory on system on chip (SOC) [13].

On a SOC (system-on-chip), Diagram 4.3 depicts the trend of logic are and Embedded memory, which has very high speed. This figure shows that how much SRAM on a chip has increased almost two times in last one decade. The demand of highly performing chip or processor are increasing but it can achieve by embedded a large number of high-speed on-chip memories, drove this massive development. This trend supports the massive efforts and ongoing research into SRAM, which aims to improve reliability while lowering cost and energy consumption, particularly leakage power. Because SRAM takes up a lot of space and leakage in the processor or a chip is totally depend on the amount of transistors in the design, because if number of transistor will be more the leakage will be more or area, area is also responsible for leakage. Any attempt to reduce SRAM leakage will improves the entire design.

### 4.2.2. ARCHITECHTURE OF SRAM

A collection of SRAM bit-cells (or cells) and peripheral circuitry make up SRAM. Address decoders for all columns and rows, sense-amplifiers, bit-line pre-charge circuits, write drivers and other peripheral circuitry facilitate writing, and reading into SRAM cells. Figure 4.4 depicts a traditional SRAM memory design with $2^n$ words of$2^{m+k}$. SRAM is accessible using 2k words. Thousands or even millions of identical cells make up an SRAM array. for illustration, we can take a 4 Mb SRAM which demands 4,194,304 bit-cells, and even minor improvements in design requirements like static power have a huge impact on the overall processor design or SOC design. High-performance processors face two significant challenges: speed and cell area, both of which designers are working to address. Energy consumption and dependability are the major or primary problems for energy-constrained applications and battery-powered devices. In this project, I want to reduce the leakage of SRAM memory bit-cells in order to lower the system's leakage power.

The memory bit-cell is the main component of an SRAM memory or we can say it is the building block of the memory, which stores single bit of data. A single word-line (WL) connects memory bit-cells in a row, allowing bit-cells to access in that row. In a column of memory cells, bit-line pairs (bit-line BL and bit-line bar BLB) are being used for reading and writing values to the cells and from the cells.

Memory having High capacity is arranged in a fashion that has the same horizontal and vertical dimensions or order. As a result, a word line allows for many memory words, with column decoders used for picking the addressed memory word. Column multiplexers connect the selected columns' bit-line (BL) and bit-line -bar (BLB) to the sensing amplifiers used for reading

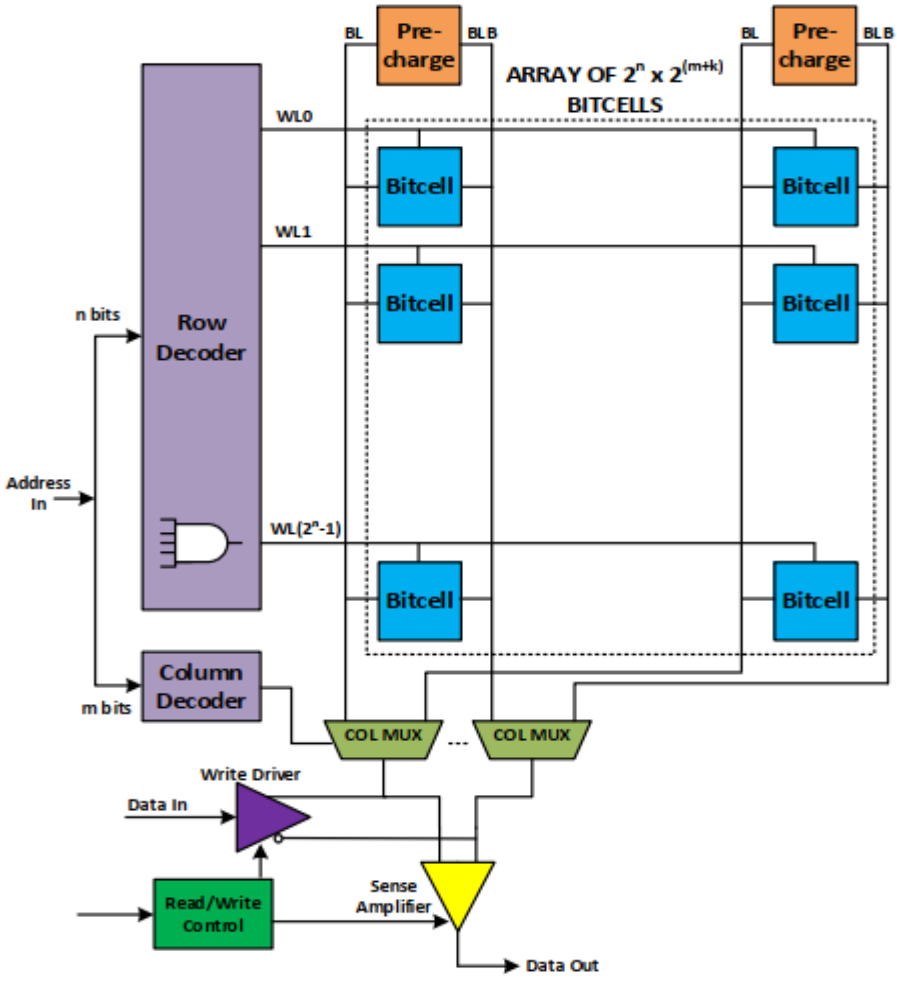


Fig. 4.4: Architecture of SRAM [14].

The cell value and write drivers for writing into cells. Row decoders are used for decoding the memory's address and trigger the memory array's associated row.

### 4.2.3 BITCELL OF SRAM

SRAM's basic building component is the bit-cell, which stores single bit of data. A basic SRAM bit-cell consists of six transistors which are shown in Figure 4.5. Four of them are NMOS and rest two are PMOS. Two pair of inverter are cross coupled connected back to back and form a one bit storage element. To create a one bit of storage element we require four transistors. Rest two are used for reading and writing the data from storage element. These two are known as the access transistors.. It is connected to the word line, also known as WL line. Because the access transistor is N type, so it will be activated when supply will be logic high. As word line connected to NMOS so during reading and writing operation it must be high. Otherwise no operation will be performing. When word line is high the NMOS will be one provide zero resistance path between drain to source and when word line is at logic low the it provide high resistance between the drain and source.

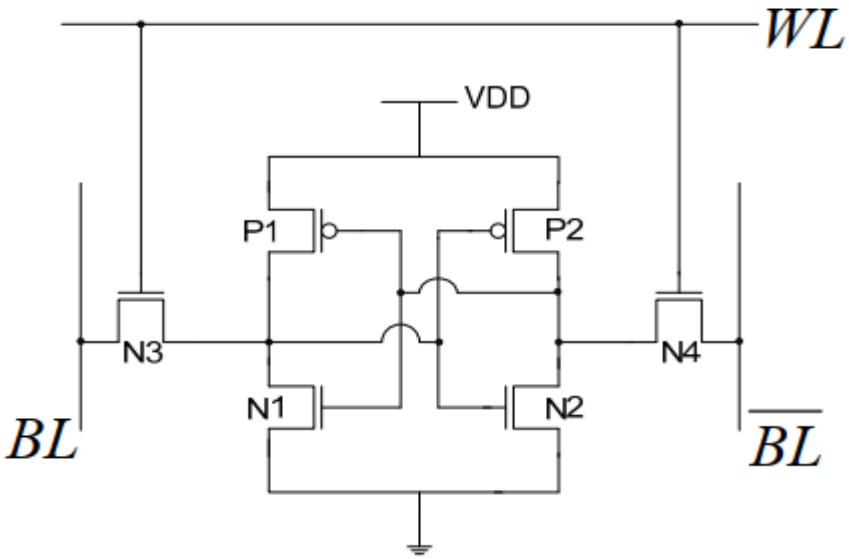


Fig. 4.5: Bit-cell of SRAM [6].

### 4.2.4 SENSE AMPLIFIERS

Sense amplifiers are a crucial SRAM peripheral among all the peripheral. The fundamental purpose of sensing amplifiers is to identify and transform the small differential voltage created during read from the bit-cells on bit-line (BL) and bit-line (BLB) to a logical value [37]. and it is also responsible for the speed of read operation of SRAM Figure 4.6 depicts a typical current mirror sensing amplifier.

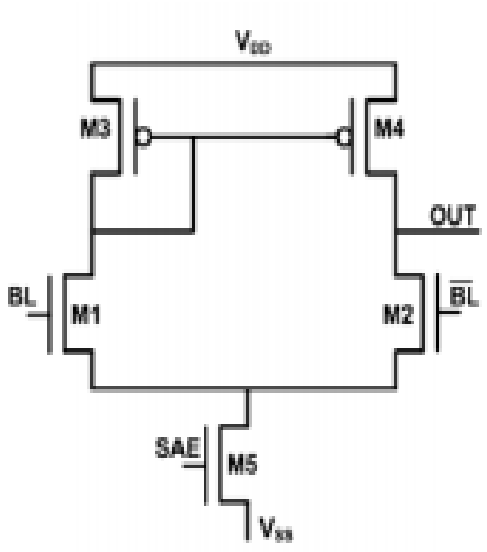


Fig. 4.6: Sense amplifier of current mirror type [8].

### 4.2.5 PRECHARGE CIRUIT

A bit-line and bit-line-bar (BL and BLB) are coupled in SRAM to a pre - charge circuit for each bit-cell in a column. The pre-charge circuit are required to speed up during the read and write process. Because the access transistors in SRAM bit-cells are NMOS transistors which is good at passing zero, and bad at passing one. N enhancement type transistors do not conduct high voltages well because they cut off when the voltage source goes Vdd-Vth. Before any operation, a pre-charge cycle is performed to speed up read and write operations in SRAM. Since PMOS transistor are good at passing one so -Two PMOS transistors are attached to BL and BLB in the pre-charge circuit, and a pre-charge circuit enabling signal controls the gate of these two PMOS transistors. BL and BLB are linked to Vdd when the

control signal is low. As indicated in, there may be another PMOS that is utilised to equalise BL and BLB.

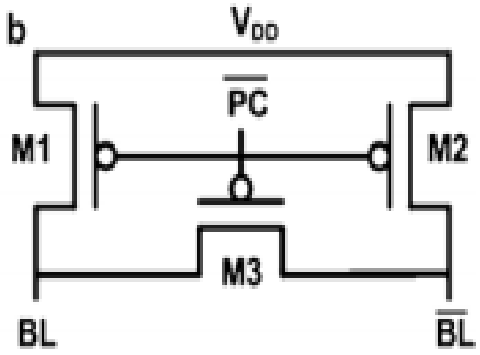


Fig. 4.7: Pre-charge in SRAM [8].

### 4.2.6 WRITE DRIVERS

When write operation is performing BL and their counterparts (BLB) are driven by write drivers. The write driver only needs to draw down the correct bit-line because Bit and Bit-bar are pre-charged to Vdd on each operation. Figure 4.8 shows an examples circuit for a write driver utilising pass gates. The WE signal is being used for enabling SRAM writing.

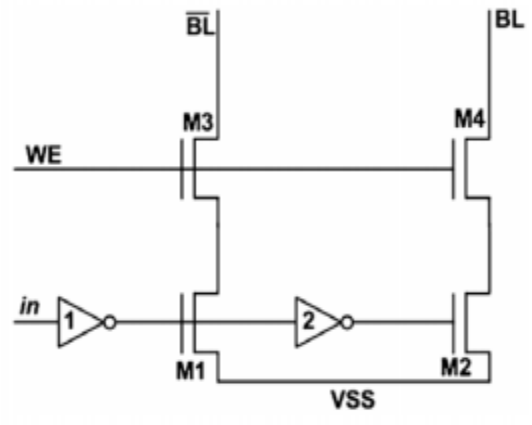


Fig. 4.8: Pass gate are used in write driver

## 4.3 READ OPERATION AND WRITE OPERATION

To read the data or the information from the SRAM, the pass transistor must be on. Here in this figure N4 and N3 both is the access transistor. To on this transistor 1(high) should be given to the word line so that it can turn on the pass transistor. Then we need a sense amplifier for recognize the stored data. The pre-charge bit-line and bit-line bar both are attached to the sense amplifier. Read process can be perform by using the single bit line but by using these two it can increase the speed of read operation.

To perform write operation pass transistor (N3 and N4) must be turn on like as read operation because the NMOS give direct access to the storing element or latch form element. Then we give the value to bit line whatever value we want to store in the cell.

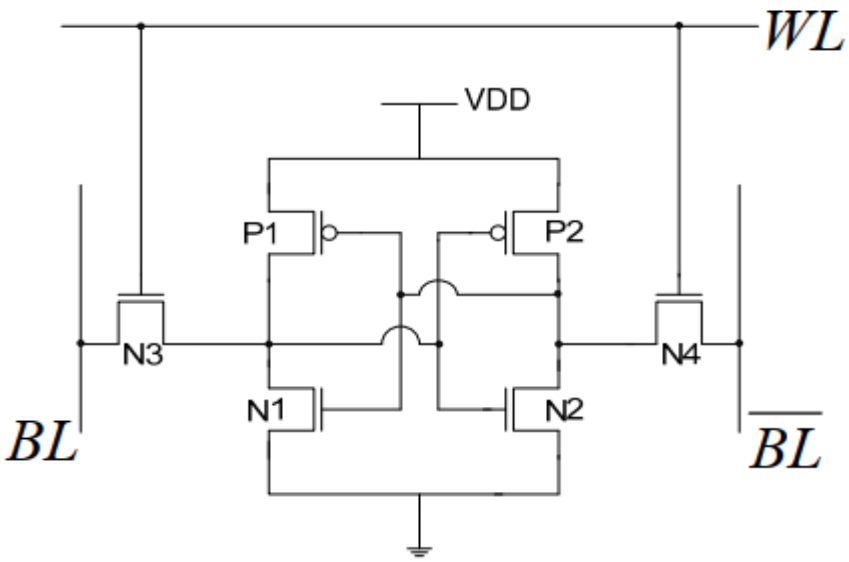


Fig. 4.9: Cell diagram of conventional 6T SRAM [4].

## 4.4 HOLD OPERATION

In the hold state the word line is given logic zero and when the value of word line is logic zero then the transistor (NMOS) whose gate is connected to this will be off because NMOS is working only when the logic given to its gate will high. When the gate of NMOS is given logic zero then it provide high resistance path between drain to source. Because word line is connected to the gate of NMOS due to this reason the access transistor of both side is

become off and The bit line and bit line bar are disconnected from the storage cell because the access transistor give high resistance value in off state. In this state SRAM can hold the data or information. In this state it will not allow the reading and writing process.

### 4.5 COMPARISON BETWEEN SRAM AND DRAM

- Different memory used for different purpose like SRAM is used as a cache memory, whereas DRAM is used as main memory.
- SRAM is very fast comparing to DRAM.
- SRAM need 6 transistors to design whereas DRAM needs only one transistor along with one capacitor, so SRAM is costlier than the DRAM.
- Density of SRAM is low where density of DRAM is high.
- Power consumption in the SRAM is less compare to DRAM.

### 4.6 PERFORMANCE METRICS

Now it is going to discuss about some parameter according to that we can decide we can decide whether following RAM is good or bad.

### 4.7 CELL RATIO and PULL RATIO

For the satisfactory operation of SRAM cell, the appropriate device sizing must be required. For that we must follow the design principal for the SRAM topology.

Cell ratio and pull up ratio is the design principal which help the SRAM to improve the stability. Cell ratio is defined as width of pull-down transistor divided by width of access transistor, whereas pull-up ratio is defined as width of pull up transistor.

If the cell ratio is greater than 1 then the read stability of the SRAM will increase. Pull down transistor that is NMOS should be much stronger than the access transistor and the pull up transistor to increase the read stability of SRAM pull up ratio should be less than 1for better write stability.

### 4.8 STABILITY

It is a useful metrics used to design SRAM cell. It has been used for years as a useful metric for optimizing the design of SRAM cell. It can able to predict the effect of parameter variation. We can calculate the cell stability by calculating the noise margin for the

memory. It is traditionally used for long time. The noise margin represents the cell ability to tolerate a certain presence of noise. Noise can be either current or voltage. The noise margin is measured in terms of electric variable.

### 4.9 POWER DISSIPATION

Power dissipation in SRAM cell involves following two major components.

1. **Dynamic power consumption:** The power dissipation happens when the circuit is in active mode. When output is changes with respect to change in input, in that case the load capacitor is charged or discharged. Due this reason we lose some power is known as dynamic power consumption.

$$E_c = \frac{1}{2}.C_L V_{DD}^2 \qquad (1)$$

2. **Static power loss:** The loss due to the leakage current in transistor in classified as the Static power loss. As technology is shrinking day by day leakage current is also increasing with it. The total leakage current can be given by following equation.

$$I_{total\ leak} = I_{(sub\_th)} + I_{(gate)} + I_{junction} \qquad (2)$$

### 4.10 STATIC NOISE MARGIN (SNM)

SNM is static noise margin, The SRAM have two cross couple inverter static noise margin is the minimum required voltage to flip the storage data or information. Static noise margin can be obtained by voltage transfer characteristic curve of both inverters plotted on the same graph. Figure 4.10 is representing the SNM curve of the SRAM. The stability of the SRAM can be decided by the largest size of square that can fit between the butterfly curve or the lobs

Read SNM is defining when the read operation is performed. During the read operation the access transistor is one. In this case we draw the butterfly curve by considering the inverter and the access transistor. Then read SNM is decided by the largest square that can fit into the butterfly lobe.

Write SNM is little bit different from the read SNM. The both access transistor is on during the write operation. When we separate the both inverters to draw the VTC curve

then it is not symmetric like Read SNM, its VTC curve cuts each other at Vdd which shows that it is mono stable. This is better for write stability in SRAM. Then the write SNM is also decided by the largest square that can fit into the butterfly lobe.

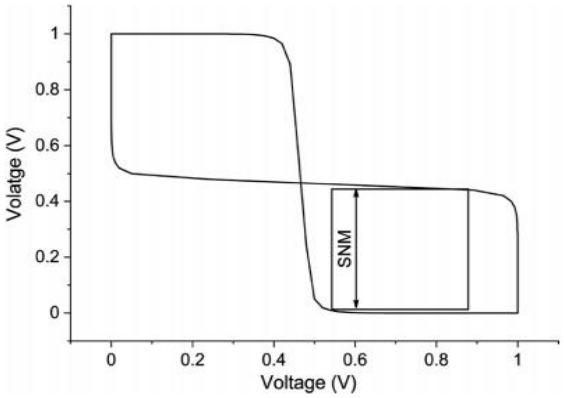


Fig. 4.10: Butterfly curve of SRAM [6].

- N-curve method - this is the alternative method of butterfly cure. It is used to determined noise metrics. In this method, a voltage sweep, VIN is applied at the storage node Q from 0V to the maximum voltage Vdd. Then the relation between the current and voltage is plotted in a single plane. In this graph current is taken at Y axis and voltage is taken to the X axis.

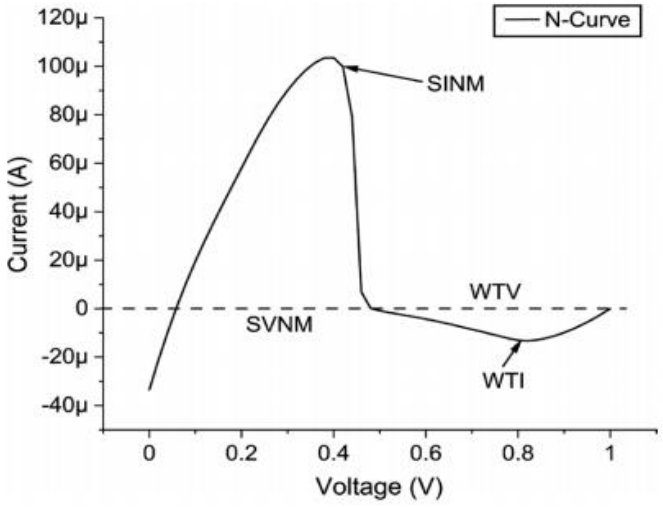


Fig. 4.11: Extracted N-curve [6].

The read stability is measured by static voltage noise margin and static current noise margin, and the write stability measured by the write trip voltage and write trip current.

# CHAPTER 5

## LEAKAGE POWER IN SRAM

In present day every electronic device which is used today are portable. Almost every portable device is runs on battery. So, designing the circuit which consume less energy and give high performance is very much important. It also affects the design process of the chip. So, we need different new technique which should not be power hungry. Complementary MOS (CMOS) devices have been scaling down in the last 30 years in order to get this type of chip with low leakage current and great performance. Area and delay were major concern in 70's and 80's. But complexity increased with the time and task of testing more difficult. After chip is manufactured then testing is done to find the defect in fabrication. Now size of chip is decrease to reduce the delay. But due to small size of the chip there is increase in leakage current. So, we need technique or we can say that we need a new design rule so that the product will consume less power. If the design circuit will consume less power can embedded with the device will increase the battery life of the device.

A scaled technology can have less area and can increase the speed but it comes with some issues, which are given below:

1. The drainage current can be increased in the device with a low threshold voltage.
2. There is reduction of worst-case performance of a chip.

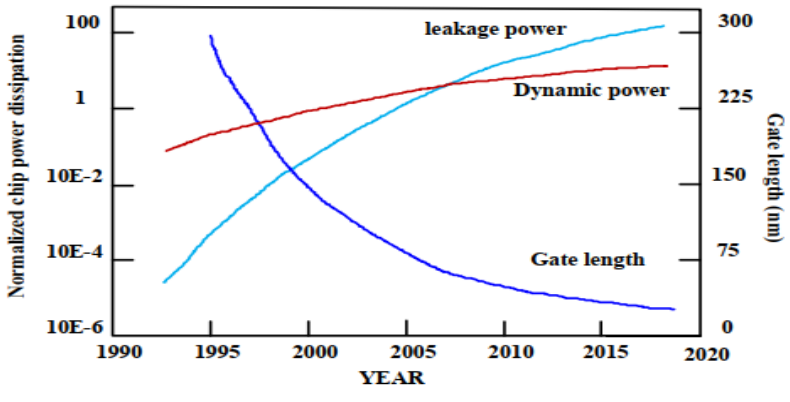


Fig. 5.1: Leakage power in a chip [4].

According to the ITRS (international technology roadmap for semiconductors), the Drainage power dissipation is shown in Diagram 5.1.For the high performance of the chip transistors are scaling down. It increases the performance undoubtedly, but it becomes the reason for the more leakage current. Leakage current of a single transistor is very less but for making a chip there are millions of chips are required, and then this leakage current become countable. Figure 5.2 shows the components that affect the leakage current.

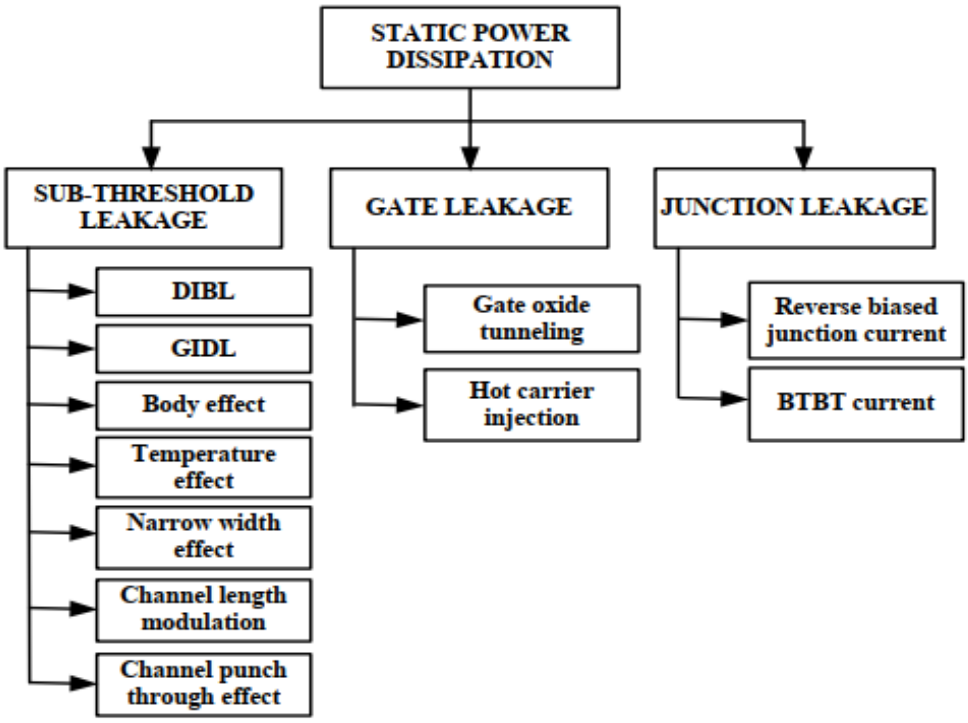


Fig. 5.2: Leakage current in MOSFET [9].

There is some leakage currents depend when there is no channel is present. That is when Vgs smaller than the Vt (threshold voltage). This current is directly proportional to the exponent for Vgs-Vt. The DIBL current is depending upon the voltage between the highest and lowest terminal. Gate leakage current is eventually tunnelling through the oxide. In MOSFET oxide is resemble as the capacitor and it provide the very high resistance and practically there is no current is passing through this. But there some tunnelling and this tunnelling can be more if it gets thinner. It is totally depending on the thickness of the oxide layer. The equation [4] represents the total leakage current.

$$I_{total\ leak} = I_{(sub\_th)} + I_{(gate)} + I_{junction} \quad (3)$$

## 5.1 LEAKAGE CURRENT IN TRANSISTOR

In order to construct a low-power SRAM, it is critical to minimise transistor leakage current. Some of the leakage current MOSFET is listed in below:

- Sub threshold leakage current
- Gate tunneling leakage current
- Gate induced drain leakage current
- Punch through leakage current

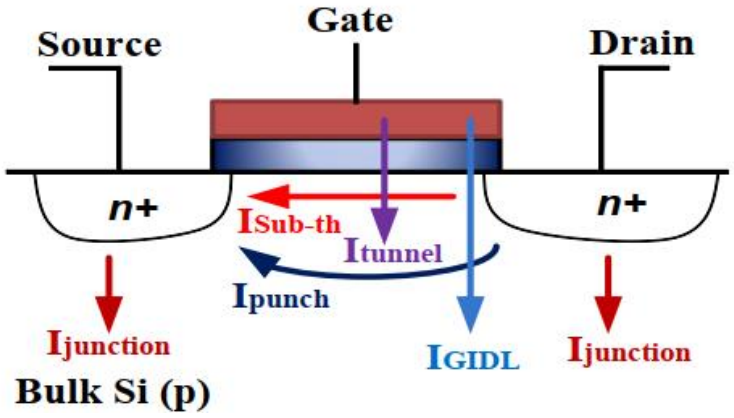


Fig. 5.3: Drainage currents in a NMOS transistor [9].

### 5.1.1 SUB THRESHOLD LEAKAGE CURRENT

At the point when the Gate to Source Voltage (Vgs) is not exactly the semiconductor's edge voltage, sub-limit spillage current creates (Vto). The Drainage current flows between the MOSFET's two terminal. This current causes the transistor to dissipate static power. The less leakage current there is, the less static power dissipation there is, and the more reliable the device is. Sub-threshold current grows exponentially as temperature rises.

$$I_{D(weak\ inversion)} = I_{on} \cdot e^{vgs/v_{th}} \qquad (4)$$

### 5.1.2 GATE INDUCED DRAIN LEAKAGE CURRENT

Under a high electric field, gate-induced drain leakage occurs due to band-to-band tunnelling at the gate and drain overlap area. When the depletion layer at the interface decreases electric field increases. This type of current increases due to various factors such as reducing oxide thickness of gate, low threshold voltage devices and when there is more potential difference between Drain and Gate terminals.

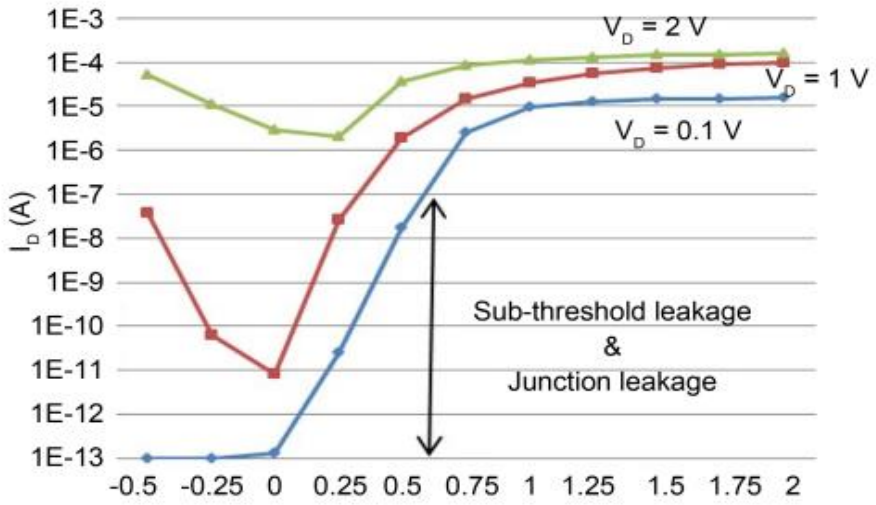


Fig. 5.4: Gate source voltage vs. drain current [7].

### 5.1.3 PUNCH THROUGH LEAKAGE CURRENT

Due to the source and drain depletion zones are close together and their junctions expand into the narrow channel, punch-through current is more common in small-geometry MOS transistors. The following methods can be used to lower this type of current:

- Small Oxides
- Substrate doping High
- Junctions are preferably long.

$$X_{dD} = \sqrt{\left[\frac{2 \in_{si}}{qN_A}\right](V_{DS} + \emptyset_{si} + V_{sb})}$$

$$X_{dD} = \sqrt{\left[\frac{2 \in_{si}}{qN_A}\right](\emptyset_{si} + V_{DS})}$$

The sub threshold surface diffusion current ($I_{Sdif}$) for the short channel at its saturation level can be express as: -

$$I_{\$dif} \propto Dn_i^2 \,.\, e^{(\frac{q\Delta\emptyset_S}{kT})/L_{eff}} \quad (5)$$

### 5.1.4 GATE TUNNELING LEAKAGE CURRENT

The strong electric field created over the tiny gate oxide layer causes gate tunnelling current. The device structure and biasing circumstances have a big impact on gate tunnelling current. Electrons tunnel from the gate to the bulk and from the bulk to the gate region in a high electric field, passing through the intermediary layer, the gate oxide layer. Due to the narrow width of the potential barrier, highly charged electrons can quickly enter or pass through the oxide layer. The gate current is increased. The charged electrons in n+ poly silicon can easily pass-through gate oxide and enter the gate when the gate voltage (Vg<0) is applied, which is known as Gate Current. The current of gate tunnelling can be characterised as follows:

$$I_g = I_{gc} + I_{gso} + I_{gdo} \quad (6)$$

# CHAPTER 6

# LEAKAGE POWER REDUCTION TECHNIQUES

We have already seen in previous chapter that we are losing some energy and power in SRAM just because of leakage current. We have also seen the different leakage current in transistor due to which we are losing the power and energy. We can reduce this kind of power lost by applying some design technique. These design techniques can not reduce the leakage power completely but it can save some energy. So, some design techniques are given below:

## 6.1 TRANSISTOR STACK

To minimize leakage current in the SRAM transistor stacking technique can be used. In this method or technique, we are connecting the transistors in series. Fig. 6.1 is representing the example of this technique. In each stage leakage current is reducing, because the resistance is increasing.

- In stacking technique NMOS transistor is used. In this configuration voltage from drain to source in decreases, and this lead to reduce in DIBL and also the other leakage current.
- Here the Gate to source voltage is not more than zero, therefore it also helps in the reduction of sub threshold leakage current.
- In this configuration the voltage from Substrate to source voltage is negative too. Therefore, due to body effect threshold voltage will increase. Hence sub threshold leakage current is reduced.

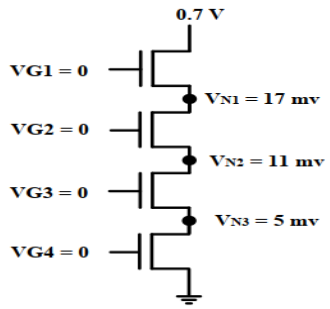


Fig. 6.1: Stacking Technique [7].

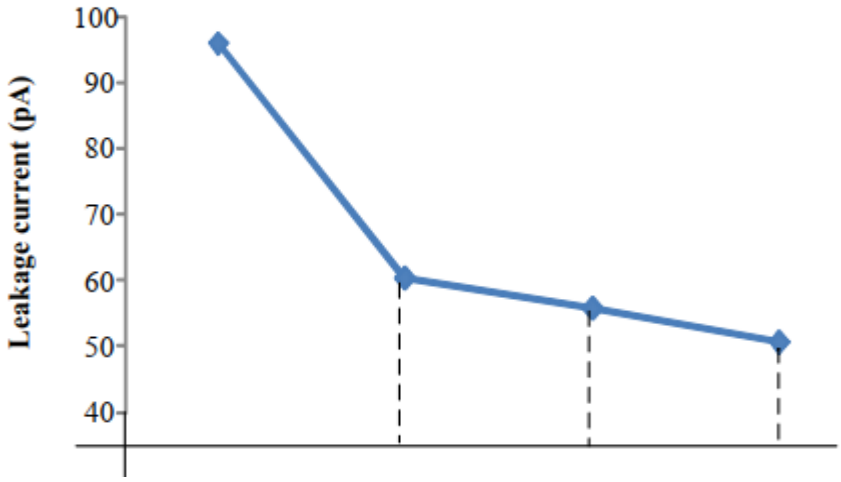


Fig. 6.2: Curve of leakage current

A novel P4-SRAM cell has shown in the figure 6.3. There are 4 NMOS and 4 PMOS are present in this configuration. It is containing 2 more transistor than the conventional 6T SRAM. The 2 PMOS are stacked together and placed between the Vdd and ground. It works as a conventional 6T SRAM when WL (word line) is given low and these PMOS will be off when word line is given high. This P4-SRAM cell configuration is used for reducing the sub threshold leakage current.

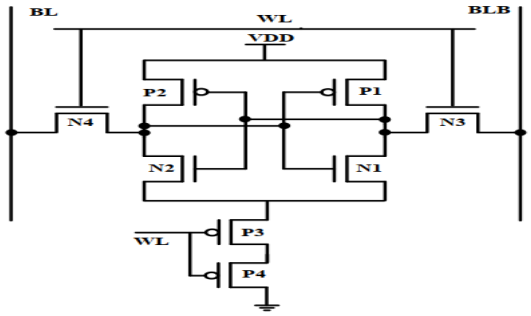


Fig. 6.3: P4-SRAM design [7].

### 6.1.1 AREA ISSUES IN STACKED TECHNIQUES

One of the biggest drawbacks of employing stacked transistors in SRAM cells could be area. Because in stacked technique more transistor are connected in series. Here attached one figure down below in order to compare the area. It is clearly seen that the area consume more in case of stacked transistor.

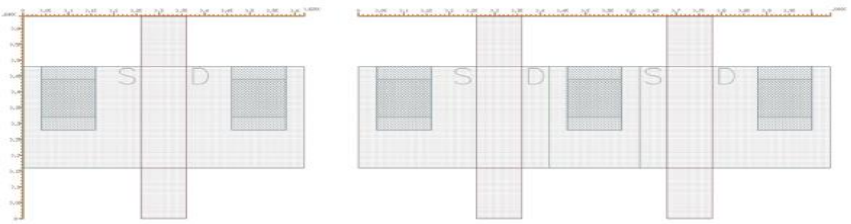


Fig. 6.4: Area comparison [11].

## 6.2 GATING TECHNIQUE

In fig. 6.5 another technique is introduced for reduction in the leakage current. This method of power reduction is very much popular in the industry. This method is known as gated technique. To design the gated technique we required 7 transistors, that is one more transistor is required than the conventional 6T SRAM. The extra NMOS transistor is place between the Vdd and the ground. This configuration work as conventional 6T SRAM when control signal is given high, and when control signal is given low NMOS will be off. Thus, this configuration reduces the leakage current by eliminating the path between the Vdd and ground.

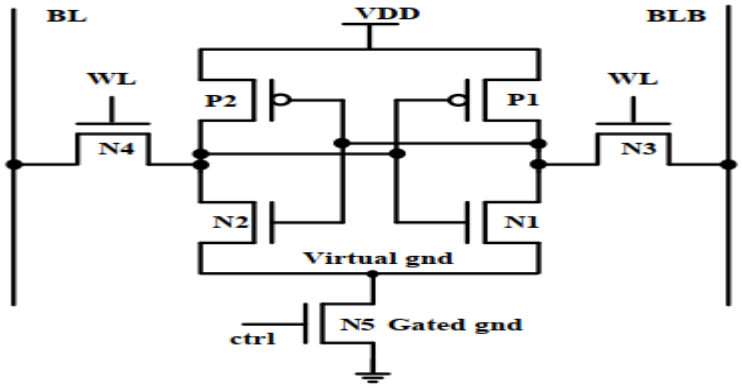


Fig. 6.5: Gated SRAM cell [8].

## 6.3 GATED WITH N CONTROL SRAM

Fig. 6.6 represents the Gated with N control SRAM cell. Its working is very much similar with Gated SRAM cell. It can disable the path between the Vdd and the ground. This technique is used to minimize the leakage current and optimize the delay. For optimizing the delay different transistor are used with different threshold voltage. The transistors under

doted circle have high threshold voltage than the other transistor. Transistor with low threshold voltage is used for high speed.

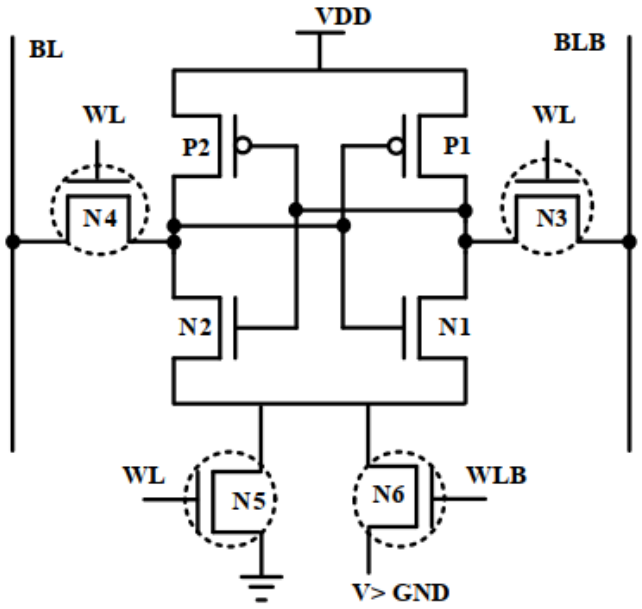


Fig. 6.6: NC SRAM cell [4].

# CHAPTER 7

## SIMULATION AND RESULT

In present era of microprocessor SRAM become the unavoidable part of it. But leakage current of the SRAM makes it more challenging. As size of the transistors are shrinking this leads to increase in leakage current. There is different type of leakage current are available (explained in previous chapter) which makes SRAM power hungry. Therefore, design engineer always tries to make SRAM with minimal power consumption.

In this chapter simulation has been done. Different kind of SRAM circuit is simulated and the parameter like SNM and leakage current is calculated. In SRAM there are problem of power loss as discuss in previous chapter, like static, dynamic and short circuit power loss. To reduce or minimize these losses there are different technique. Here through the simulation it is tried to minimize the static power. For that different stacked transistor method is used. In stacking technique NMOS and PMOS transistor is used. The schematic diagram of stacked transistor is shown below (fig. 7.1). For simulation purpose cadence virtuoso tool is preferred here. To analyse its stability butterfly curve is used.

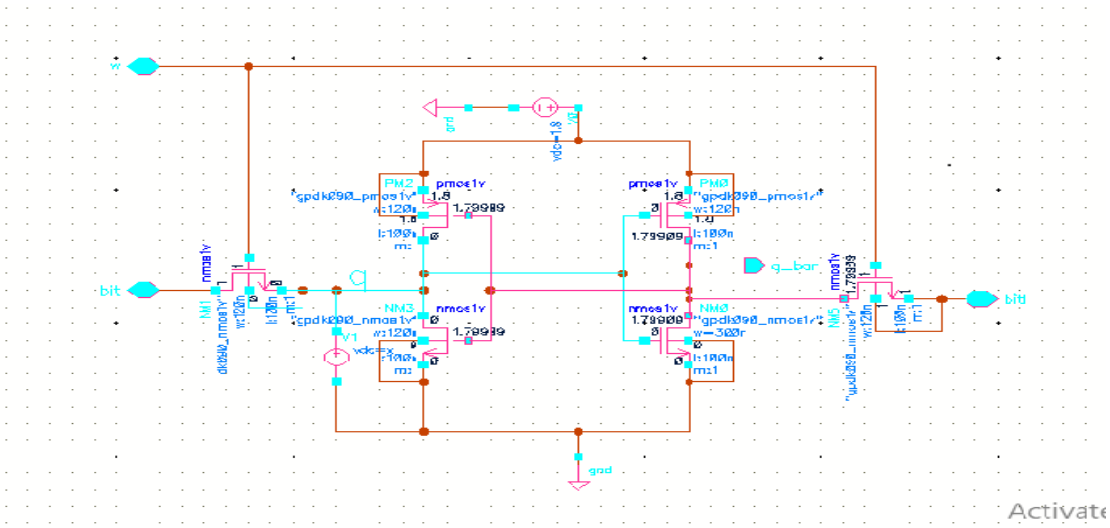


Fig. 7.1: Schematic of 6T SRAM

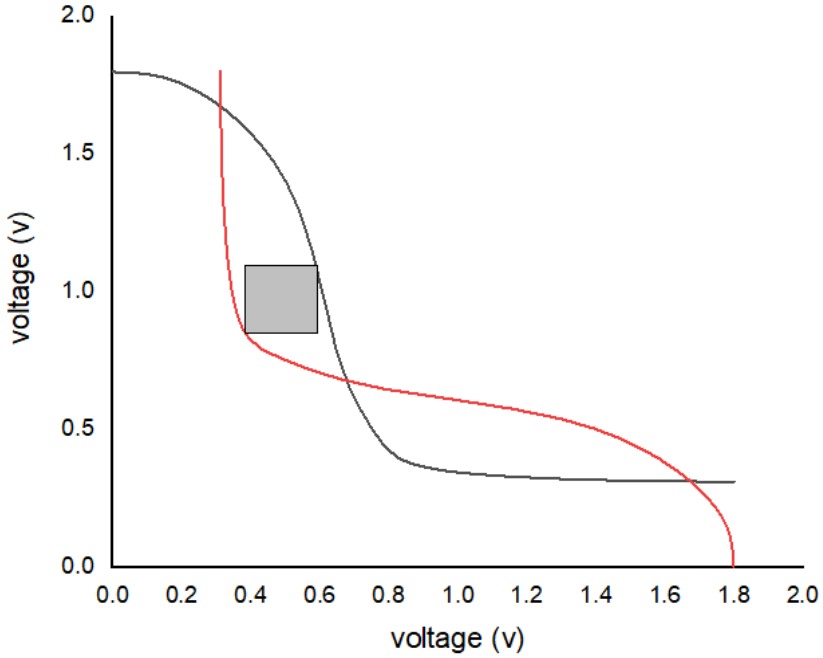


Fig. 7.2: SNM curve of 6T SRAM

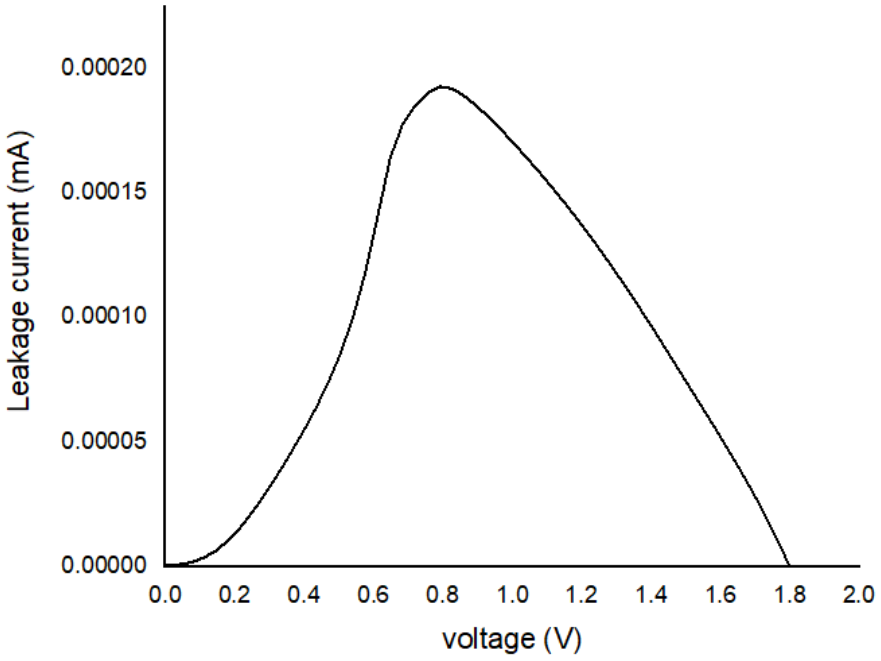


Fig. 7.3: leakage current of 6T SRAM

The above diagram fig. 7.1 is representing the conventional 6T SRAM. The transistor used here is based on 90nm technology. Fig. 7.2 and fig. 7.3 represent the SNM and leakage current for conventional 6T SRAM. The SNM for 6T SRAM has come 0.335V, and leakage current has come 388.07nA.

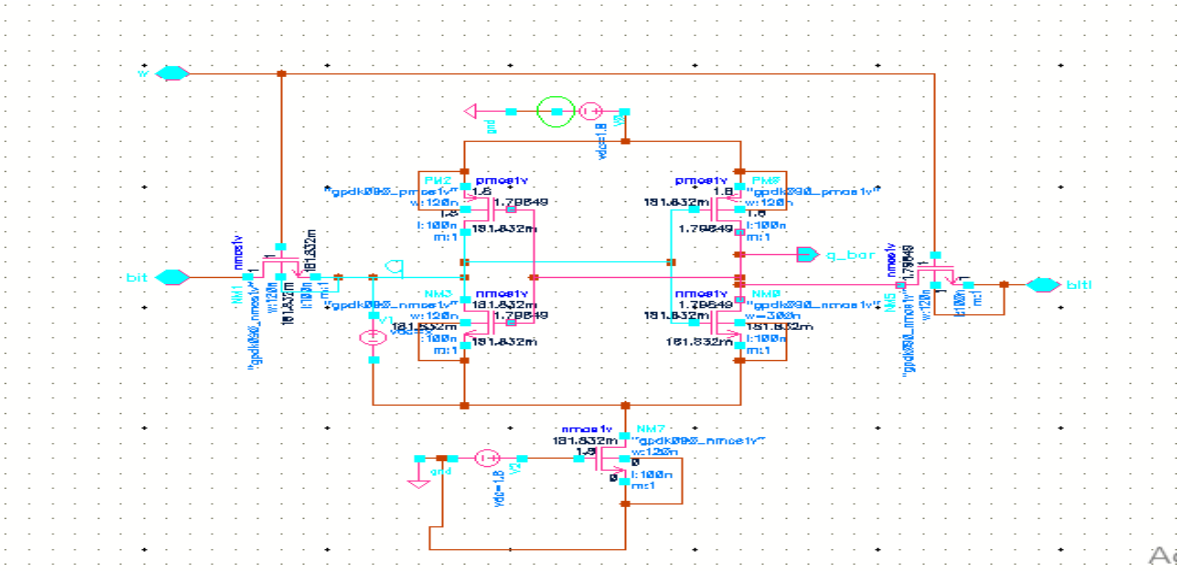


Fig. 7.4: Schematic of 2nd topology

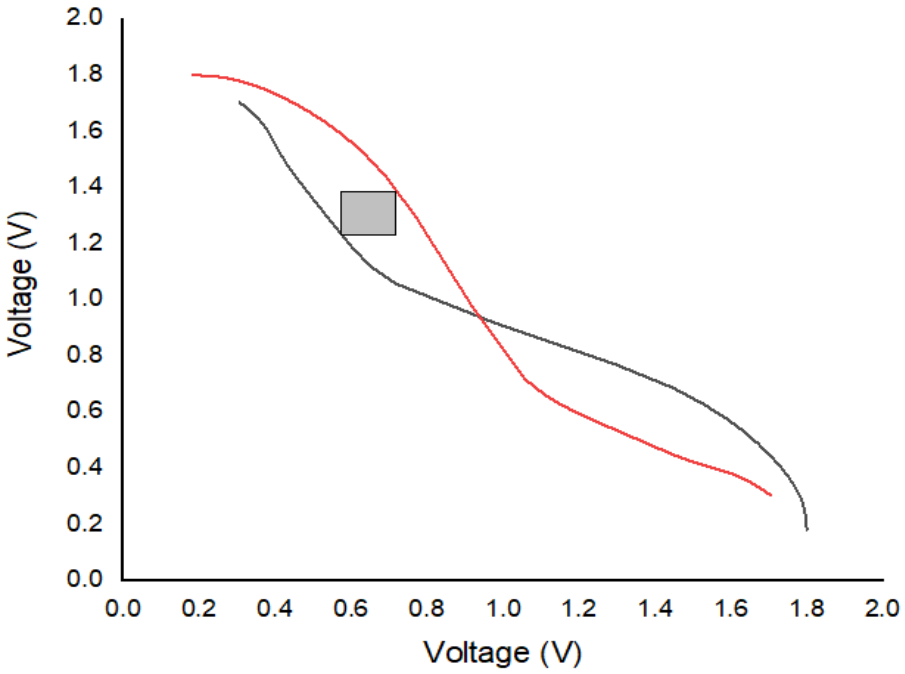


Fig. 7.5: SNM of 2nd topology

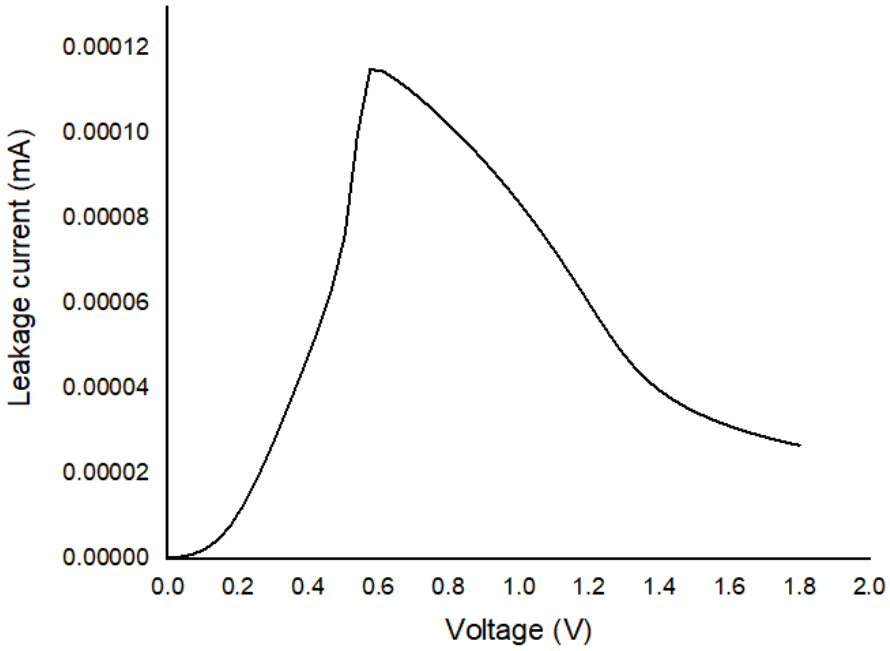


Fig. 7.6: leakage current of 2nd topology

The circuit diagram in fig. 7.4 is the new schematic of the SRAM. This SRAM represent the stacked technique and very much similar to the conventional 6T SRAM. But one extra transistor is added in between the cell and ground. This SRAM is simulated and extracted SNM and leakage current. The value of SNM and leakage is 0.240V and 235.59A. Stability of this SRAM is better than the conventional SRAM and leakage is current is also less in compare to the conventional 6T SRAM. But it also come with one demerit that is it need lager area than the conventional 6T SRAM.

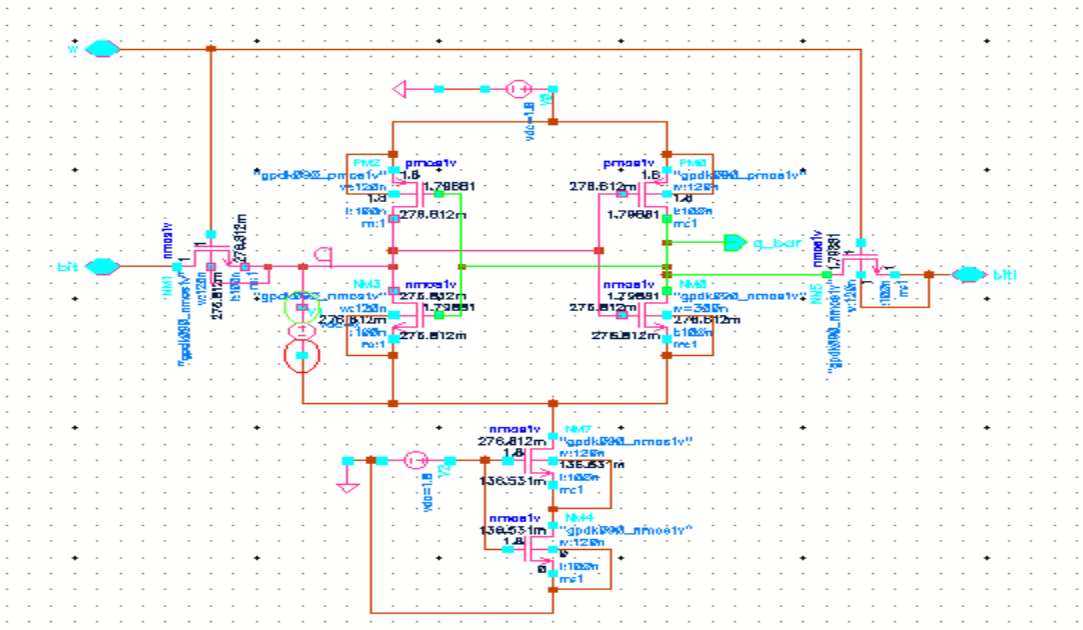

Fig. 7.7: Schematic of 3rd topology

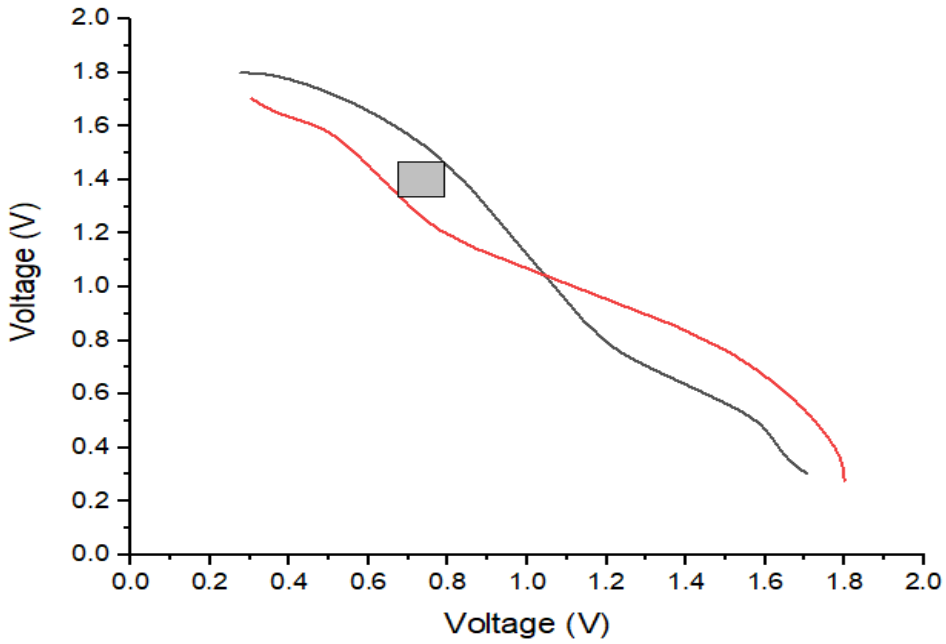


Fig. 7.8: SNM curve of 3rd topology

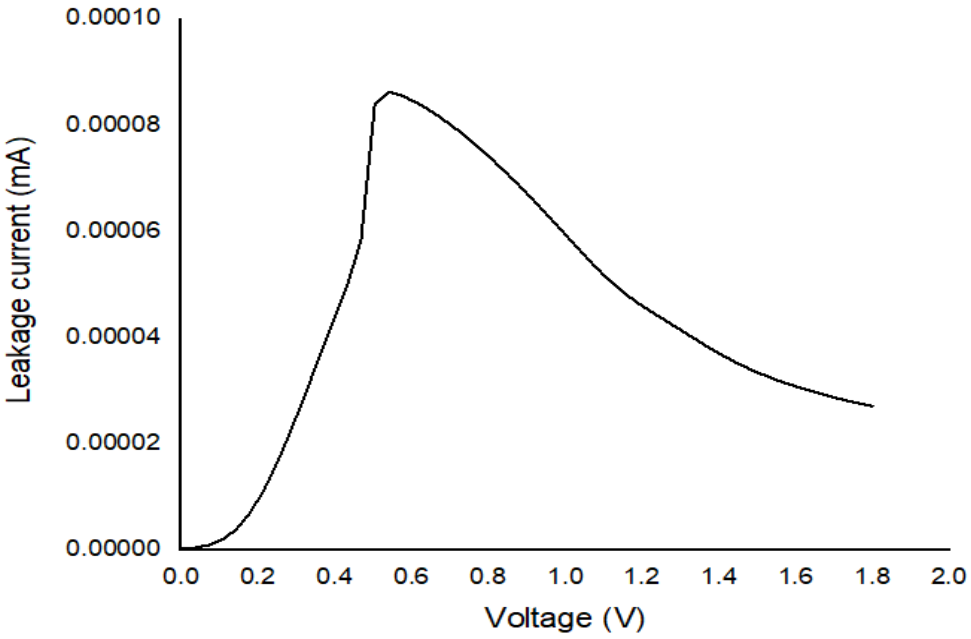


Fig. 7.9: leakage current of 3rd topology

The schematic diagram in the fig. 7.7 is representing the new stacking technique. Here two extra transistor is added to the conventional 6T SRAM. This extra transistor is added in between the storage cell and ground. After the simulation of this SRAM SNM and leakage current is calculated. The value of SNM is calculated from this schematic is 0.175V, and the leakage current is 218.83nA.

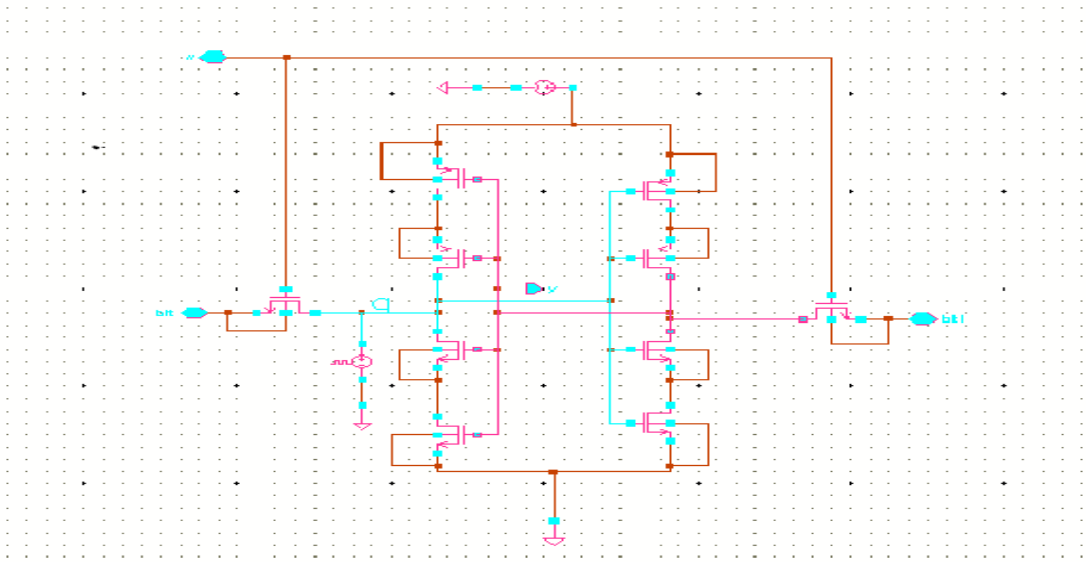

Fig 7.10: Schematic of 4th topology

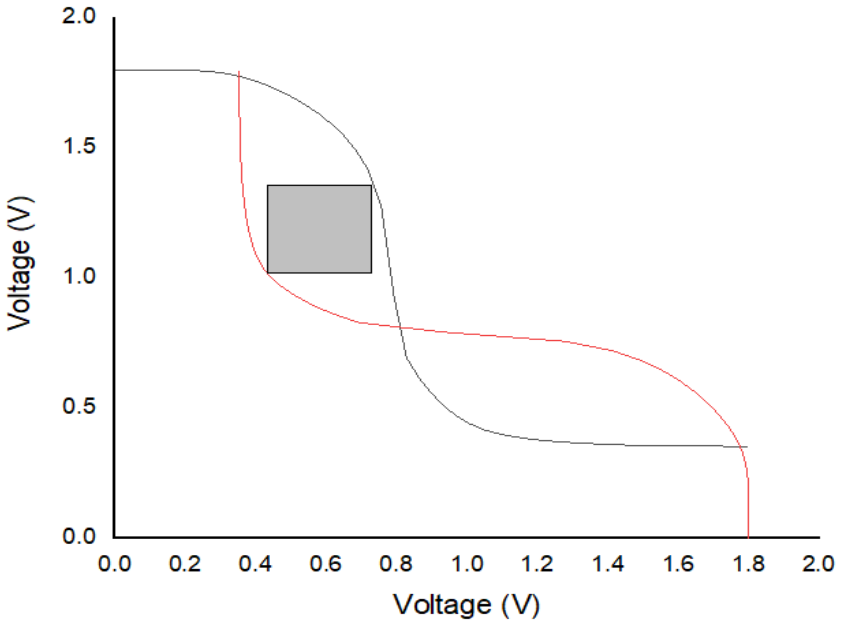


Fig. 7.11: SNM of 4th topology

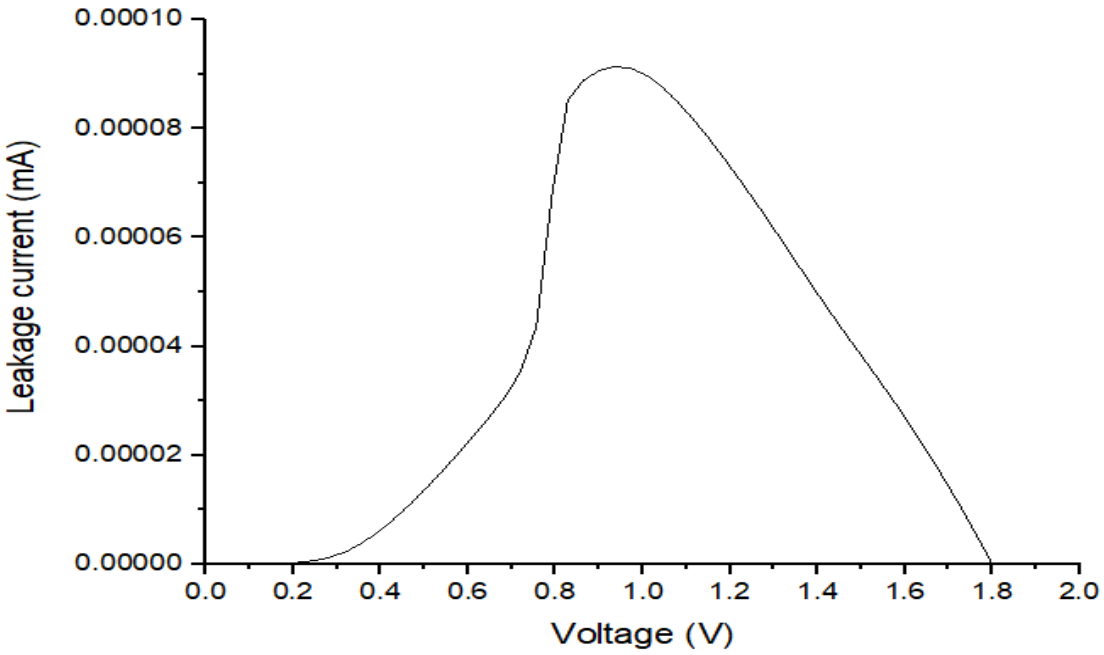


Fig 7.12: leakage current of 4th topology

Fig. 7.9 represent the another schematic of SRAM. This SRAM contains 10 transistors, 4 of them is PMOS and rest is 6 are NMOS. The storage cell of conventional 6T SRAM cell contain only 4 transistors, but this new schematic contains 6 transistors is the storage cell. SNM and leakage current of this schematic is calculated 0.439V and 30.040nA.

**COMPARISON**

| TOPOLOGIES | SNM | LEAKAGE CURRENT | NO. OF TRANSISTOR |
|---|---|---|---|
| 6T SRAM | 0.335 V | 388.07 nA | 6 |
| 2nd Topology | 0.24 V | 235.59 nA | 7 |
| 3rd Topology | 0.175 V | 218.83 nA | 8 |
| 4th Topology | 0.439 V | 32.78 nA | 10 |

The data of this table gives has taken from the above circuit simulation. It gives the idea about the stability and the leakage current of those circuit. The leakage current of 6T SRAM is highest among all the circuit, but takes least number of transistors. The last one SRAM has given lowest leakage current among the all circuits. But it need more numbers of transistors.

# CHAPTER 8

# CONCLUSION

To minimize the leakage current from conventional 6T SRAM, a modification has been done in the conventional 6T SRAM cell. In this modification extra transistors are used in order to reduce the leakage power. Those extra transistors are connected in the series, it is known as stacking technique. In stacking technique extra transistor is used. This leads to increase the overall area of the SRAM. But it reduces the power loss by decreasing the leakage current.

In 2nd topology one extra transistor is used and tried to understand the stability of SRAM and also tried to analyse that when we make the schematic of SRAM then how it effect the stability of conventional 6T SRAM. It gives better static noise margin than the 6T SRAM. The leakage current is less. It reduces the leakage current by 40.45%, than the 6T SRAM cell and its performance are better than the 6T SRAM with different temperature.

Again 6T SRAM is modified with the two extra NMOS transistor. This transistor is placed between the storage cell and the ground. In this stacking technique also give better performance than the 6T SRAM. Better SNM can be getting here. The SNM of 2nd and 3rd topology have nearly same. It also reduce the power loss by the minimizing the leakage current. It reduces the leakage current by 54.29% than the 6T SRAM cell. It also gives better performance than the 6T SRAM cell with different temperature.

The 4th topology requires 10 transistors. It gives better noise marine as well as lesser leakage current than the 6T SRAM. It reduces the leakage current nearly 9 times than the 6T SRAM. The Noise Margin of 6th topology is far better than the 6T SRAM. So overall 6th topology is better than among all the above topologies, with one demerit it will take more are because of 10 transistors.

# REFERENCES


1. Shokoufeh Naghizadeh1, · Mohammad Gholami2, "Two Novel Ultra-Low-Power SRAM Cells with Separate Read and Write Path" Springer Science Business Media, LLC, part of Springer Nature 2018.
2. Debasis Mukherjee,Hemanta Kr.Mondal,‖Static Noise Margin Analysis of SRAM Cell
   For High Speed Application‖, IJCSI International Journal of Computer Science Issues,
   Vol. 7,Issue 5,September 2010.
3. Jan M.Rabaey Anantha Chandrakasan Borivoje Nikolic ‖Digital Integrated Circuits‖,
   Pearson Education Electronics ,2003.
4. Sung-Mo Kang and Yusuf Leblebici ‖CMOS Digital Integrated Circuits‖, TATA McGRAW-HILL EDITION 2003.
5. Kunihiko Yamaguchi, Hiroaki Nambu, et. al. ―A 1.5-ns Access Time, 78-pm' Memory-Cell Size, 64-kb ECL-CMOS SRAM‖, IEEE Journal of Solid-State Circuits,
   Vol. 27, No.2. February 1992.
6. Rakesh Dayaramji Chandankhede ―Design of High Speed Sense Amplifier for SRAM‖, 2014 IEEE International Conference on Advanced Communication Control and Computing Technologies (ICACCCT).
7. Sreerama Reddy G M, P Chnadrasekhara Reddy, ‖Design and implementation of 8Kbits Low Power SRAM in 180nm Technology ‖,Proceedings of the International MultiConference of Engineers and Computer Scientists 2009 Vol II IMECS 2009,March 18-20,2009.
8. Harekrishna Kumar1 · V. K. Tomar,"A Review on Performance Evaluation of Different Low Power SRAM Cells in Nano-Scale Era"Springer Science Business Media, LLC, part of Springer Nature 2020.
9. PavankumarBikki, PitchaiKaruppanan, "SRAM Cell Leakage Control Techniques for Ultra Low Power Application: A Survey "scientific research publication,Motilal Nehru National Institute of Technology, Allahabad, India, February 2017.
10. K. Sasaki, et. al., "A 15-ns 1-Mbit CMOS SRAM", IEEE Journal of Solid State Circuits, vol. 23, no. 5, pp. 1067-1071, October 1988.
11. M. Matsumiya, et. al., "A 15-ns 16-Mb CMOS SRAM with interdigitated bit-line architecture", IEEE Journal of Solid State Circuits, vol. 27, no. 11, pp. 1497-1502, November 1992.
12. Anantha P. Chandrakasan and Jan M. Rabaey, "Digital Integrated Circuits: A Design Perspective".

13. M. Yoshimoto, et. al., “A 64kb CMOS RAM with divided word line structure”, I983 IEEE International Solid State Circuits Conference, Digest of Technical Papers, pp. 58-59.
14. T. Hirose, et. al., “A 20nS 4Mb CMOS SRAM with Hierarchical Word Decoding Architecture”, 1990 IEEE International Solid State Circuits Conference, Digest of Technical Papers, pp.132-13.