STUDY AND SIMULATION OF SECOND GENERATION VOLTAGE CONVEYOR AND ITS APPLICATION

A DISSERTATION

SUBMITTED IN PARTIAL FULFILMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE

OF

MASTER OF TECHNOLOGY

IN

VLSI DESIGN & EMBEDDED SYSTEMS

Submittted By:

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UNDERTAKING

I **Sumit Gangwar**, **Roll No. 2K20/VLS/21** student of M.Tech (VLSI Design & Embedded Systems), hereby declare that the project Dissertation titled "**Study and Simulation of Second Generation Voltage Conveyor and Its Application**", which is submitted by me to the **Department of Electronics & Communication Engineering, Delhi Technological University, Delhi** in the partial fulfillment of the requirement for the award of the degree of **Master of Technology** is my original work. I have not plagiarized or submitted the same work for the award of any other degree. In case this undertaking is found incorrect, I accept that my degree may be unconditionally withdrawn.

Date: 30/05/2022 Sumit Gangwar(2K20/VLS/21) Place: Delhi

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CERTIFICATE

I hereby certify that the work contained in the project Dissertation titled "**Study and Simulation of Second Generation Voltage Conveyor and Its Application",** submitted by **Sumit Gangwar, Roll No. 2K20/VLS/21** in the partial fulfilment of the requirement for the award of degree of Master of Technology in VLSI Design & Embedded Systems to the **Department of Electronics & Communication Engineering**, Delhi Technological University, Delhi, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree of Diploma to this university or elsewhere.

Date: 30/05/2022
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ABSTRACT

Low-power design for portable devices is becoming increasingly crucial in today's environment. This entices researchers to seek for the best solution while minimising compromises with other characteristics like as speed and area. Power consumption is becoming a critical aspect in chip design as the density of transistors on a chip rises in order to meet high performance requirements. Power dissipation is becoming a serious challenge as transistors are being scaled down.

In this project I am working upon “Second Generation Voltage Conveyor (VCII)”. VCII is based upon dual concept of CCII block. VCII is a three terminal device. It provides voltage realization atouput port. I am simulating a VCII Block using LTspice.We have used TSMC level 8, 180nm node parameter in our simulation. This block comprises of 2 stages 1st one is current buffer stage and 2nd one is voltage buffer stage. I have performed its DC analysis as current buffer and as a voltage buffer. I have calculated its impedance at all three ports. In this report I will discuss its functionality and and advantage over Op-Amp. and CCII block in detail.

In this report I will present the changes I have made, in current buffer stage, and in voltage buffer stage. In the previous simulation I used the current buffer stage with single output, this time I will use the differential current buffer stage and voltage buffer stage. These stage promises much better bandwidth, stability, and low power results in comparision to previous one. I will also implement application using this voltage conveyor. We will simulate the 1st order Low pass, High pass and Band pass active filters, current to voltage converter, voltage to current converter, voltage differentiator, voltage integrator,voltage buffer, current buffer, and perform AC analysis,DC and transient analysis.

ACKNOWLEDGEMENT

It gives me immense pleasure to present this Dissertation work for the partial fulfillment for the award of degree of Master of Technology in VLSI Design & Embedded Systems. I owe special debt of gratitude to my supervisor **Dr. Rajeshwari Pandey**, Professor in Department of Electronics and Communication Engineering, Delhi Technological University, Delhi for their constant support and guidance throughout the course of my work. Their sincerity, thoroughness and perseverance have been a constant source of inspiration for me.

I would also like to thank all other faculty members of Electronics and Communication Engineering Department, DTU for their valuable suggestions and co-operation at every step in this project. I would also like to thank my parents and batchmates for their constant motivation throughout this work. Last but not the least I would like to thank Almighty for His invisible presence and constant support.

Date: 30/05/2022 Sumit Gangwar (2K20/VLS/21)

Place: Delhi

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LIST OF ABBREVIATIONS USED

VLSI: Very Large Scale Integration

CCII: Second Generation Current Conveyor

VCII: Second Generation Voltage Conveyor

Op-Amp: Operational Amplifier

Ckt : Circuit

IC: Integrated Circuit

NMOS: n-Type Metal Oxide Semiconductor

PMOS: p-Type Metal Oxide Semiconductor

DC: Direct Current

CD: Common Drain

CG: Common Gate

CHAPTER 1

INTRODUCTION

This chapter sets the stage for Second generation voltage conveyor (VCII). In section 1.1 we have discussed about basic property of VCII block. In section 1.2 we have discussed about the motivation behind doing this project. In section 1.3 we have discussed the property of a buffer circuits. In section 1. 4, 1.5, 1.6 we discussed general properties of a buffer and amplifier circuits. We have discussed about the concept of impedance matching and impedance requirement for a voltage amplifier.

1.1 INTRODUCTION:-

In today's environment, power, area, and speed are becoming increasingly significant variables in virtually every electronic business. These three variables are intertwined and trade-offs exist. The Second Generation Voltage Conveyor (VCII) is based on the duality idea of the CCII block. The VCII block has the finest Power, Area, and Speed ratio. It has a larger frequency range than an Op-Amp, uses less power, and takes up less space. The VCII block allows for cascading, which is a particularly valuable feature in higher-level architecture.

1.2MOTIVATION

Because of the inadequacies of the CCII block, researchers moved their focus to VCII. When voltage is required at the output port in a design application, we need to use the CCII block to provide a voltage buffer to the output side. As a result, the circuitry required increases, resulting in higher power and area requirements. Some CCII-based applications have significant limitations, for example, when examining the transfer function of a voltage differentiator, voltage integrator, current to voltage converter, and voltage amplifier, two CCII blocks are required instead of one that necessitates more power and space [1]. Other

circuits produced by the CCII block, such as the current amplifier, current differentiator, and current integrator, also have issues, such as their reliance on input or output impedance or gain issues.

All of these issues drew researchers in, who set out to find the best solution for all of them. For all of these issues, the VCII block produces excellent performance. Because only a single VCII block is required, it has a minimal power and area demand.

1.3 BUFFER:-

A voltage or current buffer is a circuit that processes an input signal with a gain of one. Buffer circuitry is commonly utilised when a transition in high input impedance to low input impedance or low to high input impedance is required. When impedance matching is necessary, a buffer can be employed.

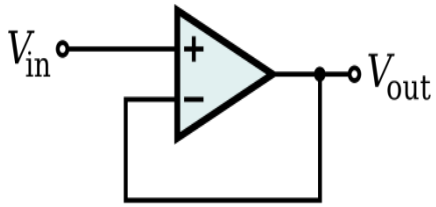

Figure 1.1: Voltage buffer circuit designed using Op-Amp

1.4 IMPEDANCE MATCHING:-

Impedance matching is a power transfer optimization approach. The signal reflection from the load circuit is minimised using this technique. For minimum signal reflection, the input and output impedances should be matched in this procedure.

1.5 HIGH INPUT IMPEDANCE:-

A high input impedance is a characteristic of a good voltage amplifier (ideally infinite). A voltage amplifier has a greater input impedance to ensure that the signal applied to the input stage is almost ready for further processing, or to avoid loading effect at the input port.

1.6 LOW OUTPUT IMPEDANCE:-

The output impedance of a good voltage amplifier should be low (ideally zero). Low output impedance is necessary for greater fanout, allowing the output stage to drive the largest number of devices possible. It aids in cascading and higher-level design. On the other hand for current buffer circuit output impedance should be high.

CHAPTER 2

REVIEW OF DIFFERENT TYPES OF VOLTAGE AND CURRENT BUFFER CIRCUITS

In this chapter we will discuss about the various method of current and voltage follower circuit design. We will review functionality of those buffer circuits, advantage of using these circuits and shortcomings associated with them. In section 2.1 we will discuss about the different type of voltage buffer circuits like circuits which are operating in differential mode, which are suitable for high voltage operation, which provide high slew rates, high value of input impedance and low value of output impedance. We will also discuss and simulate the voltage follower circuit which we are using in our proposed design. In section 2.2 we will discuss about the current buffer stages. In current buffer circuits we have reviewed circuits on the basis of the functionality they promised like low value of input impedance, high value of output impedance, differential nature, ability of high current sourcing and sinking capability, low power consumption etc. We have also simulated the current buffer stage which we are going to use in our proposed design. We performed AC, DC, transient and power consumption analysis.

2.1 VOLATAGE BUFFER:-

The voltage is passed from the 1st circuit to the 2nd circuit without any modification in amplitude in a voltage follower, also known as a voltage buffer or unity gain voltage buffer. The output voltage is simply a reflection of the input voltage. The voltage follower's voltage gain is one (Av = 1). Although there will be no voltage gain, there will be significant current gain. When a voltage follower is linked in between two circuits, it transfers voltage from one to the other without changing the amplitude and drives the 2nd circuit without overloading the 1st.

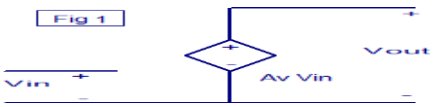

Figure 2.1: Small signal model of Ideal Voltage buffer circuit

The voltage buffer is a type of analogue cell that is utilised in the construction of analogue circuits. Large capacitive loads are driven with it at maximum speed and low power consumption. This means that symmetrical slew rate and minimal static power consumption are required. The negative slew rate in a standard voltage buffer (=Ibias/CL,where CL The bias current limits the load capacitance). (Ibias), The positive slew rate, on the other hand, has a rather high rate value. Because the speed of a large-signal is limited by the minimal value of positive, symmetrical slew rate is usually necessary. Slew rates are both positive and negative. Both the negative slew rate and the bandwidth can be increased at the cost of higher latency, Ibias and, consequently, the static power consumption will increased.

2.1.1 HIGH VOLTAGE UNITY GAIN VOLTAGE FOLLOWER:-

This circuit have EN and PD enable signal inputs. The EN and PD signals must be set to the correct value in order to power off the buffer. However, the When EN is used, high-impedance functionality is enabled. only a signal Changes in control application methods are possible. In this circuit customised control logic is used. In this instance, the logic circuitry I buffered and considered as an external circuitry Consequently, not included.

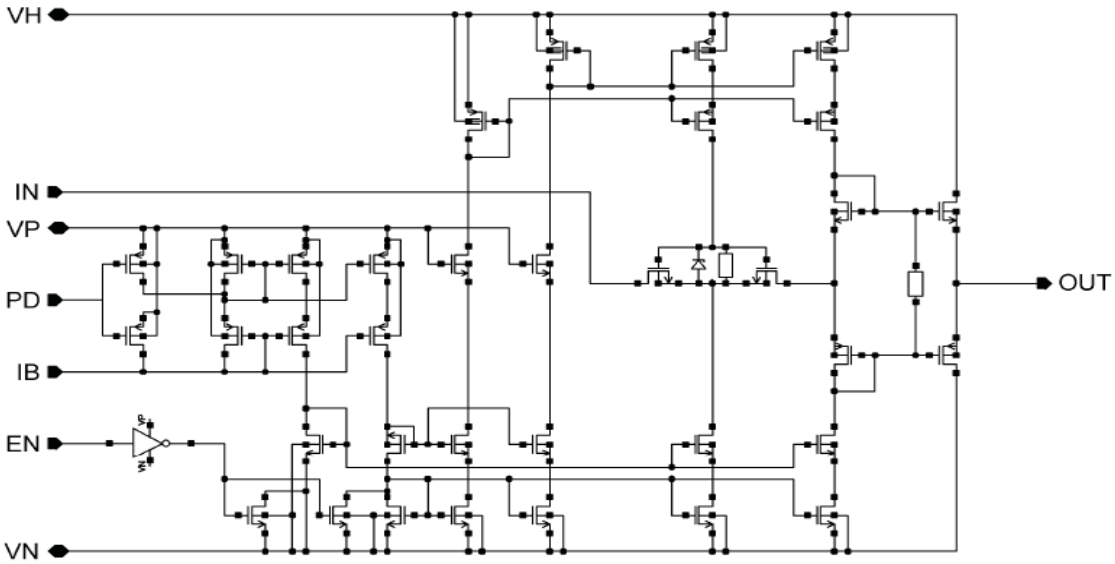

Figure 2.2: Circuit diagram of high voltage unity gain voltage follower [1]

The EN/PD signal-induced power in down mode disables complete circuit functions by cutting off all bias currents. The EN signal in Fig.2.2 is employed to drive numerous aspects of high-Z functioning, both at input and output and nodes for output. The bias current mirrors feed when the EN signal is high with the externally defined HV current-controlled switches. There are numerous current constructions, controlled switching devices [1].

These switches are each powered by two high-voltage currents. sources. This solution, in combination with a resistor-driven switch, The use of transistors ensures a smooth transition towards the cut-off situation. Both are transistor switches.

2.1.2 FULLY DIFFERENTIAL LOW VOLTAGE WIDE SWING VOLTAGE FOLLOWER:-

The voltage follower is based on the FD DA [2], which posses of a bulk-driven input stage which drives a gate-driven class-A output stage. A PMOS Since there are n differential pairings, implementation is chosen. Technology is taken into account. There are four input terminals required. in order to produce a noninverting FD unity Configuration of gain feedback The FD DA was indeed linked. As a result of the feedback system presented in Fig. 2.3, a voltage buffer with FD. Bulk-driven MOS transistors are used in The FDDA input stage enables a large input voltage range. The mid supply voltage area is included in this range. The The two-stage scheme's frequency response is corrected by A Miller network with a zero-nulling resistor is used. The The input capacitively loads the FD amplifier outputs. The CM detector's bulk-driven MOS transistors. However this capacitance is connected in parallel with the, *C*L, and it has a minor effect in most cases. The response of the FD voltage buffer's DM loop is determined by the signal path of the FD-DA in Fig. 2.3. As previously stated, this path contains of consisting of a gate-driven output stage and a bulk-driven input stage It's worth noting that the input-related

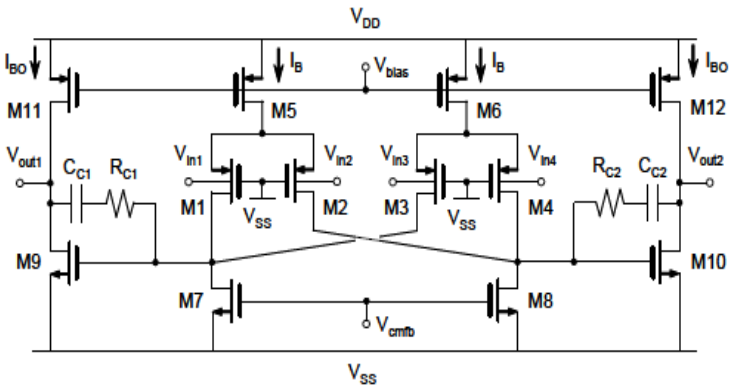

Figure 2.3: Circuit diagram of FDDA based voltage buffer [2]

noise contribution is significant. Because of the existence of the, the FDDA in Fig. 2.3 is increased. MOS transistors in the input stage that are bulk-driven In fact, the An MOS transistor generates the same intrinsic noise. Regardless of their link, there is a distinction when the The device's input terminal is chosen.

2.1.3 CLASS AB FLIPPED TYPE VOLTAGE FOLLOWER :-

The suggested class-AB FVF cell, based on bulk-driven and quasi-floating gate approaches, is shown in Figure 2.4. M6-type PMOS transistors to clone the current state, create a current mirror. Ib (= Ibias), and an NMOS transistor with a diode M5 7 gives the necessary voltage Vb. The capacitor is a device that stores electricity. Cbat between nodes "Y" and "X," as well as a high-valued resistance Rlarge is linked between NMOS transistor gate terminals M2 and M5. The opposition Rlarge PMOS transistor has been implemented. Transistor M4 operating in the cutoff zone. There is no voltage decrease in this area. Rlarge As a result, it creates well-defined quiescent voltage Vb at the transistor's gate M2 that keeps the bias current flowing through the transistor M2. As a result, the gate of

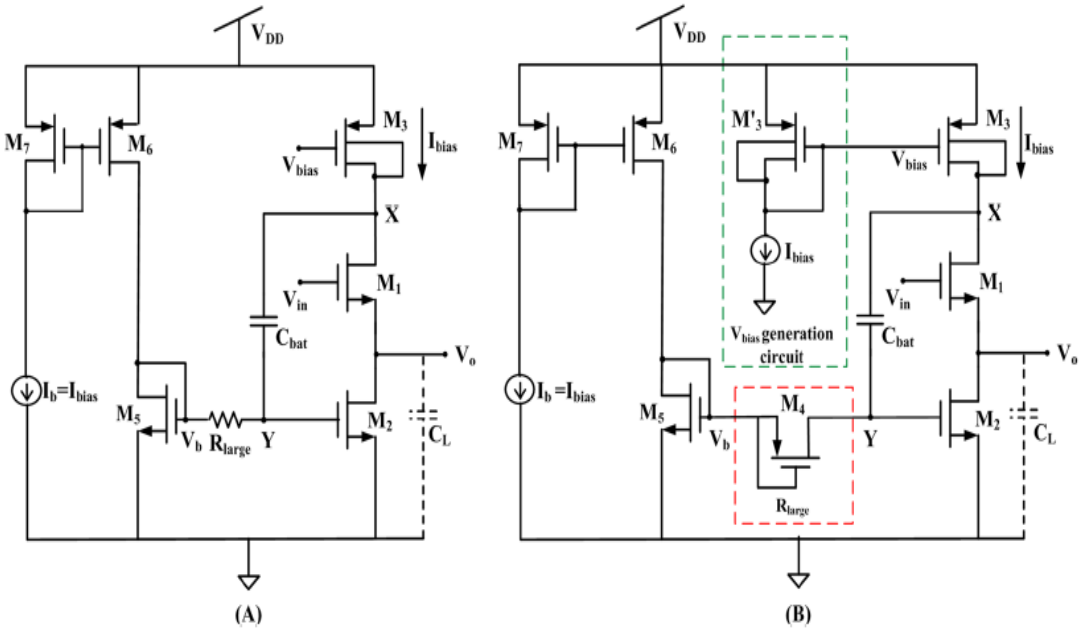

Figure 2.4: Circuit diagram of class AB type flipped voltage follower circuit a). without biasing b). with biasing [3]

Under dynamic situations, transistor M2 acts as a quasi-floating gate. The voltages are higher in DC operation. VY and VX "Y" and "X" are independent of each other at nodes "Y" and "X," however they are coupled under dynamic conditions. “ The capacitor is a device that stores electricity. Cbat and opposition Rlarge operate as a cutoff frequency HPF fo(1/ 2pRlargeCbat) for passing signals ing between nodes "X" and "Y." “A bulk-driven PMOS transistor replaces the standard FVF cell's biassing current source (Ibias). M3. In bulk 1, 2 A fixed DC voltage source is applied to the gate ends of a driven transistor, and input is applied to the bulk ends. As a result, the suggested class-AB FVF cell uses a constant DC voltage (Vbias) voltage is applied to the gate ends VX, which The bulk terminal of the transistor is used as an input. M3. To provide a constant DC voltage (Vbias), the gate station M'3 (clone of transistor) is a diode-connected transistor. M3) is used. Transistor M'3's bulk and drain connections are 3 '3 also interconnected, as well as a sinking current source Ibias where the drain terminal is linked as demonstrated in The gate voltage (Figure 1B). Vbias fixes the transistor's gate-source voltage M3 As a result, the current bias in the branch M3 to M1. The transistor is a small electronic device. M3 works as a flexible current source and improves current sourcing capability suggested FVF cell of class AB The positive output current becomes larger than the bias current as a result of this. (Ibias). The

current at Transistors are controlled by node "X." M2 and M3 to maintain the branch's bias current M1 to M3. The current VX at node Transient fluctuations in input voltage produce "X." Vin.

2.1.4 HIGH INPUT IMPEDANCE HIGH VOLTAGE UNITY GAIN VOLTAGE FOLLOWER:-

There have been attempts to develop voltage buffers that use gate as input architectures, however they lack control over gain and DC voltage offset [10] For precision, some techniques employ complicated adaptive biassing structures. suggested buffer structures are under control [11]. Unfortunately, the majority of The structures are made for low-voltage applications. The structure is intricate in order to maintain excellent quality. This is similar to a source-input voltage buffer. This is accomplished by modifying the gate-source voltage drops of the input stage transistor, which may be near to the gate-source voltage drops of the output stage transistor. The voltage falls. Alternatively, to make the input stage GS voltages are provided by transistors in the gate-input buffer. similar to gate-source voltages in the input stage of the transistor voltage source-input buffer To obtain the desired voltage drop on the It is necessary to obtain transistors for the input stage. polarised properly This is accomplished by altering the input. current sources stage bias gate input impedance voltage buffer and gain value

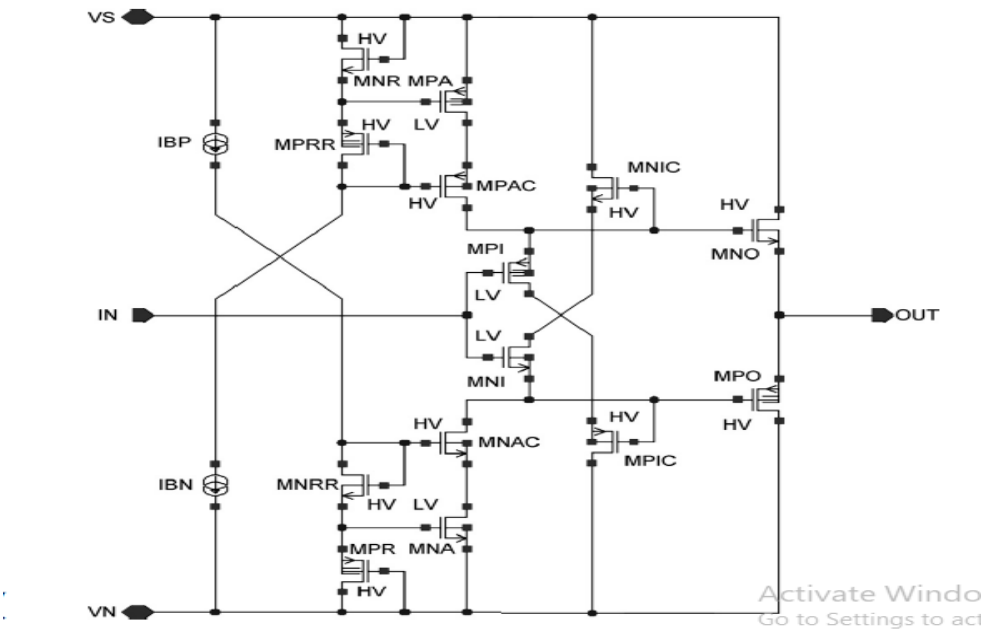

Figure 2.5: Circuit diagram of high input impedance and high voltage unity gain voltage follower circuit [4]

The idea is to create enough current to make the voltage drop at the input transistor gate-source equal to the voltage drop at the source-input voltage buffer's input-stage transistors. The principle of Fig. 2.5 is illustrated with a simple picture. The transistors' names. In the introductory form of the proposed solutions, a complimentary version of the buffers demonstrates how those employed in gate-and-source-follower are used. Figure 2.5 shows The introduction buffer structure has been supplemented. There are two current sources, and their currents are equivalent to the source-input voltage buffer's input bias current. Each securrent biassed one of the reference transistors (MPR, MNR), which is identical to one of the source-input buffer's input-stage transistors..

2.1.5 VOLTAGE BUFFER STAGE, USED IN PROPOSED VCII SIMULATED CIRCUIT:-

A source follower with pseudo functionality has a low output impedance and, is fast. Same time, can cope with When compared to a simple CD type, there is a substantial output swing. source observer. However, this strategy has a flaw. Controlling the quiescent is challenging. as a consequence of a random high transconductance and threshold voltage Parts that pull up and

down. Consequently, any a working circuit Taking this strategy necessitates incorporate additionally mechanism to govern the dormant current. Also, capacitors for compensation are required to enhance the transient responsiveness and stability leading in a substantial chip area.

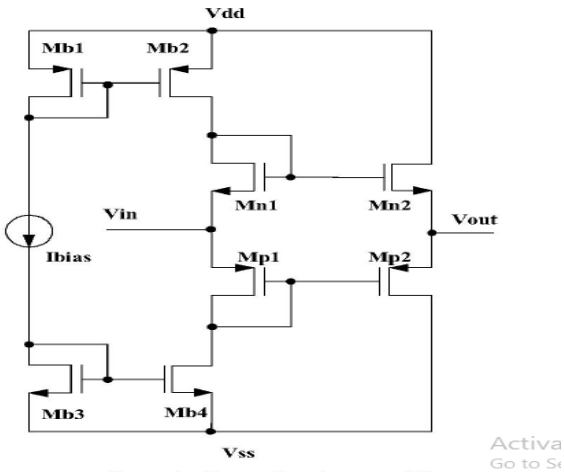

Figure 2.6: Circuit diagram of conventional voltage follower [5]

Figure 2.6 depicts a standard voltage follower. Four transistors make up the circuit. (M,11, MP1, MK2 and Mp2) which are connecting in a straightforward complimentary manner This circuit provides excellent control and efficiency in the workplace application of the quiescent current because of its simplicity, the The characteristic of frequency is excellent and is determined by The input and output nodes have a time constant linked with them. In Furthermore, the follower has a low voltage offset, which is primarily decided by transistor mismatch. There are three major disadvantages to becoming a follower: 1) The linearity is low and highly reliant on the data. 2) a high ratio between biassing and output current output impedance as a result of lower transconductance 3) a restriction of the MOS transistor

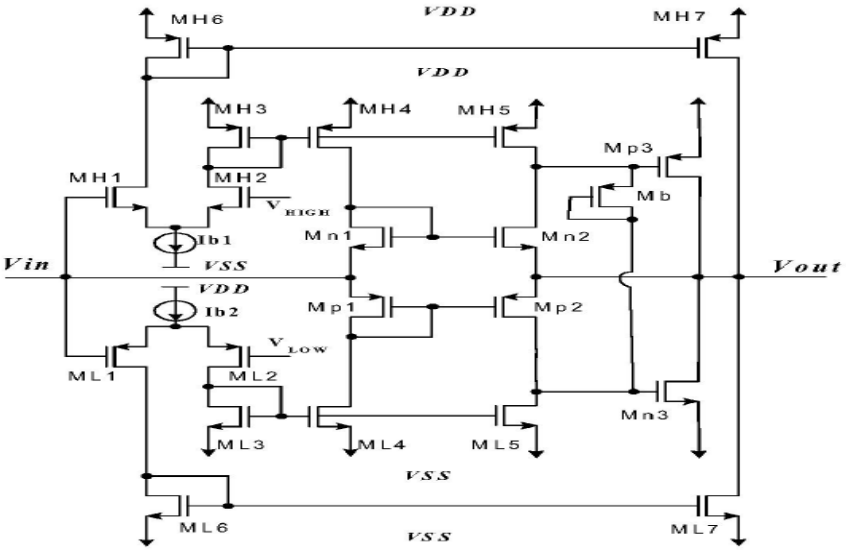

Figure 2.7: Circuit diagram of Voltage follower with rai to rail capability [5]

The symmetrical voltage buffer described in Fig. 2.6 is the basis for the proposed circuit in Fig. 2.7 Four (M,11, Mn2, Mp1, Mp2)transistor work as a traditional follower of voltage MH1, Mp2 and MH2 x are intertwined in the differential amplifier arrangement, which is in charge of sensing the amplitude of the input Mp3 and Mn3 consisting of be a second cs output stage running parallel with the traditional follower linked to negative feedback the output impedance should be reduced. The process of following diagram depicts the circuit. The circuit behaves like a traditional voltage follower when the input voltage is between VHIGH and VLOW. The input signal is amplified with the help of Mp2 and Mn2 after which it was passed to gates of Mp3 And Mn3 Respectively.Mp3 And Mn3, that are suit the purpose when coupled in a cs configuration depending on the load, to sink to source and current an incoming input signal's polarity.

2.1.6 FLIPED VOLTAGE FOLLOWER:-

Property of voltage buffer circuit is that it has high ideally infinite impedance at the input and a low ideally zero output impedance, with ideal values of infinite and zero, but in practice, the output and intput impedances are few hundreds of ohms and a several hundreds of ohms, respectively. It has unity gain, which means that the output voltage is proportional to the input voltage. The common drain amplifier is the most widely used voltage buffer circuit. Let's take a

look at the typical drain amplifier, which is frequently employed as a voltage buffer. The Circuit follows the input voltage with a dc level shift, if the body effect is ignored, as Vo = VSGM1+ Vi , where VSGM1 is the transistor's source-to-gate voltage.

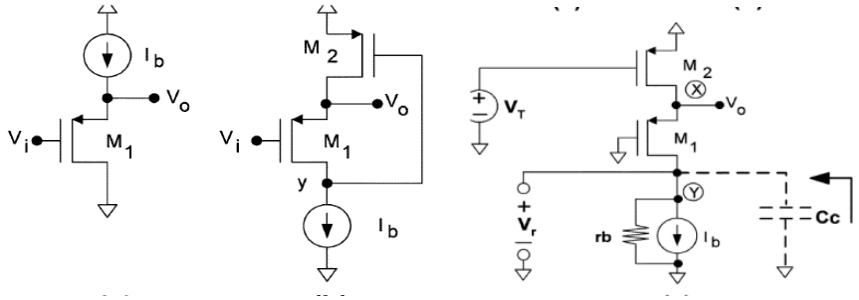

Figure 2.8: Circuit diagram of common drain voltage buffer and flipped voltage buffer [6]

In terms of large-signal behaviour, this circuit can sink a lot of current from the load, but the biassing current source limits its sourcing ability. The current through M1 transistor is dependent on the output current, hence VSGM1 is not constant and, as a result, the voltage gain for resistive loads is less than unity. At high frequencies, capacitive loads have a similar difficulty. The circuit also functions as a source follower, with the current flowing through transistor M1 being constant regardless of the output current. It's a voltage follower with shunt feedback, in a sense. Neglecting the body's effect and the short-term effects Influence of a channel The voltage gain is unity, and VSGM1 is kept constant. The circuit may generate a huge amount of current, unlike a traditional voltage follower, however its sinking capability is limited by the biassing current source Ib. The low impedance at the output node, which is about ro = 1/(gm1gm2ro1), explains the high sourcing capability. gmi and roi are the transconductance and output resistance of transistor Mi, respectively. This number is somewhere between 20 and 100. M2 gives shunt feedback, while M1 and M2 create a negative feedback loop with two poles. The identical circuit as before, but with the feedback loop open at M2's gate and a test voltage source Vt. There is an open-loop gain in this circuit. AOL = Vr / Vt = -gm2 AOL = Vr / Vt = -gm2 Roly (where the open-loop resistance at node Y is given by ROLY rb||gmro1ro2), Wpy= 1/CyROLY, a dominating pole at node Y, WPX= 1/ROLYCx (where the open-loop resistance at node X is given by ROLX((1+rb/ro1)/gm1||ro2), and a high-frequency pole at no The parasitic

capacitances at nodes X and Y are Cx and Cy, respectively (Cx also includes the load capacitor, if any). GB= gm2/Cy [14] gives the gain bandwidth product. At node X, the closed-loop resistance is given by

$$RCLX =(ROLX/(1+|AOL|) \approx 1/gm1\ (1+ rb/ro1)||ro2) / (1/gm2(rb||gm1ro1ro2))$$

RCLX tends to 2/gm1gm2ro1 if the source Ib is a simple current mirror (rb = ro1). RCLX is approximately given by 1/gm1gm2ro1 when Ib is a cascode current mirror rb gm1 ro1ro2 or when rb is quite huge. RCLX is, in any event, an extremely low resistance.

2.1.7 DIFFERENTIAL VOLTAGE BUFFER STAGE:-

The first differential structure based on the FVF cell can be built by connecting node X to an extra transistor M3. It will be known as the FVF differential structure (DFVF). The impedance at node X is relatively low for large currents through transistor M3, and its voltage remains almost constant. The condition IDM1=IDM3=Ib is satisfied if we analyse quiescent situations with V1=V3 and suppose that M1 and M3 have the same transistor sizes. When a differential voltage V1 – V3 is applied, current variations in M3 follow the MOS square law. The maximum output current Ib can be much larger than the quiescent current Ib, which is a fascinating feature of the DFVF. In comparison to V1-V3, IDM3 has a better dc transmission characteristic. It is possible to observe this.the typical Class-AB behaviour. [6].

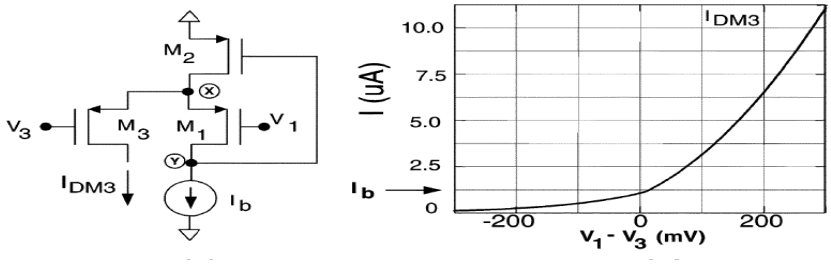

Figure 2.9: Circuit diagram of Differential flipped voltage buffer and corresponding output current plot[6]

Another feature of the DFVF is that the output can be obtained as a current (IDM3, or the current via transistor M2 reproduced by a current mirror) or a voltage (node Y). This feature can be used to simplify circuit implementations by lowering noise as well as the amount of poles and

zeros. Finally, the DFVF may work with a very low supply voltage. As with the FVFCS, the minimum supply voltage is VDD MIN = |VTP|+2VDsat. There would be no room for variance of the 25 input signals V1 and V3 with a supply of VDD MIN. It is simple to derive a formula for the expected fluctuation of V1 and V3 in relation to the minimal supply voltage. Which maintains the DFVF cell properly biased.

2.1.8 SIMULATION OF USED VOLTAGE BUFFER STAGE:-

Table 2.1: Aspect ratio used in simulation of buffer stage

Transistor name	Width (um)	Length (um)
M1,2,3,6,9	6.3	1
M4	320	1
M5	429	1
M7	0.5	1
M8	1230	0.5
M10	627	1
M11	12.5	1
M12,13,18,20,21	1.6	1
M14	3.2	1
M15	157	1
M16	108	1
M17	350	0.5
M19	82	1

We have used following biasing voltage and current parameter in our simulation:

Vhigh = 0.7 Volt, Vlow= -0.6 Volt, I_H = 1u Amp, I_L= 1u Amp, Vdd= 1.8 Volt

Tool used for simulation is LTspice.

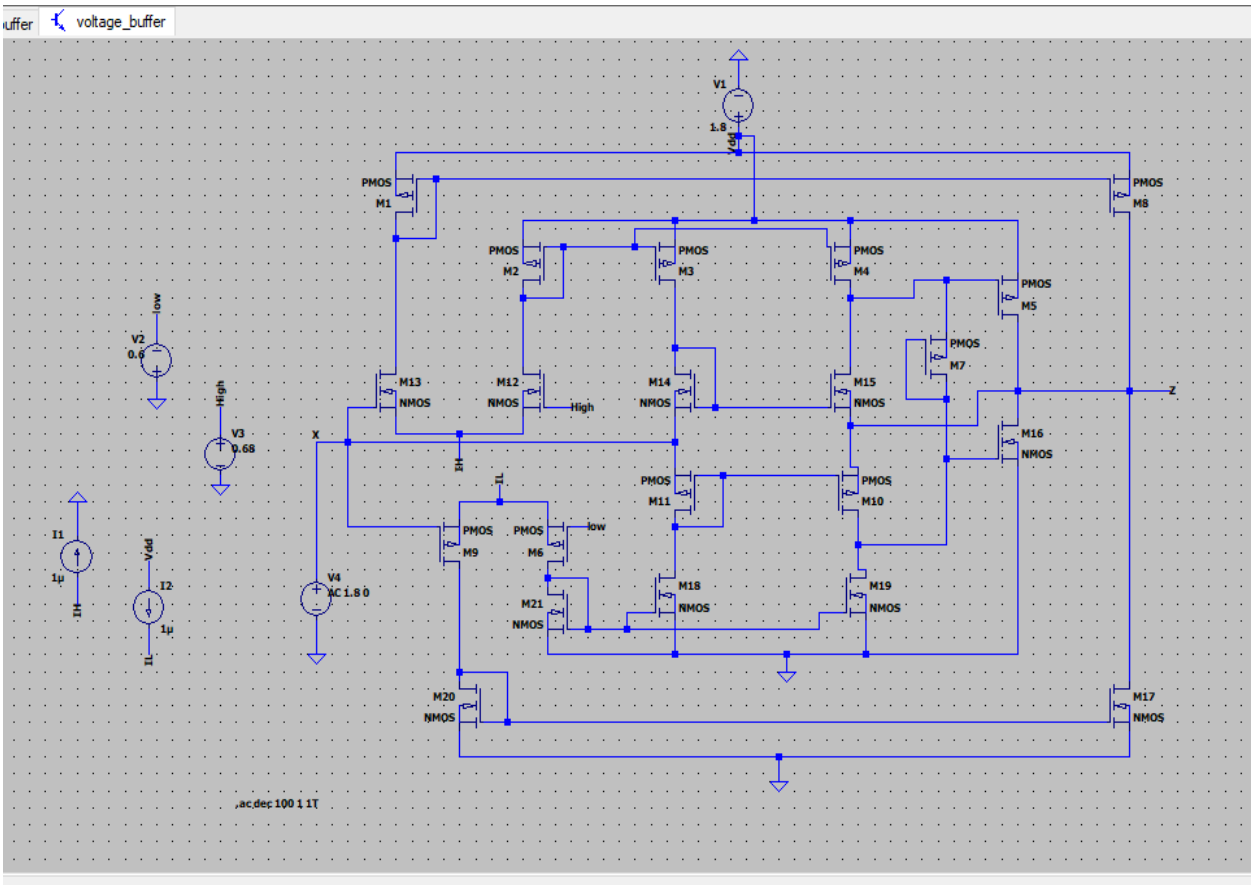

Figure 2.10: Circuit diagram of voltage follower circuit used in proposed VCII block

Node X act as a input node here and node Z work as output node. For AC analysis we use the AC voltage of magnitude 1.8 Volt and 0 degree phase. In AC analysis we have plotted Phase and magnitude plot. We achieved 10.10 MHz 3 dB frequency and the output curve of voltage buffer circuit is like a low pass filter.

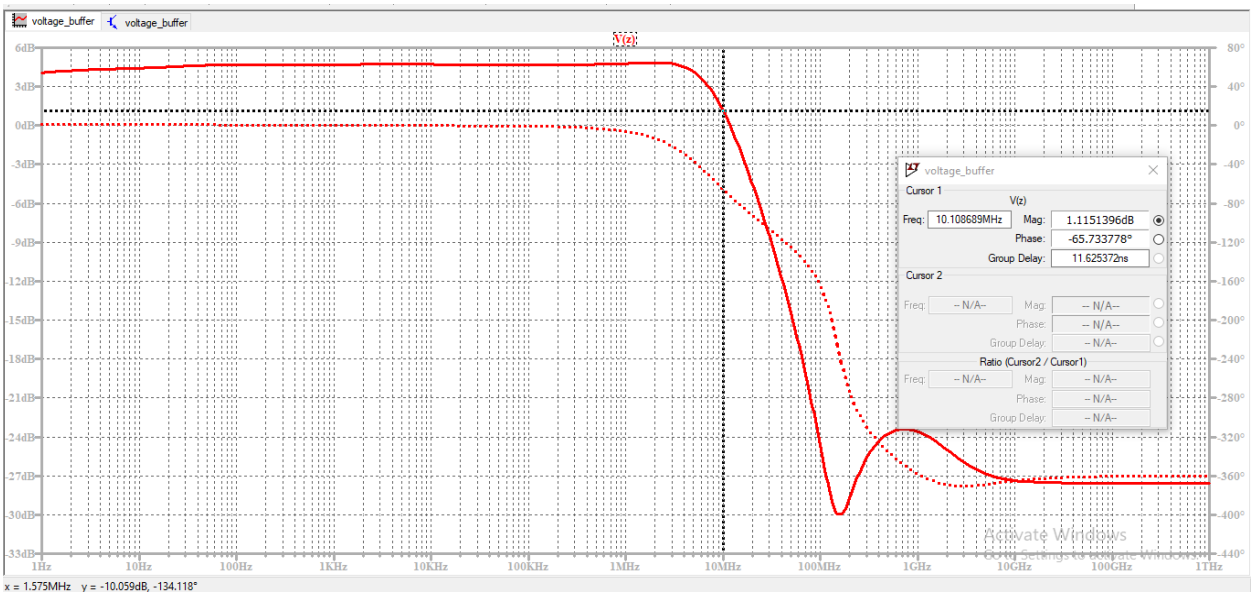

Figure 2.11: Plot of AC analysis of voltage follower circuit used in proposed VCII block

For DC analysis we sweep the input voltage from 0 to 1.8 Volt with a increment of 0.01. From the plotted result we can conclude that output voltage is following the input voltage very well, which implies the α and β value for the voltage buffer circuit is approximately 1 and its gain is also 1. In the plot V(z) is output and V(x) is input. We are getting little bit glitch at low input voltage which can be improved after biasing this circuit with appropriate resistors.

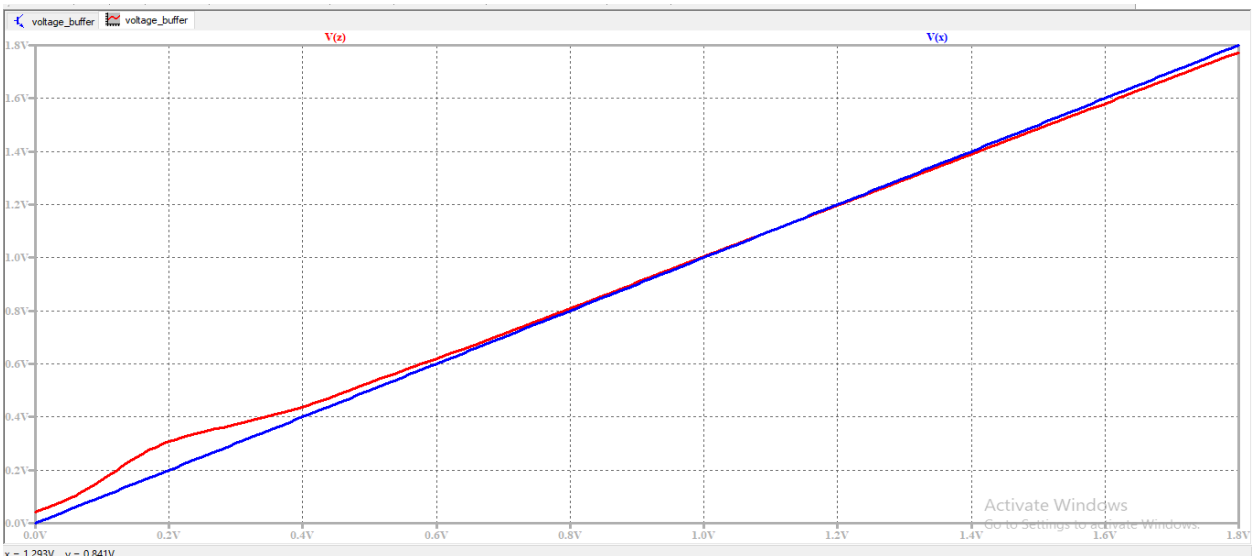

Figure 2.12: Plot of DC analysis of voltage follower circuit used in proposed VCII block

For transient analysis we provide sine wave at the input node X, with amplitude of 20mV and frequency of 10KHz. At the output side we get sinusoidal waveform with same phase, frequency and same peak to peak voltage (40mV). i.e output is following input properly. In step response plot we use step voltage at input side with amplitude of 1.8 volt, period of 10ms with 50% duty cycle.

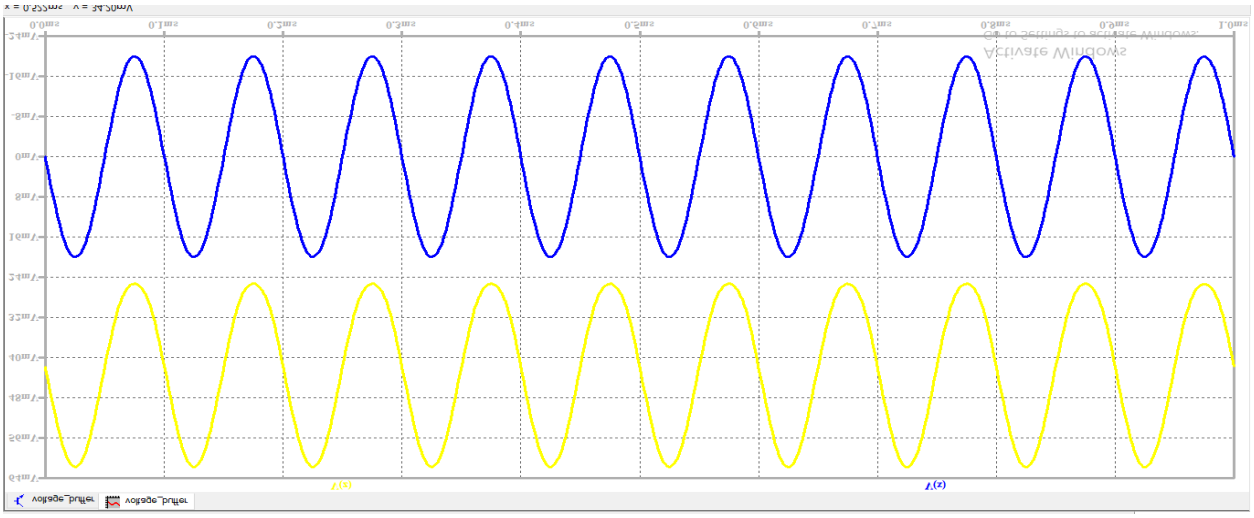

Figure 2.13: Plot of transient analysis of voltage follower circuit used in proposed VCII block

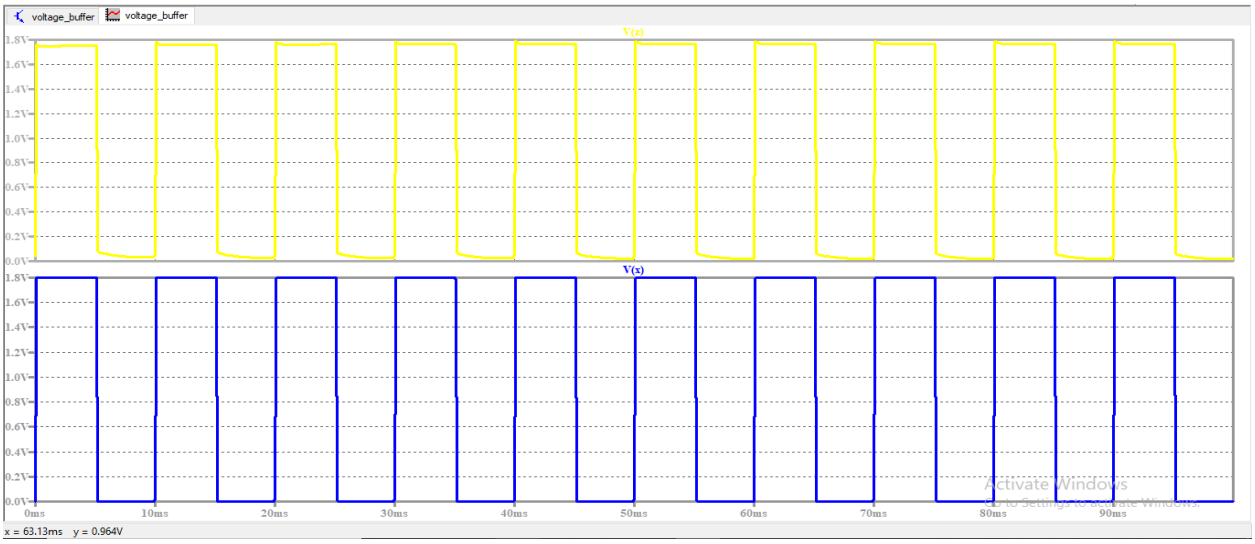

Figure 2.14: Plot of transient analysis using step response of voltage follower circuit used in proposed VCII block

For power analysis we use a load capacitor of value 1 pF at the output side and plot the power graph. From the graph we can see that the maximum power consumption is about 42 nW which is much smaller in comparision to the op-Amp circuit.

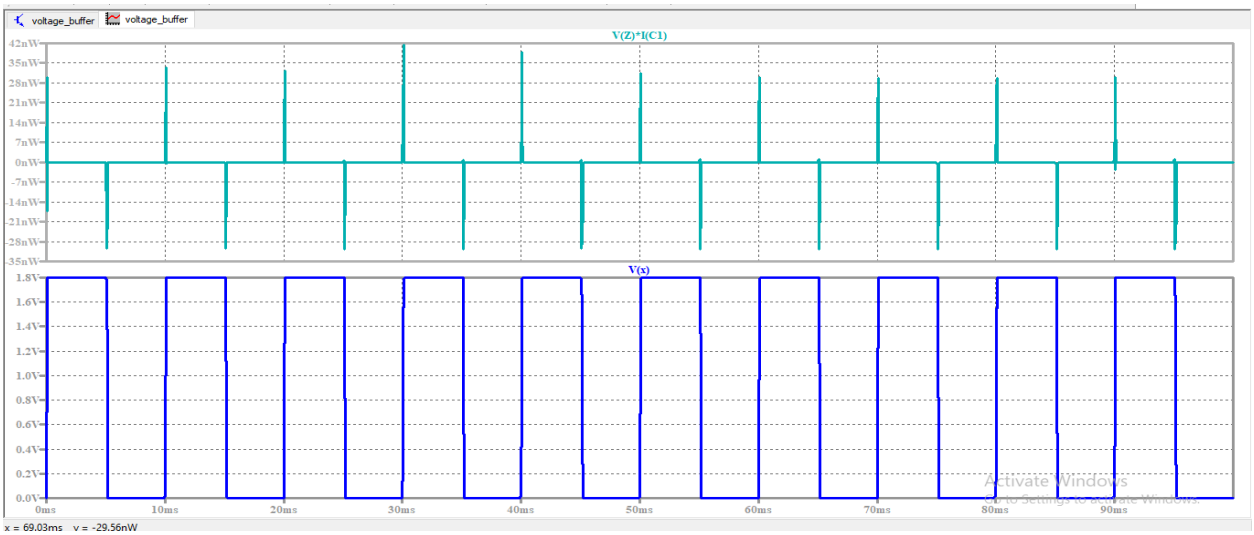

Figure 2.15: Plot of power consumption of voltage follower circuit used in proposed VCII block

2.2 CURRENT BUFFER:-

The primary building elements of signal processing in current mode, circuits are current buffers. Unity current, gain low input impedance, and high output impedance, are their major characteristics. A current follower is a circuit that transfers current from a circuit with low value input impedance to one with high value input impedance. The current follower circuit is connected in between the two circuits, to minimize loading effect using impedance matching technique the second circuit cannot load the 1st circuit. Ideally Infinite impedance at input node, zero impedance at output node, great

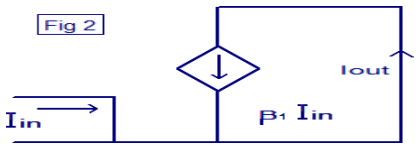

Figure 2.16: Small signal model of ideal current buffer circuit

linearity, and fast response are all characteristics of an ideal current buffer. A current buffer with unity gain or current follower is a current buffer with unity gain. The current at output simply tracks or follows the current at input node in this case. Transistors can be used to create a current buffer. Some properties and application of current follower circuits are as follows:

i). It is used to protect on-chip circuit from excessive parasitic capacitances at the chip input pads, allowing current-mode circuits to operate at their maximum speed.

ii).The adjoint network theorem based on current buffers can be used to transform voltage mode type circuits to current mode type circuits [6-7].

iii).Wide band data communication can benefit from current buffers [8-9].

iv). Current buffers can be used to create many sorts of filters and oscillators [10-11].

v). In most current mode circuits, current buffers are utilised at the input stage.

Current buffers are a fundamental component of current mode signal processing. They finding widespread use in the contemporary design applications, mode filters, and oscillators involving amazing present output sensors under dures sensors, magnetic sensors, light sensors, etc. They are also utilised in practically every present mode building design current mode amplifiers, current mode amplifiers differencing transconductance amplifiers (CDTA), CDBAs (current difference buffered amplifiers) present inverter/follower buffered transconductance amplifier (CITBA) and OFC stands for operating floating current conveyors.

2.2.1 DIFFERENTIAL CURRENT FOLLOWER:-

A current follower/amplifier is a 2-terminal device that transmits an input signal in current mode from a low impedance (preferably virtual ground) terminal (X) to a node with high impedance (ideally virtual ground) terminal (Y) (ideally infinity) terminal for output (Z). current Follower/Current Amplifiers are divided into two categories. positive (a non-inverting), with output and input currents that are equal in the same direction, and the negative currents are in opposing directions (a inverting) type.

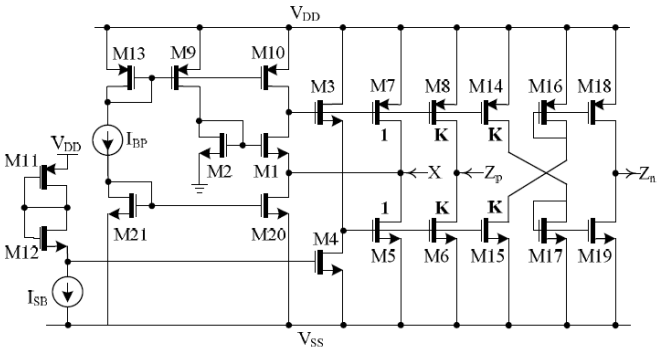

Figure 2.17: Circuit diagram of differential current follower [22]

The virtual ground required at input node X is provided by transistors M1 and M2. Equal currents are forced through both transistors to achieve this. As a result, source potentials will be equivalent because it share the same gate if it is operated in the saturation region.As we know the transconductance of a Bi-Polar transistor is high as compared to the MOS transistor's transconductance, that's why negative feedback is required when compared to a bipolar transistor. to get low input impedance at the X terminal. The activity of provides the X terminal current. transistors generate a class AB negative feedback loop M3, M4, M5 and M7. The input is reduced by the feedback. multiplied by the amount of feedback.

2.2.2 DIFFERENTAIL CURRENT BUFFER USING C OMMON FEED FORWARD TECHNIQUE:-

A circuitstructure is employed to transfer the common mode and differential currents travelling through M2-M1 to the output terminals having gains of one and zero, respectively. The structure is based on the CMFF(Common Mode Feed Forward) approach, which is implemented by the two existing mirror groups, The first category includes the two halves of the circuit have current mirrors (M3, M1, M5) and (M4, M6, M2). The second group is comprised of (M13-M11). The input current Iina (Iinb) that passes through M2 (M1) is mirrored into the output current. By the operation of the first, transistors M5 and M3 (M6 and M4) with gains of A/2 and A are created. current mirror group Connecting the transistor M5-M6's drains, current equal to –A The input is multiplied by (Iina+Iinb)/2.

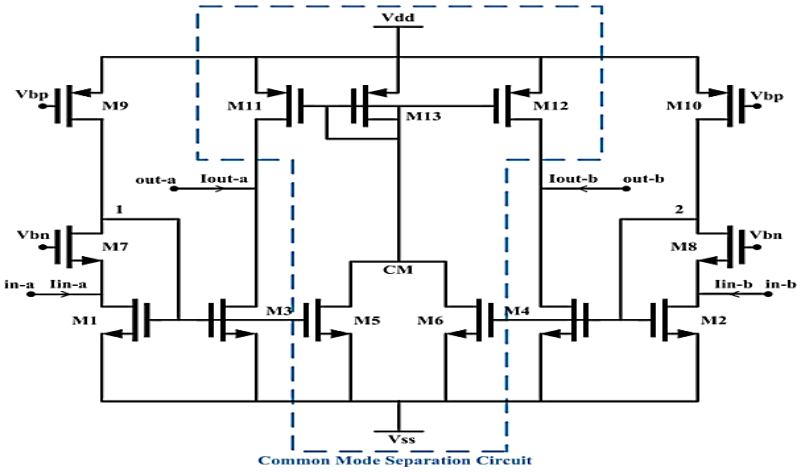

Figure 2.18: Circuit diagram of current buffer using common feed forward technique [7]

2.2.3 FULLY DIFFERENTIAL CURRENT FOLLOWER HAVING LOW INPUT IMPEDANCE AND LOW POWER CAPABILITY:-

The suggested current buffer has a low input node impedance, simple structure, good operational frequency, and high efficiency CMRR and PSRR. Other merit of the proposed present buffer is its very robust performance which has been achieved by to avoid a possible problem associated with positive feedback like negative input impedance and the closed loop stability problem of negative feedback approaches. Favorably because of its simplicity It features a very low consumption of power, construction, and high frequency operation. The input node voltage is reduced by the auxiliary amplifier by a factor of A (voltage gain), yielding a a reduction in input impedance of the same magnitude.

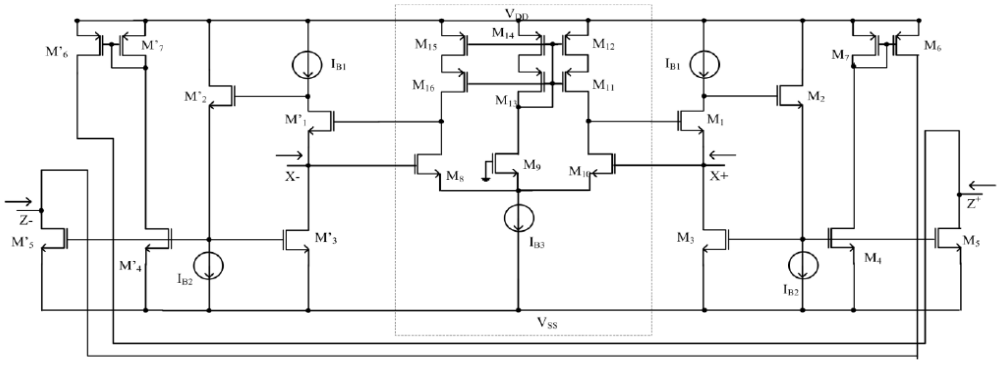

Figure 2.19: Circuit diagram of fully differential current follower having low input impedance capability [26]

The input impedance is further reduced in the suggested current buffer by using other negative value resistor. The input node voltage is further reduced by transistors by lowering M1's gate-source voltage It is a The shunt-shunt feedback system works in such a manner that any M3 drains any change in the input current instead of M1, resulting in a smaller gate-source lowered input node due to lower voltage for M1 voltage. Its operation can be summarised as follows: Due to M1's low input node impedance , ()1/A.gm) vs the output node impedance of M3, the input current enters M1 first and then M2. at the gate, transformed to voltage.

If input voltage exceeds VHIGH, (VHIGH <VIN), M,11, Mp3 And M are pushed into the cutoff area. The present mirror (MH6) is reflected. MH7, which - has N number times the breadth of MH6, now operates as a current bias (Mp1, M113). for the follower with a lower voltage Mp2 And The capable output signal to within swing one overdrive of the positive supply. The Impedance output in this situation is provided by

2.2.4 HIGH CMRR AND LOW POWER FULLY DIFFERENTIAL CURRENT FOLLOWER:-

Figure 2.20 depicts the proposed current buffer (CB) circuit (1). The source grounded transistors M2 and M6 are connected to the CB's input transistors M1 and M5. Thus The planned CB's inputs become virtually grounded, and While the input current is changing, their voltages remain constant. varying, which ideally means zero input impedance Because of the wonderful concept of virtual ground (1) The mutual transconductances value of related transistors, gm1,5 and gm2,6, can be determined by bias and voltage. The lower the input impedance, the better. the CB. However, there is a trade-off between the worth of time and the value of money. Rin, as well as the process's robustness and power consumption the planned CB that has been taken into account in this design a unique current feedback circuit is another powerful concept, created that both keeps the CB's CMRR high and ensures the input impedance is low The routes are set up in such a way that the common mode signal is cancelled at the output while the differential signal is increased (added).

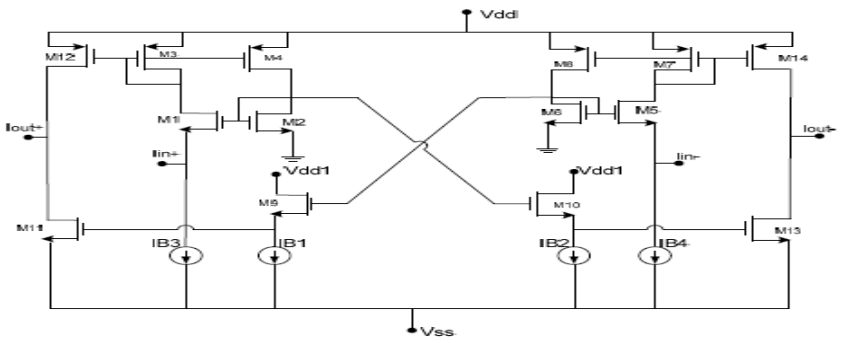

Figure 2.20: Circuit diagram of high CMRR and Low power current follower [9]

2.2.5 COMMON MODE SEPERATION TECHNIQUE BASED CURRENT BUFFER:-

CG stages which were Traditionally, differential signals are processed using this method. In this situation, MN1-MN2 are typical gates transistors with a bias Ibias sources currently available and MB transistor. Currently available mirrors Mm1-Mm2 and M'm2- M'm1 The input signals are sent to the loads. In this method both undesired common mode Currents, both differential and normal , are conveyed resulting in CMRR of 0 dB for the loads. It employs MN1-MN2 CG phases and typical M1-M mode separation circuit implemented M M5 transistors. Favorably M3-M the transistors of M M4

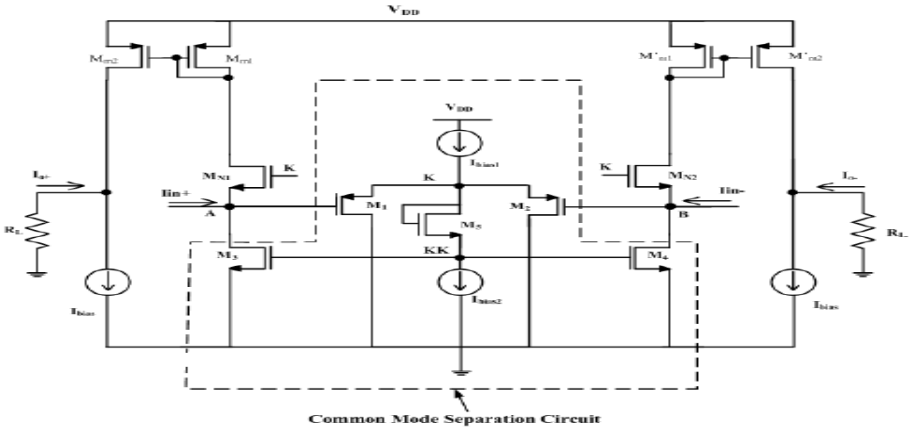

Figure 2.21: Circuit diagram of common mode separation technique based current buffer [10]

Because of M1-M2's voltage monitoring action at node K’s voltage, differential pair will be roughly equivalent to the voltages at the input terminals i.e. VK=VA=VB. This means that the

gate-source is zero. for voltage MN1-MN2 transistors with the same gate stages. As previously stated, in the situation of common input modes, M3-M4 The voltage value between gate-drain are also important. Turning mentioned transistors into diodes equal to 0 ones that are connected and have a low impedance.

As a result, M3-M4 drain current Is is because of common mode input currents are equal to the gate-source voltage is 0 MN1-MN2, their mutual ground the current drain in mode will be nil. However, on the other side, MN2-MN1 in CG stages, transistors have demonstrate high output with 0 gate-source voltage resistance of roN for currents in common mode in which roN is output impedance of MN2-MN1 transistors. Fully differential gain in common mode is available at

2.2.6 CURRENT BUFFER STAGE USED IN PROPOSED VCII SIMULATED CIRCUIT:-

Two CG stages are made up of MN1-MN2 input transistors and the appropriate bias current sources. Bias voltages are provided via the circuit enclosed in the dashed rectangle. MN1 and MN2 gates. 1/gm is the input resistance, where gm is the unit of measurement. is the input transistors' transconductance (MN2-MN1). Unfortunately, most people's input resistance is too high. circuits for current mode processing One common way to Increasing transistor gm by lowering input resistance As a result, electricity usage increases. On the other hand, The CMRR of the hand structure in Fig.2.22 is 0 dB. This is mostly because Since common mode currents are present in this design. With differential mode, transfered to loads since there is no way to cancel out the common mode inputs, the structure of Fig.2.22 can be turned into a completely differential current follower with a high common mode rejection ratio and low differential mode value of input impedance.

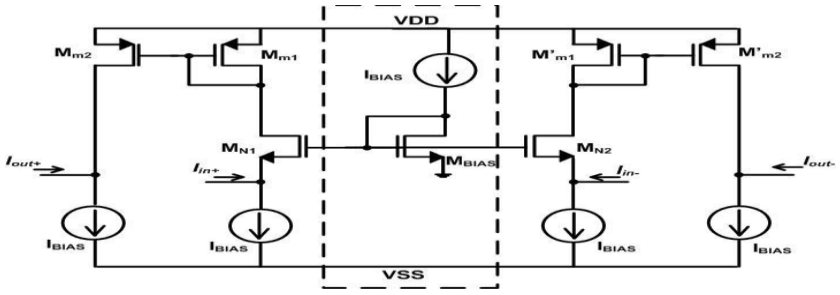

Figure 2.22: Circuit diagram of common gate based current buffer [8]

$$Av = Vo+ / (Vin+ - Vin-) = Vo- / (Vin+ - Vin-)$$

$$= - RF / (R+ Rind) \approx - RF/ R \quad 4.2$$

$$CMRR (dB) = CMRRcb (dB) + 20log10 [(R+Rinc)/ (R+Rind)]$$

It's made up of by adding the source coupled pair to the circuit in Figure 2.23 of MS1-MS2, Mp1-Mp2 PMOS transistors, and current instead of the bias circuit of the MB1-MBR1 and MB2-MBR2 mirrors Figure 2.23 shows Ibais-Mbias. These additional components are depicted in Figure 2.24 (dash rectangle). MB2-MBR2 is currently mirrored along with High CMRR and MS1-MS2 source are provided by MB1-MBR1. MP1-MP2 and the connected pair give a low difference. The suggested current buffer's mode input impedance as it will be discussed later. Opting a low-cost option total bias current for additional circuit in Fig.2.24, dashed line usage of energy The suggested current buffer relies heavily on the source linked pair MS1-MS2. For the differential mode inputs, the MS2-MS1 differential pair's source node. The current is caused by the virtual ground (i.e. C node). As indicated in Figure 2.25, there is a buffer to consider. As may be observed, MN2-MP2 and MN1-MP1 have a positive feedback loop. compels the input nodes (i.e. nodes in2 and in1) to be virtual ground which implies a very low value of differential mode input impedance value for the current follower.

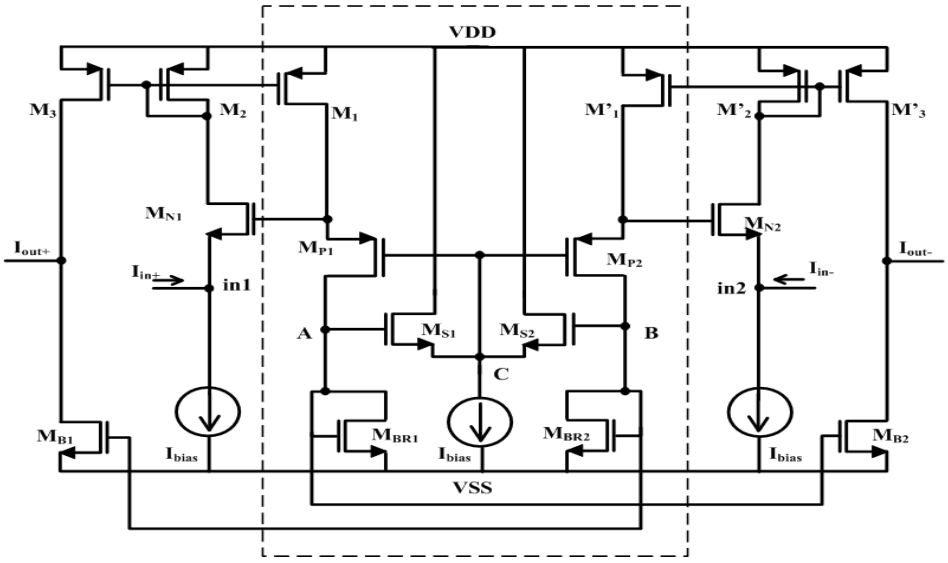

Figure 2.23: Circuit diagram of current buffer stage used in proposed VCII block [8]

Differential mode input impedance of the current follower can be found from:

$$Rind=1/gmn-1/gmp$$

Here gmn is the transconductance of the input transistors (MN2-MN1) and gmp is the tranconductance of MP2-MP1. The existing mirrors MBR1-MB1 and MBR2-MB2 transport the data. Differential mode of currents to the output port's lower branch (as seen in Fig.2.24), where they are combined with the upper M2-M3 and M4 transfer branch currents to the same port current.

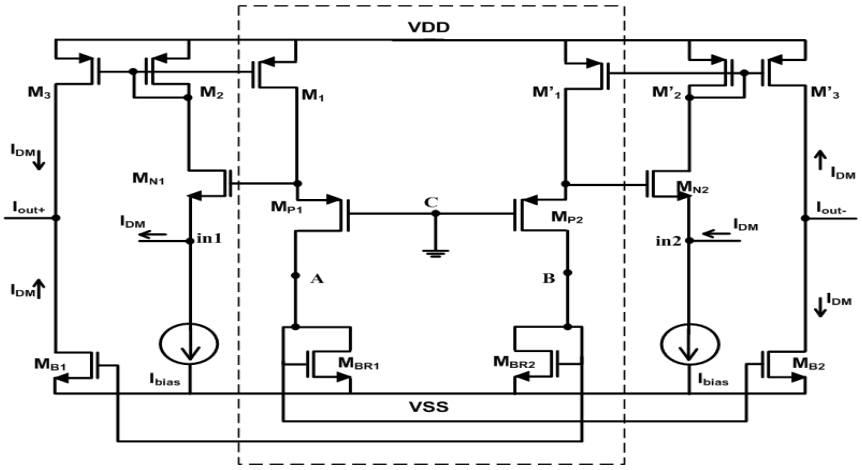

Figure 2.24: Diagram of current buffer circuit in differential mode used in proposed VCII block [8]

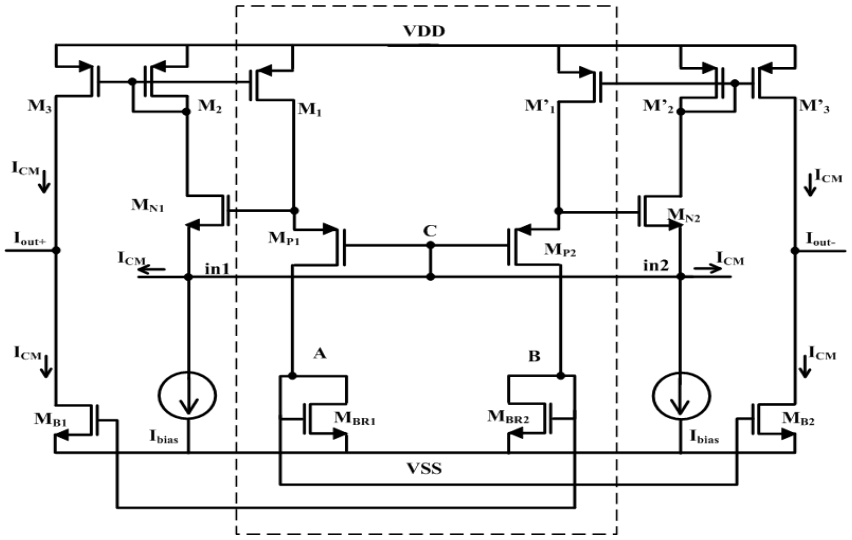

Figure 2.25: Diagram of current buffer circuit in common mode used in proposed VCII block [8]

mirrors M2'-M3' As a result, the current gain is two, which is advantageous for current amplifiers. To ensure that the current buffer differential has a unity value We must set aspect ratios of M3, MB1, and M'3 for mode gain. and MB2 as 1/2 of MBR1, M2, M'2 W/L ratios respectively, MBR1 and MBR2. The voltages produced at input ports are proportional to the voltages produced at A and B nodes in common mode inputs (i.e. in2 and in1). As a result of the voltage tracking effect of the The voltage at the C node can be given as proportional to the voltage at the differential pair. voltages of input nodes As a result, we can suppose a in common simplified circuit for the suggested current buffer Figure 6 shows the mode. There was no favourable feedback in this situation. As a result, the common mode input resistance exists. will not be affected and can be obtained from:

$$Rin_c = 1/gm$$

The input transistors MN1-MN2 have a transconductance of gm. When comparing, it is clear that differential mode value of input impedance can be significantly reduced. one common mode The output upper branches' common mode current is when they're removed from each other, the CMRR is really high.

2.2.7 SIMULATION OF USED CURRENT BUFFER STAGE:-

Table 2.2: Aspect ratio used in simulation of current buffer stage

Transistor name	Width (um)	Length (um)
M1,4	2.5	0.5
M2,3,5,6	5	0.5
M7,15	1.21	0.6
M8,14	10.2	1
M9,11	20	2
M10,16	2	0.5
M17,18	30	0.5

In the simulation of current buffer circuit we used following current and voltage biasing parameter:

I1, I2 =5uA, I5= 1uA, Vdd= 1.8, I3 is input current source.

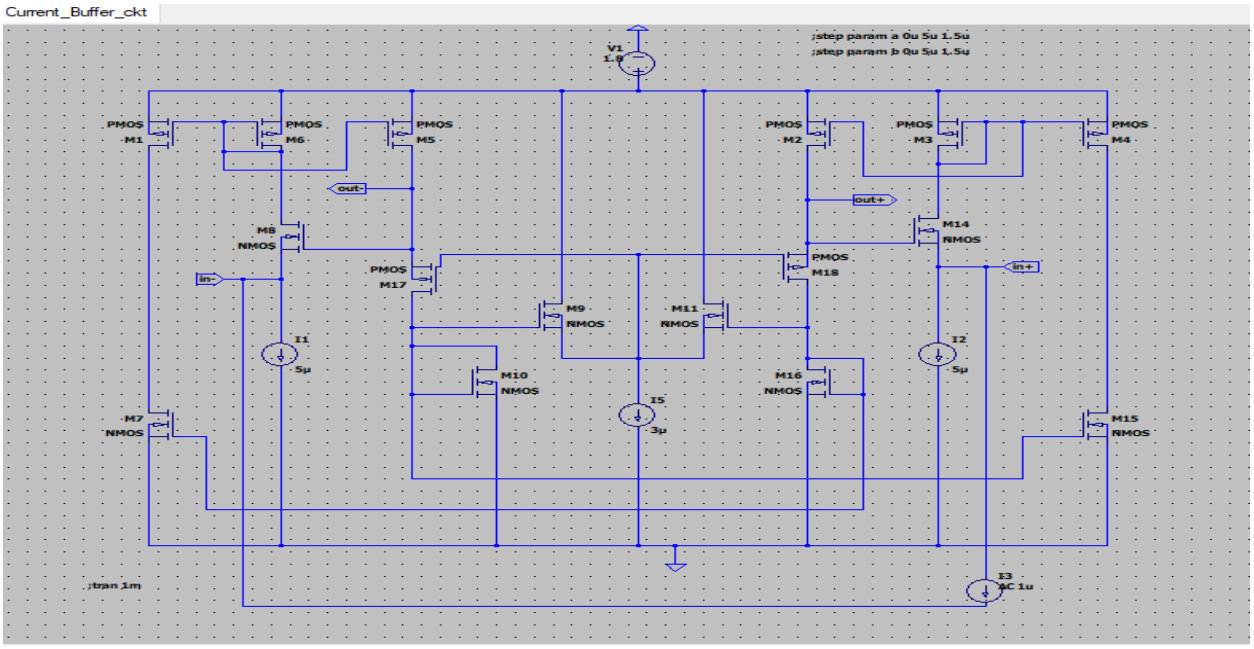

Figure 2.26: Circuit diagram of current buffer stage used in proposed VCII block

For AC analysis we provide AC signal with magnitude of 1uA and 0 degree phase at the input pin. We have measure the phase and gain plot at the output node pin. From the plot we can see that we achieved 783.04 MHz cut-off frequency which is much higher than other available current buffer stage.

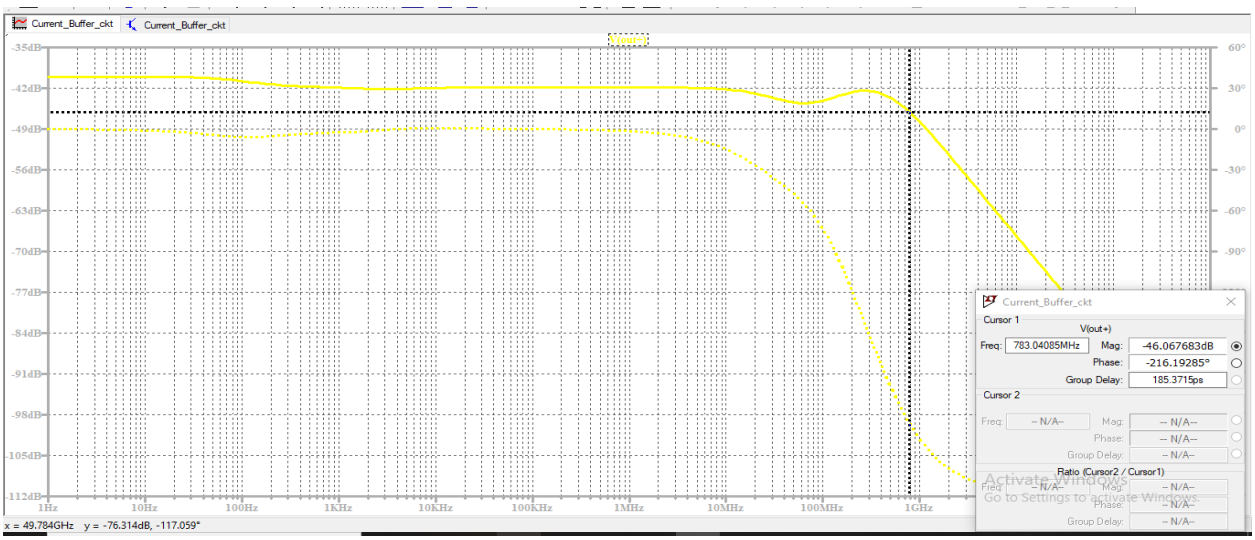

Figure 2.27: Plot of AC analysis of used current buffer stage

For DC analysis we sweep the input current source from o to 5uA with a increment of 0.01. From the waveform plot we can see the slop for the input voltage and output voltage is same. Output has a DC offset which is due to the biasing current source, otherwise output current is following the input current.

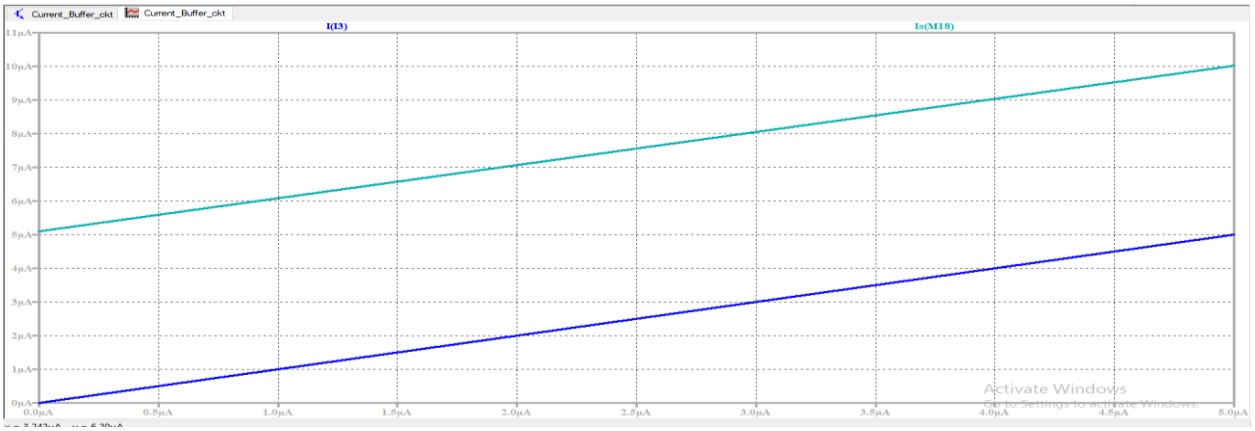

Figure 2.28: Plot of DC analysis of used current buffer stage

For transient analysis we provide a sinusoidal waveform at the input node with magnitude of 1nA and with 10KHz frequency. We are getting same sinusoidal waveform with same phase and frequency and with a DC shift because of biasing current source. For step response we used step voltage source at the input side with 10uA amplitude and 10ms time period with 50% duty cycle.

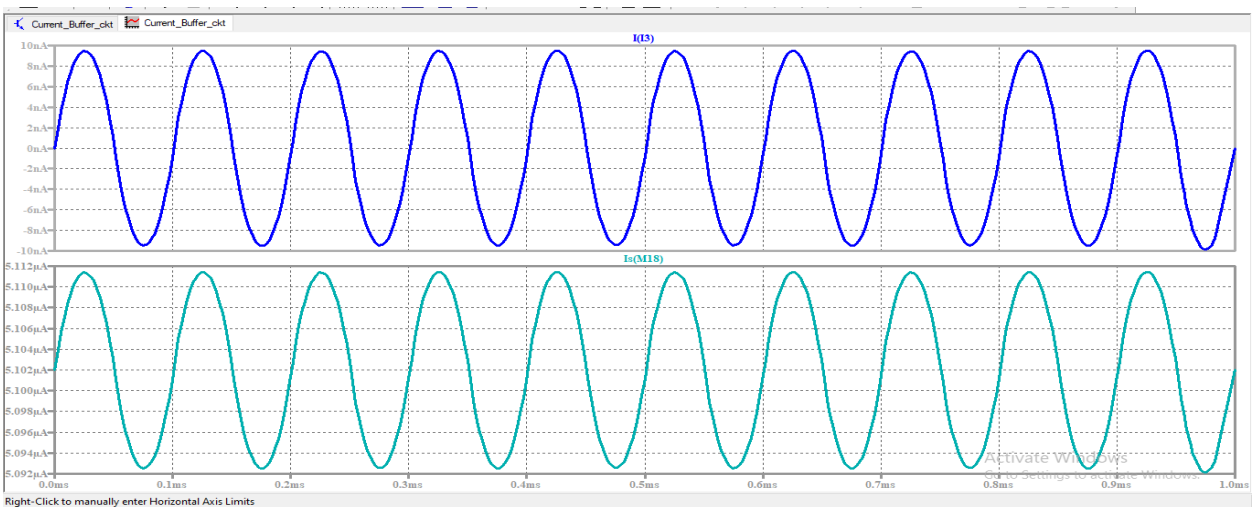

Figure 2.29: Plot of transient analysis of used current buffer stage

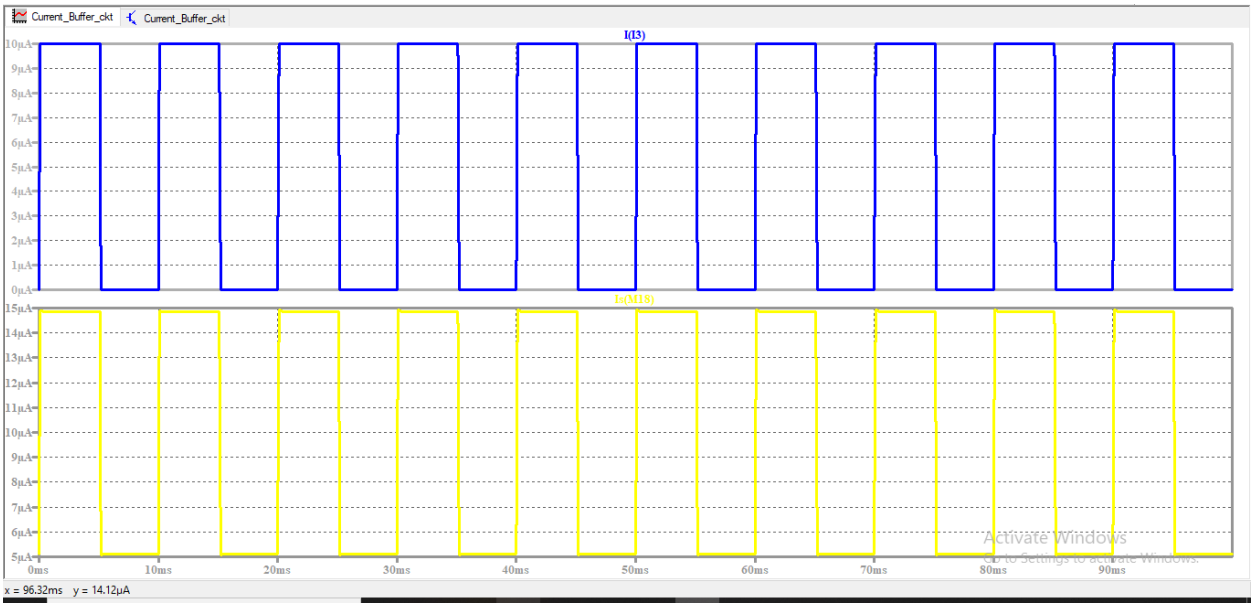

Figure 2.30: Plot of transient analysis using step response of used current buffer stage

For power analysis we provide the square waveform at the input node and plot the output power curve across load capacitor. We add a load capacitor of 1pF. From the graph we can see that maximum power consumtion is in nW, which is much lower than other available current buffer technique.

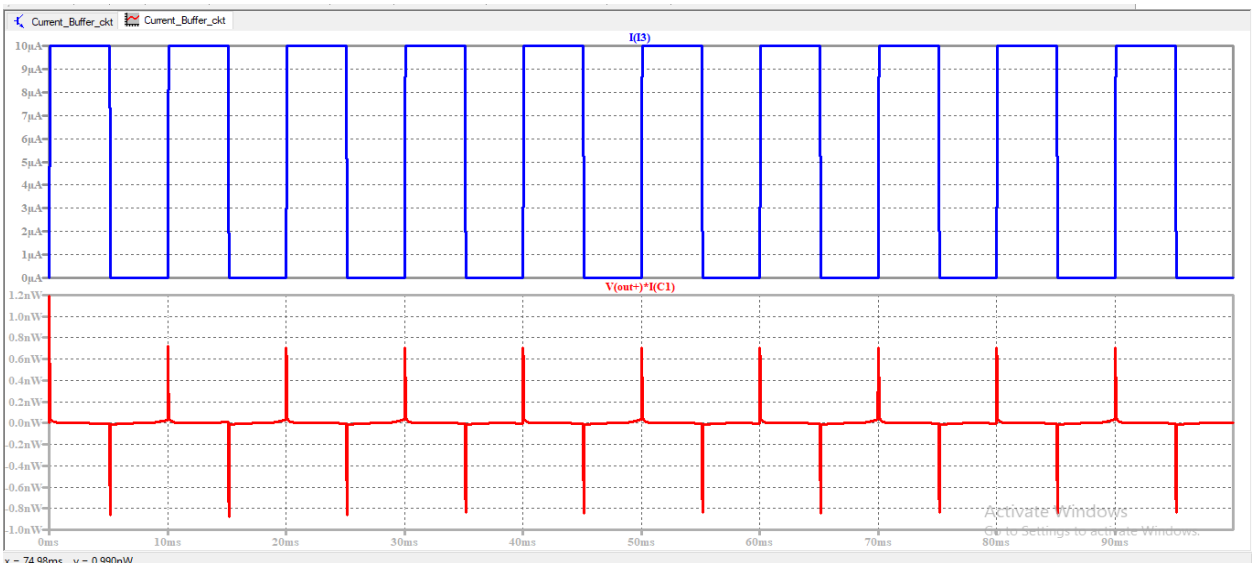

Figure 2.31: Plot of power consumption of current buffer stage

CHAPTER 3

REVIEW OF DIFFERENT TECHNIQUES OF CURRENT AND VOLTAGE CONVEYOR

This chapter presents a basic idea about current mode operation, voltage mode operation, about working of current conveyor, and voltage conveyor. In section 2.1 we discuss about current mode operation and its advantages. In section 2.2 we discuss about current conveyor and its basic functioning, its transistor level implementation. Took a brief idea about the different stages of a current conveyor, discuss its application. In section 2.3 we discuss about voltage mode operation and its merits and demerits. In section 2.4 we discuss about voltage conveyor its functioning, its transistor level implementation, working of different stages of VCII block. In section we will see application of VCII. In section 2.6 we have discussed about advantage of VCII block over CCII and Op-Amp.

3.1 CURRENT MODE OPERATION:-

For most analogue applications, the invention of the operational amplifier places voltage first. Current mode emerged as a result of Sedra and Smith's creation of current conveyor. The response of circuits when operation in current, circuits is determined in the basis of current at various stages of the circuits. Current conveyor can be thought of as a current mode alternative for the op-amp circuit.

Advantage of current mode in comparision to voltage mode are:

1) It have nodes with low value impedance.
2) Adding the current signals is simpler because it only requires only circuit port.
3) The presence of current reflectors makes replication and scaling of current signals easier.
4) Current mode circuits have a lot of bandwidth.
5) The dynamic range is less affected by supply voltage.

Currentmode circuits can be little bit smaller in size and function at low value of voltages due to its less complex building blocks. This reduces both the amount of space and the amount of energy used. needs, as well as better performance at high frequencies. When it comes to ICs, Current-Mode has a few benefits over Voltage-Mode:

• Improved performance: high speed, wide signal with dynamic range, low requirement of power consumption at high frequencies, reduced low switching noise and cross-talk.

• structural advantages: no extra components for current summation, less complex schematic, and regulated gain without using feedback components[2]

3.2 CURRENT CONVEYORS:-

A voltage buffer at the input side end and a current follower at the output end make up a Current Conveyor, which is an active building block. It's a circuit with a gain of one. Current conveyors have a high linearity, which is one of the most desirable characteristics of analogue circuits, as well as a large dynamic range and a higher working frequency. Current conveyors, unlike op-amp circuits, operate in an open loop mode, resulting in better bandwidth. It does not have a bandwidth and does not have a gain conflict.

$$\begin{bmatrix} iy \\ vx \\ iz \end{bmatrix} = \begin{bmatrix} 1/ry & 0 & 0 \\ \alpha & rx & 0 \\ 0 & \pm\beta & 1/rz \end{bmatrix} \begin{bmatrix} vy \\ ix \\ vz \end{bmatrix}$$

where ry, rz, rx, and are, respectively, parasitic valued resistance at the X terminal, parasitic valued resistance at the Z terminal, , parasitic resistance at the Y terminal, voltage gain in between the X and Y terminals, and current gain between the Z and X terminals. CCII+ and CCII, respectively, are related to the + and –.

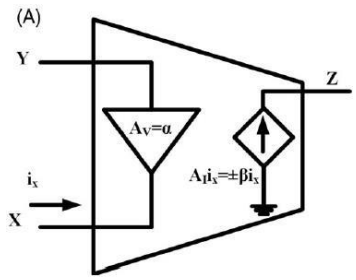

Figure 3.1: Block diagram of Current CCII [11]

As depicted in Figure 3.1, the CCII is a 3-terminal network. In Between the Y and X ends, there is unity voltage gain, and between the Z and X nodes, there is unity current gain. It has a high (preferably infinite) value impedance at the input voltage node Y, a very low (ideally 0) impedance at the input current node X, and a very high (ideally infinite) impedance at the output current port.

3.2.1CURRENT CONVEYOR'S TRANSISTOR LEVEL IMPLEMENTATION:-

The second generation CCII can be implemented in two different topologies. These are the classes A and AB. Class AB is superior to class A in parameters of bidirectional current output, bandwidth, and current gain or voltage gain stability. To ensure proper operation, the bias currents Ibais1 and Ibais2 must be equal; in order to set the quiescent current IB, the bias currents Ibais1 and Ibais2 must be equal. The current flow through X in this circuit is not linearly separated into two signal paths by using either an PMOS or a NMOS current mirror, which are then summed at port Z [4].

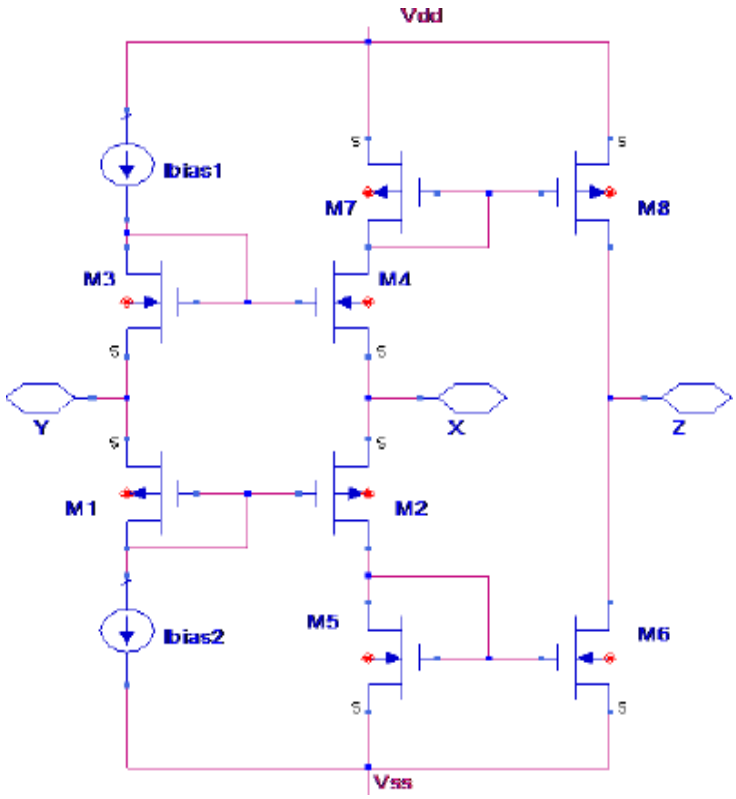

Figure 3.2: Transistor level implementation of CCII+ block [12]

3.2.2 QUASI FLOATING TYPE CURRENT CONVEYOR:-

Figure 3.3 shows the LP LV CCII class AB based on folded cascode OTA. For the operational transconductance amplifier design, the folded cascode architecture was adopted. Because to its increased gain potential and bandwidth. In addition, the input common-mode range is greater than to describe a 2-stage OTA structure. The CCII is made up of a folded and cascode OTA (M1-M11, M1-M11, M1-M11, M1-M11, M1-M11, M1- To produce the unity gain feedback, M11c-M8c) with 1 gain feedback were used. Between the X and Y nodes, there is a gain buffer. The stage of input N-MOST QFG differential N-MOST QFG differential N MOST QFG differential N-MOST QFG differential N-MOST Q-FG differential N-MOST M2 and M1 are two pairs of gate terminals that are coupled to each other. The enormous resistance value of reverse-biased junction is used by VDD. MR1 and MR2 are diode-connected MOS transistors that operate in the cut-off region. MR4 and MR3 posses large-value resistances that are coupled

in the same way. In parallel with the input capacitors Cin2 and Cin1, This connection has the advantage of allowing the QFG transistors to be used. can also process DC signals M7 and M6 transistors offer a level shift functionality, and the current cascaded. A differential to singleended (M8, M9, M8c, M9c) is provided by mirror (M8, M9, M8c, M9c). conversion. Two more pieces are required for the folded version. M3 and M4 are current sources that provide the current. For the output and input branches, this is required transistors. The 2nd stage of OT A is made up of (M10, M10c) and (M11, M11c).

The branch including the transistors (M12c, M12) and (M13c, M13), which are identical to (M10c, M10) and (M11c, M11), respectively, is the second half of the CCII. IX = IZ Transistors (M13c, M12c) are utilised to boost the voltage. The Z terminal's output resistance. To ensure that this does not happen, a compensation capacitor also be required. stability. As a result, a CC capacitor has been add to form a kind of network of compensation in between the first and second. The folded cascode OT A is at this stage. Mb3-Mb1 transistors with Ibias creates the required current and voltage biases for the device. The folded cascode OTA's first stage. It's worth mentioning that some applications will necessitate the use of additional Z- or Z+ nodes.

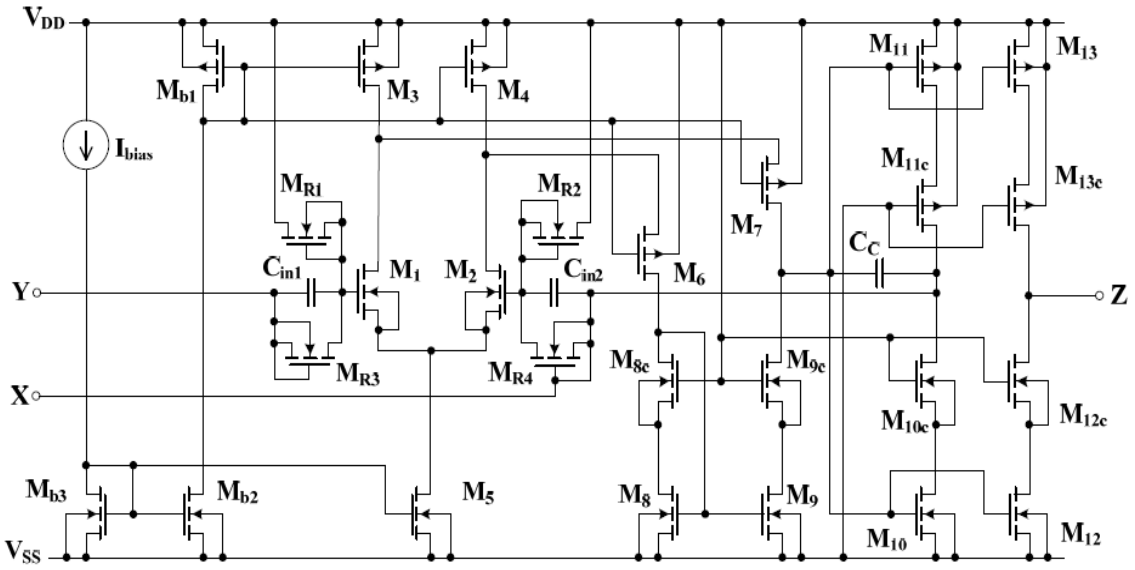

Figure 3.3: Circuit diagram of quasi floating type current conveyor [13]

The number of Z+ nodes can be increased at will. Using the existing mirror approach, for example, an appropriate connection or a cross-coupled current mirror approach To reach the

Zterminals, more CCIIs could be used. are two examples. These many implementation options The parameters of X are unaffected by the Z terminals. The original Z+ terminals, as well as the Y terminals.

3.2.3 FULLY DIFFERENTIAL TYPE CURRENT CONVEYOR:-

The FDCCII's suggested CMOS implementation is based on a technology, difference that is entirely differential as an input stage, a transconductor is used. With two output stages of class AB The FDCCII has the following features: advantages of the single-ended CCII as well as the advantages of the double-ended CCII Fully-differential in nature signal processing is a type of signal processing that uses fully-differential signals. Similarly to how the single ended, The FDCCII, also known as CCII [1], has a wide range of uses. The As indicated in the diagram, FDCCII is essentially a fully differential device.

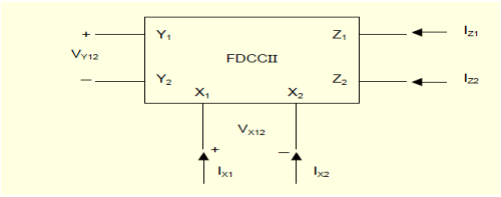

Figure 3.4: Block diagram of FD current conveyor [14]

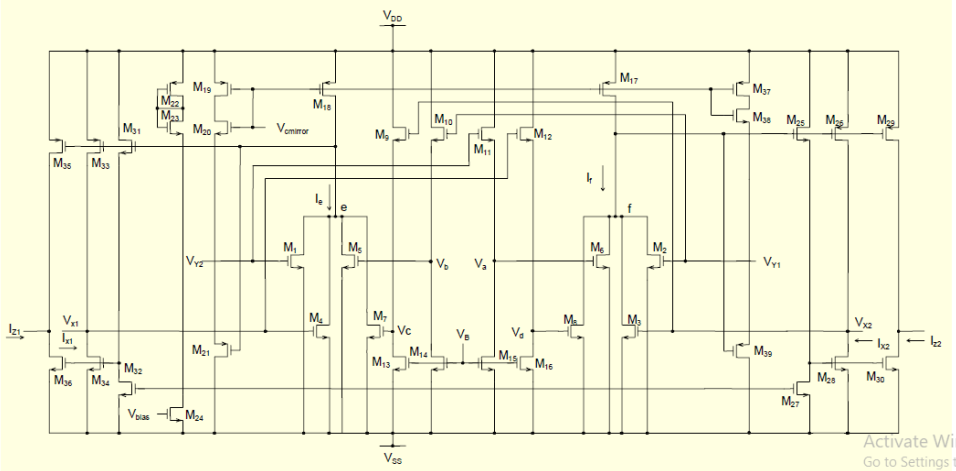

Figure 3.5: Diagram of FD current conveyor circuit [14]

Y2 and Y1 are highvalue of impedance node, while X2 and X1 are low value of impedance points. VY12 is a differential type input voltage provided across the Y2 and Y1 terminals. VX12, a differential voltage, is applied to the terminals. (VX12 is the same as VY12). Currents applied

to the X1 and X2 inputs The terminals are delivered to the Z2 and Z1 nodes, respectively. (Iz1 equals Ix1 and Iz2 equals Ix2). The Z1 and Z2 connectors have a lot of power. appropriate impedance nodes for current outputs.

3.2.4 CURRENT CONVEYOR APPLICATION:-

It be treated as op-amp in current mode.

i). It can be used as voltage to current converter, voltage buffer, current buffer.

ii). It can be used as current amplifier.

iii). It can be used as current differentiator, current integrator.

iv). It can be used in active filter design.

3.3 VOLTAGE MODE OPERATION:-

In general, voltage mode circuits make up the majority of analogue circuits. And the performance of these circuits was measured in terms of voltage at various stages along the circuit. When we use the VCII block to design a circuit, we can eliminate the problems associated with voltage mode operation. For example, when we compare the voltage mode operation of VCII to that of an Op-Amp, we can eliminate the problems of slew rate and gain bandwidth product because VCII is operated in an open loop configuration, whereas an Op-Amp is typically used in a closed loop configuration. It is possible to overcome the impedance and lower frequency response issues.

3.4 VOLTAGE CONVEYOR:-

The current buffer at the input end and the voltage buffer at the output end make up the Voltage Conveyor, which is an active construction block. It's a circuit with a gain of one. Voltage conveyor has an advantage over current conveyor in that it can be utilised in both voltage and current modes. VCII has a very low output impedance, making it suitable for higher-order design and cascading with other blocks. It has the current conveyor property of being able to deliver current summation of current signals at the Y port. It is preferable to op-amp because it has a larger frequency range and is less complex. This means it can operate with less electricity, less space, and less cost. A higher bandwidth allows for faster operation. In other words, we may

argue that voltage conveyor can provide the best answer for problems with current conveyor circuits and op-amp circuits.

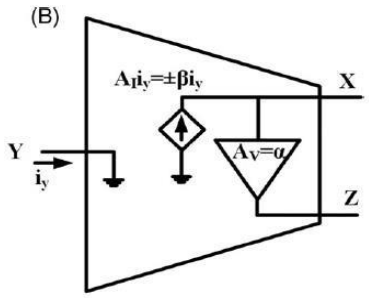

Figure 3.6: Block diagram of Second Generation Voltage Conveyor[11]

The Voltage Conveyor has three terminals. The input current terminal is Y, and output voltage terminal is Z. Between the Y and X ends, the Voltage Conveyor has unity current gain, and between the Z and X ends, it has unity voltage gain.

$$\begin{matrix} ix \\ vy \\ iz \end{matrix} = \begin{matrix} \frac{1}{\pi} + scx & \pm\beta & 0 \\ 0 & ry + sLy & 0 \\ \alpha & 0 & rz + sLz \end{matrix} \begin{matrix} vx \\ iy \\ iz \end{matrix}$$

Where, Ly, ry, Cx, rx, Lz, and rz are the voltage gain between Z and X ends, the current gain in between X and Y terminals, the parasitic resistances associated with Y end (ideally = 0), the parasitic type inductance at Y end (ideally = 0), the parasitic type resistance of X ends (ideally = 0), the parasitic type capacitance of X ends (ideally = 0), the Negligible parasitic values can be attained with the right design. If = +1, we're talking about a VCII+, but if = 1, we're talking about a VCII [1].

$$i_x = \pm\beta . i_y$$

$$V_z = \alpha . V_x$$

$$V_y = 0$$

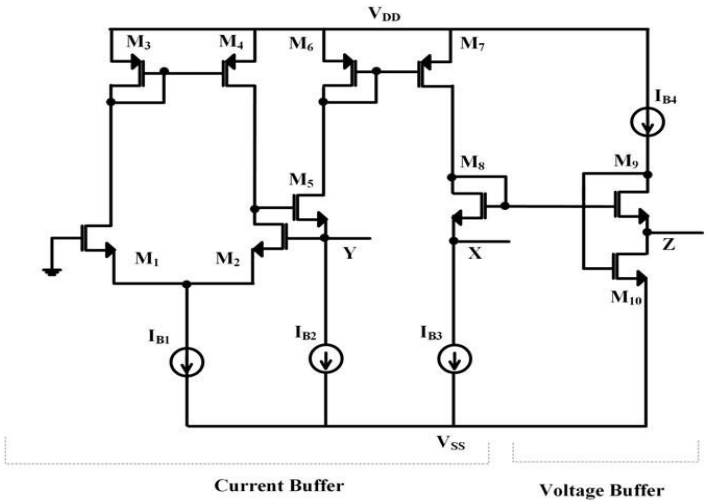

Figure 3.7: Transistor level implementation of VCII block[11]

The circuit depicted above is a transistor-based implementation of the Voltage Conveyor II block. This Voltage Conveyor II block is made up of two stages: a current buffer stage on the input side and a voltage buffer stage on the output port side. This circuit is a class A circuit. A single input stage serves as the input current buffer, while the output voltage buffer is a flipped voltage follower circuit. The VCII's output stage has an extremely low value output impedance, that makes it ideal for voltage mode operation. VCII has a very low input current port impedance, making it ideal for current subtraction. This attribute comes in handy for creating higher-order filters.

3.4.1 RAIL TO RAIL VCII:-

A class AB type of current follower in between the X and Y ends and a R to R rectified voltage follower in between the Z and X terminals make up the planned RtR-VCII. Figure 2 depicts the current buer as envisioned. Transistors M7–M1 and current sources Ib3–Ib1 make up this structure. M3 Transistor in The CG arrangement is biassed by value of voltage that is regulated by the M2–M1 (-)ive feedback loop, which provides virtual ground at the Y end and further reduces its size. impedance. Implementation of the voltage follower is based on a customised version of a defined standard class. Figure 3.8 shows an AB voltage follower [23]. The PMOS ML2–ML1 and NMOS MH2–MH1 directinal pairs drive a switching circuit which activates the correct component of the buer, which is the known standard voltage follower Mn2, Mn1, Mp2,

Mp1, or the R to R pair MH8 and MH7 dependent on the reference voltages VHIGH and VLOW. ML7. [23] explains the operating principle in detail. The voltage is fixed via M8 and Ib3. at the M6's drain The gate voltage of M8 (Vbias) can then be set to precisely tune the device. The Y and thus the X terminals are subjected to a bias current. To attenuate the noise, capacitors C1 and C2 are utilised. The system's stability is ensured by the parameter transfer function. The impedances are as follows: derived from Figure 5 shows the tiny signal equivalent model. The impedance value at the Y end is calculated as follows:

$$Z_Y = 1 / g_{mM3} g_{mM1} (r_{dsM1} // r_{OIB1})$$

The planned VCII's topology permits it to be used as a trans-impedance amplifier. It is also possible to accomplish high value gain conversion, even for huge currents, by combining the high drive capacity at X with the R to R behaviour on Z and X. In this example, a VCII is being used as a TIA. Figure 6 shows how a simple resistance value can be used to easily set the conversion gain. ideal formula:

$$V_{out} \_ V_X = I_Y R_{gain}$$

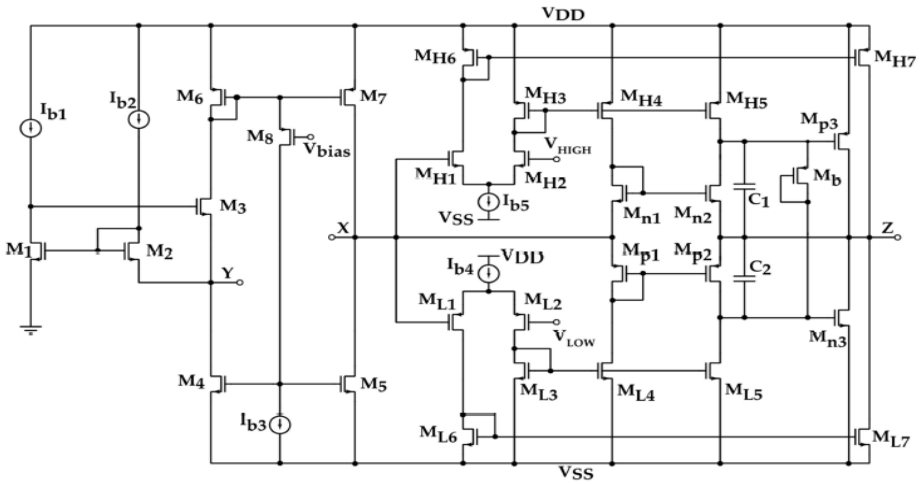

Figure 3.8: Circuit diagram of rail to rail VCII [15]

3.4.2 2nd GENERATION VC:-

A CMOS implementation of a Voltage Conveyor II+. A current follower connects the X and Y ends, and a voltage buffer connects the X and Z terminals. This is the current buffer. It made up of M1-M7 transistors and IB1-IB4 current sources M8, MA1-MA3 and M8 are also used in the voltage buffer. Current sources IB5-IB7 Establishing a negative feedback loop M1-M3 equalises the offset voltage at the Y ends. It also lowers its value of impedance. The second negative feedback loop is referred to as transistors M4-M7 are used to further lower the impedance. At the Y end, current is transferred is input current to the X end. a little amount Based on the corresponding circuit in Fig. 7, signal analysis yields the impedance at X and Y ends and also the current transfer gain beta between Y and X terminal.

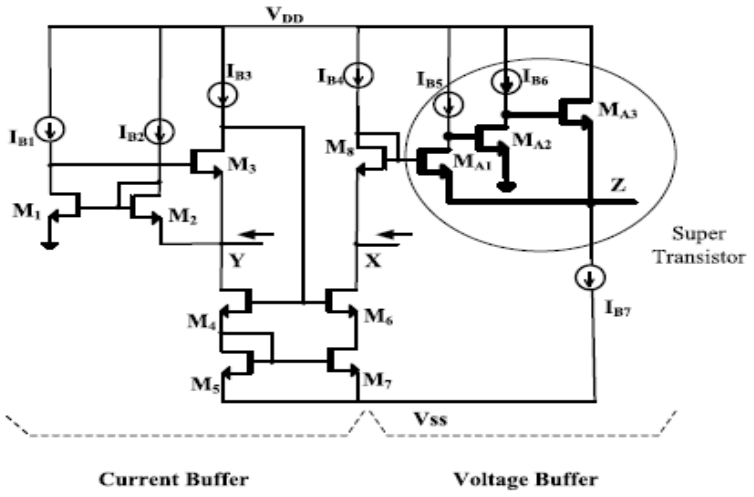

Figure 3.9: Circuit diagram of VCII using super transistor concept[16]

A voltage buffer has also been implemented using a super transistor (MA1-MA3) [13], [14]. The super transistor's negative feedback loop produces an extremely low impedance at high frequencies. The Z terminal, as well as a high level of precision in transferring voltage signals between the terminals Z and X The examination of the little signal [14] describes a super transistor.

CHAPTER 4

PREVIOUSLY IMPLEMENTED VCII SIMULATION RESULTS

In this chapter we have shown the results which we obtain after simulation. First we have shown the parameters which we used in our simulation then the parameters which were given in followed research paper. After then we have pasted the results we have achieved. In last we tabulated all the results.

4.1 SIMULATION RESULTS:-

Table 4.1: Transistor sizing used in simulation of the Voltage Conveyor II circuit

Transistor	W(nm)	L(nm)
$M_{1,2}$	900	120
$M_{3,4}$	360	120
M_5	720	120
$M_{6,7}$	540	120
$M_{8,9}$	740	120
M_{10}	240	120

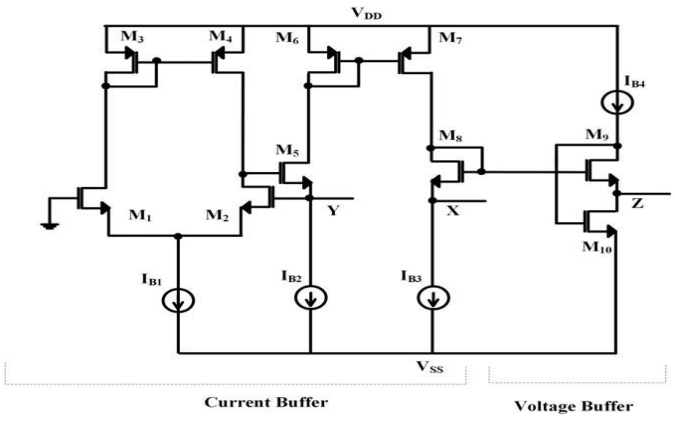

Figure 4.1: Circuit diagram of Voltage Conveyor II [11]

Table 4.2: Transistor sizing used in circuit given in refrence paper[3]

Transistor	Width	Length
$M_{1/2}$	21 µm	0.35 µm
$M_{3/4}$	4.2 µm	0.35 µm
M_5	7 µm	0.35 µm
$M_{6/7}$	72.8 µm	4.6 µm
$M_{8/9}$	28.7 µm	1.4 µm
M_{10}	14 µm	52 µm
Bias current	Value	
I_{B1}	30 µA	
$I_{B2/B3/B4}$	40 µA	

Tool usedfor simulation is Cadence Virtuoso.

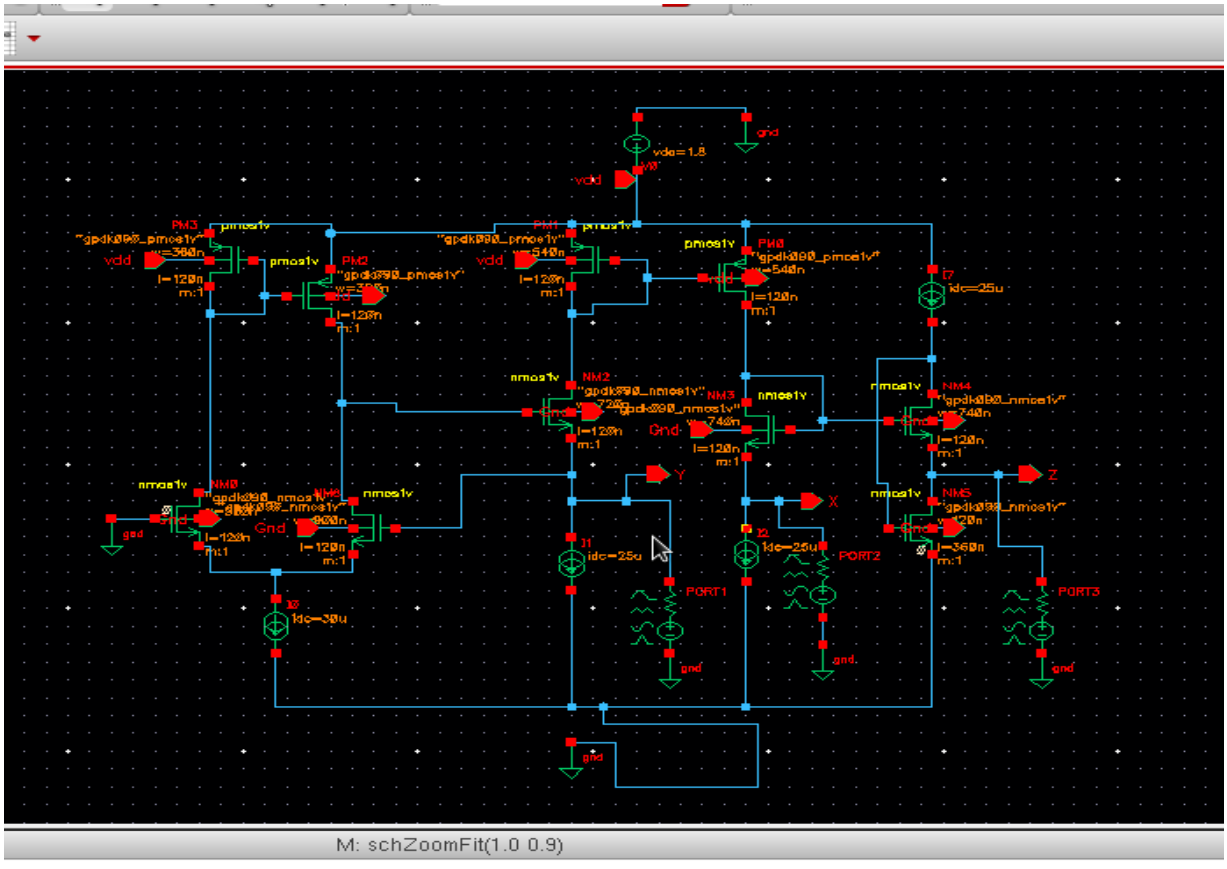

Figure 4.2: Circuit diagram of voltage conveyor II

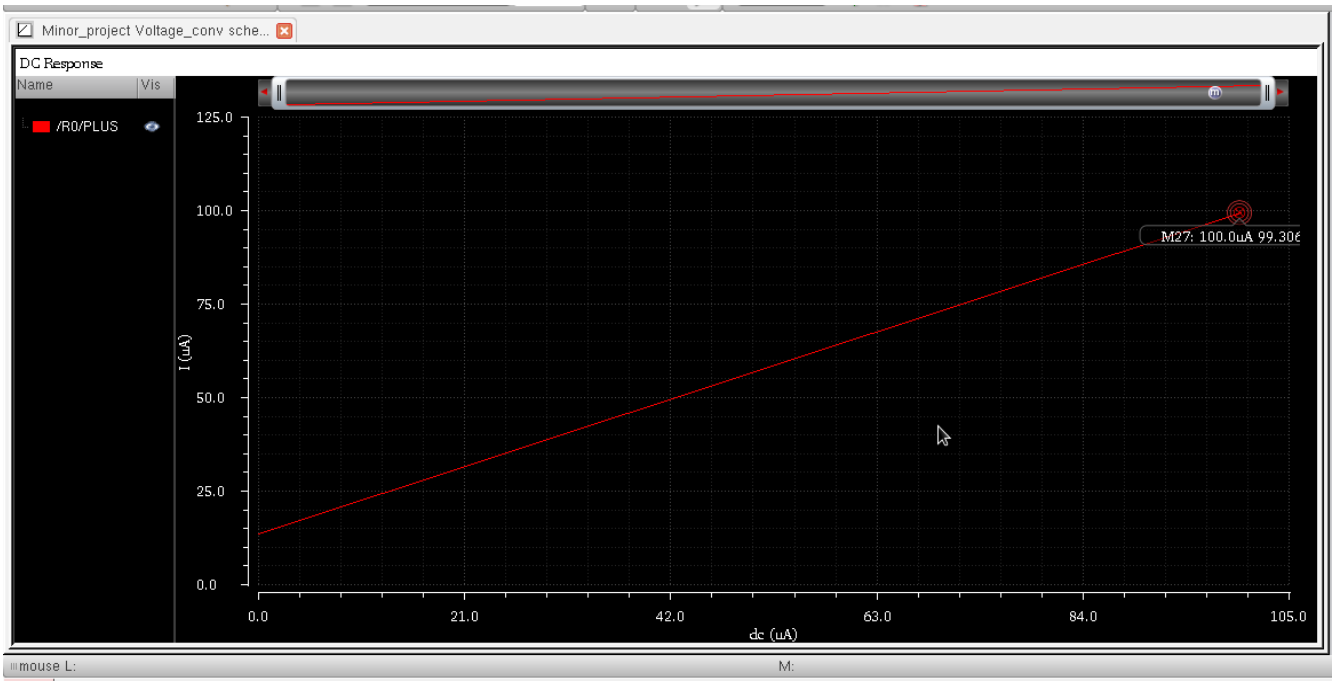

Figure 4.3: Graph plotted between current at y port and at x-port (Current DC analysis)

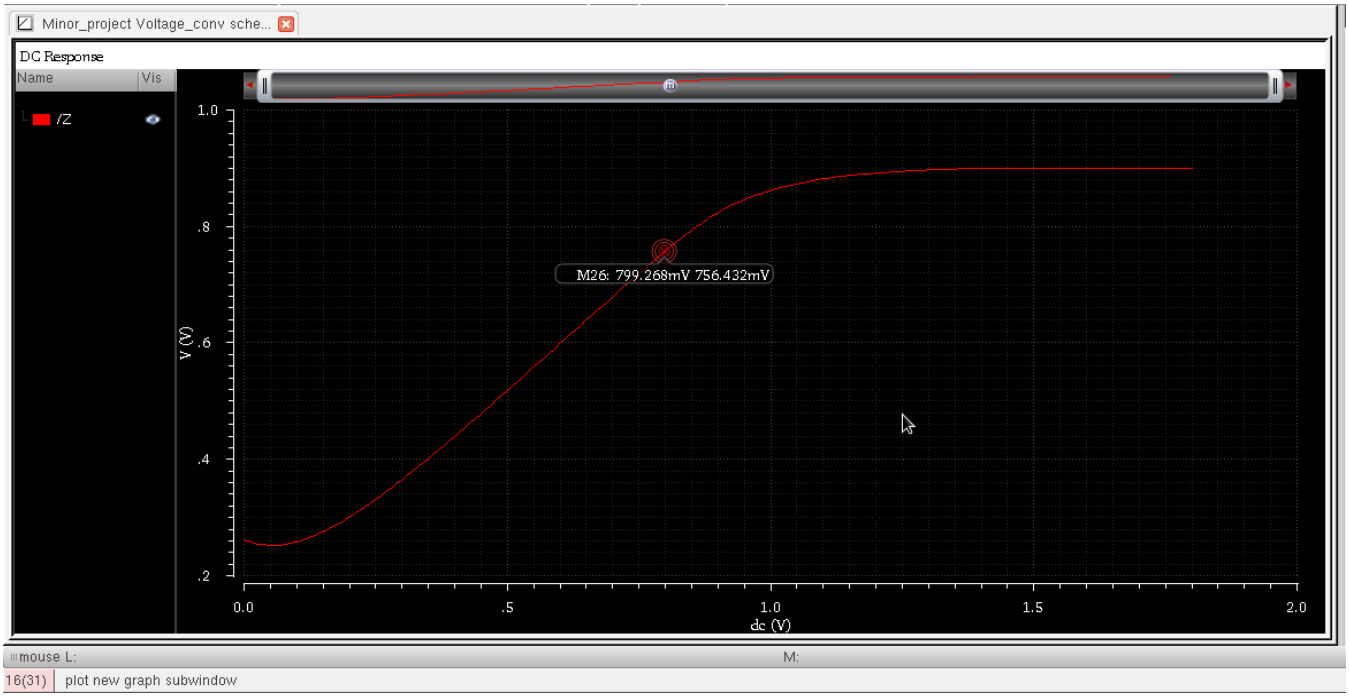

Figure 4.4: Graph plotted between Voltage at x port and z port (Voltage DC analysis)

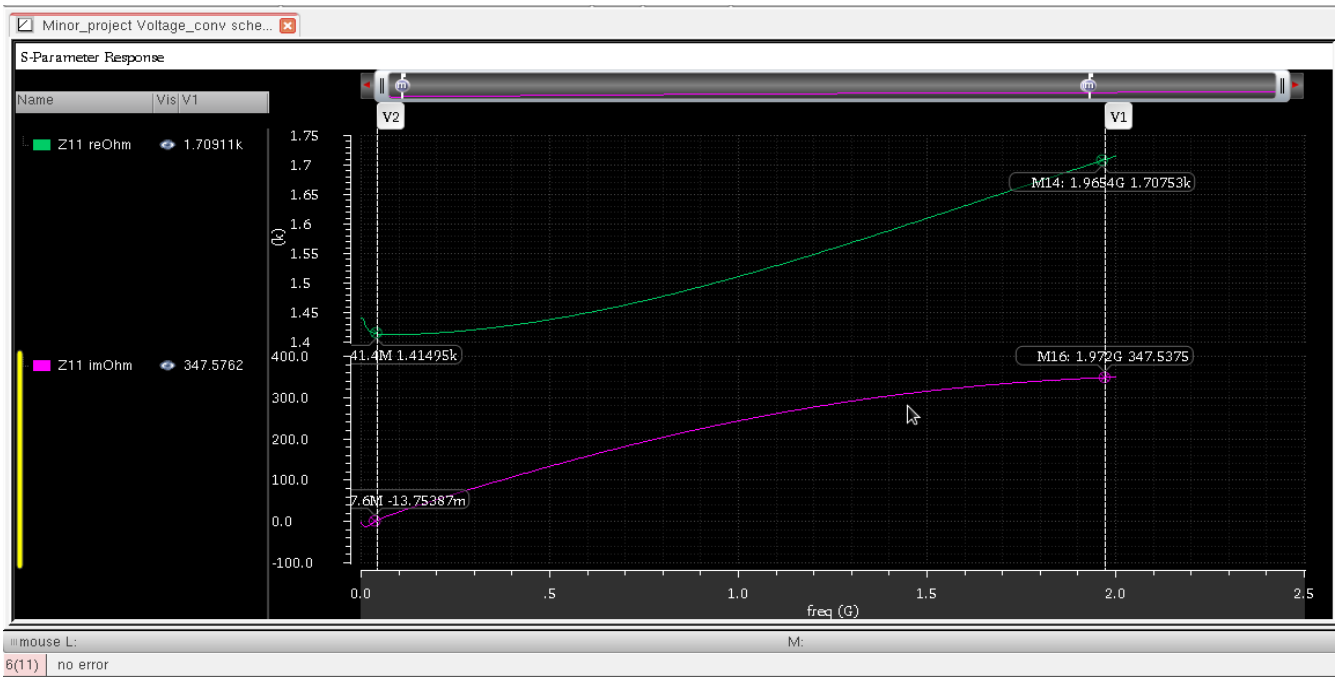

Figure 4.5: Graph plotted for impedance at y port (real & imaginary)

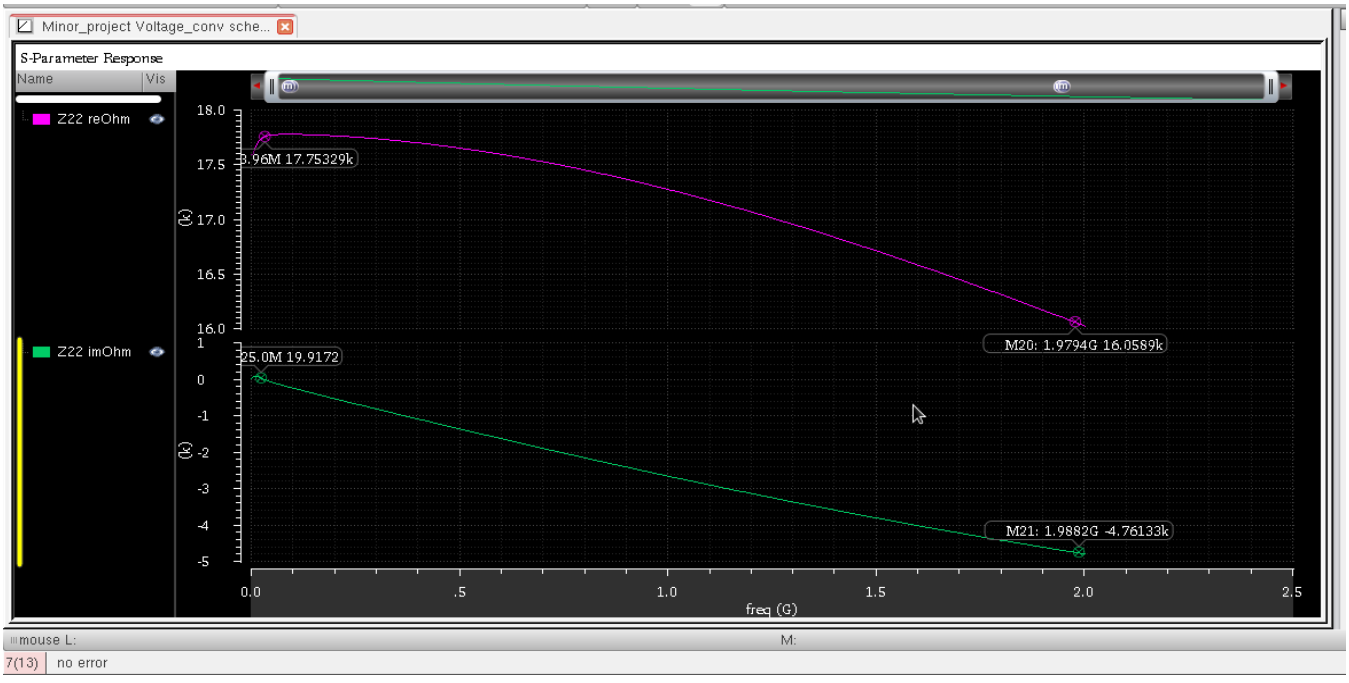

Figure 4.6: Graph plotted for impedance at x port (real & imaginary)

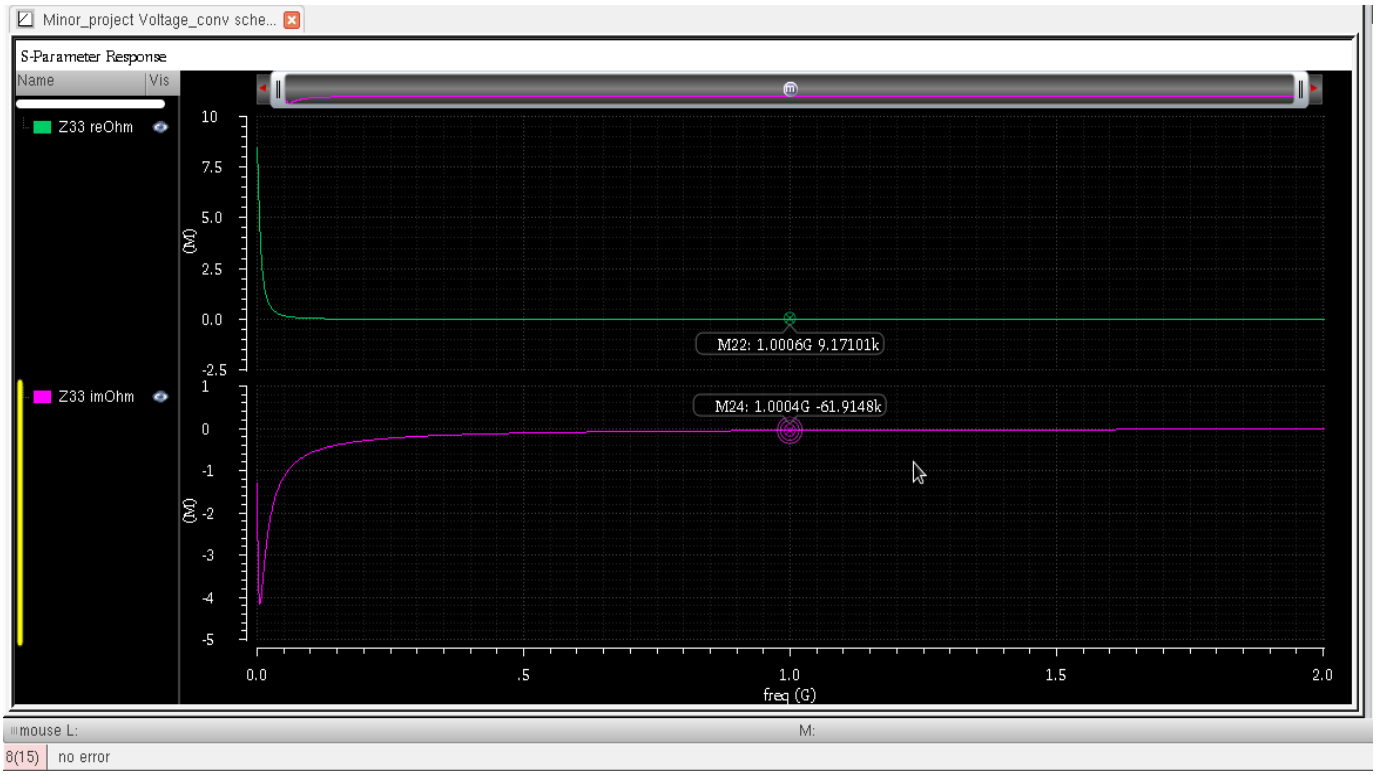

Figure 4.7: Graph plotted for impedance at z port (real & imaginary)

Simultion Results:-

$\beta = 0.993$

$\alpha = 0.945$

$(Z_{11})_{max} = 1.742K$ $(Z_{11})_{min} = 1.414K$

(impedance at Y port) $(Z_{22})_{max} = 17.753K$

$(Z_{22})_{min} = 16.749K$ (impedance at X port)

$Z_{33} = 62.590K$ (impedance at Z port)

4.1.1 Simulatuion Result of fully Differential Current Buffer stage:-

We have used Level 8 parameter file of TSMC (180nm technology node). We have provided 5u ampere and 3u ampere sine wave with 1K Hz frequency, and corresponding fully differential output has observed at the output stage. The channel length parameters and biasing current we used is as follows:

Tool used for simulation is LTspice.

Table 4.3: Aspect ratio and biasing parameters used in simulation of current buffer

Transistor/ Current Source	**Channel Width(um)**	**Channel Length(um)**
M8-M14	10.2	1
M17-M18	30	0.5
M5-M6	5	0.5
M2-M3	5	0.5
M1-M4	2.5	0.5
M10-M16	2	0.5
M7-M15	1.21	0.6
M9-M11	20	2
I1,I2	20uA	
I5	3.6uA	
Vdd	1.8 Volt	

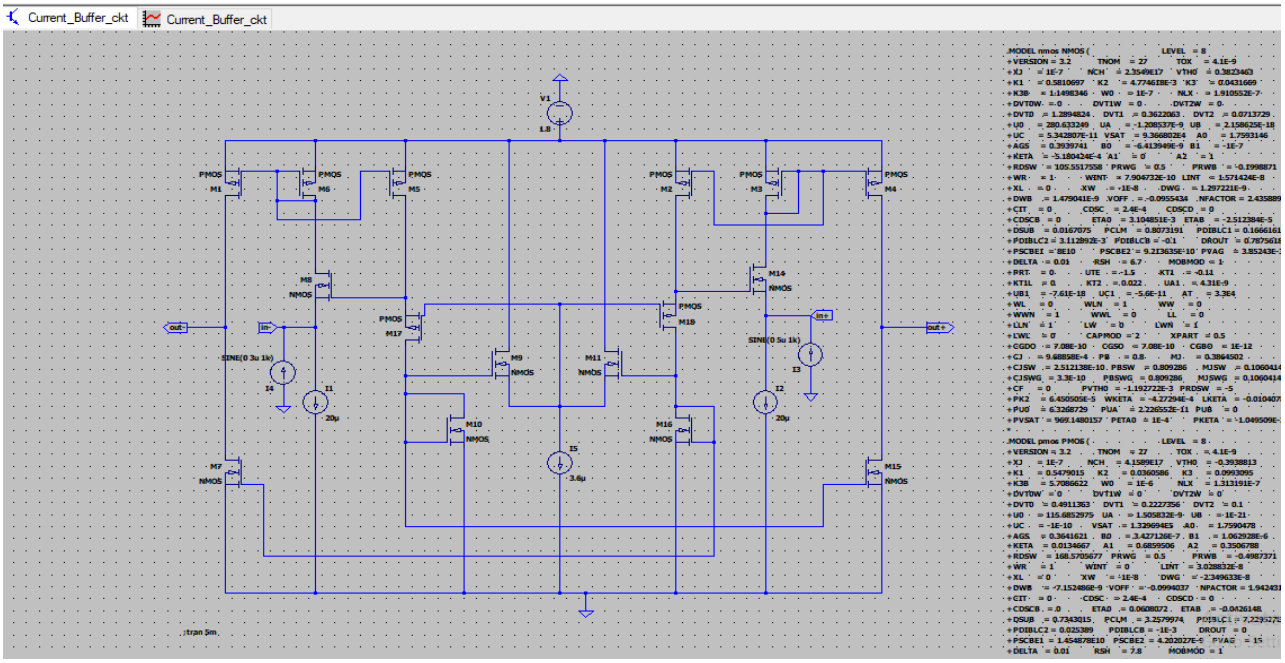

Figure 4.8: Circuit diagram of fully differential current buffer source

For transient analysis we provide sinusoidal waveform at input node since it is a differential type current buffer stage so we can provide both the input with same magnitude and phase or different magnitude and out of phase waveform accordingly output will be plotted at the output stage.

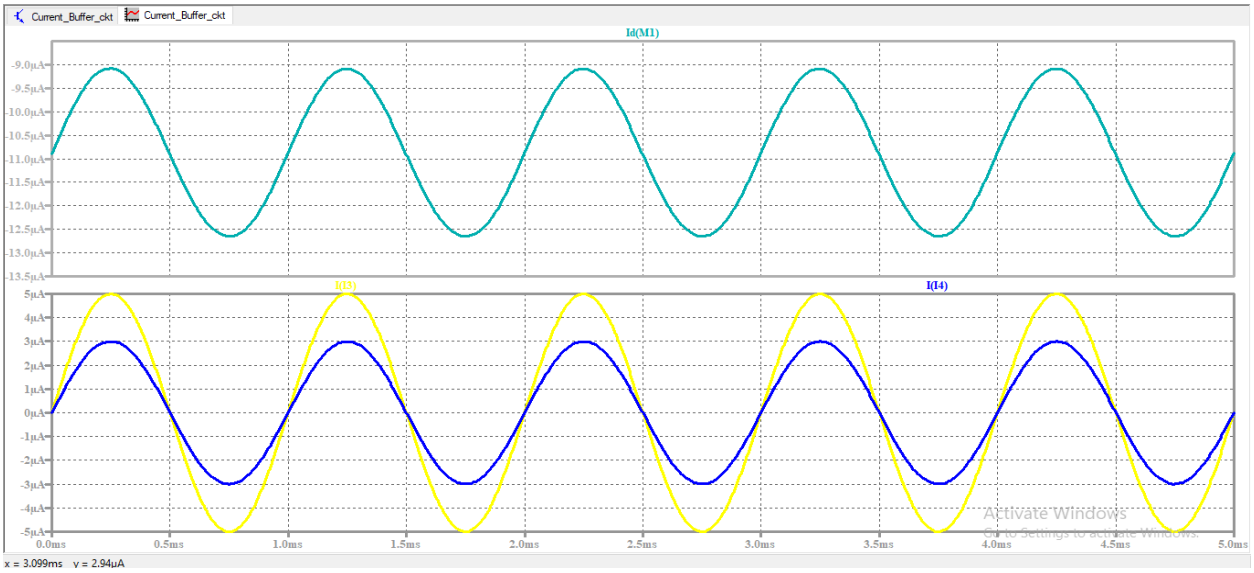

Figure 4.9: Transient response of fully differential current buffer

Table 4.4: Aspect ratio used in voltage conveyor circuit

Transistor/ Current Source	Channel Width(um)	Channel Length(um)
M8-M14	10.2	1
M17-M18	30	0.5
M5-M6	5	0.5
M2-M3	5	0.5
M1-M4	2.5	0.5
M10-M16	2	0.5
M7-M15	1.21	0.6
M9-M11	20	2
M17-M19	30	8
M18	15	1.5
I4	35uA	
I1, I2	20uA	
I5	3.6uA	
Vdd	1.8 Volt	

Y is the input port of conveyor, X is the input port of voltage buffer stage and output port for current buffer and Z is the output port of VCII conveyor.

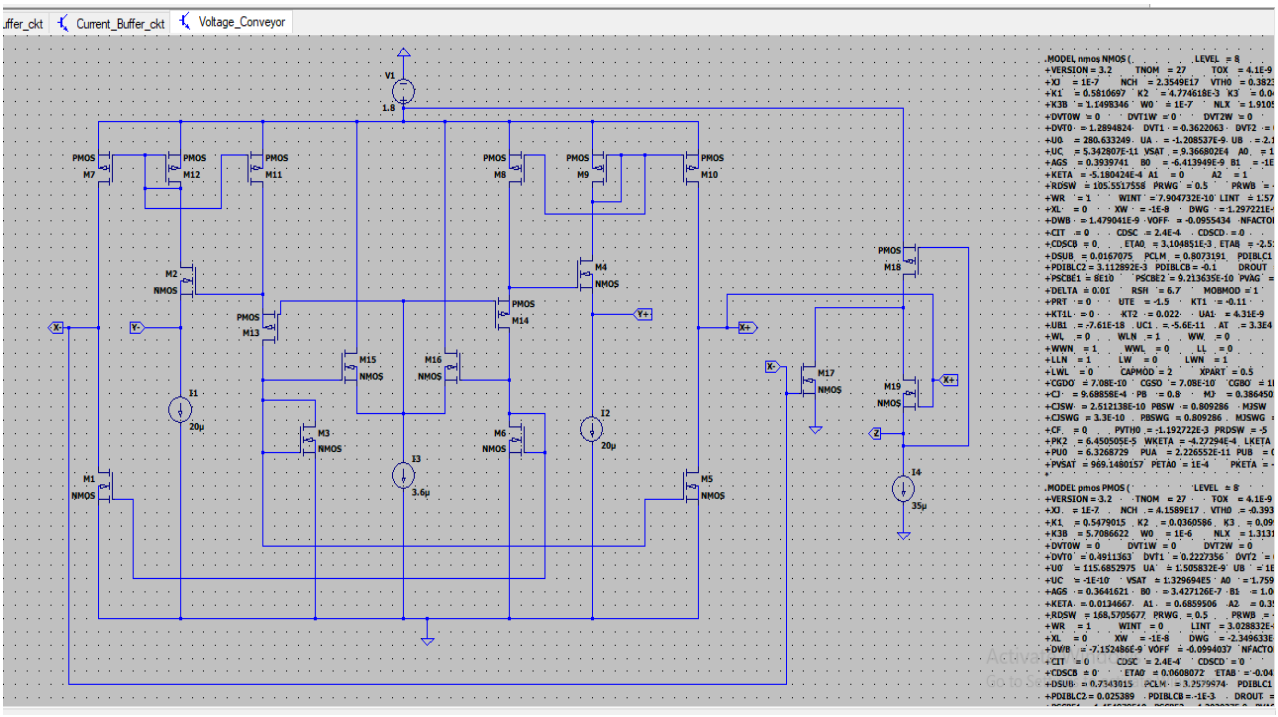

Figure 4.10: Circuit diagram of second generation voltage conveyor

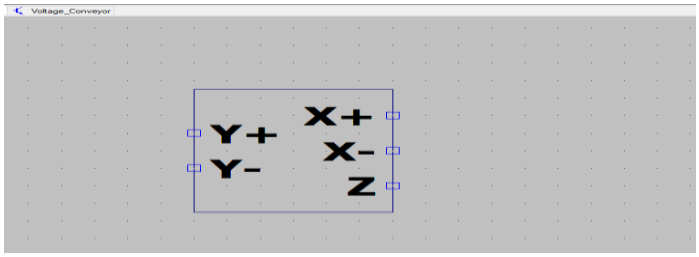

Figure 4.11: Hierarchical symbol of voltage conveyor block

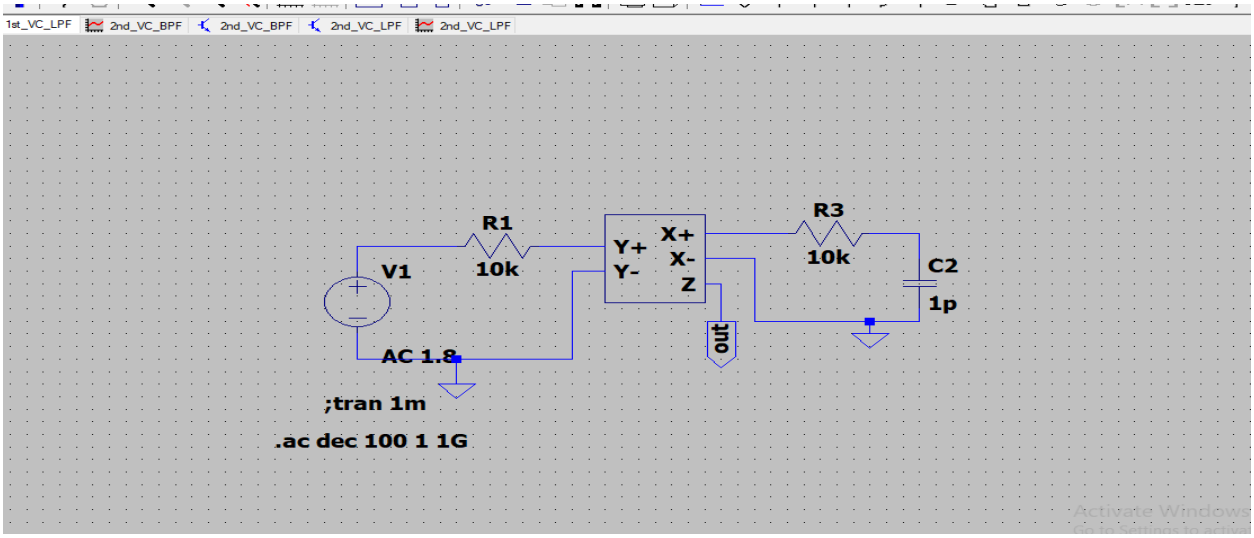

Figure 4.12: Circuit diagram of 1st order active low pass filter using VCII block

Output waveform of 1st order active low pass filter. We have achieved 26.4 MHz cut off frequency for simulated LPF.

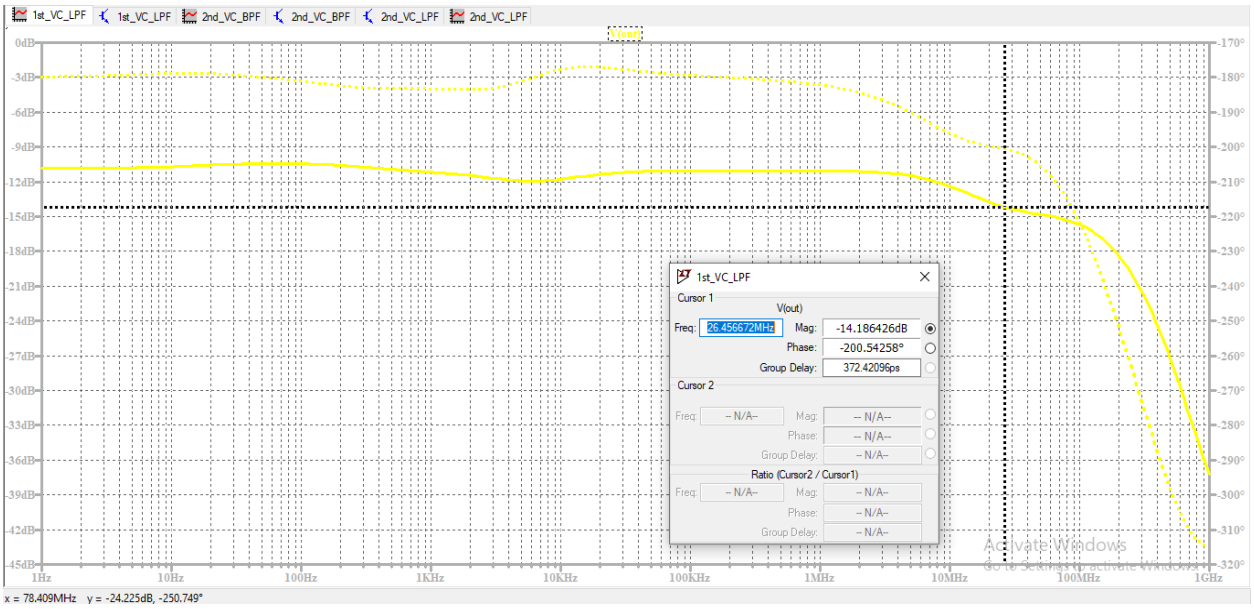

Figure 4.13: Frequency response plot of 1st order active low pass filter

We have designed a Band pass filter using VCII block. We provide a AC signal at the input stage for the AC analysis. From the output plot it is clear we have achieved 72.91MHz 3 dB bandwidth for the designed filter.

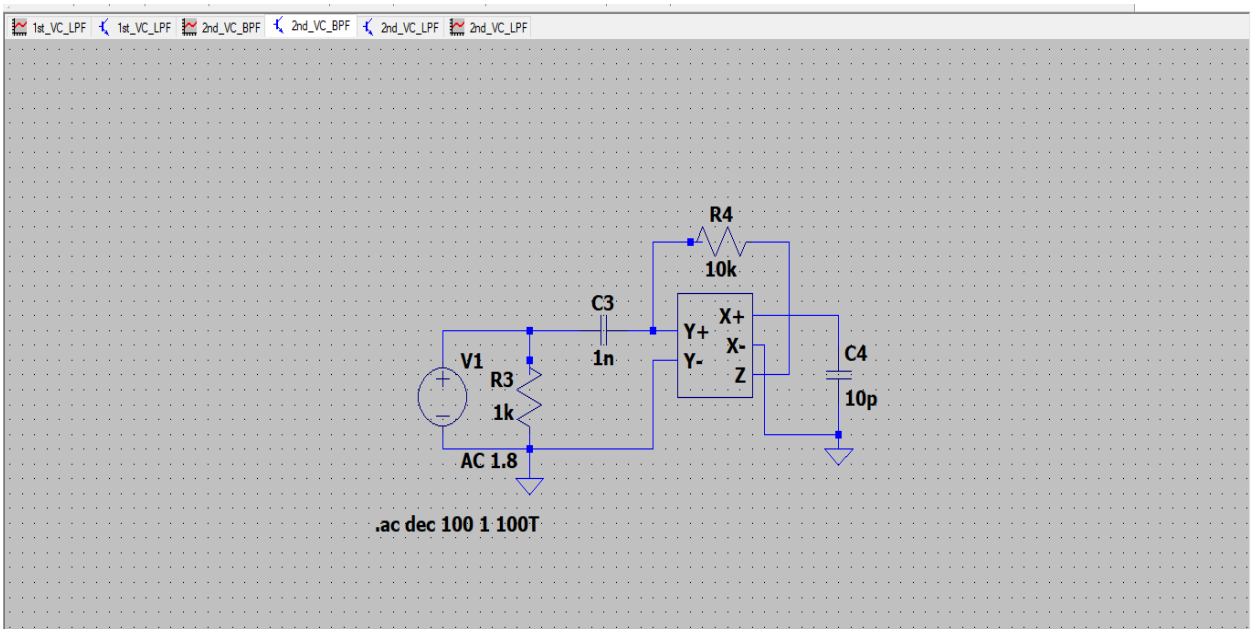

Figure 4.14: Circuit diagram of band pass filter using VCII block

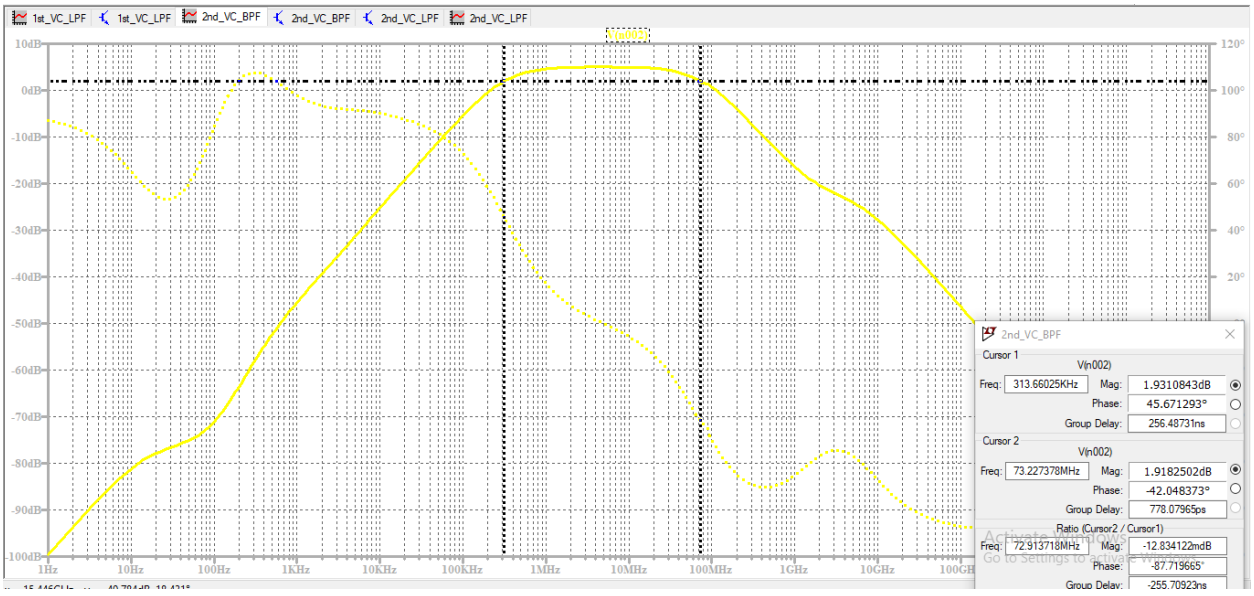

Figure 4.15: Frequency response of active band pass filter

Here we have designed a 2nd order active low pass filter using our simulated VCII block. At the input stage we provide a voltage source with AC signal having magnitude of the signal is 1.8. From the designed circuit we achieved the cut off frequency for the 2nd order LPF is 120.8 MHz. But from the plot we can see that the gain plot is not stable as it should be.

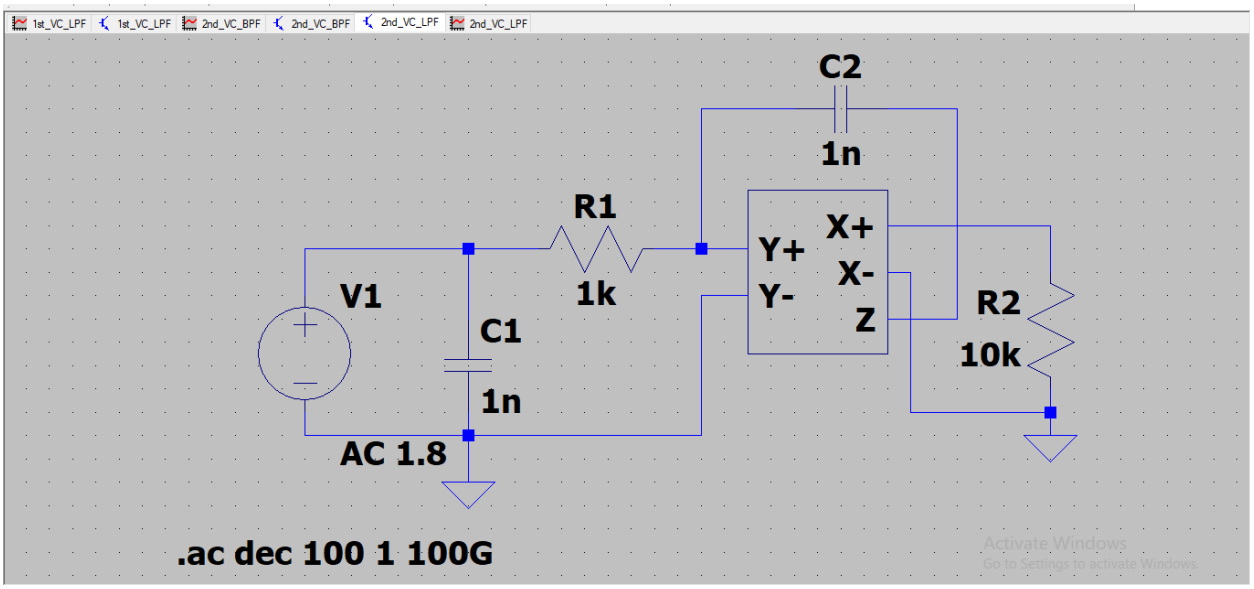

Figure 4.16: Circuit diagram of 2nd order active low pass filter using VCII block

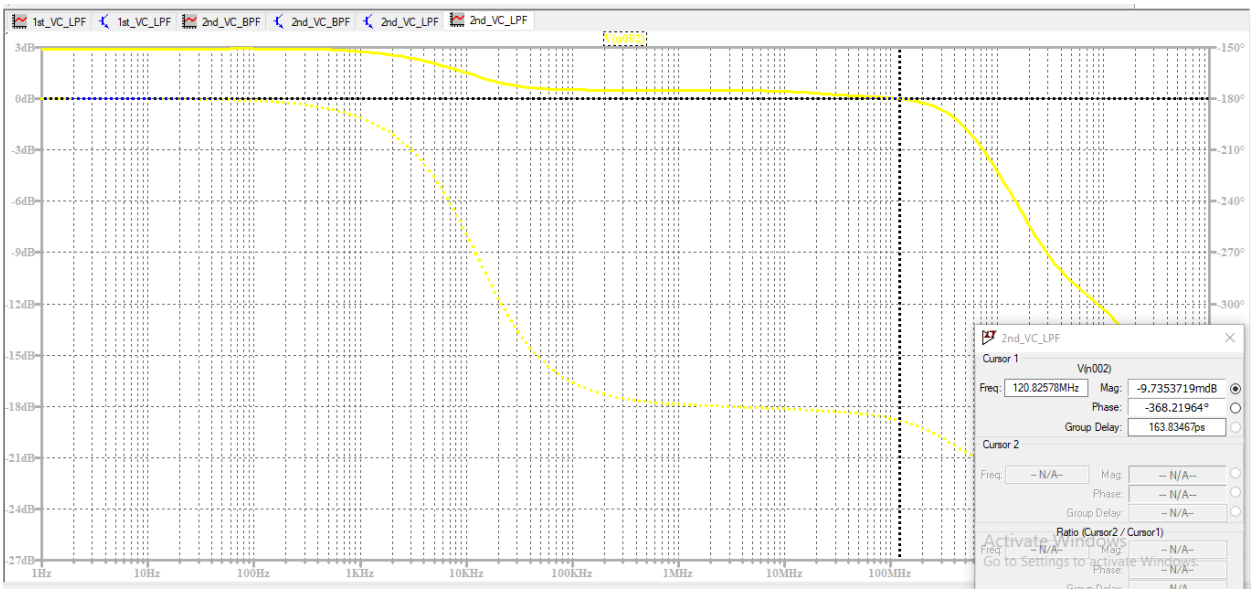

Figure 4.17: Frequency response of 2nd order active low pass filter

CHAPTER 5

SIMULATION RESULTS OF PROPOSED VCII STRUCTURE AND ITS APPLICATION

5.1 Simulation ofProposed voltage conveyor:-

Proposed voltage conveyor consists of two stages firsr one is current buffer and second one is voltage buffer. We have already discussed about the current buffer and voltage buffer stages in previous chapter in much detail. We have simulated these stages individually and verified the results. Results of these stages following almost ideal behavior. In simulation of proposed voltage conveyor we have used TSMC 180 nm parameter file (Level 8).

Table 5.1: Table of aspect ratio used in proposed voltage conveyor circuit

Transistor	Channel Width(um)	Channel Length(um)
M8-M14	10.2	1
M17-M18	30	0.5
M5-M6	5	0.5
M2-M3	5	0.5
M1-M4	2.5	0.5
M10-M16	2	0.5
M7-M15	1.21	0.6
M9-M11	20	2
M12,13,19,22,25	6.3	1
M20	320	1
M21	429	1
M23	0.5	1
M24	1230	0.5
M26	627	1
M27	12.5	1

M28,29,34,36,37	1.6	1
M30	3.2	1
M31	157	1
M32	108	1
M33	350	0.5
M35	82	1

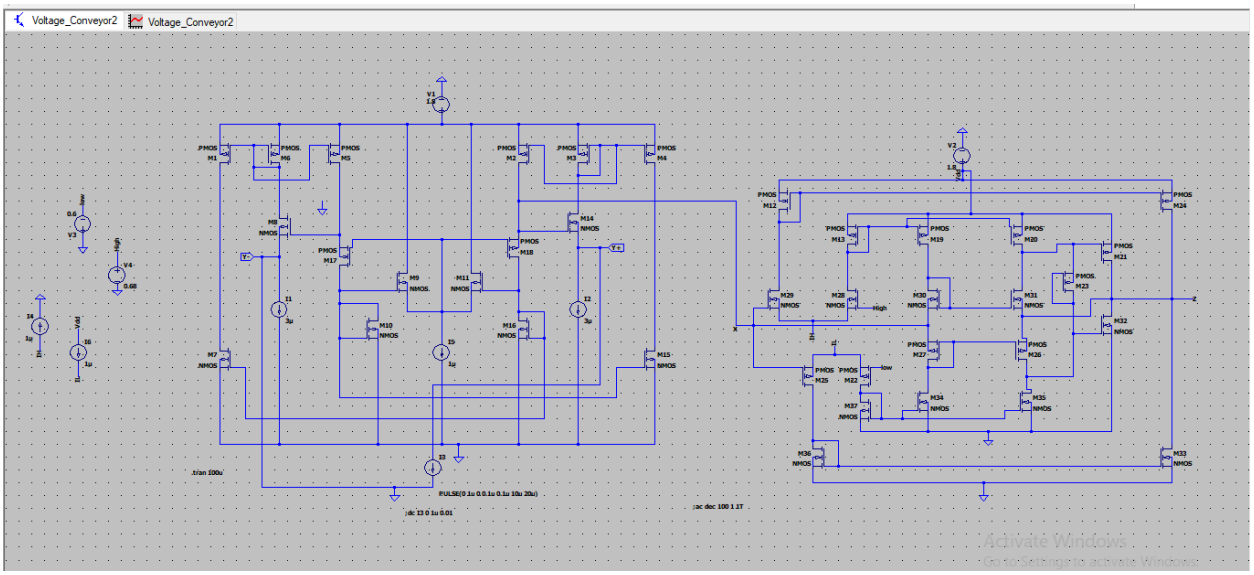

Figure 5.1: Circuit diagram of Proposed second generation voltage conveyor

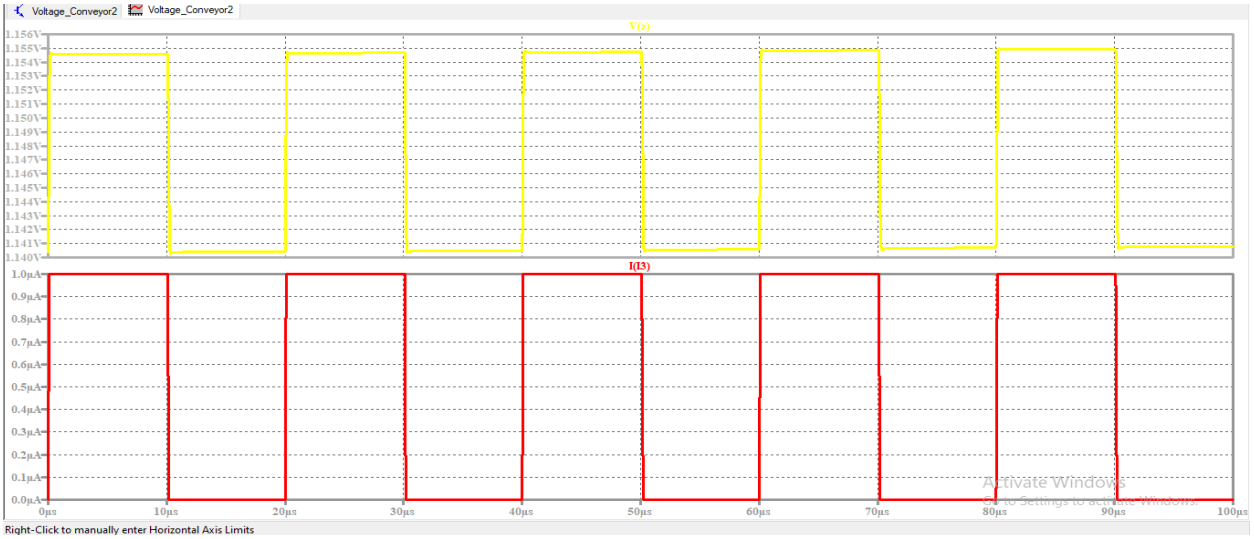

Figure 5.2: Transient step response of proposed VCII circuit

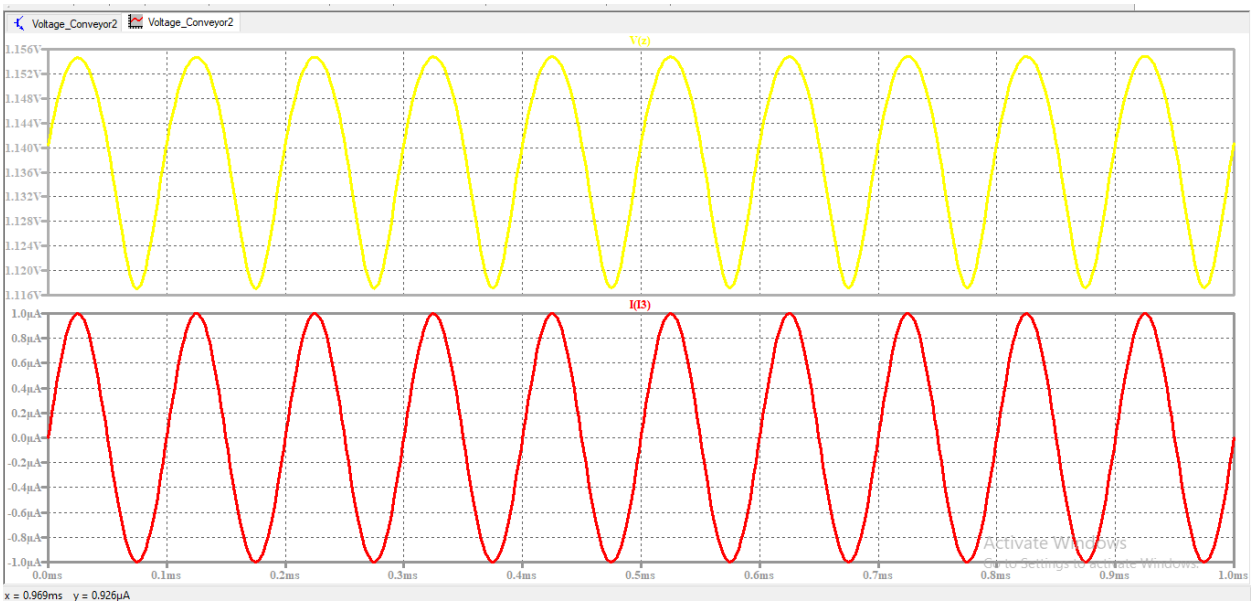

Figure 5.3: Transient response of proposed VCII circuit

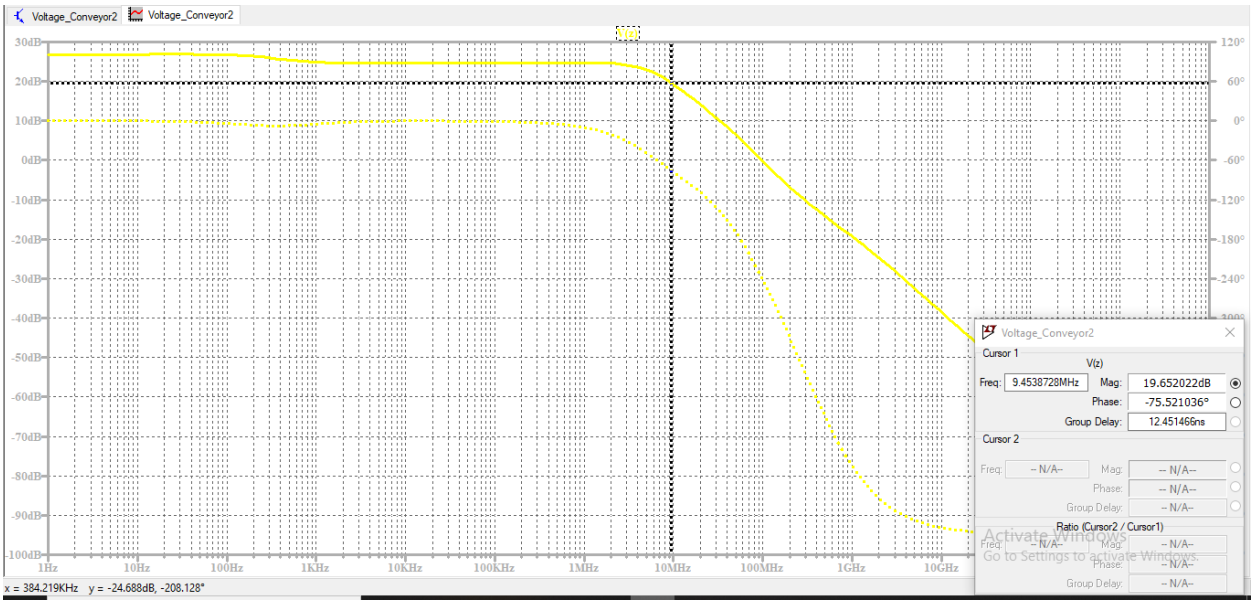

Figure 5.4: AC analysis of proposed VCII circuit

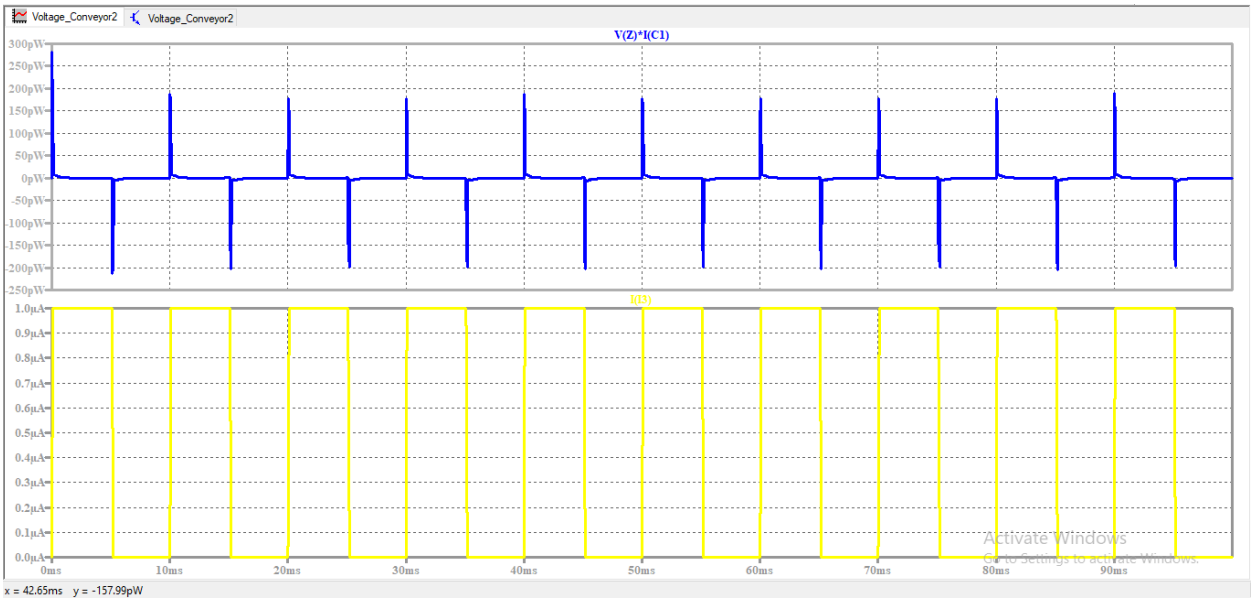

Figure 5.5: Plot of Power consumption across the load capacitor with respect to the square waveform at the input

5.2 Simulation of Applications of VCII block:-

i). Simulation of voltage amplifier circuit using voltage conveyor

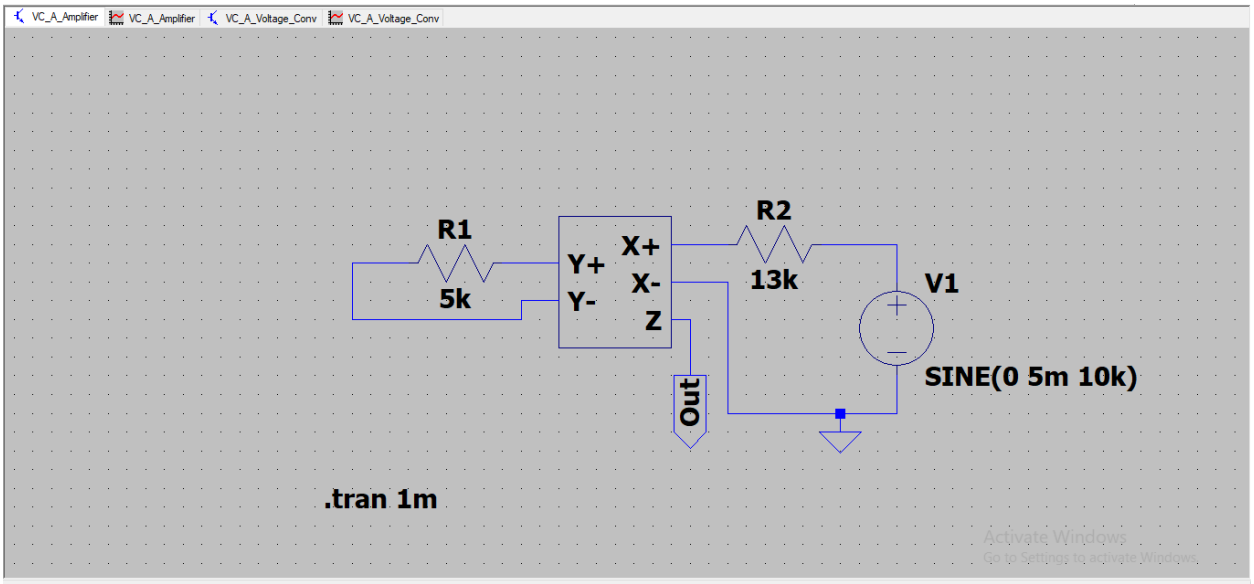

Figure 5.6: Circuit diagram of Voltage Amplifier using VCII block

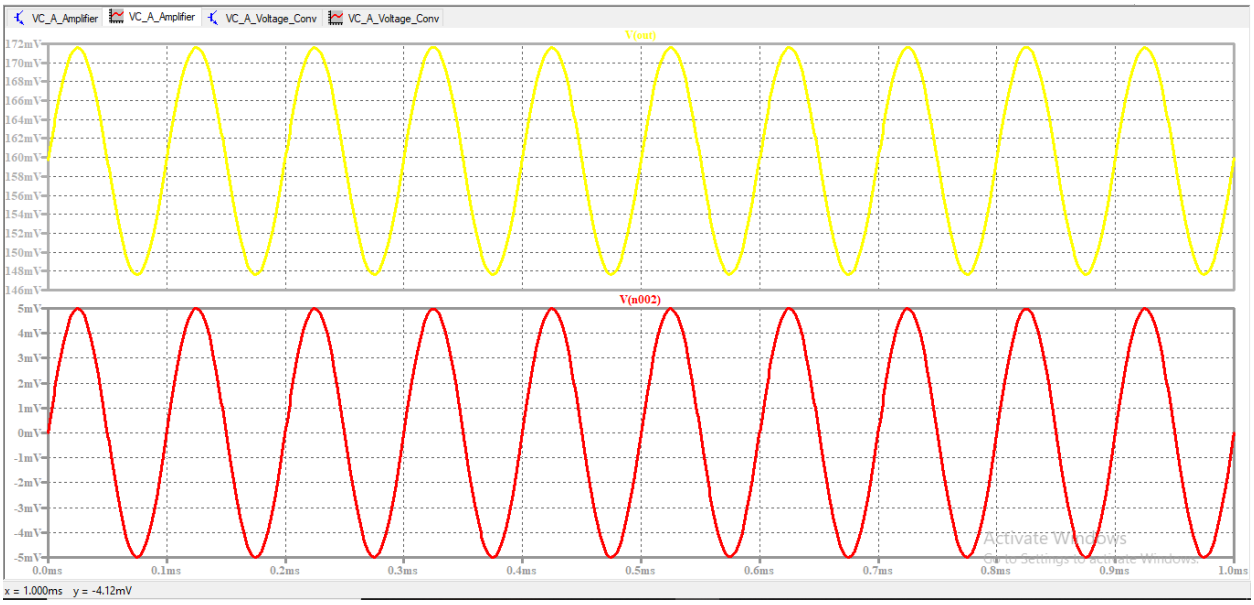

Figure 5.7: Transient response of voltage amplifier implemented using proposed VCII block

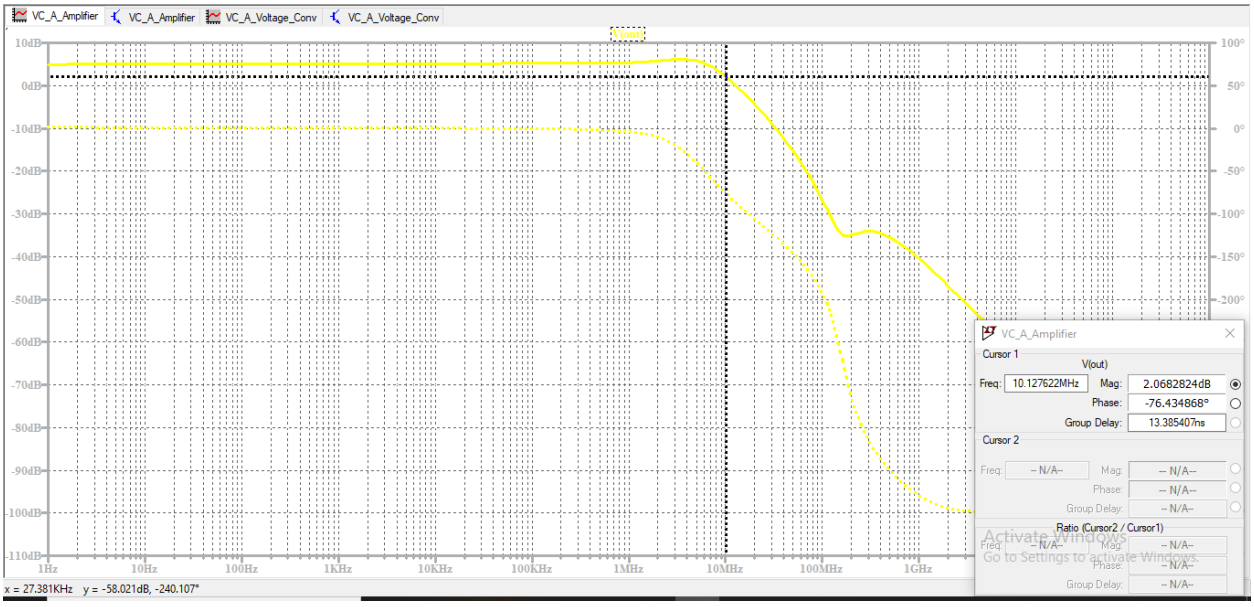

Figure 5.8: Plot of AC analysis of voltage amplifier

ii). Simulation of Current Buffer using VCII block

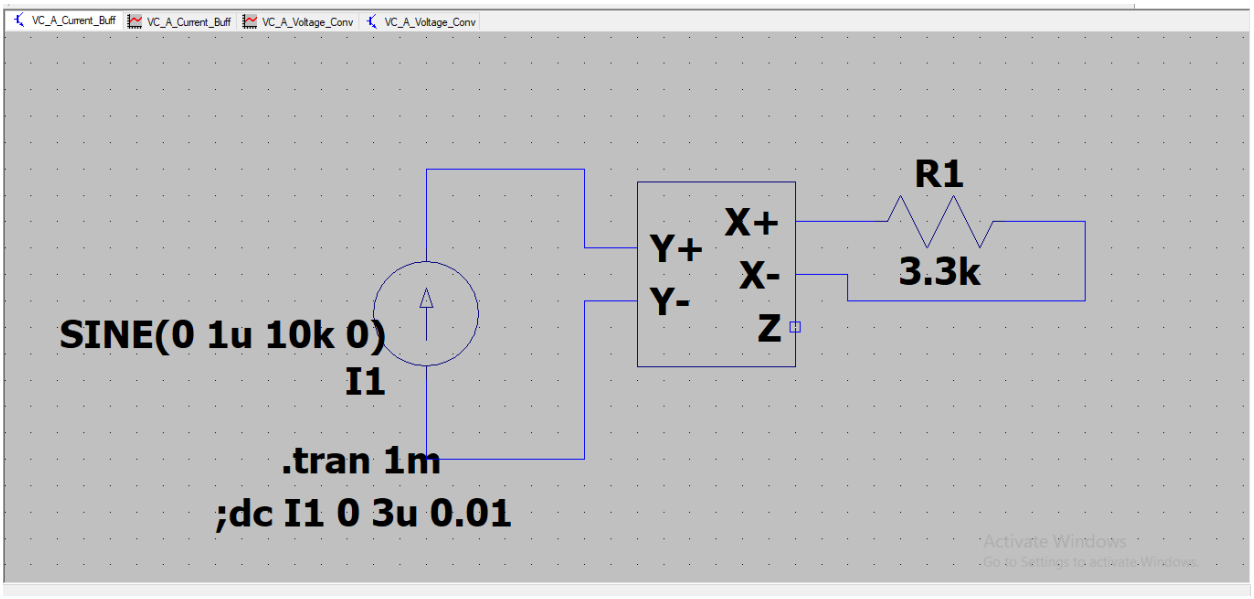

Figure 5.9: Circuit diagram of Current Buffer using proposed VCII block

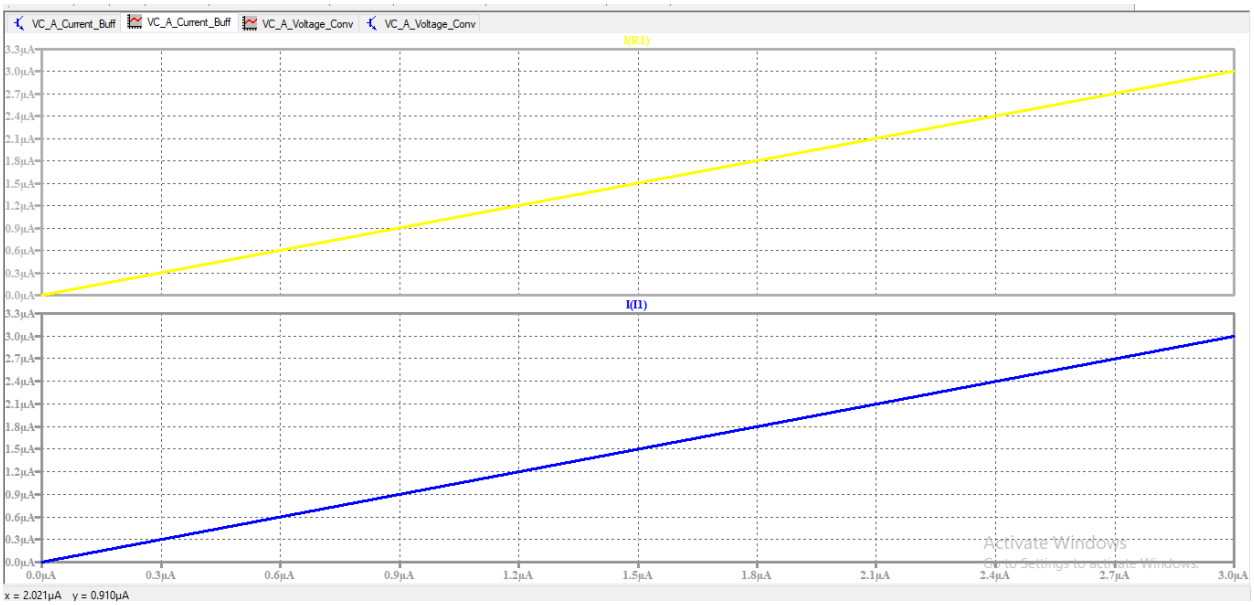

Figure 5.10: Plot of DC analysis of current buffer circuit using VCII block

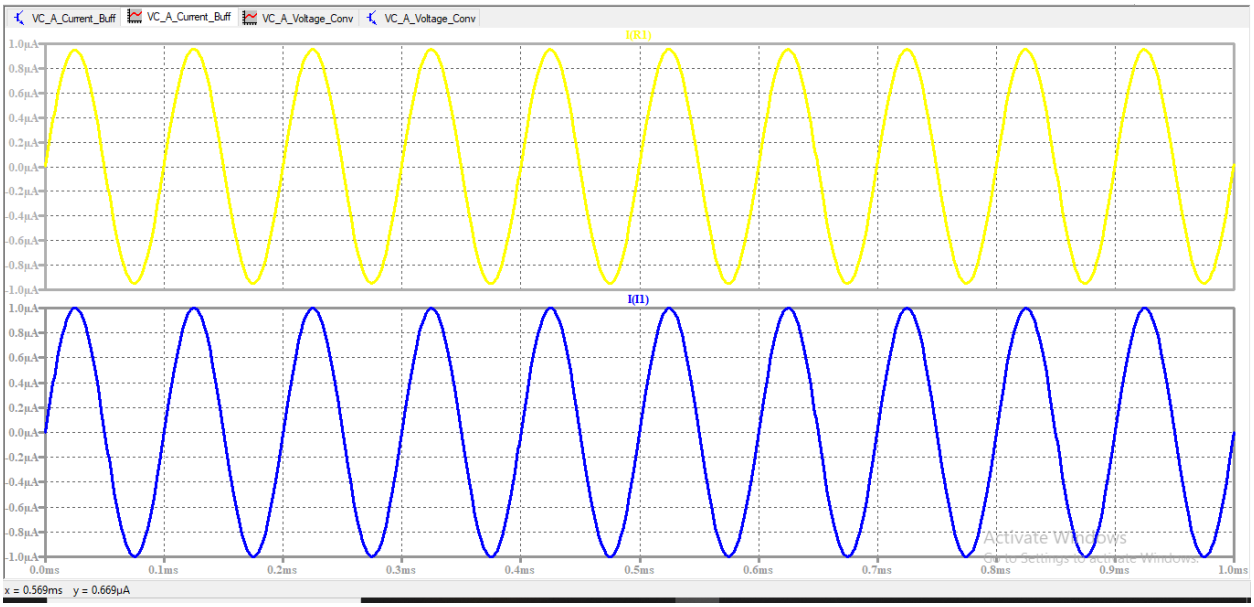

Figure 5.11: Plot of Transient analysis of current buffer circuit using VCII block

iii). Simulation of current to voltage converter using VCII block

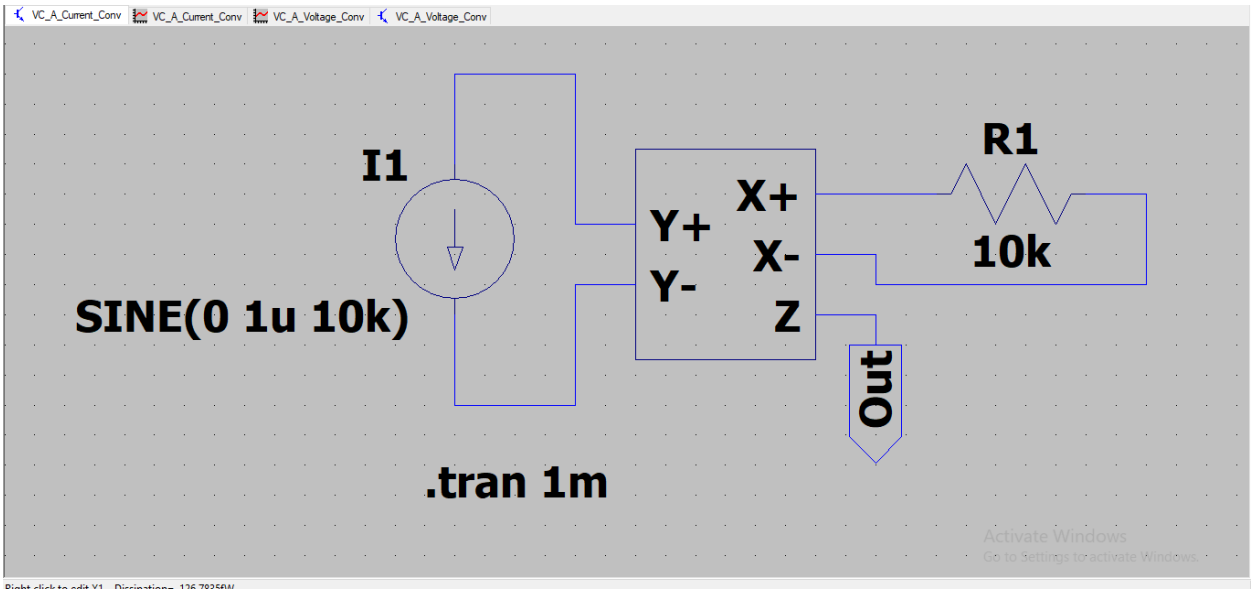

Figure 5.12: Circuit diagram of current to voltage converter using proposed VCII block

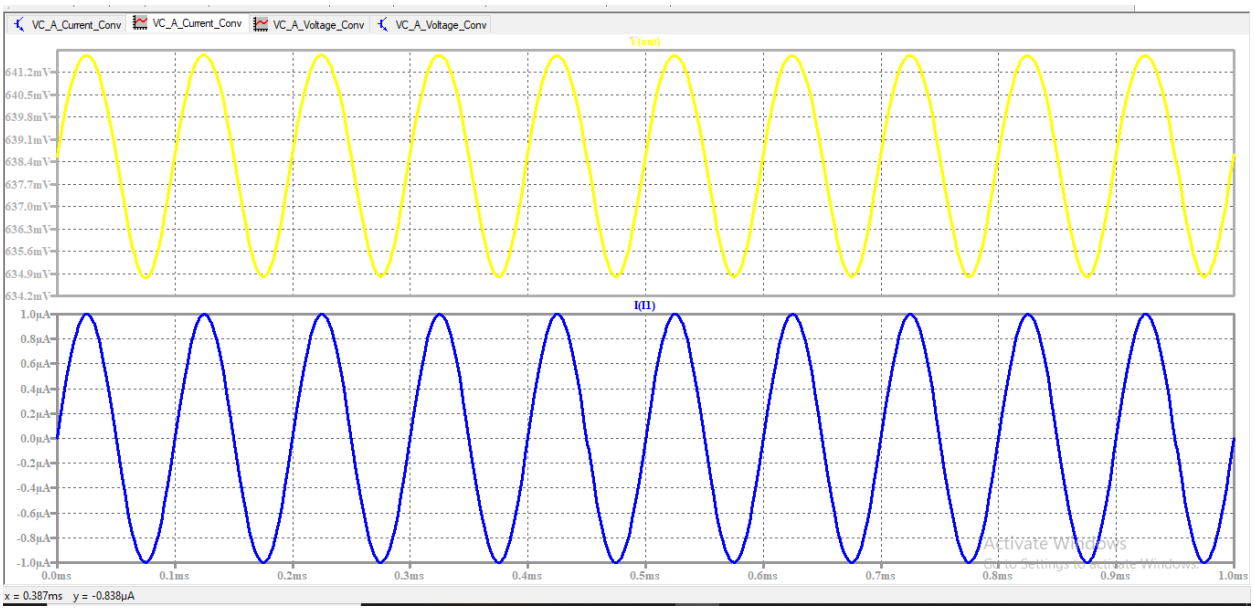

Figure 5.13: Plot of transient analysis of current to voltage converter

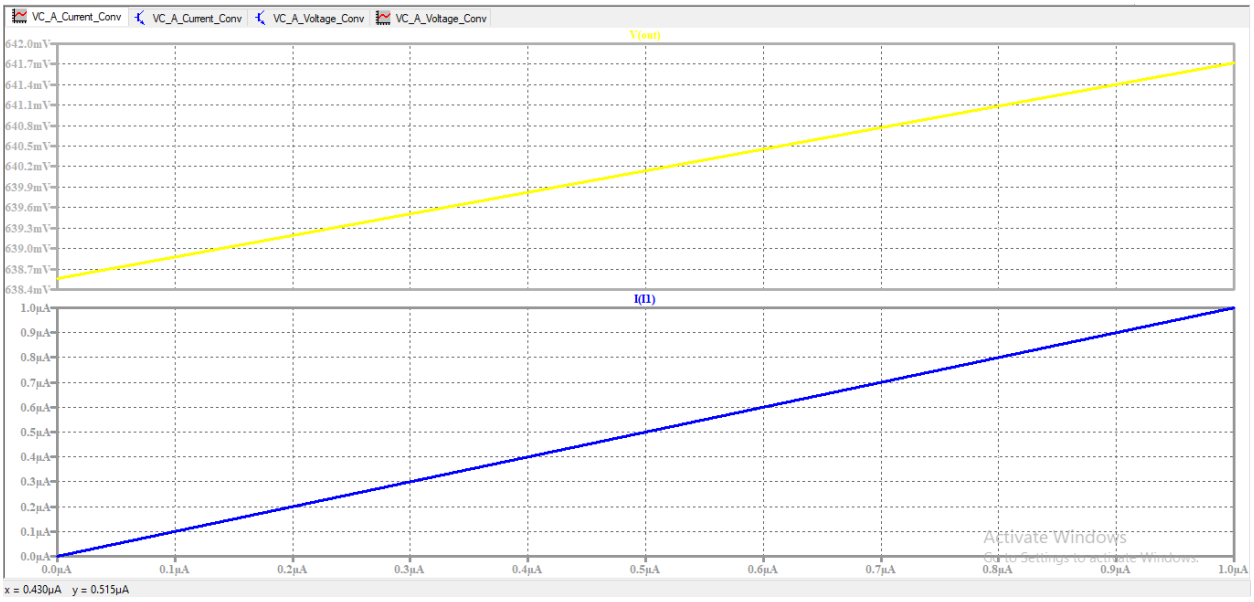

Figure 5.14: Plot of DC analysis of current to voltage converter

iv). Simulation of Voltage differentiator circuit using VCII block

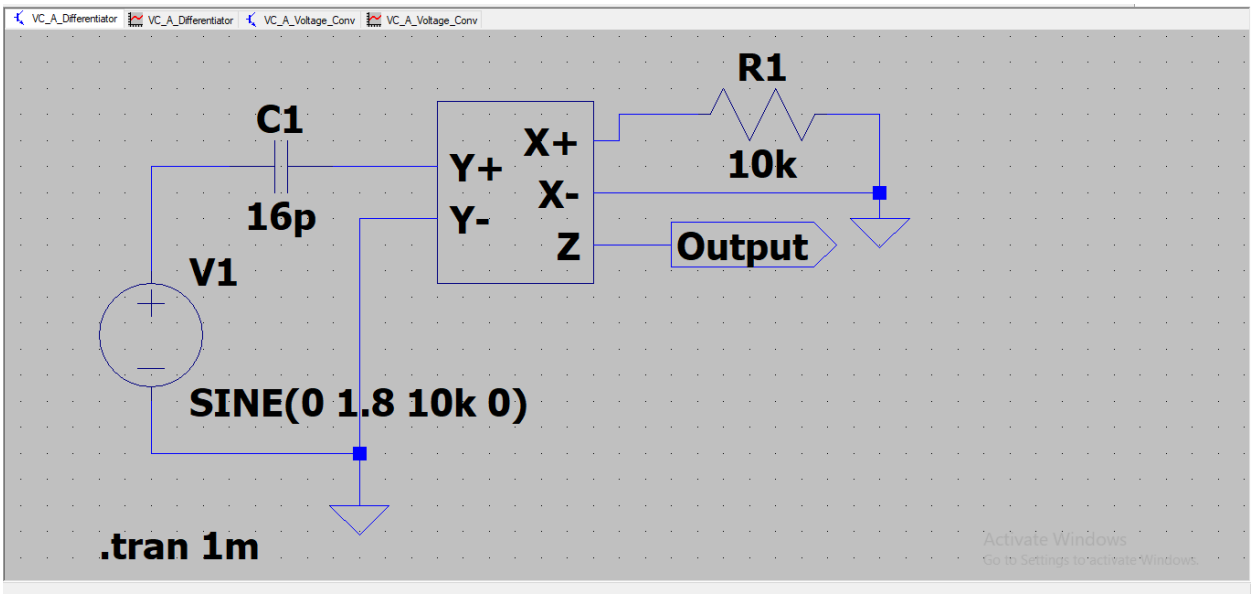

Figure 5.15: Circuit diagram of voltage differentiator using VCII block

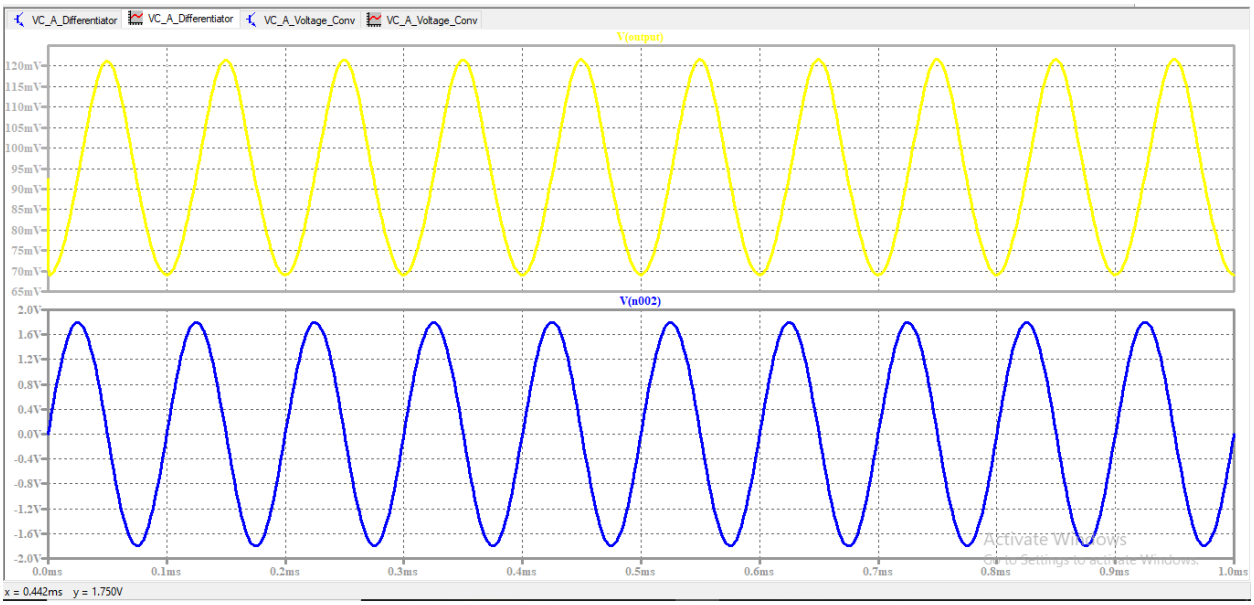

Figure 5.16: Transient analysis of voltage differentiator circuit using VCII block

v). Simulation of voltage integrator using VCII block

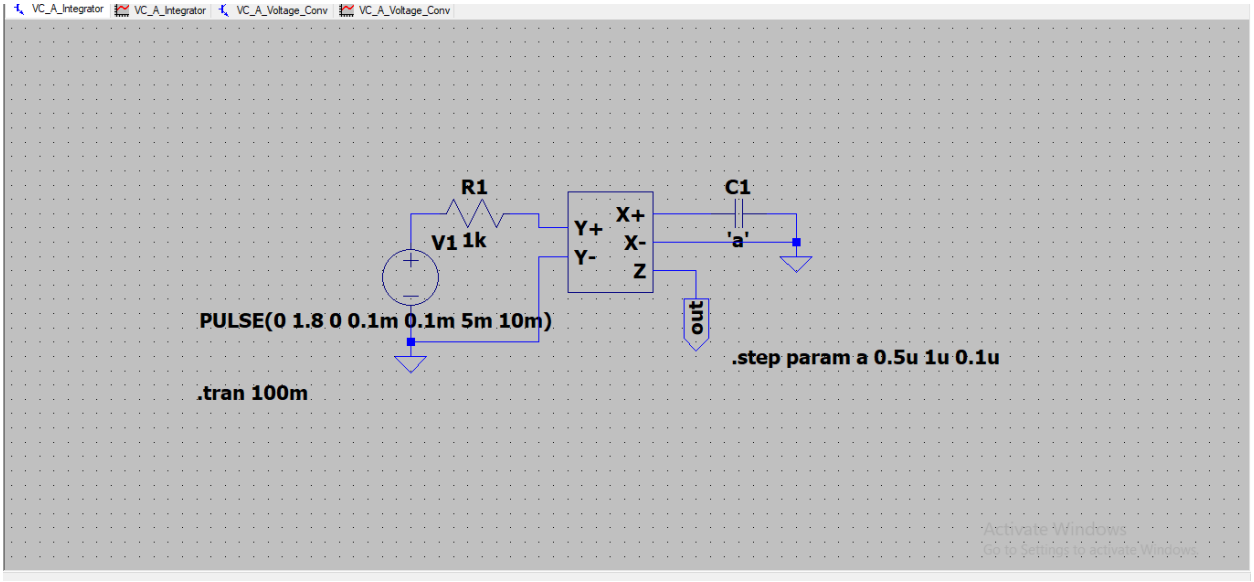

Figure 5.17: Circuit diagram of voltage integrator using proposed VCII block

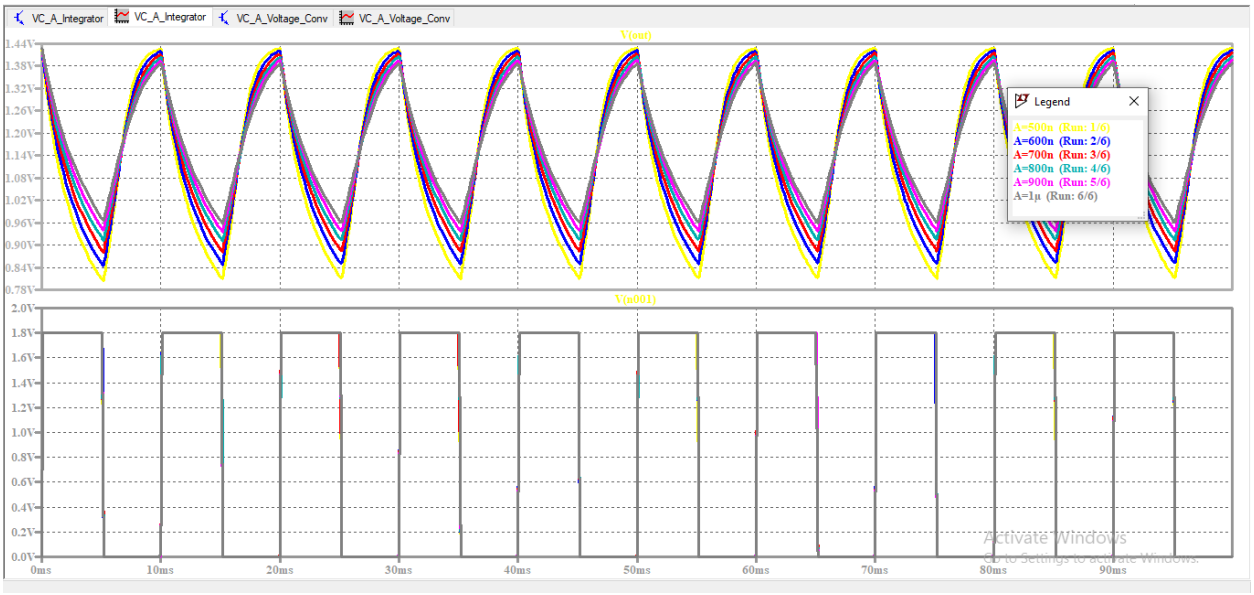

Figure 5.18: Transient analysis of voltage integrator implemented using VCII block

vi). Simulation of voltage buffer circuit using VCII block

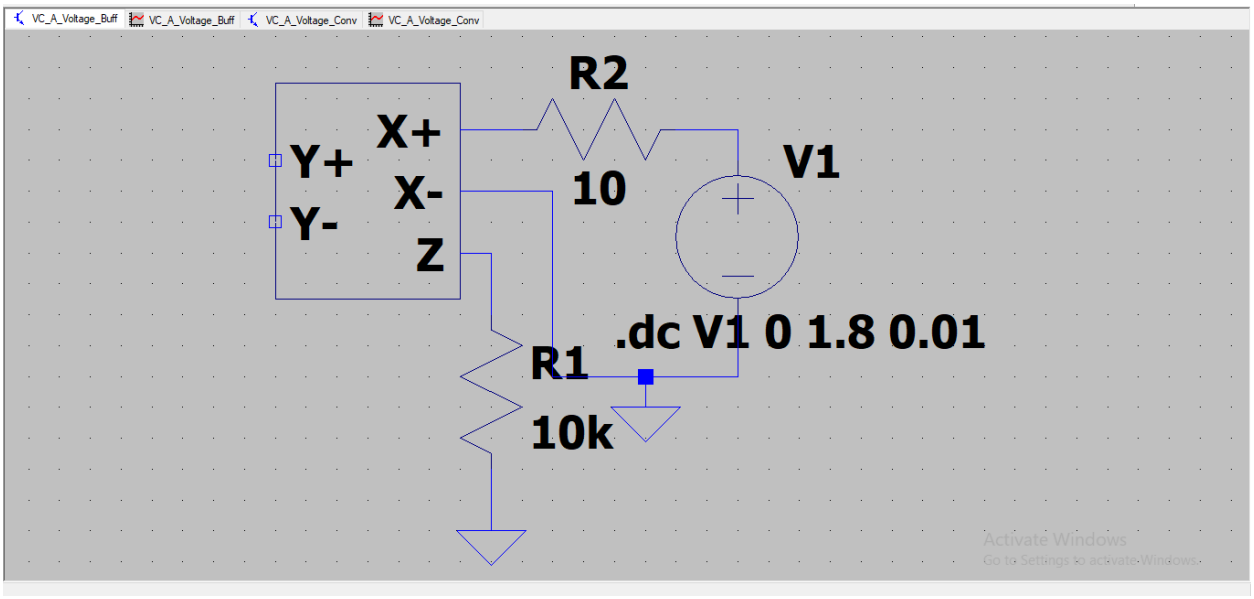

Figure 5.19: Circuit diagram of voltage buffer using proposed VCII block

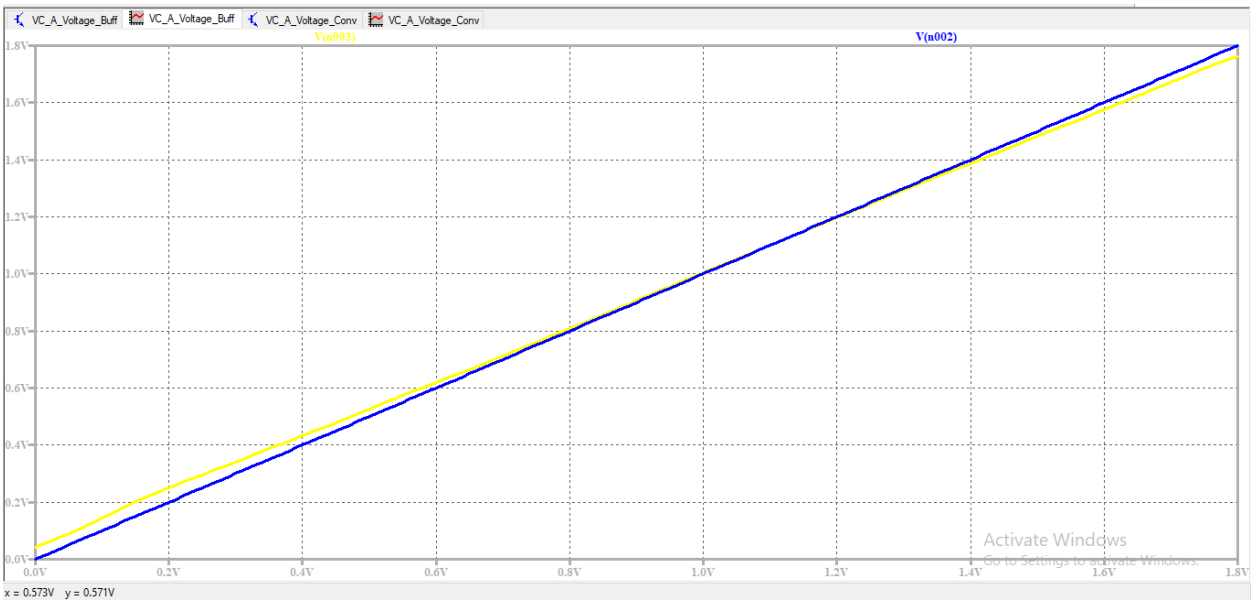

Figure 5.20: Plot of DC analysis performed for voltage buffer circuit

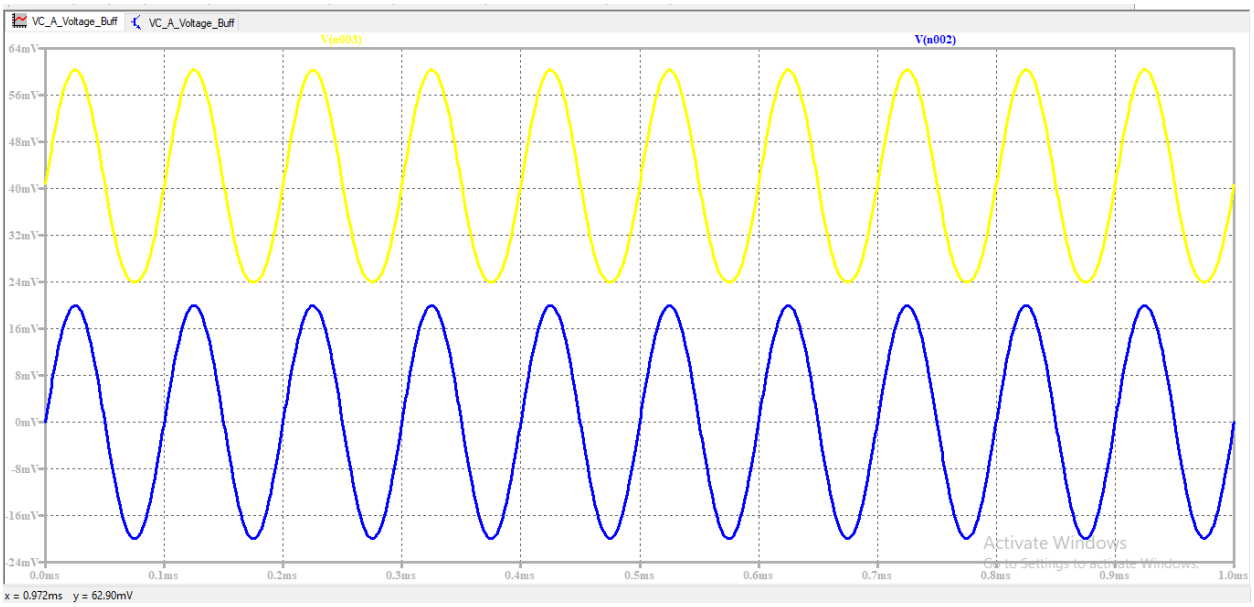

Figure 5.21: Plot of transient analysis performed for voltage buffer circuit

vii). Simulation of voltage to current converter circuit using VCII block

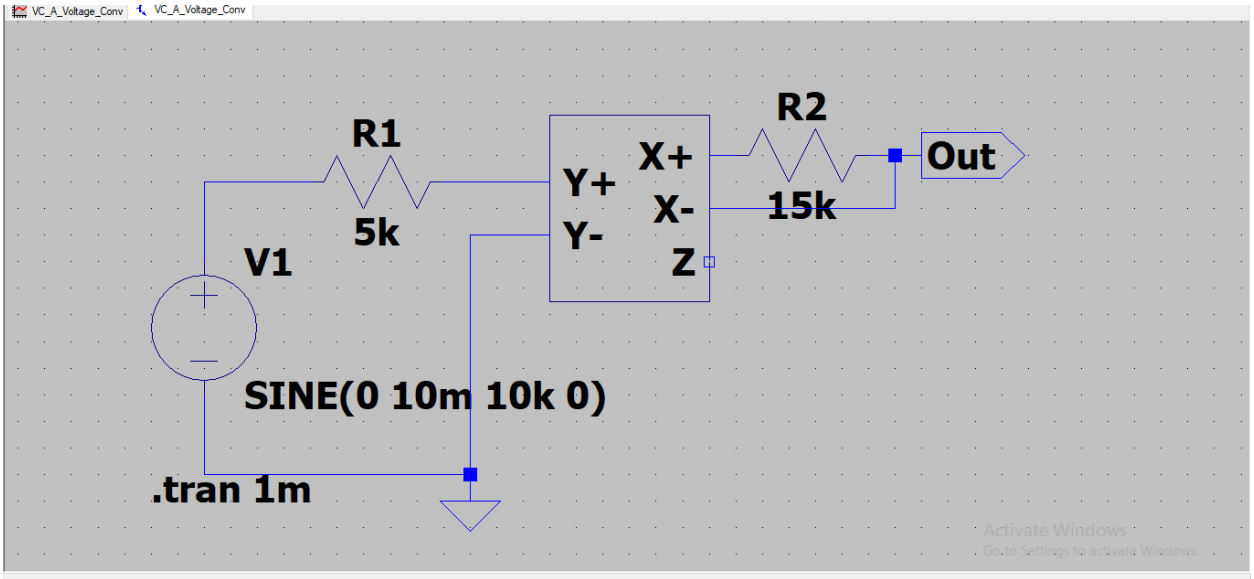

Figure 5.22: Circuit diagram of voltage to current converter using proposed VCII block

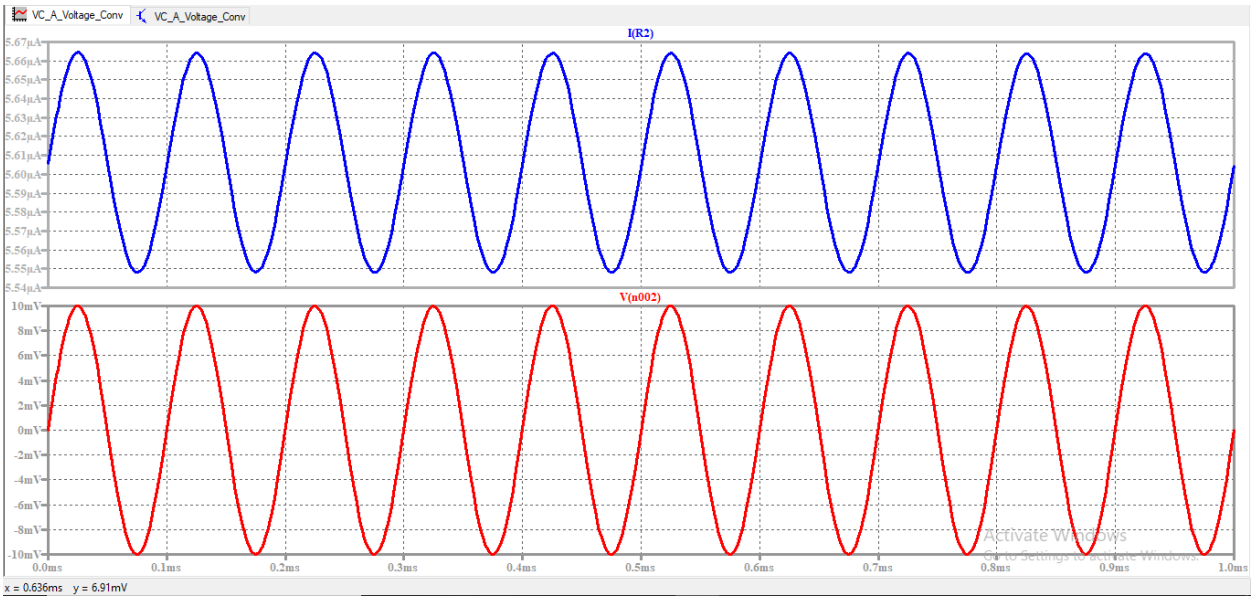

Figure 5.23: Plot of transient analysis of voltage to current converter

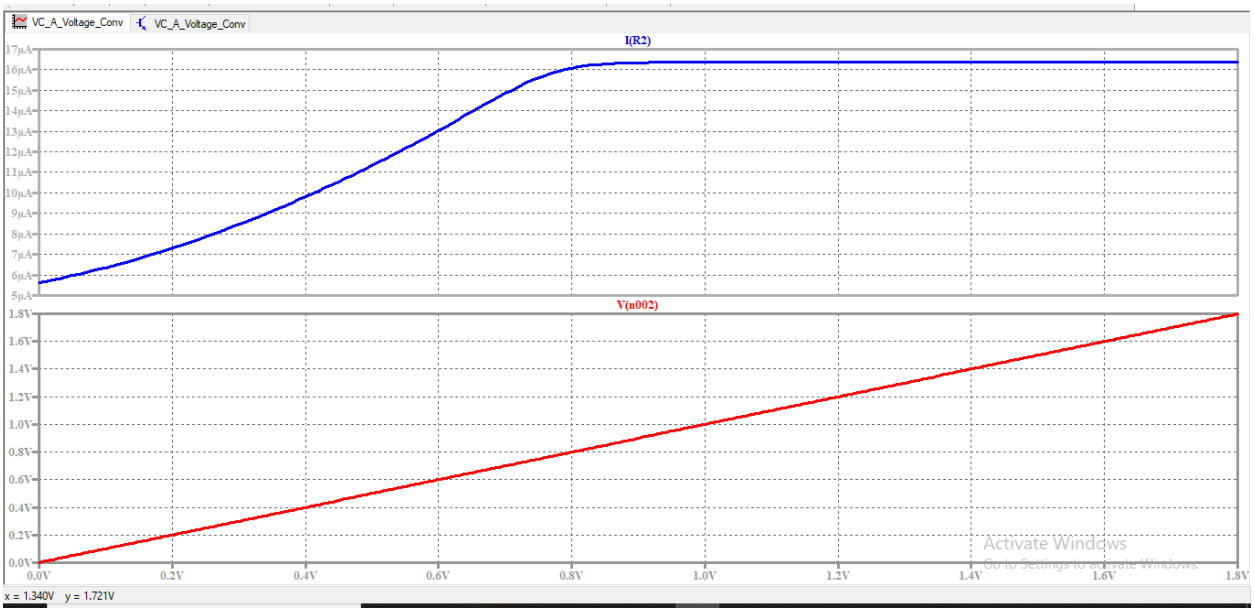

Figure 5.24: Plot of DC analysis of voltage to current converter

viii). Simulation of Band Pass filter using VCII Block

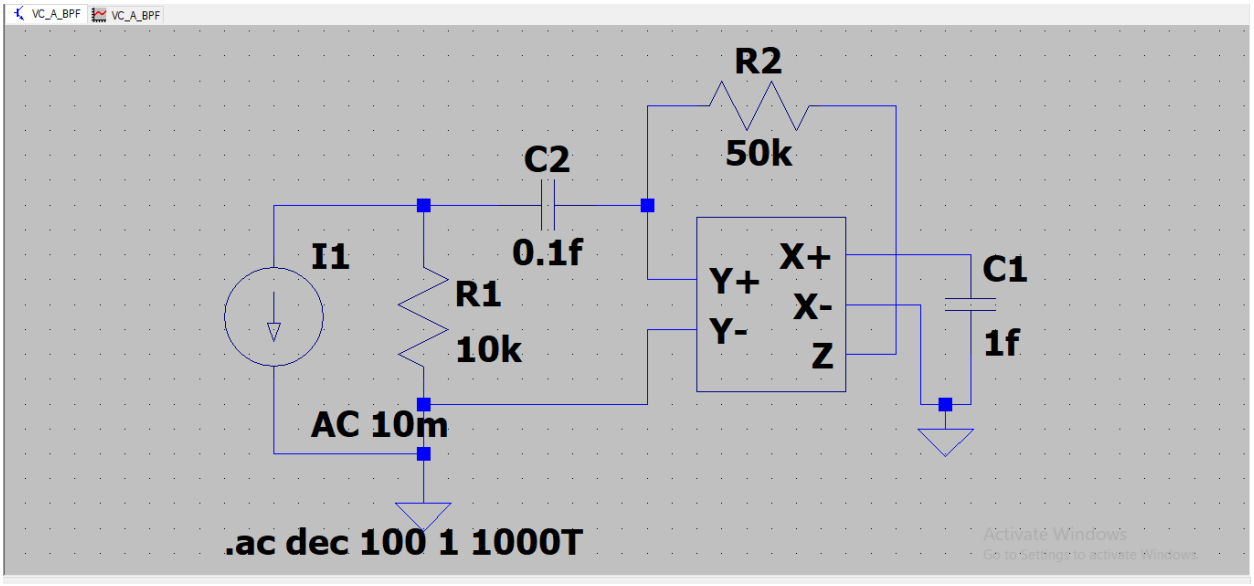

Figure 5.25: Circuit diagram of band pass filter using proposed VCII block

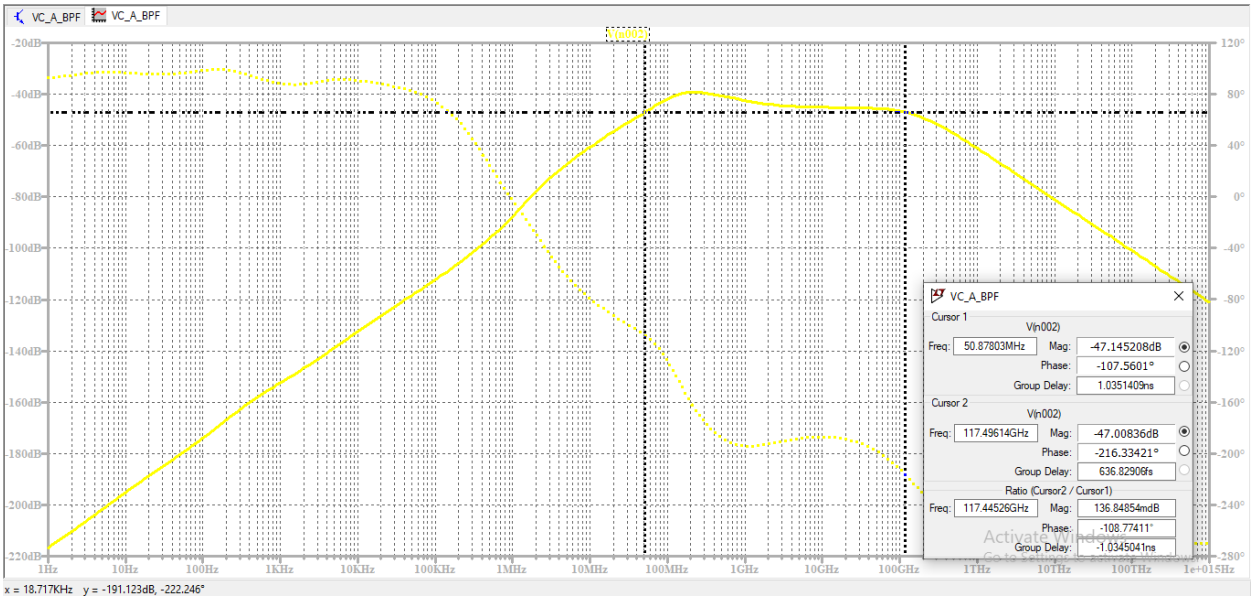

Figure 5.26: Plot of AC analysis of band pass filter

ix). Simulation of low Pass Filter using VCII Block

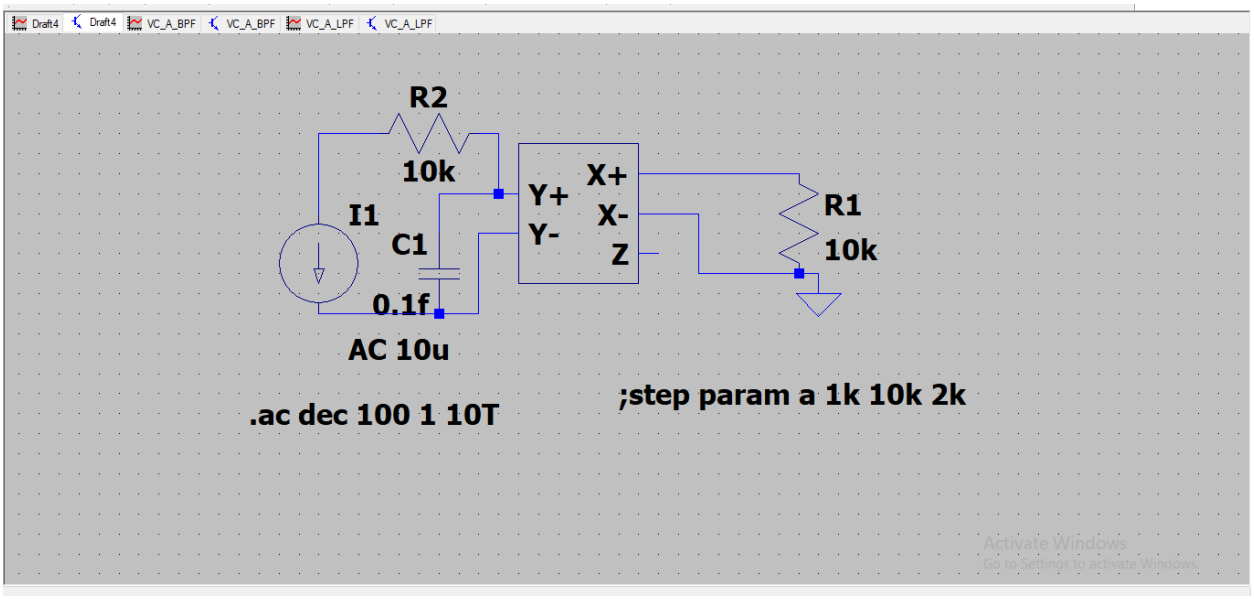

Figure 5.27: Circuit diagram of low pass filter using proposed VCII block

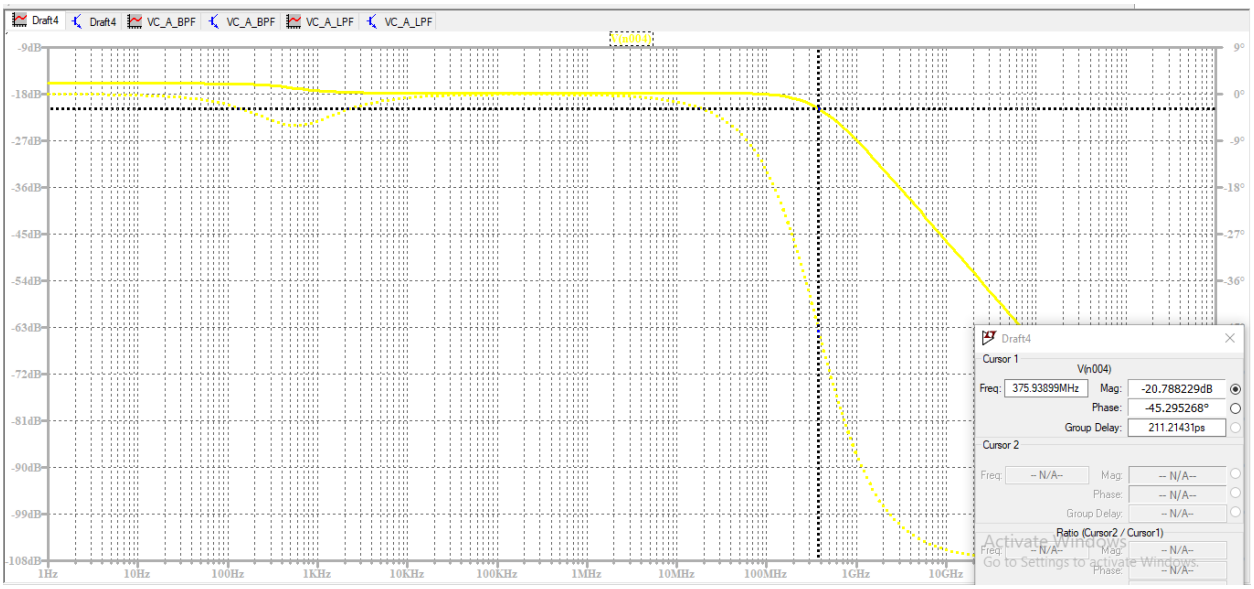

Figure 5.28: Plot of AC analysis of low pass filter

CHAPTER 6

LEARNINGS FROM PROJECT

In this chapter we have concluded our work, why VCII should be a preferable choice over CCII and Op-Amp. We have discussed about results and their significance, how these results are better in comparision to previously implemented technique and previously existing method to implement those applications.

Learnings from Project:-

On the basis of above discussion, results and literature I reviewed I can conclude following points:

i). VCII can provide the best answer to Op-Amp difficulties such as fixed slew rate, gain-bandwidth conflict, high power consumption, and a limited operational frequency range. The slew rate and gain bandwidth conflict can be resolved because VCII operates in an open loop arrangement. VCII has a basic and easy-to-build circuit, and in many applications where two stages of an op-amp block are required, VCII may perform those applications with a single block, saving power and space. For instance, a precise full wave rectifier, a wave form generator circuit, and a band pass filter are just a few examples.

ii). The VCII block has various current mode qualities, including a decreased node impedance and the ability to do current summing of signals due to its low input impedance. Because of the current mirror we employ in VCII, similar to CCII, current signal replication and scaling is simple. In comparison to op-amp, it also provides a wide bandwidth. VCII blocks utilise less electricity and take up less space due to their simple design. It has a greater switching speed, lower crosstalk, and lower switching noise.

iii). We have used class AB configuration which will result in low powerrequirement and higher efficiency. From the DC analysis simulation results we can conclude that β and α value for our proposed structure is almost equal to 1 since output voltage is following input voltage. Impedance of output is very low which implies we can drive multiple devices and using

cascaded state we can further improve in the results. We are getting very high input impedance which will help the device from self loading and to maintain the signal integrity.

iv). From the simulated results we can conclude that we achieving much higher bandwidth which further improve the device performance in high speed operaton. We achieved approx. 900 MHz cut off frequency for low pass filter and and approx. 34 GHz bandwidth for band pass filter which is much higher than op-amp designed filters.

v). For Voltage buffer and current buffer application our design is showing almost ideal behavior. From the power consumption graph we can see that power consumption is in range of n watt, which is much lower than existing designs and op-amp.

vi). For voltage mode operation VCII can provide a optimum solution since it consists of advantage of both CCII block and Op-Amp circuit.

vii). We have used differential current buffer stage and voltage buffer stage which provides higher higher CMRR and PSRR. Which provides higher immunity against the noise and signal interference.

REFRENCES

[1]. Mariusz Jankowski, Andrzej Napieralski, High-voltage SoI Unity-gain Voltage Buffers with Function-enable and Power-down Functionality, INTERNATIONAL JOURNAL OF MICROELECTRONICS AND COMPUTER SCIENCE, VOL. 4,NO. 1, 2013.

[2]. J. M. Carrillo, M. A. Domínguez, J. F. Duque-Carrillo, et.al. - Low-Voltage Wide-Swing Fully Differential CMOS Voltage Buffer, 2011 20th European conference on circuit theory and design (ECCTD)

[3]. Caffey Jindal, Rishikesh Pandey, A class-AB flipped voltage follower cell with high symmetrical slew rate and high current sourcing/sinking capability, DOI: 10.1002/cta.2782

[4]. Mariusz Jankowski , Andrzej Napieralski, High-voltage high input impedance unity-gain voltage buffer, Microelectronics Journal44(2013)576–585

[5]. Surat Wongfoo, Weerachai Naklo,et.al., A Simple Rail-to-Rail CMOS Voltage Follower, 1-4244-0549-1/06/$20.00 (2006) IEEE.

[6]. R.G. Carvajal,et.al., The flipped voltage follower: A useful cell for low-voltage low-power circuit Design, IEEE Transactions on · August 2005.

[7]. Hassan Broomandnia, Seyed Javad Azhari, Design of a Fully Differential Current Buffer (FDCB) based on a new Common Mode Feedforward (CMFF) based Common Mode Separation Technique, International journal of Mechatronics, Electrical and Computer Technology, Vol. 6(19), Jan. 2016, PP. 2749-2759

[8]. L. Safari, S.J. Azhari, -A New Low Voltage Low Power Fully Differential Current Buffer and its Application as a Voltage Amplifier, International Journal of Modeling and Optimization, Vol. 2, No. 3, June 2012.

[9]. Seyed javad azhari, et.al., A Novel Fully Differential Current Buffer with Ultra Low Input Impedance, High CMRR, Low power and Low voltage, 978-1-4244-8679-3/11/$26.00 ©2011 IEEE

[10]. S. J. Azhari, et.al., FULLY DIFFERENTIAL CURRENT BUFFERS BASED ON A NOVEL COMMON MODE SEPARATION TECHNIQUE, doi: 10.5829/idosi.ije.2011.24.03b.04, Vol. 24, No. 3, October 2011 – 237.

[11]. L. Safari, G. Barlie, et.al. ‒An Overview on the Second Generation Voltage Conveyor: Features, Design and Applications‖, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 66, NO. 4, APRIL 2019.

[12]. R. V. Yenkar, R. S. Pande, SS Limaye, ― Design and Implementation of Different Generations of Current Conveyor using 100nm CMOS Technology‖, International Journal of Recent Development in Engineering and Technology, Volume 2, Issue 3, March 2014.

[13]. Fabian Khateb, Nabhan Khatib, David Kubanek, ‒Low-Voltage Ultra-Low-Power Current Conveyor Based on Quasi-Floating Gate Transistors‖, RADIOENGINEERING, VOL. 21, NO. 2, JUNE 2012.

[14]. Soliman A. Mahmoud, New Fully-Differential CMOS Second-Generation Current Conveyer, ETRI Journal, Volume 28, Number 4, August 2006.

[15]. Gianluca Barile, Vincenzo Storneli, et.al., ‒A New Rail-to-Rail Second Generation Voltage Conveyor‖, MDPI, Electronics 2019, 8, 1292; doi:10.3390/electronics8111292.

[16]. L. Safari, G. Barile, et.al., An Overview on the Second Generation Voltage Conveyor: Features, Design and Applications, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: EXPRESS BRIEFS, VOL. 66, NO. 4, APRIL 2019.

[17]. Ankit Gupta, ―A Study on Current Conveyors and their Applications‖, Journal of Multi Disciplinary Engineering Technologies (JMDET) ISSN: 0974-1771.

[18]. Leila Safari, Vincenzo Starnelli, et.al. ,‖ High Performance Voltage Output filter Realization using voltage conveyor‖, International Journal of RF and Microwave Computer Aided Engineering, 2018; e21534.

[19]. Francesco Centurelli, Pasquale Tommasino, et.al., ―On the Use of Voltage Conveyors for the Synthesis of Biquad Filters and Arbitrary Networks‖, IEEE, 2017, 978-1-5386-3974-0/17/.

[20]. Josef Čajka, Kamil Vrba, ―The Voltage ConveyorMay Have in Fact Found its Way into Circuit Theory‖, Int. J. Electron. Commun. (AE¨U) 58 (2004): 244–248.

[21]. Jaroslav KOTON, Norbert Herencsar, Kamil Vrba, ‗‗Current and Voltage Conveyors in Currentand Voltage-Mode Precision Full-Wave Rectifiers‘‘, RADIOENGINEERING, VOL. 20, NO. 1, APRIL 2011.

[22]. Ramón González Carvajal, Jaime Ramírez-Angulo,et.al., ―The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design‖, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—I: REGULAR PAPERS, VOL. 52, NO. 7, JULY 2005.

[23]. J. Koton , K.Vrba, N. Herencsar, ―Tuneable filter using voltage conveyors and current active elements‖, International Journal of Electronics, 09 October 2014.

[24]. Jaroslav Koton, Aleksander Shadrin, ―Universal Voltage Conveyors in Fractional-Order Filter Design‖, IEEE, 2016, 978-1-5090-1288-6/16/.

[25]. Ramon Gonzalez, et.al. , - The Flipped Voltage Follower: A Useful Cell for Low-Voltage Low-Power Circuit Design, IEEE Transactions on Circuits and Systems-I: Regular Papers, Vol. 52 No. 7, July 2005.

[26]. Leila Safari, Seyed Javad Azhari, A Novel Low Input Impedance Low Power Fully Differential Current Buffer with ±0.65V Supply Voltage and high bandwidth of 520MHz, WSEAS TRANSACTIONS on CIRCUITS and SYSTEMS, Issue 8, Volume 11, August 2012.