DESIGNING OF 2:4 DECODER USING DIFFERENT LOGIC STYLES

A MAJOR PROJECT-2 REPORT

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OF

MASTER OF TECHNOLOGY
IN
VLSI DESIGN AND EMBEDDED SYSTEMS

Submitted by:

POORVA AGGARWAL
2K20/VLS/13

Under the supervision of

Dr. Sonal Singh

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, Poorva Aggarwal, Roll No. 2K20/VLS/13, student of M. Tech (VLSI and Embedded Systems), hereby declare that the major project-2 titled **"Designing of 2:4 decoder using different logic styles"** which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: Delhi **Poorva Aggarwal**

Date: **(2K20/VLS/13)**

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Major Project-2 Report titled **"Designing of 2:4 decoder using different logic styles"** which is submitted by **Poorva Aggarwal**, Roll No. **2K20/VLS/13** of Electronics and Communication Department, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision.

To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date:

Dr. Sonal Singh

SUPERVISOR

ACKNOWLEDGEMENT

A successful project can never be prepared by the efforts of the person to whom the project is assigned, but it also demands the help and guardianship of people who helped in completion of the project. I would like to thank all those people who have helped me in this research and inspired me during my study.

With profound sense of gratitude, I thank Dr. Sonal Singh, my Research Supervisor, for her encouragement, support, patience and guidance in this project work. I heartily appreciate the guidance given by her in the project presentation that has improved my presentation skills with her comments and advices. I take immense delight in extending my acknowledgement to my family and friends who have helped me throughout this project work.

POORVA AGGARWAL
Roll no: 2K20/VLS/13

ABSTRACT

Decoders are combinational circuits that convert binary information into 2N output lines. N input lines are used to transfer the binary information. The binary information is encoded in a 2N-bit code on the output lines. When the decoder is activated, one of these outputs will be active High dependent on the mix of inputs present. That is, the decoder recognises a certain code. When the decoder is activated, the decoder's outputs are nothing more than the min terms of 'n' input variable lines.

In this project, I have designed and implemented 2:4 decoder using different logic styles such as Complementary MOS (CMOS) Logic, Transmission Gate Logic (TGL) and Pass-transistor Dual Value Logic (PDVL) using LTspice software. I have also designed two modified circuits of 2:4 decoder using the same software. A comparative study of the five different circuits is represented based on their area (in terms of number of MOSFETs), average energy and propagation delay. Simulations are done at 1.8V for 180nm and 90nm technology nodes and at two different temperatures i.e. 27C and 120C.

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CHAPTER 1

INTRODUCTION

Every logic style has its own relevance and influence on VLSI circuit performance. Essentially, each VLSI circuit is developed with three goals in mind: to decrease propagation delay, reduce power consumption, and optimize layout area. The majority of battery-powered applications are concerned with ways to extend battery life. CMOS logic types, which dissipate relatively less power, might allow for such systems.

Most of logic gates in integrated circuits are developed utilising static CMOS circuits. A pMOS pull-up network and a nMOS pull-down network make up the Complementary Metal Oxide Semiconductor (CMOS) circuits, which have good performance against device variations and noise. CMOS circuits operate reliably at low voltages and smaller transistor sizes.

Inputs are applied to transistor gate terminals exclusively in CMOS circuits, resulting in fewer design variants and cell-based logic design and synthesis. The number of n-type and p-type MOSFETs in CMOS architectures is balanced. The input logic values are sent to MOSFET poly layers. CMOS logic has a high input impedance because of the oxide layer between the poly and channel of MOSFETs.

Universal gates, such as NAND and NOR gates, should ideally be designed using CMOS logic. Using CMOS logic, you'll need an extra inverter to obtain un-complemented/non-inverting output.

Pass Transistor Logic (PTL) was first proposed in the 1990s as an alternative to CMOS logic. In comparison to CMOS logic, pass transistor logic improves speed, power, and area. Pass transistor circuits are distinguished by the fact that inputs are

linked to the transistors' gate or source/drain diffusion terminals. Pass transistor circuits can be implemented in two different ways.

Individual pMOS or nMOS transistors are utilised in the first technique, but in the second way, pMOS and nMOS transistors are employed in a parallel combination termed a transmission gate.

Transmission Gate Logic(TGL), on the other hand, may solve this issue. The TGL requires a pair of n-type and p-type MOSFETs with the source and drain terminals short-circuited. Because the transmission gates are bidirectional, input can be applied to either the short circuited source or drain terminals. TGL is a type of logic that differs from CMOS logic.

When compared to CMOS logic, Double Pass-transistor Logic (DPL) can simply and effectively achieve AND/OR logic. The use of DPL to provide noninverting output necessitates fewer MOSFETs.

TGL introduces the Adapting Transmission Gates (TG) idea, which enhances the full swing of the output signal as well as the noise margin. For certain of the specific input combinations, TGL is slower in restoring the output charge/voltage. PDVL is a third alternative logic that can create full-swing output voltage and quick charge/voltage restoration at the output node.

In the case of PDVL, switching speed, i.e., charging and discharging of voltage at the output node, is enhanced. In conventional Pass Transistor Logic there is a single channel for charging and discharging, whereas PDVL introduces a distinct discharging path. As a result, the switching speed is increased.

In comparison to other logic approaches, PDVL requires fewer MOS devices. The PDVL design layouts can be enhanced. As a result, low-power devices are becoming increasingly important in the semiconductor industry. Simultaneously, we must minimize the devices' critical path delay while minimizing their power.

Benefits of optimization are: -

- Less Delay
- Less Power Consumption
- Less Area Consumption
- Less Complexity
- Reduced Cost
- High throughput

Rapid advancements in VLSI technology, such as downsizing and voltage scaling, have necessitated the development of low-power, high-speed, and energy-efficient logic devices. In high-performance computing systems such as microprocessors and digital signal processors, low-power design is a key concern.

A decoder is a basic combinational circuit that takes an input code and turns it to a series of output signals. Line decoders are used in a broad range of applications, including memory array address decoding, data demultiplexing, seven-segment displays, and microchip/microcontroller-based frameworks.

Address decoders are crucial in SRAM memory blocks since the power consumption and access time are substantially determined by the decoder design. The goal of this project is to provide a novel mixed logic technique for creating decoders that minimises average energy, delay, and transistor count.

1.1 SOFTWARE: LTspice

LTspice is a SPICE-based analog electrical circuit simulator computer software developed by Analog Devices, a semiconductor company (originally by

Linear Technology). It is the industry's most extensively distributed and utilized SPICE software.

LTspice is not purposely constrained to limit its possibilities, even if it is free (no feature limits, no node limits, no component limits, no sub circuit limits). LTspice includes a schematic capture tool for entering an electronic circuit's electronic schematic, an upgraded SPICE analog electronic circuit simulator, and a waveform viewer for viewing the simulation's results.

Circuit simulation analysis using transients, noise, AC, DC, DC transfer function, and DC operating point, as well as Fourier analysis, may be conducted and plotted. Component's heat dissipation may be evaluated, and efficiency reports can be produced. It has been updated with new features and specific models to make simulation of switched-mode power supply (SMPS) in DC-to-DC converters quicker.

Although LTspice does not produce printed circuit board (PCB) layouts, it may export netlists to PCB layout tools. While LTspice can simulate simple logic gates, it isn't intended to be used to simulate logic circuits. Many people utilize it in domains including radio frequency electronics, power electronics, audio electronics, digital electronics, and many others.

Many of the LTspice files are saved as ASCII text files that may be viewed or modified with any ASCII text editor. One of the advantages of an ASCII file format is that it allows a schematic to be included in a printed document, book, magazine, datasheet, research paper, or homework assignment, allowing the reader to reproduce LTspice files without having to download them.

LTspice filename extensions:

- asc - schematic. It consists of a netlist based on SPICE text-based commands.

- `asy` - electronic symbol shown in a schematic.
- `cir` - external netlist input.
- `fft` - FFT binary output.
- `lib` - model library subcircuits.
- `plt` - waveform viewer plot settings.
- `raw` - binary output, optional ASCII output.
- `sub` - subcircuit.
- `lib` / `sub` / `mod` / `model` - device model. While any file extension is allowed, users tend to gravitate towards common ones.

1.2 MOSFET

The metal oxide semiconductor field-effect transistor (MOSFET) is a form of insulated-gate field-effect transistor constructed by controlled oxidation of a semiconductor, generally silicon. The electrical conductivity of a device is controlled by the voltage supplied to the gate terminal; this capability to modify conductivity with the amount of applied voltage may be utilised to amplify or switch electronic signals.

When compared to bipolar junction transistors(BJTs), a MOSFET has the benefit of requiring nearly zero input current to manage the load current. When a voltage is supplied to the gate terminal of an enhancement mode MOSFET, the conductivity can be increased from the "normally off" condition. The conductivity of a depletion mode MOSFET can be reduced from the "normally on" condition by applying voltage to the gate.

MOSFETs have a high scalability and can be readily scaled down to smaller dimensions as downsizing progresses. In comparison to BJTs, they offer a higher

switching speed (perfect for digital signals), are considerably smaller, require substantially less power, and allow much higher density (excellent for large-scale integration). MOSFETs are also less expensive and have fewer processing stages, which results in a higher production yield.

1.2.1 MOSFET CONSTRUCTION

Two severely doped p+ areas diffused into a weakly doped n- material termed the well constitute the p-channel device. Drain and source are the two p+ areas that are separated by a distance L. (referred to as the device length). A gate electrode is located between the drain and source and is separated from the silicon by a thin dielectric layer (silicon dioxide). Similarly, two severely doped n+ areas within a weakly doped p-substrate create the n-channel transistor. It, too, has a gate on the surface between the drain and source, which is separated from the die silicon by a thin dielectric (silicon dioxide).

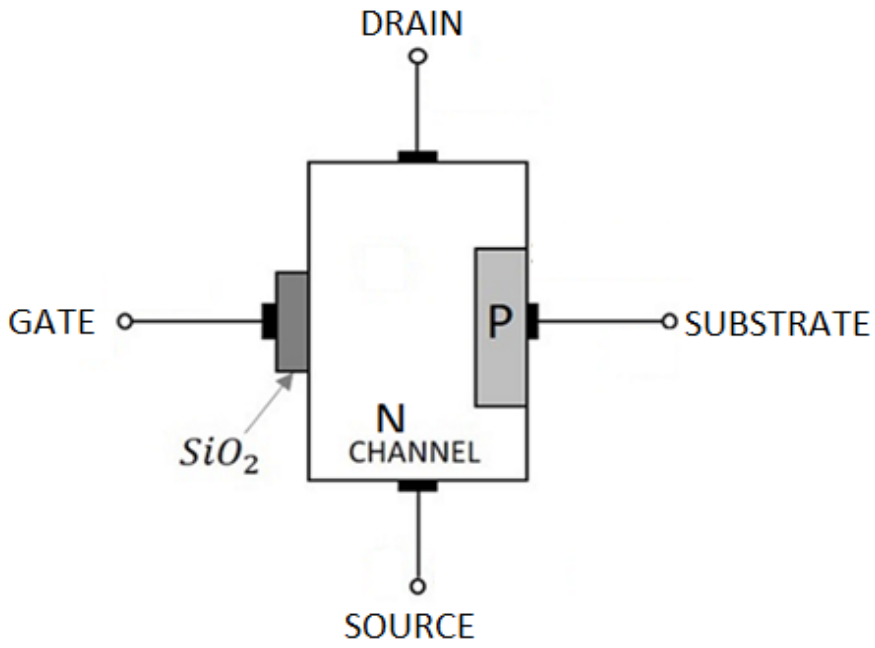

Fig. 1.1 Construction of a mosfet

1.2.2 MOSFET TYPES

The classification of MOSFET based on the construction and the material used is given below in the flowchart.

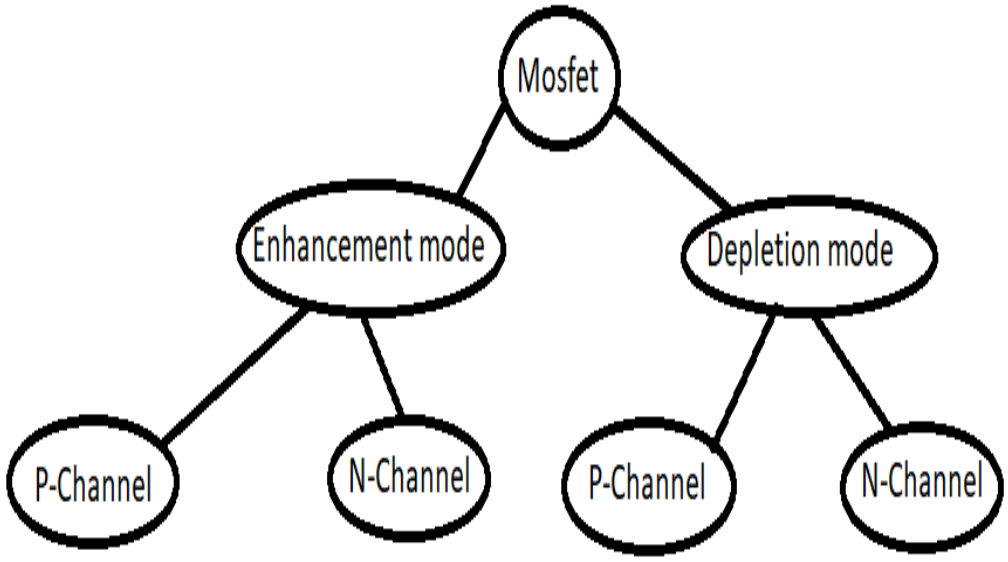

Fig. 1.2 Types of mosfet

Depletion Mode- The channel has the highest conductivity when no voltage is applied at the gate terminal. The channel conductivity reduces when a positive or negative voltage is applied at the gate terminal.

Enhancement Mode- The transistor does not conduct if no voltage is applied at the gate terminal. When the maximum voltage is applied at the gate terminal, the device's conductivity improves.

1.2.3 MOSFET WORKING PRINCIPLE

A pn junction is formed when the p- substrate and the n + source and drain are in equilibrium. As a result, between the n+ source and drain and the p- substrate, a depletion area exists. The resistance between the source and drain is extremely high (>10^12 ohm) because the source and drain are separated by back-to-back pn junctions.

The MOS transistor's gate and substrate serve as the parallel plates of a capacitor, with SiO2 serving as the dielectric. The Cox factor is calculated by dividing the capacitance by the gate area. When a positive potential is supplied to the gate in relation to the source, boles are pushed away from the silicon-silicon dioxide contact, forming a depletion area under the gate. Fixed ions with a negative charge make up the depletion area.

The substrate behind the gate gets inverted, or transforms from a p-type to an n-type semiconductor, when the gate voltage reaches a value known as the threshold voltage, indicated as Vt. As a result, between the source and the drain, an n-type channel exists that permits carriers to pass. The surface potential must be increased from its original negative value to zero and subsequently to a positive value in order to achieve this inversion. The threshold voltage, Vt, is the value of gate-source voltage required to generate this shift in surface potential. Strong inversion is the term for this situation.

The threshold for an n-channel transistor can be made negative by implanting opposing impurities in the channel area of the substrate. For zero values of the gate-source voltage, this type of transistor is known as a depletion transistor, and current can flow between the drain and source.

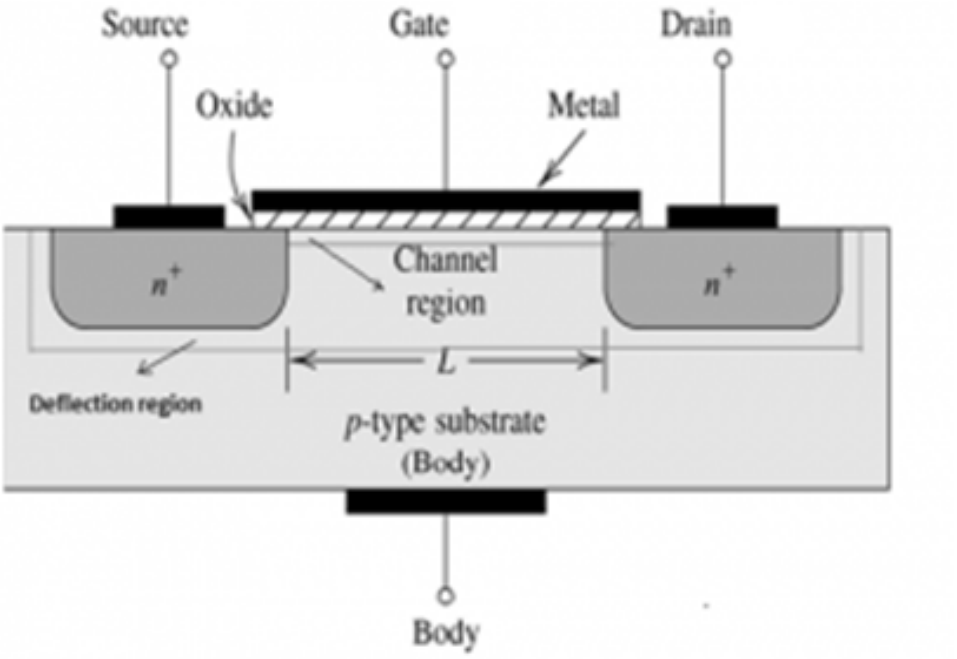

Fig. 1.3 Mosfet block diagram

1.2.4 MOSFET OPERATING REGIONS

Three operating regions may be recognized in a MOSFET. We'll talk about those regions here.

1. Cut-Off Region- The cut-off region is a region where no conduction occurs, and so the MOSFET is turned off. MOSFET functions as an open switch in this situation.

2. Ohmic Region- The ohmic region is defined as a region where the current (IDS) rises as the value of VDS rises. MOSFETs are employed as amplifiers when they are designed to function in this range.

3. Saturation Region- The MOSFETs' IDS remains constant despite a rise in VDS in the saturation region, which happens when VDS surpasses the pinch-off voltage VP. In this case, the device will operate as a closed switch, allowing a saturated value of IDS to pass through it. As a result, anytime MOSFETs are required to execute switching operations, this operating region is selected.

1.2.5 MOSFET APPLICATIONS

• MOSFET amplifiers are widely used in radiofrequency applications.

• A MOSFET is a passive circuit component.

• DC motors may be regulated using power MOSFETs.

• MOSFETs are employed in the chopper circuit design.

1.2.6 MOSFET ADVANTAGES

- At lower voltages, MOSFETs have a higher efficiency.
- When there is no gate current, the input impedance is large, resulting in a high switching speed.
- These devices can run on very little energy and draw very little current.

1.2.7 MOSFET DISADVANTAGES

- Because of the thin oxide layer, MOSFETs are sensitive to damage by electrostatic charges.
- MOSFETs become unstable when they are overloaded with voltage.

1.3 CMOS

MOS Field Effect Transistor (MOSFET) is the most basic component in MOS and CMOS digital integrated circuits. In practically all digital circuit applications, the nMOS transistor is employed as the principal switching device, although in CMOS circuits, the pMOS transistor is generally used in combination with the nMOS device.

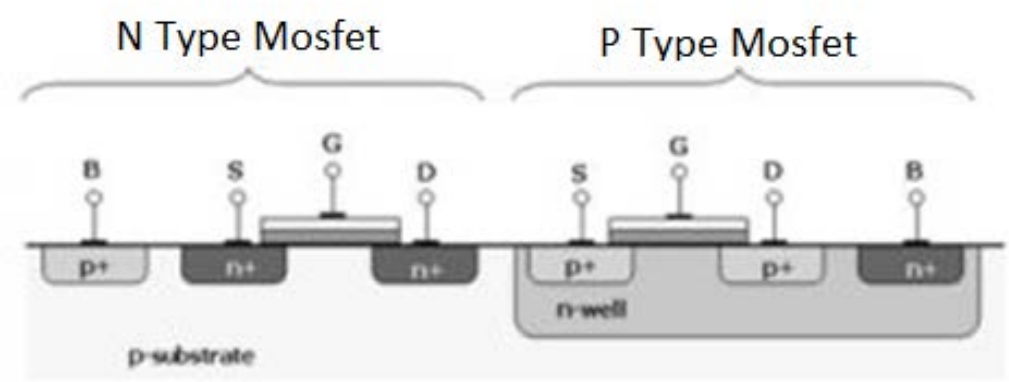

Fig. 1.4 CMOS construction

In comparison to conventional inverter architectures, the CMOS inverter offers two significant benefits. The first and possibly most important advantage is that, except for modest power dissipation owing to leakage currents, the CMOS inverter circuit's steady-state power dissipation is almost low.

When the driver transistor is turned on in all other inverter topologies studied thus far, a non-zero steady-state current is obtained from the power supply, resulting in considerable DC power consumption. The voltage transfer characteristic (VTC) of the CMOS arrangement also displays a complete output voltage swing between 0 V and VDD, and the VTC transition is generally fairly abrupt. As a result, the CMOS inverter's VTC is similar to that of an ideal inverter.

The CMOS method is more complicated than the typical nMOS-only technique since nMOS and pMOS transistors must be produced side by side on the same chip. An n-type substrate for pMOS transistors and a p-type substrate for nMOS transistors must be provided by the CMOS process.

1.3.1 CMOS WORKING PRINCIPLE

For decades, Poly-Si has been employed as the MOSFET gate material. Poly-Si gate technology concerns like as gate depletion and boron penetration become increasingly significant when CMOS devices scale down to the sub-100 nm region.

A pull-down network of n-type MOSFETs is positioned between the output and the low voltage power supply rail (Vss or quite often ground) in CMOS logic gates.

Furthermore, a number of high-k gate-dielectric possibilities have been claimed to be incompatible with poly-Si. As a result, metal gate technology for sub-100nm CMOS devices has been presented.

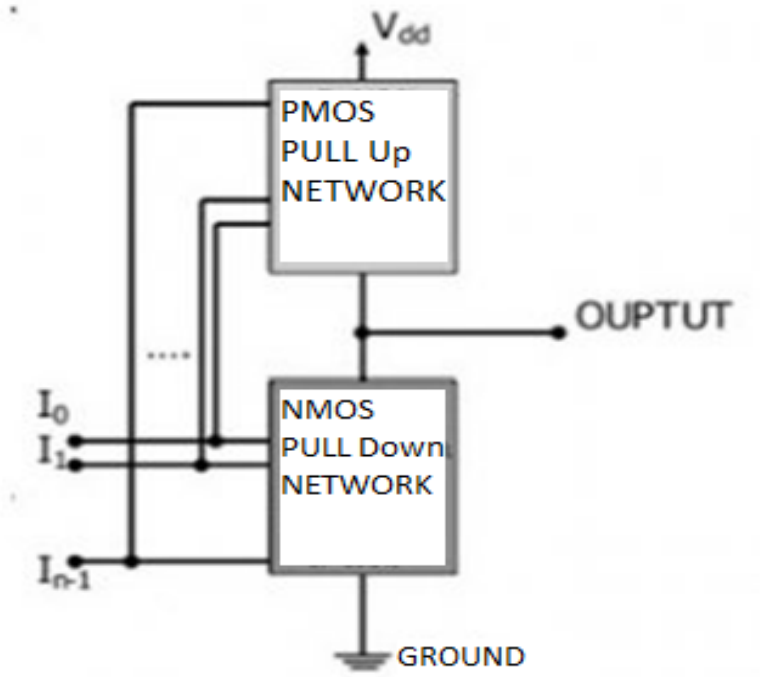

Fig. 1.5 CMOS using pull up and pull down

As a result, if the gates of both a p-type and an n-type transistor are attached to the same input, the p-type MOSFET will be ON while the n-type MOSFET is OFF, and vice versa. For every input pattern, one network is turned on and the other is turned off. In both stages, CMOS has a fast speed, low power dissipation, and large noise margins, and it can function over a broad range of source and input voltages (provided the source voltage is fixed).

1.4 TRANSMISSION GATE

A control signal with practically any voltage potential equivalent to that of a relay can cause a transmission gate to conduct in both directions or to block. It's a CMOS switch with PMOS passing a strong 1 but a weak 0 and NMOS passing a strong 0 but a bad 1. Both PMOS and NMOS are active at the same time.

1.4.1 TRANSMISSION GATE WORKING PRINCIPLE

In concept, a transmission gate made consisting of two field effect transistors in which the substrate terminal (Bulk) is not linked internally to the source terminal, unlike standard discrete field effect transistors.

The two transistors, an n-channel MOSFET and a p-channel MOSFET, are linked in parallel, but only their drain and source terminals are connected. To produce the control terminal, their gate terminals are linked to each other via a NOT gate (inverter). The substrate terminal is linked to the source connection, much as discrete transistors, resulting in a transistor to the parallel diode (body diode) that passes backwards.

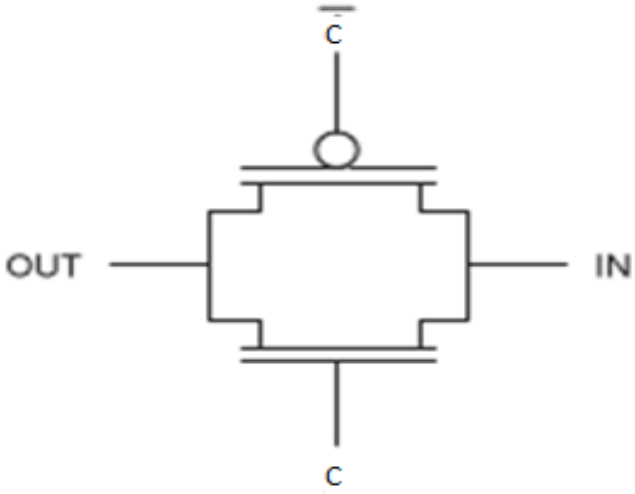

Fig. 1.6 TG schematic

The substrate terminals are linked to the relevant supply voltage potential to guarantee that the substrate diode is always operated in the reverse direction, since a transmission gate must block flow in both directions. The p-channel MOSFET's substrate terminal is therefore linked to the positive supply voltage potential, while the

n-channel MOSFET's substrate terminal is connected to the negative supply voltage potential.

The gate-source voltage of n-channel MOSFETs is always negative, whereas the gate-source voltage of p-channel MOSFETs is always positive, regardless of which switching terminal of the transmission gate (A or B) a voltage is applied (within the permitted range). As a result, none of the two transistors will current, and the transmission gate will be disabled.

The gate terminal of the n-channel MOSFETs is situated at a positive supply voltage potential when the control input is a logic one. The gate terminal of the p-channel MOSFETs is now at a negative supply voltage potential thanks to the inverter.

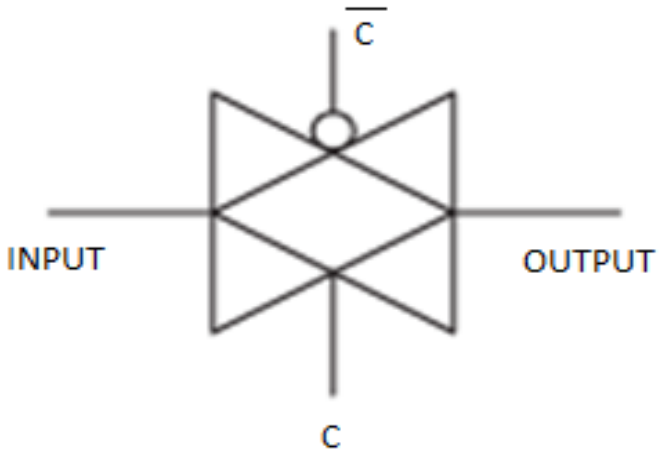

Fig. 1.7 TG symbol

The drain and source terminals are almost identical since the transistors' substrate terminal is not linked to the source terminal, and the transistors begin at a voltage differential between the gate terminal and one of these conducts.

Instead of using typical CMOS pull-up and pull-down networks, transmission gates can be used to build logic circuits. Such circuits may frequently be made smaller, which is a key concern in silicon implementations. They can selectively prohibit

essential signals or data from being transferred without adequate hardware-controlled authorisation in a security application.

1.5 PASS TRANSISTOR

Low transistor count and low power dissipation are achieved via Pass Transistor Logic (PTL). The fundamental disadvantage of PTL is the loss of threshold voltage. As a result, PTL may be used to build any digital circuit when the influence of threshold voltage loss is minimal.

Furthermore, shorter connection lengths and fewer transistors reduce fabrication costs. Furthermore, in pass transistor logic implementation, manufacturing procedures and resources are reduced/consumed less. As a consequence of the findings in both architectures, it can be concluded that pass transistor design is more area efficient than traditional CMOS architecture.

The benefit of PTL is that it is best suited for implementing power reduction approaches since it can minimise switching activity in the circuit by minimising glitches. This is accomplished by adjusting the delays of each pass transistor (controlling the widths and lengths). To achieve acceptable performance, circuit simulation may be needed.

1.5.1 PASS TRANSISTOR WORKING PRINCIPLE

A single NMOS transistor can be used as a PTL switch; when the voltage supplied to the gate is logic high, the switch is closed; when the voltage applied to the gate is logic low, the switch is open.

The AND function is implemented in the diagram below using just NMOS pass transistors. If the B input is high, the left NMOS in this gate is turned on, copying the input A to the output Y. When B is low, the right NMOS pass transistor is turned on, and the output Y receives a '0'.

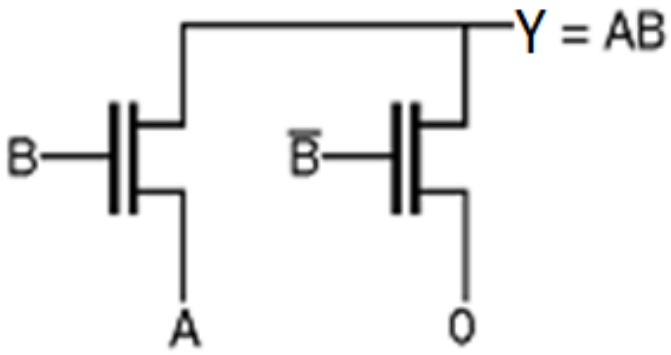

Fig. 1.8 AND gate using pass transistor

The main benefit of pass transistor logic is that it requires fewer transistors to accomplish a given function. Consider the implementation of an AND gate using complementary CMOS logic as an example. When we compare this to the similar AND gate solution utilizing pass transistor logic, we see that we need four transistors, including the two needed to invert the input B.

Another feature of pass transistor logic is that it has a lower capacitance due to the fewer number of transistors. As previously mentioned, NMOS devices are good at passing strong '0' but not so good at pulling a node to VDD. As a result, when a node is pulled to high logic by the pass transistor, the output merely changes to VDD–VTh. The main drawback of pass transistors is this.

1.6 2:4 DECODER

The reverse action of an encoder with 'n' input lines and 2n output lines is performed by a decoder. If it is active high, only one of the output lines will be 1 (high), while the other output lines will be 0 (low). If it is active low, only one of the output lines will be 1 (low).

The appropriate control signal is activated when the encoded signal takes on a specific code value. A decoder is a circuit that generates control signals in this manner. If every code word in an n-bit code is legitimate, the decoder will have 2n outputs. Decoders are a crucial component of memory architecture.

By looking at the appropriate code word, we may construct the Boolean equation for each decoder output. Consider the following scenario: we have a 4-bit encoded input signal (a3, a2, a1, a0), and we need to find the Boolean equation for the output corresponding to the code word 1011. When a3=1, a2=0, a1=1 and a0=1, the outcome is 1.

Other outputs are subject to the same reasoning. Each is the logical AND of the input bits, either directly (for bits that are 1 in the corresponding code word) or negated (for bits that are 0 in the corresponding code word) (for bits that are 1 in the corresponding code word).

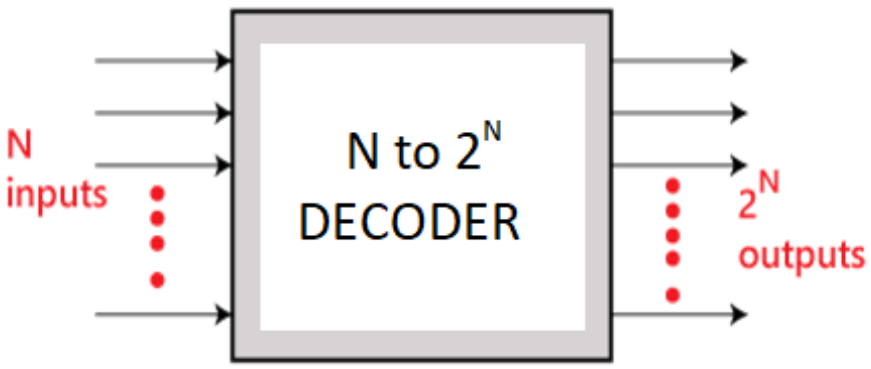

Fig. 1.9 Block diagram of decoder [1]

There are three inputs (A, B, and E) and four outputs (I0, I1, I2, and I3) in the 2:4 line decoder. When the enable 'E' is set to 1, one of these four outputs will be 1 for each combination of inputs.

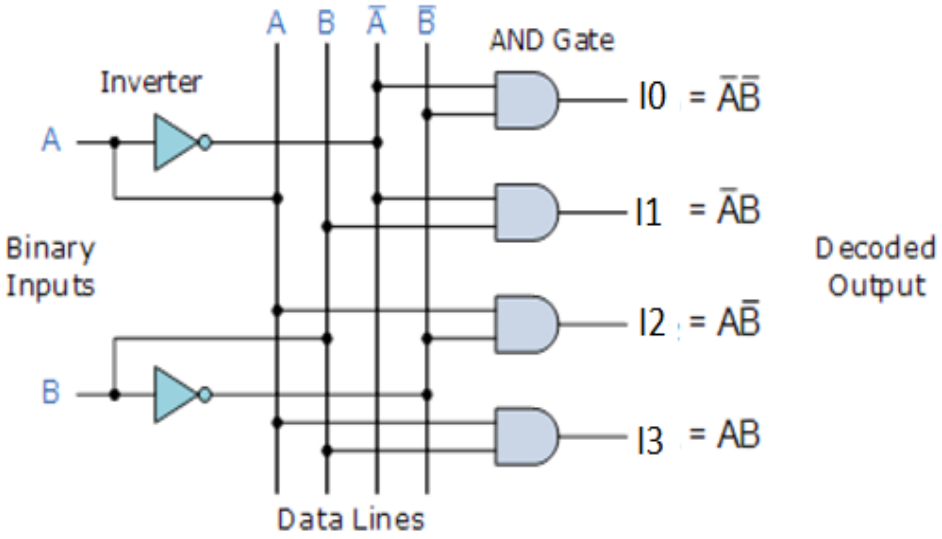

Fig. 1.10 Circuit diagram of 2:4 decoder

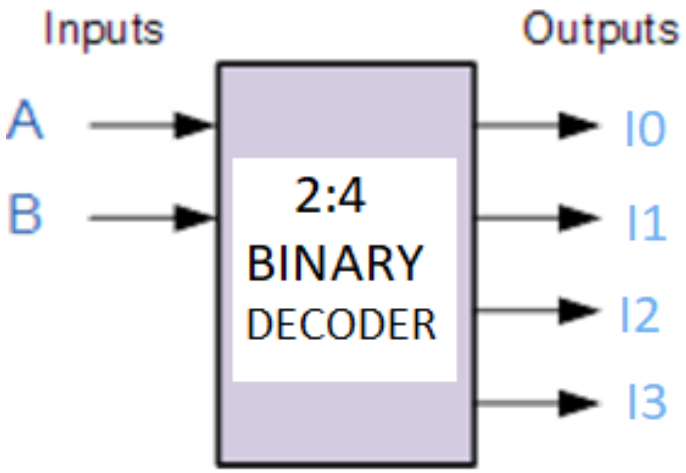

Fig. 1.11 Block diagram of 2:4 decoder [1]

Table 1.1 Truth table of 2:4 decoder

A	**B**	**I0**	**I1**	**I2**	**I3**
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

An array of four AND gates is used in the above simple example of a 2-to-4 line binary decoder. One-hot encoding refers to a k-bit binary code in which exactly one of the bits is set to 1 at a time, with the single bit that is set to 1 being considered "hot." An activated binary decoder's outputs are one-hot encoded.

The binary inputs A and B select which of the output lines from I0 to I3 is "HIGH" at logic level "1," while the remaining outputs are "LOW" at logic level "0," allowing just one output to be active (HIGH) at any given moment. As a result, whatever output line is marked "HIGH" identifies the binary code present at the input, or "decodes" the binary input.

1.6.1 DECODER APPLICATIONS

- Code converters
- A computer's memory system that allows it to access a specific memory region depending on the address generated by a computing device.
- To activate the control lines in the CPU's Arithmetic Logic Unit, decoders decode the instruction set.

CHAPTER 2

LOGIC STYLES

2.1 CMOS LOGIC STYLE

Two inputs and four outputs make up a 2-4 line decoder. For Active High Output (AHO) decoders, only one of the outputs is high and the rest are low for each feasible input. For Active Low Output (ALO) decoders, the situation is reversed. Multiplexers are constructed using AHO decoders. An ALO decoder is required for a conventional Static RAM configuration. CMOS logic is used to construct both kinds of decoders.

According to the report, CMOS logic produces complemented outputs and is employed to build universal gates such as NAND and NOR gates. The AHO kind of decoder is used as an example in this short. CMOS logic is used to construct a 2-4 AHO decoder. The pull-up network is made up of P-MOSFETs, whereas the pull-down network is made up of n-MOSFETs. Because all inputs are transmitted through MOSFET gate terminals, CMOS logic has a high input impedance.

In all logic designs, MOSFETs are used as switches. When the logic '1' input is applied to the gate of an n-MOS, it functions as a closed switch with the status "ON." When the same logic '1' is applied to the p-MOS, it functions as an open switch in the "OFF" state. If a logic '0' input is provided to the gate terminal of an n-MOS, it will be in the "OFF" state. When an input logic of '0' is provided, p-MOS stays in the "ON" state.

The state of eight n-MOSFETs and eight p-MOSFETs is determined using this approach, as illustrated in Table 2.1. Monotonic gates, such as NAND/NOR gates, are

best designed using CMOS logic designs. Using NOR gates, a 2-4 decoder is developed, resulting in an AHO type decoder, as shown in Fig.2.1. As shown in Fig.2.1, with inputs A and B and outputs I0, I1, I2, and I3.

Low static power dissipation and high supply voltage stability are two advantages of CMOS devices. These circuits have large noise margins and are not affected by transistor size. Ratio-less logics are another term for CMOS systems. However, it is recommended that the aspect ratio of a p-MOS transistor be 1.5 times that of an n-MOS transistor.

To get a high-performance gate, this ratio must be maintained. Even when the supply voltage is lowered, the CMOS design generates allowed output voltage values. CMOS circuits have a straightforward layout architecture that may be made very small. In an n-Well, the p- MOS devices are arranged. The n-type and p-type devices are separated by a demarcation line. During the manufacturing process, more compactness can be achieved.

In comparison to other logic designs, this logic has a high density of devices. However, CMOS gates will have a limited driving capability. Additional buffers or inverters are needed to increase the voltage to a level that is almost identical to the source voltage.

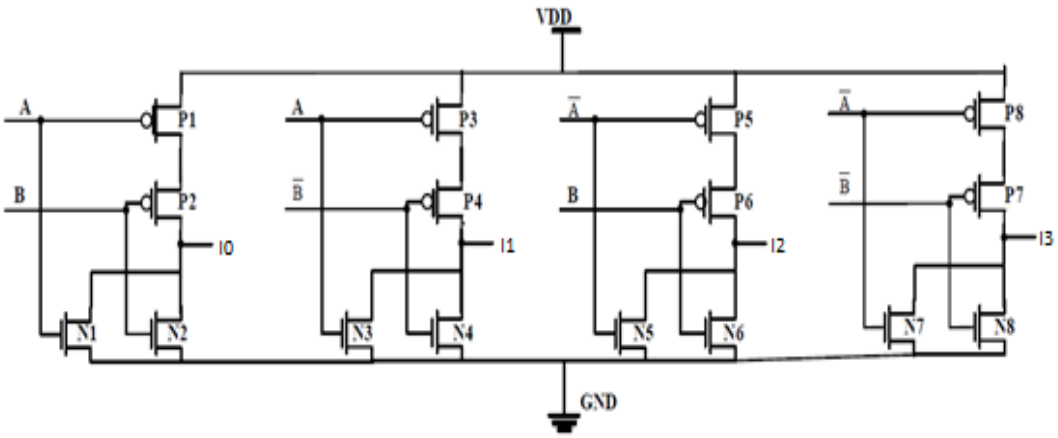

Fig. 2.1 2:4 decoder in CMOS logic style

Table 2.1 Functional table of CMOS 2:4 decoder

A	B	N1	N2	P1	P2	N3	N4	P3	P4	N5	N6	P5	P6	N7	N8	P7	P8	I0	I1	I2	I3
0	0	OFF	OFF	ON	ON	OFF	ON	ON	OFF	ON	OFF	OFF	ON	ON	ON	OFF	OFF	1	0	0	0
0	1	OFF	ON	ON	OFF	OFF	OFF	ON	ON	ON	ON	OFF	OFF	ON	OFF	OFF	ON	0	1	0	0
1	0	ON	OFF	OFF	ON	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	ON	ON	OFF	0	0	1	0
1	1	ON	ON	OFF	OFF	ON	OFF	OFF	ON	OFF	ON	ON	OFF	OFF	OFF	ON	ON	0	0	0	1

2.2 TRANSMISSION GATE LOGIC STYLE

A transmission gate (TG) is a device that combines one n-type and one p-type transistor. The source and drain connections are short-circuited; thus the two devices are linked in parallel. The switching behaviour of TGs is controlled by the gate terminals of n-MOSFETs and p-MOSFETs. TGL has the benefit of being able to create strong '1' and '0'. At output nodes, certain logic designs can generate a full voltage swing.

TGL gates have the following key concerns:

• When compared to ordinary CMOS gates, TGL gates need less transistors.

• TGL can readily provide non-inverting AND/OR outputs with full-swing output voltage.

• To increase the switching speed of TGL gates, pre-charge through p-MOS (additional) and discharge through n-MOS (additional) are implemented.

• The voltage restoration is not as expected for some inputs.

Figure 2.2 shows the TGL circuit for a 2-4 decoder. At the output, an AHO type decoder is designed to create four AND terms. Table 2.2 shows the state of TGs and extra n- MOSFETs. The input signal passes via TGs, and the output signal only changes from logic '1' to logic '0' if the n-MOSFET is turned on. Only four TGs and four n-MOSFETs are required to create a 2-4 decoder.

TG MOSFETs receive complementary inputs. To increase the speed of logic swing, a discharging path is included. MOSFET aspect ratios must be appropriately set in order to provide full-swing output voltage. n-MOS and p-MOS are almost one-third and two-thirds the size of n-MOS utilised in general pass transistor logic, respectively. When compared to typical CMOS logic gates, TGLs gates are extremely fast.

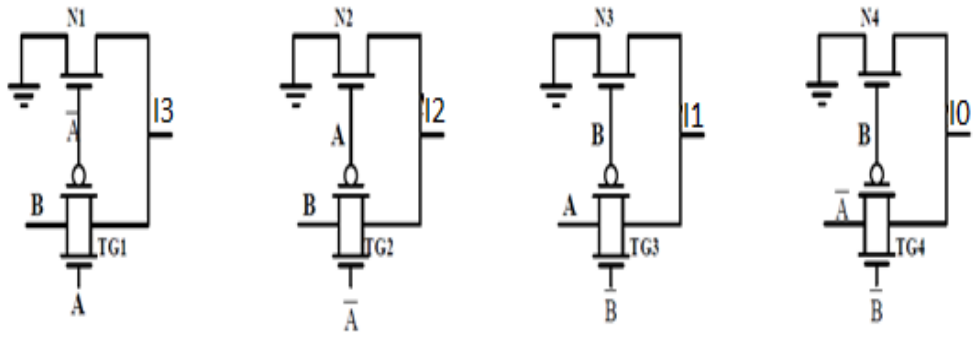

Fig. 2.2 2:4 decoder in TG logic style

Table 2.2 Functional table of TG 2:4 decoder

A	B	TG1	N1	TG2	N2	TG3	N3	TG4	N4	I0	I1	I2	I3
0	0	OFF	ON	ON	OFF	ON	OFF	ON	OFF	1	0	0	0
0	1	OFF	ON	ON	OFF	OFF	ON	OFF	ON	0	1	0	0
1	0	ON	OFF	OFF	ON	ON	OFF	ON	OFF	0	0	1	0
1	1	ON	OFF	OFF	ON	OFF	ON	OFF	ON	0	0	0	1

2.3 PASS TRANSISTOR DUAL VALUE LOGIC STYLE

The PDVL gates offer a few advantages over the Double Pass Transistor Logic gates (PDPL). PDVL gates were created by removing unnecessary branches from DPL gates. Instead of two pull-up p-MOS, just one is employed. Simultaneously, the aspect ratio of a single p-MOS in a pull-up circuit must be carefully set to maintain a balance with a pull-down n-MOS network.

As a result, PDVL is also known as Ratio Logic. To keep the benefits of DPL, such as equal rise and fall times and signal restoration capabilities, the W/L values must be fixed.

PDVL gates have the following primary advantages:

- Maintains high speed even when only one p-MOS is used in the pull-up network.
- Full output voltage swing is obtained.
- There are fewer transistors.
- Redundant branches are deleted, resulting in the elimination of some nodes and transitions at those nodes.

In Fig.2.3, a 2-4 decoder is developed utilising the PDVL approach. The gate and drain terminals of a single p-MOS situated above the output node receive two inputs. When A='0' and B='0,' the output I0='1' because P1 will be ON, but N1 and N2: will be OFF. The state of MOSFETs changes in a similar manner when the input combination is altered, as indicated in Table 2.3. PDVL is used to create an AHO kind of decoder.

This approach is ideal for creating AND/OR logic. The AND gate for the AHO kind of decoder is implemented in PDVL manner. It is necessary to create an ALO type decoder OR gate. When using OR gates, a single n-MOS device in the pull-down network and two p-MOS devices in the pull-up network can be employed.

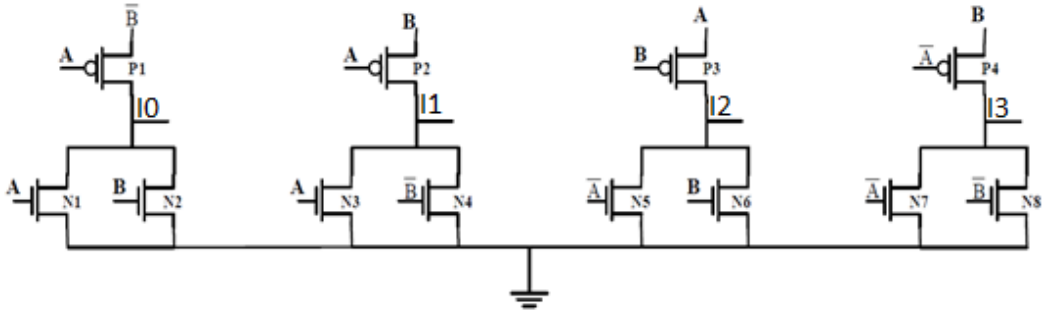

Fig. 2.3 2:4 decoder in PDV logic style

Table 2.3 Functional table of PDV 2:4 decoder

A	B	N1	N2	P1	N3	N4	P2	N5	N6	P3	N7	N8	P4	I0	I1	I2	I3
0	0	OFF	OFF	ON	OFF	ON	ON	ON	OFF	ON	ON	ON	OFF	1	0	0	0
0	1	OFF	ON	ON	OFF	OFF	ON	ON	ON	OFF	ON	OFF	OFF	0	1	0	0
1	0	ON	OFF	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	ON	0	0	1	0
1	1	ON	ON	OFF	ON	OFF	OFF	OFF	ON	ON	OFF	OFF	ON	0	0	0	1

When compared to CMOS and TGL logic styles, this logic style has a medium speed and power dissipation. In general, the layout design of PDVL and TGL should be done with extreme caution. Despite employing a smaller number of components, the arrangement would not be as compact as CMOS.

The gate and source terminals get the supply voltage, whereas the gate and source terminals receive the input logic values. As illustrated in Fig.2.3, all of the source terminals of pull-down n-MOSFETs are tied to ground.

In a pull-down network, the aspect ratio of a single p-MOS is balanced with the aspect ratio of all n-MOS. This logic will output strong '1' and strong '0' for almost all input combinations. Only inverters get true supply voltage in order to provide complemented inputs for the PDVL decoder.

CHAPTER 3

SIMULATIONS

3.1 90nm TECHNOLOGY NODE

NMOS: W/L = 135nm/90nm

PMOS: W/L = 270nm/90nm

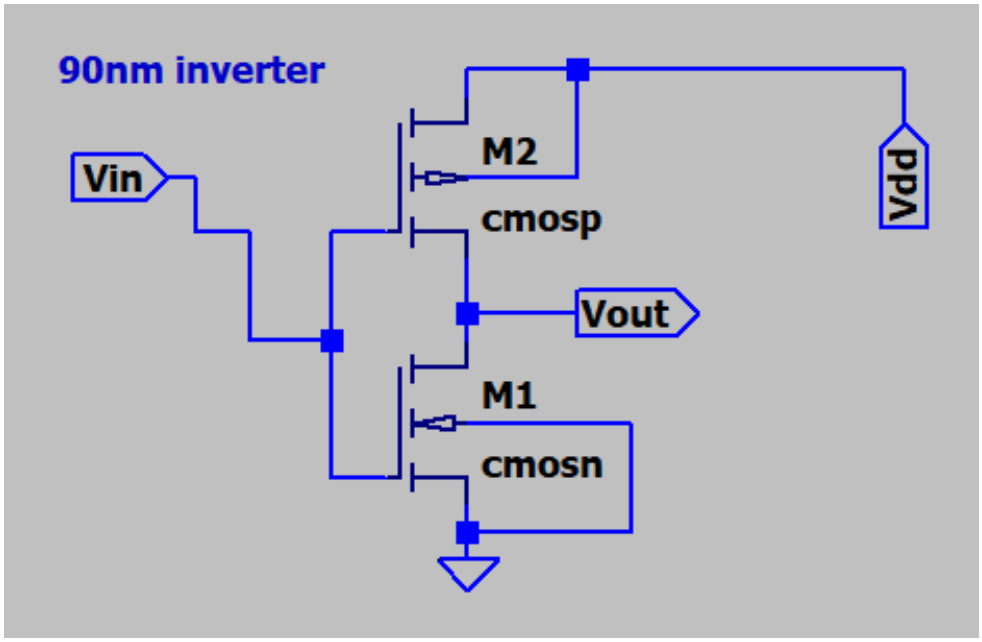

Fig. 3.1 CMOS inverter schematic

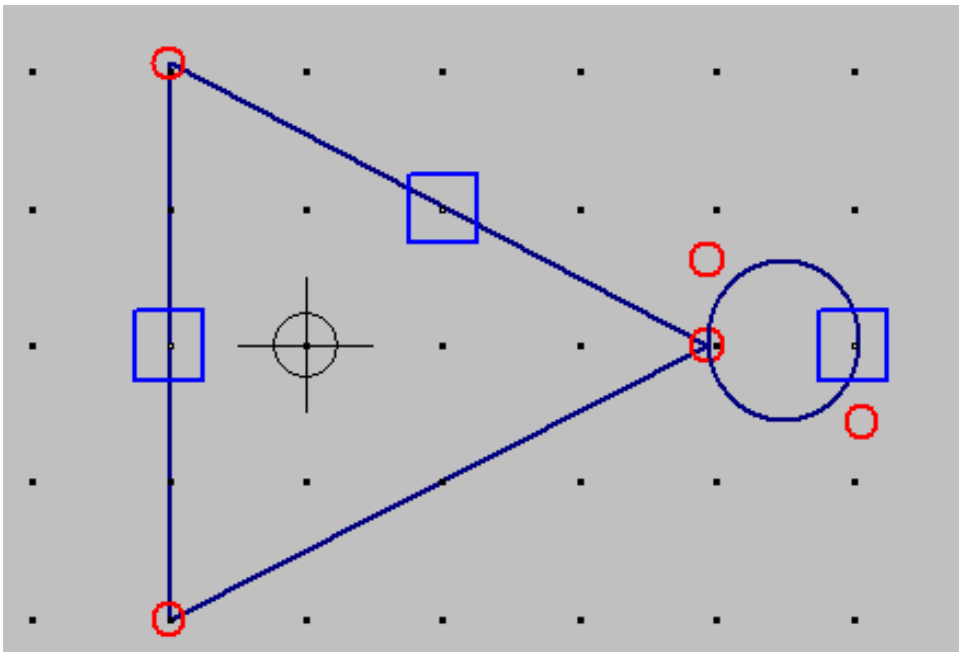

Fig. 3.2 CMOS inverter symbol

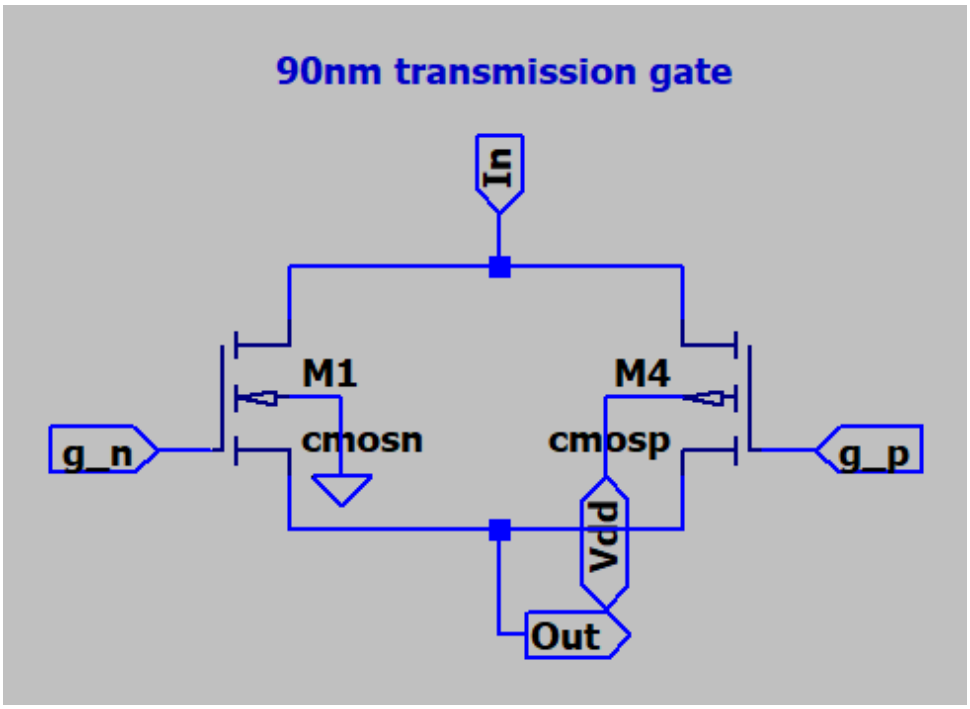

Fig. 3.3 TG schematic

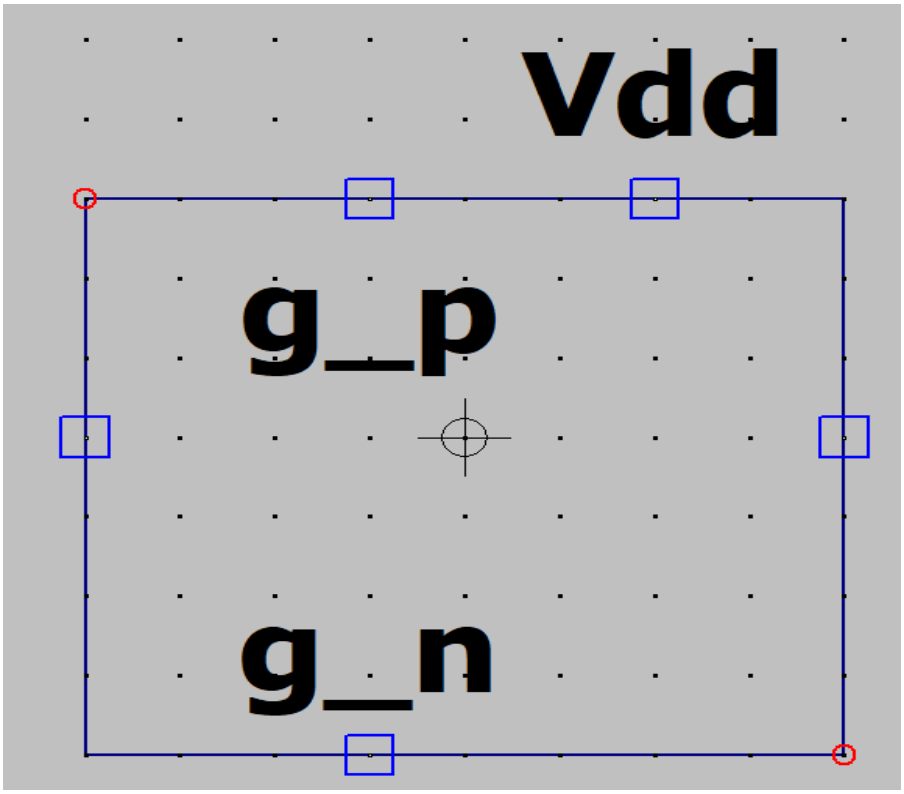

Fig. 3.4 TG symbol

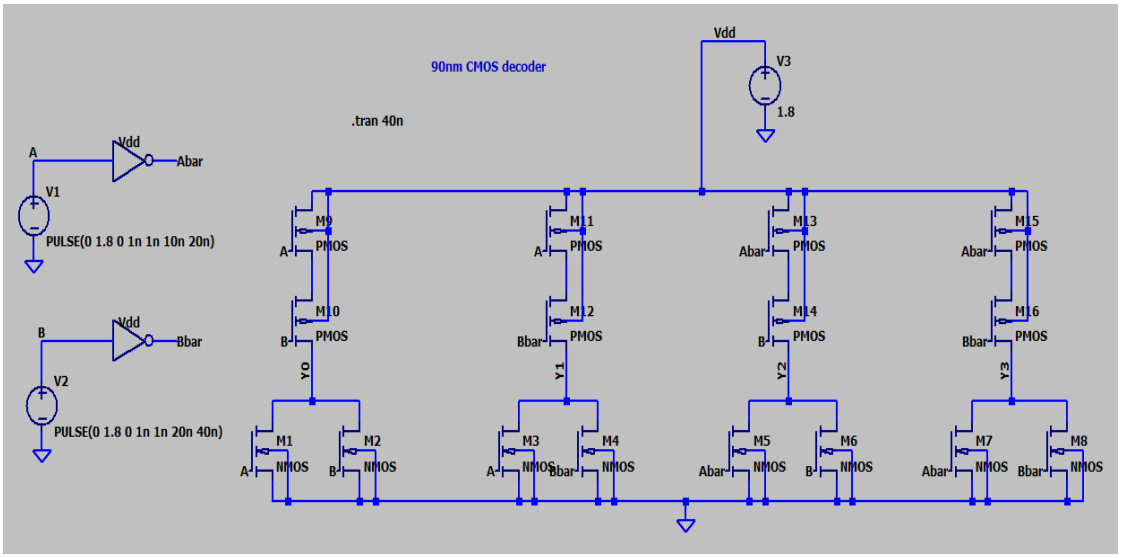

Fig. 3.5 2:4 decoder using CMOS logic style

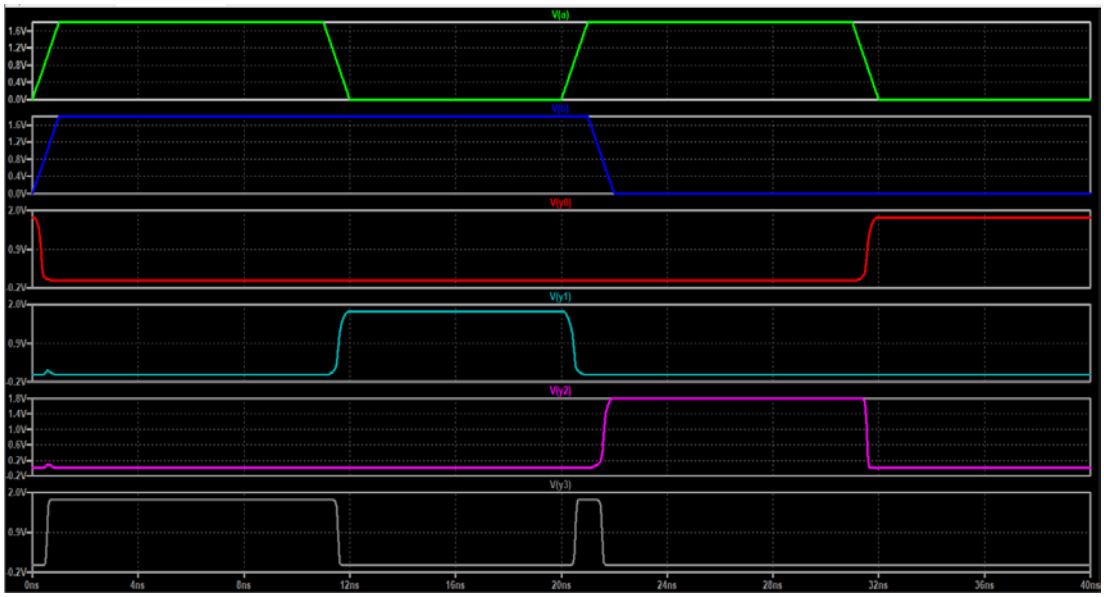

Fig. 3.6 Output of 2:4 decoder using CMOS logic style

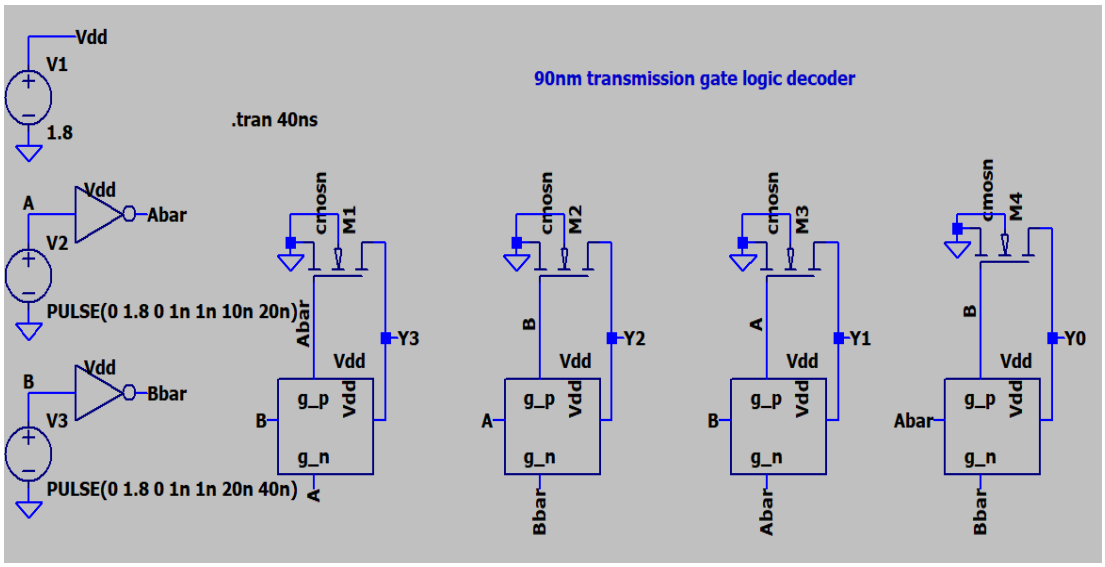

Fig. 3.7 2:4 decoder using TG logic style

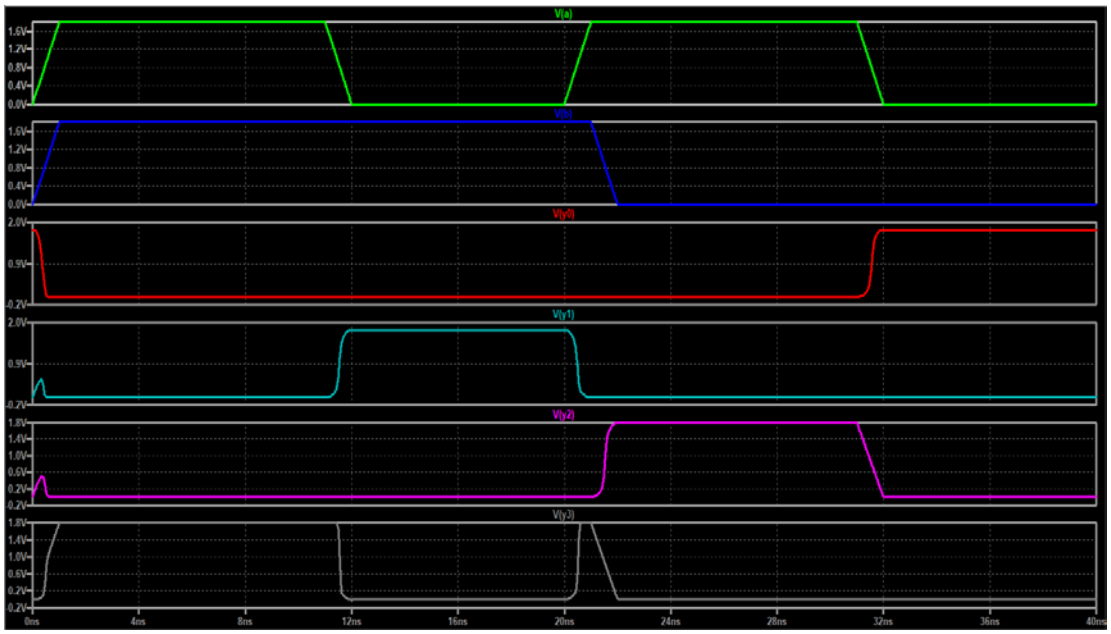

Fig. 3.8 Output of 2:4 decoder using TG logic style

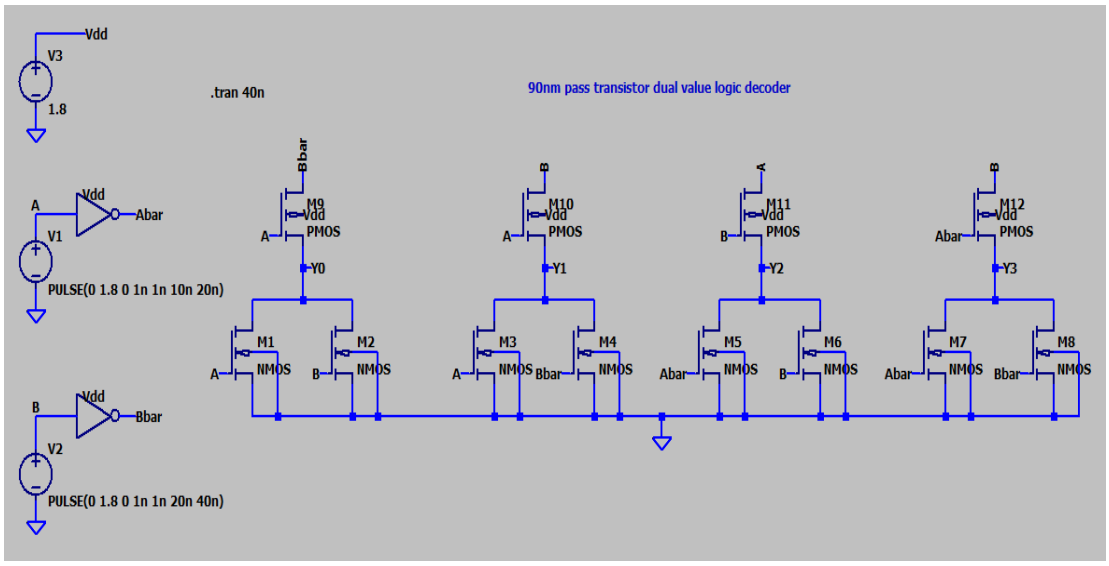

Fig. 3.9 2:4 decoder using PDV logic style

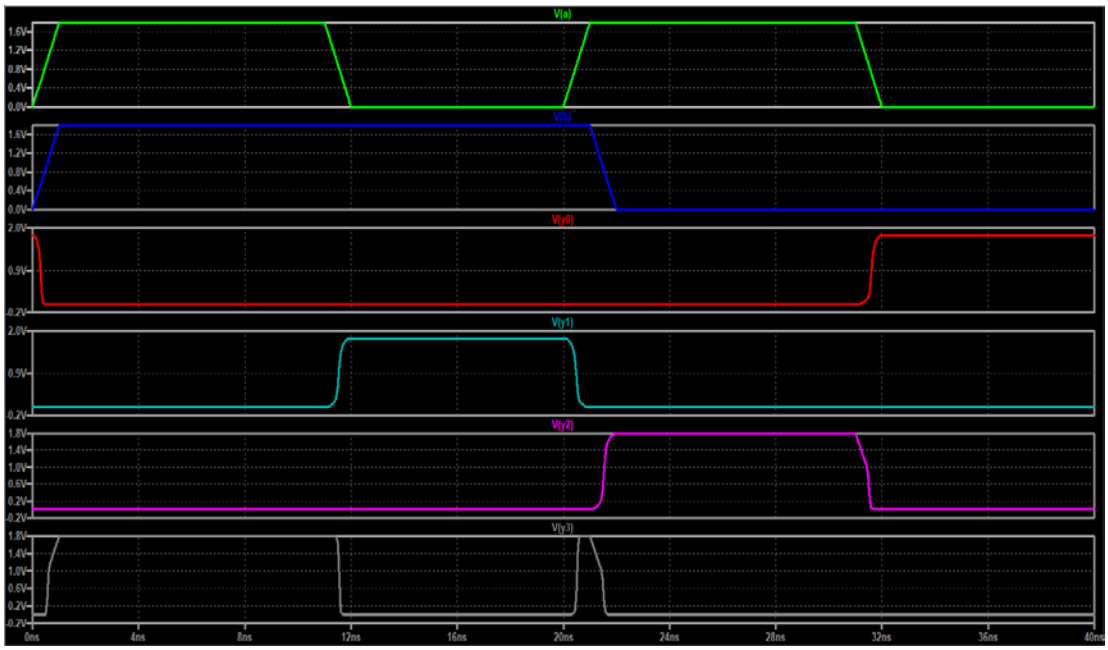

Fig. 3.10 Output of 2:4 decoder using PDV logic style

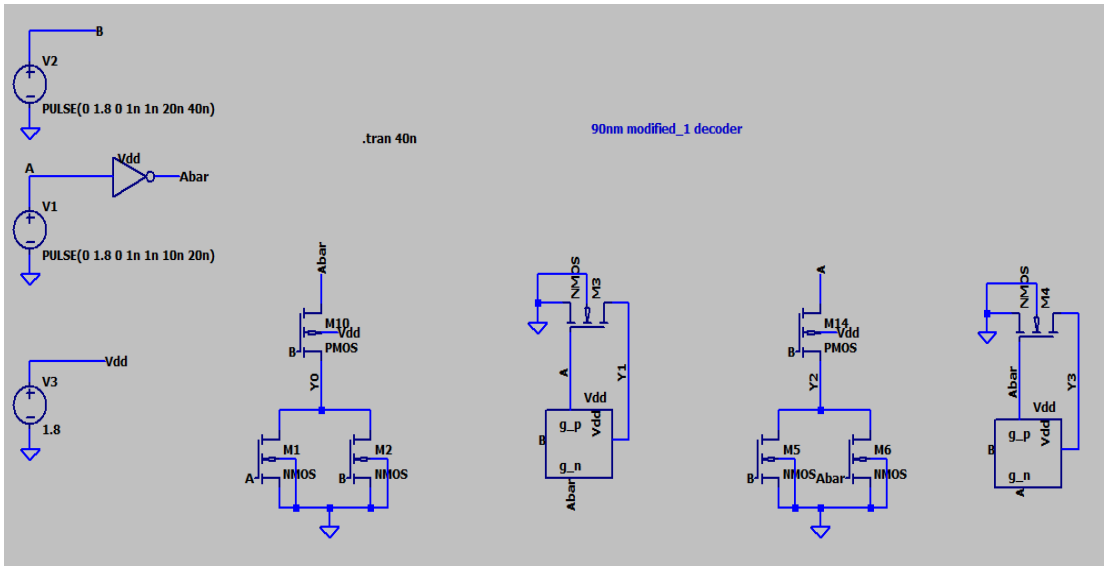

Fig. 3.11 2:4 decoder modified 1 circuit

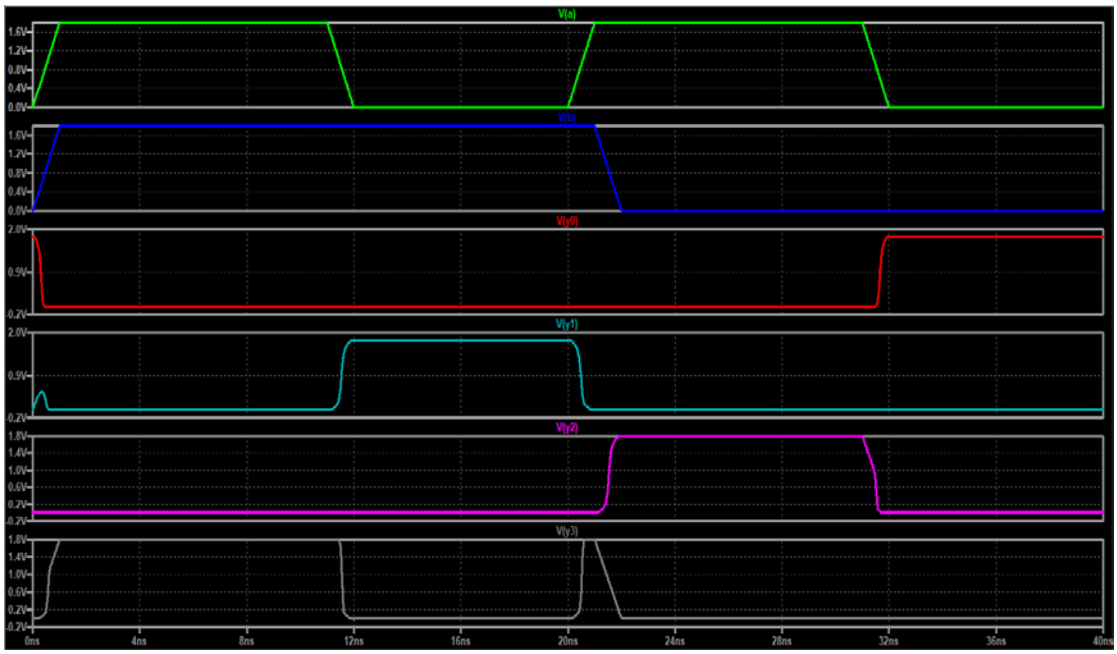

Fig. 3.12 Output of 2:4 decoder modified 1 circuit

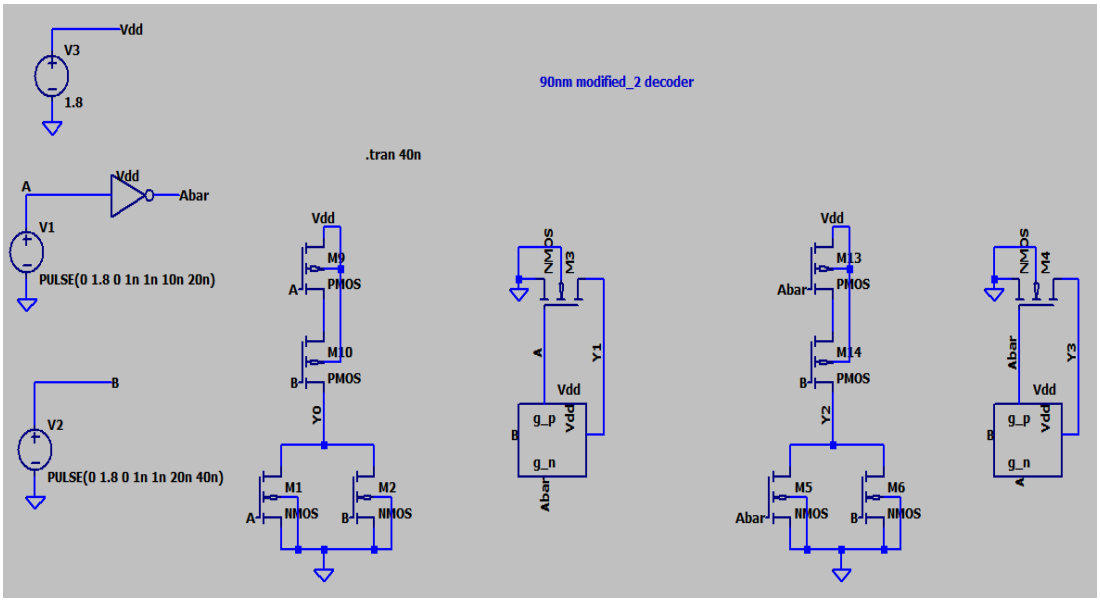

Fig. 3.13 2:4 decoder modified 2 circuit

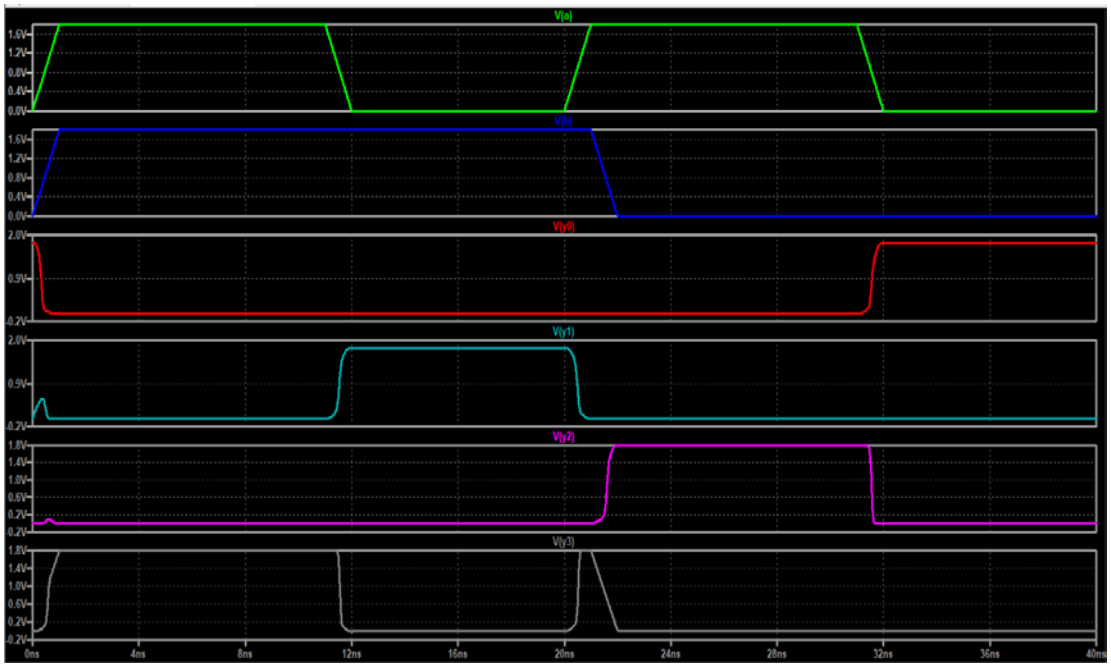

Fig. 3.14 Output of 2:4 decoder modified 2 circuit

3.2 180nm TECHNOLOGY NODE

NMOS: W/L = 360nm/180nm

PMOS: W/L = 720nm/180nm

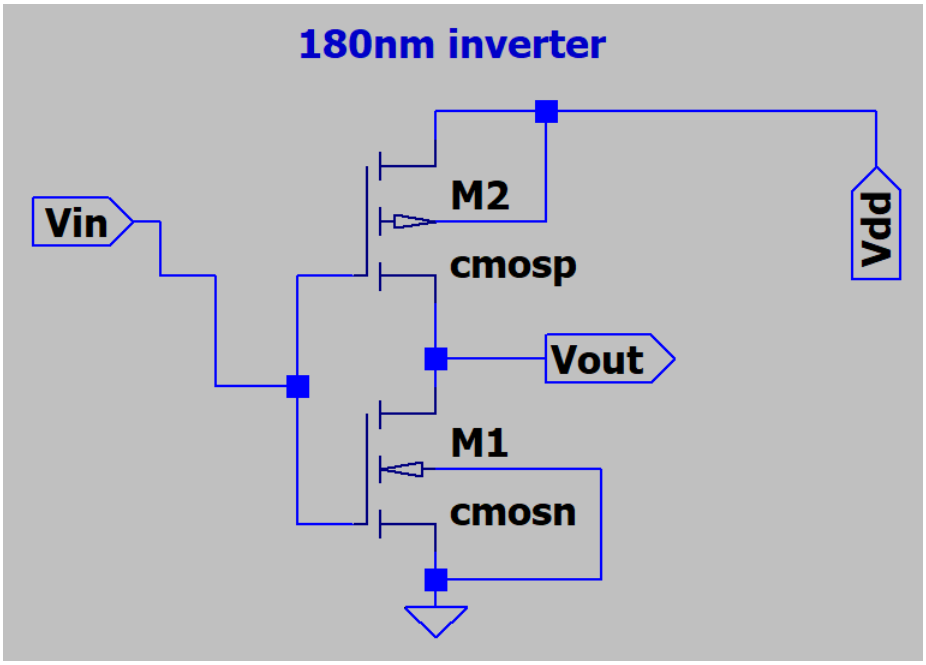

Fig. 3.15 CMOS inverter schematic

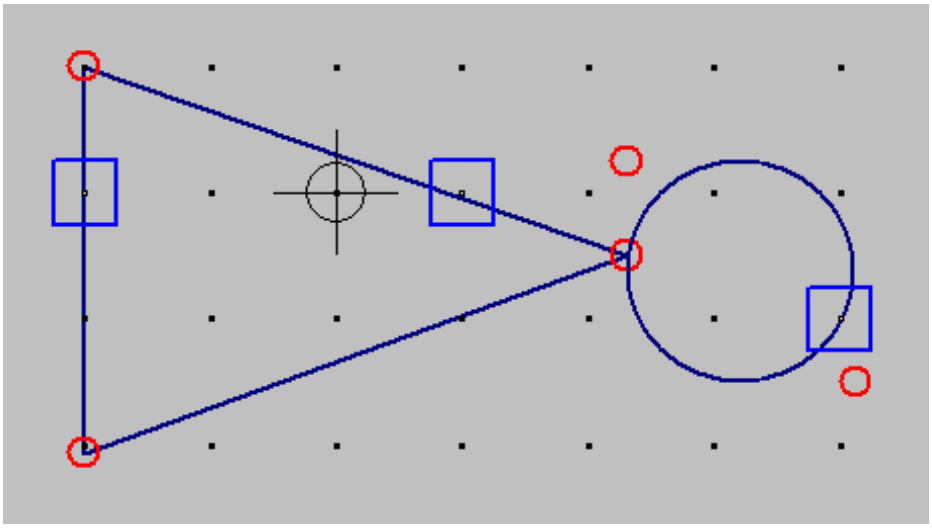

Fig. 3.16 CMOS inverter symbol

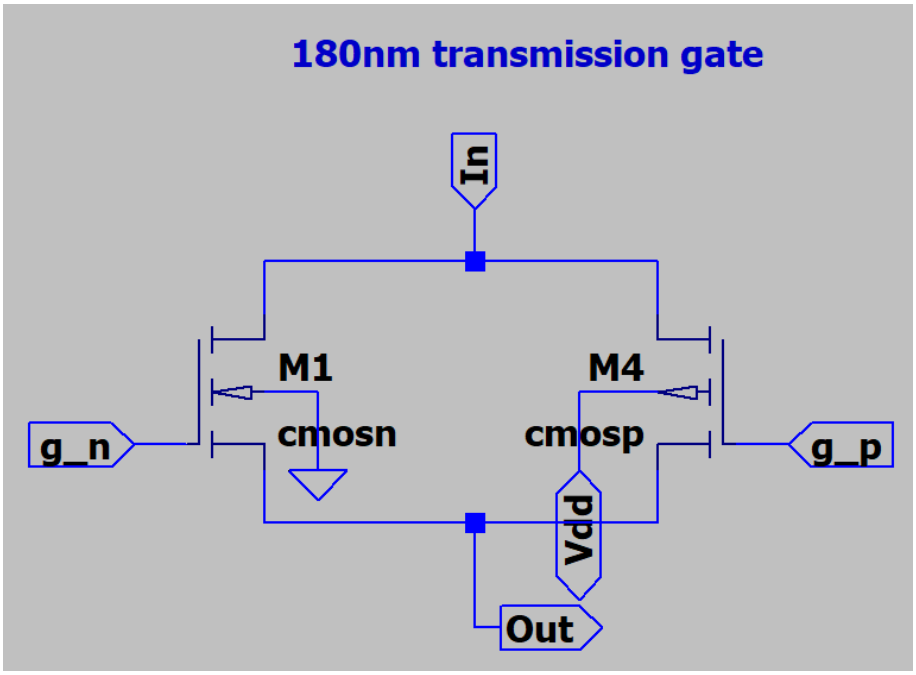

Fig. 3.17 TG schematic

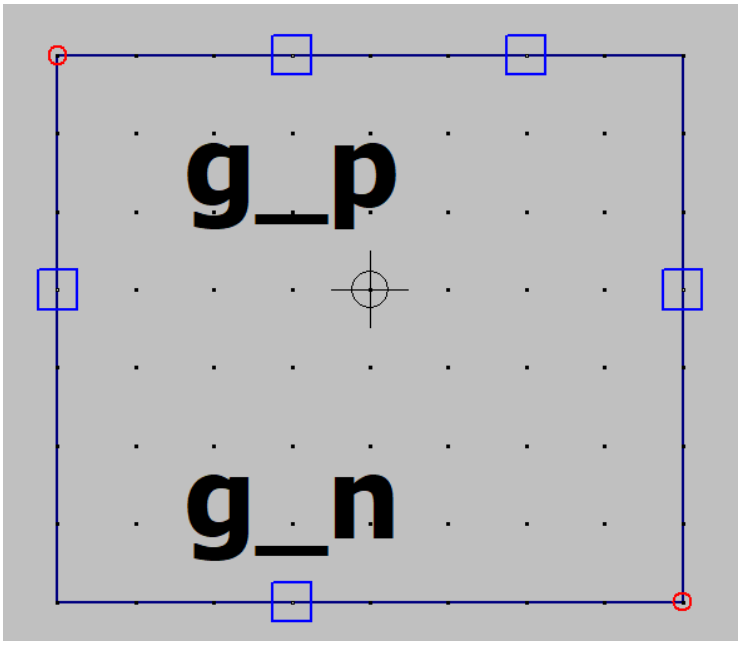

Fig. 3.18 TG symbol

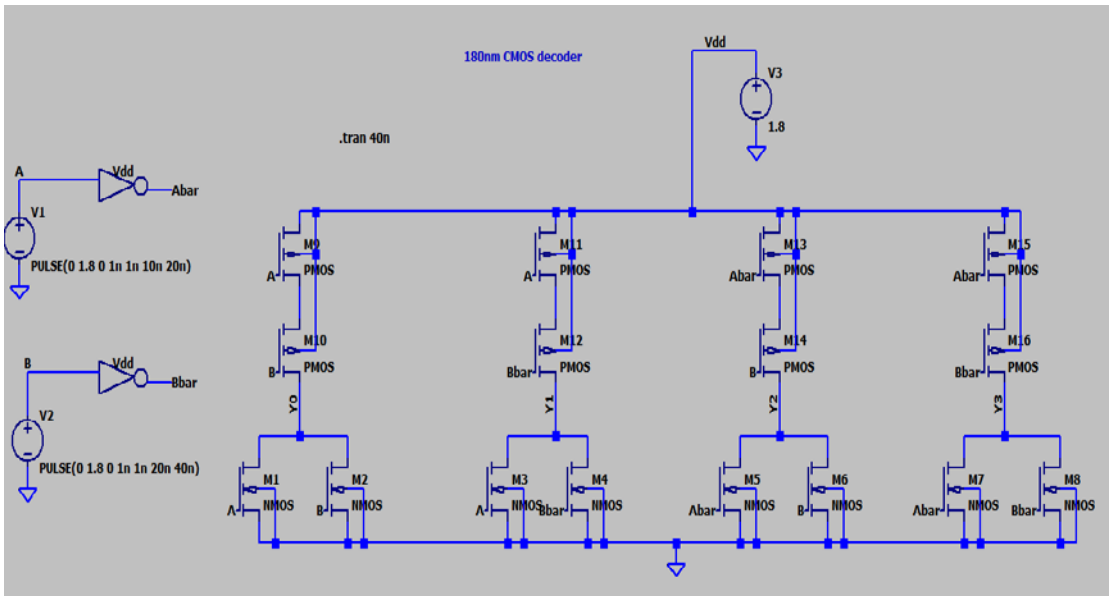

Fig. 3.19 2:4 decoder using CMOS logic style

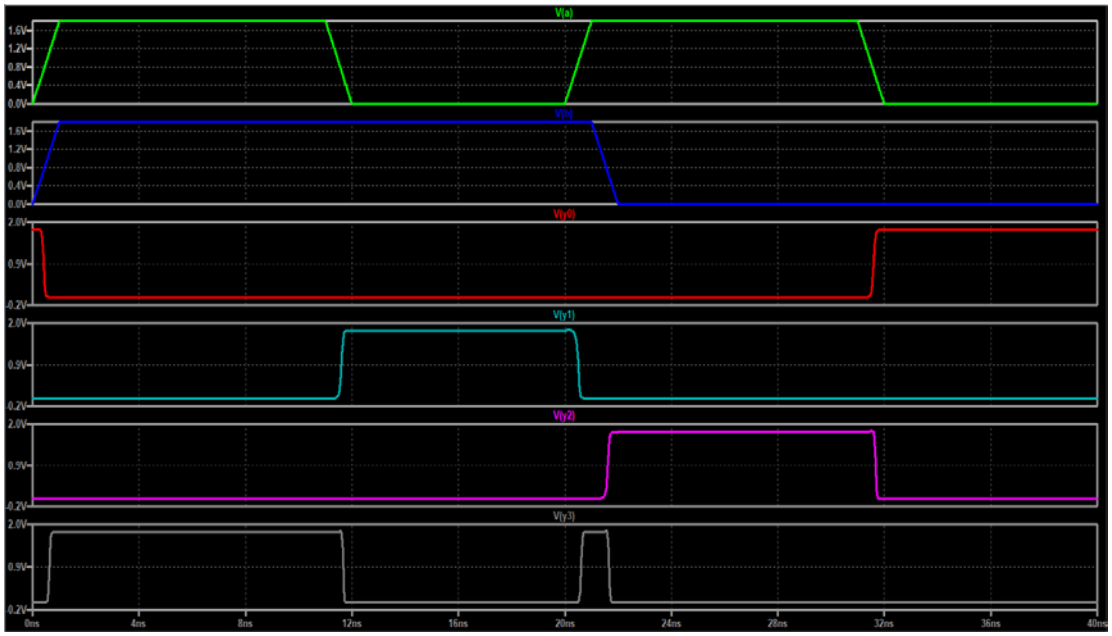

Fig. 3.20 Output of 2:4 decoder using CMOS logic style

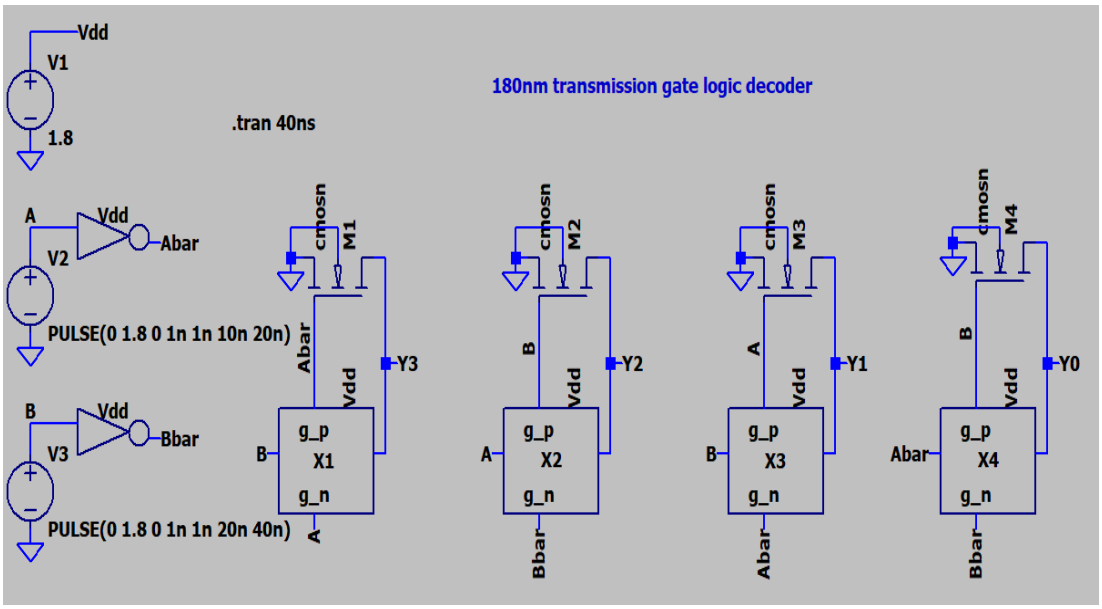

Fig. 3.21 2:4 decoder using TG logic style

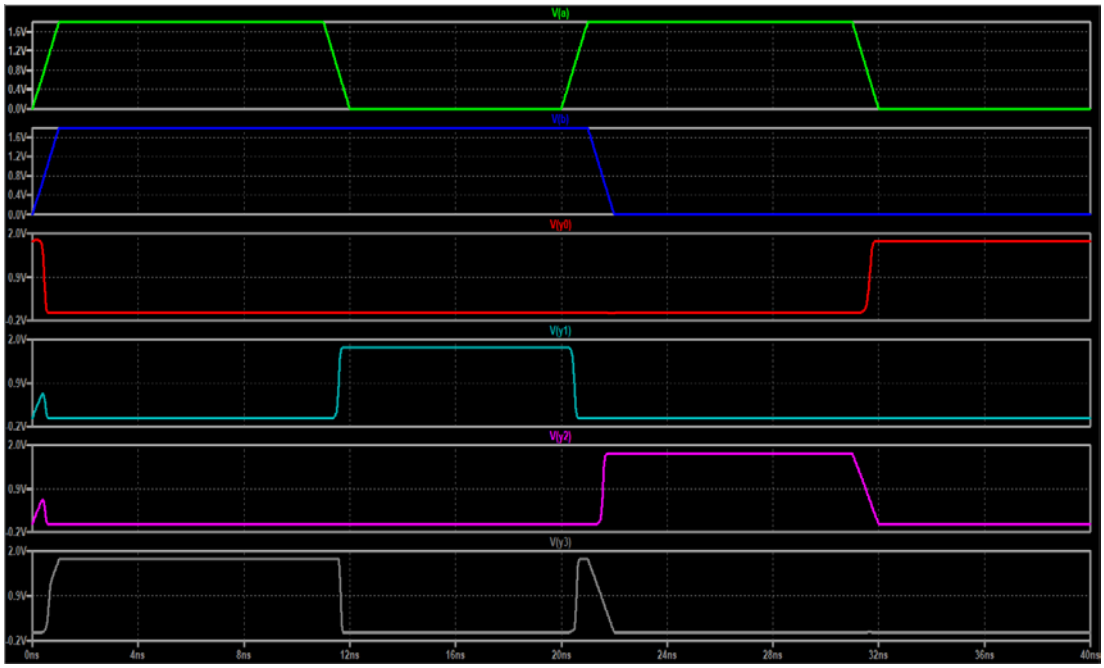

Fig. 3.22 Output of 2:4 decoder using TG logic style

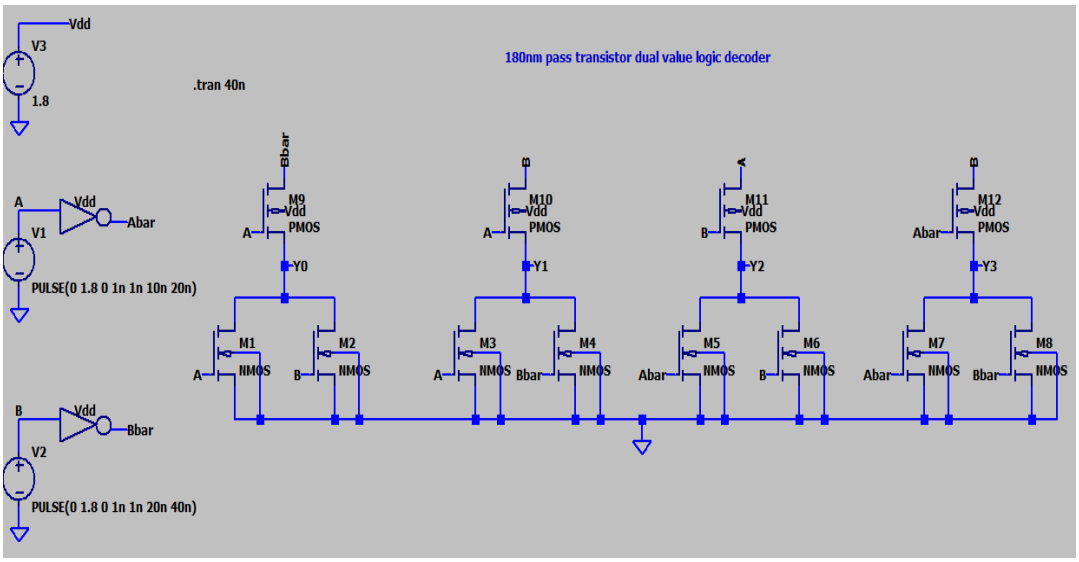

Fig. 3.23 2:4 decoder using PDV logic style

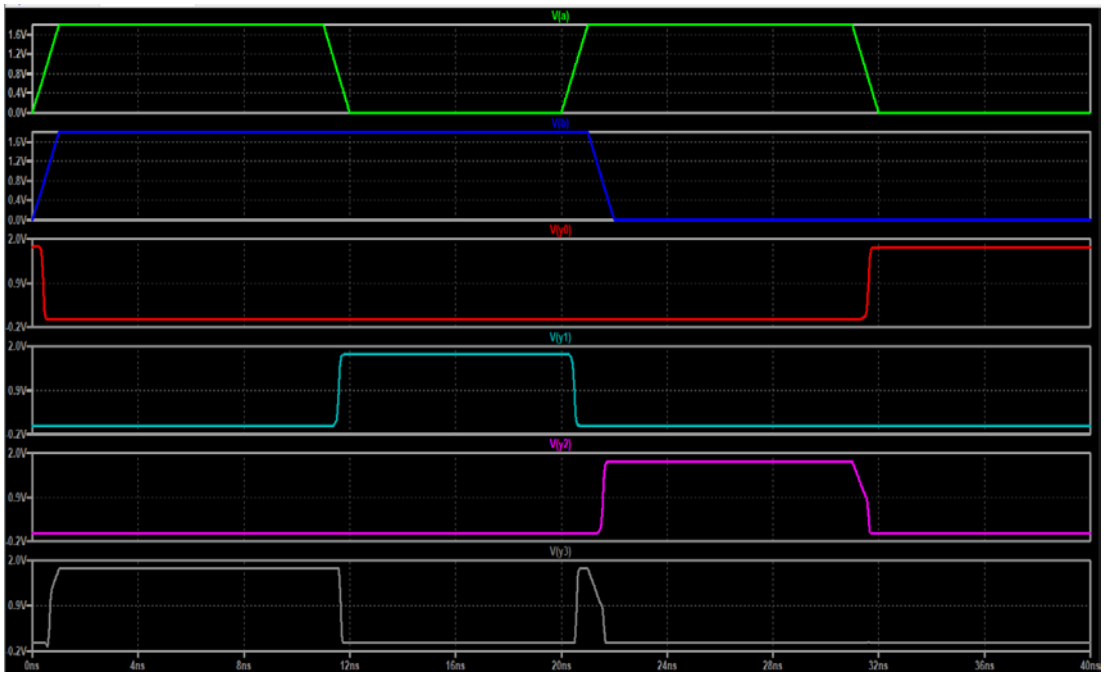

Fig. 3.24 Output of 2:4 decoder using PDV logic style

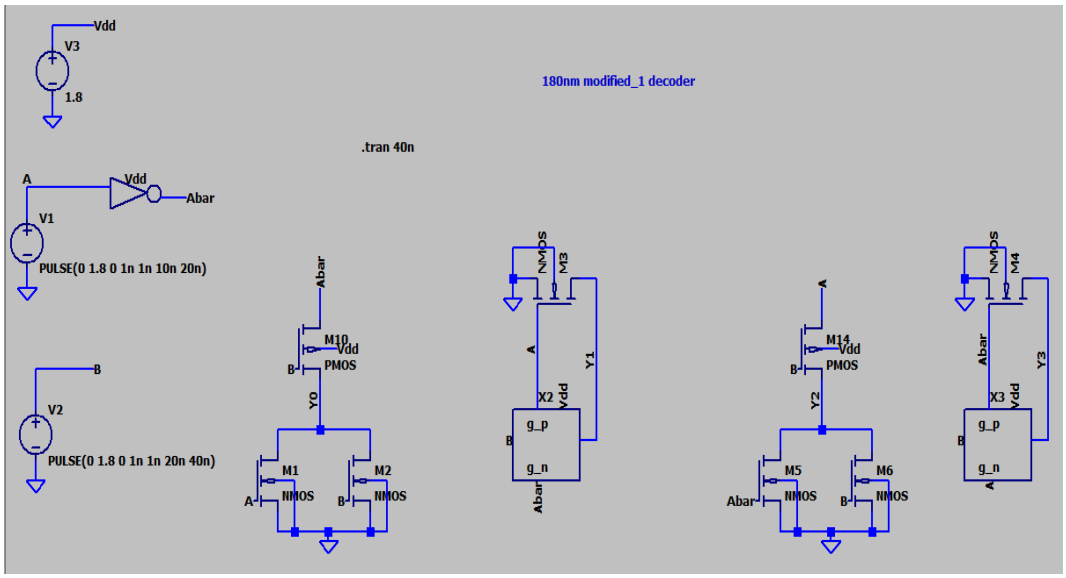

Fig. 3.25 2:4 decoder modified 1 circuit

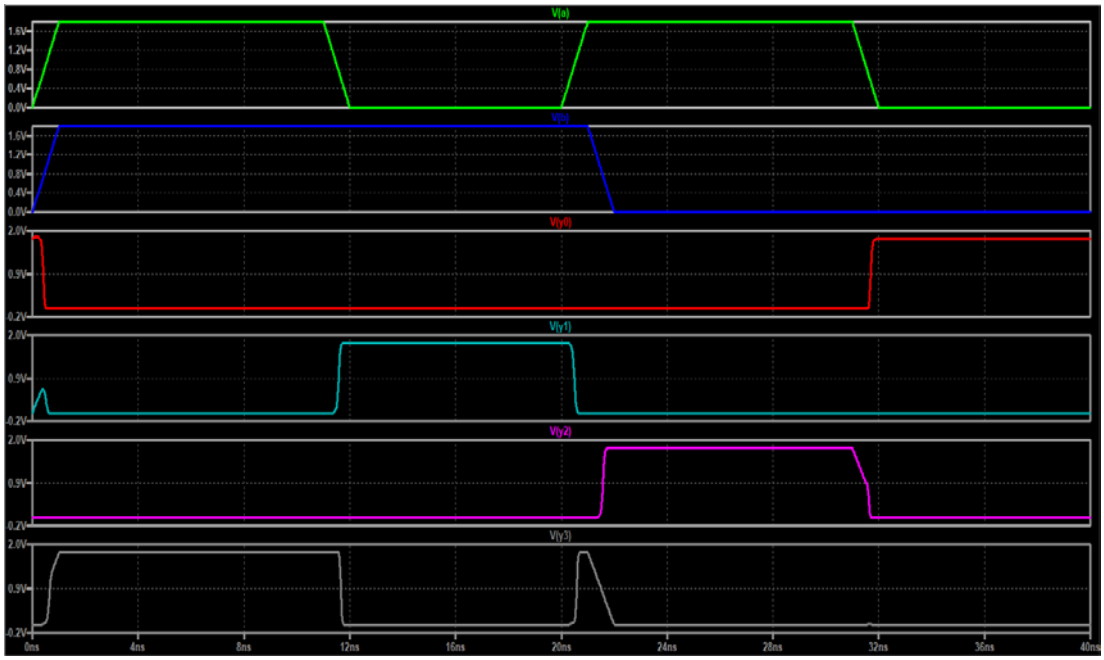

Fig. 3.26 Output of 2:4 decoder modified 1 circuit

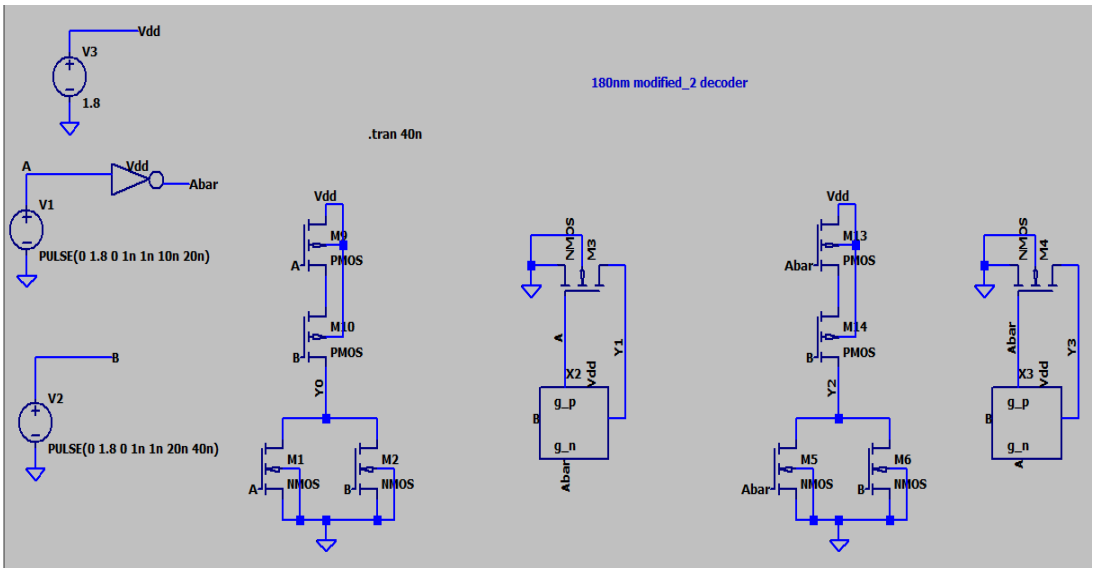

Fig. 3.27 2:4 decoder modified 2 circuit

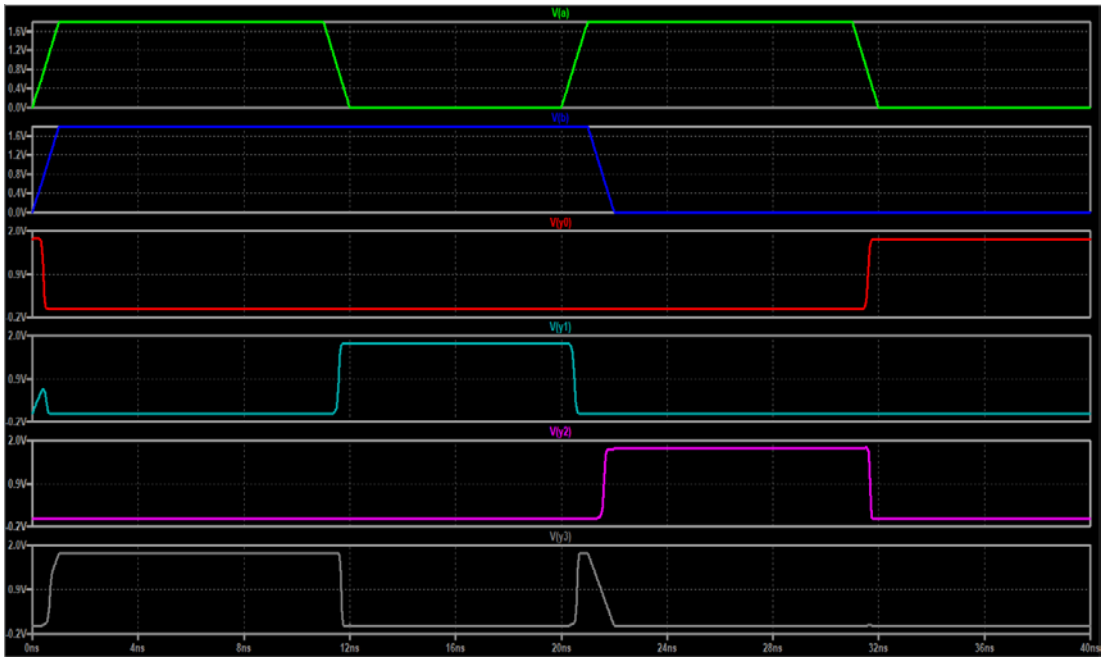

Fig. 3.28 Output of 2:4 decoder modified 2 circuit

CHAPTER 4

RESULT

A 2:4 decoder is designed in three different styles i.e. CMOS style, TGL style and PDVL style. Two different 2:4 decoder circuits have also been proposed in this project. These designs are simulated using LTspice software at 90nm and 180nm technology node and at two different temperatures i.e. 27C and 120C. This work focuses on the analysis of the CMOS, TGL, PDVL and two proposed circuits in terms of area, average energy and propagation delay.

Table 4.1 Area comparison

Decoder	**No. of transistors**
CMOS	20
TGL	16
PDVL	16
Modified 1	**14**
Modified 2	16

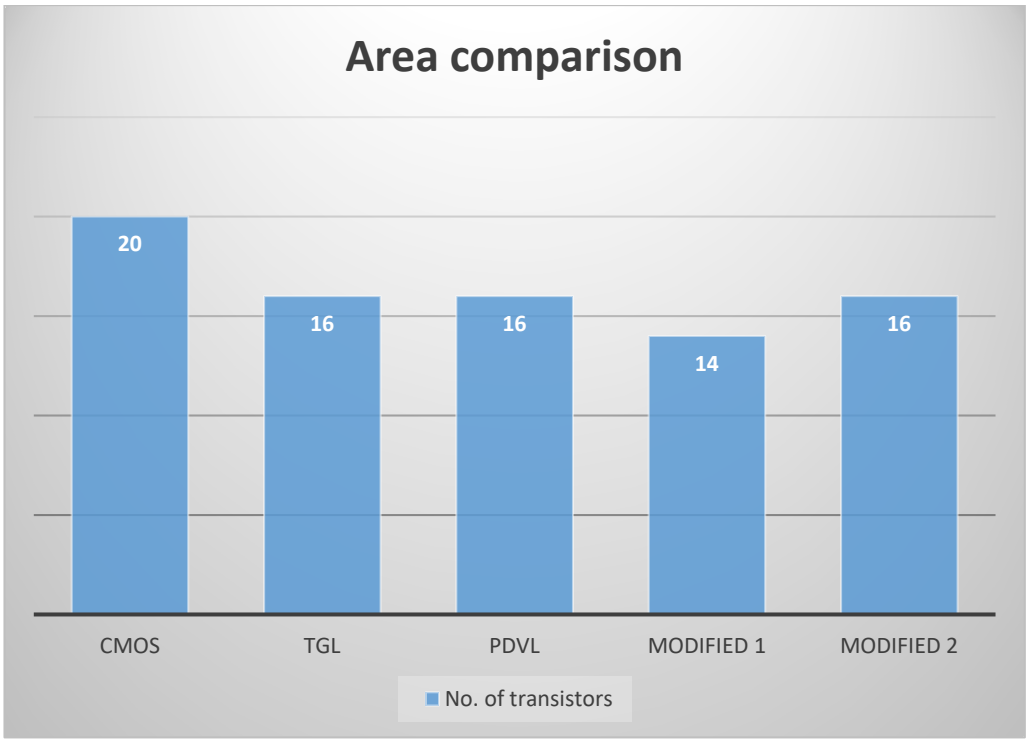

Fig. 4.1 Area comparison

Table 4.2 Average energy comparison at 90nm

Decoder	**27C**	**120C**
CMOS	742.66fJ	551.21fJ
TGL	403.29fJ	296.89fJ
PDVL	450.7fJ	326.19fJ
Modified 1	**289.17fJ**	**207.15fJ**
Modified 2	436.05fJ	315.45fJ

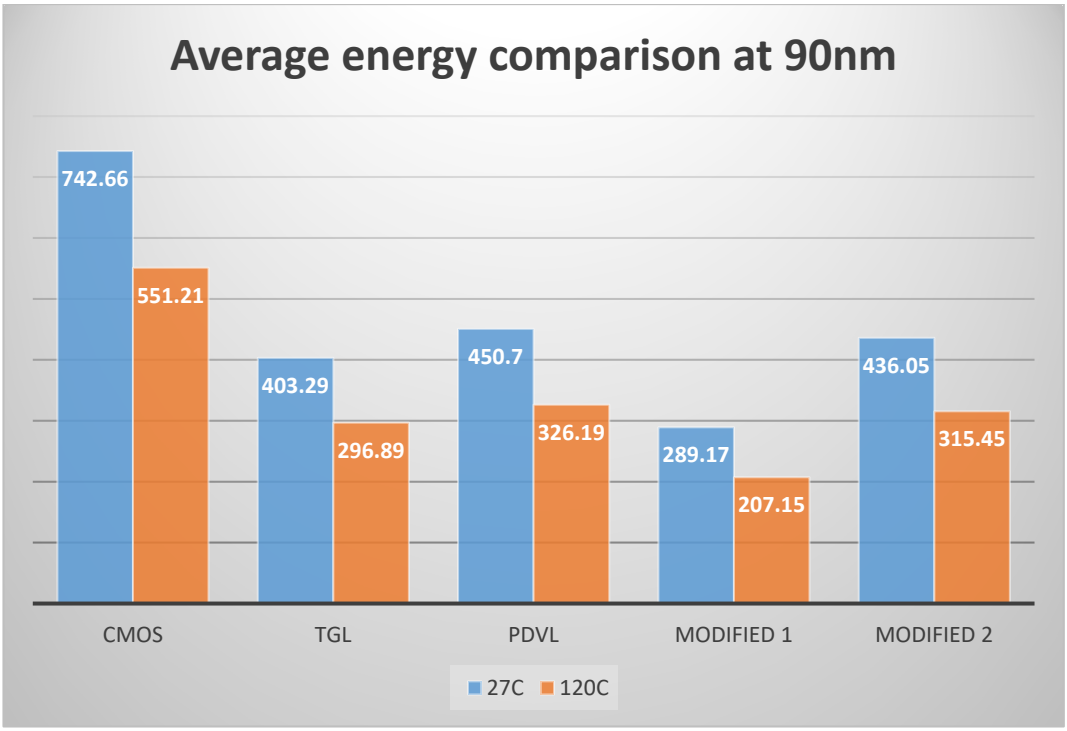

Fig. 4.2 Average energy comparison at 90nm

Table 4.3 Average energy comparison at 180nm

Decoder	**27C**	**120C**
CMOS	215.26fJ	173.64fJ
TGL	108.76fJ	85.167fJ
PDVL	123.81fJ	97.011fJ
Modified 1	**83.123fJ**	**66.621fJ**
Modified 2	128.13fJ	103.04fJ

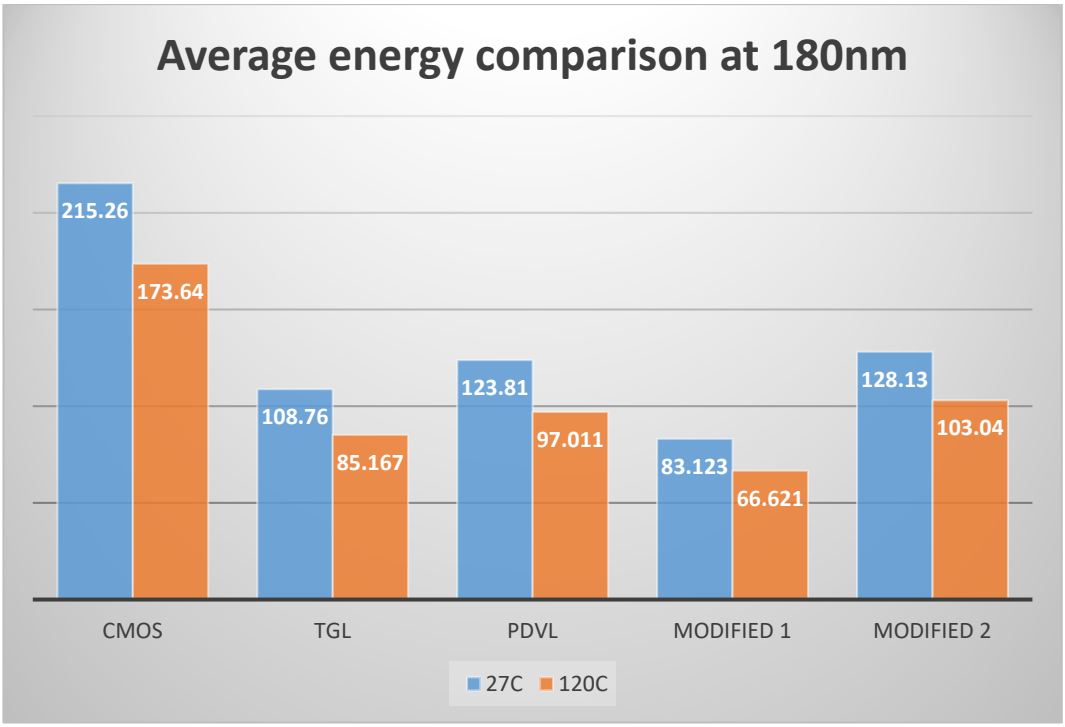

Fig. 4.3 Average energy comparison at 180nm

Table 4.4 Average energy comparison at 27C

Decoder	**90nm**	**180nm**
CMOS	742.66fJ	215.26fJ
TGL	403.29fJ	108.76fJ
PDVL	450.7fJ	123.81fJ
Modified 1	**289.17fJ**	**83.123fJ**
Modified 2	436.05fJ	128.13fJ

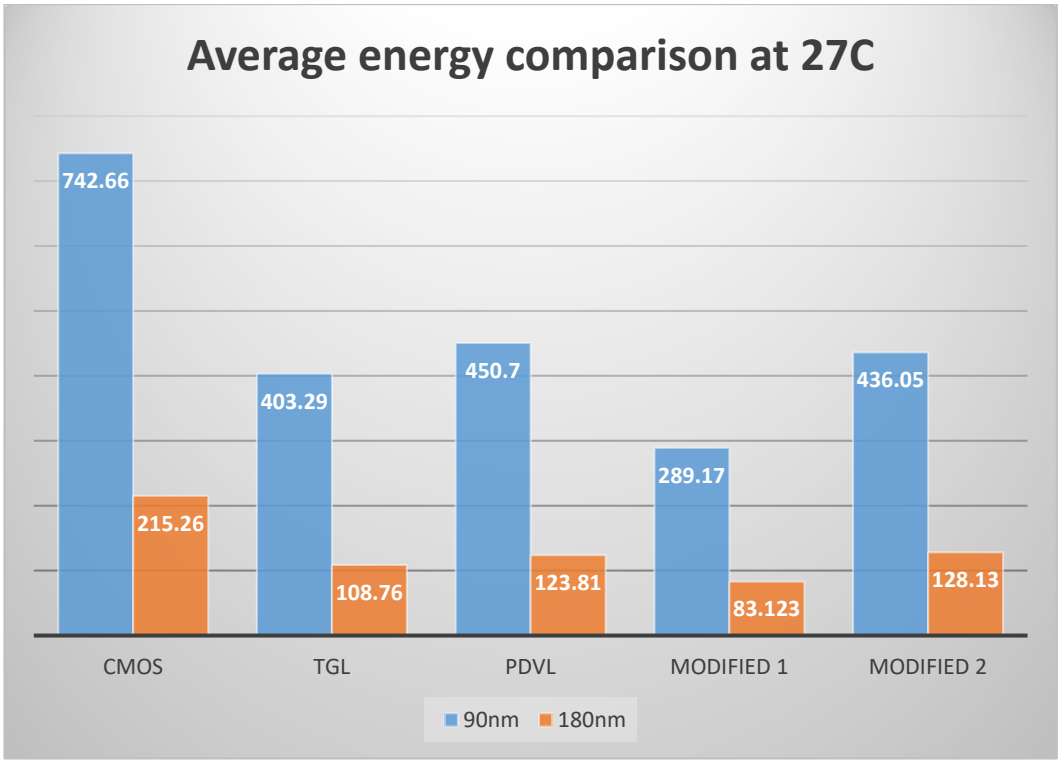

Fig. 4.4 Average energy comparison at 27C

Table 4.5 Average energy comparison at 120C

Decoder	**90nm**	**180nm**
CMOS	551.21fJ	173.64fJ
TGL	296.89fJ	85.167fJ
PDVL	326.19fJ	97.011fJ
Modified 1	**207.15fJ**	**66.621fJ**
Modified 2	315.45fJ	103.04fJ

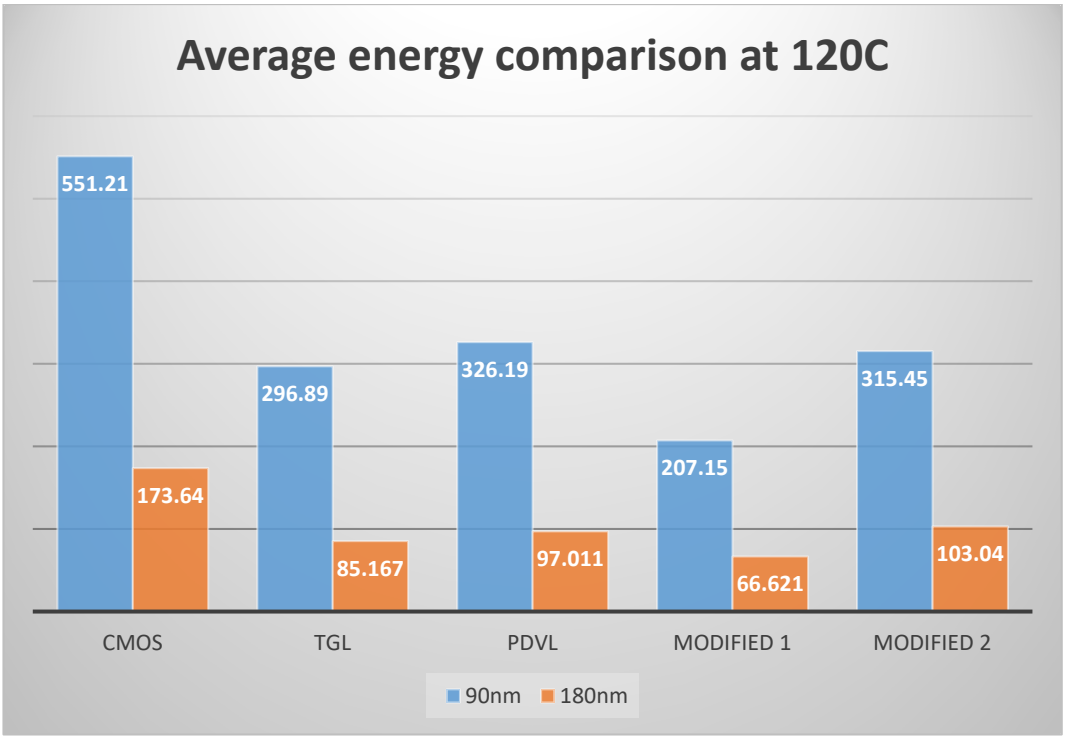

Fig. 4.5 Average energy comparison at 120C

Table 4.6 Propagation delay comparison at 90nm

Decoder	**27C**	**120C**
CMOS	103.71ps	115.47ps
TGL	101.66ps	108.01ps
PDVL	107.02ps	119.84ps
Modified 1	96.78ps	104.89ps
Modified 2	**84.32ps**	**97.12ps**

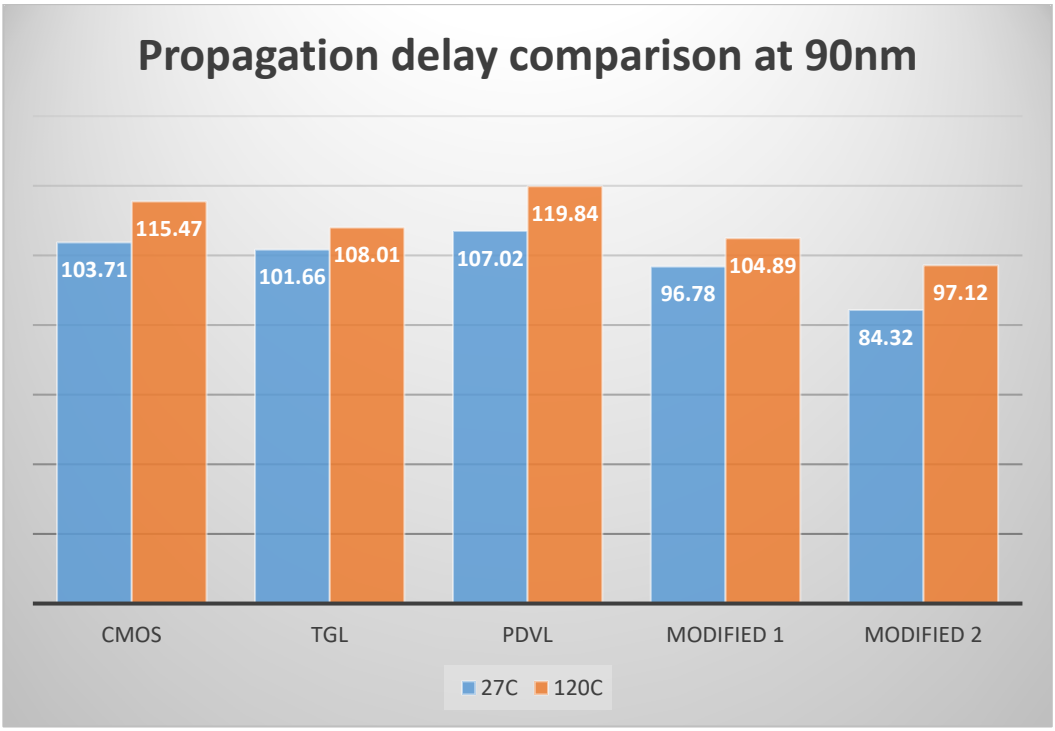

Fig. 4.6 Propagation delay comparison at 90nm

Table 4.7 Propagation delay comparison at 180nm

Decoder	**27C**	**120C**
CMOS	269.32ps	271.74ps
TGL	261.48ps	268.39ps
PDVL	272.79ps	288.89ps
Modified 1	249.11ps	254.13ps
Modified 2	**235.67ps**	**241.37ps**

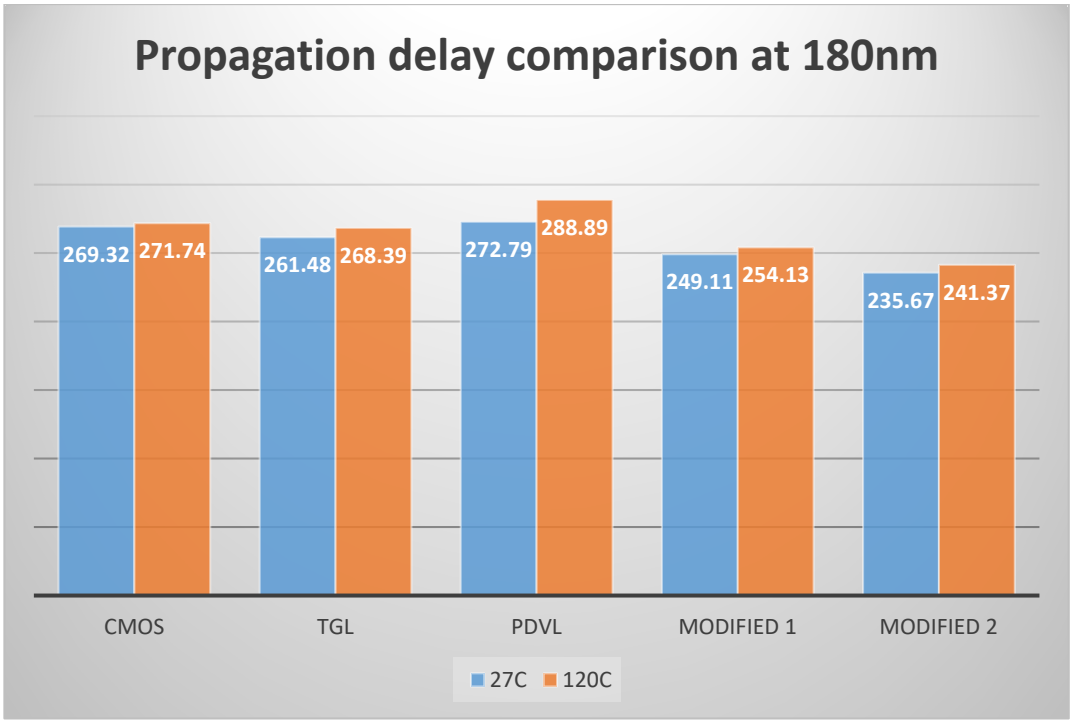

Fig. 4.7 Propagation delay comparison at 180nm

Table 4.8 Propagation delay comparison at 27C

Decoder	**90nm**	**180nm**
CMOS	103.71ps	269.32ps
TGL	101.66ps	261.48ps
PDVL	107.02ps	272.79ps
Modified 1	96.78ps	249.11ps
Modified 2	**84.32ps**	**235.67ps**

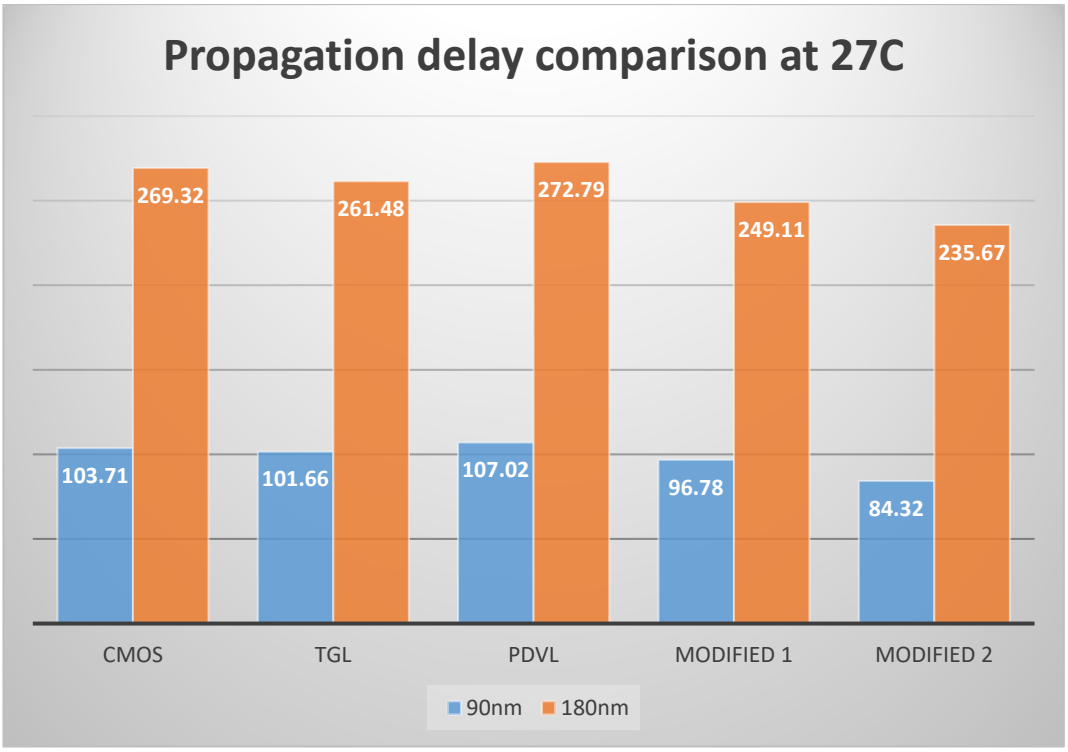

Fig. 4.8 Propagation delay comparison at 27C

Table 4.9 Propagation delay comparison at 120C

Decoder	**90nm**	**180nm**
CMOS	115.47ps	271.74ps
TGL	108.01ps	268.39ps
PDVL	119.84ps	288.89ps
Modified 1	104.89ps	254.13ps
Modified 2	**97.12ps**	**241.37ps**

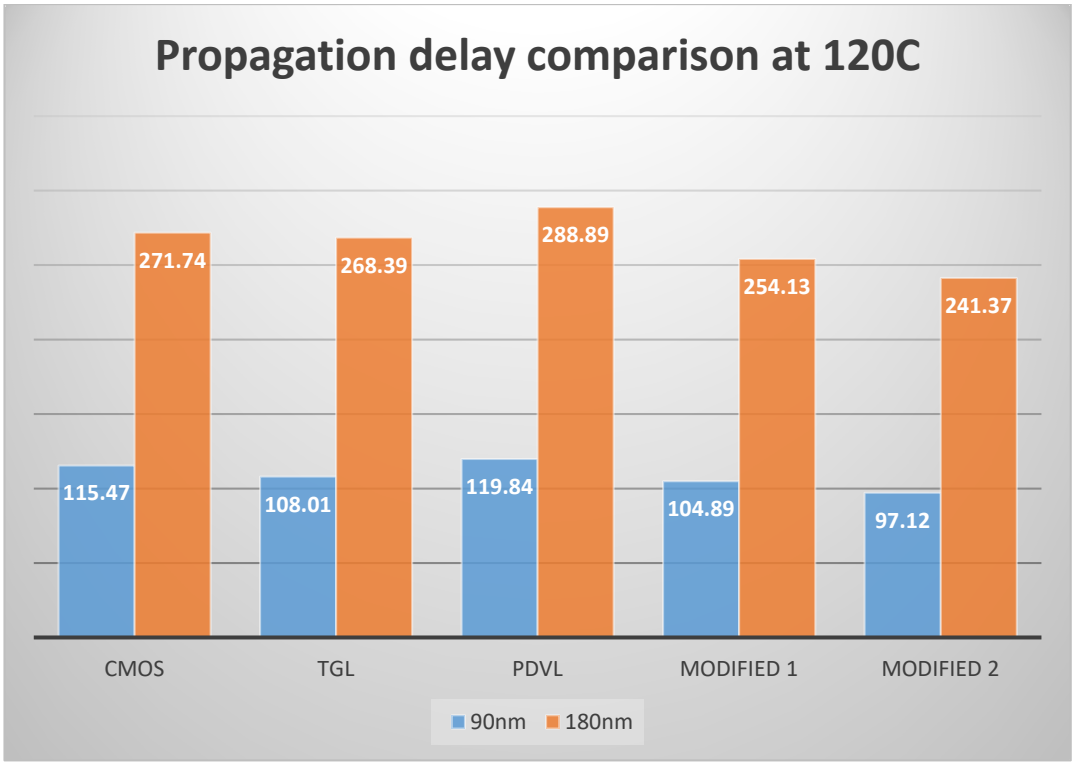

Fig. 4.9 Propagation delay comparison at 120C

At low speeds, the CMOS style is symmetric, ratio-less logic, and dual in nature, with the least static power dissipation. Even if the voltage is scaled down, CMOS logic architecture will create strong '1' and strong '0'. For the same purpose, TGL takes up less space, dissipates less power, and is very simple. Logic swing can be improved by appropriately selecting the W/L ratio of n-MOS and p-MOS transistors coupled in parallel of a TG.

TGL, however, was unable to create the requisite logic swing as the voltage was reduced. The layout area of a TGL-based decoder would most likely be smaller. By keeping the features of CMOS logic, the PDVL design requires fewer transistors. PDVL produces adequate logic swing for specified input combinations, has a lower transistor count than CMOS, and does not require a supply voltage input.

By analysing the data above, it can be deduced that modified 1 circuit consumes the least area with only 14 transistors. Therefore, whenever we want the design to be compact, modified 1 circuits is an optimum choice. For 90nm technology

node, modified 1 circuit consumes the least amount of average energy at both the temperatures. For 180nm technology node also, modified 1 circuit consumes the least amount of average energy at both the temperatures.

At 27C, modified 1 circuit consumes the least amount of average energy at both the technology nodes. At 120C also, modified 1 circuit consumes the least amount of average energy at both the technology nodes.

We can observe that as the temperature increases, the average energy consumption decreases. It implies that temperature is inversely proportional to average energy. We can also see that as we increase the technology node, the average energy consumption decreases. It implies that technology node is inversely proportional to average energy.

For 90nm technology node, modified 2 circuit has the least propagation delay at both the temperatures. For 180nm technology node also, modified 2 circuit has the least propagation delay at both the temperatures. At 27C, modified 2 circuit has the least propagation delay at both the technology nodes. At 120C also, modified 2 circuit has the least propagation delay at both the technology nodes.

We can observe that as the temperature increases, the propagation delay increases. It implies that temperature is directly proportional to propagation delay. We can also see that as we increase the technology node, the propagation delay increases. It implies that technology node is directly proportional to propagation delay.

Furthermore, innovative circuits may be created by mixing these circuits and taking use of their benefits.

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