LOW POWER LOW NOISE PLL DESIGN

MAJOR PROJECT

SUBMITTED IN PARTIAL FULFILLMENT OF THE
REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI DESIGN AND EMBEDDED SYSTEMS

Submitted by:

VISHAL AGRAHARI

2K20/VLS/23

Under the supervision of

Prof. J.Panda

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I **Vishal Agrahari** student of M.Tech (VLSI Design and Embedded Systems), hereby declare that the project Dissertation titled "**Low Power Low Noise PLL Design**" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: Delhi **Vishal Agrahari**

Date:

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Report titled "**Low Power Low Noise PLL Design**" which is submitted by **Vishal Agrahari**, **2K20/VLS/23** of Electronics and Communication Department, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi
Date:

Prof. J. Panda
SUPERVISOR

ACKNOWLEDGEMENT

A successful project can never be prepared by the efforts of the person to whom the project is assigned, but it also demands the help and guardianship of people who helped in completion of the project. I would like to thank all those people who have helped me in this research and inspired me during my study.

With profound sense of gratitude, I thank Prof. J Panda, my Research Supervisor, for his encouragement, support, patience and his guidance in this thesis work. Their kind comments and guidance let me complete this study in an improved manner.

I take immense delight in extending my acknowledgement to my family and friends who have been supporting me morally to keep going with this study and inspired me to come up with the expected results throughout this research work.

Vishal Agrahari

ABSTRACT

Traditionally, the PLL has been a linear circuit. While the first PLLs were built with discrete components, they were made available in discrete ICs across 1965. Each of these was linear devices (LPLLs), which were constructed through semiconductor technologies similar to the operational amplifiers of the time. A few years later (around 1970s), the first digital PLLs (DPLLs) became available, however when we look at their schematics, we could see that only the phase detector was built from logic, while the VCO and loop filter remained analog. As a consequence, PLL can be considered of as a hybrid system. Furthermore, we integrate LPLLs and DPLLs into a single class known as mixed signal PLLs.

A PLL is a very versatile device that can be found in most of the devices we use every day. Since its inception, it has been constantly evolving and implemented in various technologies a, whereas the basic phase look loop circuit hasn't changed.. The PLL circuit is broadly utilized communication systems, including, mobile phones, radio, telephone personal computers and electronic devices.

PLLs oftenly finds its uses in mobile or wireless communications for synchronization, clock synthesis, and jitter reduction. A PLL used in a microprocessor to generate clocks appears to be very similar to a frequency synthesizer used in a cell phone, but the actual circuits are designed very different manner.

This report describes the design and the basic concepts of the PLL, along with its operation principle and block diagram, have indeed been explained first. This is based on a detailed explanation and stability analysis of individual blocks in the PLL, which uses negative feedback to achieve phase/frequency lock.

Ltspice is used for the design and implementation, and 90nm technology was used. Simulations of each individual block were described to further explain the function of each individual block, such as the Phase Frequency Detector (PFD), charge pump, Low pass filter (LPF), and Current Starved Voltage controlled Oscillator (CSVCO), as well as the calculation of performance measures such as capture range, lock range, and settling time. Finally the simulation for the complete PLL has been presented along with the calculation of its performance metrics like capture range, lock range and settling time.

CONTENTS

List of Figures

LIST OF TABLES

CHAPTER-1
Introduction to Phase Locked Loops

1.1 Need of PLL

A very simple question arises here that can we have a reference clock generate it on a chip and distribute it across the entire chip. Is it possible?

Answer is Very easy - No, In general it is not possible.

Essentially, the objective is having a reference clock and the frequency of this clock cannot be very high. We already know that we can have a Quartz crystal and crystals have a very high Q (which is called Quality Factor and for the crystals it ranges of 20000 to 100000 and can be above it) thus by virtue they produces a very stable clock signal Q is inversely proportional to bandwidth (W_H - W_L).

Thus we may have a crystal, generate the reference clock and the problem is solved. Actually this is not that easy as it said.

Why not we do this and Why Phase locking is required?

Reasons can be multiple but essential gist of it is:-

Range of frequency cannot be achieved and also crystal cannot produce a very high frequency.

We cannot generate a square wave using a crystal oscillator.

See Crystal is a piezoelectric material which works on the principle of piezoelectricity where the mechanical energy being constantly converted to electric energy and by nature the **mechanical** systems are very slow but they are very perfect. We can emulate a mechanical system to an electrical system or vice-versa but there will be significant difference between speed of operation and size of the system.

Now, if we want to have a high frequency then we essentially needs to multiply the frequencies and to perform a frequency multiplication we need a frequency multiplier which is very accurate on its own. There cannot be skew in output.

For example - if we need to multiply the frequency 10 times than it cannot be 9.8 or 10.2. It should precisely be 10 and the phase of signal should not change quite a lot.

First thing I do need a very perfect frequency multiplier. Second thing is suppose I need to distribute this signal over a large area and off course the periodic nature needs to be maintained.

So the most prominent advantage of a PLL in CMOS technology is it helps to control jitter, the phase of the clock and also it helps to control the frequency. Yes we can control the phase and frequency both. This provides a significant advantage of distributing a low frequency signal easily across the chip.

So the whole idea is - We put a crystal for the reference clock outside the chip, put a PLL with whatever module you want to implement which multiplies the input frequency by N (fixed number) and thus enables us to locally generate those frequencies which are in sync with the main frequency and there is no phase shift or very negligible phase shift which can be ignored hence getting our job done.

1.2 What is a PLL?

A PLL is a circuit that enables one system to track with another. A PLL is a circuit which synchronizes an output signal (generated by the reference oscillator) in both frequency and phase with a reference signal. The phase deviation between the oscillator's output signal and the reference signal is negligible or remains consistent in the synchronized-also known as locked-state.

If the phase error rises, a control mechanism acts on the oscillator to minimize the phase shift to a minimum value. The phase of the control signal is completely locked to the phase of the input/reference signal in such a system. This is why it's called a phase-locked loop.

A Phase-locked loop is a mixed-signal electronic circuit that generates a high frequency output clock. It is a feedback control system that constantly works on the input and the output clock phase relationship to get the desired output frequency. It has wide variety of application in analog, digital and RF communication systems where clocks with high spectral purity are needed.

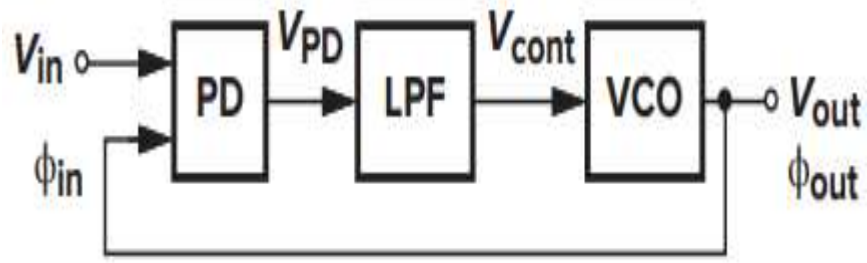


Fig.1.1:- PLL Block Diagram

The Phase Locked Loop (PLL) circuit is composed of three major components:-

1. Phase Frequency Detector (PFD)
2. Charger (CP)
3. The Low Pass Filter (LPF)
4. Oscillator with Voltage Control (VCO)

The PLL circuit is composed of all of these components. PLL layout has undergone numerous changes as a result of its applications. Some blocks are introduced into the loop while others are excluded depending on the circumstances. PLL design is rapidly advancing as they are useful in implementing greater frequencies ranging GHz to instantly latch them. To achieve the desired results, the VCO, which is at the soul of the PLL circuit, has advanced dramatically. To minimize Phase Noise and increase the locking range of the VCO, a resistor is added.

We simply cannot proceed further without knowing the details of these blocks. So the following subsections will have a detailed study of these blocks.

1.2.1 PHASE / FREQUENCY DETECTOR

By Definition: - A phase detector is a circuit whose average output $V_{out}(t)$ is linearly proportional to the phase difference $\Delta\Phi$ between two inputs.Starting from a simple XOR, we want to make a feedback loop which receives the reference frequency and let this be clear that the *amplitude of the reference signal doesn't matter*. So loop receives a frequency then this loop provides a feedback, this frequency is integrated therefore we have phase information, the feedback will give information about the phase of the signal which is available for the system then these two phases are compared at the input of loop and accordingly the loop will adjust itself.

The only difference is the variable is not a voltage, variable is frequency here.

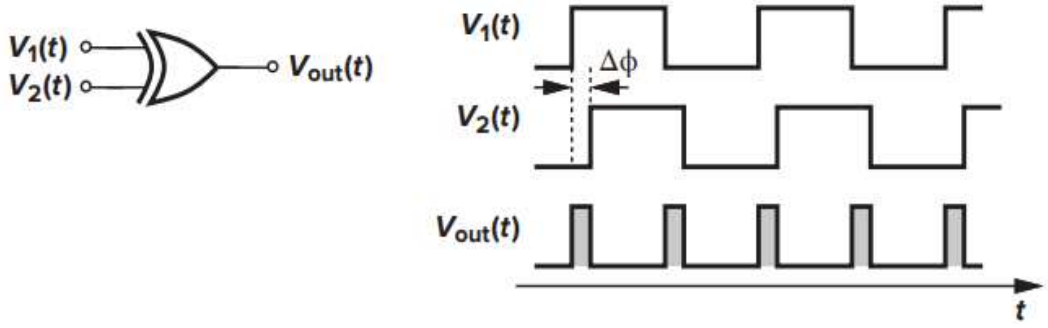


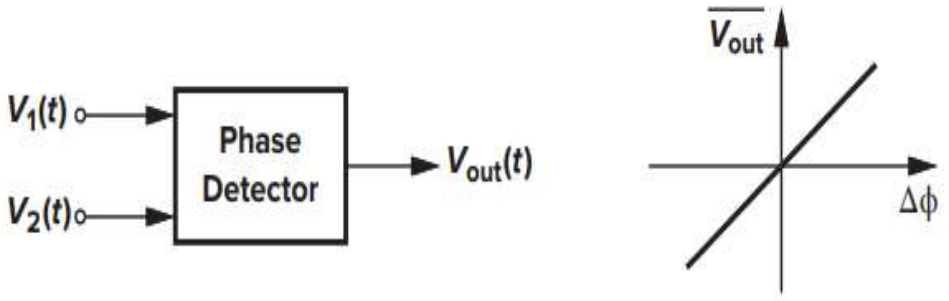
Fig 1.2:- EXOR gate as a Phase Detector

How an XOR can be used a simple phase detector?

XOR as a "Differential Phase Amplifier or Digital Phase Detector".

V_1 (t) *and* ***V_2 (t)*** *are two square wave signals with same amplitude and having a small phase shift denoted by* ***$\Delta\Phi$*** .Based on the phase shift of the two input signals it generates the timing information which is the ***V_{out} (t)*** or ***V_{avg} (t)*** pulse.

So what will XOR do .If there exists a phase shift in between two signals the duty cycle at the XOR output will change as shown in the output in Fig 1.2 and that ***V_{out}(t)*** pulse will have different average output value associated with it. Therefore, I am able to convert phase shift into voltages. Then this voltage information is used to control the phase for the signal.



.

Fig 1.3:- ***V_{out}(t)*** vs. ***$\Delta\Phi$*** plot for a phase detector

In ideal scenarios as shown in Fig 1.3, the relationship between $V_{out}(t)$ and $\Delta\Phi$ is linear across the origin for $\Delta\Phi = 0$.The slope of the $V_{out}(t)$ vs. $\Delta\Phi$ is called the gain of the PD and the slope is expressed in V/rad .

If $V_1(t)$ leading is the phase difference between $V_1(t)$ and $V_2(t)$ is positive and similarly when $V_1(t)$ is lagging phase difference between $V_1(t)$ and $V_2(t)$ is negative as shown in Fig 1.4.

However, the behavior of XOR is not monotonic meaning whether it is lagging or leading XOR cannot judge this. Also if we just have a look over the variation of $V_{avg}(t)$ with the $\Delta\Phi$ considering the amplification of the circuit, the gain is coming out to be sometimes positive and sometimes negative. This will create stability issues in the circuit like if I design my circuit for a positive gain we cannot switch it into negative gain region.

So we could end-up in a situation where the system working for the phase lead might not work for the phase lag or vice-versa.

But we need to remind that - Even though we may consider unstable systems being unworthy but we still use is in our designs because of its regenerative feedback action and also gain of a practical system cannot reach to an infinite value, it saturates over a certain value. And that's how we utilize the behavior of the unstable systems for our purpose.

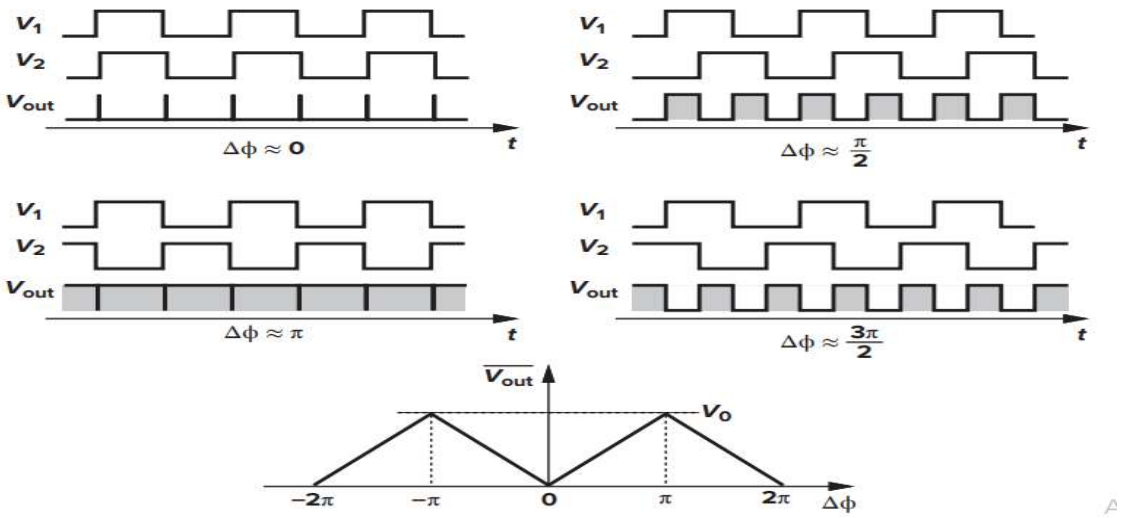


Fig 1 4:- $V_{out}(t)$ vs. $\Delta\Phi$ plot with respect to different phase relation between $V_1(t)$ and $V_2(t)$.

Another possibility seems to be that the loop locks to harmonics of the input signal when a multiplier is used as the phase detector. The PLL code, for example, can lock twice the frequency of the input signal, three times the frequency of the input signal, or just about any multiple. It might get latched to a sub-product of the input signal frequncy. This ***false lock*** will occur whenever the VCO's free running frequency is comparable to a multiple or some multiple of the frequency of the input signal than the real frequency. ***False lock*** can only be prevented by ensuring that the oscillator's free running frequency is closer to the real input frequency than to some multiple or submultiples.
The dilemma of lock accretion in type-1 PLLs has already intensively investigated, but we affirm without evidence that the "acquisition range" is on the order of $\boldsymbol{\omega_{LPF}}$ i.e., the loop latches only if the separation among $\boldsymbol{\omega_{in}}$ and $\boldsymbol{\omega_{out}}$ is close to $\boldsymbol{\omega_{LPF}}$. The issue of lock accretion further complicates the quid pro quo in type-1 PLLs. When the LPF is minimized, the acquisition range is scaled down to reduce the control voltage ripple.

To overcome this drawback, PFDs are used in PLLs. PLLs based on such phase comparator have a lot of beneficial characteristics. Firstly, they do not exhibit a false lock. Second, whenever the system is locked, the input signal and the oscillator output waveforms are accurately in phase, even if the input frequency is not the same as oscillator's free running frequency. Eventually, the PLL achieves lock rapidly even when the input frequency is considerably different from the oscillator's free running frequency.

The PFD block, Fig 1.5, tracks the phase and frequency of the reference clock and the divided clock. It generates two pulses, UP and DN, based on the phase difference between the two incoming signal (error signal). When the frequencies of the two inputs become the same and the error signal acquires a small constant value over time, the PLL accomplishes a lock.

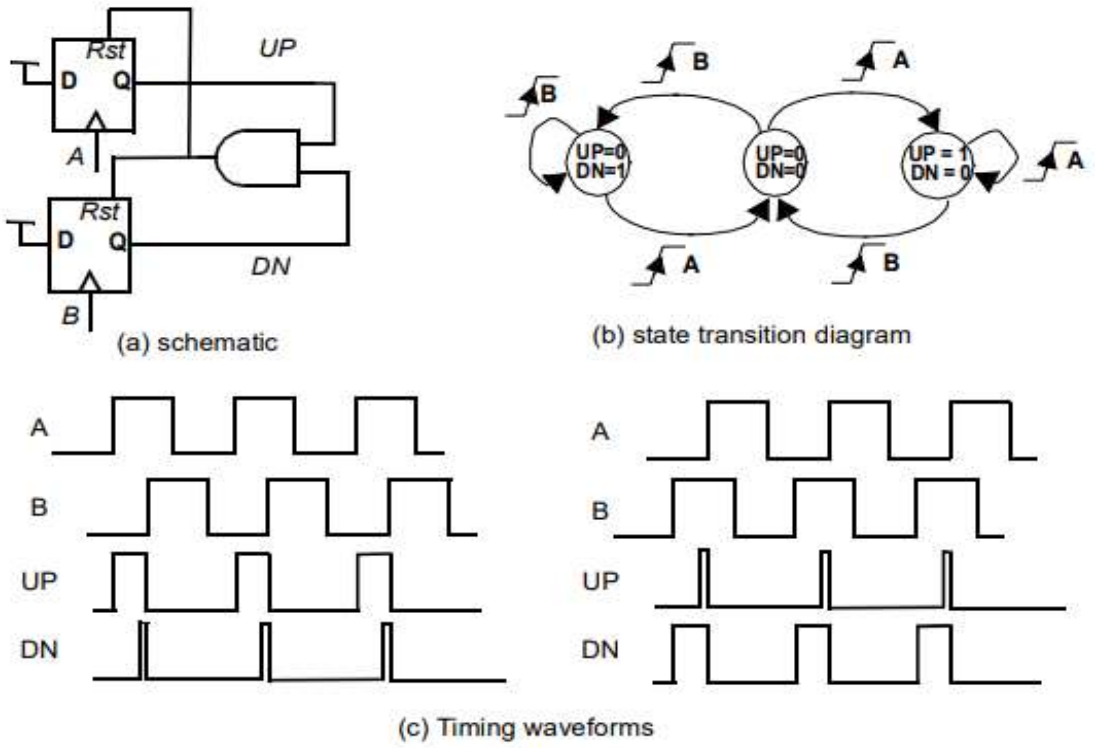


Fig 1.5:- Phase Frequency Detector (a) Schematic (b) Transition Diagram (c) Timing Waveform

The PFD is a three-state state machine. Suppose that the ***UP*** and **DN** outputs are both low initially. Once input A precedes input B, the **UP** output is asserted on input A's positive edge. The **UP** signal will continue to stay in this state unless there is a low-to-high transition on input B. The **DN** output is asserted at around that time, causing both flip-flops to reset through the asynchronous reset signal. On the ***DN*** signal, a relatively brief pulse proportional to the phase difference is generated, and there is a narrow pulse on the ***DN*** output with a duration equal to the delay through the AND gate and register reset delay.

On the DN signal, a short pulse proportional to the phase difference is produced, and there is a limited pulse on the DN output with just a duration equal to the delay through the AND gate and register reset delay. The UP pulse's pulse width equals the phase difference between the two signals. When input B lags behind input A, the situation is reversed, and a pulse proportional to the phase difference is produced on the DN output. Short pulses will be obtained on the UP and DN outputs if the loop is locked.

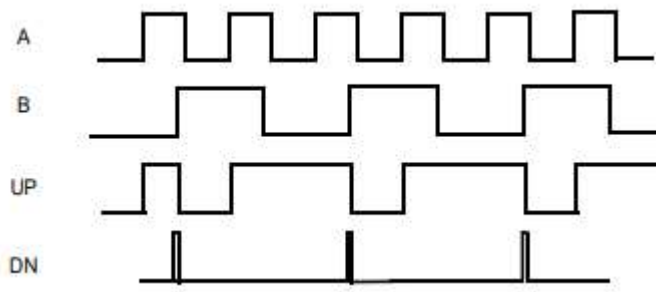


Fig 1.6:- Timing of PFD measuring frequency error

1.2.2 CHARGE PUMP

To mitigate the bounded phase inaccuracy encountered in type-I Locked Loops, we really would like to increase the gain of the loop to almost infinity, probably using an integrator. As our first step, we interpose a "***charge pump***" (CP) between the PFD and the loop filter. A charge pump is comprised of two switched current sources that pump charge into or out of a loop filter based on two logical inputs i.e., UP and DN signals. Fig 1.7 depicts a Charge Pump circuit powered by a Phase Frequency Detector and driving a capacitor.

The charge pump converts the ***UP and*** **DN** input pulses coming from PFD into current pulses that charge/discharge the Loop Filter to give the desired control voltage (***Vctrl***).

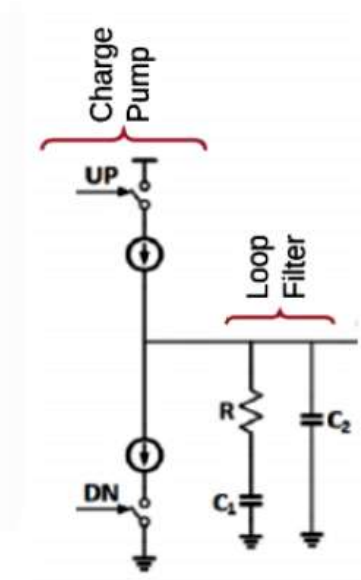


Fig 1.7:- Basic Charge Pump schematic

The operation can be understood in detail with the help of the following waveforms

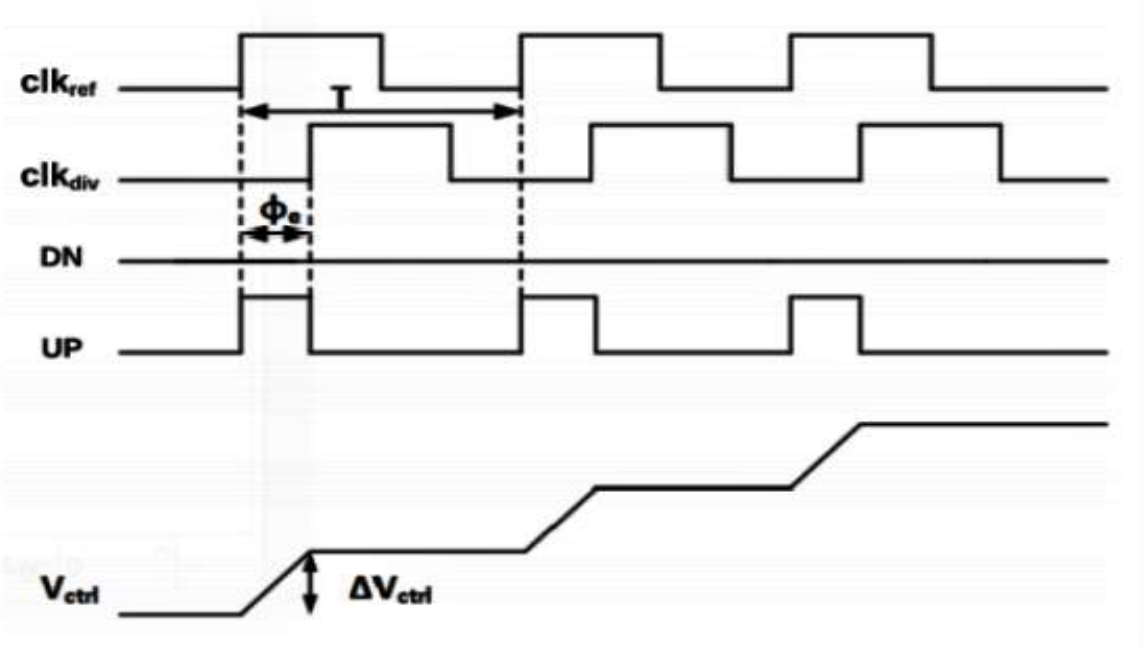


Fig 1.8:- Charge Pump Waveform

Due to a phase difference between ***clkref*** and ***clkdiv*** signals, PFD produces UP and DN pulses as shown in the waveforms. Since ***clkref*** leads ***clkdiv***, UP pulse goes high. This causes the UP current to dump charge into the Loop Filter capacitor and hence increase ***Vctrl(t)***. Thus ***Vctrl(t)*** increases as long as ***clkref*** leads ***clkdiv***.

1.2.3 LOOP FILTER

The loop filter is very important for lock acquisition, phase/frequency tracking and noise filtering. The Low Pass Filter is used to remove out the PFD's high frequency components, allowing only lower frequency components to pass through. It produces a direct current voltage that controls the output. The output frequency of the voltage controlled oscillator is determined by this DC voltage. The LPF output is fed into the VCO as an input.

The loop filter circuit discussed in thesis is a low-pass filter consisting of two capacitors and a resistor as shown in Fig 1.9 shown below.

Resistor, ***R***, introduces a zero and capacitor, C_1, adds a pole to system function such that it is stable in the desired frequency realm. Capacitor, C_2, reduces V***ctrl (t)*** ripple but works against ensuring the stability of the system. The values of R, C1 and C2 are

chosen to have optimum stability and good high frequency noise rejection. Ideal the value of C_2 capacitor should be $1/5^{th}$ to $1/10^{th}$ of the C_1 capacitor.

Working of the loop filter: -

It transforms digital error pulses from the PFD's output to analog error currents. The charge pump is composed of switched a current source which charges the capacitor and generate the corresponding voltage. The current sources and switches are accomplished using PMOS and NMOS transistors. PMOS and NMOS serve as current sources and therefore are biased to function in the saturation mode. PM0 and NM0 are used to implement the switches. The ***UP*** output is forwarded through the inverter, which is linked to the PMOS switch (PM0). The output ***DN*** is forwarded through a transmission gate to reimburse for the gate delay caused by the inverter before even being fed into the NMOS switch (NM0). The charge pump input variables can be in one of three states. If ***UP*** and ***DN*** are both zero, both PM0 and NM0 are turned off, but the control voltage across the capacitor remains unchanged. If ***UP*** is high and ***DN*** is low then PM0 is one and PM1 charges the capacitor increasing the control voltage. If ***DN*** is high, NM0 is turned on, and NM1 discharges the capacitor. Because both ***UP*** and ***DN*** are on for such a short period of time, any imbalance in current flow through PM0 and NM0 during this time produces ripple effects in the control voltage.

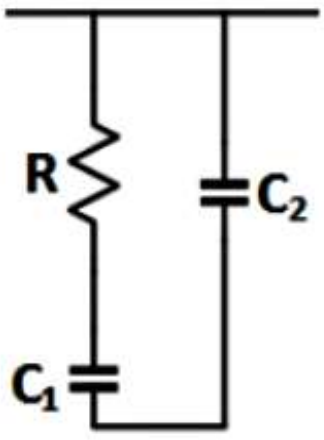


Fig 1.9:- Loop Filter Circuit

The transfer function for this filter is given by-

$$F(s) = \frac{s + \frac{1}{RC_1}}{C_2 s\left(s + \frac{C_1 + C_2}{RC_1C_2}\right)}$$

..... 1.1

1.2.4 VOLTAGE CONTROLLED OSCILLATOR

The very first step in constructing a voltage controlled oscillator is to realize an oscillator and then add a means for trying to control its frequency of oscillation through the use of input voltage, but in some cases the control signal could be a current. Oscillators are categorized into two categories: those that produce pure sine wave outputs explicitly and those that produce square wave outputs. Sinusoidal output oscillators are typically realized using a feedback frequency selective or tuning circuit, whereas square wave output oscillators are typically actually realized using a nonlinear circuit such as a relaxation oscillator or ring counter.

An ideal VCO block generates a periodic output whose frequency out is a linear function of input control voltage $V_{ctrl}(t)$. The plot below shows the linear relationship-

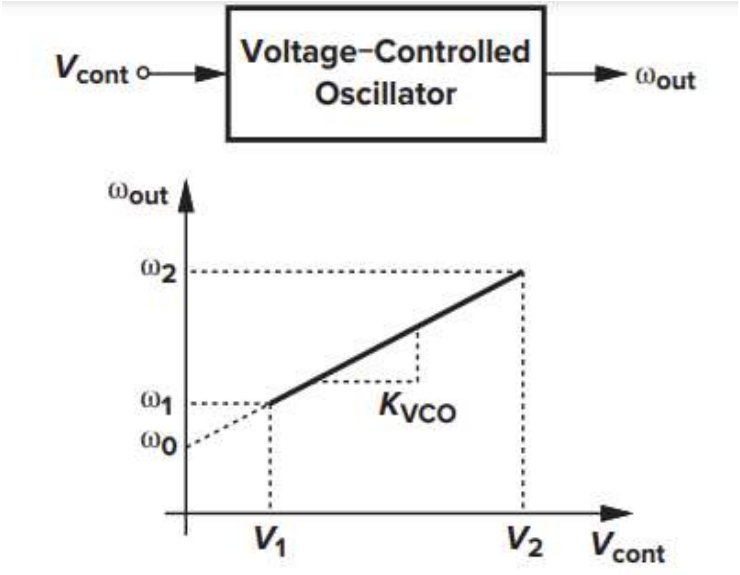


Fig 1.10:- Frequency vs. Voltage plot of an Ideal VCO

The linear relationship can be described by the equation:-

$$\omega_{out} = \omega_0 + K_{VCO} \text{ x } V_{cont} \quad \text{.....1.2}$$

Here, ω_0 represents the intercept corresponding to $V_{cont} = 0$ also called the "**Free running frequency**" and K_{VCO} denotes the "**gain**" or "**sensitivity**" of the circuit (expressed in rad/s/V). The achievable range, $\omega_2 - \omega_1$, is called the "**tuning range**."

As the phase is the time integral of the frequency, the phase output of the VCO block is given by:-

$$\phi_{out} = \omega_0 t + K_{vco} \cdot \int_{-\infty}^{t} v_{cont} dt \quad \text{.....1.3}$$

The VCO is one of the main contributors to jitter in the output clock, so the topology needs to be chosen carefully according to specification. The two broad categories of VCOs are Ring oscillators and LC tank oscillators. LC oscillators offer lower jitter than ring oscillators but occupy more on-chip area.

CHAPTER-2
Study of PLL behavior under Phase and Frequency Transience

Basic PLL has a ***phase detector*** to generate the phase difference information to an equivalent voltage levels. An LPF (Low Pass Filter) to deduce the average value of the output voltage and we also need some module to convert this voltage to an equivalent frequency value which is performed by non-other than a VCO (Voltage Control Oscillator).

Output of a VCO can actually be ω i.e. frequency or ωxt i.e. phase anyway both of these are interrelated hence both are correct. Therefore, I have a VCO whose output will have a phase which is changing with time and input signal is also variable with time.

Suppose I have a periodic signal with frequency ω_0 hence its phase is $\omega_0 t$ therefore the phase is changing linearly with time.

Suppose my loop is locked the VCO will generate the frequency ω_0 and the static phase of $V_1(t)$ is also zero, making the phase difference between $\mathbf{V_1(t)}$ and $\mathbf{V_2(t)}$ to be zero. 'Or' I can have two linearly varying phase such that there phase difference is also zero.

See we can't say that we have phase information but don't have frequency information. This sounds illogical. Phase and frequency are two sides of a coin.

Question may arise here, *why I need to compare two phases? Can't we simply perform the frequency comparison?*

Off course yes frequency comparisons can also be performed, the loop will have go to a locking position if those two frequencies are close to each other and there exists a constant phase difference between them. Let's just prove it mathematically,

2.1 Frequency Transience:-

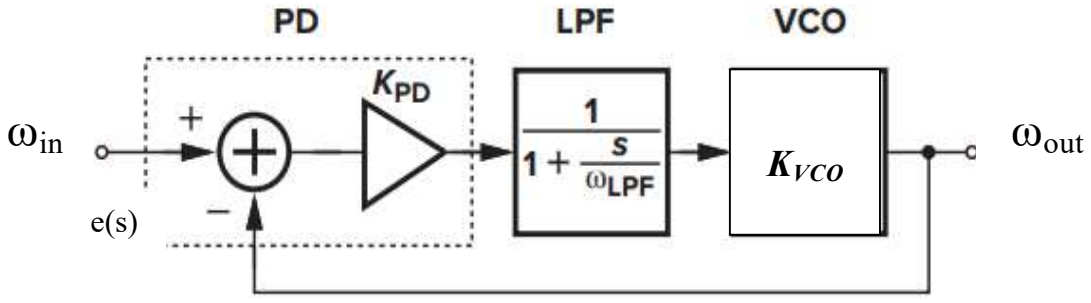


Fig 2.1:- Block Diagram of a PLL circuit where frequency is feed to the comparator

$$\frac{e(s)}{fin(s)} = \frac{1}{1+\beta(s)G(s)}$$

.....2.1

where, e(s) = $fin(s) - fout(s)$, that is the error between input and output frequency G(s) is the forward path loop gain; β(s) is the feedback factor. From the block diagram shown in the Fig 2.1,

$$\frac{e(s)}{fin(s)} = \frac{1}{1+\frac{K}{1+\frac{S}{P}}}$$

.....2.2

$K = K_{vco} \times K_{PD,}$ is the D.C. gain and P is the pole of the system.

Now suppose, there occur a step change in the input frequency Δf_e .

Taking its Laplace transforms;

$$fin(s) = \frac{\Delta f0}{s}$$

.....2.3

Now,

$$e(s) = \frac{\Delta f0}{s} \times \frac{1}{1+\frac{K}{1+\frac{S}{P}}}$$

.....2.4

Solving this equation, we will get;

$$e(t) = \frac{f0}{(1+k)}u(t) + \frac{K}{P(1+K)^2}e^{-t\ (t+1)}u(t)$$

.....2.5

At steady state, the exponential component will vanish; we will be still left with,

$$e(t) = fin(s) - fout(s) = \frac{f0}{(1+k)}u(t)$$

.....2.6

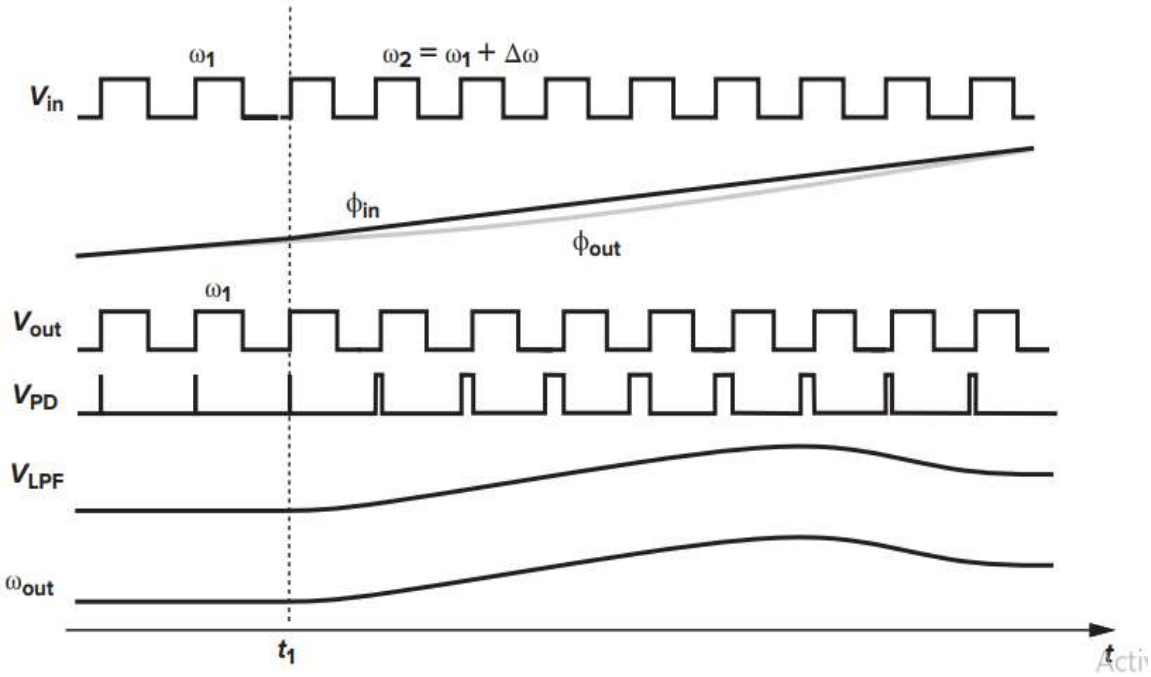


Fig 2.2:- Response of PLL for small frequency step

PLL response to a small frequency step input at $t = t_1$. Still, the VCO persists to oscillate at ω_1 instantly after t_1 because the voltage across the capacitor cannot be changed at an instant. As a result, the PD produces extremely broad pulses as well as $V_{LPF}(t)$ increases over time. As ω_{out} approaches $\omega_1 + \Delta\omega$, the width of the PD pulses reduces, finally settle downs to a level which generates a DC offset equivalent to $\frac{(\omega 1 + \Delta\omega - \omega 0)}{KVCO}$. In comparison to a phase step, *a PLL's answer to a step frequency involves a radical shift in both the voltage and the phase steps*.

Hence, it can be concluded from the above derivation that while performing the frequency comparison rather than phase there always occurs an error at the steady state which is inversely proportional to the loop gain.

2.2 Phase Transience:-

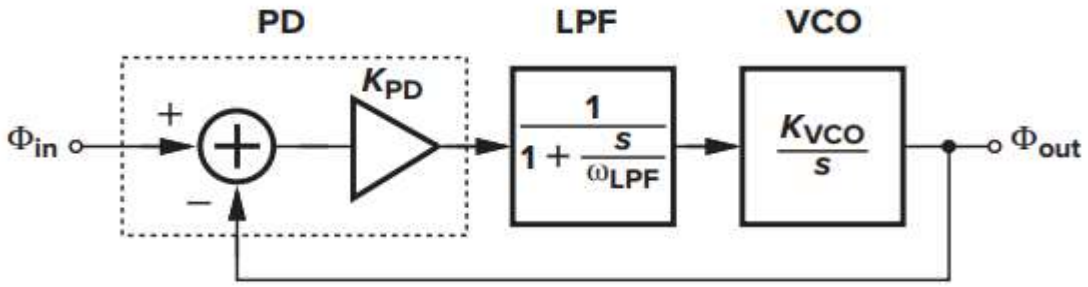


Fig 2.3:- Block Diagram of a PLL circuit where phase is fed to the comparator

$$\frac{e(s)}{\Phi in(s)} = \frac{1}{1+\beta(s)G(s)}$$

.....2.7

Now, let's just do all of this for the phase detector in spite of frequency detector.

where, e(s) = $\Phi in(s) - \Phi out(s)$, that is the error between input and output phase. G(s) is the forward path loop gain; β(s) is the feedback factor. From the block diagram shown in the Fig 2.3,

$$\frac{e(s)}{fin(s)} = \frac{1}{1+\frac{1}{S}\times\frac{K}{1+\frac{S}{P}}}$$

.....2.8

$K = K_{vco} \times K_{PD,}$ is the D.C. gain and P is the pole of the system.

Now suppose, there occur a step change in the input frequency $\Delta\Phi_e$.

Taking its Laplace transforms;

$$\Phi in(s) = \frac{\Delta\Phi 0}{s}$$

.....2.9

Now,

$$e(s) = \frac{\Delta\Phi 0}{s} \times \frac{1}{1 + \frac{1}{S} \times \frac{K}{1 + \frac{S}{P}}}$$

.....2.10

Even without solving this equation, we can deduce that the steady state error of the above described system is zero because it is a type-1 system, because of the open loop pole at origin, *error of a type-1 system for step input at steady state is zero*.

Therefore, at steady state, $e(s) = \Phi in(s) - \Phi out(s) = 0$

Since,

$$\omega = \frac{d\Phi}{dt}$$

.....2.11

$$\frac{d\Phi in(t)}{dt} - \frac{d\Phi out(t)}{dt} = 0$$

.....2.12

$$\omega in(t) - \omega out(t) = 0$$

.....2.13

$$\omega in(t) = \omega out(t)$$

.....2.14

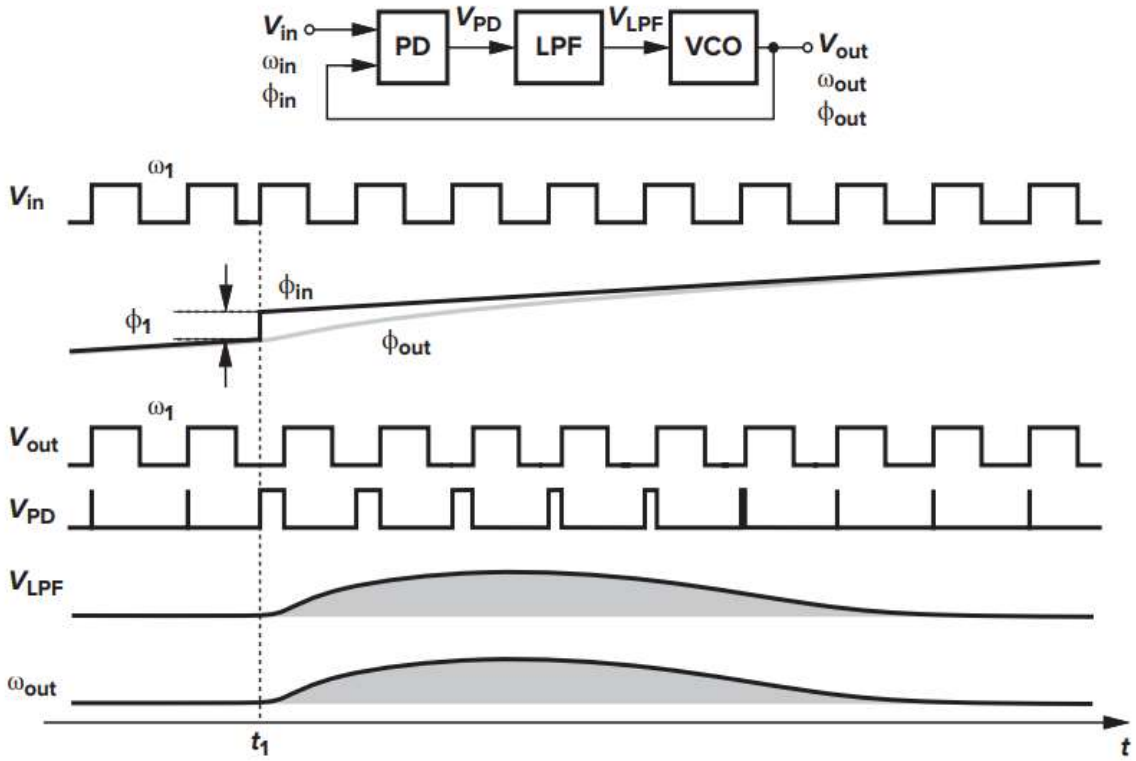


Fig 2.4:- Response of a PLL for phase step

As shown in Fig 2.4, suppose the input has a phase step of Φ_1 at $t = t_1$, i.e., $\Phi_{in} = \Phi_1(t) + \Phi_1 u(t-t_1)$. The phase step does seem to be a positive edge in ***Vin (t)*** that occurs earlier (or later) than the periodicity suggests. The phase step, on the other hand, causes a contraction (or lengthening) of the duration well before t1. The VCO initially oscillates at ω_1 because the LPF output does not change immediately. The increasing phase shift between input and output generates broad pulses at the PD's output, causing VLPF to gradually increase. As a result, the VCO frequency starts to vary in an effort to minimize phase shift. Because the phase error varies over time, the loop does not get locked during the transient.

In case the loop comes back to lock state, ω_{out} must eventually returns to ω_1, which needs V_{LPF} and therefore $\Phi out - \Phi in$ also return to their actual values. The disparity in the output frequency of VCO is such that the area under ω_{out} provides an access phase of $\Phi 1$ in Φout because Φ in has changed by Φ1. As

$$\int_{t1}^{\infty} woutdt = \boldsymbol{\Phi}1$$

.....2.15

All variables (except the total input and output phases) revert to their initial values when the loop returns to the lock state. That is, the $\boldsymbol{\Phi_{in}}$-$\boldsymbol{\Phi_{out}}$, $\boldsymbol{VCO}$, and $\boldsymbol{V_{LPF}}$ frequencies stay intact expected result considering that all these three variables have a one-to-one correlation and the input frequency stays constant.

Two observations highlight the significance of this property. In certain applications, even a really small (deterministic) frequency inaccuracy may be unacceptable. For example, if a digital signal is to be processed simultaneously by a clocked system, a subtle change in data rate and operating frequency may end up causing "drift," which causes errors. Aside from that, if the PLL tried to compare input and output frequencies instead of phases, the equality would simply not exist. A loop using a frequency detector (FD) would have a finite difference between in and out due to mismatches and other non-idealities.

CHAPTER-3
Dynamics of type-I PLLs and CP-PLLs

The only justification for including this chapter is to provide an in-depth examination of the PLL's behaviour and attitude. In this chapter, we will look at the mathematical model between input phase and output phase for the open-loop and closed-loop systems, as well as the behaviour of the system in time domain.

Why $\boldsymbol{\Phi_{out}(s) / \Phi_{in}(s)}$ hold so much significance?

Reason being, it reveals whether the output phase tracks the input phase slowly or rapidly.

3.1 Dynamics of type-I PLLs

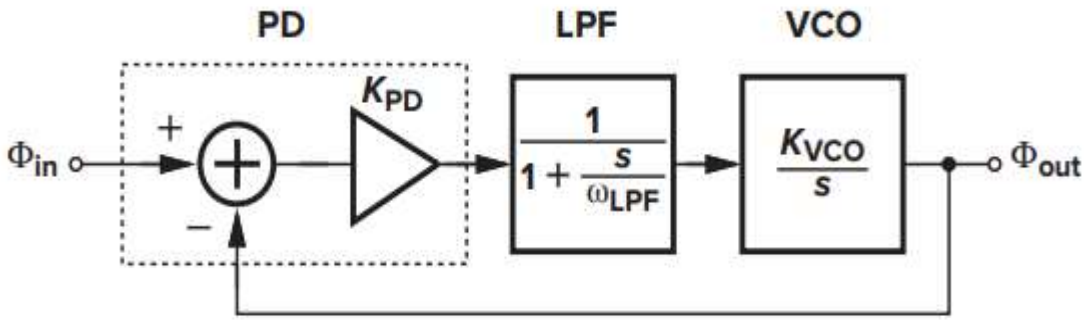


Fig 3.1:- Block Diagram of a PLL circuit

Let's just consider a model of a PLL which is linear, consider a 1st order low pass filter for the sake of simplicity in the analysis.

The Phase Detector output contains a dc component equal to $\boldsymbol{K_{PD}(\Phi_{in} - \Phi_{out})}$ as well as the higher frequency components. This output is fed to the next block which is an LPF. The LPF will eliminate the high frequency component and allows only the DC components to pass. This simple looks like both the PD and the LPF in a combine way works like an "subtractor" circuit.

Before starting the whole analysis it must be made clear that in following cases $\boldsymbol{\Phi_{in}}$ & $\boldsymbol{\Phi_{out}}$ are the excess phase in the input and output respectively because anyway we will be getting the $\boldsymbol{V_{PD}(t)}$ which will be proportional to the phase difference only.

For the block diagram shown in Fig 3.1, the open loop transfer function can be given as:-

$$H(s) = \frac{\Phi out(s)}{\Phi in(s)} | open = Kpd. \frac{1}{1 + \frac{s}{\omega LPF}} . \frac{Kvco}{S}$$

.....3.1

The equation (1) reveals that, the open loop system has two poles one at s=0 and other at s=$\omega_{LPF.}$ Since at the origin for the open loop system there exist a pole, such systems also called type-I system.

The equation (1) reveals that, the open loop system has two poles one at s=0 and other at s=$\omega_{LPF.}$ Since at the origin for the open loop system there exist a pole, such systems also called type-I system.

In the above equation, it can be seen at as s →0, the gain of the system moves to infinity. This can be interpreted as if the excess phase of the input varies slowly, the loop will ensure that the input phase change $\boldsymbol{\Phi_{in}}$ will exactly matches with output phase change $\boldsymbol{\Phi_{out}}$.

In a similar way, closed loop equation can be derived as:-

$$F(s) = \frac{\Phi out(s)}{\Phi in(s)} | closed = \frac{Kpd\ .Kvco}{\frac{S^2}{\omega LPF} + S + Kpd\ .Kvco}$$

.....3.2

Since,

$$\omega = \frac{d\Phi}{dt}$$

.....3.3

Equation (3.2) can also be interpreted as :-

$$\frac{\omega out(s)}{\omega in(s)} | closed = \frac{Kpd\ .Kvco}{\frac{S^2}{\omega LPF} + S + Kpd\ .Kvco}$$

.....3.4

This outcome indicates that only if ***ωin*** changes very slowly ***(s → 0)***, then ***ωout*** tracks ***ωin***, that is another expected outcome because the loop is believed to be locked. Also itindicates that if ***ωin*** varies sharply and the system is provided sufficient time to relax i.e. ***(s→ 0),*** the variation in ***ωout*** equalise the variation in ***ωin.***

Comparing the equation (4) with the standard second order system equation shown below:-

$$F(s) = \frac{\omega n^2}{s^2 + 2\Sigma\omega n s + \omega n^2}$$

…..3.5

Let's assume that, K = $Kpd\,.Kvco$. We have

$$\omega n = \sqrt{\omega LPF \;\; \times K}$$

…..3.6

$$\Sigma = \frac{1}{2}\sqrt{\frac{\omega LPF}{K}}$$

…..3.7

Also, the damping factor, from above relations,

$$\alpha = \Sigma\omega_n = \frac{1}{2}\omega\mathrm{LPF}$$

…..3.8

α is a critical parameter to define the speed of the closed loop system i.e. settling time of the closed loop system is inversely proportional to α.Lower the value of $\omega_{LPF,}$ lesser will be the high frequency components however the system will gets slower and require more time to settle down.

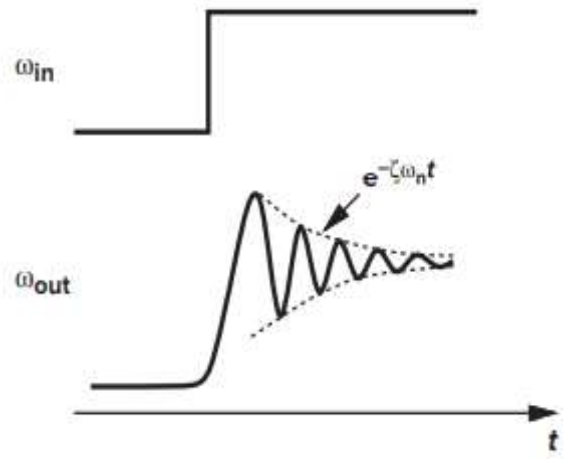


Fig 3.2:- Variation in ω_{out} with time because of transience in ωin

Also, to avoid excessive ringing in the output waveform, Σ is chosen between $\frac{1}{\sqrt[2]{2}}$ and 1.

3.2. Dynamics of Charge Pump PLLs:-

To estimate the behaviour of chage-punp PLLs, we generate a liner model that incorporates PFD, charge pump, and the low-pass filter, yielding the transfer function.

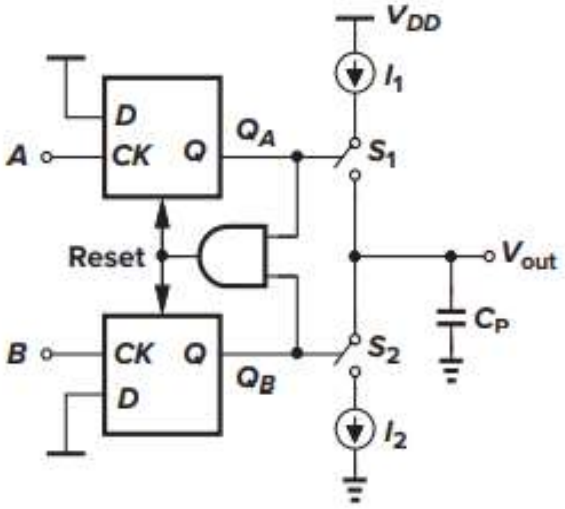


Fig 3.3:- PFD circuit along with charge pump and low pass filter

Question arise here is - Does the combined PFD+CP+LPF circuit shown in Fig 3.3 a linear system?

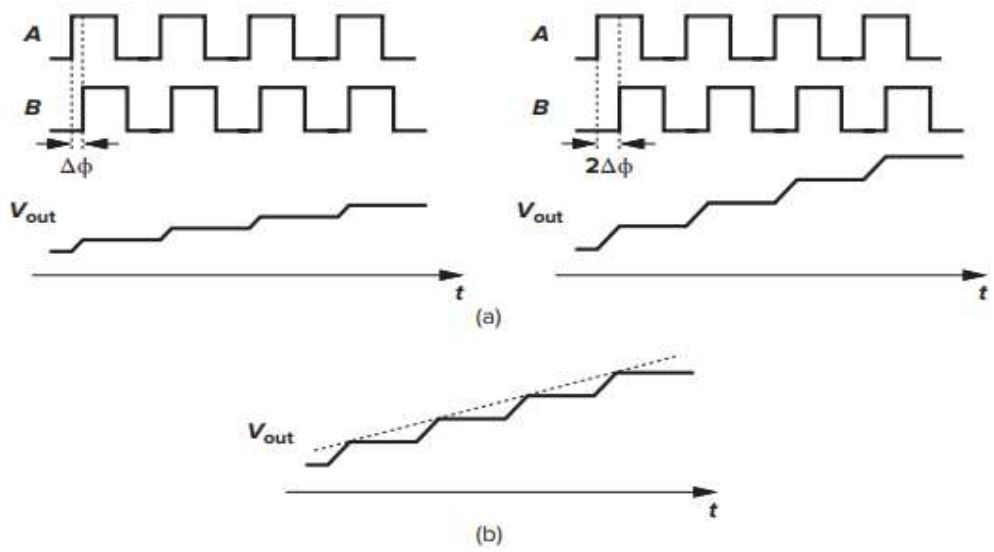


Fig 3.4:- (a) linearity test of the combine block (b) Response approximation

To put it in simple terms, we run the system through a linearity test. As shown in Fig 3.4, We have doubled the input phase shift and will see if Vout as well doubles. Surprisingly, Vout's flat sections get double but the ramp segment remains the same. This is because of the current charging or discharging capacitor C_P is stable, the ramp has a constant slope. As a consequence, the system is not strictly linear.

To solve this dilemma, we will be using a ramp to estimate the output waveform a ramp signal shown in Fig 3.4 (b), resulting in a direct interdependence between ***Vout*** and phase ***Φ***.

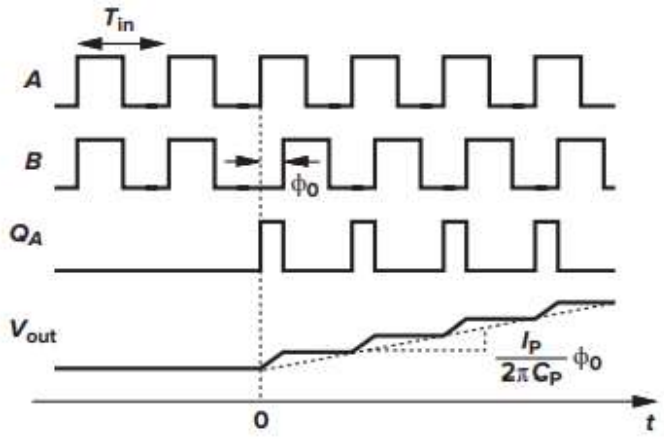


Fig 3.5:- Behaviour of PFD+CP+LPF combination under step input

Let's suppose the input period is Tin and the charge pump circuit delivers an $\pm I$p current to the capacitor. As illustrated in Fig 3.5, we starts with a phase shift of zero radian and, at t = 0, the phase of step signal B by Φ0, i.e., = Φ0u (t). As a consequence, Q_A or QB

continues to generate pulses of Φ0Tin/(2x $\boldsymbol{\pi}$) seconds width, raising the output voltage by (IP/CP) x Φ0Tin/(2 $\boldsymbol{\pi}$) for each period.

Thus, ***Vout(t)*** can be expressed as

$$\boldsymbol{Vout(t) = (I_P/C_P)\ x\ \Phi_0 Tin/\ (2\ \pi\ )}$$

…..3.9

The impulse response is therefore given by:-

$$\boldsymbol{h(t)\ = \frac{Ip}{2\pi Cp} u(t)}$$

…..3.10

Yielding the transfer function,

$$\boldsymbol{\frac{Vout(s)}{\Delta\Phi} = \frac{Ip}{2\pi Cp} . \frac{1}{S}}$$

…..3.11

Consequently, the PFD/CP/LPF combination contains a pole at the origin, a point of contrast to the PD/LPF circuit used in the type-I PLL. In analogy with the expression K_{VCO} /s, we call I_P /(2πC_P) the "gain" of the PFD and denote it by K_{PFD}.

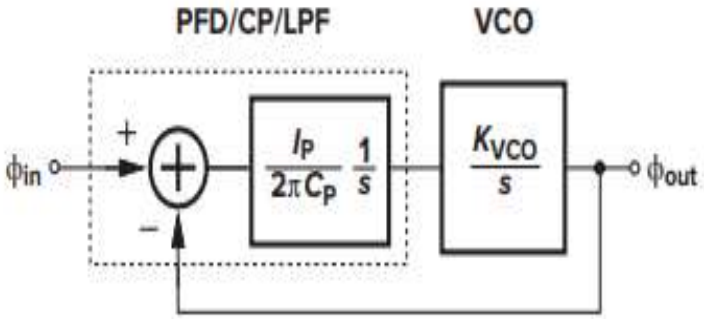


Fig 3.6:- Frequency domain modelling of charge pump PLL

Let's build a linear model of charge-pump PLLs now. The prototype, as shown in Fig 3.6, provides an open-loop transfer function.

$$\frac{\Phi out(s)}{\Phi in(s)} |open =. \frac{Ip}{2\pi Cp} . \frac{Kvco}{S^2}$$

....3.12

This topology is referred to as a "type II" PLL because the loop gain has two poles at the origin. The closed-loop transfer function, abbreviated H(s), is thus equal to

$$\frac{\Phi out(s)}{\Phi in(s)}|closed = \frac{\frac{Ip.Kvco}{2\pi Cp}.}{S^2 + \frac{Ip.Kvco}{2\pi Cp}}$$

....3.13

This outcome is concerning reason being the closed-loop system has two non-real poles. at $s1,2 = \pm j \sqrt[2]{Ip\ Kvco\ /(2\pi Cp)}$ and is therefore unstable.
To improve the stability, we must modify the phase aspect such that the phase shift at the gain crossover is less than 180. This would be accomplished, as shown in Fig 3.7, by incorporating a zero in the loop function, i.e., by integrating a resistor in series with the loop filter's capacitor.

The combined PFD+CP+LPF circuit now has a transfer function,

$$\frac{\boldsymbol{Vout(s)}}{\boldsymbol{\Delta\Phi}} = \frac{\boldsymbol{Ip}}{\boldsymbol{2\pi}}.(\boldsymbol{Rp} + \frac{\boldsymbol{1}}{\boldsymbol{SCp}})$$

....3.14

Open-loop transfer function for the PLL design is equal to,

$$\frac{\boldsymbol{\Phi out(s)}}{\boldsymbol{\Phi in(s)}}|\boldsymbol{open} =. \frac{\boldsymbol{Ip}}{\boldsymbol{2\pi}}.\frac{\boldsymbol{Kvco}}{\boldsymbol{S}}(\boldsymbol{Rp} + \frac{\boldsymbol{1}}{\boldsymbol{SCp}})$$

....3.15

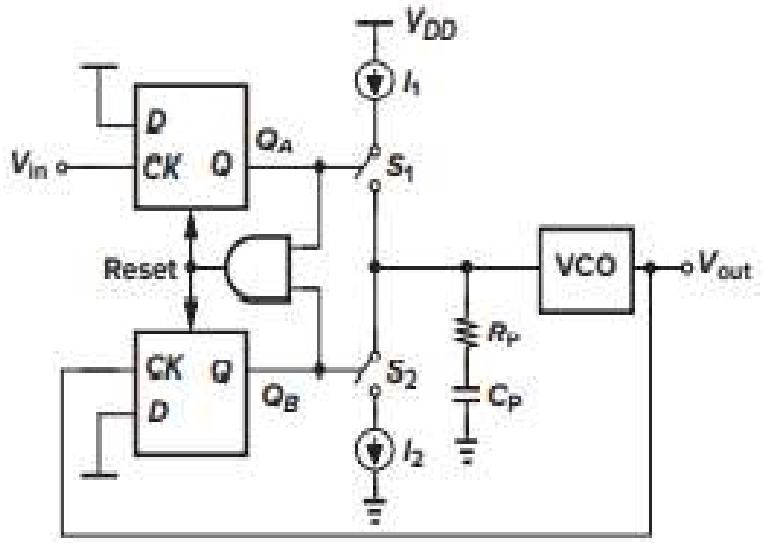


Fig 3.7:- Charge-pump PLL circuit with an added resistor for the zero addition

And hence,

$$F(s) = \frac{\Phi out(s)}{\Phi in(s)} | closed = \frac{\frac{Ip}{2\pi} . \frac{Kvco}{Cp} (SCpRp + 1)}{S^2 + \frac{Ip}{2\pi} Kvco. RpS + \frac{Ip}{2\pi} . \frac{Kvco}{Cp}}$$

....3.16

$$\omega n = \sqrt[2]{\frac{Ip}{2\pi} . \frac{Kvco}{Cp}}$$

....3.17

$$\Sigma = \frac{Rp}{2} \sqrt{\frac{Ip}{2\pi} Kvco. Cp}$$

....3.18

If Rp = 0, then, as expected, Σ= 0. The decay time constant for complex poles is given by ***1/(ζωn) = 4π/(Rp Ip Kvco).***

If Rp = 0, then, as expected, Σ= 0. The decay time constant for complex poles is given by ***1/(ζωn) = 4π/(Rp Ip Kvco).***

Fig 3.7 shows a critical flaw in the compensated type-II PLL. When a current is injected into the loop filter, the control voltage jumps dramatically because the charge pump drives the series combination of Rp and Cp.Even when the circuit is locked, voltage jumps in Vcont are caused by the imbalance between I_1 and I_2, as well as the charge injection and clock feed through of S1 and S2. The resulting ripple heavily perturbs the VCO, exacerbating the corrupted output phase.

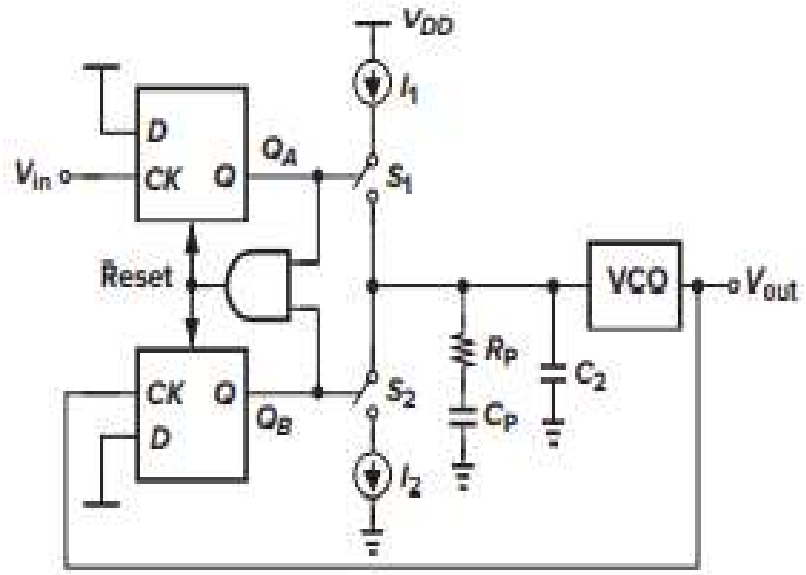


Fig 3.8:- Capacitor C2 is added to reduce ripple on the control line.

To tackle this question, a second capacitor is normally connected in parallel with Rp and Cp in Fig 3.8, curbing the initial step. The loop filter is now of second order, resulting in a third-order PLL and instability issues. Even if C2 is chose between one-fifth to one-tenth of Cp, the closed-loop time and frequency responses remain constant.

CHAPTER-4
Non-ideal Effects in PLL

4.1. PFD/CP Non-idealities

4.1.1 Reset Delay of PFD:-

Even when the phase difference between the inputs is zero, the PFD implementation in Fig 1.5 generates narrow, coincident pulses on both QA and QB. As shown in Fig 4.1, if A and B start rising at the very same time, so do QA and QB, triggering the reset. That is, even when the PLL is locked, QA and QB turn on the charge pump synchronously for a predefined timeframe TP ≈ 5TD, where TD signifies the gate delay.

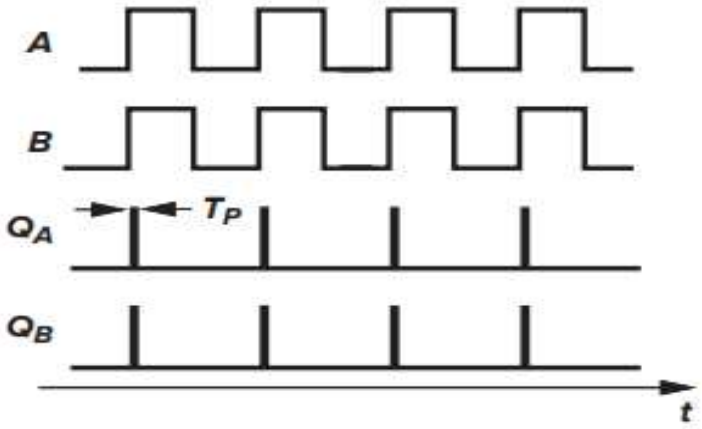


Fig.4.1- PFD-generated collinear pulses with zero phase shift.

What impact do the reset pulses have on QA and QB? Consider a purely theoretical Fig 4.2 (a) shows a PFD that creates no pulses for a zero input phase shift. What is the PFD's response to a small phase error? Fig 4.2(b) shows how the circuit generates very narrow pulses on QA or QB.

Nevertheless, due to the finite rise and fall times prompted by capacitance at these nodes, the pulse wouldn't have enough time to achieve a logical high level and thus will fail to turn on the charge pump switches. In other words, if the input phase shift exceeds the threshold value of, the output voltage of Φ, the PFD/CP/LPF combination circuit is no longer a function of Φ0. Because the charge pump injects no current for $|\Delta\Phi| < \Phi 0$, as shown in Fig 4.3, the loop gain falls to zero as well as the output phase is not locked. The PFD/CP circuit appears to have a dead zone equal to $\pm \Phi 0$ around $\Delta\Phi = 0$.

Nevertheless, due to the finite rise and fall times prompted by capacitance at these nodes, the pulse wouldn't have enough time to achieve a logical high level and thus will fail to turn on the charge pump switches. In other words, if the input phase shift exceeds the threshold value of, the output voltage of Φ, the PFD/CP/LPF combination circuit is no longer a function of Φ0. Because the charge pump injects no current for $|\Delta\Phi| < \Phi 0$, as shown in Fig 4.3, the loop gain falls to zero as well as the output phase is not locked. The PFD/CP circuit appears to have a dead zone equal to $\pm \Phi 0$ around $\Delta\Phi = 0$.

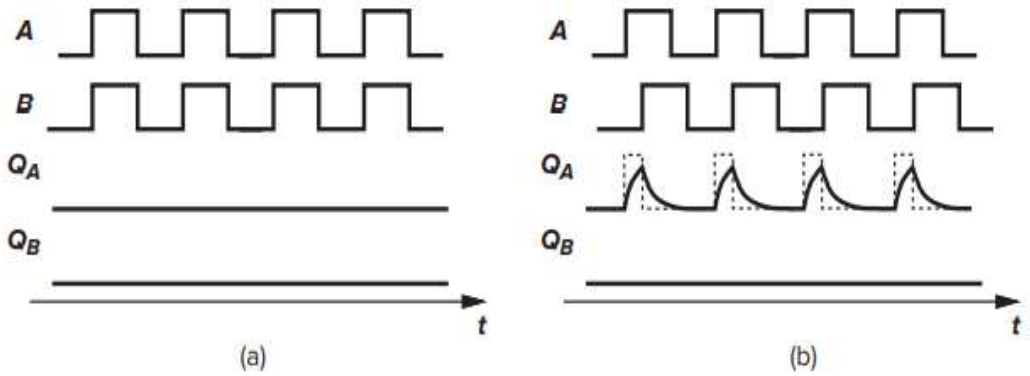


Fig 4.2:- (a) Zero input phase shift output wave (b) Output wave with minor phase shift in the input.

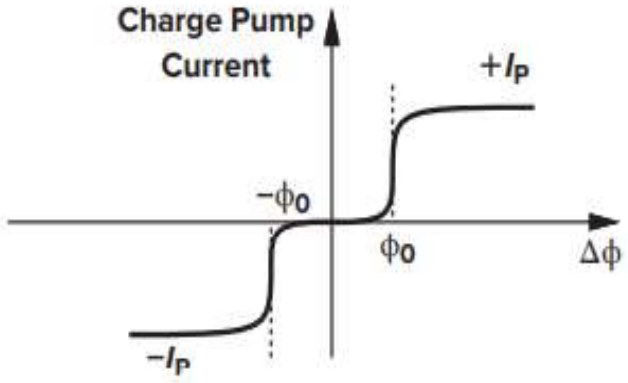


Fig 4.3:- Fig showing dead zone in the charge pump current

Astonishingly, concurrent pulses on QA and QB can totally eradicate the dead zone. This is because, for $\Delta\Phi = 0$, the pulses always power up the charge pump once they are

sufficiently wide. As a result, as illustrated in Fig 4.4, even a slight rise in the phase shift causes an approximately equal increase in the net current of the charge pump. In other words, if TP lasts long enough for QA and QB to reach a logically valid level and turn on the charge pump switches, the dead zone disappears.

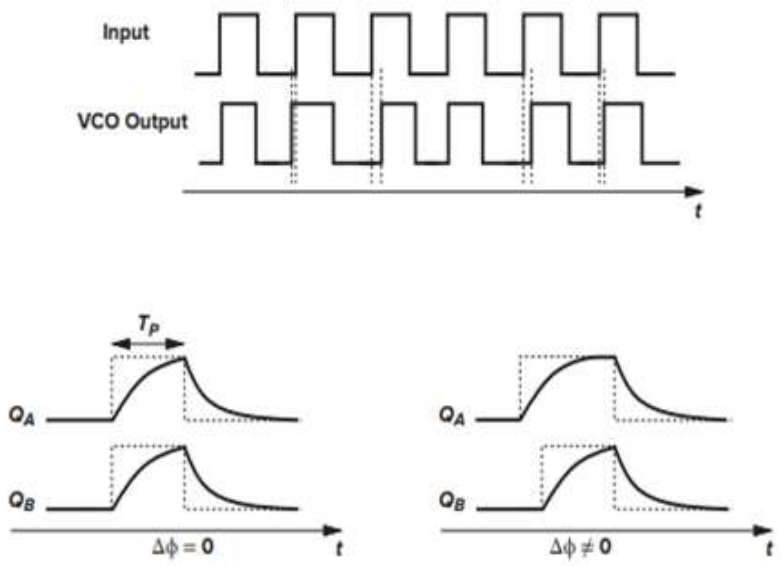


Fig 4.4:- Real Response of a Phase Detector to a small input phase shift.

4.1.2. Inverter Delay

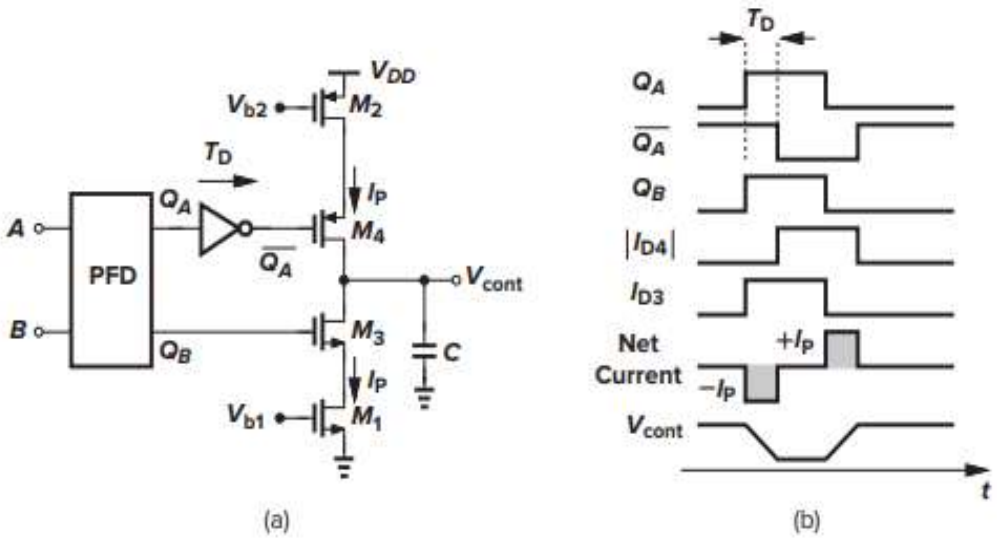


Fig 4.5 (a) Charge pump implementation (b) Skew effects between Q_A and Q_B

The first issue in the circuit shown in Fig 4.5 is caused by the delay between QA and QB in turning on their respective switches (a). The total current injected into the loop filter by the charge pump jumps between +Ip and Ip, causing the oscillator control voltage to rise or fall even though the loop is locked, as shown in Fig 4.5. (b).To counterbalance this effect, a complementary pass gate can also be placed between QB and the gate of M3, resulting in the delays shown in Fig 4.6 being compensated.

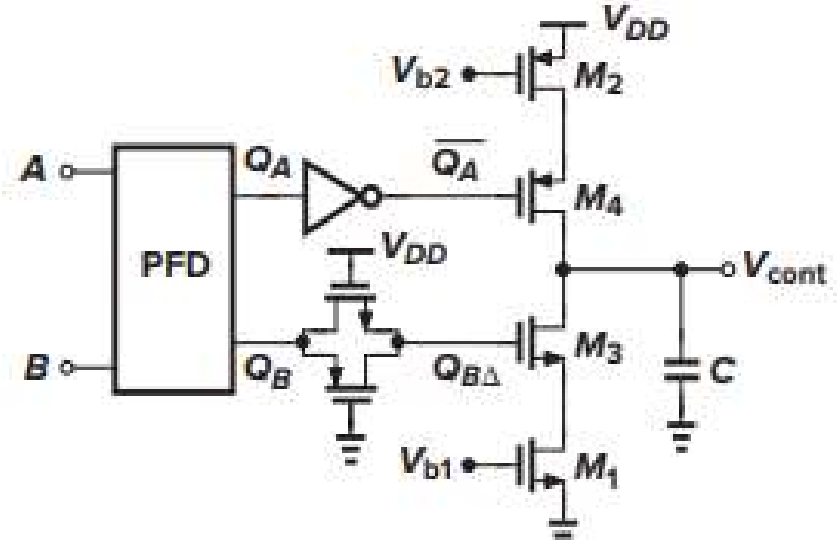


Fig 4.6:- Pass gate logic used to thwart skew.

It is worth noting:-

(1) The control voltage's periodic ripple continues.

(2) The terminal voltage affects the current mismatch.

(3) The phase shift & ripple are amplified by the clock feed through and charge injection mismatch between M3 and M4.

4.1.3. Charge sharing at the drain of the current sources

The third problem in the PFD circuit of is caused by the finite capacitance seen at the current source drains. As shown in Fig 4.7 (a), assume S_1 and S_2 both are turned off, allowing M_1 to discharge X to ground and M_2 to charge Y to VDD. If indeed the voltage drop across S1 and S2 is neglected, both S1 and S2 turn on at the next phase comparison moment, V_X rises, V_Y falls, and $V_X \approx V_Y \approx$ Vcont at the next phase comparison instant as shown in Fig 4.7 (b). Does Vcont stay constant after the switches are turned on if the phase error is zero and $ID_1 = |ID_2|$? Even if C_X equals C_Y, the change in V_X is not the same as the change in V_Y. The difference between the two changes must therefore be supplied by C_P, leading to a jump in Vcont.

The aforementioned charge-sharing phenomenon can be suppressed by "bootstrapping." The idea, as shown in Fig 4.8, is to "pin" V_X and V_Y to Vcont once the phase correlation is complete. Once S_1 and S_2 are turned off, S_3 and S_4 are turned on, permitting the unity-gain amplifier to hold nodes X and Y at a potential equal to Vcont.

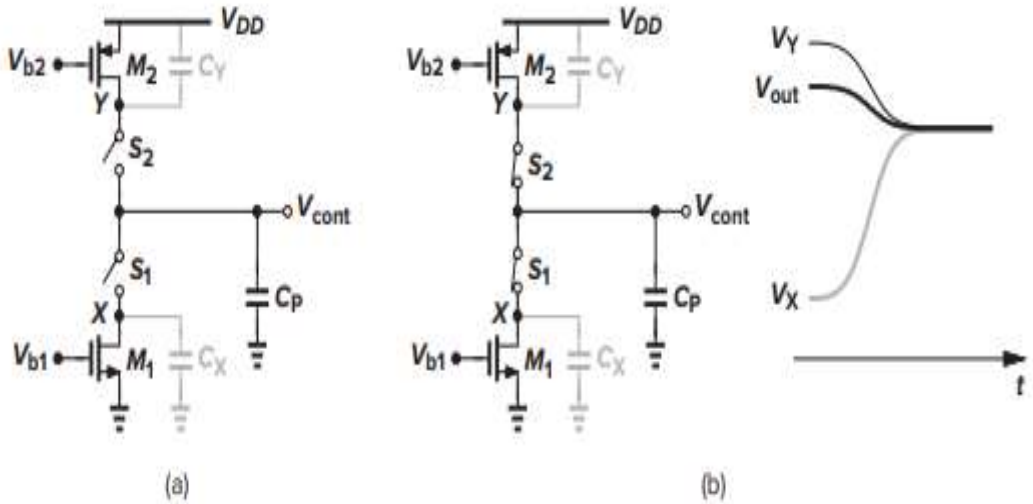


Fig 4.7 (a) Charge pump integration (b) Skew influence between QA and QB.

It really should be noted that the amplifier does not have to to provide a lot of current because I1≈I2.

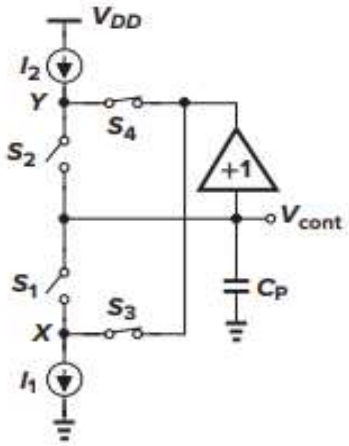


Fig 4.8:- X and Y are being bootstrapped to minimise charge sharing.

4.2 PLLs Jitter

A strictly periodic wave function, x1(t), has crossovers that are equally separated in time, as shown in Fig 4.9. Consider the nearly periodic signal x2(t), the period of that which varies slightly, going to cause the zero crossings to differ from their ideal points. Jitter is a term used to describe the latter waveform. By plotting the overall phase, Φtot, excess phase, Φex, we can see that jitter introduces itself as a randomness of the surplus phae with time.

Take a look at the jittery waveforms in Fig 4.10. Because its instantaneous frequency changes gradually through one period to another, the first signal, y1(t), showcases "slow jitter." y2, the second signal, has "fast jitter" (t). The excess phase plots of the two waveforms also show the rate of change.

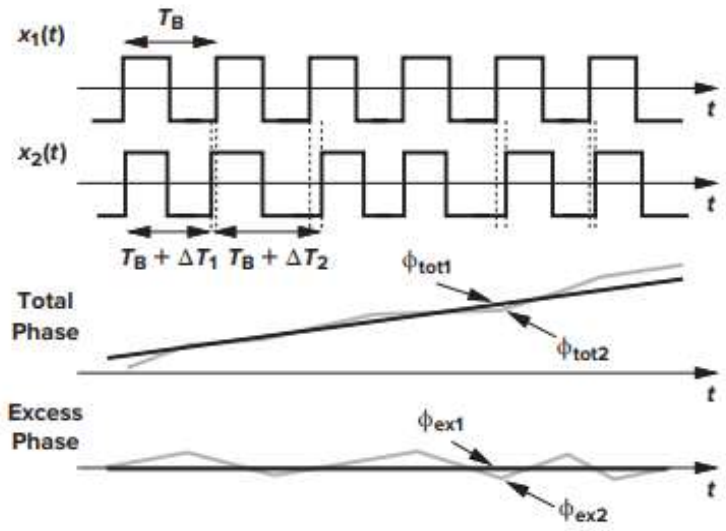


Fig 4.9:- Ideal and jittery waveforms.

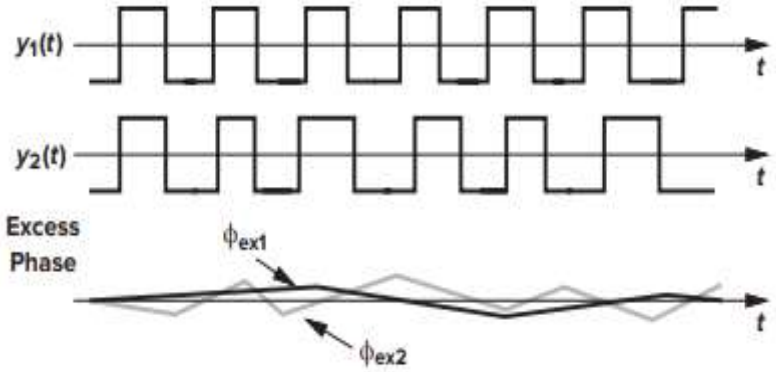


Fig 4.10:- Figure illustrating slow & fast jitter

There are two particularly interesting jitter phenomena in phase-locked loops namely:-

(1) Jitter in the input.

(2) Jitter produced by the VCO

The obtained transfer functons for type-1 and type-2 PLLs have low-pass qualities, implying that if Φin(t) tends to vary quickly, Φout(t) somehow doesn't fully record the variations. In other words, slow jitter doesn't quite affect output but fast jitter does. PLL low-pass filters are known as Φin (t). Suppose that the input is purely periodic but the VCO does have jitter. We design the system shown in Fig 4.11, wherein the input

additional phase is reduced to 0 and an erratic part VCO is introduced to the VCO's output to depict its jitter.

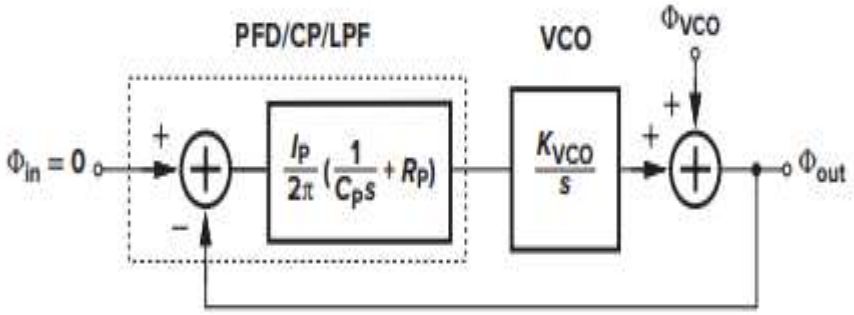


Fig 4.11:- Effect of jitter because of VCO

Surprisingly, the defining feature is high-pass, denoting that the VCO's slow jitter constituents but not its fast jitter constituents are suppressed. If ΦVCO (t) varies gradually (for example, drifts in oscillation with temperature), the similarity with Φin = 0 produces a time varying error, which proliferates the LPF and revises VCO's frequency to compensate for the transition in ΦVCO (t). When VCO differs quickly (for example, when high-frequency noise modulates the oscillation period), the phase detector inaccuracy is hugely damped by the loop poles, and the transformation is not rectified.

CHAPTER-5
Applications of PLL

After nearly a century of development, phase locking is still finding new applications in electronics, communication, and instrumentation. Memory, microprocessors, hard disc drive electronics, RF and wireless transceivers, and optical fibre receivers are some examples. In this chapter, we will see a variety of applications that exhibits phase locking versatility.

5.1. Frequency Multiplier and Synthesiser

5.1.1. Frequency Multiplier:-

The input frequency of a PLL can be multiplied by a M factor. Once we divide the generated frequncy signal of a PLL by Multiple (M) and apply it to a phase detector circuit, we get fout equals M times fin. In another context, because fD equals to fout/M and fD and fin must equal in the latched state, the PLL amplifies fin by M. The M circuit is designed as a counter, producing single pulse for each M input. The frequency-multiplying loop in Fig 5.1 has two attractive features. First, unlike the voltage amplifier, the PLL has a multiplication factor that is exactly identical to M, which is a unique property of phase locking Second, by varying the divide ratio M, the output frequency can be varied, which is a very useful property when synthesising frequencies.

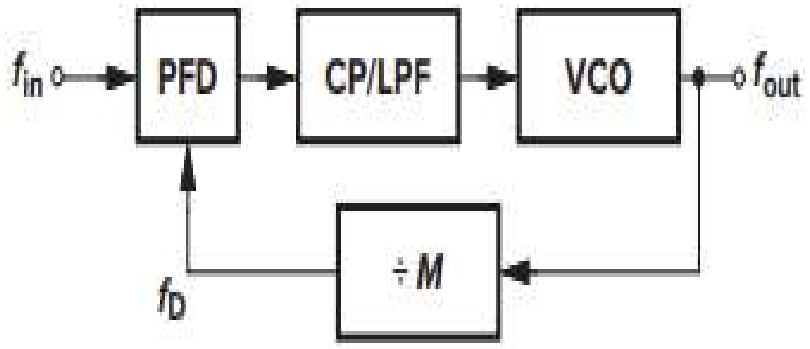


Fig 5.1:- Block diagram to showing frequency multiplication using PLL and ÷M circuit

5.1.2. Frequency Synthesiser:-

Some devices necessitate a periodic waveform with such a frequency that is (a) incredibly precise (e.g., below 10 ppm) and (b) variable in ultra delicate step (example, 30 kHz steps from 0.9 GHz to 0.925 GHz). PLL frequency multiplication can always meet these requirements, which are common in wireless transmitters and receivers.

The design of a phase-locked frequency synthesiser has been depicted in Fig 5.2. A digital word defining the value of M is used as the channel control input. Given that f_{out} equals to M times f_{REF}, the comparative accuracy of f_{out} is the same as that of f_{REF}. As a result, f_{REF} is obtained from a low-noise, stable crystal oscillator. If M shifts by one each time, fout varies in steps equal to f_{REF}.

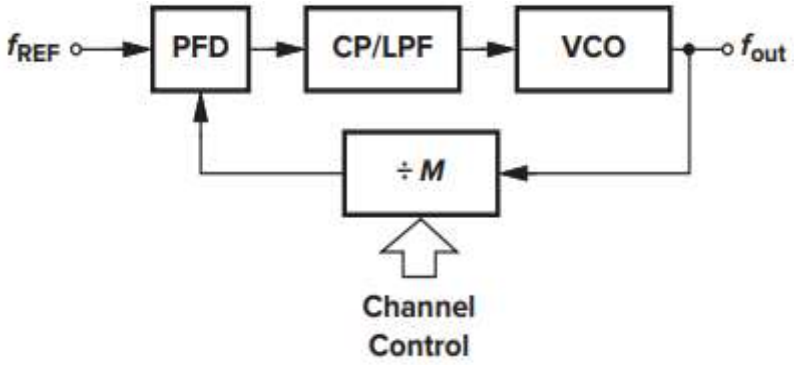


Fig 5.2:- Block diagram to showing frequency synthesiser using PLL and ÷M circuit

5.2. Clock Skew Suppression

Phase locking was first used in digital systems to reduce skew. Suppose a synchronous set of clock and data paths reaches a huge digital chip, as illustrated in Fig 5.3. Because the clock is typically used to drive many tranistors and lengthy interconnects, it is first provided to a huge buffer. As a result, the clock distributed on the chip may exhibit significant skew, T, in relation to data, which is an unwanted effect as it minimises the timing closers for on-chip functions. The skew is eliminated because the PLL maintains a nominally zero phase shift between CKin and CKB. In another way, the feedback system's infinite loop gain is divided by the buffer's constant phase shift.

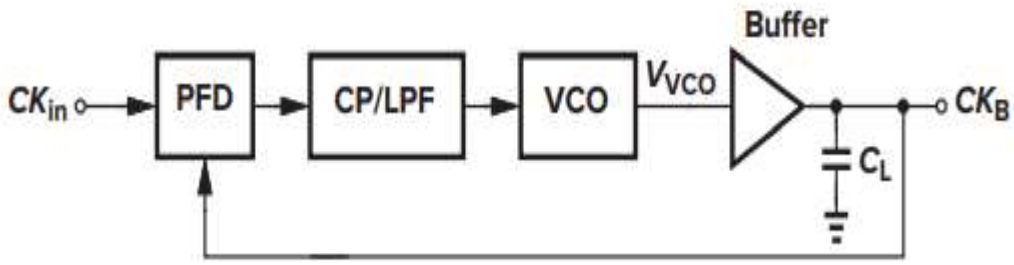


Fig 5.3:- Block diagram to showing use of PLL to eliminate clock skew

5.3 Jitter Reduction

At the input, PLLs inhibit fast jitter components. When a GHz signal along with the jitter is put as an input to a PLL with the bandwith of 1 MHz, jittery components of the input that vary faster than 1 MHz are suppressed . The phase-locked-loop, in some ways, functions as a narrowband filter with an overall bandwidth of 20 MHz, concentrated around 1 GHz. PLLs have yet another important and useful property.

The suggestion would be to use a D flip-flop guided by the clock to resample the halfway point of each bit, as shown in Fig 5.4. (a). However, the clock may not be available individually in many applications. Because an optical fibre, for example, only conveys an arbitrarily defined data stream, it lacks a distinct clock waveform at the receiver end. Fig 5.4 (b) depicts a circuit in which a "clock recovery circuit" generates the timming from data.. The circuit reduces the impact of input jitter on the retrieved clock by using phase locking with a pretty narrow loop bandwidth.

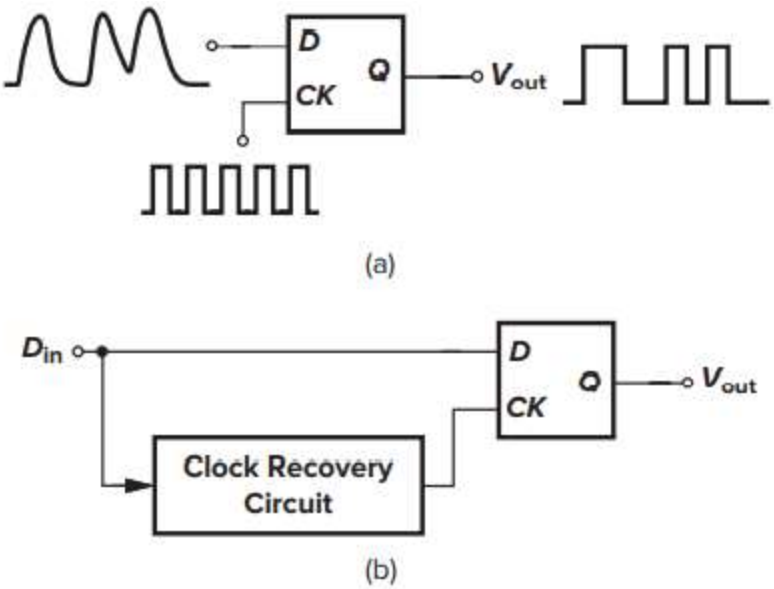


Fig 5.4:- Block diagram to showing (a) Retiming data with a D flip-flop steered by a low-noise clock; (b) creating the clock with a phase-locked clock recovery circuit.

CHAPTER-6
Current Starved VCO

6.1. 7-Stage Current Starved Inverter Circuit based Ring Oscillator

The supply voltage, VDD, of a ring oscillator circuit varies in real time, and the voltage imbalance causes an output frequency variation. As a result, current must be delivered to each inverter to make sure that the output frequency remains stable. This can be accomplished by using a current-starved inverter, as illustrated in Fig 6.1, which controls the amount of current used to charge and discharge the capacitive load at each stage. M1 and M2 act as current sources, limiting the current flowing through M3 and M4. M3 and M4 are inverters that are currently said to be current starved. The current of M5 and M6 is controlled by the input control voltage, and the values are mirrored in each inverter or current source voltage.

MOS MP1 and MN1 drain currents are identical and are controlled by the input control voltage. Currents in MOS MN1 and MP1 are reflected in every inverter. The frequency of the N stages CS-VCO oscillation is given by eq. (6.1), ID can be calculated using eq. (6.2), and thus the total drain capacitance of MOS MN3 and MP3 is fixed by eq. (6.3) Fig 6.2 depicts the control voltage versus output frequency of a three and seven stage current starved VCO.

$$Fosc = \frac{Id}{NCtotVdd} \quad .....6.1$$

$$Id = \frac{\beta}{2}(Vgs - Vth)^2 \quad .....6.2$$

$$Ctot = Cox(WpLp + WnLn) + \frac{3}{2}Cox(WpLp + WnLn) \quad .....6.3$$

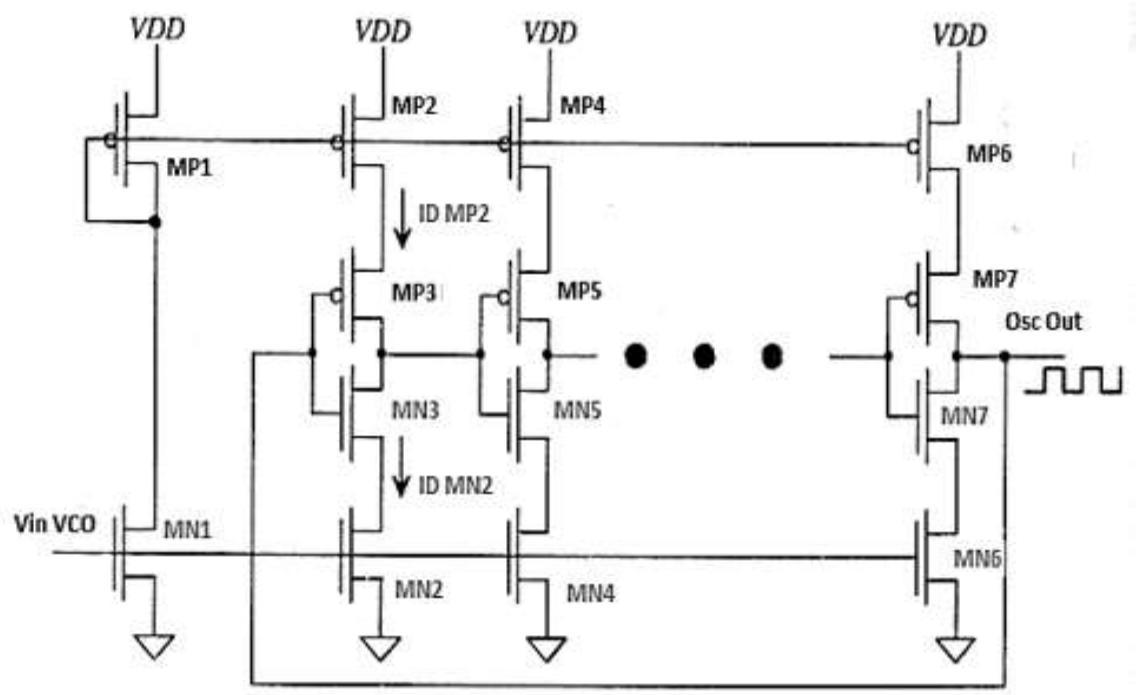


Fig 6.1:- Architecture of Current Starved VCO

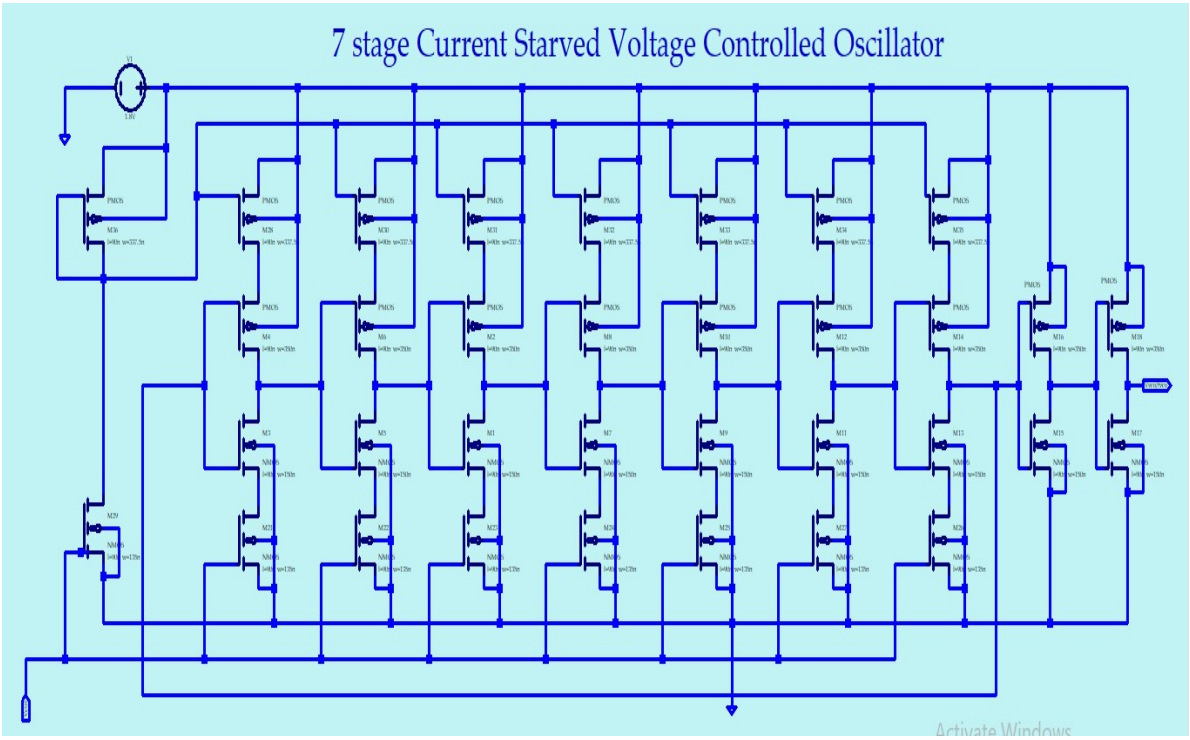


Fig 6.2:- Implementation of 7-stage CSVCO using Ltspice at 90nm technology node

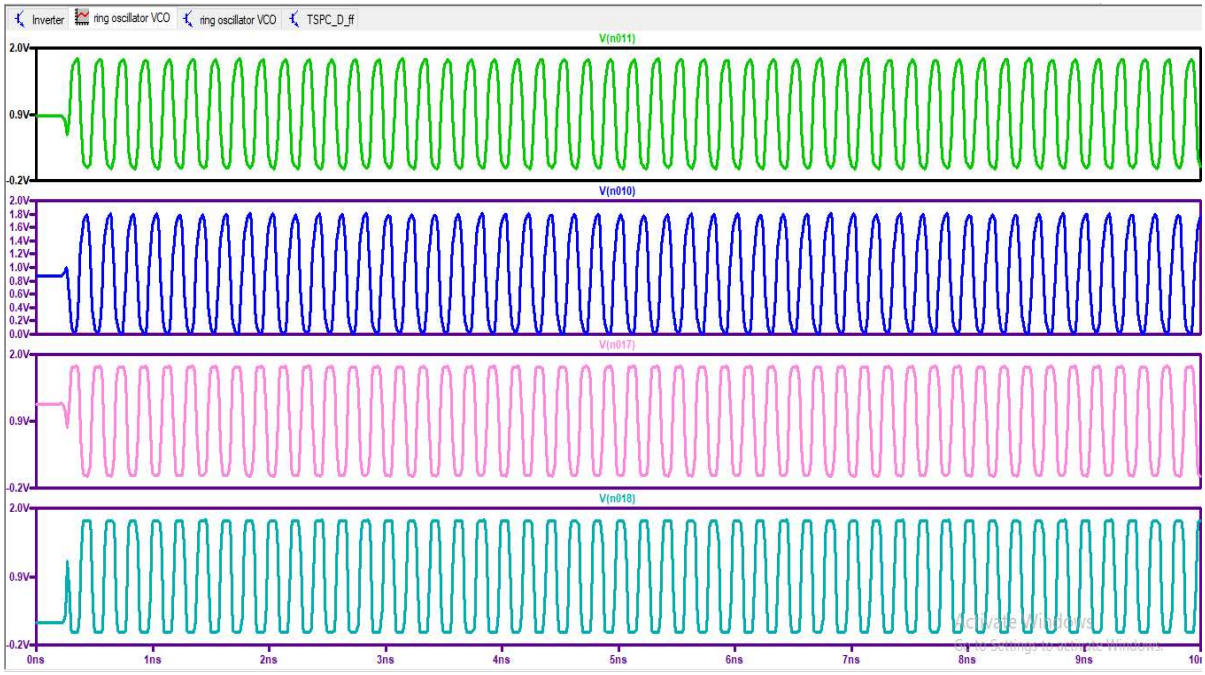


Fig 6.3: Fig showing the output wave form of the Oscillator at different inverter stages

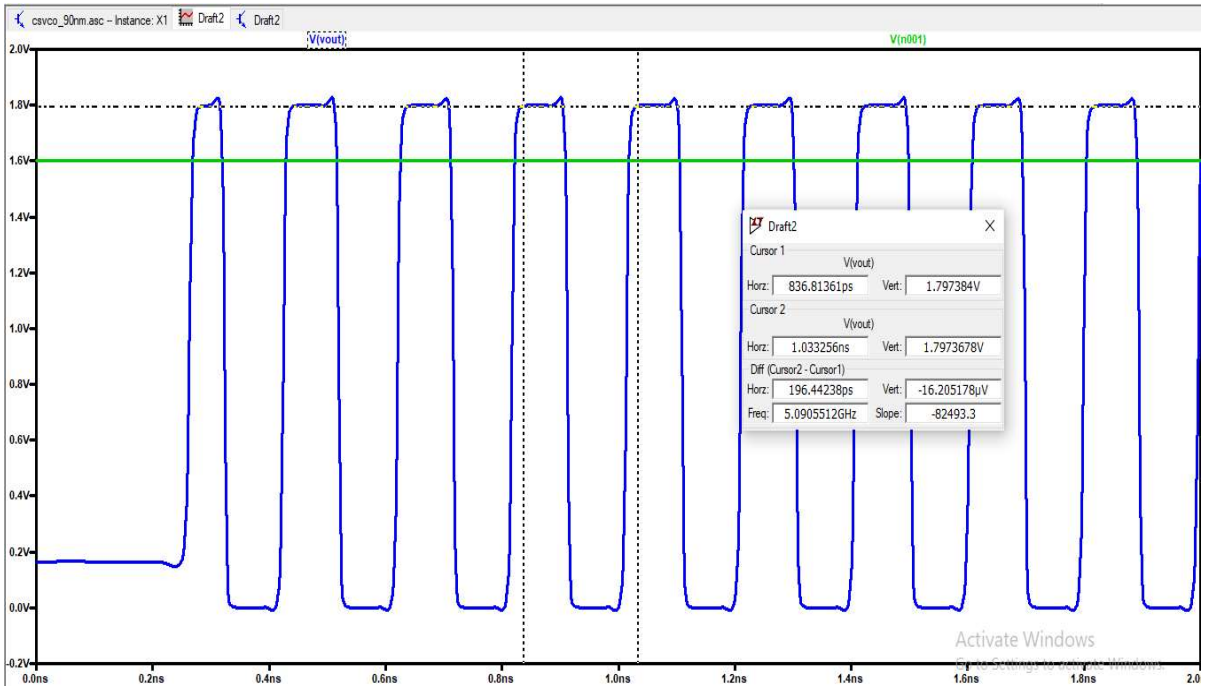


Fig 6.4:- Fig showing the measurement of the oscillation frequency for Vctrl = 1.6 V using Ltspice

Table 6.1 – Specifications of the implemented CSVCO

Technology node	90nm
Biasing Voltage	1.8V
Number of Current Starve stages	7
Total Number of transistors used	30 + 4 (inverter used for wave shaping)
Variation in Vctrl	0.4V – 3.6V
Frequency Range	0.5771 – 5.4033 GHz
Centre Frequency	3.5135GHz
Tuning Range	1.3187
Average Power Dissipation per cycle	142.29nW
Operation Frequency for linear output	0.5771 - 5.0906 GHz
VCO gain	23.633 rad/ns/V

Table 6.2: Vctrl vs. Fvco from the implemented CSVCO

Vctrl(V)	Fvco(GHz)
0.2	0
0.4	0.5771
0.6	1.724
0.8	2.9795
0.9	3.5135
1	3.9398
1.2	4.5437
1.4	4.8919
1.6	5.0906
1.8	5.2103
2	5.2944
2.2	5.2944
2.4	5.3374
2.6	5.3812
2.8	5.4033
3	5.3374
3.2	5.4033
3.4	5.5168

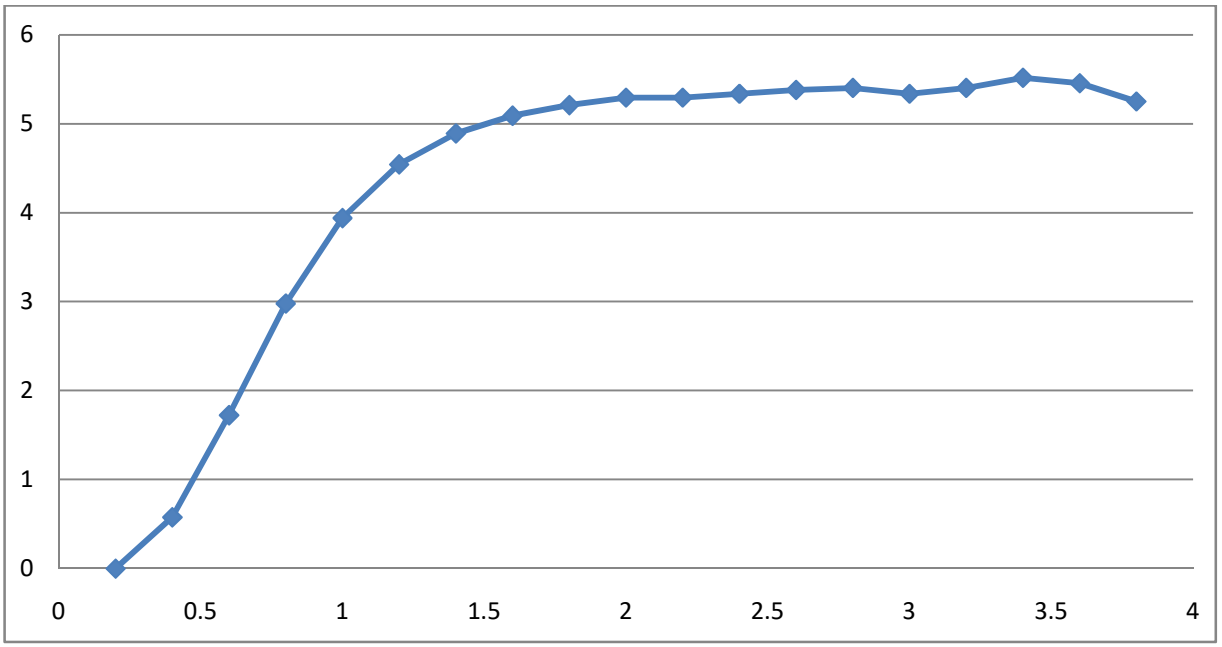


Fig 6.5: Fig showing Fvco (GHz) plot with varying Vctrl (Volts) for 7-stage VCO

The Tuning Range graph is a voltage vs. frequency graph. It can be viewed as proportional region obtained by drawing a voltage and frequency plot. A mathematical formula can also be used to calculate it. –

Tuning Range = (High frequency – low frequency) / (Central frequency)

6.2. 5-Stage Current Starved Inverter Circuit based Ring Oscillator

Table 6.3 – Specifications of the implemented CSVCO

Technology node	90nm
Biasing Voltage	1.8V
Number of Current Starve stages	5
Total Number of transistors used	22 + 4 (inverter used for wave shaping)
Variation in Vctrl	0.4V – 2.4V
Frequency Range	0.8006 – 7.3886GHz
Centre Frequency	4.8272 GHz
Tuning Range	1.3187
Average Power Dissipation per cycle	130.44 nW
Operational Frequency for linear operation	2.3446 – 6.7076 GHz
VCO gain	34.2669 rad/ns/V

Table 6.4: Vctrl vs. Fvco from the implemented CSVCO

Vctrl(V)	Fvco(GHz)
0.2	0
0.4	0.8006
0.6	2.3446
0.8	4.081
0.9	4.8272
1	5.4256
1.2	6.2524
1.4	6.7076
1.6	7.0159
1.8	7.1667
2	7.2889
2.2	7.3263
2.4	7.3886

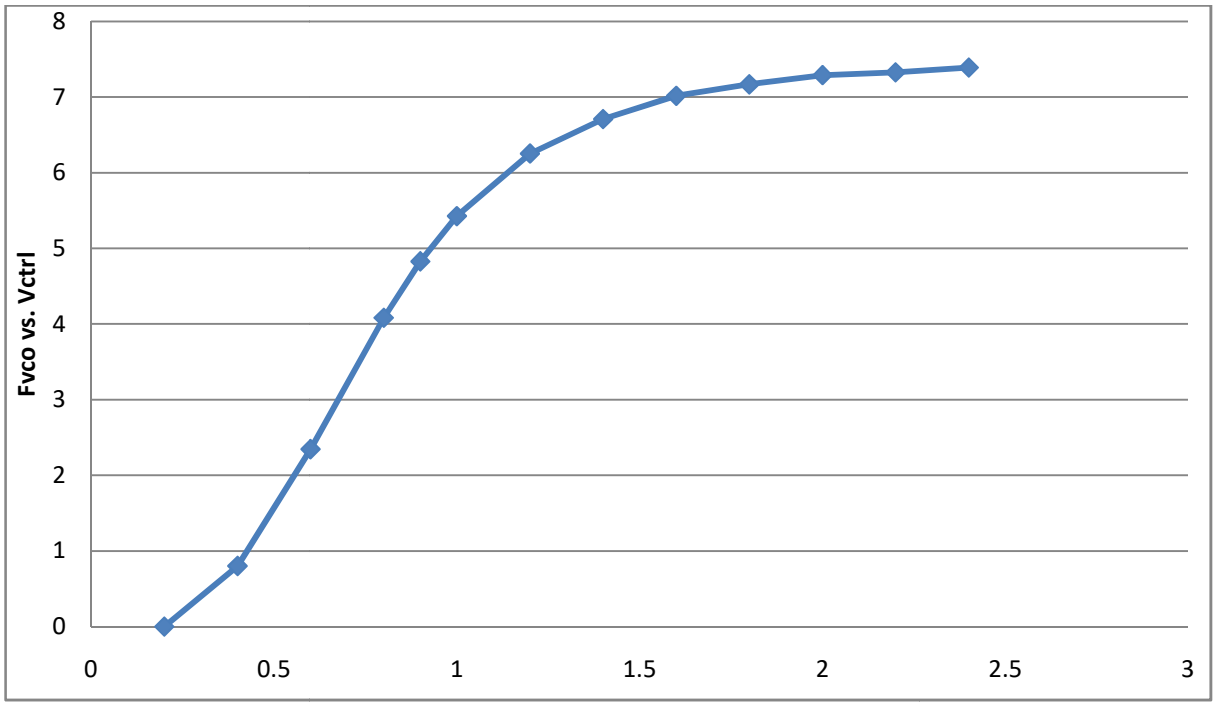


Fig 6.6: Fig showing Fvco (GHz) plot with varying Vctrl (Volts) for 5-stage VCO

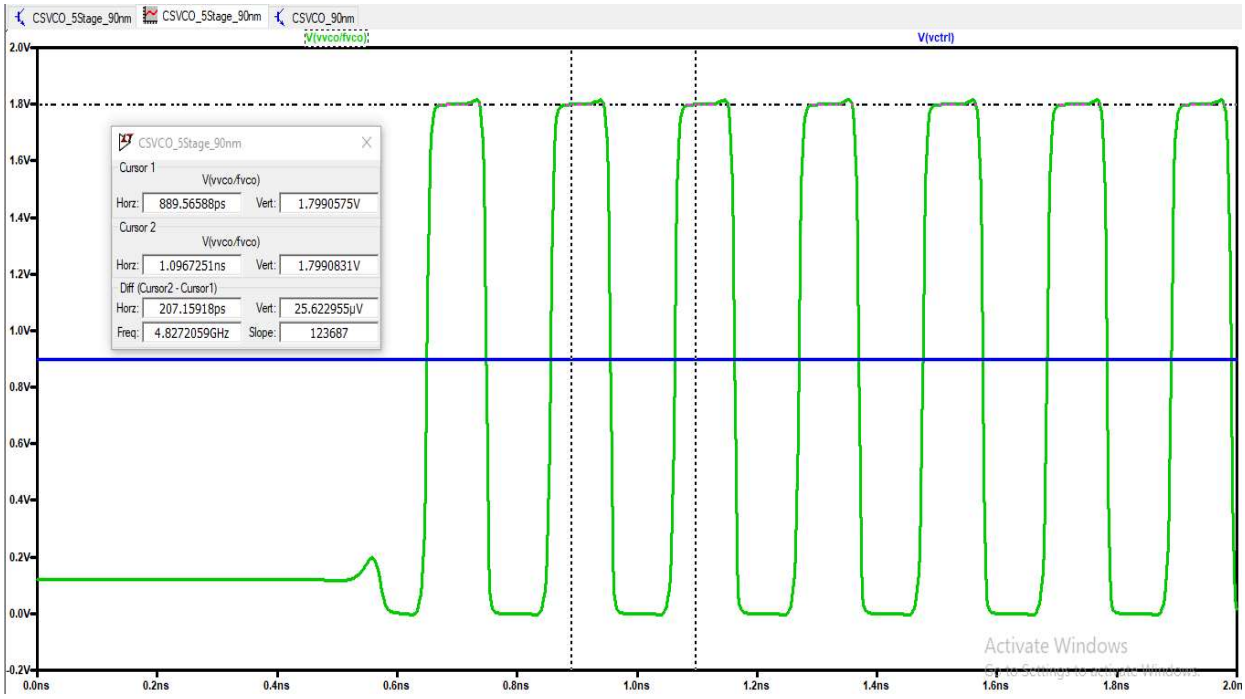


Fig 6.7: Fig showing the measurement of the oscillation frequency for Vctrl = 0.9 V using Ltspice for 5-stage VCO

Conclusion:- The CSVCO used here is a five-stage CSVCO. The linearity range of a three-stage CSVCO deteriorated, and the output frequency of operation was drastically reduced for a seven-stage VCO. As a result, a 5 stage VCO was used, which provided a good linearity range as well as a higher output frequency. To achieve optimal PLL performance, it is important to ensure that the output voltage range of the PFD CP-LPF block is within the dynamic linearity range of the VCO when designing the PLL.

CHAPTER-7
Phase Frequency Detector

7.1. Gate Based Phase Frequency Detector

The overall PFD at the gate level is depicted in Fig 7.1. In case the network starts with values A equals 1, $Q_A = 1$, and $Q_B = 0$, arising edge at input node B forcing Q_B to move to a low and then high on a single gate delay later. This change affects every depicted node in the figure below, and finally QA and QB. As a result, the pulse width of QB is approximately equal to 5 gate delays.

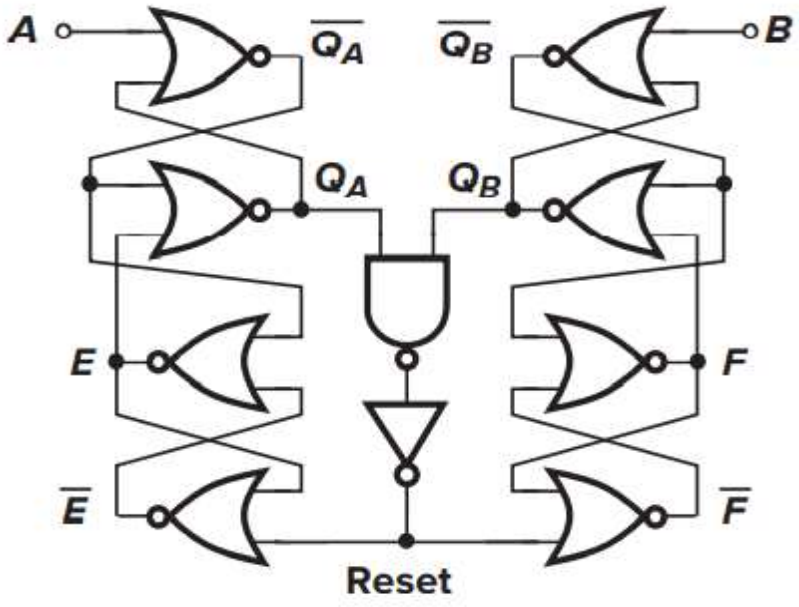


Fig 7.1:- Block Diagram of a Gate Level Phase Frequency Detector

Table 7.1 – Specifications of the implemented Gate Level PFD

Technology node	90nm
Biasing Voltage	1.8V
Total Gate Count	10 (8 NOR, 1 NAND, 1 NOT)
Total Number of transistors used	38 (19 PMOS, 19 NMOS)
Reset Delay when Q_B goes high	107.2227ps
Reset Delay when Q_A goes high	104.6106ps
Pulse width for Overlapping case	130.687ps
Average Power Dissipation per cycle	19.7205µW

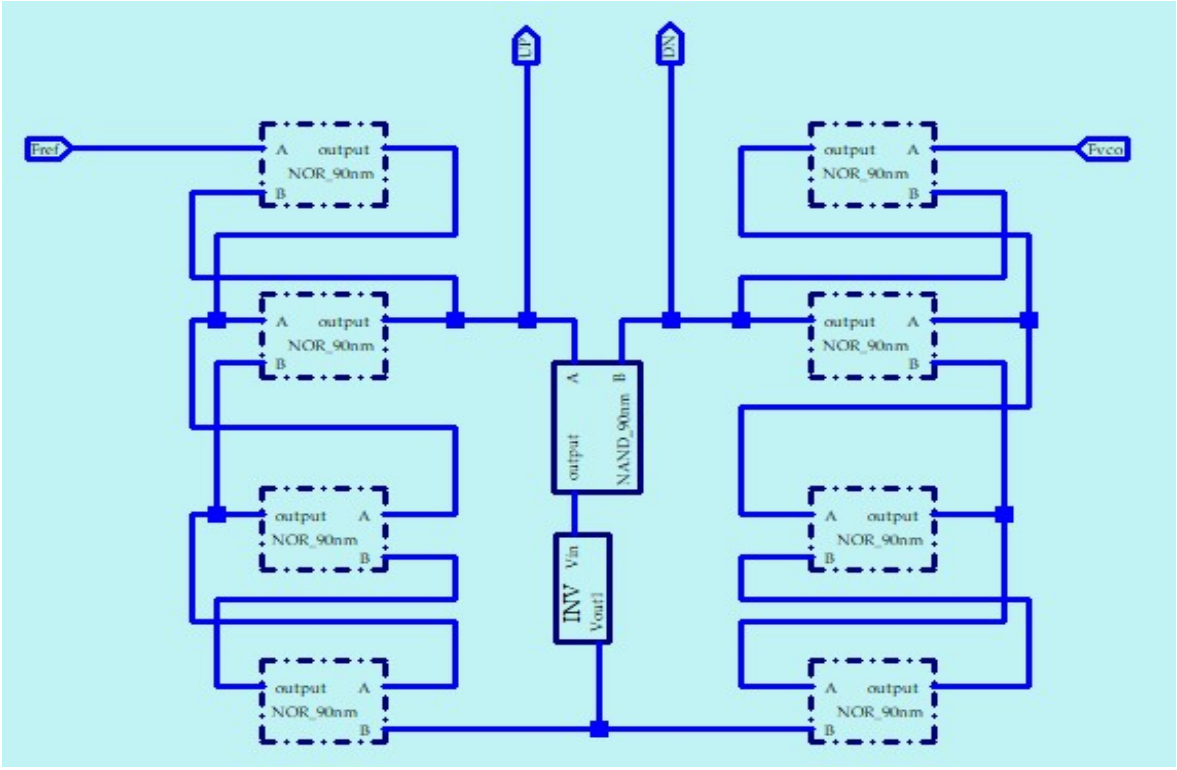


Fig 7.2:- Schematic Diagram of a Gate Level Phase Frequency Detector

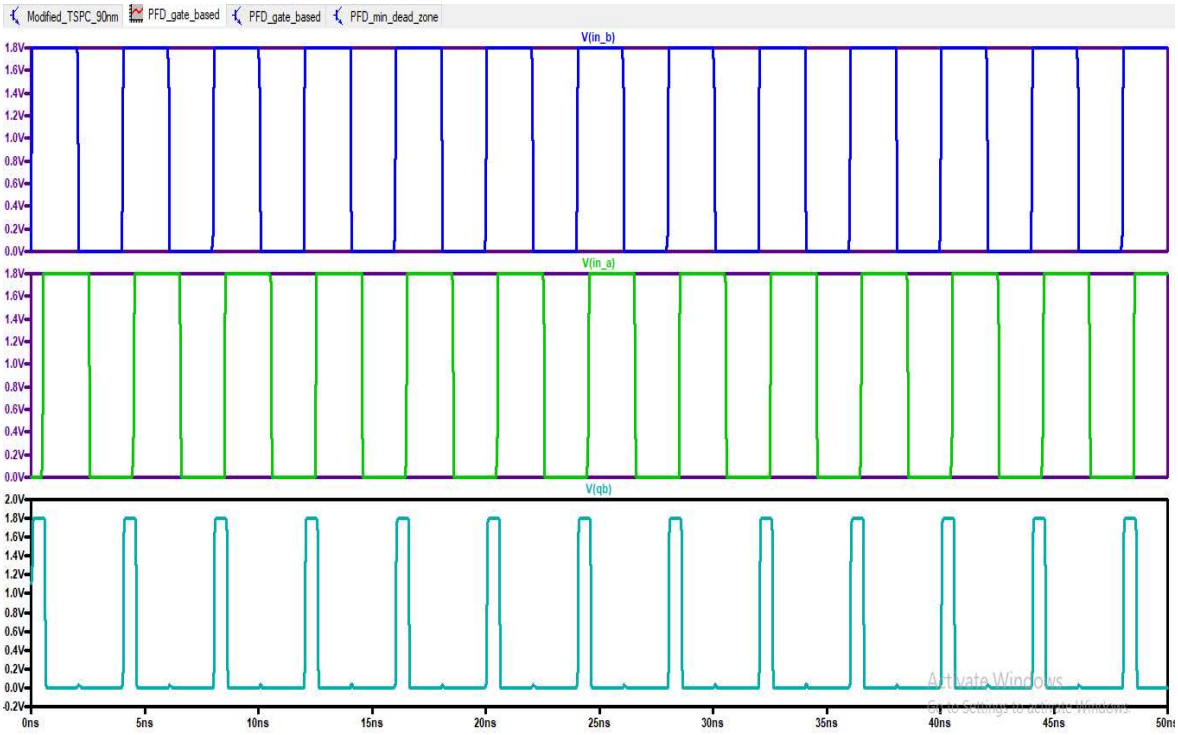


Fig 7.3:- Output Waveform at Q_A & Q_B when fref / Vref at V(in_a) is lagging

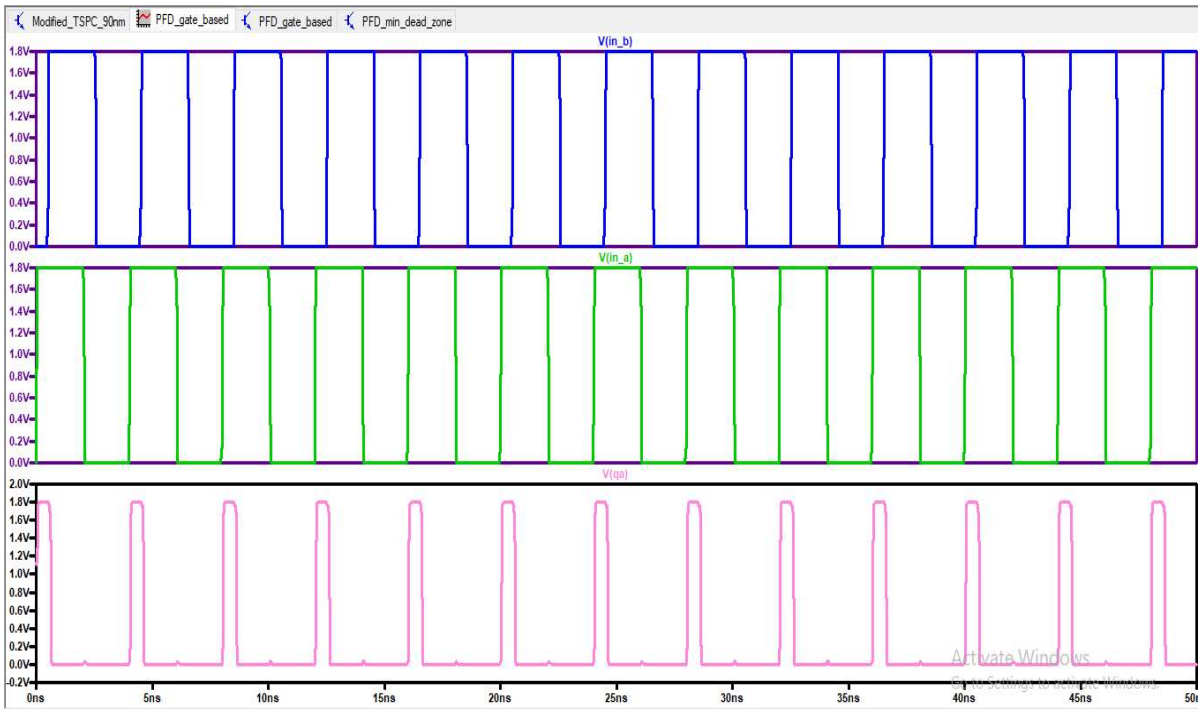


Fig 7.4:- Output Waveform at Q_A when fref / Vref at V(in_a) is leading

7.2. Modified TSPC Master-Save edge triggered D-FF based PFD

When there is a path to ground, node B is always precharged to HIGH when clock (Clk) is LOW and returns to LOW when Clk is HIGH. As a result, node B experiences continuous toggling whenever the input D is stable LOW in relation to Clk for an extended period of time. This wasteful behaviour not only wastes power, but it also causes noise on the output node, Q, due to erroneous glitches caused by Clk's LOW-to-HIGH transitions. To address this issue, the proposed MTSPC DFF architecture demonstrates that whenever the path to ground is ON, pre-charging node B should be suspended to avoid toggling.

A simple technique that works here is to add a PMOS transistor that prevents the pre-charging phase from occurring without affecting the flip-overall flop's operation. If Clk is LOW and D is LOW, node B and, as a result, node Qb retains their previous values. Node B pre-charges to HIGH when D is changed to HIGH; the output remains unchanged. If Clk changes from LOW to HIGH, node B retains its charge (HIGH), while node Qb loses its charge (LOW). Even if D is reset to LOW, the output will remain

unaffected. In case Clk switches from 0 to 1 while D is 0, node B discharges & nodes Qb and Q become 1.

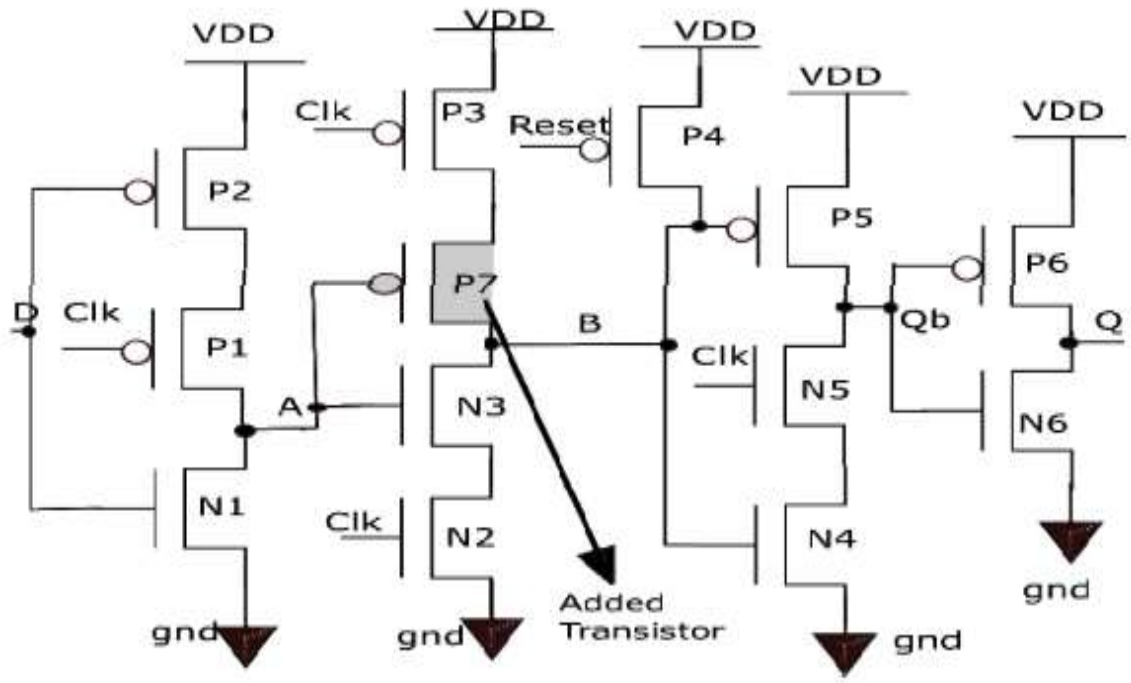


Fig 7.5:- Transistor level circuit diagram of a modified TSPC Positive edge triggered D-FF

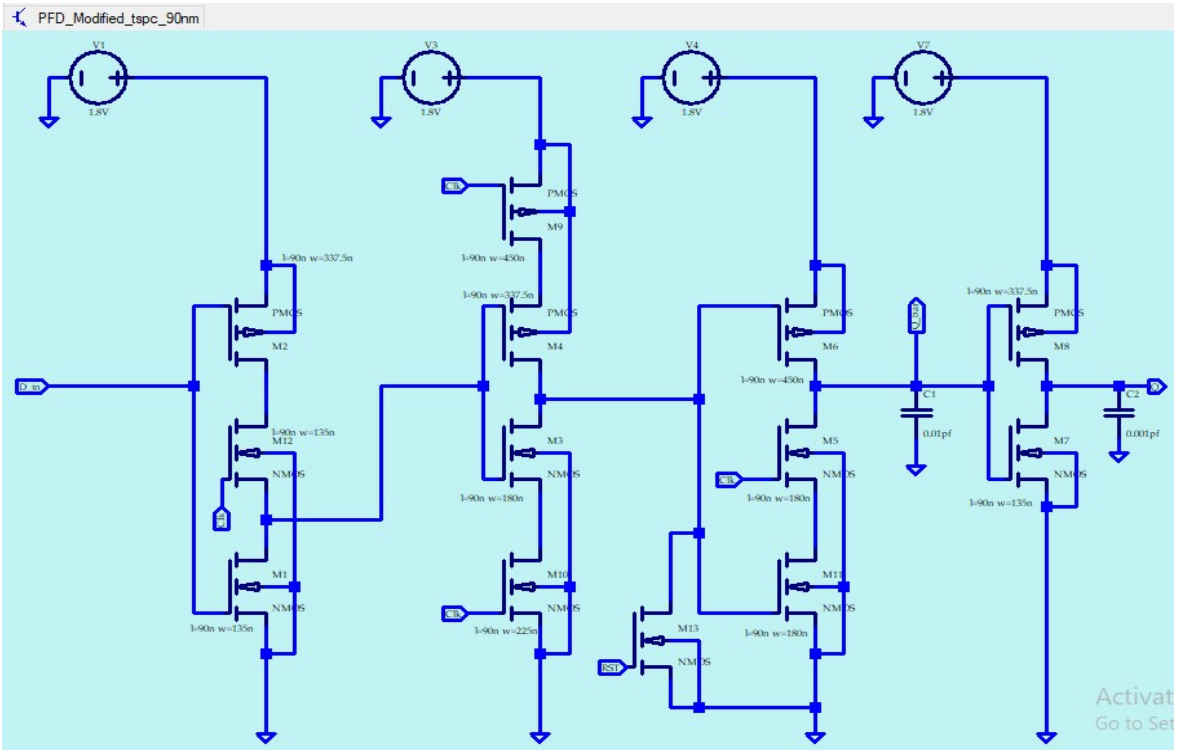


Fig 7.6:- Schematic diagram of a modified TSPC Positive edge triggered D-FF using LTspice at 90nm technology node.

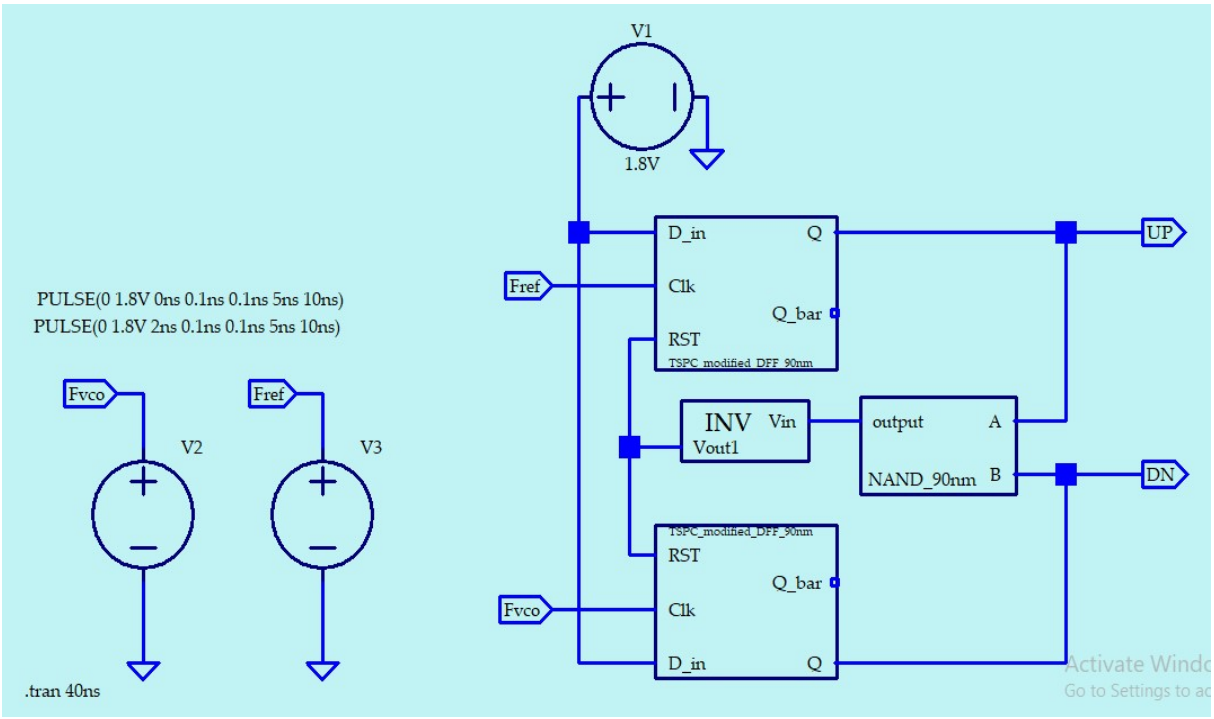


Fig 7.7:- Schematic diagram of D-FF based Phas/Frquency Detector implemented with modified TSPC.

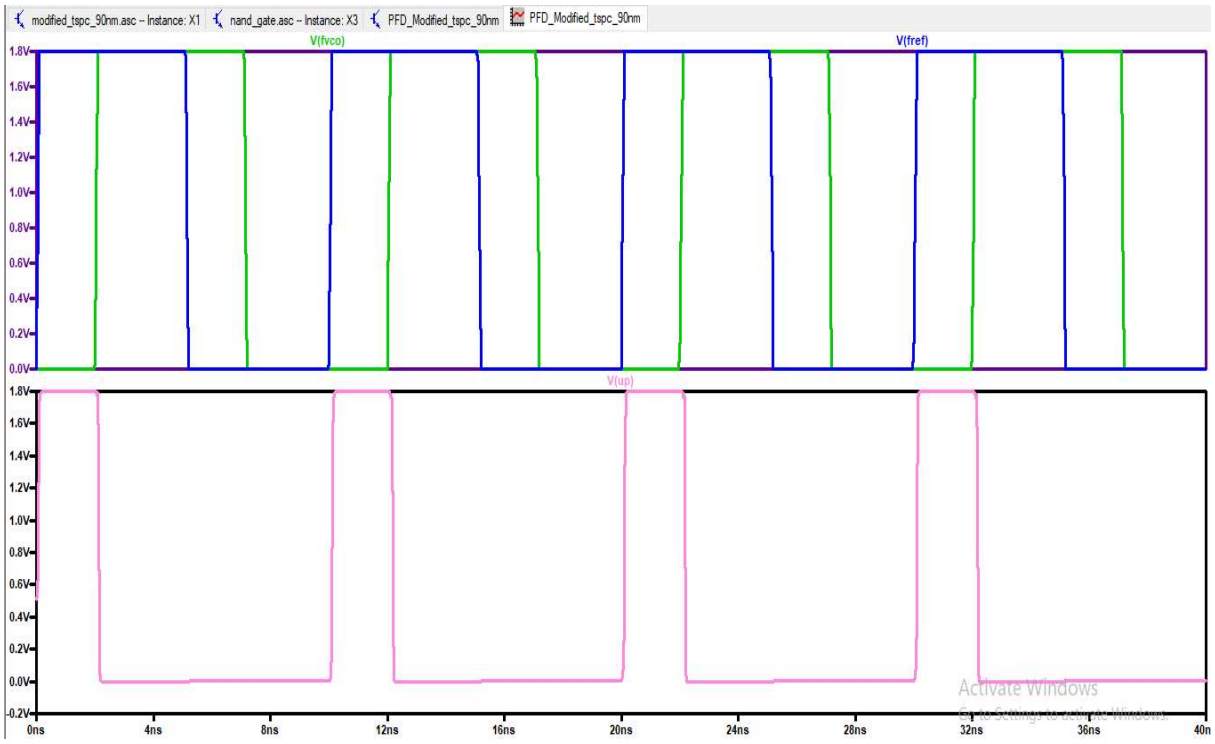


Fig 7.8:- Output Waveform at Q_A when fref / Vref at V(in_a) is leading

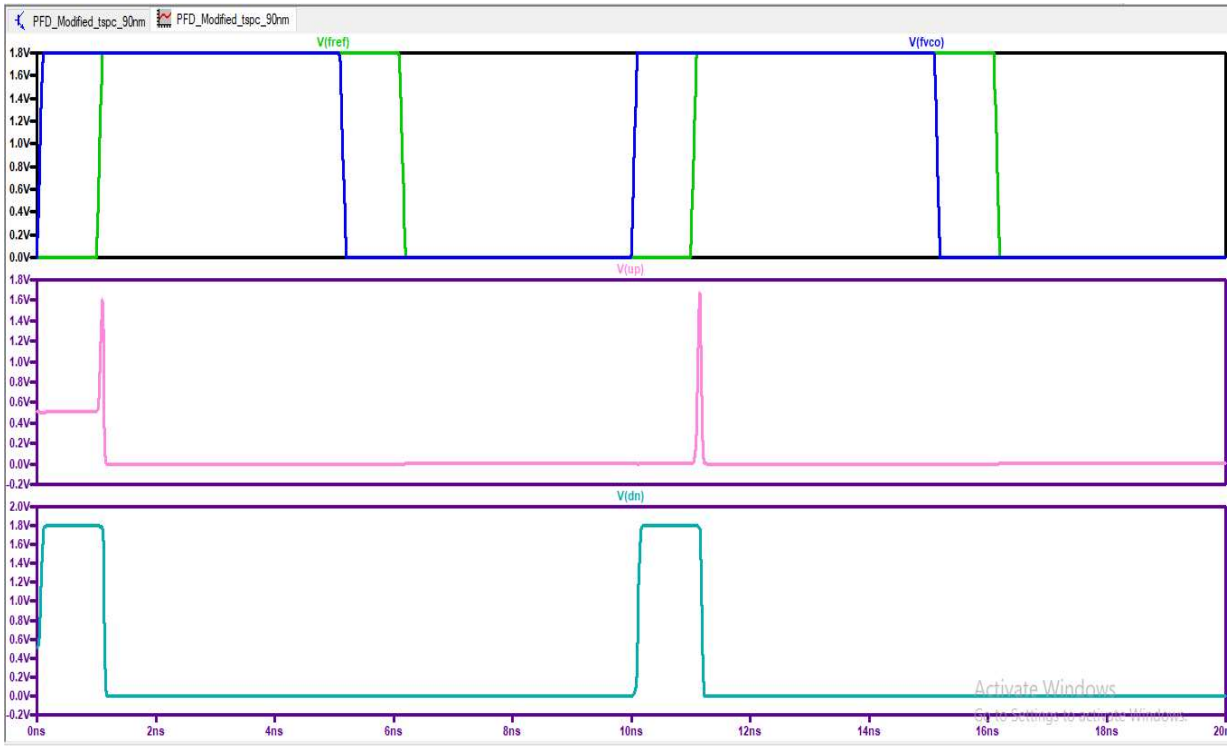


Fig 7.9:- Output Waveform at Q_A & Q_B when fref / Vref at V(in_a) is lagging

Table 7.2 – Specifications of the implemented Modified TSPC based PDF

Technology node	90nm
Biasing Voltage	1.8V
Total Gate Count	2 D-FF, 1 NAND, 1 NOT)
Total Number of transistors used	32 (13 PMOS, 19 NMOS)
Reset Delay when Q_B / Fvco goes high	143.3665ps
Reset Delay when Q_A / Fref goes high	140.0153ps
Pulse width for Overlapping case	201.0712ps
Average Power Dissipation per cycle	4.173µW

7.3. 5T TSPC edge triggered master slave D-FF based PFD

The diagram below depicts a Positive Edge triggered D Flip-Flop with 5T TSPC latches connected in master-slave mode. This configuration requires fewer transistors than a standard TSPC D flip-Flops configuration. As a result, this circuit can save both power and area.

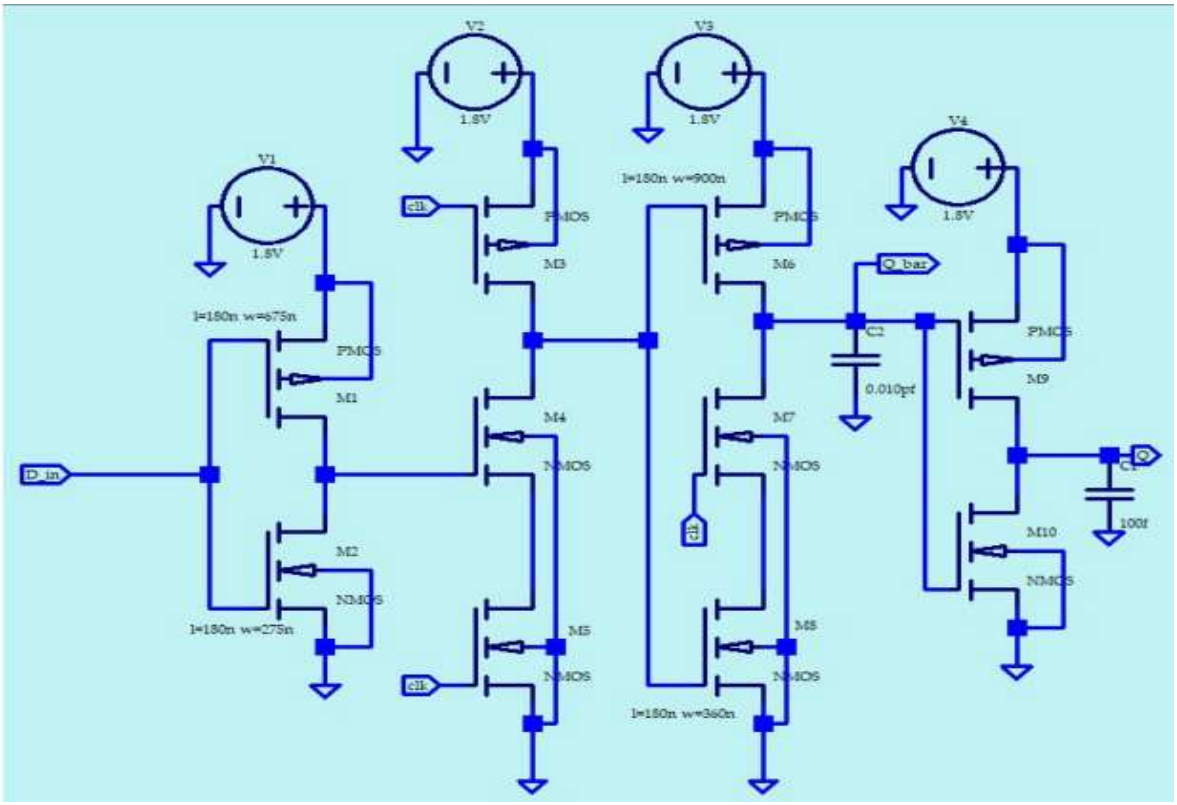


Fig 7.10:- Schematic diagram of a 5T TSPC Positive edge triggered Master-Slave D-FF.

.

Table 7.3 – Truth Table a 5T TSPC Positive edge triggered Master-Slave D-FF

Clk	D	M1	M2	M3	M4	M5	M6	M7	M8	M9	M10	Q
1	0	ON	OFF	OFF	ON	ON	ON	ON	OFF	OFF	ON	0
0	0	ON	OFF	ON	ON	OFF	OFF	OFF	ON	OFF	ON	0
1	1	OFF	ON	OFF	OFF	ON	OFF	ON	ON	ON	OFF	1
0	1	OFF	ON	ON	OFF	OFF	OFF	OFF	ON	ON	OFF	1

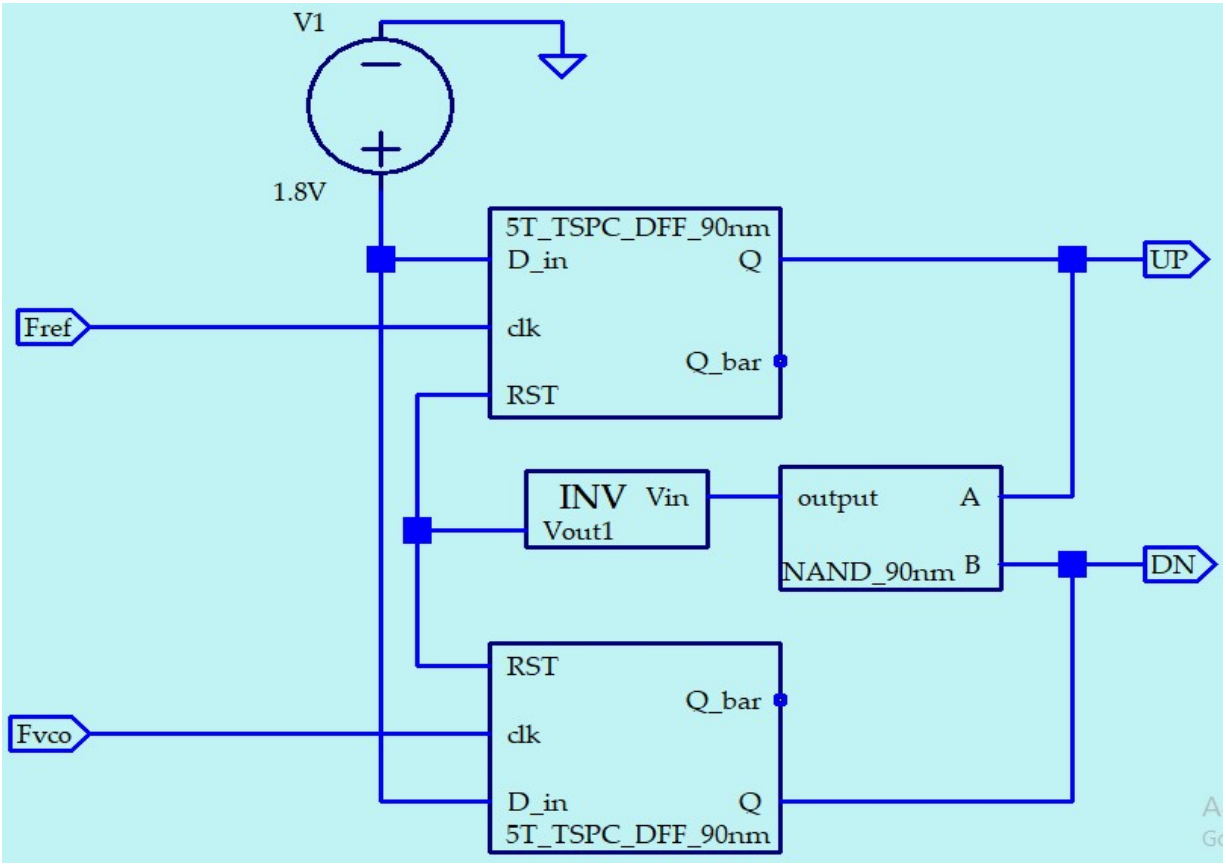


Fig 7.11:- Schematic diagram of a 5T TSPC Positive edge triggered D-FF based Phase Frequency Detector.

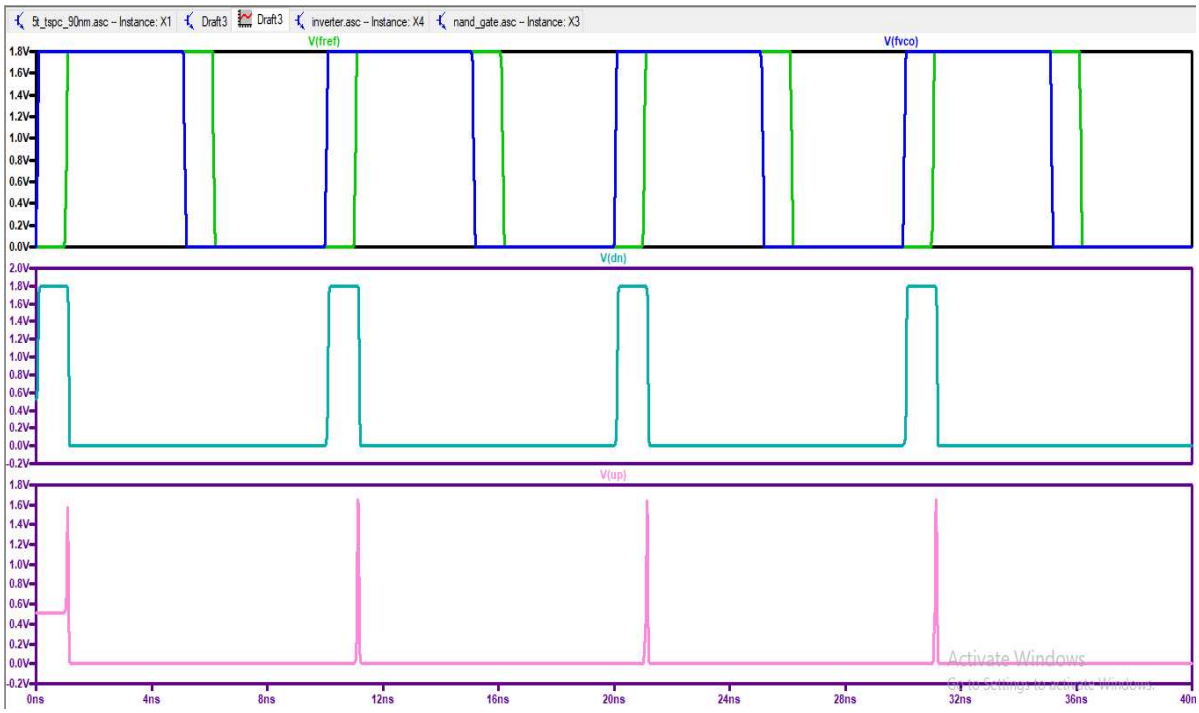


Fig 7.12:- Output Waveform at Q_A & Q_B when fref / Vref at V(in_a) is lagging

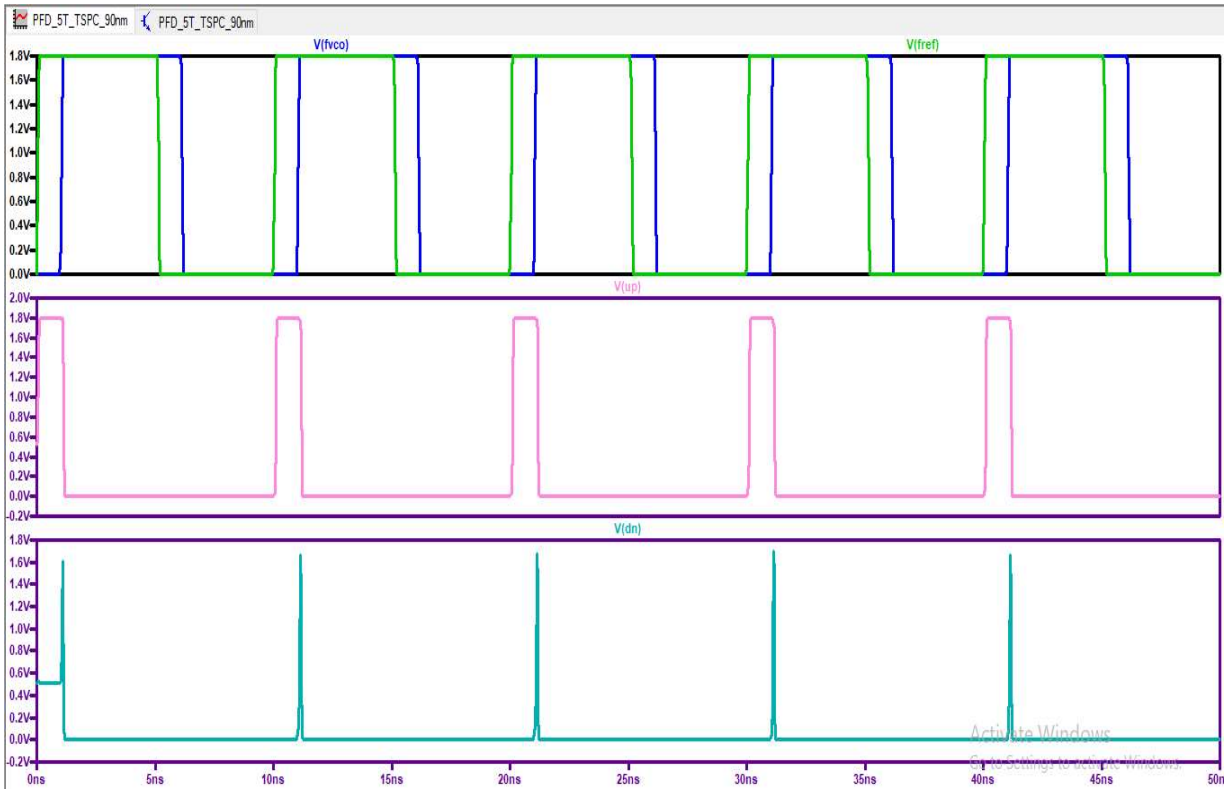


Fig 7.13:- Output Waveform at Q_A & Q_B when fref / Vref at V(in_a) is leading

Table 7.4 – Specifications of the implemented 5T TSPC M-S based PDF

Technology node	90nm
Biasing Voltage	1.8V
Total Gate Count	2 D-FF, 1 NAND, 1 NOT)
Total Number of transistors used	28 (11 PMOS, 17 NMOS)
Reset Delay when Q_B / Fvco goes high	135.5012ps
Reset Delay when Q_A / Fref goes high	134.2617ps
Pulse width for Overlapping case	192.2197ps
Average Power Dissipation per cycle	6.3244µW

7.4. Fast Frequency Acquisition with Minimum Dead Zone PFD

These flip flops have been modified to perform the required function of the D flip-flop for PFD. The proposed D flip flop operates in a very simple manner. When the input clock and reset signals are low, node A is connected to VDD via M1, M2 and charged to VDD, as shown in Fig 7.14. At the rising edge of the clock signal, the output node is connected to ground via M3 and M4. Once node A is charged to VDD, the input clock signal has no effect on the output node.

Since the charges at node A turn off the M3, the output node is not pulled up. As a result, the output node is disconnected from the input node. When the reset signal is given, node A is disconnected from VDD by M1 and connected to ground by M2. As soon as node A is discharged, the output node is pulled up via M2. The M1 is included to prevent the short circuit that occurs when the reset signal is applied. If the clock signal is low while the reset signal is high, a current path is formed from VDD to ground without the use of M1.

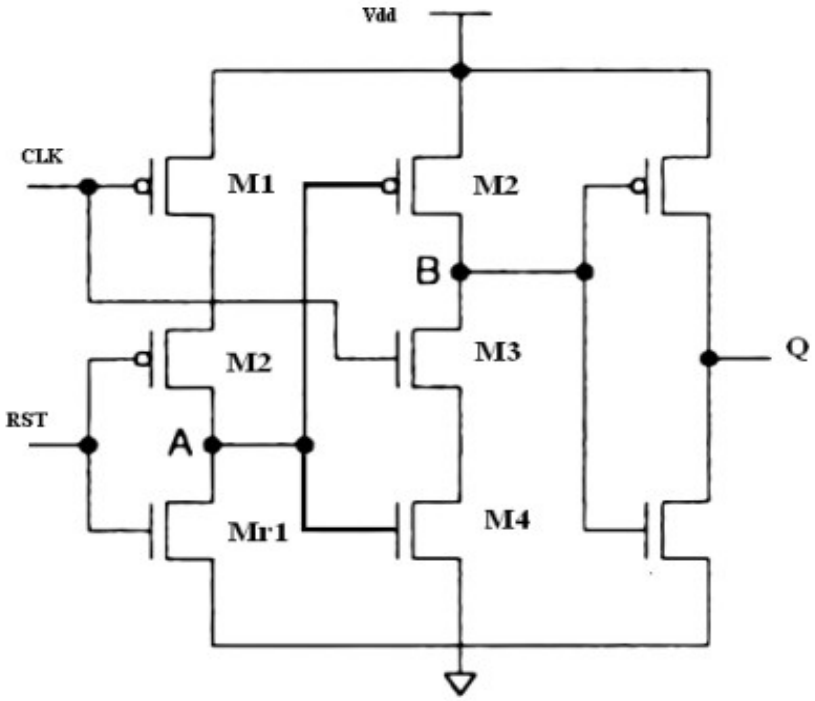


Fig 7.14:- Transistor level circuit diagram of a modified D-FF for Minimum Dead Zone

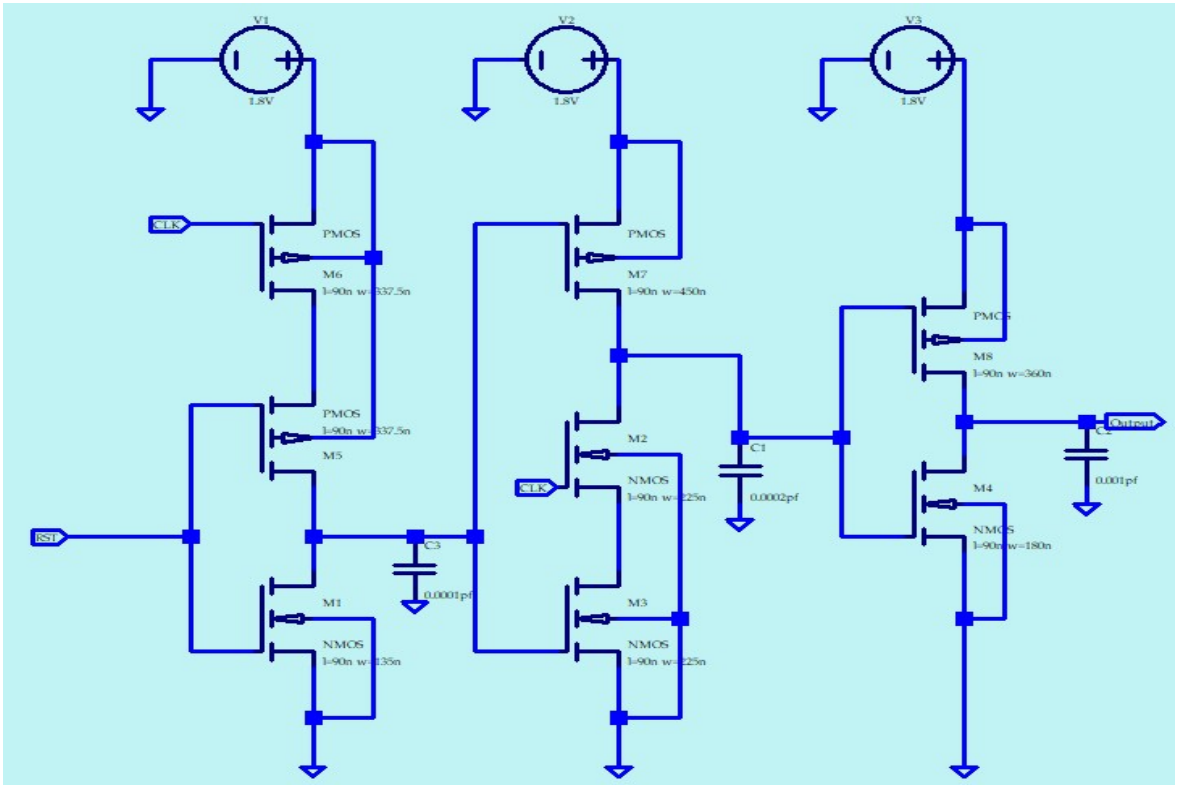


Fig 7.15:- Schematic diagram of a modified D-FF for Minimum Dead Zone

Table 7.5 – Specifications of the implemented Fast Frequency Acquisition with Minimum Dead Zone PDF

Technology node	90nm
Biasing Voltage	1.8V
Total Gate Count	2 D-FF, 1 NAND, 1 NOT)
Total Number of transistors used	24 (11 PMOS, 13 NMOS)
Reset Delay when Q_B / Fvco goes high	67.2336ps
Reset Delay when Q_A / Fref goes high	64.8359ps
Pulse width for Overlapping case	109.4874ps
Average Power Dissipation per cycle	10.6526µW

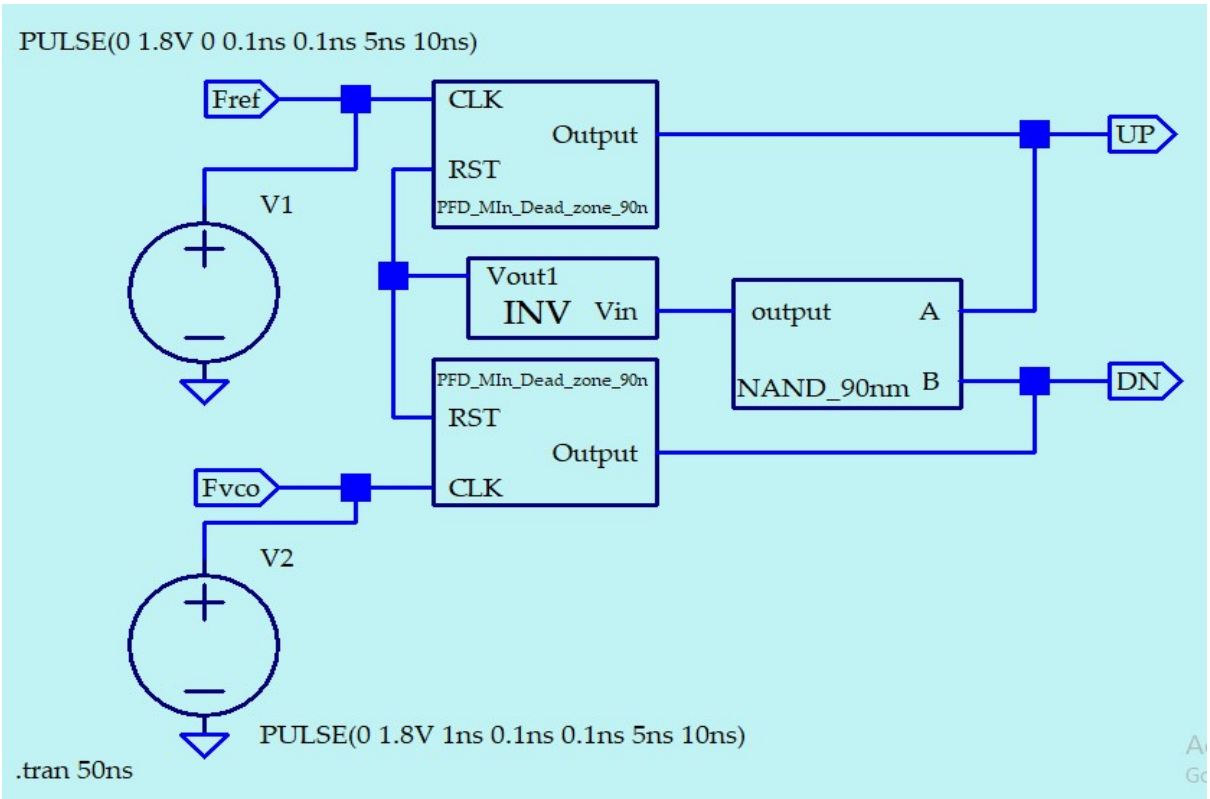


Fig 7.16:- Schematic diagram of a Positive edge triggered D-FF with minimum dead zone based Phase Frequency Detector.

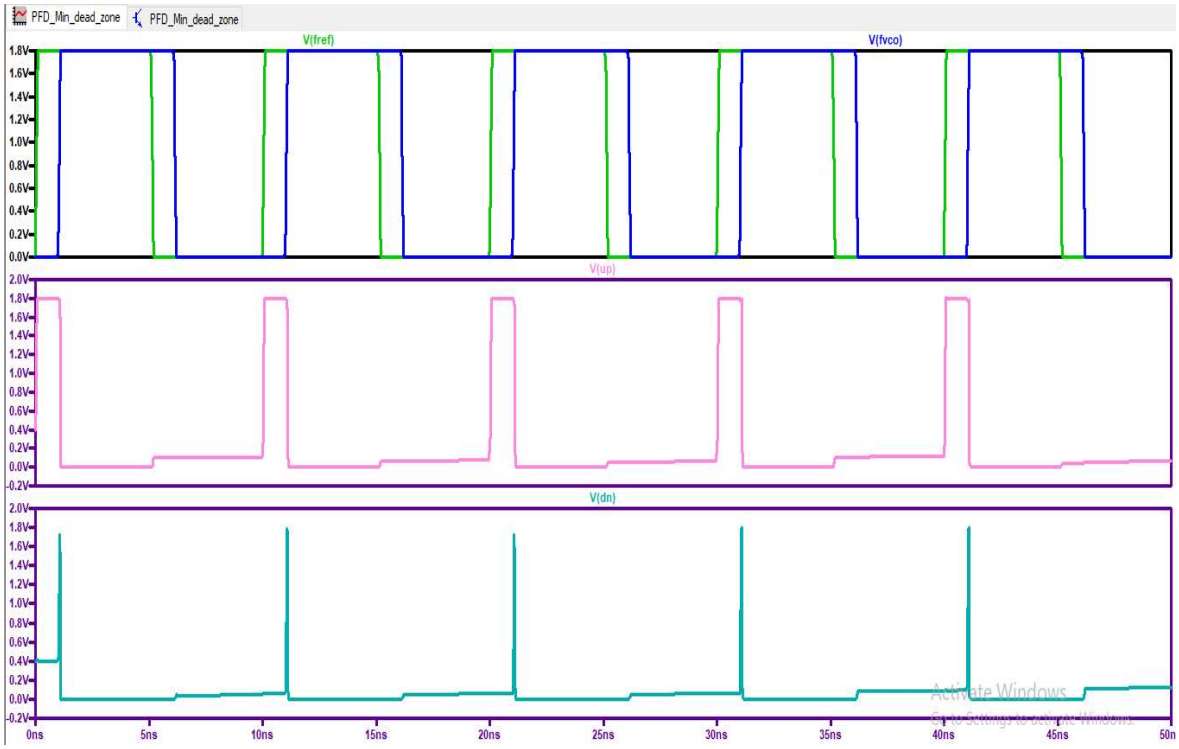


Fig 7.17:- Output Waveform at Q_A & Q_B when fref / Vref at V(in_a) is leading

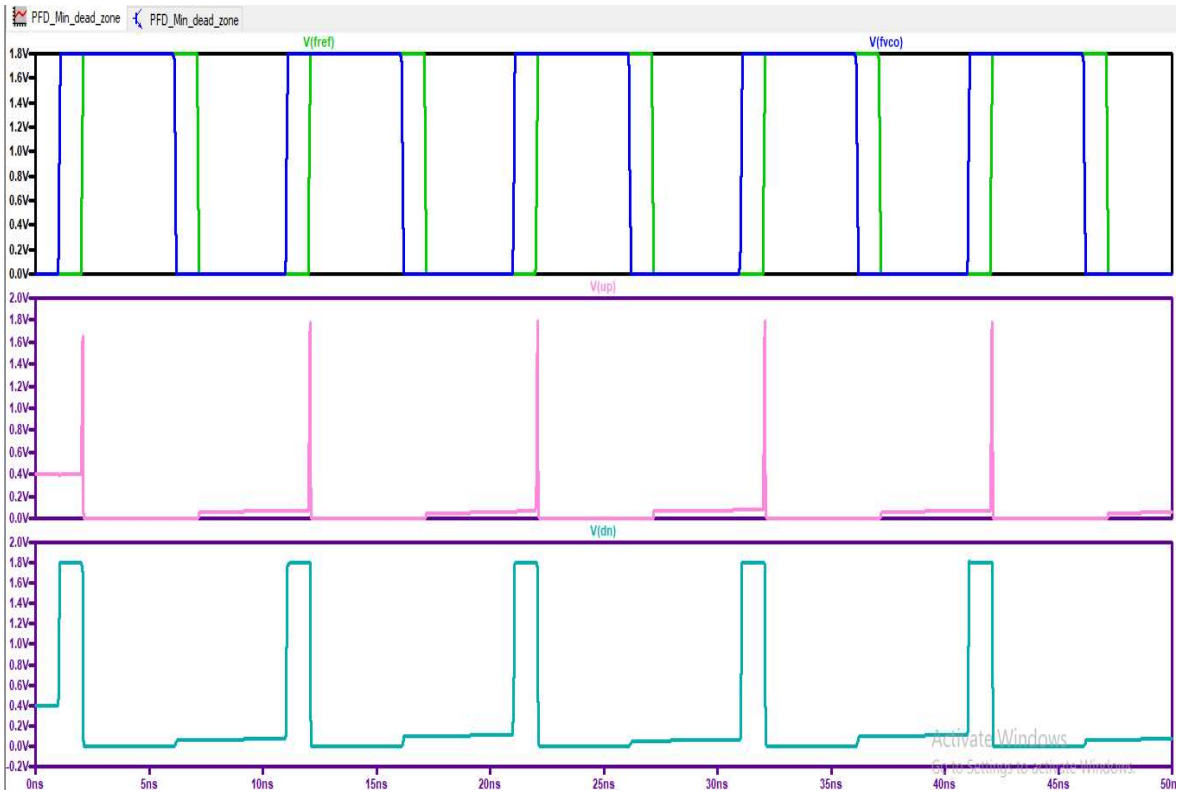


Fig 7.18:- Output Waveform at Q_A & Q_B when fref / Vref at V(in_a) is lagging

Table 7.6 – Comparative Study of Implemented PFDs

Parameters	Gate Level PFD	5T TSPC	Modified TSPC	Min. Dead Zone PFD
No. of transistors used	38	28	32	24
Power Dissipation (μW)	19.7205μW	6.3244μW	4.173μW	10.6526μW
Average Reset Delay (ps)	105.9188 ps	134.8815ps	141.6909ps	66.0345ps
Overlapping Pulse Width (ns)	130.687ps	192.2197ps	201.0712ps	109.4874ps

Conclusion: - For our PLL design we will be choosing Minimum Dead Zone PDF as it has lesser *transistor counts and Average Reset Delay and Overlapping pulse width* compared to the modified TSPC however it is the *power dissipation* of the Modified TSPC is almost half of the chosen circuit but overall performance of Min. Dead Zone PFD is better.

CHAPTER-8
Charge Pump and 2nd order LPF Designs

8.1 SWITCH AT DRAIN CMOS CHARGE PUMP

Fig 8.1 shows the fundamental switch-at-drain CP model. The basic CP switch-at-drain scheme introduces two MOS switches but works sub-optimally because of charge sharing. Leakage current, current mismatch and timing mismatch are three other major causes of non-ideal charge pump characteristics on which the level of reference spurs of the PLL depends. Switching errors caused by leakage current, charge injection, clock feed through, and charge sharing are also undesirable effects in charge pumps. When turned on, the MOS switch S1 stores charge in its channel. When they are partially turned off, some charge flows to the drain terminal, charging the charge pump's output load capacitor.

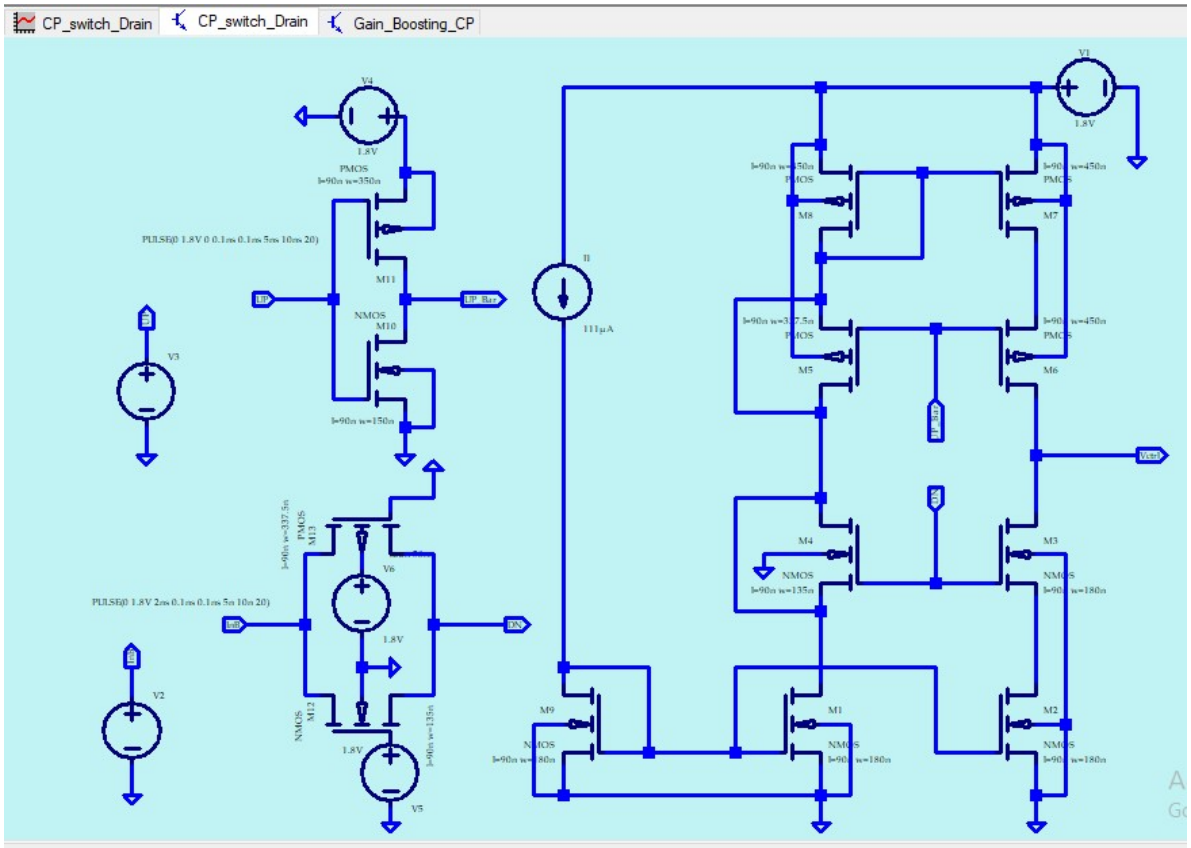


Fig 8.1:- Schematic Diagram of Switch at Drain based charge pump circuit

This causes charge injection, which amplifies the control voltage spikes. The charge pump output floats when the switch transistors are turned off. Sharing of charges occurs among the parasitic capacitance and the charge pump's output node when these transistors switch from OFF to ON, causing a deviation in the control voltage level. Clock feed through is caused by the fast rise and fall of the clock signal coupled into the signal node via the gate to source and gate to drain parasitic capacitances. It raises the signal level, which may cause the MOSFET's PN junction to forward bias, resulting in electron injection into the MOS's body and false operation as it passes through a nearby large impedance terminal.

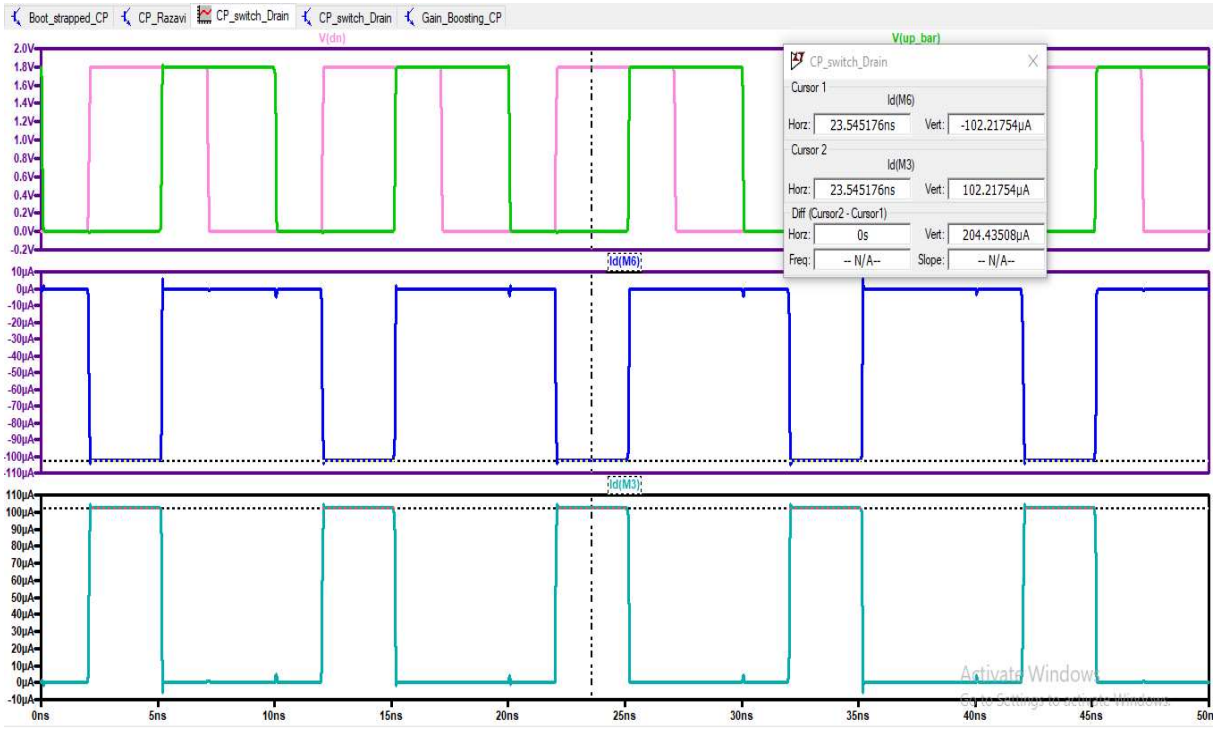


Fig 8.2:- Current Waveform plot at the output node of the Switch at Drain based CP circuit

8.2. BOOT STRAPPED CHARGE PUMP DESIGN

Fig 8.3 shows the Boot Strapped Charge Pump (CP) implementation used in design of the PLL. The supremacy of the Bootstrapped architecture is that it permits differential current steering; and can operate with low-swing UP, DN signals. Because of this, this circuit finds a strong space in PLLs used in high-speed reference clock signals. The term bootstrapped are fitting as the voltage follower opamp placed between the pull-up and

pull-down current networks which ensure an equal voltage level is maintined on either ends such a way that the pull-up current and the pull-down current is equal.

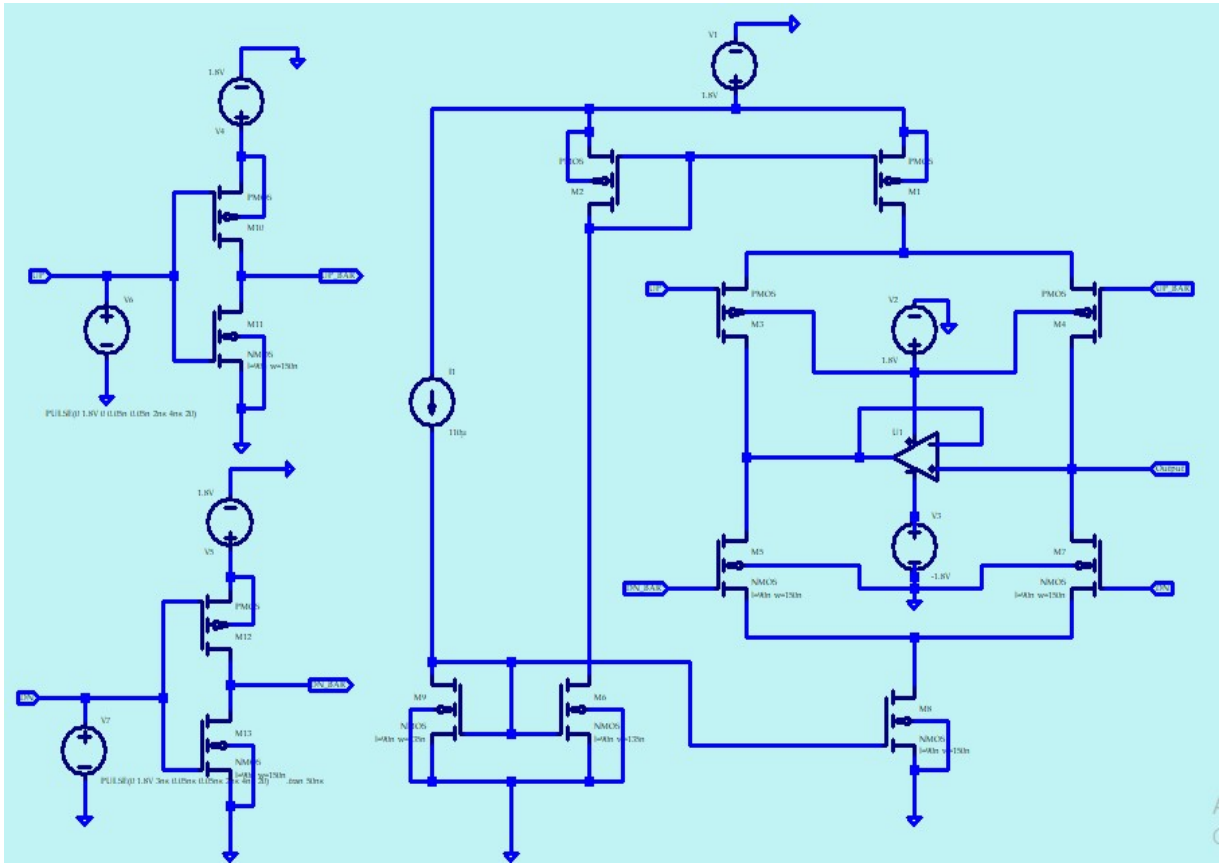


Fig 8.3:- Schematic Diagram of Boot Strapped Charge pump circuit

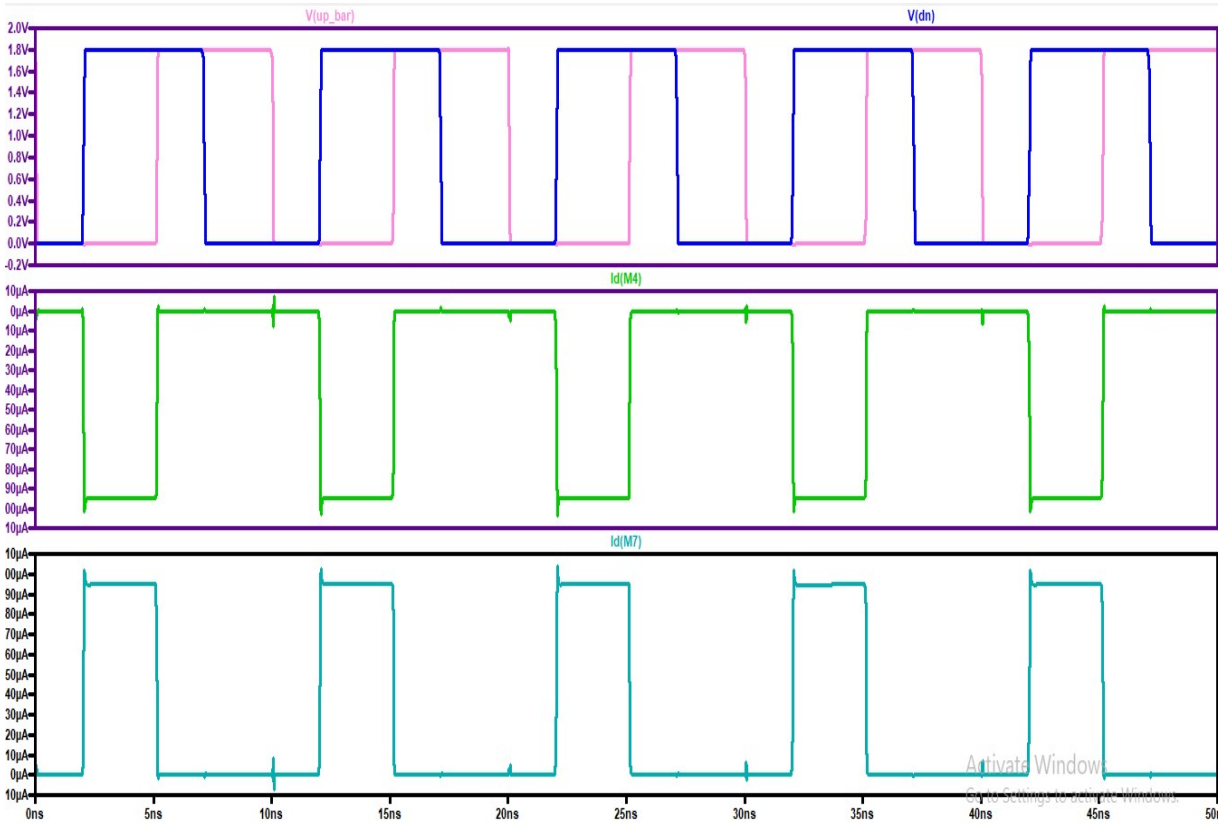


Fig 8.4:- Current Waveform plot at the output terminal of the Bootstrap C-P circuit

8.3. GAIN BOOSTING CHARGE PUMP DESIGN

Up and Down switches in conventional CMOS CPs are typically made of P_MOS & N_MOS, respectively. When depositing the charge to the LPF, a mismatch if currents happens due to the pMOS and nMOS Drain-Source voltage differences. In this note, a new CP circuit has been proposed with a gain-boosting circuit that uses only a little more transistors than a traditional CP. Idea is to use an amplifier to drive the gate of M2 and force V_x to equal V_b. As a consequence, because A3 regulates Vx, voltage variations at M2's drain have a lesser impact on Vx. Since the variability are smaller at node X, the current through r01 and thus the output current remain relatively constant, resulting in higher output impedance.

As a result, Rout can be significantly increased without the requirement to stack additional cascode devices on top of M2.

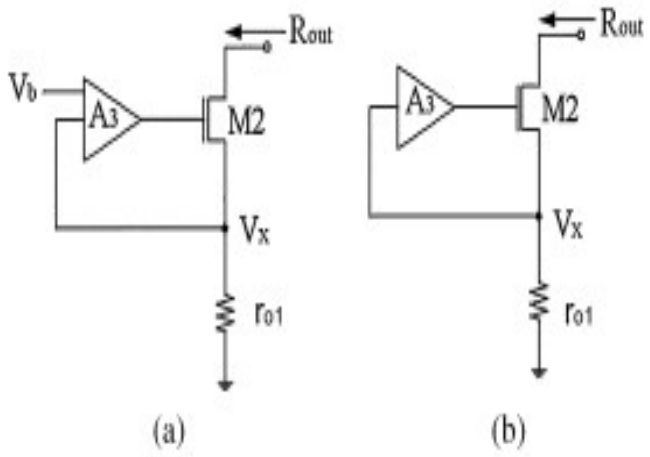


Fig 8.5:- (a) Gain boosting circuit principle (b) Condensed Structure

The proposed CP circuit, Transistor M_P4 and M_N4 are current springs for the single-transistor amplifiers M_N3 and M_P3 are shown in Fig. 8.6. The output impendence of M_N1 and M_P1 are used as R_{01} as shown in Fig. 8.5. M_N2 and M_N3 form a gain-boosting circuit with MN1 when the DN signal is active. This enhances the output impedance of the CP circuit and inhibits its current miss-matching attributes. This gain-boosting CP circuit is preferable for a low power supply voltage as it does not necessitate cascading more cascode circuits to increase the output impedence.

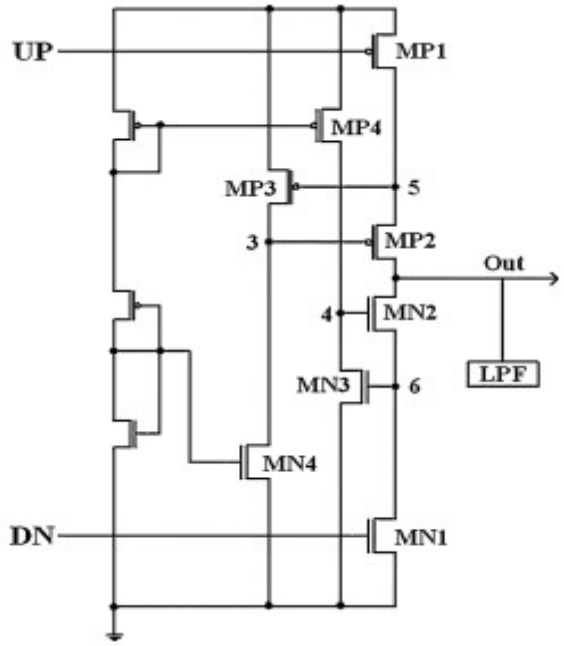


Fig 8.6:- Transistor level circuit diagram of a gain boosting circuit

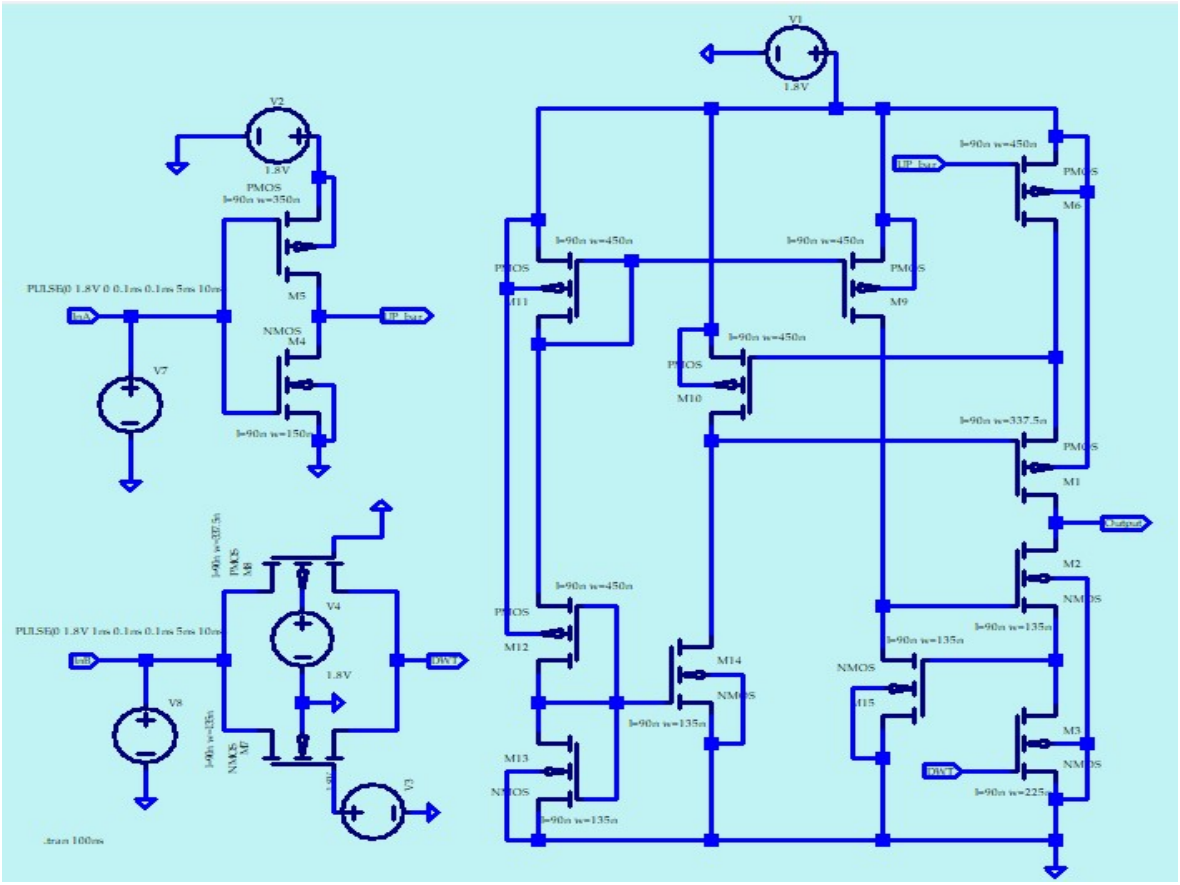


Fig 8.7:- Schematic Diagram of Gain Boosting Charge pump circuit

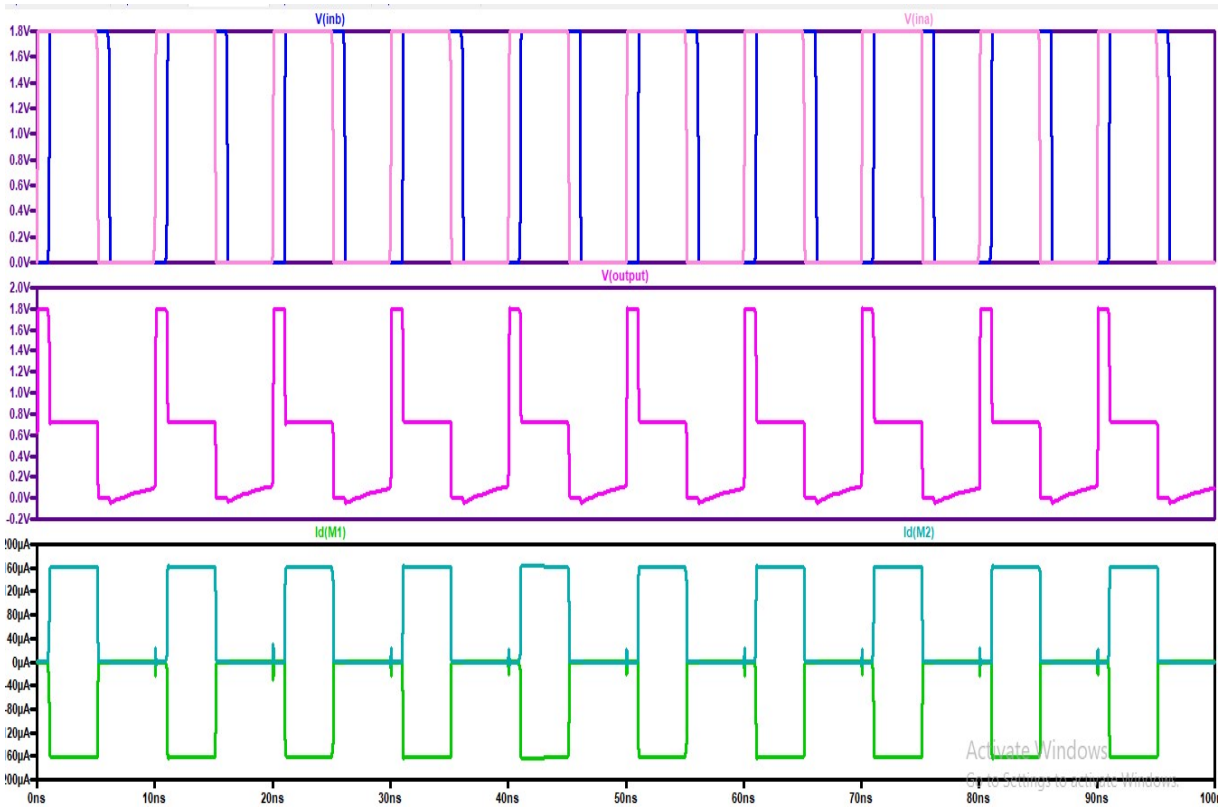


Fig 8.8:- Current Waveform plot at the output node of the Gain Boosting CP circuit

Table 8.1:-Calculations for Rp, Cp and C2 of Low Pass Filter using equations as mentioned in section 3.2 under Dynamics of Charge Pump Circuits

Type of CP	Icp (μA)	Rp (kΩ)	Cp (pf)	C2(pf)
Switch at drain CP	102.2175	1	7.63143	1.0902
Bootstrapped CP	117.12	1	8.0158	0.80158
Gain Boosting CP	161.707	1	4.8235	6.029

For the calculations of the parameters, Kvco is taken to be 34.3 rad/nsec/V (5.454 GHz/V), Σ is considered to be 0.8 and for simplification Rp is assumed to be 1 KΩ

Conclusion: - Bootstrap CP is chosen for PLL implementation as it has greater noise minimization over other.

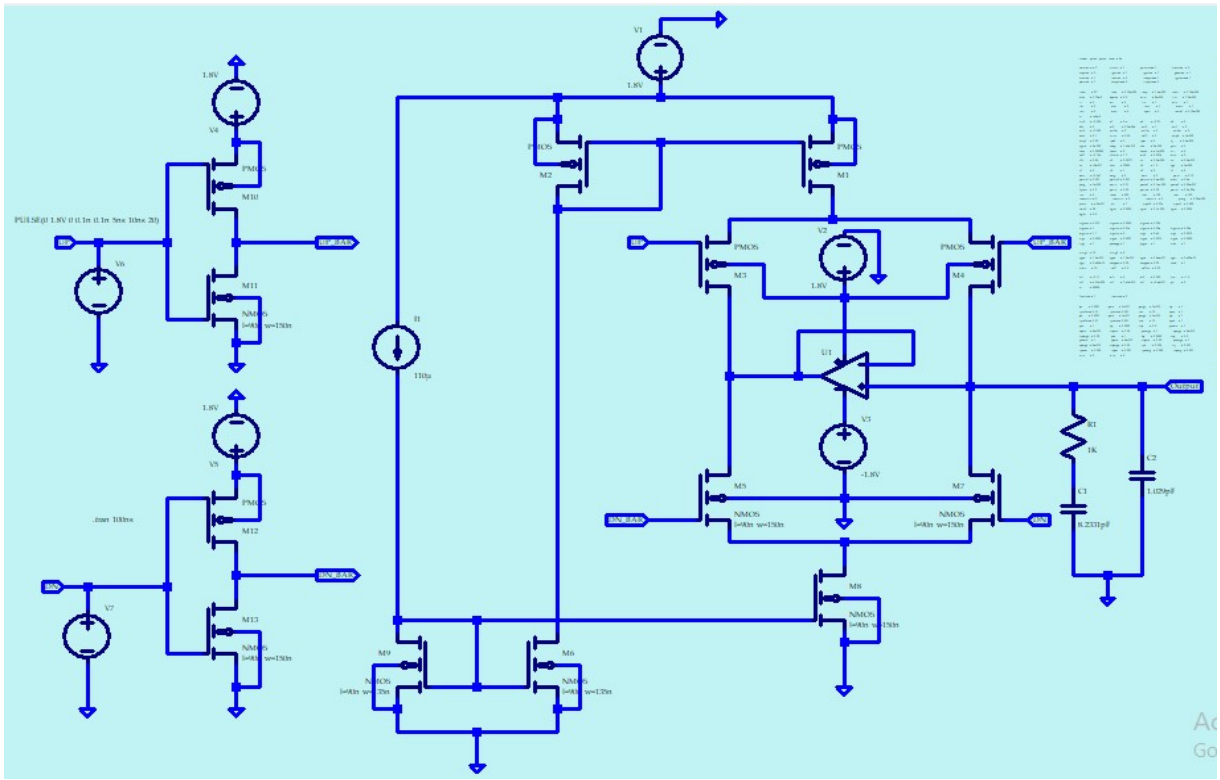


Fig 8.9:- Schematic of the Boot strapped circuit with 2nd order LPF implemented using Ltspice

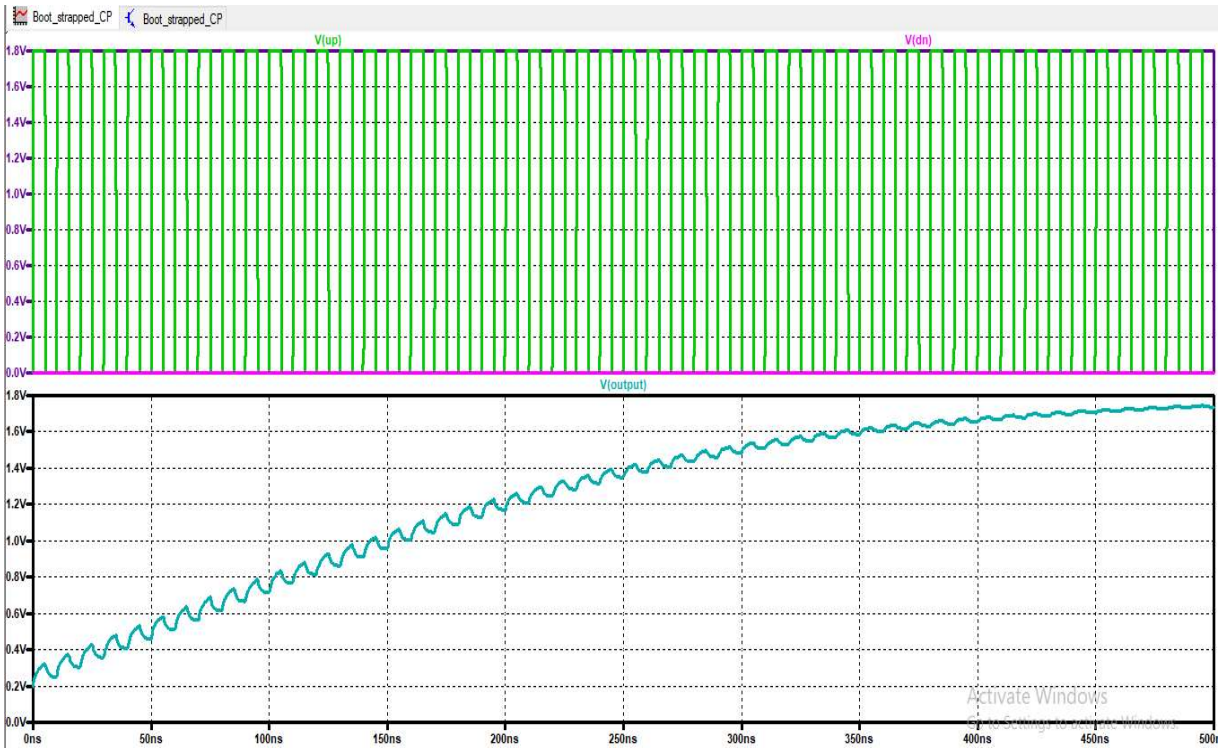


Fig 8.10:- Voltage Waveform plot at the output node of the Low Pass Filter circuit

CHAPTER-9
PLL Implementation and Simulation Results

Lock Range: It is the range of input frequencies over which the PLL will track the input frequency signal and has the capability of achieving the phase/frequency lock is called the Lock Range. If the input signal frequency is outside the PLL lock range then the PLL will be unable to lock the frequency/phase.

Capture Range: It is a subset of Lock Range and is the range of input frequencies over which the PFD and the VCO will react fast enough to achieve the phase/frequency lock.

Free Running Frequency: When there is no input control voltage given to the VCO, the output frequency that is obtained inherently is called the free-running frequency of the VCO.

Settling time: The time take for the output signal to achieve phase and frequency lock with the input signal is called the Settling time.

9.1. Schematic and Simulation Results of the Frequency Divider circuit:-

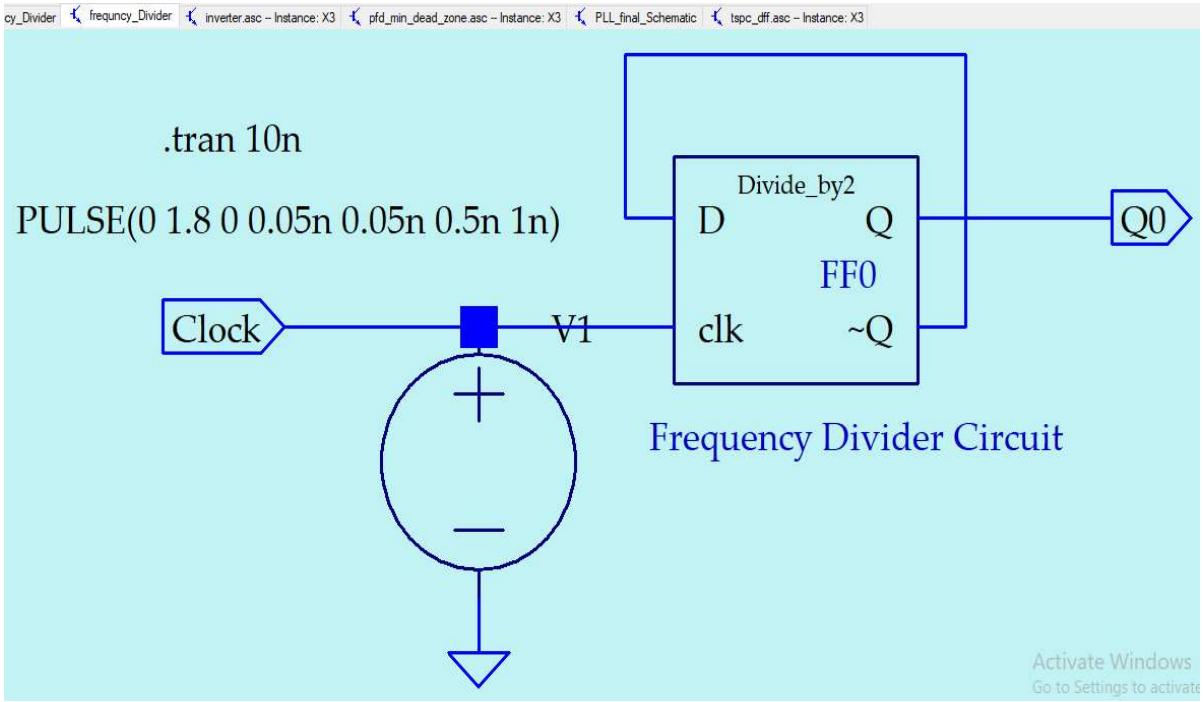


Fig 9.1:- Schematic diagram of the Frequency Divider Circuit

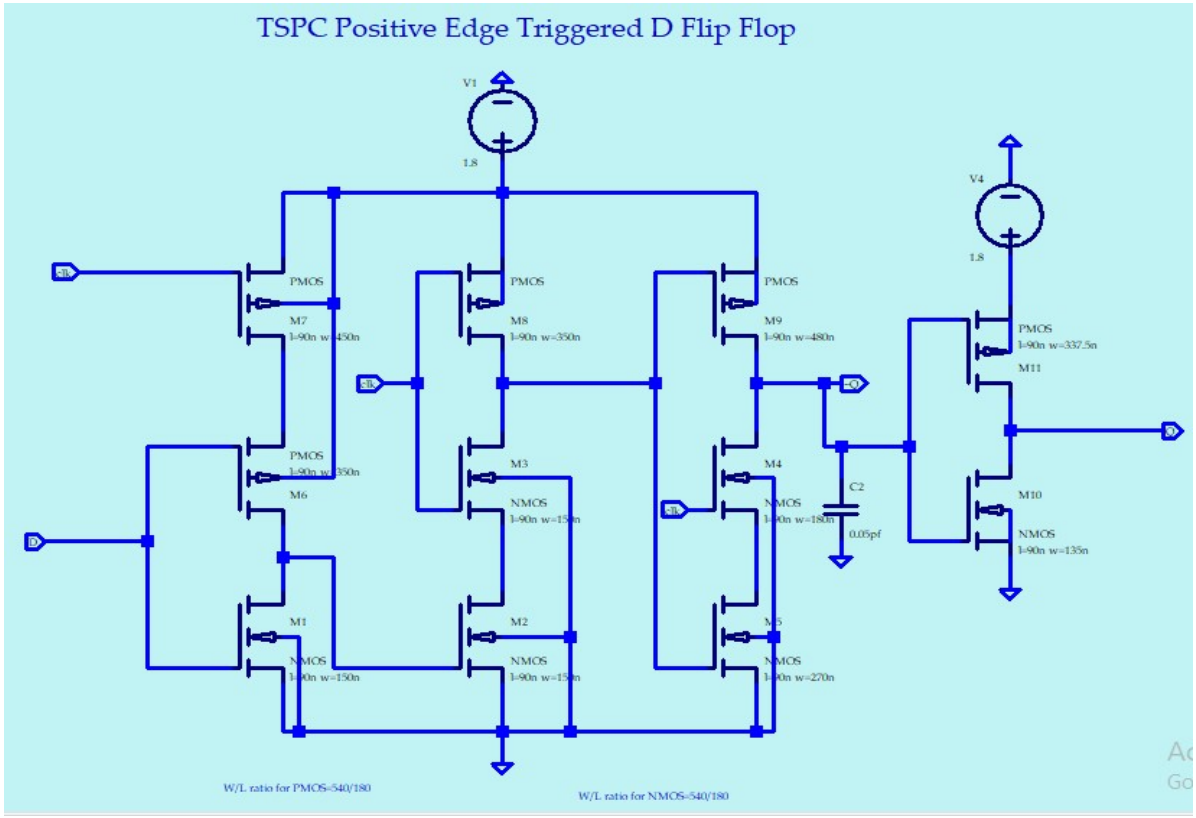


Fig 9.2:- Schematic diagram of the TSPC Master-Slave edge triggered D-FF

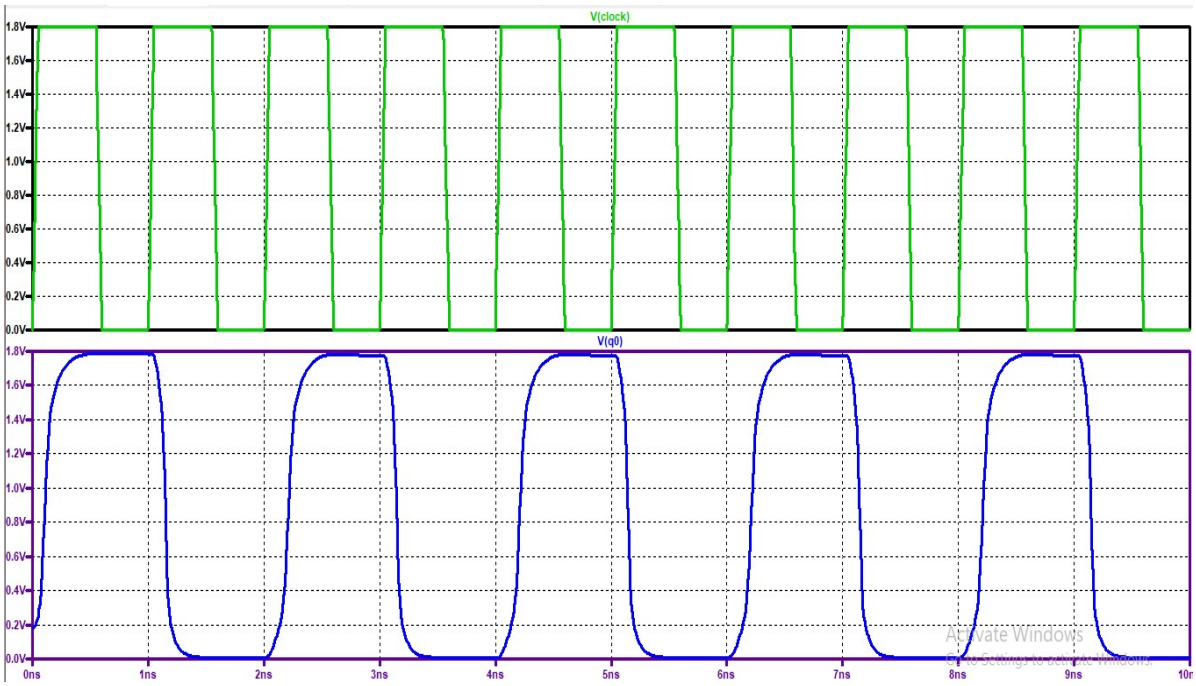


Fig 9.3:- Output Waveform of the frequency divider circuit simulated using Ltspice

9.2. Schematic and Simulation Results of the PLL circuit

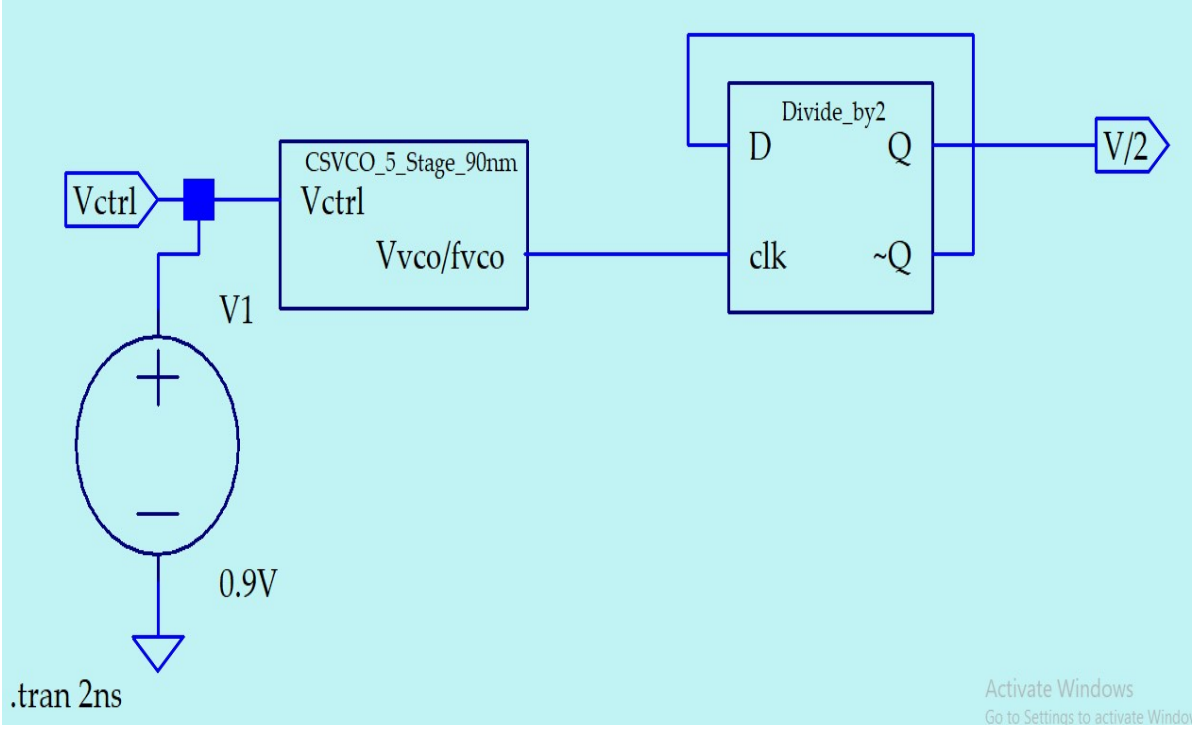


Fig 9.4:- Schematic diagram of the interconnection of CSVCO and TSPC DFF for Fvco/2

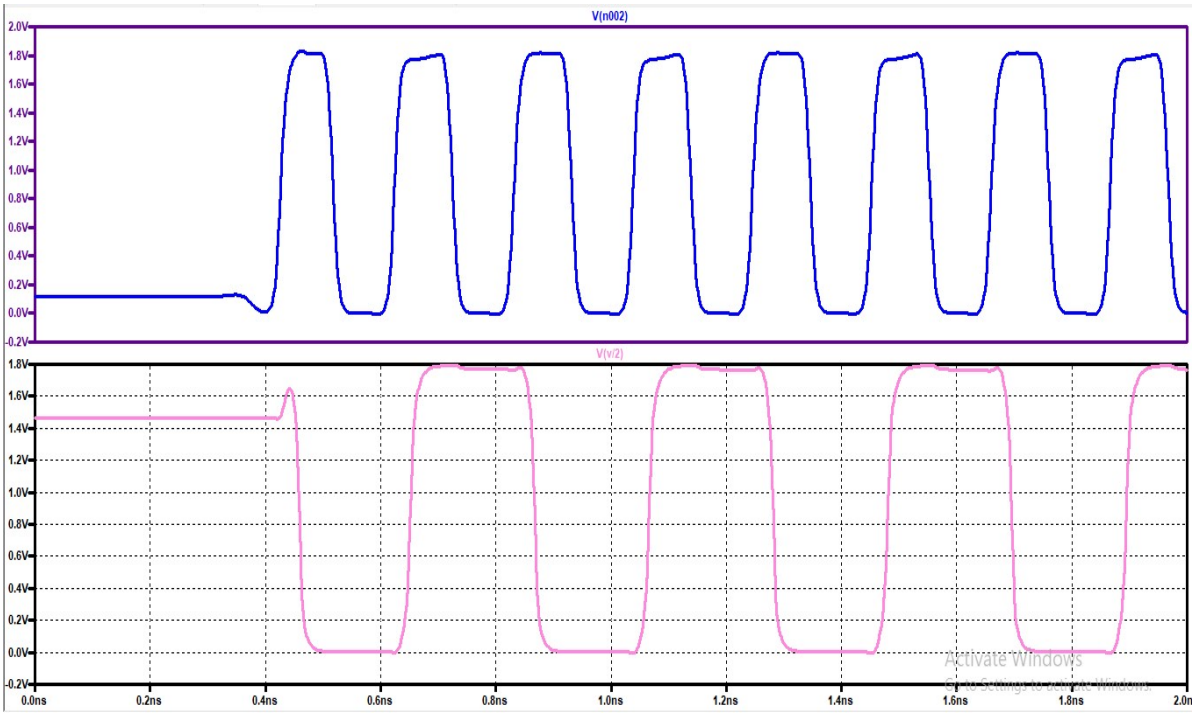


Fig 9.5:- Output wave form of the Fvco and Fvco/2 signal

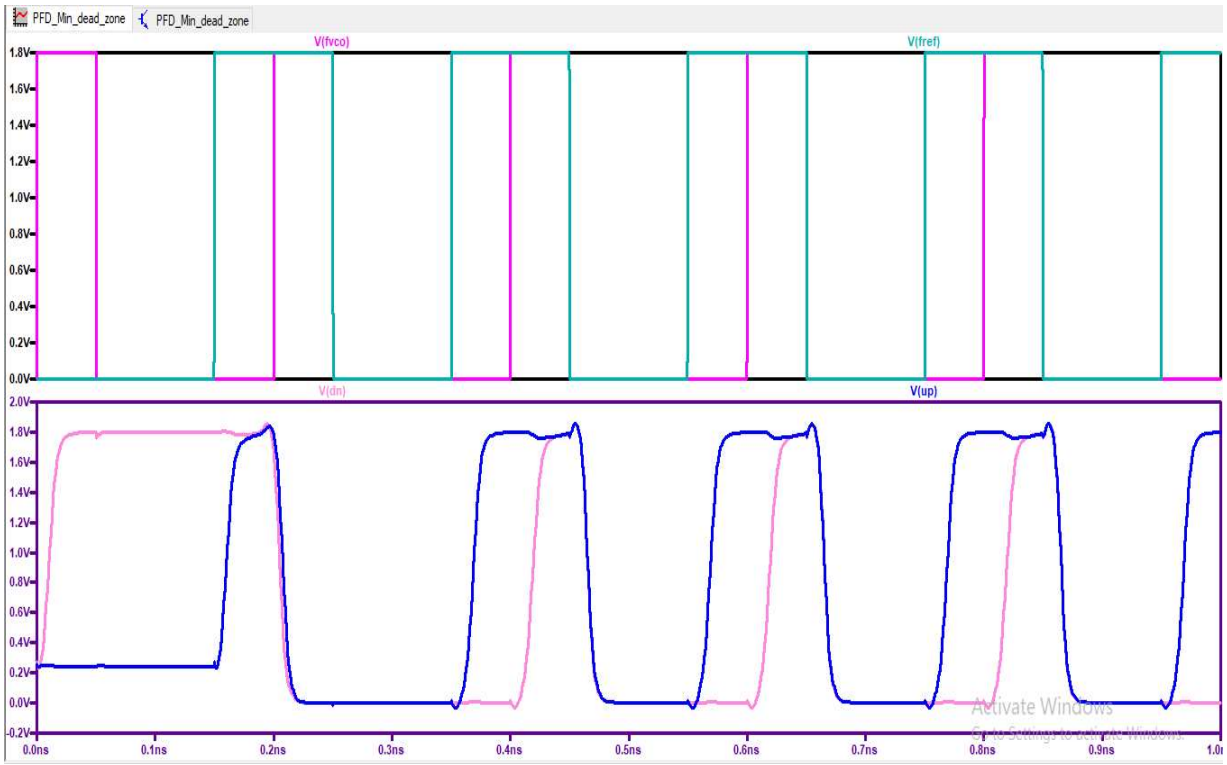


Fig 9.6:- Input and output waveform plot of the PFD block

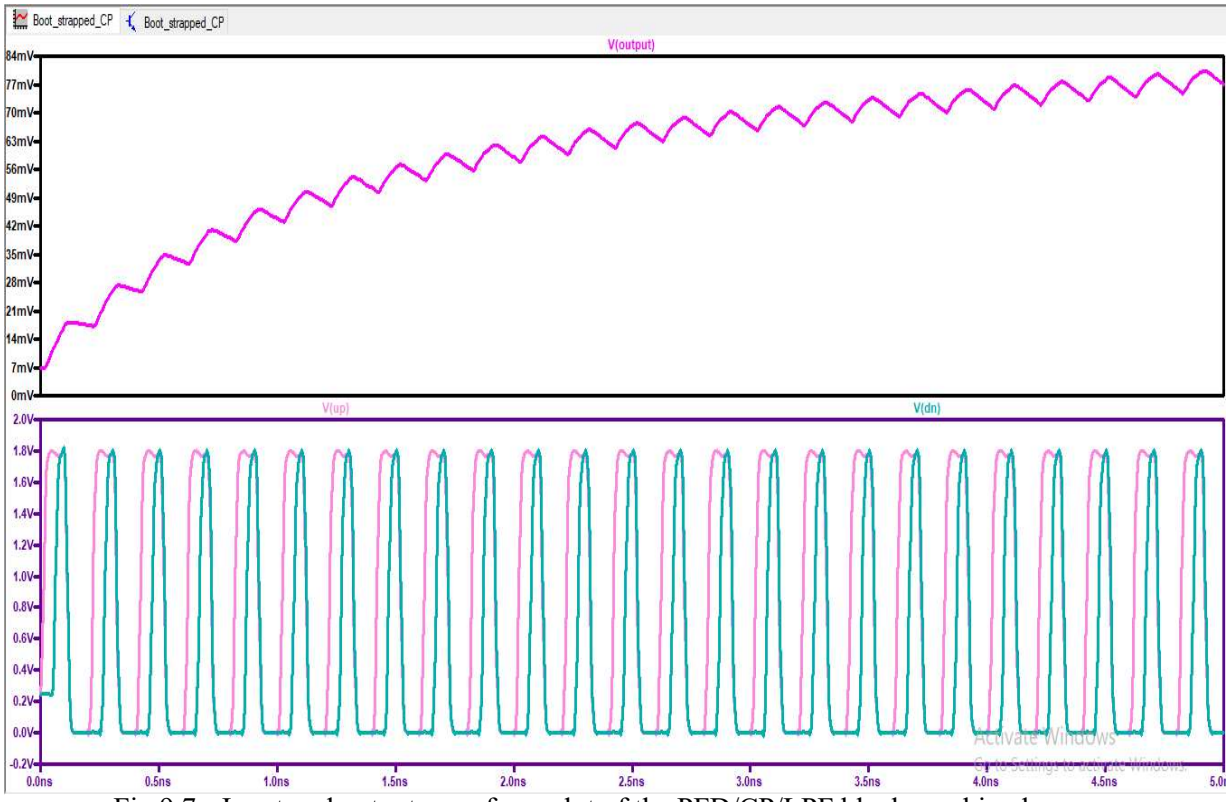


Fig 9.7:- Input and output waveform plot of the PFD/CP/LPF block combined

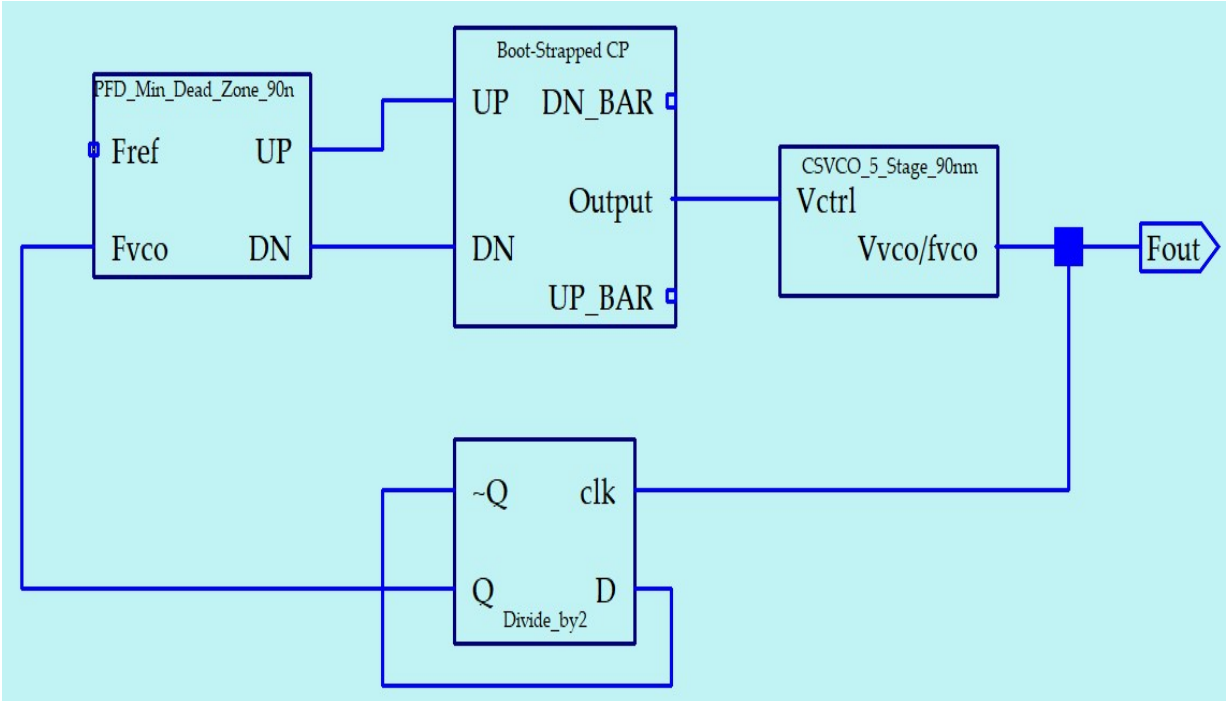


Fig 9.8:- Schematic Diagram of the PLL with no input for the calculation of Free Running Frequency

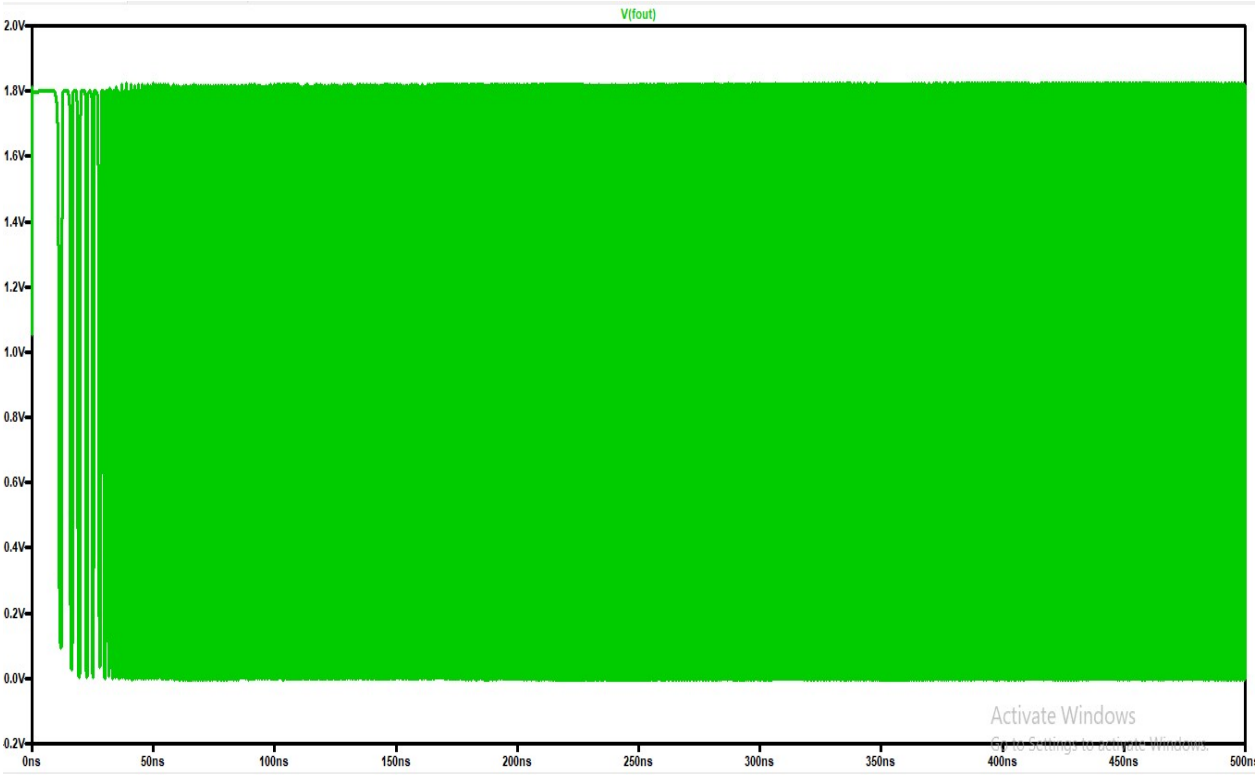


Fig 9.8:- Output waveform of the PLL for the calculation with no input signal

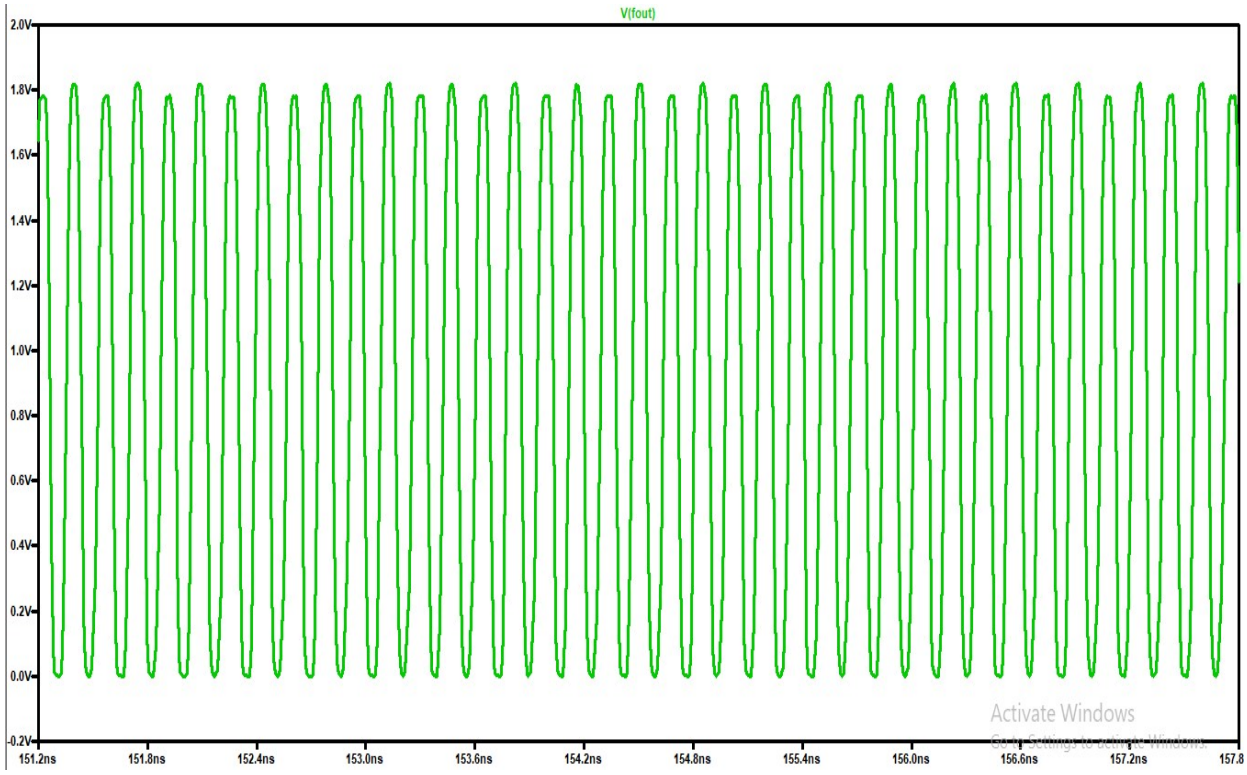


Fig 9.9:- Expended view of output waveform of the PLL for the calculation with no input signal

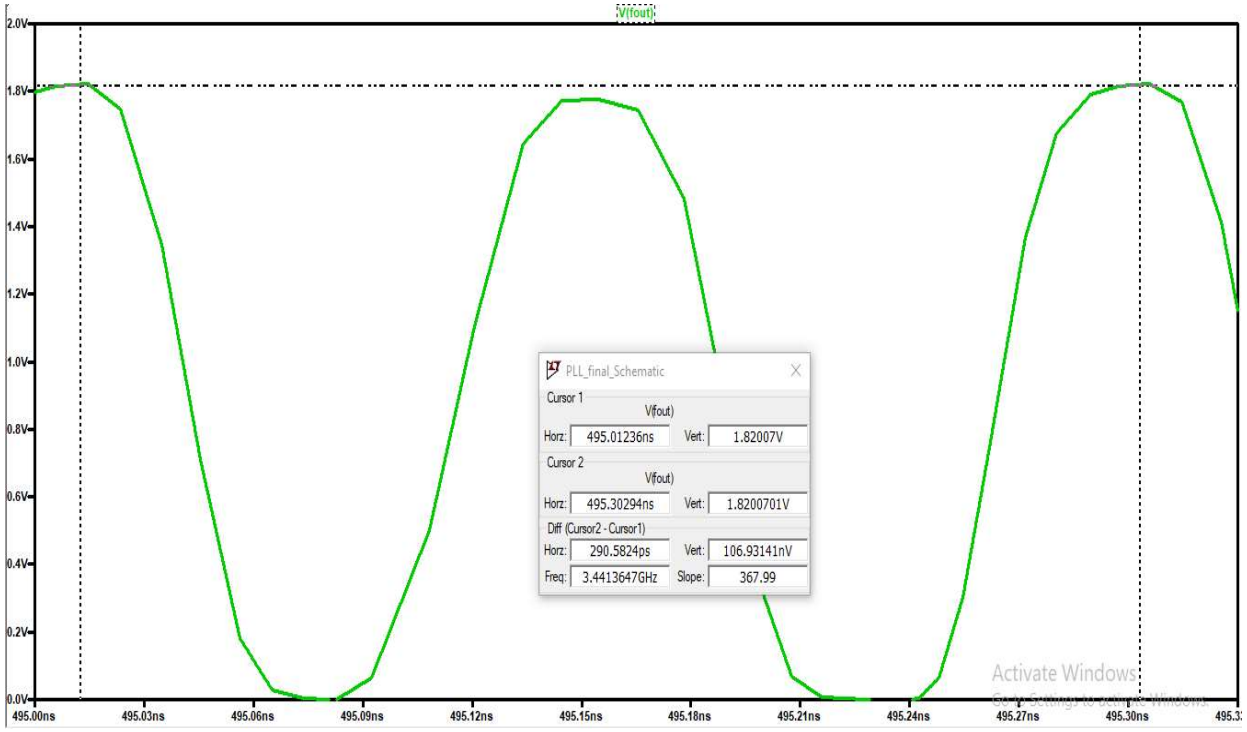


Fig 9.10:- Expended view of output waveform of the PLL for the calculation with free Running frequency of the PLL

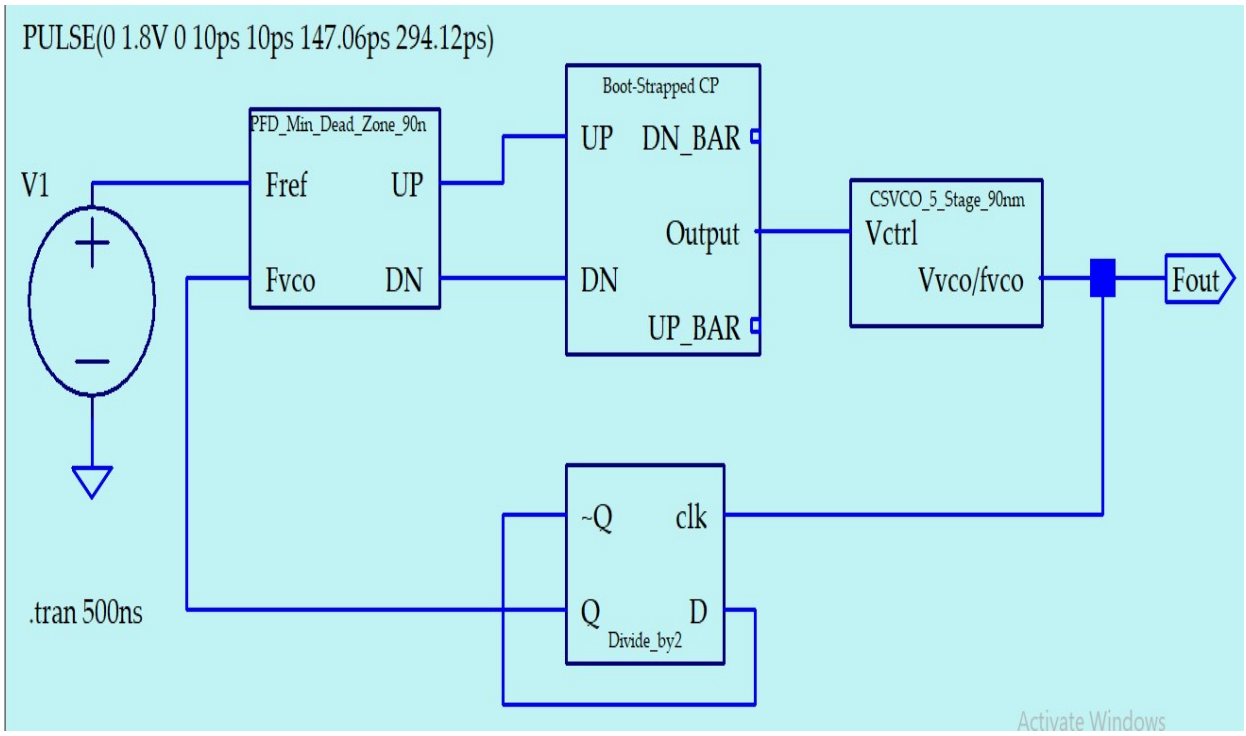


Fig 9.11:- Schematic Diagram of the implemented PLL circuit

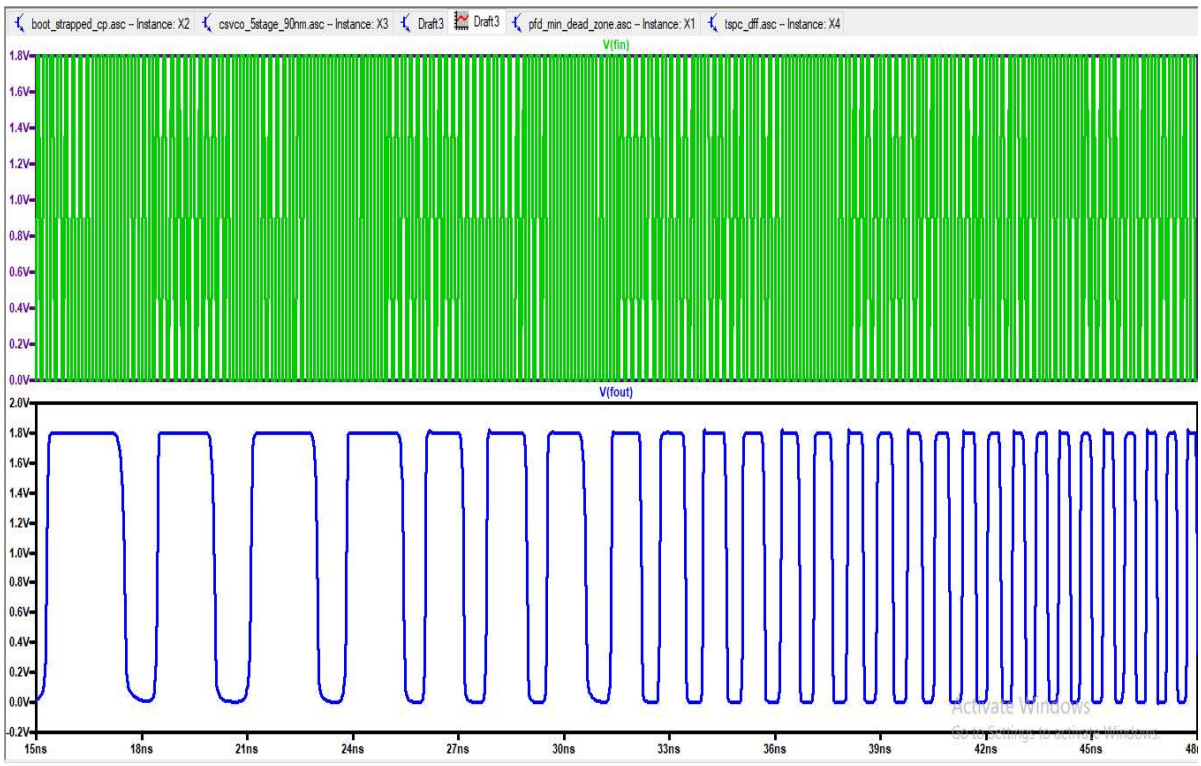


Fig 9.12:- Zoom in view of the Input and output waveform plot of the PLL

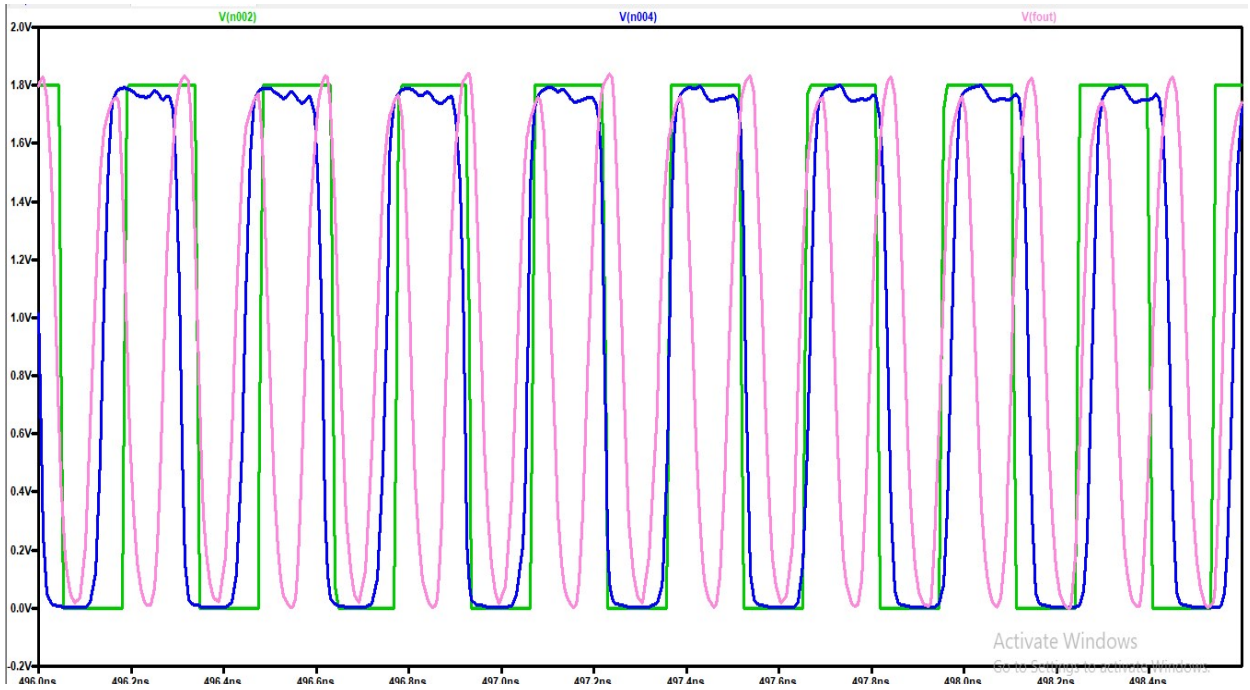


Fig 9.12:- Zoom in view of the Input waveform (V(n002)), Divider waveform (V(n004)) and VCO output waveform (V(fout))

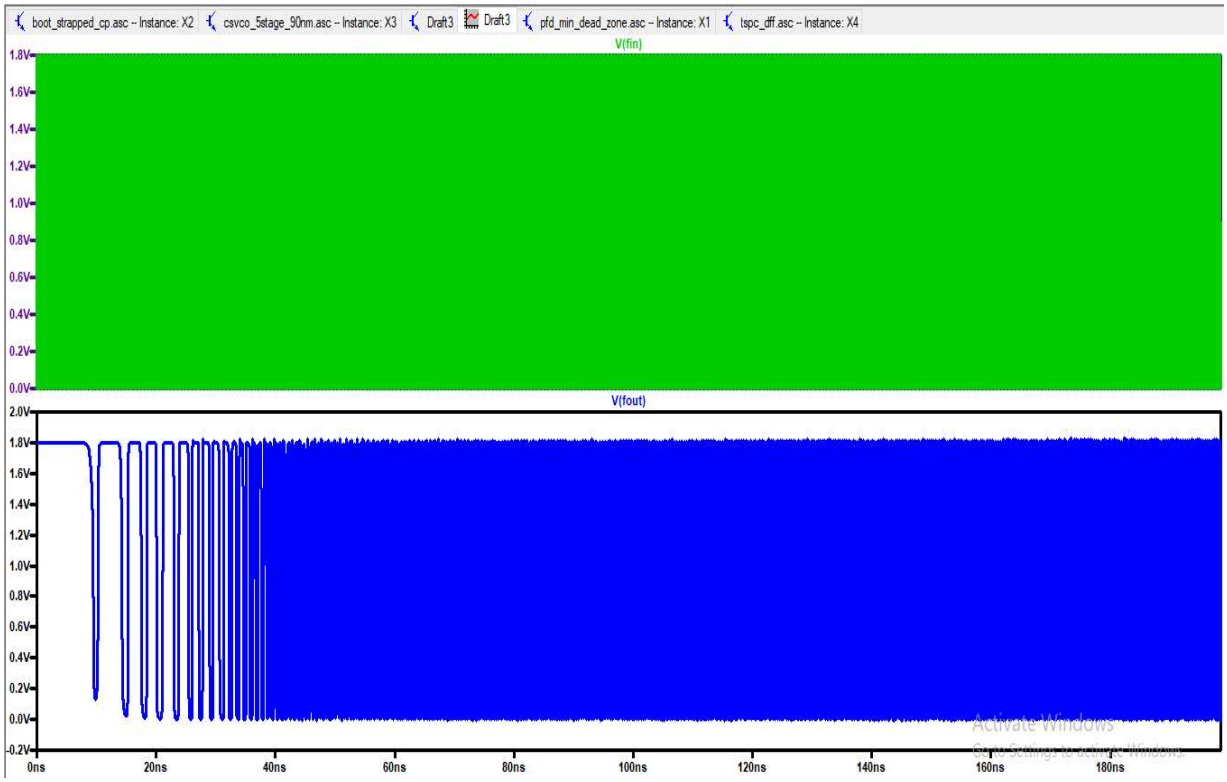


Fig 9.13:- Input and VCO output waveform plot of the PLL in a normal view.

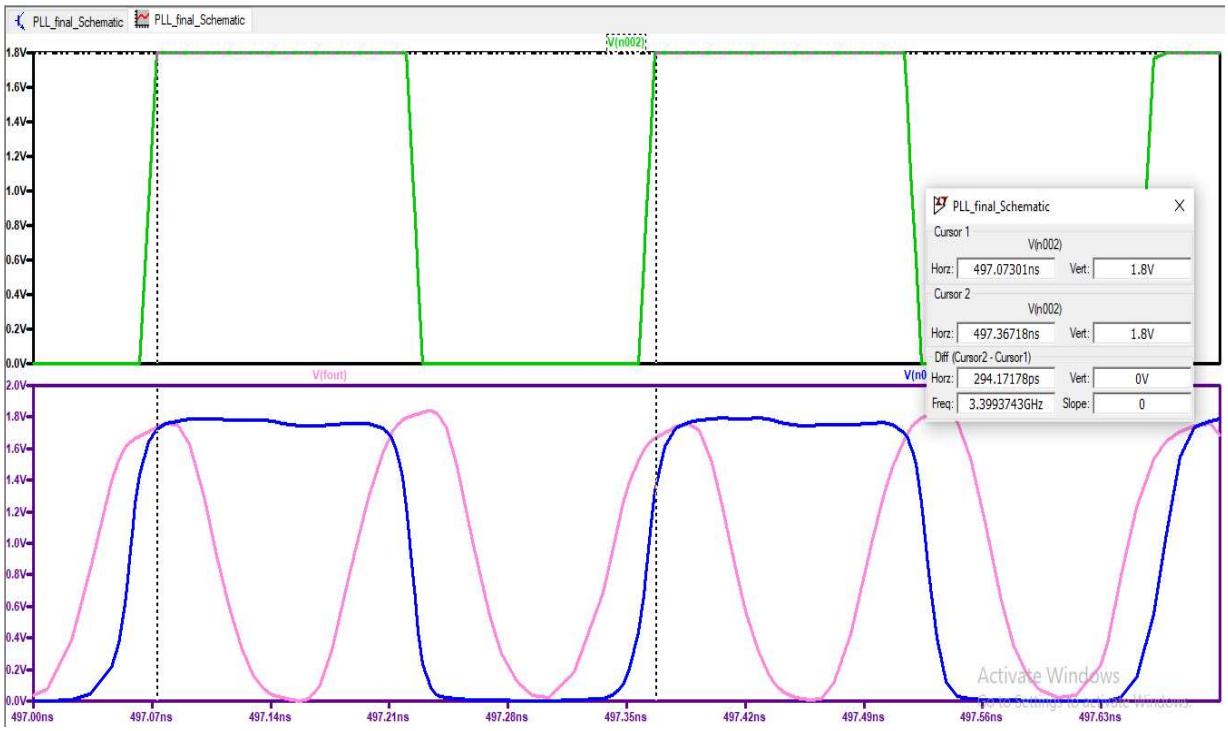


Fig 9.14:- Frequency measurement of the input signal from the output waveform.

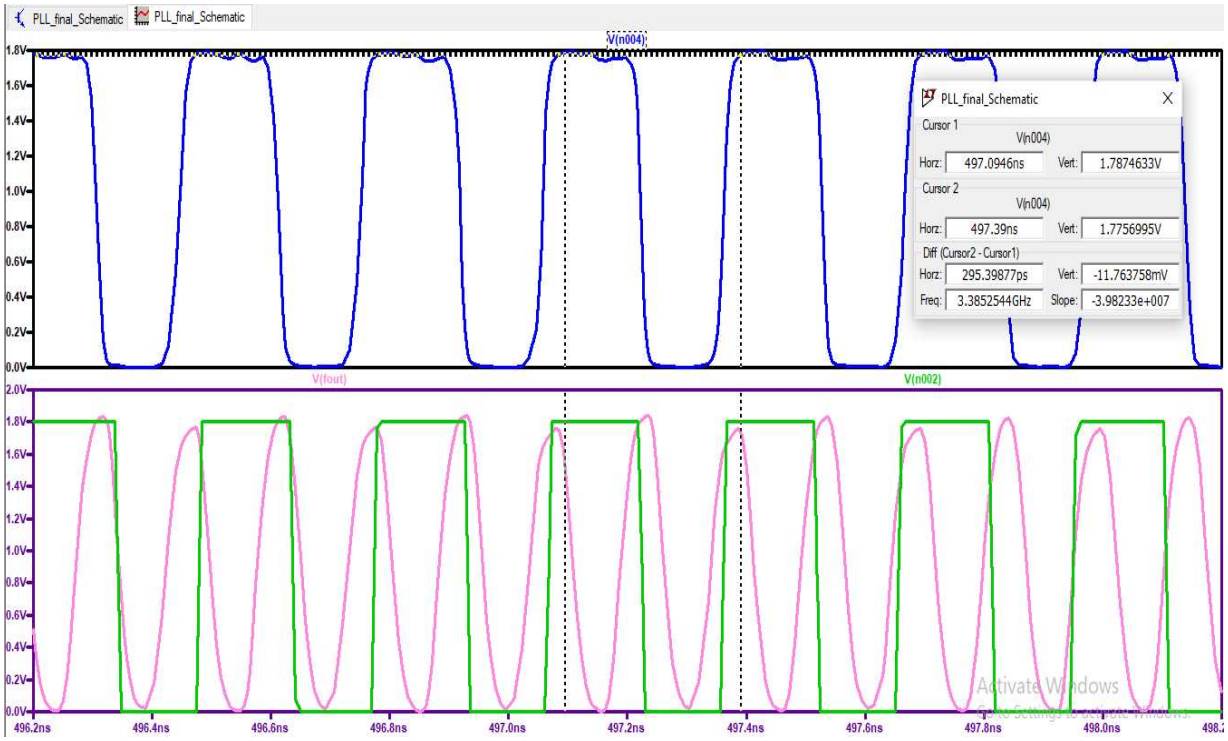


Fig 9.15:- Frequency measurement of the frequency divider output signal from the waveform

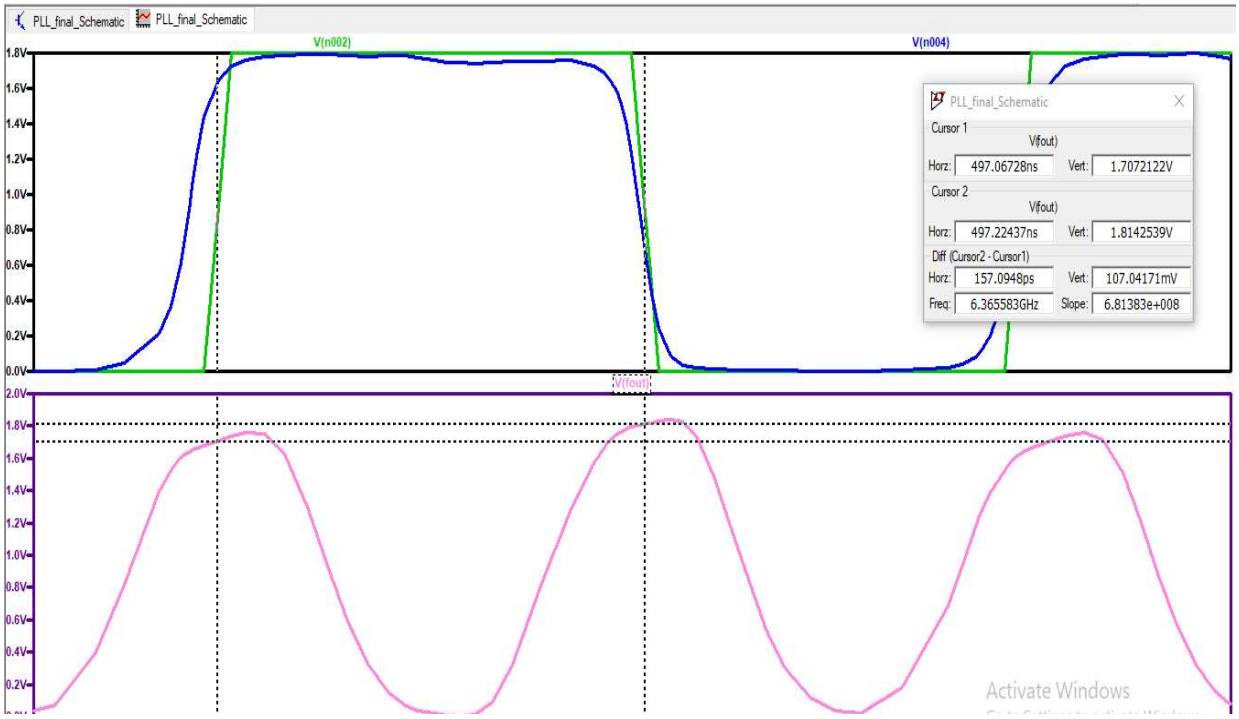


Fig 9.16:- Frequency measurement of the VCO output signal for given input.

Table 9.1:- Calculated values and Measured Values of PLL parameters

Cutoff frequency of the LPF (ω_{LP})	**1.985 GHz**
Natural frequency of the PLL (ω_n)	**3.29 GHz**
Quality Factor	**1.6575**
Free Running Frequency	**6.883 GHz**
Lock Range Δf_{Lock}	**5.7115 GHz**
Capture Range $\Delta f_{capture}$	**4.1234 GHz**
Input Frequency	**3.4 GHz**
VCO output Frequency	**6.3656 GHz**
Frequency Divider Output	**3.384 GHz**

CHAPTER-10
Conclusion and Future Scope

A PLL is an interconnection of different blocks that has their own individual task to be performed to provide desire output. Various design styles of CMOS based ***Charge Pump, Phase and Frequency detectors and Voltage controlled Oscillators*** have been studied thoroughly for implementation of PLL and are analysed and simulated at 90nm technology using Ltspice simulator.

The 5-stage Voltage Controlled Ring Oscillator was chosen for the PLL implementation because the linearity range of a three-stage CSVCO deteriorated and the output frequency of operation for a seven-stage VCO was drastically reduced. As a result, a 5 stage VCO with a good linearity range and a higher output frequency was used.

The Minimum Dead Zone PFD design is chosen because it has fewer transistors count, a relatively short reset delay and overlapping pulse width compared to the other PFD designs. However, the power dissipation of the modified TSPC based PFD design is nearly half that of the chosen circuit, but its overall performance of prior one is superior.

The CP is chosen based on the PLL's application and the scheme's complexity. The CP output characters have the greatest influence on PLL presentation. Least current miss-match, zero mean current, and net zero charge are required for CP-based PLLs because they have a noticeable impact on phase offset, which enhances spurr in PLL. The phase offset may limit the locking range and impair PLL performance. Because it provides perfect current matching, the source switching op-amp CMOS CP outperforms the other two alternatives.

Working onwards on PLL, I would like to design Voltage Controlled Oscillators using multiple techniques and then integrate with the Phase Detector, Charge Pump and Low Pass designs which should not compromise the fidelity of the PLLs while utilizing least power and transistors.

REFERENCES

[1] Behzad Razavi, “Design of Analog CMOS Integrated Circuits”, McGraw Hill International Edition, (2001).

[2] Roland E. Best, “Phase-Locked Loops – Design, Simulation and Applications”, Fifth Edition McGraw Hill.

[3] David A. Johns and Ken Martin, “Analog Integrated Circuit Design”, John Wiley & Sons,Inc.

[4] Jan M. Rabaey, “ Digital Integrated Circuits – A Design Pespective”, Pearson Education Second Edition 2008.

[5] Jyoti Gupta, Ankur Sangal, Hemlata Verma- “ High Speed CMOS Charge Pump Circuit for PLL Applications using 90nm CMOS Technology”- IEEE World Congress on Information and Communication Technologies - 2011

[6] Young- Shig Choi and Dae-Hyun Han – “ Gain Boosting Charge Pump for Current Matching in Phase-Locked Loop”, IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 53, NO. 10, OCTOBER 2006

[7] Nabihah Ahmad, Nur Atikah Binti Ishaimi, M. Hairol Jabbar, “Charge Pump and Loop Filter for Low Power PLL Using 130nm CMOS Technology”, International PostGraduate Conference on Applied Science & Physics 2017

[8] Hiren B. Ravisaheb , Bharat H. Nagpara, “Design and Implementation of Phase Frequency Detector Using Different Logic Gates in 45nm CMOS Process Technology“ - International Research Journal of Engineering and Technology 2017.

[9] Aniruddha Kailuke , Pankaj Agrawal , R. V. Kshirsagar, “Design of Low Power, Low Jitter PLL for WiMAX Application in 0.18 µm CMOC Process” International Conferernce on Pervasive Computing Advances and Applications – 2019.

[10] Kanika Garg and V. Sulochana Verma, “Low Power Design Analysis of PLL Components in Submicron Technology”, Springer-Verlag Berlin Heidelberg 2013.

[11] Yashpal, “Design and Implementation of Phase Locked Loop Using Current Starved Voltage Controlled Oscillator”, Research India Publications.

[12] Guan-Chyun Hsieh, “Phase-Locked Loop Techniques-A Survey” , IEEE Transactions On Industrial Electronics, VOL. 43, NO. 6, DECEMBER 1996.

[13] Ashish Tiwari and Renu Prabha Sahu, “Design and Analysis of Low-Power PLL for Digital Applications”, , International Conference on Advanced Computing Networking and Informatics, Advances in Intelligent Systems and Computing 870, Springer Nature Singapore Pvt Ltd. 2019.

[14] Ashwini. H, Rohith. S, Sunitha. K. A, “Implementation of High Speed and Low Power 5T-TSPC D Flip-flop and Its Application”, IEEE International Conference on Communication and Signal Processing, April 6-8, 2016, India.

[15] Aniruddha C. Kailuke, Pankaj Agrawal , R. V. Kshirsagar,” Fast Frequency Acquisition Phase Frequency Detector with Minimal Dead Zone for High Frequency Phase Lock Loop”, Conference Paper 2021.

[16] Jahangir Shaikh, Hafizur Rahaman, “High speed and low power preset-able modified TSPC D flip-flop design and performance comparison with TSPC D flip-flop”.

[17] M. Bhardwaj and S. Pandey, "Design and Performance Analysis of Wideband CMOS Voltage Controlled Ring Oscillator," 2nd International Conference on Electronics and Communication Systems (ICECS), Coimbatore, pp. 142-145, 2015

[18] Rahul Shandilya, RK Sharma "Low Power Positive-Edge Triggered D-type flip-flop" ICEI IEEE 2017

16% Overall Similarity

Top sources found in the following databases:

- 9% Internet database
- Crossref database
- 12% Submitted Works database
- 7% Publications database
- Crossref Posted Content database

TOP SOURCES

The sources with the highest number of matches within the submission. Overlapping sources will not be displayed.

1	**electrovolt.ir** Internet	1%
2	**ee.nchu.edu.tw** Internet	<1%
3	**Aniruddha Kailuke, Pankaj Agrawal, R.V. Kshirsagar. "Design of Low Po...** Crossref	<1%
4	**slideshare.net** Internet	<1%
5	**archive.org** Internet	<1%
6	**Malaviya National Institute of Technology on 2012-06-15** Submitted works	<1%
7	**ethesis.nitrkl.ac.in** Internet	<1%
8	**Universiti Putra Malaysia on 2018-05-28** Submitted works	<1%

9	Institute of Technology Carlow on 2021-04-22 Submitted works	<1%
10	Vel Tech University on 2018-01-11 Submitted works	<1%
11	troindia.in Internet	<1%
12	iGroup on 2011-03-24 Submitted works	<1%
13	B.V. B College of Engineering and Technology, Hubli on 2020-06-06 Submitted works	<1%
14	CSU, San Jose State University on 2008-12-11 Submitted works	<1%
15	Universiti Sains Malaysia on 2018-06-06 Submitted works	<1%
16	University of Southampton on 2006-10-06 Submitted works	<1%
17	freepatentsonline.com Internet	<1%
18	9lib.co Internet	<1%
19	University of Brighton on 2018-06-21 Submitted works	<1%
20	fliphtml5.com Internet	<1%

21	Yoshimura, Tsutomu, Shuhei Iwade, Hiroshi Makino, and Yoshio Matsu... Crossref	<1%
22	Sheffield Hallam University on 2020-04-27 Submitted works	<1%
23	Taylor's Education Group on 2016-06-20 Submitted works	<1%
24	Universiti Sains Malaysia on 2018-07-20 Submitted works	<1%
25	Higher Education Commission Pakistan on 2017-08-16 Submitted works	<1%
26	Imperial College of Science, Technology and Medicine on 2018-09-06 Submitted works	<1%
27	Kenji Suyama. "Target sound extraction utilizing similarity between sig... Crossref	<1%
28	Indian Institute of Technology, Kharagpure on 2013-04-24 Submitted works	<1%
29	P. Nagarajan, N. Ashok Kumar, Joshuva Arockia Dhanraj, T. Senthil Ku... Crossref	<1%
30	Vel Tech University on 2018-01-17 Submitted works	<1%
31	mafiadoc.com Internet	<1%
32	pt.scribd.com Internet	<1%

33	Coventry University on 2010-03-02 Submitted works	<1%
34	Imperial College of Science, Technology and Medicine on 2020-09-02 Submitted works	<1%
35	Integrated Fiber-Optic Receivers, 1995. Crossref	<1%
36	L. Hebrard, J.-B. Kammerer, F. Braun. "A chopper stabilized biasing cir... Crossref	<1%
37	dbatu.ac.in Internet	<1%
38	ijarf.com Internet	<1%
39	qspace.library.queensu.ca Internet	<1%
40	Cranfield University on 2010-01-08 Submitted works	<1%
41	Griffth University on 2017-03-30 Submitted works	<1%
42	M. A. van Wyk, W.-H Steeb. "Chapter 6 Driven Systems", Springer Scien... Crossref	<1%
43	University of Southampton on 2006-09-28 Submitted works	<1%
44	"Current-Mode Phase-Locked Loops with Active Inductors & Transform... Crossref	<1%

45	Handong Global University Graduate School on 2015-08-13 Submitted works	<1%
46	Texas A&M University, College Station on 2021-01-27 Submitted works	<1%
47	Thomas C. Jackson, Rongye Shi, Abhishek A. Sharma, James A. Bain, ... Crossref	<1%
48	sportdocbox.com Internet	<1%
49	Li Su-jie Gong Qian. "Design of a CPPLL-based clock multiplier for USB... Crossref	<1%
50	M.-L. Yeh. "A Low-voltage low-power programmable 5 GHz frequency s... Crossref	<1%
51	T. Baba. "Demonstration of a novel multiple-valued T-gate using multip... Crossref	<1%
52	doc.rero.ch Internet	<1%
53	epdf.pub Internet	<1%
54	"Proceedings of the International Conference on Nano-electronics, Circ... Crossref	<1%
55	CSU, San Jose State University on 2006-12-02 Submitted works	<1%
56	Kwan Wai Li, Ka Nang Leung. "A low-power MICS fractional-N frequenc... Crossref	<1%

57	Thejusraj. H, Prithivi Raj, J Selvakumar, S Praveen Kumar. "Design of H... Crossref	<1%
58	www3.ntu.edu.sg Internet	<1%
59	CSU, San Jose State University on 2013-12-12 Submitted works	<1%
60	Cardiff University on 2011-04-07 Submitted works	<1%
61	Design of Higher-Performance CMOS Voltage-Controlled Oscillators, 2... Crossref	<1%
62	Staffordshire University on 2010-07-21 Submitted works	<1%
63	UM, Twin Cities on 2006-02-22 Submitted works	<1%
64	CSU, San Jose State University on 2009-12-12 Submitted works	<1%
65	De La Salle University - Manila on 2014-08-12 Submitted works	<1%
66	University of Southampton on 2009-10-15 Submitted works	<1%
67	"Modeling and Simulation for RF System Design", Springer Science and... Crossref	<1%
68	Baker, R. Jacob. "Digital Phase-Locked Loops", CMOS, 2011. Crossref	<1%

69	Blackpool and The Fylde College, Lancashire on 2016-10-31 Submitted works	<1%
70	CSU, San Jose State University on 2011-12-09 Submitted works	<1%
71	Jouko Heikkinen, Jouni Gustafsson, Markku Kivikoski, Esko Liukkonen,... Crossref	<1%
72	Jung, Melanie, Georg Fischer, Robert Weigel, and Thomas Ussmueller. ... Crossref	<1%
73	Moorthi, S., D. Meganathan, M. Shankar, R. Sridhar, and J. Raja paul pe... Crossref	<1%
74	Seong-Jun Song, Sung Min Park, Hoi-Jun Yoo. "A 4-gb/s CMOS clock ... Crossref	<1%
75	University of Birmingham on 2018-04-03 Submitted works	<1%
76	University of Liverpool on 2015-05-14 Submitted works	<1%
77	University of Southampton on 2011-09-26 Submitted works	<1%
78	University of Sydney on 2018-06-10 Submitted works	<1%
79	helix.dnares.in Internet	<1%
80	tel.archives-ouvertes.fr Internet	<1%

81	lhu.edu.tw Internet	<1%
82	Associatie K.U.Leuven on 2017-06-12 Submitted works	<1%
83	CSU, San Jose State University on 2008-11-10 Submitted works	<1%
84	Furness College on 2017-03-22 Submitted works	<1%
85	M. Afghahi. "A robust single phase clocking for low power, high-speed ... Crossref	<1%
86	N V Butyrlagin, N I Chernov, N N Prokopenko, V Ya Yugai. "Current Thre... Crossref	<1%
87	Nereo Markulic, Kuba Raczkowski, Jan Craninckx, Piet Wambacq. "Digi... Crossref	<1%
88	Sung-Dae Lee. "A high speed and low power phase-frequency detector ... Crossref	<1%
89	University of Birmingham on 2018-09-02 Submitted works	<1%
90	University of Edinburgh on 2016-04-18 Submitted works	<1%
91	University of Northampton on 2021-05-09 Submitted works	<1%
92	University of Nottingham on 2010-04-10 Submitted works	<1%

93	University of Strathclyde on 2014-08-22 Submitted works	<1%
94	Yue-Fang Kuo, Ro-Min Weng, Chun-Yu Liu. "A 5.4-GHz Low-Power Swal... Crossref	<1%
95	Zhongtao Fu, Alyssa Apsel. "A tool for power and phase noise optimiza... Crossref	<1%
96	ijeat.org Internet	<1%
97	zackrauen.com Internet	<1%
98	B. C. Sarkar, M. K. Mandal. "A ring oscillator based frequency synthesi... Crossref	<1%
99	Christian Kauth, Marc Pastre, Maher Kayal. "A self-regulating oscillator... Crossref	<1%
100	Malaviya National Institute of Technology on 2012-06-18 Submitted works	<1%
101	Sabanci Universitesi on 2009-05-15 Submitted works	<1%
102	University of Pretoria on 2017-05-05 Submitted works	<1%
103	"IEEE-ICDCS conference proceeding", 2012 International Conference o... Crossref	<1%
104	Adnan Gundel, William N. Carr. "Ultra Low Power CMOS PLL Clock Synt... Crossref	<1%

105	Birla Institute of Technology and Science Pilani on 2018-04-30 Submitted works	<1%
106	Cyro Scarano Hemsi. "Digital signal processing techniques for the com... Crossref posted content	<1%
107	Universiti Putra Malaysia on 2016-05-12 Submitted works	<1%
108	University of Leeds on 2015-03-13 Submitted works	<1%
109	VIT University on 2009-07-19 Submitted works	<1%