DESIGN AND IMPLEMENTATION OF OPTIMISED MAGNITUDE COMPARATOR USING DIFFERENT LOGIC STYLES

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IN

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Submitted by

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I, Rakesh Kumar Ray, Roll No. 2K20/VLS/15, student of M.Tech (VLSI Design & Embedded System), hereby declare that the Project Dissertation titled **"DESIGN AND IMPLEMENTATION OF OPTIMISED MAGNITUDE COMPARATOR USING DIFFERENT LOGIC STYLES"** which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not derived from any source without appropriate citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate-ship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled **"DESIGN AND IMPLEMENTATION OF OPTIMISED MAGNITUDE COMPARATOR USING DIFFERENT LOGIC STYLES"** which is submitted by Rakesh Kumar Ray, Roll No. 2K20/VLS/15 Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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I extend my sincere thanks to all my friends who have been patiently helped me directly or indirectly in accomplishing this project successfully.

Place: Delhi RAKESH KUMAR RAY

Date:

ABSTRACT

With the semiconductor industry scaling down to the nanoscale regime, the three factors come hand in hand that are namely the speed, power and the area. These three factors are inter-relatable and furthermore the power is classified as power consumed and the power dissipated. As we reduce the size of the Integrated Circuits (ICs), the power consumed by the circuit should also be reduced, and at the same time some effects become prominent at the nanoscale and therefore need to be considered. At the nanoscale, as these effects became prominent, this led to the modification in the structure of the devices to be used for the low power applications.

Moore's law has been the backbone of the VLSI industry which says that the transistors on the chip doubles every eighteen months and this has been followed up till now. The designing of the devices and the circuits on the EDA tools provided by the industry reduces the cost of manufacturing by a large scale as the fabrication of the devices is costly process.

In the advanced technology low power, speed and size play a significant role specifically in the field of magnitude VLSI circuits. 2-Bit magnitude comparator design using different logic style is proposed in the brief. Comparison is the most basic arithmetic operation that determines if one number is greater than, equal to or less than the other number. The main objective of this project is to design and implement of magnitude comparator using different logic techniques and compared in terms of power

consumption, propagation delay and transistor count in cadence virtuoso 90nm technology file.

Keywords and Phrases- Propagation delay, magnitude comparator

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LIST OF ABBREVIATION

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IC	Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
MC	Magnitude Comparator
DIBL	Drain Induced Barrier Lowering
VLSI	Very Large Scale Integration
FET	Field Effect Transistor
ALB	A less than B
AGB	A Greater than B
AEB	A equal to B

CHAPTER 1.
INTRODUCTION

1.1 OVERVIEW

We are living in the era of artificial intelligence where everything which we can imagine is in our hands with the help and emergence of the ongoing technology. comfortable with the growing pace of the world of technology. With the increase demand of the technologies and the evolution of the products, the big giants of semiconductor industries like Qualcomm, Intel, NXP Semiconductors and Mentor graphics are finding their way in a best appropriate manner to design the product which is user friendly. There is a need for the semiconductor industries, as well, to make themselves.

Over the era of two decades, the CMOS technology has revolutionized the semiconductor industry whether we talk about the Analog Integrated Circuits or the Digital Integrated Circuits and the EDA tools have reduced the cost of manufacturing by a huge amount. The silicon and the compound semiconductors including III-V compounds still finds the niche applications [1]. The fabrication cost of the circuits is the major part including the minute steps of lithography and others similar steps in the fabrication. The CMOS technology still serves as the basic technology to design electronic circuits and will continue as it is. For the property of controlled conduction the semiconductors have been explored and this has led to the various experiments performed including the material engineering which performs the experiments on the different material that can be used to improve the conducting properties of the device. The effects at different-different scale are the reason to find a novel device which can

carry the legacy of CMOS technology further. Finding the good properties (electrical) of the device with the reducing channel length is the first objective of the research in the VLSI Industry .

The electrical properties include the ON current of, OFF current, subthreshold swing of the device and mitigating the effects that come into the picture while we minimize the channel length. The effects such as the hot electron effect, second order effects and the fringing effects from the electric field at gate. The whole story of the VLSI industry revolves around the three parameters speed, power, and area of the chip or the Integrated circuit designed [9]. Reducing power or low power techniques are being implemented at different level that could be at device level, circuit level or a system level.

In present scenario, the important concern for most of VLSI engineer for DIGITAL logic circuits is to optimization like power optimization, timing constraint optimization etc. and also the logic optimization are also concern from Boolean expressions. Magnitude Comparator is one of the design which is used in digital design to compare two number and decide whether the number will be greater, lesser or equal to other number.

There are various constraints which are implemented, which are imposed by these industries like functionality of the electronic device, power dissipation by the product, area occupied and also the reliability of the product. All these constraints, require some special attention and the measurements, which needs to be fulfilled by the design engineers, so that the reputation of the industry, and the competition in the products will be sustained [2]

It is a circuit which is used for comparison of two numbers and determines magnitudes (Fig.1). Magnitude comparator has two input as a number like 2-BIT, 4-BIT etc and their result is three like greater than, equal to or less than which are specified .[4] [5]

The different style which is used in gates basically affects the different parameters like propagation delay, number of transistors on chip, power dissipation, and complexity of a circuit in terms of layout design. The chip sizing depends on the number of transisors used in designing and their sizes and on the circuit and complexity in terms of layout design. All these above described features may changes from one logic style to another logic style and it depends on the designer what are the important parameters for it like propagation delay, number of transistors, power consumption or circuit performance. In order to distinguish all different logic style, simulations are carried out for comparison among different parameters like propagation delay, number of transistors, power consumption in circuits at supply voltages 1.0 v. Simulations are carried out in cadence virtuoso at 90nm technology. [2][5]

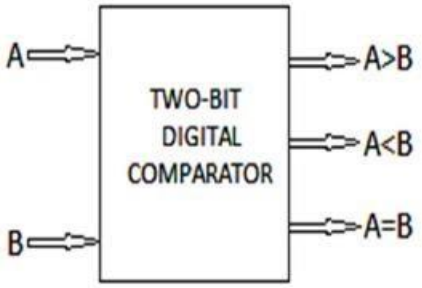

Fig.1 2 BIT MC BLOCK DIAGRAM [4].

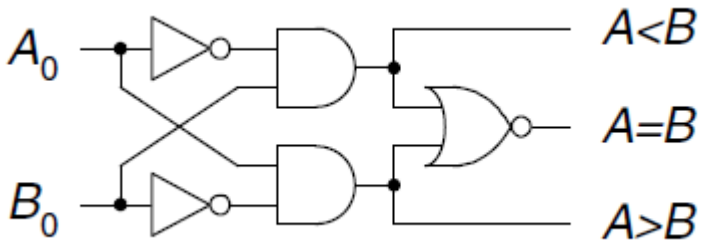

Fig2. GATE-LEVEL 1- BIT MC [7]

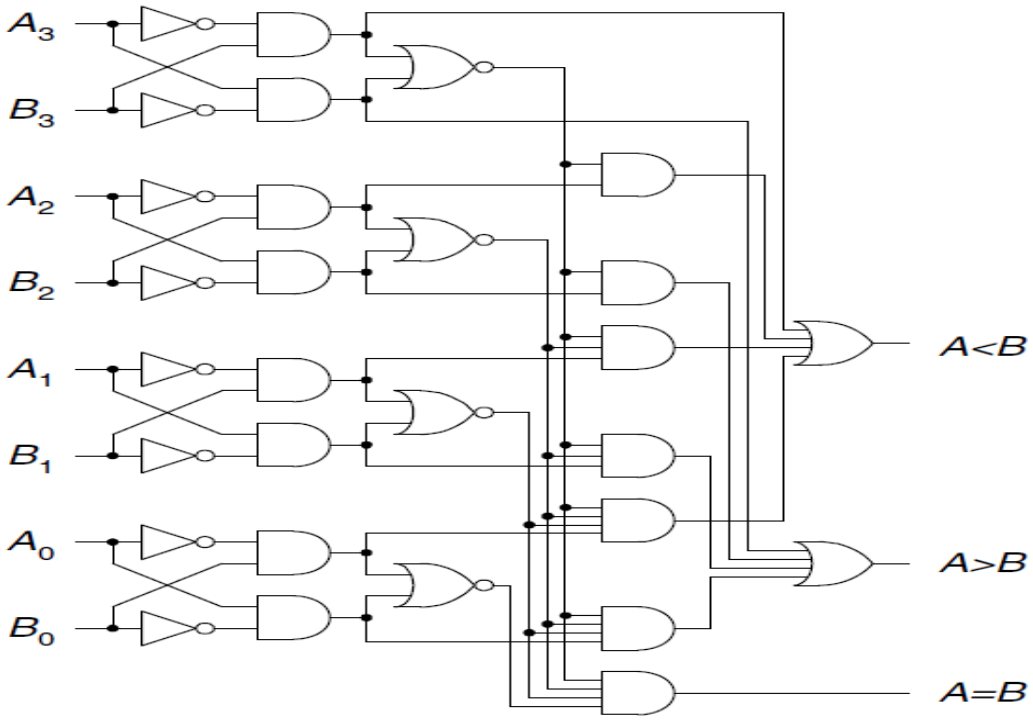

Fig 3. SCHEMATIC OF 2 BIT MC [7]

1.2 2- BIT MAGNITUDE COMPARATOR

This is a digital circuit. Digital comparator which is used for comparison of two binary value. There are two types of comparator which are namely below

(i) Identity Comparator

(ii) Magnitude Comparator.

- IDENTITY COMPARATOR: This comparator has only one output terminal for when A=B, either A=B=1 or A=B=0 .
- MAGNITUDE COMPARATOR: This type of comparator has three output terminals and depending on the magnitude of input of given two number one of these output terminal will be high like high for greater than, equal to or less than.

•

Table.1 TRUTH TABLE OF 2 BIT MC

INPUTS				OUTPUTS		
A0	A1	B0	B1	A>B	A=B	A<B
0	0	0	0	0	1	0
0	0	0	1	0	0	1
0	0	1	0	0	0	1
0	0	1	1	0	0	1
0	1	0	0	1	0	0
0	1	0	1	0	1	0
0	1	1	0	1	0	0
0	1	1	1	0	0	1
1	0	0	0	1	0	0
1	0	0	1	1	0	0
1	0	1	0	0	1	0
1	0	1	1	0	0	1
1	1	0	0	1	0	0
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1	1	1	0	1	0	0
1	1	1	1	0	1	0

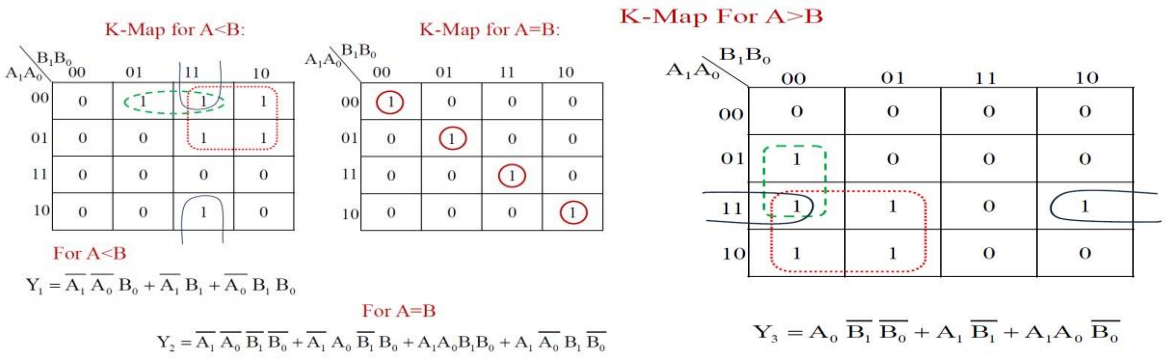


Fig 4. K-MAP OF 2-BIT MC

We have different method for realization of Boolean expression for solving expression by using K-MAP and also by using truth table. One of the best method to solve the magnitude comparator expression by using XOR- XNOR , AND and OR which I have used in designing the 2BIT magnitude comparator in proposed technique which is good as compare to other different logic style in terms transistors, power dissipate in circuits and also simple for making layout for proposed technique.

This thesis conclude that MAGNITUDE COMPARATOR FOR n- BIT for comparison of two numbers by using hierarchy method and simplified it by taking two number as input and gives output which n- bit number will be greater , less or equal to in terms of magnitude as compare to the other number which area shown below block diagram.

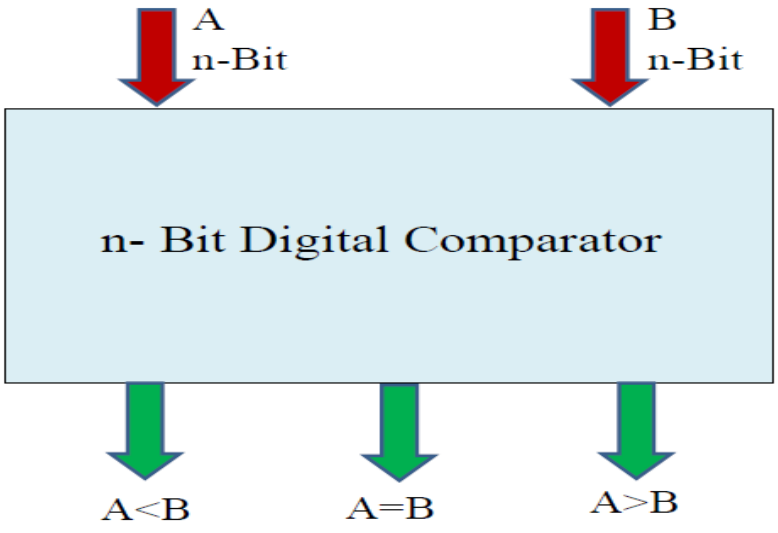


Fig 5. BLOCK DIAGRAM OF MAGNITUDE COMPARATOR [9]

1.3 TOOLS USED

This thesis work has been carried out in the cadence virtuosos and LT- Spice software for designing the schematic of different logic style using 90 nm technology file and compare them in terms of different parameters.

1.4 ORGANIZATION OF WORK

The thesis work has been described in the following ways are shown below:

Chapter 1: Describe the introduction part of this thesis and tools used in this thesis.

Chapter 2: Describes the Literature survey of done during and before carrying out the work and also the Research gap and the Objective of the work carried out.

Chapter 3: Describe the different logic style which I have implemented

Chapter 4: In this chapter all different logic style are implemented are depicted here.

Chapter 5: In this chapter I have discussed all implemented simulation of different logic style.

Chapter 6: In this chapter I have discuss conclusion which I have implemented of different logic style of 2 BIT MC in terms of different characteristics like transistors, propagation delay and power dissipated in the circuit which are perform in cadence virtuoso.

Chapter 7: This chapter talks about the work that can be done in future and the conclusion of the work that has been carried out.

CHAPTER – 02

LITERATURE SURVEY AND OBJECTIVE

2.1 LITERATURE REVIEW

The researcher has design the 2- bit magnitude comparator using static CMOS logic style techniques which has advantage part is that we get full swing and there is disadvantage part is that they required larger number of transistors that is 66 and also dissipate higher amount of power in the designing circuit so to reduce the transistors in terms of quantity and they moved to the other styles that they give same functionality but demand less transistors in terms of quantity.[1][2]

In present scenario various implementation of logic, MC has become a concern interest for magnitude comparator designs have been put into action by researchers [19-20]. Two-bit MC are implemented using pass transistor logic which required 40 CMOS transistors [3][6]. The major disadvantage with the pass transisor logic is that there is voltage degradation and N-MOS transistor passe only strong 0 and it passes weak 1 in circuit associated. Therefore the pass transistor logic has consumed higher.[10]

The researcher observed that there is problem in PTL hence they move to other logic style in order to overcome the problem of pass transistor logic and complementary [8][12]

CMOS style has been developed. This logic style is famous for the full swing at the output means there is no degradation in voltage level because of C-CMOS is made from a set of N-MOS and P-MOS transistors.[11]. Transistor count (TC) for this logic style is 66 which is very high in number. This high number of transistors on chip makes the input resistance very high which lead for high propagation delay in circuit.[16][19]

Transmission gate logic style do not show the voltage degradation like pass transistor logic style. Hence, large number of transistor count in transmission gate logic style that leads high area in silicon chip and also complexity increase in circuit designing. Two-bit MC using TGL is reported in which required 66 transisors.[18][20]

2.2 OBJECTIVE

The main purpose of this thesis is to designing and implementation of 2-BIT magnitude comparator in different logic style like using static CMOS, pass transistor logic style, transmission gate logic style and powerless techniques and compare them in terms of different parameters like power dissipated in circuit, propagation delay in circuit like rise time and fall time and number of transistors and complexity in implantation of different logic style

CHAPTER 03

DISCUSSION OF DIFFERENT LOGIC STYLE

3.1 STATIC CMOS LOGIC STYLE

The static CMOS circuit is a combinational circuit and has comination of two networks i.e. called Pull-up network (PUN) and another one called Pull-down network (PDN). This style of logic circuits known as static circuit in which for each and every point in time each gate output is either connected to Vdd (Power supply) or Vss (Ground) through a path which has low resistance. Actually Pull-up network is made up from the combination of PMOS transistors and Pull-down network is made up from combination of NMOS transistors[1]

The output of static CMOS logic style is connected to VDD when the Pull-up network is active and the output is connected to the ground when the pull- down network is active. This type of logic style we called complementary in nature because at a time either pull-up network in active or pull-down netwrk is active. The main advantage part of using this logic style is that we get full swing i.e. there is no degradation in output and the disadvantage part of using this logic style is that required large number of transistors to make a circuits or a logic that become very complex and also making layout of such circuit become complex. The power dissipation in such type of circuit is also very high because that required very large number of transistors as compared to other style. [2][4]

In static CMOS logic style there is no static power dissiption but there is power dissipation in static CMOS logic style due to toggling activities in output and there is also low leakage current in the circuit which lead dissipation of power. In this logic style and when we reduce the technology size then leakage current is also increases which leads to power dissipated as heat. As compare to other logic style the propagation delay in this type of logic style is more or higher because of larger number

of transistors in designing circuit. This type of logic style required larger number of transistors hence to making layout of such type of logic style is complex. The output of this logic style not depend on the ratio of (W/L) means this type of logic style is also called ratio less circuit. Actually we prefer most of the design for making the circuit from static CMOS logic style. As we conclude that static CMOS are preferred from most of the logic style because of low static power, Robust and most important it is supported by most synthesis and back-end tools. Therefore, we use this logic style when we required full swing and there is no problem of large transistors so we move to another type of logic style according to requirement and complexity.[4]

3.2 TRANSMISSION GATE LOGIC STYLE

Actually transmission logic style has been used for also a bidirectional switch with input and output connected via a path which has low resistance. Transmission logic style consists of N-MOS transistors and P-MOS transistors which share common point connections from source and drain and gate connection of respective transistors with complemented signals. Transmission logic style also requires transistors which is high in number and higher area as compared to other logic like pass transistors. The transmission gate logic style is famous for the stylre to have higher speed and low dissipation of power . The resistance of single N-MOS and P-MOS transistors are higher when they are used or connected in parallel then overall resistance of transmission gate becomes lower and hence there is lower power dissipation in designing the circuit from using transmission gate logic style. In this style, we get the full swing and there is no degradation in voltage level at the output. The designing of circuit using transmission style requires higher area in silicon chip as compared to PTL style. The total 66 nmber of trasistors are required for designing the two but MC. [5]

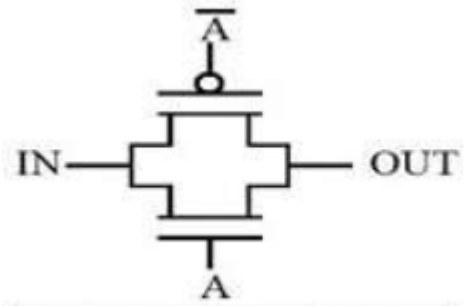


Fig.6 SCHEMATIC OF TGL

Here is the symbol is depicted of transmission gate logic style. When the signal is high the N-MOS transistor and P-MOS transistor both are ON through a low resistance path because when two wire are connected in parallel then equivalent resistance becomes lower and we get full swing or there is no degradation at output signal because through N-MOS transistor we get low value and through P-MOS transistors we get the exact Vdd without any degradation in output i.e. . the beauty of using transmission gate logic . When we using this style the overall resistance will decrease and that lead to less power dissipation in circuit as compared to other logic style in design.

3.3 PASS TRANSISTOR LOGIC STYLE

In modern VLSI, We more focused on the less propagation delay, lesser area and also lesser number of transistors requires for designing the circuit hence the pass transistor logic style is more fit where we comprise the delay but we not able to make comprise from area. Another advantage part of this logic style is that either N-MOS transistor or P-MOS transistor is required for designing the circuit. The pass transistor logic style has advantage over using another logic style is that the number of transistors required for designing the circuit is lower i.e. less number of transistors. Due to less number of transistors required, the power dissipation is also lower as compared to other

Styles. In the pass transistor logic style we connect the input signal to the source terminal of –N-MOS transistor and take output from the drain terminal and gate terminal is used to connect or disconnect the source terminal and drain terminal through a low resistance path. The disadvantage part of using this logic style is that we are not getting full swing i.e. we get the degradation at the output terminal (Vdd –Vtn) and hence for removing this part of problem i.e. voltage degradation, we use voltage restorer so that we get full level of volatge at the output. The another things is that output of one transistor should not drive the gate of another transistor so this is not allowed in such logic style because we get higher or more voltage degradation in the signal at the output terminal. There is no static power dissipation is observed in pass transistor logic style. It is also a ratio less circuit means output doesn't depend on the size of transistors. The minimum voltage i.e. Vtn is required to make pass transistor ON that allow to connect the source terminal and drain terminal via a low resistance path. The another advantage of using this logic style is that delay of the circuit is lower and making of the layout of this style is less complex as compared to other logic style because of transistors which is minimum in quantity is required and also area required is less that have great advantage part. [6][7]

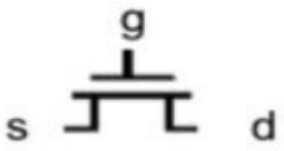
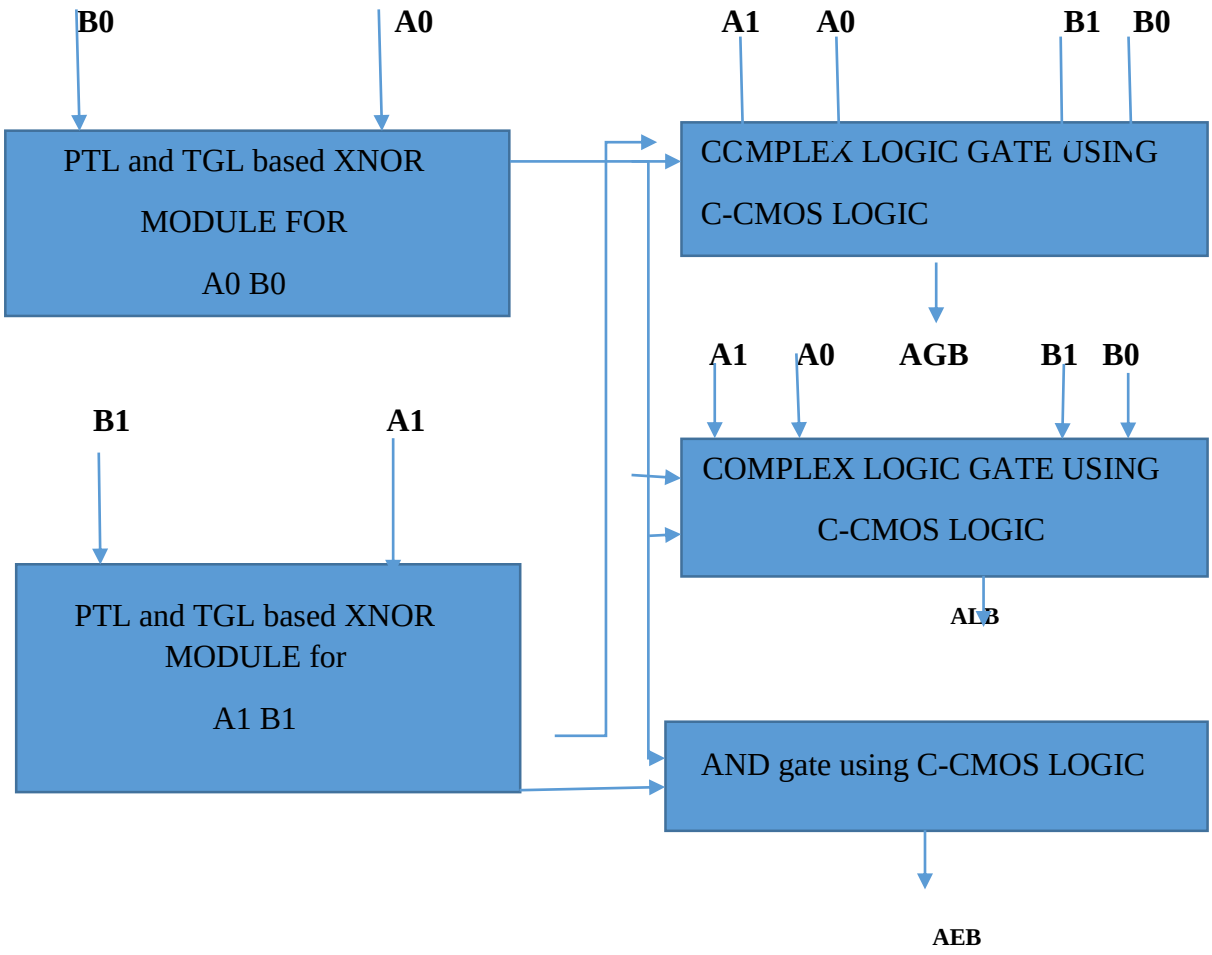


Fig 7 SCHEMATIC OF PTL [6]

In Pass transistor style, it has three terminal named as GATE, SOURCE and DRAIN terminal. At the source terminal we provide input and take output from the drain terminal and this source and drain terminal are connected via low resistance path when the signal at the gate terminal is high. In the pass transistor logic style we get strong 0 because N-MOS transistor allow and pass strong 0 but at the output terminal we get weak 1 because

that signal pass through N-MOS transistor and N-MOS transistor passes the signal at drain terminal with degradation which is equal to the threshold voltage drop. Similarly if we make PTL using P-MOS transistors then we get weak 0 and strong 1and that is disadvantage part of using the pass transistor logic for designing the circuit so we move to the transmission gate logic style which are parallel combination of both N-MOS and P-MOS transistors and in this logic style we get both strong o through N-MOS transistors and strong 1 through P-MOS transistors but that required larger number of transistors.

3.4 POWERLESS TECHNIQUE



Fig, 8 BLOCKED DIAGRAM OF POWERLESS TECHNGIQUE MC[1]

Basic building the gate for designing the magnitude comparator is using XNOR gate which is efficient in consuming less power as compare to other logic gate with better switching activities and also required less number of transistor.

There are various techniques for designing the magnitude comparator and the basic one is to compare the two signal and note down the its truth table and finally got their Boolean expression and compute the output accordingly.

Power consumption in this technique is less as compare to other logic style because in this technique less number of transistor are required for designing the magnitude comparator. The propagation delay in this logic is also minimum as compare to other logic style and also observed that making of layout for such technique is little bit less complex as compare to other styles. The power delay product for such techniques is minimum or smaller as to other techniques discussed above like static CMOS, PTL style and TGL [9]

As this thesis conclude that designing magnitude comparator is depends on the customer that what they want that like less propagation delay, less number of transistors or lesser power dissipation in circuit.

CHAPTER 04

DIFFERENT PARAMETERS

4.1 POWER DISSIPATION IN CIRCUITS

In VLSI circuits, we have different type of dissipated powere in circuits occurs like short-circuit dissipated power , power dissipated due to small leakage current, power dissipation due to toggling activities i.e. dynamic power dissipation etc and so many type of power dissipation in circuit.

In short circuit , when there is connection between the power supply and ground and the power dissipate due to this path we called it short circuit power dissipation[15], generally this type of power dissipation occurs in static CMOS logic style. The dissipated power occurs in VLSI circuits due to switching activities of logic or charging and discharging of capacitors, we called it such type of power dissipation in circuits called dynamic power dissipation and hence we try to shut down or stop extra toggling in circuits so dynamic power dissipation in circuit will decrease. When we decrease the channel length of transistors the power dissipation in circuits due to leakage current is increases that is the disadvantage part of the using lower technology node so to minimize the leakage power dissipation in circuits, we have to increase the supply voltages.

Another type of dissipated power in circuits is static power dissipation, this type of power dissipation occurs when the circuit in static mode or in off mode means power dissipated due to leakage current in this circuit.[11][16]

We have different techniques for reduction of power dissipation in circuits like clock gating, use ratioed circuits, pin assignment, pin swapping in the circuit, the input or signal which has more switching activities placed far from the output pin so we get lesser switching activities.

4.2 PROPAGATION DELAY IN CIRCUITS

The propagation delay in circuits depends on many parameters like capacitance value, length and width of transistors, Trans conductance (Kn) parameters and also depend on supply voltage of circuits. The relation between propagation delays on power supply is inversely proportional and directly proportional to the capacitance value and also the ration of width and length of transistors.[16][19]

The average value of rise & fall time in circuits defined as the delay in circuits. The rise time which is called as the time taken by the voltage signal to reach the 50% of input and 50% of output is defined as the rise time in circuits similarly the time taken to by the signal to down the 50% of its value is defined as the fall time in circuits. The average of both the rise and fall time is called the propagation delay in circuits. Propagation delay of circuits are also depend on the number of transistors, more number of transistors in circuit leads maximum delay in circuits so we optimized the logic so minimum number of transistors are required hence the propagation delay in circuits become minimum.[20]

CHAPTER 5

CIRCUIT DIAGRAM OF 2 BIT MC USING DIFFERENT LOGIC STYLE

5.1 STATIC CMOS LOGIC STYLE

The static CMOS style is realized by connecting the source of pull up device with power supply and by connecting the source to Vss of pull down device and taking the output from drain of pull down .[7]. It is ratio less circuit and give strong "high logic level and low logic level and there is no static dissipated power in circuits" but realization of Boolean functions using this logic style require large area because of large number of transistors.

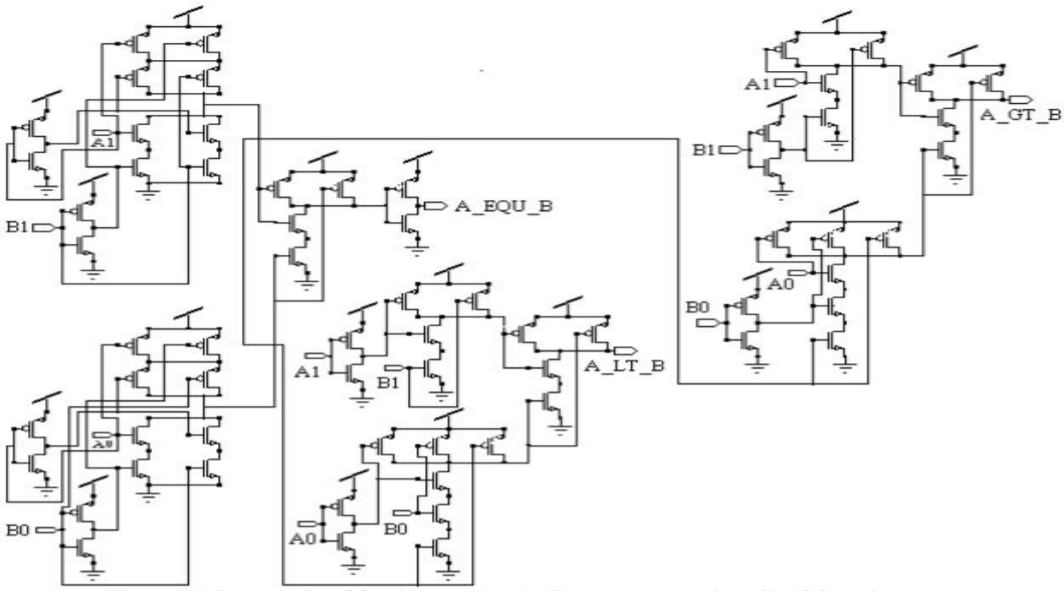


Fig.9 2- BIT MC USING STATIC CMOS LOGIC TECHNIQUE [4]

5.2 MC USING PASS TRANSISTOR LOGIC

Pass transistor logic style is also a ratio less circuit means output does not depend on the ratio of width and length of transistors. Lower interconnection effects and small area due to minimum transistors in terms of quantity and less power dissipation because no static dissipated power in circuits. But there is multi threshold voltage drop and higher delay in long chain of pass transistors and also there is sneak path in pass transistor logic style. [7][8]

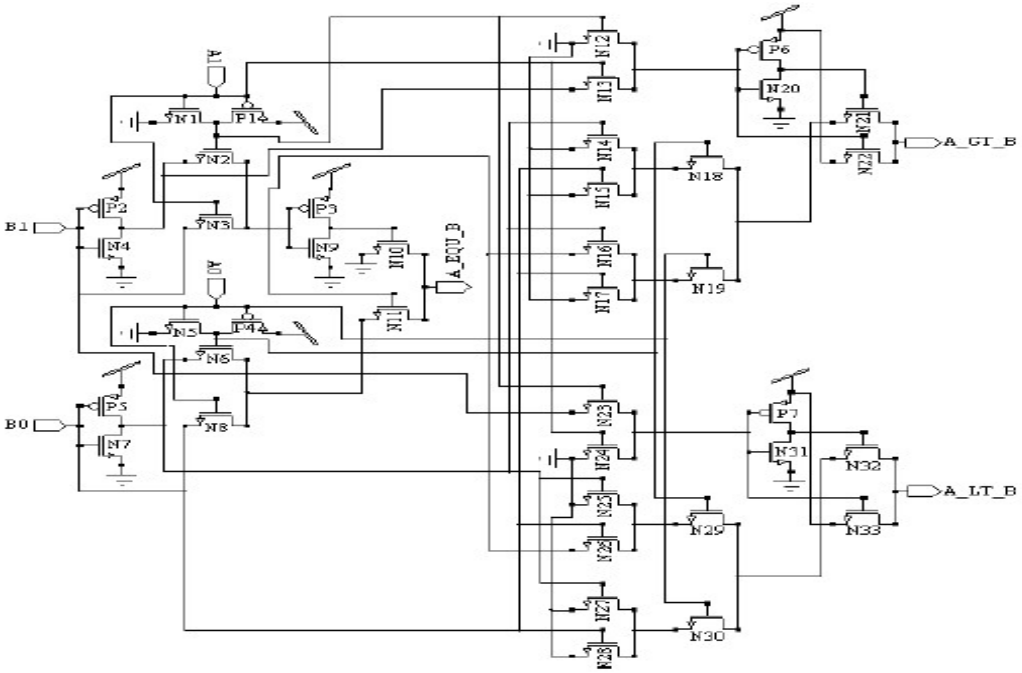


Fig.10 2 BIT MC USING PASS TTRANSISTOR LOGIC [1]

5.3 MC USING TGL STYLE

TGL style can be analyzed by connecting a NMOS transistor and a PMOS transistor in parallel and provide complementary input voltage to the gates. It offers low resistance path when both transistors are ON and provides high resistance

path when transistors are off. The total equivalent resistance of the TG remains constant and it act as a bidirectional switch. It provides strong high logic level and low logic level. But realization of Boolean functions using transmission gate require large area because of large number of transistors. [3][7]

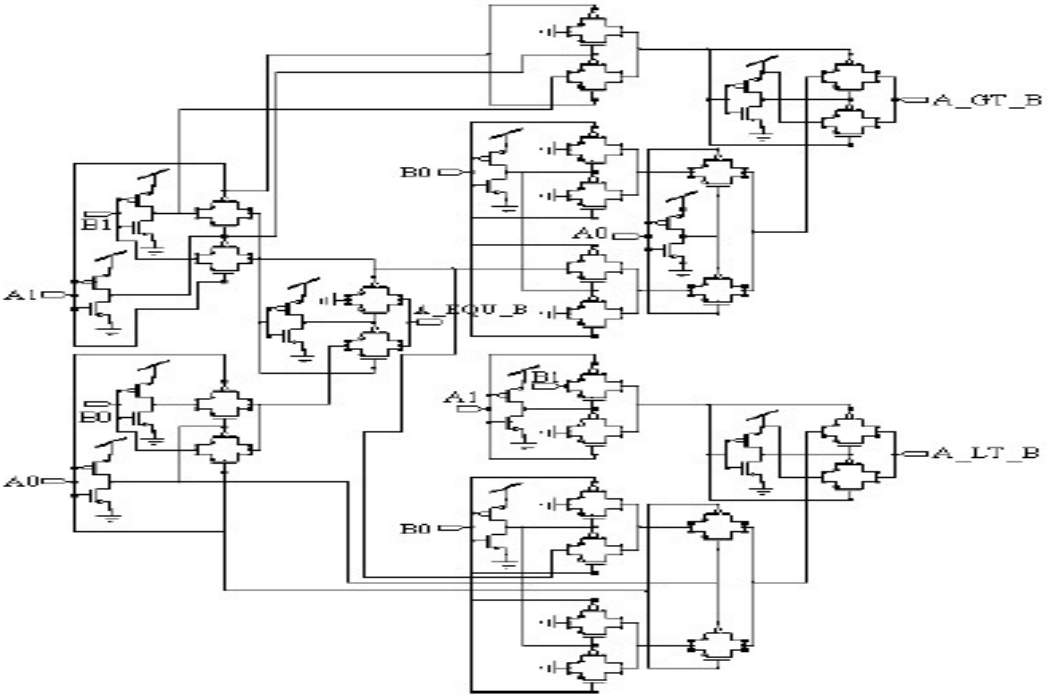


Fig.11 2 BIT MC USING TRANSMISION GATE LOGIC [4]

5.4 MC USING POWERLESS TECHNIQUES

The proposed techniques it requires less number of transistor (46) for magnitude comparator implementation and less power consumption in this techniques. [4]

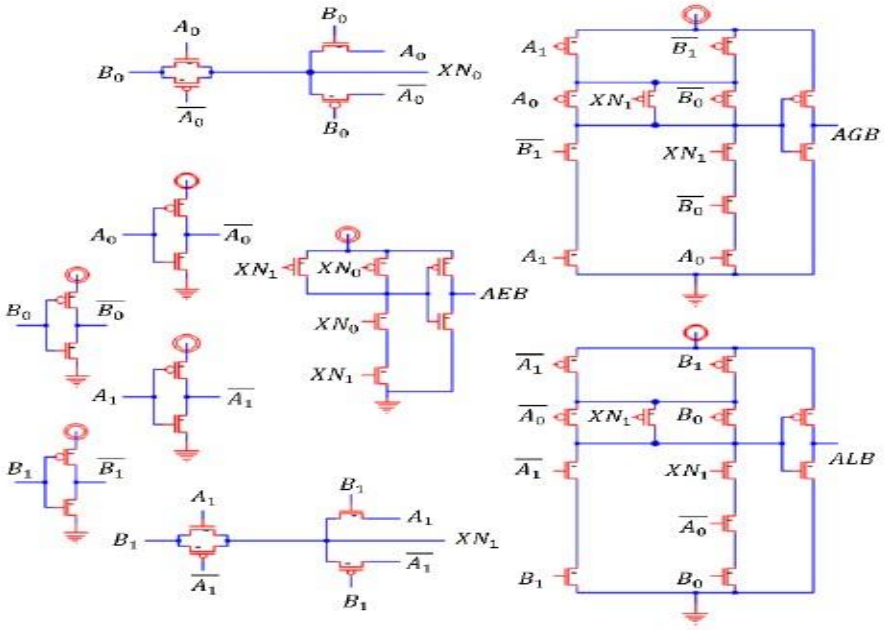


Fig.12 2 BIT MC USING POWERLESS TECHNIQUE [1] [2]

CHAPTER 06

SIMULATION AND RESULT

6.1 PARAMETERS OF SIMULATION

- All simulation has performed in Cadence virtuoso platform and used (gpdk090) 90nm technology node for plotting the waveform for different logic style and also for the calculation of power consumption, propagation delay, rise time, fall time.
- The ratio of width and length of PMOS and NMOS are taken as: (W/L) p = 2.4 (W/L) n = 1.2
- The value of capacitance is c: = 100f F.
- The supply voltage used is 1v.
- Time period for 4 different input as follow as are: A0: 10ns A1: 20ns B0: 40ns B1: 80ns.

6.2 RESULT

6.2.1 MC USING STATIC CMOS LOGIC STYLE

In this thesis, I have implemented 2-BIT MC using various style, here the MC is depicted using static CMOS logic style and simulation performed in cadence virtuoso platform that total 66 number of transistor are required to make this logic style i.e. takes lot of area on chip and compare the different parameters like propagation delay, number of transistor, area and power dissipation. The all parameters which are used in simulation are mentioned above like capacitance, width and length of transistors. All simulation of this logic style and their result are depicted in fig 6 ,7, 8

.

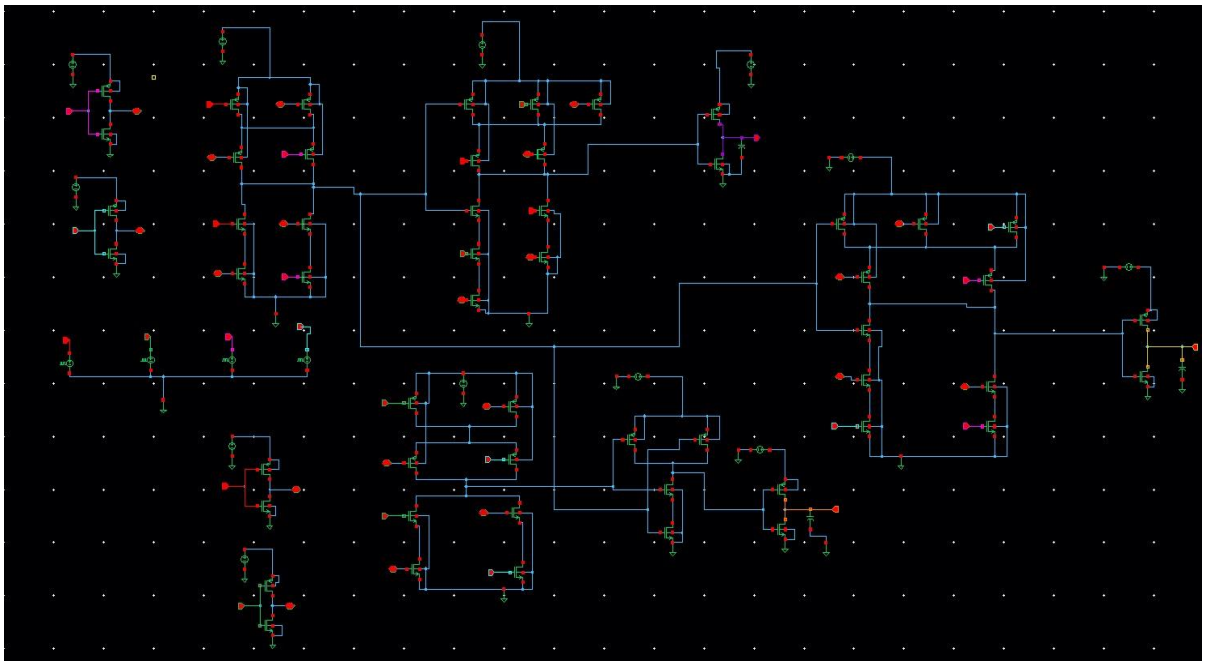


Fig.13 MC USING STATIC CMOS LOGIC

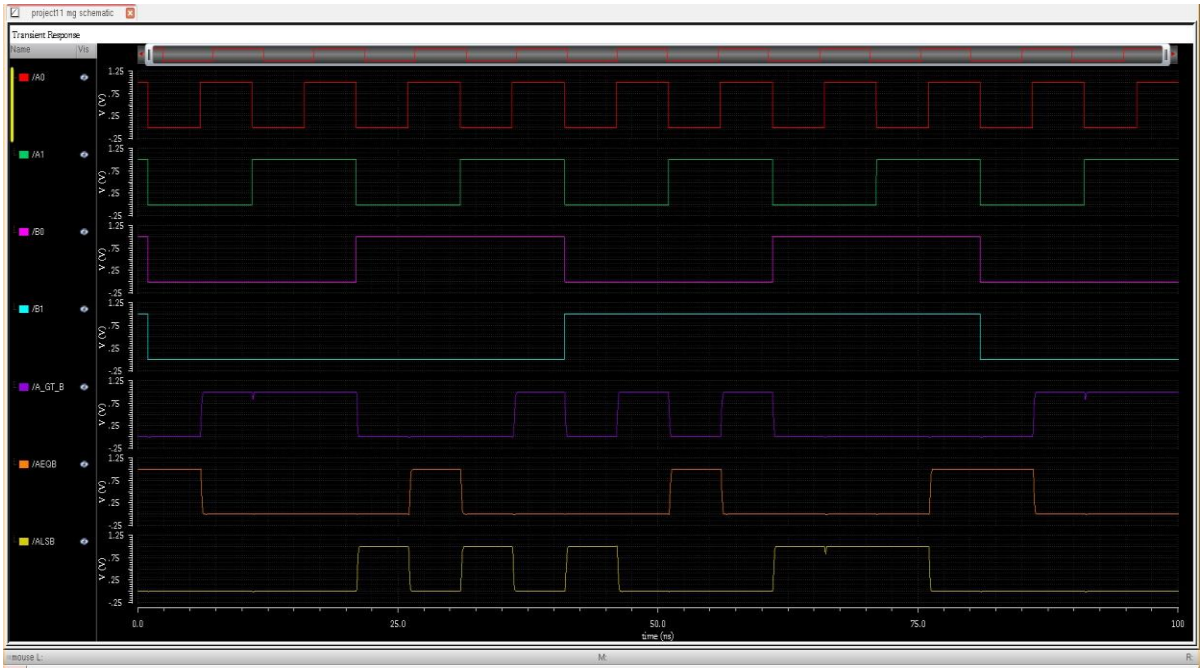


Fig.14 WAVEFORM OF MC USING STATIC CMOS LOGIC

6.2.2 MC USING POWERLESS TECHNIQUES

The logic implementation using this techniques required less number of transistors i.e. 46 number of transistors which is less in umber as compare to static CMOS logic style and also less area is required on chip for designing the circuit and also less power dissipation. Below page I have discussed all parameters like power dissipation, number of transistors and propagation delay in table. All simulation and results are depicted in below given fig 8, 9.

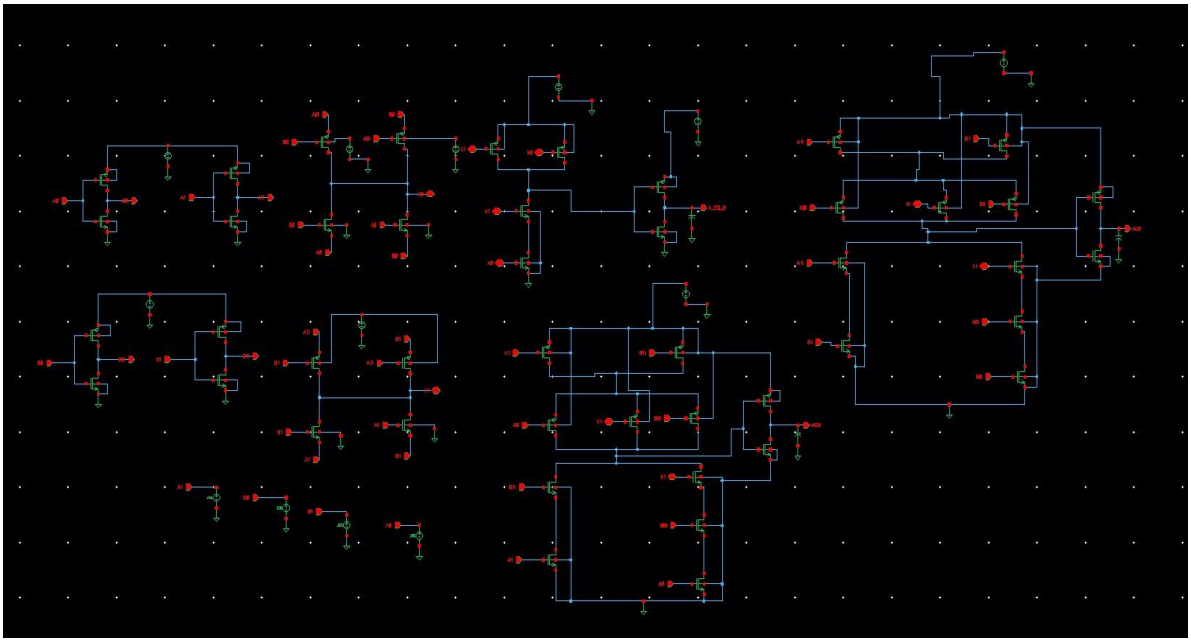


Fig.145SCHEMATIC OF MC USING PROPOOSED TECHNIQUES

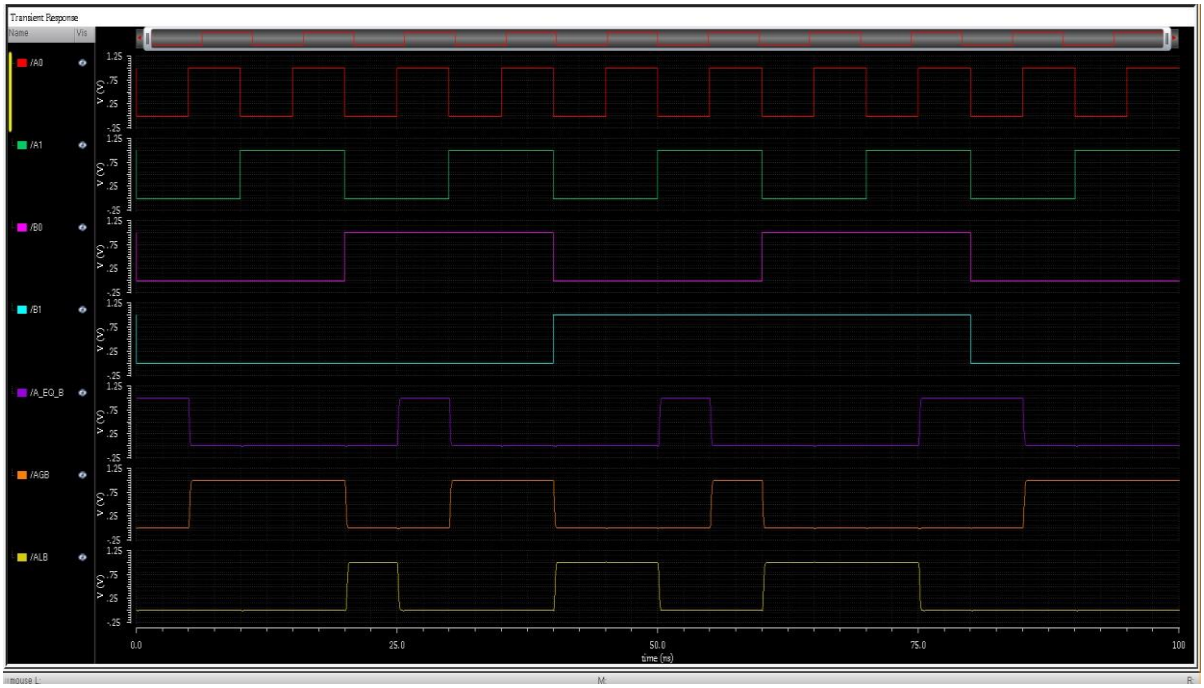


Fig.15 WAVEFROM OF MC USING PROPOSED TECNQIUES

6.2.3 MC USING TRANSMISSION GATE LOGIC STYLE

The designing of the magnitude comparator using TGL style requires 66 transistors in terms of quantity as equal to the static CMOS style but more than powerless techniques but power dissipation in this techniques is less. In this techniques we get full level at the output and there is no degradation in output signal. All simulation which are performed in cadence virtuoso platform and their result are depicted in fig 10, 11and their comparison results are depicted in table 1.

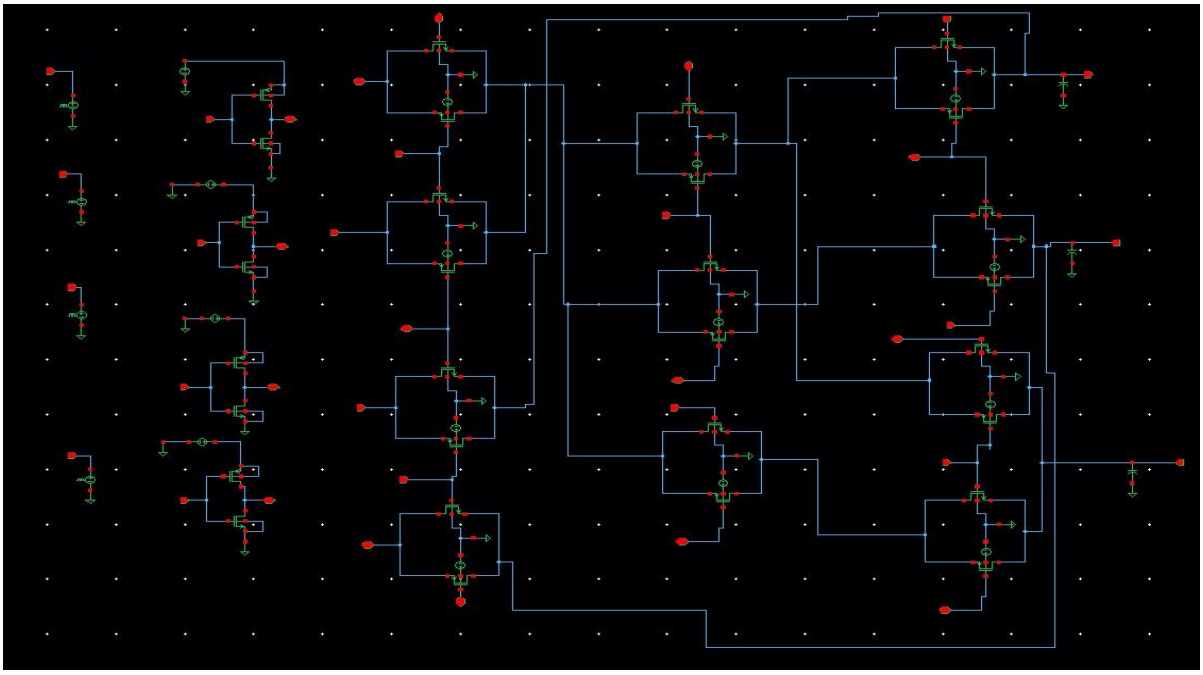


Fig.16 SCHEMATIC OF MC USING TGL

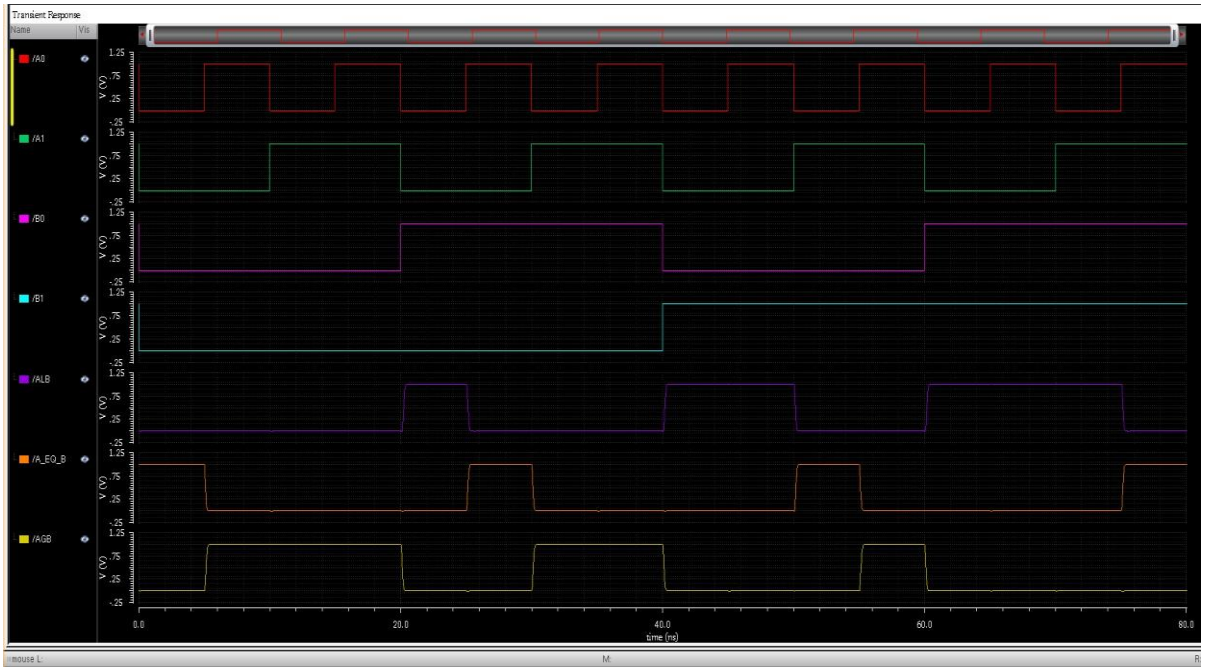


Fig.17 WAVEFORM OF MC USING TGL

6.2.4 MC USING PASS TRANSISTOR LOGIC STYLE

In this style i.e. PTL style the smaller number of transistor are required is less that is equal 40 which is least number of transistor as compare to other style and less area required for designing.

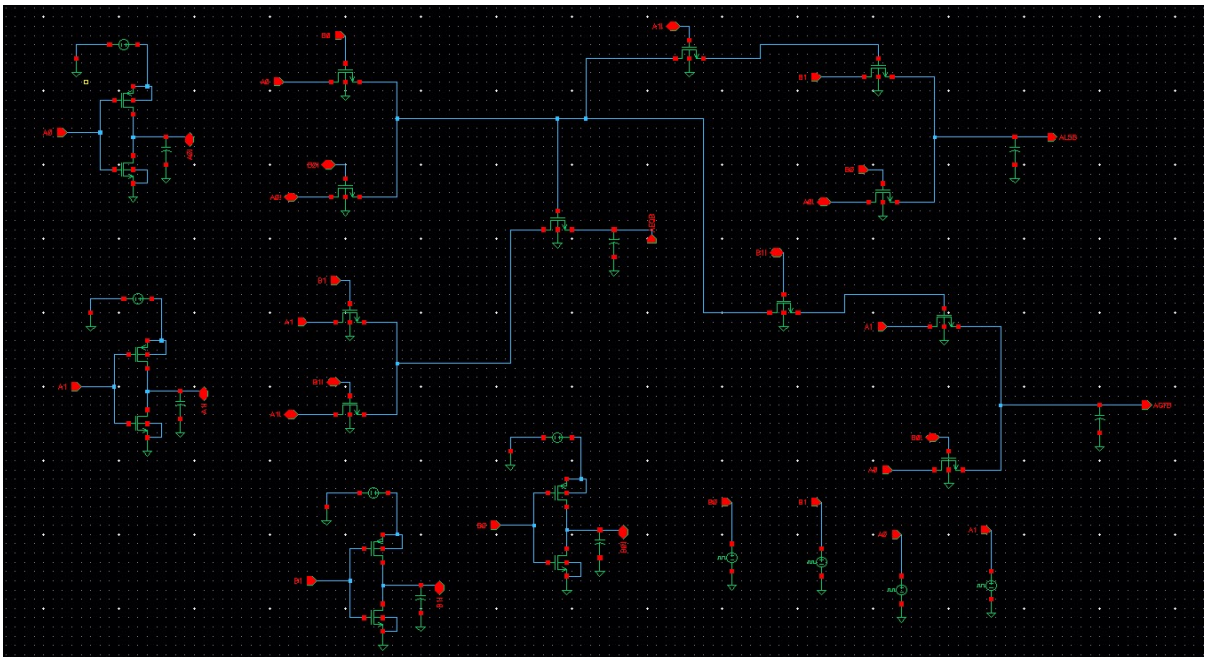


Fig.18 SCHEMATIC OF MC USING PASS TRANSISTOR LOGIC

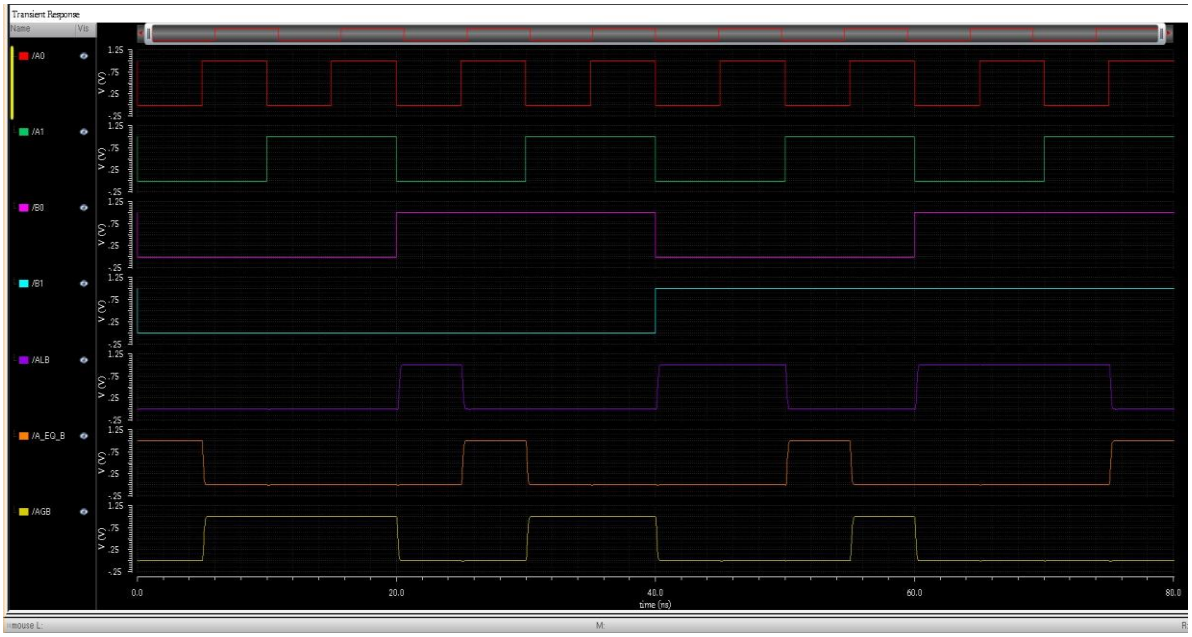


Fig.19 WAVEFORM OF MC USING PASS TRANSISTOR LOGIC

CHAPTER 07

OBSERVATION TABLE

7.1 TABLE

Table 7.1 COMPARSION TABLE AMONG DIFFERENT PARMETERS OF DIFFERENT LOGIC STYLE

	PROPOSED MAGNITUDE COMPARATOR (POWERLESS)				MAGNITUDE COMPARATOR USING CMOS LOGIC			
PROPAGATION DELAY	5.11ns 5.14ns 18.14ns				5.11ns 5.15ns 20.24ns			
		AEQB	AGB	ALSB		AEQB	AGB	ALSB
	RISE TIME	0.126ns	0.132ns	0.124ns	RISE TIME	0.127ns	0.144ns	0.139ns
	FALL TIME	0.129ns	0.127ns	0.145ns	FALL TIME	0.128ns	0.148ns	0.137ns
POWER COMSUMPTION	43.27uW				52.57Uw			
TRANSISTOR COUNT	46				66			

Table 7.2 COMPARSION TABLE AMONG DIFFERENT PARMETERS OF DIFFERENT LOGIC STYLE.

	MAGNITUDE COMPARATOR USING TRANSMISSION GATE LOGIC				MAGNITUDE COMPARATOR USING PASS TRANISTOR LOGIC			
PROPAGATION DELAY	5.12ns 5.10ns 16.04ns				4.98ns 5.05ns 15.80ns			
		AEQB	AGB	ALSB		AEQB	AGB	ALSB
	RISE TIME	0.128ns	0.131ns	0.134ns	RISE TIME	0.124ns	0.126ns	0.131ns
	FALL TIME	0.126ns	0.130ns	0.132ns	FALL TIME	0.124ns	0.125ns	0.134ns
POWER CONSUMPTION	48.32uW				45.69uW			
TRANSISTOR COUNT	66				40			

7.2 OBSERVATION

From the observation table that proposed technique consume less power consumption (43.27uW) and less propagation delay but large number of transistors (46). Through PTL implementation, it requires transistor which is minimum (40) but there is degradation in logic level to remove it then i moved to other logic implementation using transmission gate, it produces full swing but requires large number of transistor (66).

The static CMOS logic style gives full swing but it required maximum number of transistors so we move to the pass transistors logic style which required 44 i.e. number of transistors but here we voltage degradation in logic hence the powerless technique required only 44 number of transistors also there is no degradation in voltage logic.

The dissipated power in static CMOS logic style is higher among all the discussed techniques then we moved to other techniques TGL style. The least power consumption in the powerless techniques as compare to all other simulated techniques. The propagation delay of circuits depends on the various factor like parasitic capacitance, width and length of transistors. The maximum propagation delay is in static CMOS logic style because maximum parasitic capacitance in this logic style because of maximum transistors are needed in terms of quantity to make this logic style.

CHAPTER 08

CONLCUSION AND COMPARSION

8.1 CONCLUSION AND COMPARSION

- After simulation of all four different logic styles in cadence virtuoso tools final results are concluded for Power Consumption, Propagation delay and transistors in terms of quantity on silicon chip.
- The 2-bit MC is designed which is used for analyses of magnitude of two number that is which number will be the less than, equal to or greater than the third number.
- This 2-bit MC which is designed by the method of PTL provides better performance by reducing transistor in terms of quantity and also minimize the power consumption in circuit also maintain the low complexity of the circuit but it doesn't provide full swing.
- The voltage swing is far better than in CMOS style logic design & Transmission Gate design but transistor in terms of big number and more dissipated power in circuit.
- In the proposed technique, minimum number of transistor and less power dissipation in circuit so this techniques provides low power design as compared to other logic style and also less complexity in circuit in terms of layout design.

We choose the design logic that what are the requirement like less power consumption, less area or adjust with the number of transistors. I observed that there are trade-off among the number of transistors, power consumption, propagation delay of circuit, rise tand fall time. So according to the needs or requirement we choose the logic or style and proceed further have different type of methodologies and style for which we design the circuit or logic like we also design the magnitude comparator using half adder, full adder, and GDI techniques etc. to make the logic more easily designable, which dissipate less power and also consume less area on chip hence according to the need of customer/ researcher .

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