M. Tech (Signal Processing and Digital Design)

PRANJALI AGRAWAL

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Design Of Low Power TIQ Flash ADC Using Tanner Tool

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IN

SIGNAL PROCESSING AND DIGITAL DESIGN

Submitted by:

Pranjali Agrawal

2K20/SPD/09

Under the supervision of

Mr. Rajesh Birok (Associate Professor)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

MAY, 2022

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

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I, **Pranjali Agrawal, Roll No. 2K20/SPD/09** student of M.Tech. (Signal Processing and Digital Design), hereby declare that the project Dissertation titled "**DESIGN OF LOW POWER TIQ FLASH ADC USING TANNER TOOL**" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate ship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "**DESIGN OF LOW POWER TIQ FLASH ADC USING TANNER TOOL**" which is submitted by **PRANJALI AGRAWAL**, Roll No. **2K20/SPD/09**, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere..

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Date: 31/05/2022

Mr. RAJESH BIROK

(SUPERVISOR)

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

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Date: 31/05/2022

Pranjali Agrawal

Pranjali Agrawal
M.Tech. (SPDD)
Roll No: 2K20/SPD/09

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ABSTRACT

ABSTRACT

An internal reference comparator array consisting of complementary metal oxide semiconductor inverters replaces the Vref generator, resistor voltage divider circuit, as well as arrays of differential comparators in a standard flash ADC. The aforementioned design also promises significant improvements in chip space, power dissipation, and speed control because the inverters' threshold voltage acts as the reference voltage. Because the inverter threshold voltage is sensitive to operating temperature/process variations, perturbations in these ADC systems are challenging, necessitating a compensation mechanism. A TIQ-dependent flash ADC with inverter threshold voltage control is presented in this study.The 5-bit flash ADC is developed and evaluated in 180nm technology using TANNER EDA via modifying the TIQ comparator as well as using Power gated, as well as a multiplexer-oriented encoder using transmission gate logic as well as the lector technique.

TIQ comparator as well as Multiplexer-based encoder are used in the architecture. The 2:1 multiplexer are used in this Mux-based encoder. The Multiplexer could be built in a variety of topology, including CMOS, PTL, TGL, as well as Gate Diffusion-Input. The transistor counts in CMOS technology, which is referred to as Area in electronics, is greater, resulting in increased energy usage and latency. Although there are fewer transistors in PTL as well as GDI logics than in CMOS, output stability also isn't maintained. In order to preserve output stability, buffers must be included to the PTL setup. However, the outcomes are insufficient. In order to retain output stability, GDI technologies should use the same algorithm or make certain essential tweaks.

The purpose of this report is on Transmission Gate Logic, as well as the Multiplexer was designed using a lector method. Lector is a low-power technology. Inside the 2:1 multiplexing construction, this method is used with Transmission Gate Logic.

The power gating method is used to create a TIQ comparator in this research. Another low-power option is power gating technique. Power gating is done in

a variety of ways. The injection of an extra transistors at the Vdd connector (known as header switching energy gating) or the earth (GND) connections are used in power gating technology (which is named as footer switch power gating). The second transistor is positioned at the Vdd connector to minimize power dissipation when compared to the traditional technique.

CHAPTER 1
INTRODUCTION

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INTRODUCTION

1.1 Introduction:

Because of the quick advancement of science and technology, digital signal processing had made huge strides. Signal processing does have a number of benefits in the majority of digital fields, including design as well as programmability versatility, decreased silicon space, high precision, as well as lower power consumption. The design approach is both affordable and quick. As a result, a device with a small footprint and high performance can be designed. In wireless technology, picture processing, and other applications, an analogue to digital converter with significantly higher performance is necessary.

MOS has dominated the electronics market for the past few years. Designing analogue circuits with smaller feature sizes, lower supply voltages, and shorter transistor channel lengths becomes more difficult. All performance factors, such as gain, phase, phase margin, unity gain bandwidth, and so on, may be simply traded-off using an opto amplifier. The architecture can be performed using a variety of aspect ratios, such as adjusting the width as well as length of transistors to bring them into the saturated area, which will enhance performance.

Digital systems with high battery capacity and portability are desired. Only by creating applications that use less energy can this be possible. Because ADCs are employed as front-end elements in the bulk of mixtures, we concentrated on creating ADCs that consume less power and hence provide faster performance. ADC designs include serial communication type ADCs, Flash type ADCs, sigma-delta ADCs, and so on. For its parallelism, the result of continuous is not restricted by resolution, and these ADCs are used in systems that demand a wide range of bandwidth as well as fast speed [2].

Analog-to-digital converters (ADCs) are a very well signal circuitry that connect the analogue, digital, as well as computer worlds. The accuracy, speed, and energy usage of an ADC are three critical criteria that cannot be modified once the device has been developed. The architecture of today's ADCs must have a high

performance in terms of speed while consuming less power. Because performance criteria such as sampling rate, power consumption, as well as resolution are largely dictated by an ADC's design, a single ADC type cannot serve all requirements. As a result, picking the right ADC for the job is crucial. There are other types of ADCs available, including SAR ADCs, Dual Slope ADCs, Sigma Delta ADCs, and Flash ADCs, however the Flash ADC is perhaps the most widely utilized for its superior performance indicators. The Flash ADC is primarily utilized in applications requiring high speed and poor resolution. Because of their high performance compared to other ADCs, flash ADC architectures have indeed been extensively researched. It is also known as parallel ADC for its parallel architecture, which makes it quicker.

An A/D converter transforms analog inputs like voltage into digital outputs that a microcontroller can read and operate. Some microcontrollers have A/D converters built-in. The exterior A/D converter can be used with any sort of microcontroller. A/D converter typically have 256–1024 quantization levels and are 8–10 bit. Multiplexed A/D converters are found in most PIC microcontrollers using analogue input channels. The 10-bit, 8-channel A/D converters on the PIC18F452 microcontroller, for instance.

ADCs transform analogue signal, such as heat, pressure, voltages, power, length, or light levels, into digital representations. Following that, the digital model can be handled, modified, calculated, transmitted, or stored. Figure 1 shows a block diagram of the digital signal.

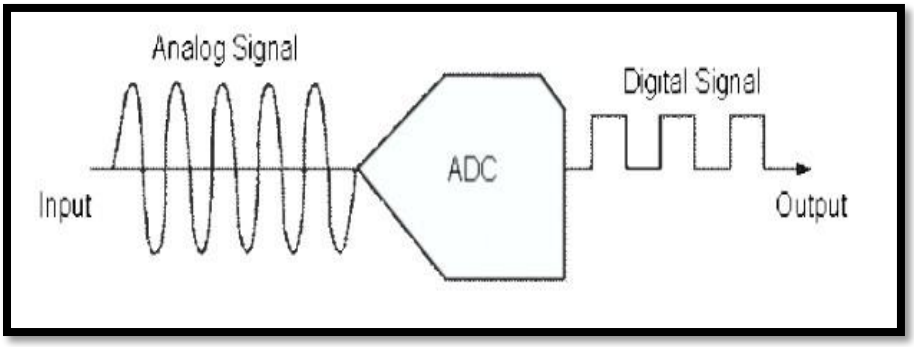

Fig.1: Analog to digital conversion

Digital to analogue translation is usually about a level of a wider measurement and control cycle, in which data in the form is assessed and then reconverted to analog form to operate peripheral transducers. Motors, heaters, and acoustic divers such as speakers are examples of transducers. The ADC's effectiveness will be determined by the measurement and control loop's performance metrics. The ADC's performance indicators will reflect the capabilities and requirements of all the other process control devices in the system.

In today's digitized world, an analog–to–digital converter is a crucial instrument. Among all types of ADCs, the flash converter is the fastest. It is made up of 2N comparators that produce temperature coded output that is then translated to a digital output by an encoder. When applying minimization techniques in high-speed ADCs, the comparator plays a significant role. Because the fundamental drawback of flash type A/D Converter is that it consumes a lot of power, the goal is to create a low-power flash type A/D Converter with such a low-power comparator. Gain, phase, obtain bandwidth, resolution, speed, as well as size and power dissipation, are all design considerations. A high gain comparator can be made using a two-stage op-amp with miller capacitance. Low-power operation is simple.

1.2 ADC:

Analog to Digital Converters (ADCs) convert analogue information into a digital information (ADC). A binary sequence, which would be a combination of bits 0 or 1, is used to describe a bit stream.

ADCs are divided into two categories: direct and indirect.

1.2.1 Direct type ADC

By correlating analogue input against internally generated digital (binary) information, direct type ADCs allow direct analogue to digital conversion.

Examples of Direct type ADCs are listed below.

- Counter type ADC
- Successive Approximation ADC
- Flash type ADC

1.2.2 Indirect type ADC

An ADC is classified as an Indirect type ADC if it performs analogue to digital conversion in an indirect manner. It converts the analogue input to a linear function of time (or frequency) before producing the digital (binary) output. The best example of an ADC of the indirect type is the dual slope ADC.

1.2.3 Flash ADC

Whereas the flash or parallel A/D Converter made up of differential comparators is the quickest type of Analog to Digital Converter [1] and is preferred for its speed as well as monotonicity, it has a large chip area and power need due to the large number of (2n -1) parallel working differential comparators. They also generate a lot of return distortion in the input signal as well as power supply lines [1].

This architecture is also less suitable for VLSI because it necessitates a constant supply voltage "Vref" with a low temp factor, robust line/load control features, and an energy wasteful resistance relied comparison potential divider mechanism.

Tangel et al. [2] proposed a TIQ-based flash ADC that uses a Complementary MOS inverter like a comparator circuit of voltage and changes the threshold voltage to act as an interior baseline voltage level for the assessment. In a conventional flash ADC, a differential amp oriented comparator arrangement is replaced with an ensemble of reverse Complementary MOS inverters, removing the need for a steady supply voltage as well as a potential divider circuit. This method increases throughput, space, and static energy usage by using properly calibrated Complementary MOS inverters as a comparator with such an internal reference voltage signal. Every TIQ module in the comparator arrays must be in equilibrium since it serves as a different internal voltage level against which the input is evaluated.

1.3 Low Power Techniques

Power gating, clock gating, and transistor stacking just are a few of the low-power approaches available. Leakage currents of MOSFET devices are the main cause of static power consumption. It occurs when an undesired power (sub threshold current) flows through the transistor's channels even if it is turned off. The threshold voltage for transistors in circuitry is substantially influenced by this. Scholars have devised a variety of power gating approaches to mitigate this flaw. In this research, we

use the lector technique to propose a Mux-based encoder for transmission gate logic. One of the power gating strategies is the lector approach. We can save energy by turning off the circuit's electricity using this method.

1.3.1 Basic Lector Approach

The efficient layering of transistors in the circuit from supply voltage to ground is the core notion behind our strategy for reducing leakage power. "A condition with much more than a transistors switched out in a supply voltage to GND path is considerably less leaking than a condition with a single mosfet switched out in any supply to earth path." In our method, each CMOS gate has two leakage control transistors (LCTs), one of which is near its cutoff zone of activity.

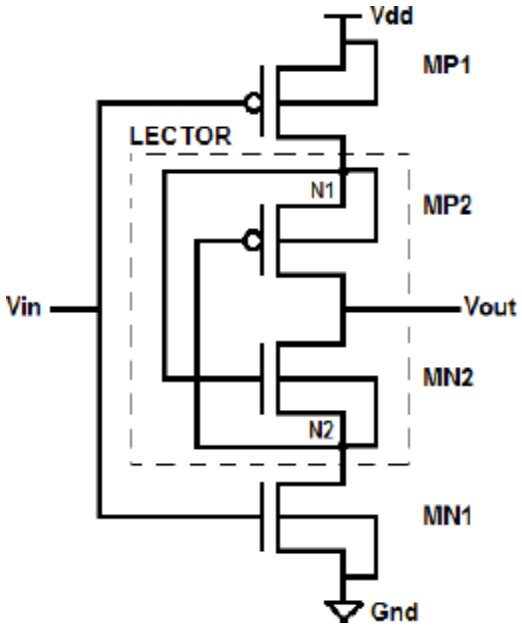

Fig.2: Circuit diagram for Lector approach of Inverter.

1.3.2 Transmission Gate Logic:

- A parallel connection of PMOS and NMOS makes up the transmission gate.
- PMOS and NMOS gate voltages are complementary.
- Because PMOS and NMOS are connected in parallel, the effective transmission gate resistance is nearly constant.
- The circuit is bidirectional, meaning it may carry current in either way.

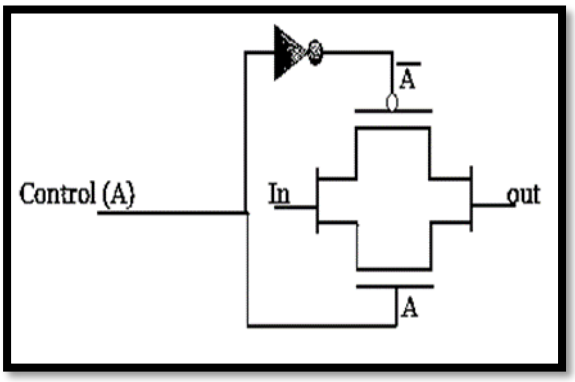

Fig.3 Basic circuit of Transmission Gate

Working: Whenever control is adjusted to high (1), each transistors are turned on together at the same time, as well as whatever is given to the inputs is sent to the output. Whenever control is low (0), dual transistors are turned off at the same time, and whatever is given to the input does not touch the output, resulting in high output impedance (Z).

1.3.3 Power Gating:

Whenever specific blocks are not functioning towards to the outputs or are in idle state, power gating is used to switch off the power source to them. Transistor stacking techniques could also be used to power gate. The sub-threshold leakage current running through a sequence of transistors is bent off in this approach.

New power gating systems using energy recycling technologies have indeed been devised, allowing for a reduction in the amount of switch power lost when switching devices are turned on and off. Both at the sleep-in and wake-up times, charge sharing between virtual VDD and VSS lines saves electricity. The PMOS and NMOS switches are used to connect the virtual VDD as well as VSS lines to the true power supply as well as ground supply, respectively.

When the sleep time is relatively short, charge-recycled power gating can lose more energy than power gating systems that do not include charge sharing. It also takes longer to equalise the charge-recycled power gating's virtual VDD and VSS lines. It takes longer to wake up as a result. Charge recycled power gating may not be appropriate for use in fine grain leak control approaches, where circuits flip between active and sleep states often and quickly, due to the substantial energy loss and delayed wake-up time.

As a result, the sleep duration of a fine-grain leakage control strategy is likely to be substantially shorter than the sleeping period of a coarse-grain leakage suppressing method that can wake the logical blocks as quickly as feasible at the awake point. Moreover, any energy lost as a result of this power gating must be minimal.

CHAPTER 2
LITERATURE REVIEW

CHAPTER-2

Literature Review

2.1 Literature Survey on Advance & Research Trends in Information & communication technologies

ADC are critical in today's digital world because they can handle a wide range of tasks. The quickest ADC accessible is the Flash ADC, although it has a high power consumption. This study intends to establish an ultralow-voltage development strategy to increase the energy efficiency of fast-performance medium-resolution flash ADCs. Lowering the line voltage lowers the power consumption of a digital system, but only if the latency is extended. The flash ADC is made with 45nm CMOS technology and a voltage boosting focused comparison approach using forward body biasing. This method reduces power consumption by keeping the latency nearly unchanged while the input voltage is reduced. For offset compensation, a body-bias calibration method is used.

K. N. Hosur et al. present a concept for a 4 bit flash analogue to digital converter in a cadence system using 90nm gpdk technology, as well as a new voltage comparison circuit called TMCC. Unlike traditional differential voltage comparators, TMCC comparators are designed to control input offset voltages while also methodically and continuously altering the difference device pair's transistor size and form. To evaluate extremely minor voltages, minimize the resistance ladder approach, plus enhance uniformity in ADCs, TMCC comparators have been used. The resistor ladder can be fully removed to reduce bulk and power consumption.

In today's digital age, analog-to-digital (ADC) converters have become a highly significant aspect of electronics since they have a wide range of uses, as Rakesh Ranjan explains[5]. The Flash ADC is among the quickest ADCs available, but it has one major disadvantage: it consumes a lot of power. As a result, the primary goal of this work is to create a high-speed, low-power Flash ADC. A 3-bit resolution design was developed utilizing seven OTA-based comparators with such a voltage level of 250mV, and a high-speed encoding was created using four full adders upon which incorporation of multiple blocks ADCs was developed. Inside the Cadence Virtuoso Design, all circuitry are modeled employing 180nm technology. The power supply is 1.8 volts. The

encoder receives the analogue output of the each comparator based on the comparison between both the input as well as the reference voltage, and the digital format data is generated.

This paper describes a Flash ADC with such a Wallace tree encoder and a TIQ comparison. For 3 bit ADC, there is a DC and transient analysis report. The project includes a comparison of Wallace tree as well as ROM encoders to show how electricity could be saved through using Wallace tree encoders rather than ROM encoders. Piece-wise linear as well as sinusoidal input were modeled and simulated for the concept. There are additional descriptions of the 4 bit as well as 5 bit flash ADCs with TIQ comparator as well as Wallace tree encoder.

2.2 Literature Survey on Control, Power, Signals, Communication & computational Applications.

M.P. Anjayya makes the following proposal: The flash ADC, also known as parallel ADC, is the fastest analogue to digital conversion. It's perfect for high-bandwidth applications[11]. A resistance ladder, comparison, as well as encoder circuits all are part of the circuit. A thermometers value is the comparator's result. A appropriate encoder must be used to transform it to binary digits. When building a low-power Flash ADC, reducing the encoder's power consumption is a crucial consideration. ROM encoders, fat tree encoders, Wallace tree encoders, and MUX oriented encoders all are compared in this article. The fatty tree encoder is the quickest, but its structure is much more complicated. The design and layout become complex as a result of this. In term of bubble error checking, the Wallace tree encoder is the best, but it is also the most power-hungry. The multiplexer-based encoder is the most power-efficient and straightforward of the three. As a result, it's better for designing low-power Flash ADCs.

This study compares and contrasts various comparator architectures for flash ADC architecture. The charge sharing dynamic latching comparator, with such an energy dissipation of 0.00133 W and a transmission latency of 1.699 ns, verifies the minimal wattage, super-fast circuit characteristics anticipated. In comparison to other systems examined, this one has the shortest power delay product. A charge sharing dynamic latching comparison is a superior alternative for a low-power, high-speed Flash ADC. The next stage is to build and implement a Flash ADC based on this comparator build, as well as to validate that the overall power consumption and

propagation latency are as low as stated. The next stage is to create a new design in order to acquire space-saving comparator circuit.

Pradeep Kumar explains the planning and development of a 3-bit flash Analog into Digital converter with low power (ADC)[9]. It contains seven comparator circuit as well as a thermometers into binary encoder. It uses 0.18um CMOS technology. T-Spice is used for ADC pre-simulation, while Microwind3.1 is used for post-simulation. A three-bit flash ADC architecture featuring reduced hardware cost as well as delay is proposed in this research. For accurate results, the input voltage must be greater or less than the comparator's predicted values by around 0.05 volt.

Flashing design is well renowned for its quickness while Analog to Digital conversion, according to Biswas & Suman. This paper demonstrates a 4bit Flash analogue to digital converter. This research uses a variety of thermometer into binary encoders as well as compares their delays and power. This Flash ADC's functioning is confirmed through transient analysis. The primary goal is to create a Flash ADC with such a low-power comparison in order to reduce total power usage. The goal is to utilize a low power comparator in order to lower the device's energy usage because it uses 2n1 number of comparator. Cadence virtuoso design environment simulator is used to model the flash ADC in 180nm tech.

The concept of a two-stage op amp is presented by K.J Raut and A.C Bhagli (Op Amp). The circuitry was created using a 180 nm digital n-well CMOS technology. Massive open loop gain, high uniform gain bandwidth, high input impedance, low output impedance, as well as high speed are the essential requirements for just an operational amplifier. Many analogue subsystems, especially switching capacitance filters, require these amplifiers. For decades, CMOS analogue circuit design has outperformed its competitors since the same technique could be utilized to build both analogue and digital basic components on the same chip.

A 3-bit threshold inversion quantized oriented flash analogue to digital converter chip is demonstrated by A. Talukder and M. S. Sarker in a simple as well as upfront construction[3]. In contrast to previous ADCs, this TIQ-oriented A/D Converter does not need an on-chip or off-chip reference signals of voltage. By altering the W/L ratio of the nMOS as well as pMOS in CMOS technology, an inverter's switch voltage

could be tuned to a needed input voltage. The ADC circuit is designed in Cadence Layout Suites in AMI's C5 method, then it was built & evaluated in Cadence Virtuoso.

2.3 Literature survey on Applications involving two protocols

Ultra-Wideband (UWB) communications is a relatively new elevated wireless network which transmits data using sub-nanosecond pulses. According to the FCC, ultra-wide band technology is a type of wireless technology wherein transmissions occupy a broad bandwidth of more than 500MHz or 20% of the signal's center frequency. The processing of the UWB signal necessitates the use of a high-speed low/medium resolution ADC. In high-speed communication applications, the flash A/D Converter is frequently the best choice because to its low latency and rapid conversion speed. As a result, we analyzed and constructed a 5-bit Flash A/D Converter having 500Msamples/s sampling rates. This 5-bit Flash ADC has 31 comparators, a 32-resistor resistor ladder, as well as a thermometer-to-binary code conversion. Every one of the layouts were simulated using UMC 0.18m technologies and a 1.8V power source.

This 24 GS/s, 3 bit flash ADC on 28nm low-power (LP) digital CMOS is designed as well as characterised by G. Tretter as well as M. Khafaji[15]. The circuitry was created with the purpose of outperforming state-of-the-art achievement for just a single ADC unit. To the best of our knowledge, the ADC can give its entire sampling rate without temporal interleaving, making it the fastest single thread ADC in CMOS. Through modest time interleaving, the given ADC's high sampling frequency allows for ultra-high-speed ADC systems.

Even though flash ADC is the quickest accessible, it requires a large amount of IC real estate to execute, according to Megha R as well as Pradeep Kumar K A[9]. The biggest downside of flash ADC is that it requires a large amount of space and generates a lot of heat. The number of comparators is reduced by employing mux to solve this complexity. To produce reference voltages, multiplexers are utilised. The presenter will demonstrate a 4-bit CMOS-based flash ADC with a simplified comparator as well as multiplexer design.

For high-speed applications, S. Mishra, A. Vidyarthi, and S. Akashe recommended The ADC is optimised in terms of resolution, speed, as well as power[8]. With just an operating voltage ranging of 700 mV to 1V, the high integrated flash ADC is built with three-bit precision. This paper also explains how to use the folding

approach to reduce the size of a flash ADC and enhance its bit size. To reduce the number of comparators as well as resisters needed to generate the reference voltage, a factor of four is implemented. Interpolation decreases input capacitance, latency, and increases input signal bandwidth. Folding as well as interpolation ADC is suitable for ultra-low-power applications.

Sequential approximations register analog-to-digital converter for biological needs is presented by You-Kuang Chang[14]. The shifting pattern dominates the power dissipation needed to charge and discharged the capacitance array. The traditional switching sequence is wasteful, as it wastes a lot of energy charging / discharging the capacitance array. A low-power switching sequencing technique has been proposed. When contrasting to a standard switching approach, the capacitance array's average switching energy can be lowered by 56%.

2.4 Literature Survey on VLSI designs

A low-power (adaptive) flash ADC is proposed in this project. The ADC allows for exponentially power loss as well as linear precision reduction. Just the leakage power is consumed in the suggested architecture since unused parallel voltage comparators were converted to stand - by mode. The ADC has a sample frequency of 1 to 2 GSPS and is capable of 4-bit, 5-bit, and 6-bit precision. Cadence tools were used to develop as well as simulate the ADC in 65nm CMOS.

A switching reference voltage is used to generate the most significant bit (MSB). The reference voltage was switched over mid-point voltage (Vk) in relation to the input signal using a control circuit. In contrast to typical flash ADCs, which require two N1 comparators, the current design only requires two N1.

CHAPTER 3

Flash ADC using TIQ Comparator

CHAPTER 3

Flash ADC Using TIQ Comparator

3.1 Background:

With N bit precision, a flash type ADC uses 2N-1 comparers, 2N resistors, as well as an encoder. To contrast input voltage to sequential reference voltages, each voltage comparator receives an analogue input. A succession of pmos loads could be used as a reference voltage ladders to save chip area complexities. VDD R1 & R8 are taken as 2K ohms, whereas the others are 1Kohms. If Vref is less than Vin, each comparator returns 1; otherwise, it returns 0. The binary encoder receives the digital output from the compared analogue input. These are the fundamental components of a flash ADC. Figure 4 illustrates the layout of the Flash ADC.

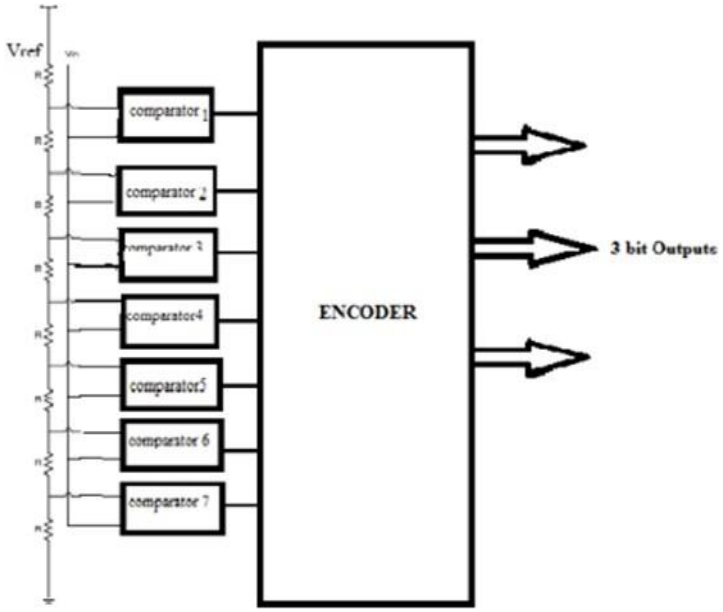

Fig.4: Circuit diagram of Flash ADC

3.2 TIQ Comparator:

A TIQ comparator-based Flash ADC is designed in this project. The threshold adjusted TIQ module is shown in Figure 5. Three CMOS inverter structures are used in the concept. A DC feedback loop is used in this self-tuning design to self-correct the inverter threshold voltage. The threshold self-tune approach is

detailed in detail below. The threshold voltage of the master as well as slave inverters is set using a resistive divider consisting of R0 and R1. The master inverter, which is coupled to the supply rails via an NMOS (NM3) as well as a PMOS, is the most important component of the threshold adjusted TIQ-comparator (PM3).

Those mosfets act as negative feedback in this design since they are biased in their linear (triode) operating areas. Those transistors' gate terminals are powered by the master inverter's output terminal, effectively acting as voltage regulator resistance, with resistors regulated by the master inverter's output voltage.

The aspect ratios of the master and slave inverters match. The master inverter produces voltage level to self-correct the impedance of the twin MOSFETS connected to the electrical supply when its source is tuned to the requisite threshold voltage. The negative feedback loop acts as a self-correcting feature, allowing the master as well as slave inverters to retain their pre-set changeover thresholds regardless of processing or temperature fluctuations.

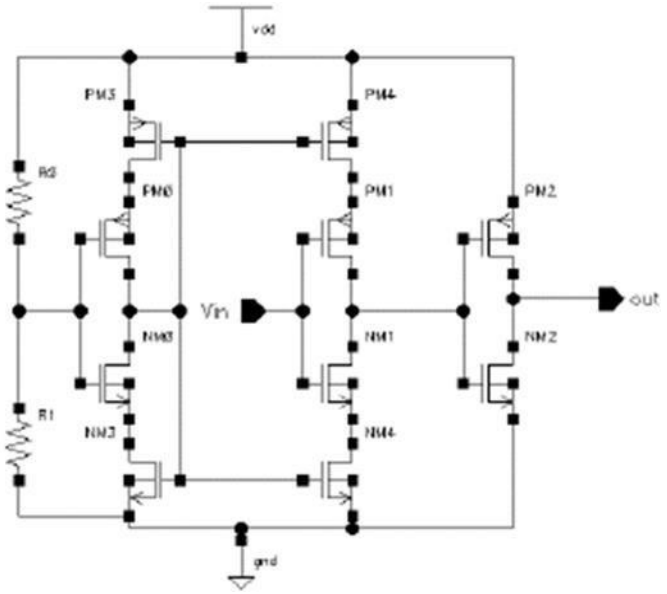

Fig.5: TIQ comparator with Threshold compensation

If the master inverter's threshold drifts below the preset value due to processing or thermal faults, the output voltage falls below the set point value, causing NMOS (NM3) channel impedance to rise and PMOS channel impedance to fall (PM3). Because of changes in impedance toward its electrical connections, the inverter's shifting threshold climbs linearly to the prescribed value. The negative feedback loop continues until the threshold is reached. When the transitional threshold

crosses the set point value, the system uses a similar negative feedback method to self-adjust the threshold to the required value.

The slave inverter tracks the master inverter by taking into account resistance changes of PM4 and NM4. The ability of this circuit design to self-tune the inverter threshold voltage and so stable the comparator's inner reference signal is a critical benefit, as it eliminates the requirement for Analog to digital converter calibration during startup or operation.

TIQ Comparator transforms analogue input data to thermometer data. We will now transform thermometer information to binary format using the mux-oriented thermometer to binary encoder circuit. It requires a 32-bit TIQ Comparator array and a 32-bit mux-based encoder circuit because it is a 5 bit flash ADC.

3.3 MUX Based Encoder:

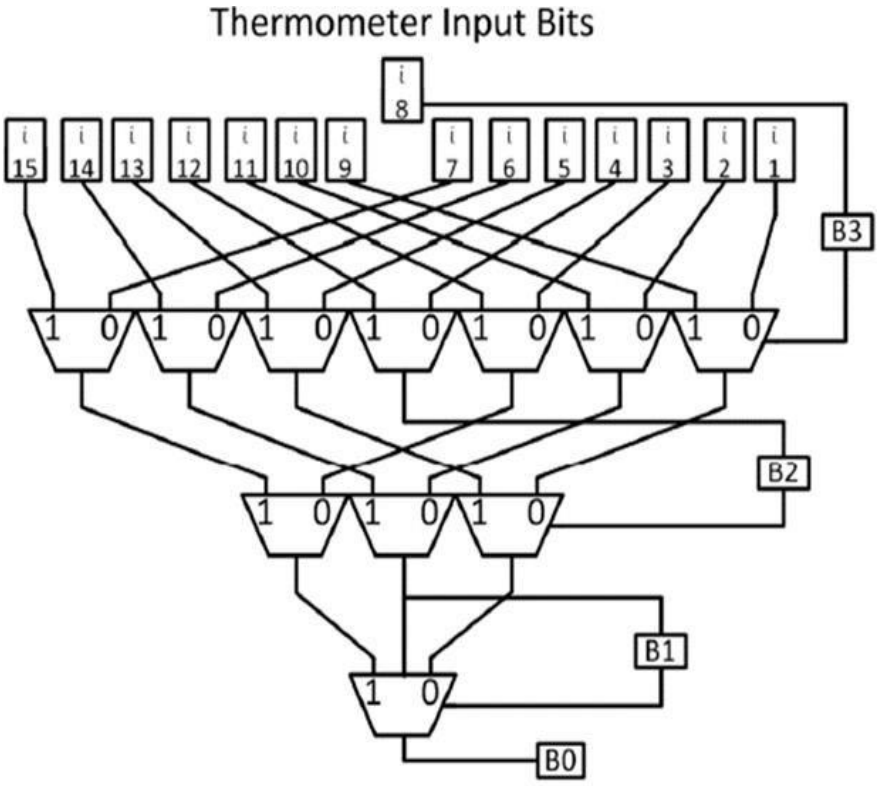

Fig.6: Schematic of Mux based Encoder

Figure 6 depicts the structure of Mux based encoder. The most significant bit in binary code is also high if half of the thermometer code indicates logic high. In binary output, the value 2n-1 indicates MSB. This thermometer code is broken into 2 codes again in order to determine a binary output. To get a choose line for the second phase Mux, the prior phase multiplexer result is used. The process is repeated until the last 2:1 mux is finished, about which point the LSB of binary output is obtained. Even if the resolution is enhanced, with this 2:1 multiplexer, we can quickly build an encoder while consuming less power.

In this concept, the Mux design is implemented using CMOS technology. The schematic for 2:1 Multiplexer is illustrates in Fig.7

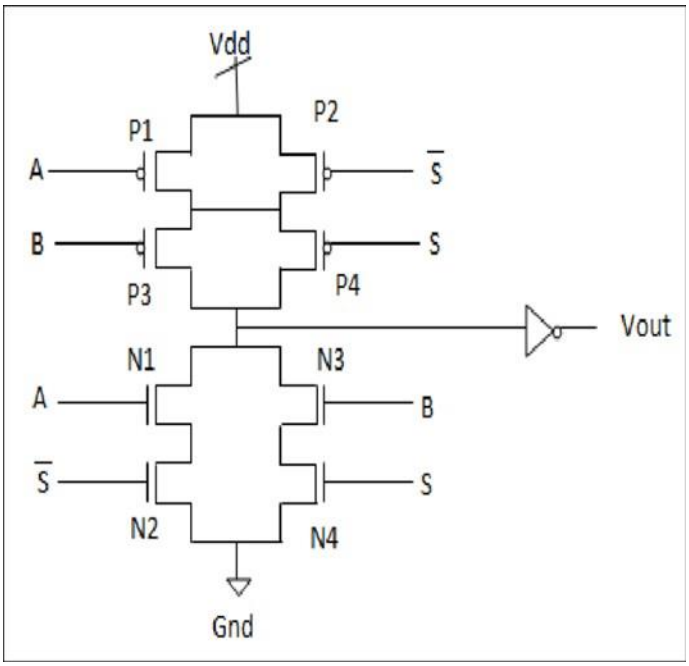

Fig.7: Circuit diagram for 2:1 multiplexer using CMOS logic

The fundamental benefit of this model is that it can perform any Boolean expression using PMOS devices in a pull-up circuit, although a pull-down network uses NMOS devices thus result is achieved here between voltage as well as ground ends. The main disadvantage of this architecture is that as the amount of transistors increases, so do the size, power, and latency of the circuit.

3.4 Overall structure of TIQ Flash ADC:

The overall structure of TIQ flash ADC includes TIQ comparator instead of Op-Amp and Mux based encoder instead of Priority encoder or Wallace tree encoder. The overall schematic diagram of TIQ flash ADC is shown below in fig.8.

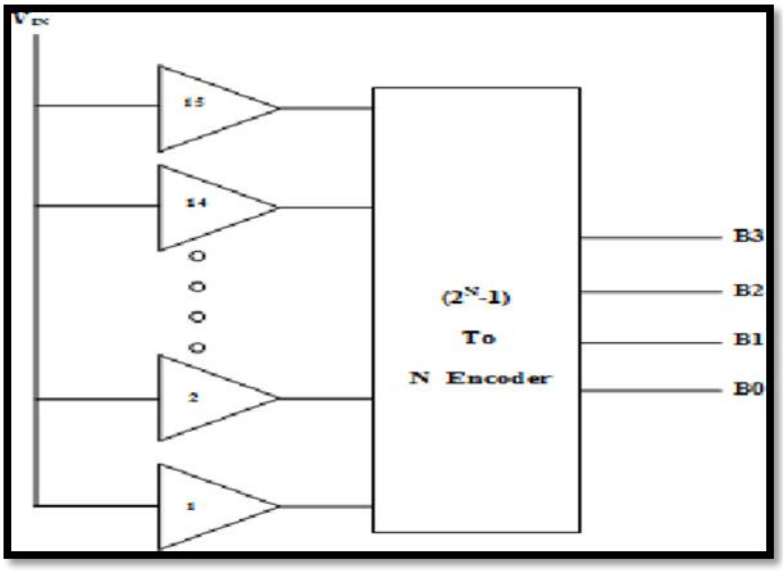

Fig.8: schematic of TIQ Flash ADC

CHAPTER 4

FLASH ADC USING MODIFIED TIQ COMPARATOR & MUX BASED ENCODER

CHAPTER 4

FLASH ADC USING MODIFIED TIQ COMPARATOR & MUX BASED ENCODER

4.1 Introduction:

In this section, we are describing the TIQ comparator using Power Gating Technique and also Mux based encoder using transmission gates along with lector approach. And implementation of flash ADC by employing modified TIQ comparator as well as Mux related encoder. Here, the modifications in TIQ comparator as well as Mux based encoder are done in order to achieve better results in terms of power consumption.

The above changes made possible the below listed advantages:

- Due to the employment of low-power techniques, power consumption is relatively low.
- Transistor count is also less due to the use of MUX designed in TG Logic.
- Power consumption is reduced in Modified TIQ comparator by using Power Gating.
- Area & power dissipated as well reduced using TG logic along with lector approach.
- Even though adopting these techniques, output stability is better.

4.2 Modified TIQ comparator:

In this project, a Threshold Inverted Quantizer comparator based Flash type of Analog to Digital Converter is implemented. The threshold compensated TIQ module can be shown in Figure 9 below. Three CMOS inverter architectures are used in this design. In this self-tuning system, a DC feedback loop is used to self-correct the inverter threshold voltage. The threshold self-tune procedure is explained in the following section. A resistive divider consisting of R0 and R1 is used to set the threshold voltages of the master and slave inverters. The master inverter, which is coupled to the electric lines via an NMOS (NM3) as well as a PMOS, is the threshold compensated TIQ-heart

comparator (PM3).

In this configuration, these mosfets are biased in corresponding linear (triode) functioning regions as well as serve as negative feedback. These devices' gate contacts are powered by the master inverter's output node, merely acting as voltage controlled impedance, with resistances regulated by the master inverter's output signal.

The aspect ratios used by the master as well as slave inverters are identical. The master inverter produces the control signal needed to self-correct the impedance of the two Transistors access to the main supply whenever its input is changed to a predefined threshold value. The negative feedback loop acts as a self-correcting function, allowing the master and slave inverters to maintain their pre-set switching thresholds despite PVT fluctuations.

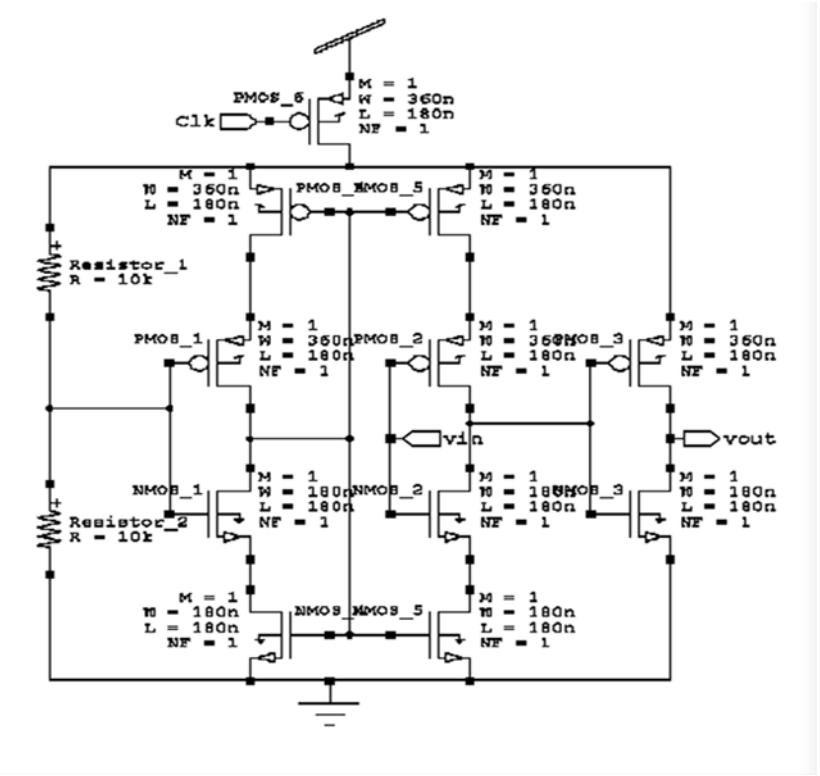

Fig.9: TIQ comparator using power gating

Here, an additional pmos transistor is inserted to interrupt the supply to the circuit. By that, it disrupts the path provided between vdd to gnd. So that, we can reduce the power consumption. And the additional transistor is controlled by Clk input signal.

4.3 Modified MUX Based Encoder

The schematic shown below the structure of Mux based encoder. This schematic is designed for 3-bit encoder. Based on this architecture of encoder, in this research, we are implemented the mux oriented encoder for 5- bit in order to implement 5-bit flash ADC.

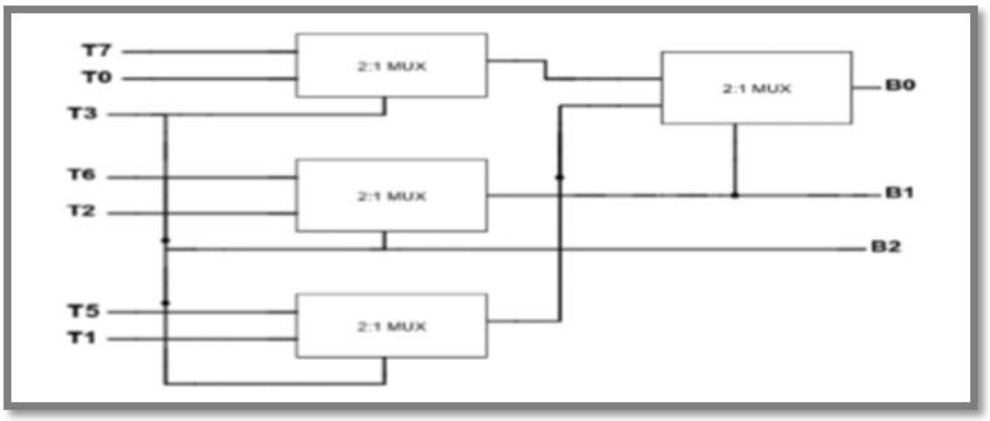

Fig.10: Schematic of Mux based encoder

Here, 2:1 MUX is designed in switch logic which is also known as transmission gate logic. By this, we reduce the count of transistors which is nothing but area on comparing with 2:1 Mux based on CMOS technology. In this paper, we are not only using transmission gate logic but also we included lector approach in the design of Mux based encoder. From this, the power consumption is further reduced over CMOS technology.

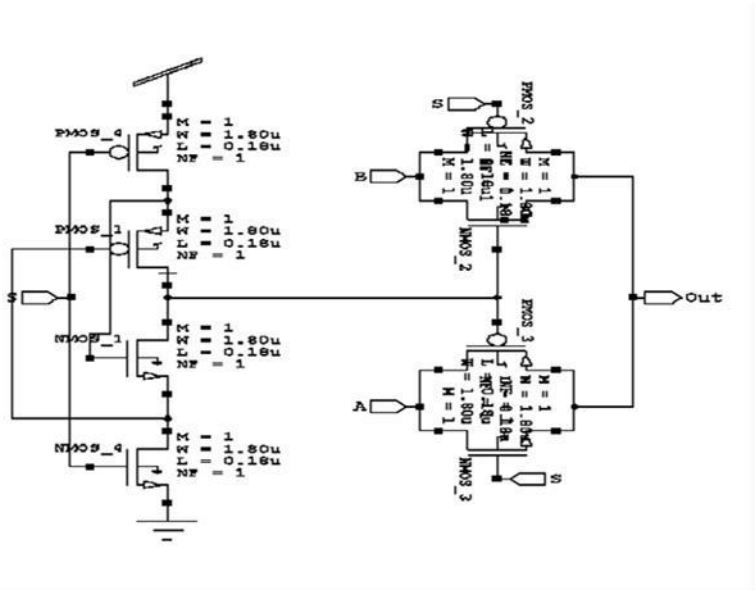

Fig.11: schematic of 2:1 Mux based on transmission gate logic using lector approach.

In this schematic, the lector approach is used in the inverter employed in the design. Basically, Lector approach is one of the low power techniques. The appropriate stacking of mosfets in the circuit from power supply to ground is the core notion underlying our strategy for reducing leakage power. "A condition with more than one mosfet turned off in a voltage source to ground pathway is considerably lesser leaky than that of a condition with only one mosfet turned off in any source to earth route." In our approach, every CMOS gate has two leakage control transistors (LCTs), one of which is near its cutoff zone of functioning.

4.4 Proposed structure of 5-bit flash ADC

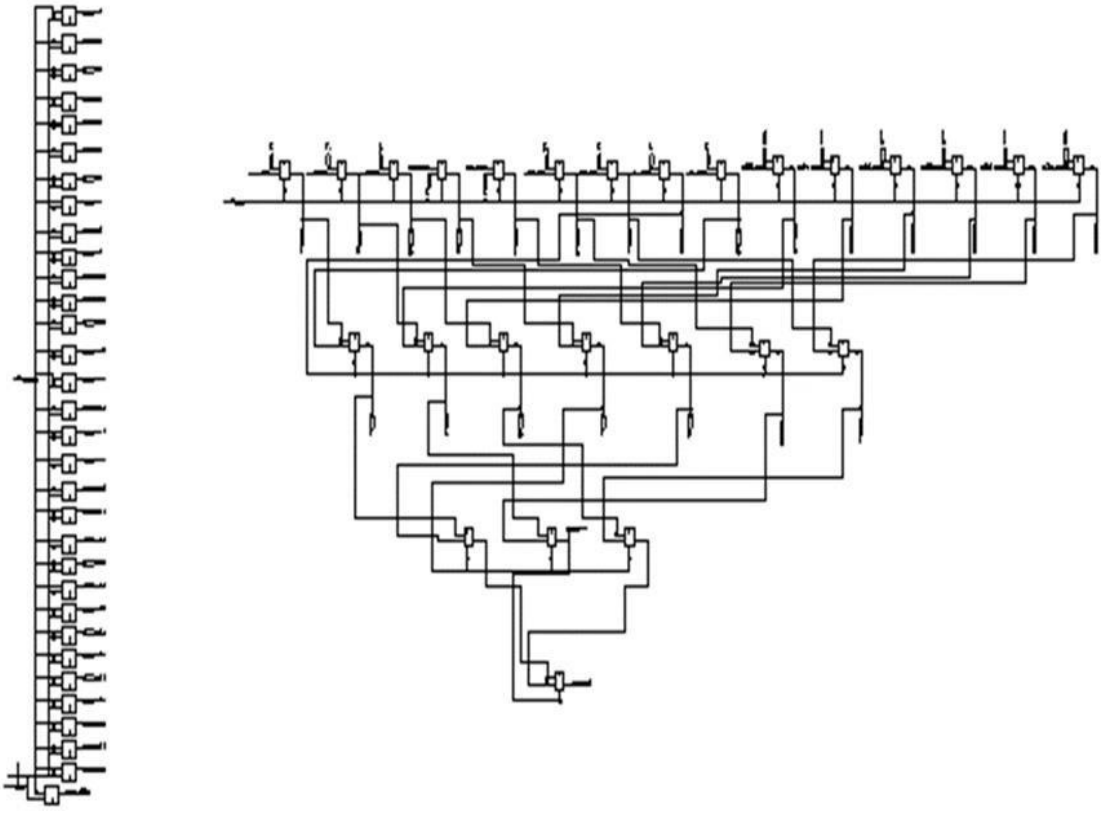

Fig.12: Structure of proposed flash ADC using modified TIQ comparator and Mux based encoder.

CHAPTER 5

DESIGN SPECIFICATION

CHAPTER 5

DESIGN SPECIFICATION

5.1 Introduction:

In the period of integrated circuits, engineers had to take a seat down and physically draw transistors and their connections on paper to style them specified it will be fancied on semiconducting material. Larger and complicated circuits demanded a lot of engineers, time and different resources and shortly enough there was a requirement to own a more robust approach of planning integrated circuits.

To draw the schematics in Tanner EDA tool. Some specifications are required which includes which bit flash ADC is to be designed, what is the (W/L) ratios of PMOS Transistors as well as NMOS Transistors and finally what is supply voltage to be provided for the design.

In the (W/L) ratio, the Length L remains same for a particular technology. For an instance, if we have to design the schematic using 45nm. The value of L represents the length of channel and it remains same 45nm for both NMOS as well as PMOS transistors. In this aspect ratio, the variations takes place in the W parameter which represents Width of the channel.

In Tanner EDA tool, there exists some default specification which we may also change as per our requirements. Those default specifications includes the technology as the 250 nm technology library and the (W/L) ratio is also considerably fixed to the value of 10. For an instance, L=250nm which is also represents as 0.25µm. W will be 2.50µm.

As per the study of Analog Electronics, Digital Electronics & Pulse and Digital circuits. We can strongly define that the width of PMOS is twice as that of NMOS. And this can also vary at certain application or conditions such as fixed PVT variations, changes in threshold voltages and also as per the default constraints of the circuits or designs.

5.2 Procedure to Design in Tanner EDA:

Tanner EDA software has four main tools for application. They are S-edit, T-spice, W-edit and L-edit. S-edit represents the schematic editor which is used to

design the circuit, whereas T-spice represents the Tanner-spice, in which the automated code for the design is generated. W-edit is referred as Waveform editor, which is used to display the waveforms for particular instances or ports in the design. While L-edit represents Layout editor which is used to draw Layout for schematic drawn in S-edit.

5.2.1 Launching of S-edit.

To launch S-Edit, double-click on the S-Edit icon.

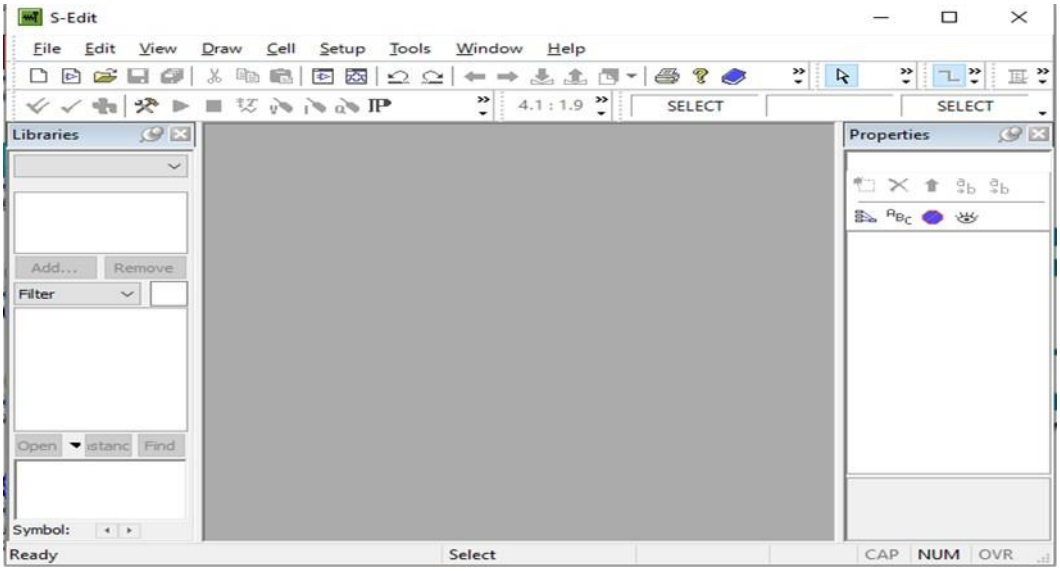

Fig.13: Launching of S-edit

Go to >>file >> New >> New Design

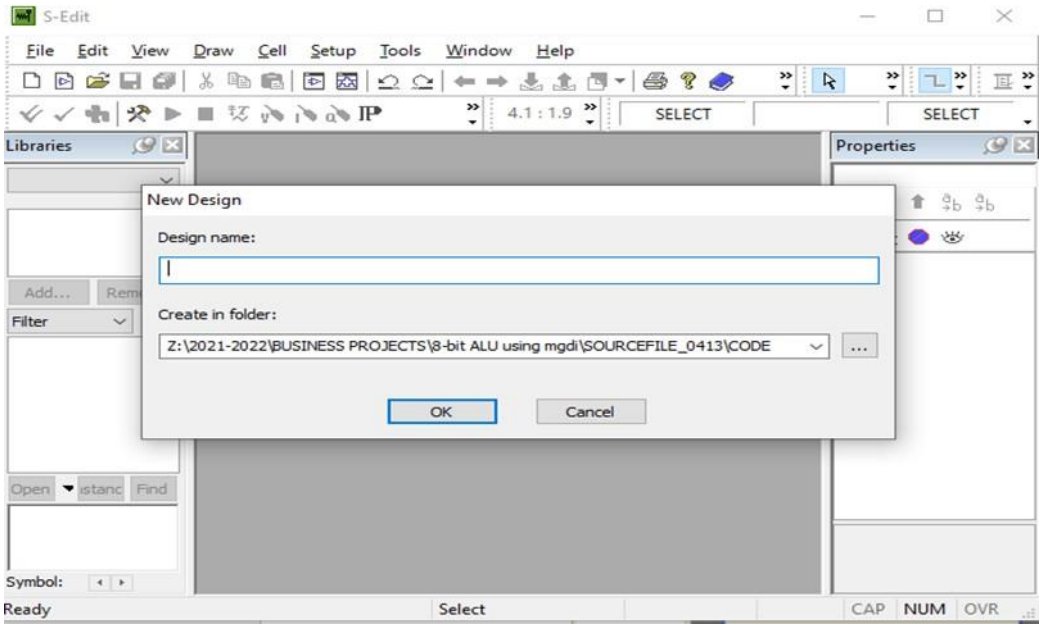

Fig.14: Window to provide Design name and creation of folder

Give your design a name of your choice.

Make a Folder: Specify the location where the S-Edit records should be saved.

After that, select 'OK.'

To add libraries to your project, go to the library window and click Add on the left.

Indicate the location of the Libraries.

For example,

Z:\PAVANI\Tools\Tanner EDA\Tanner Tools v13.0\Libraries\All\All.tanner

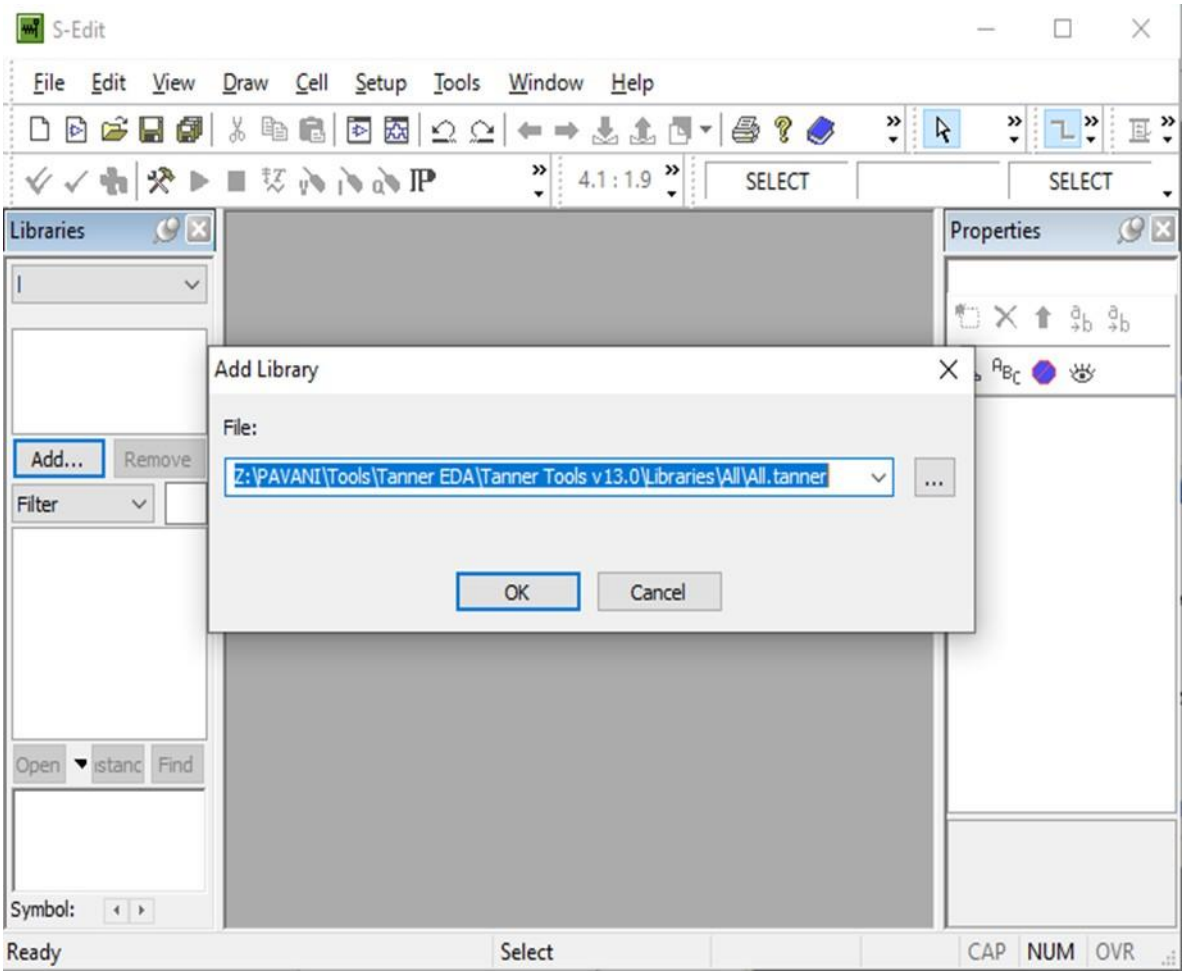

Fig.15: Window to add libraries required to draw the design.

Develop a new cell here.

>> Select a cell >> New view

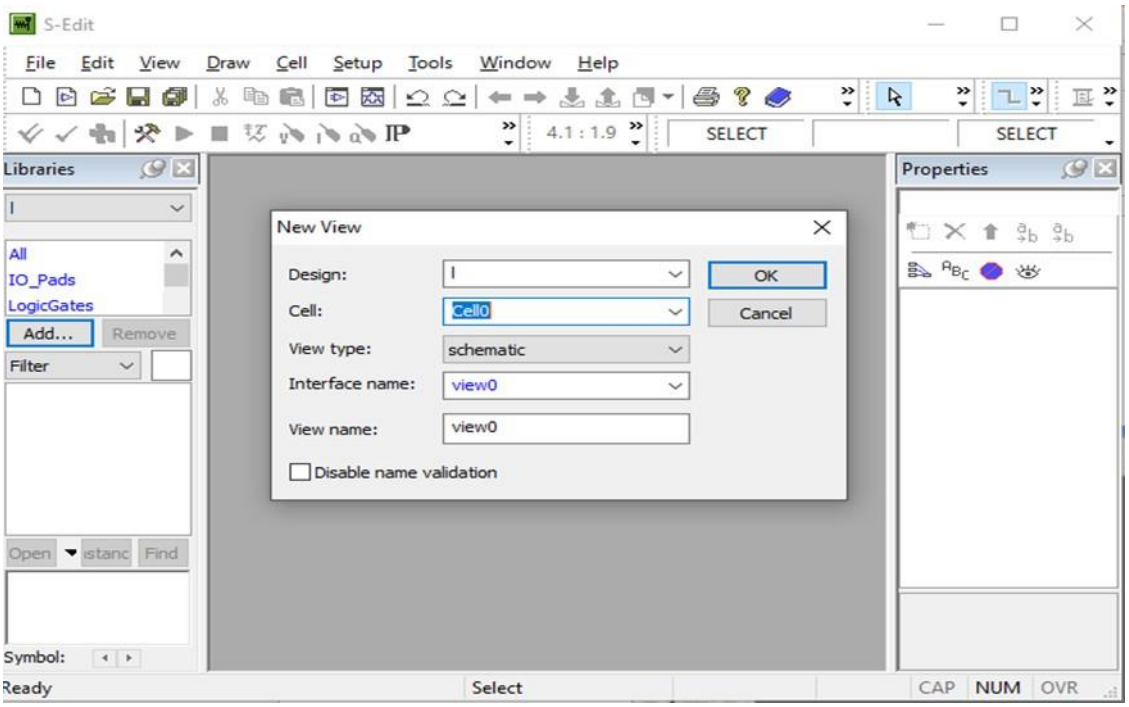

Fig.16: Window to provide cell name & view type

The schematic of any circuit will then show in a cell. Some white bubbles were positioned in a certain order in the black pane. Grid is the term for this type of arrangement. Click on the black screen and then scroll the mouse to modify the grid distance.

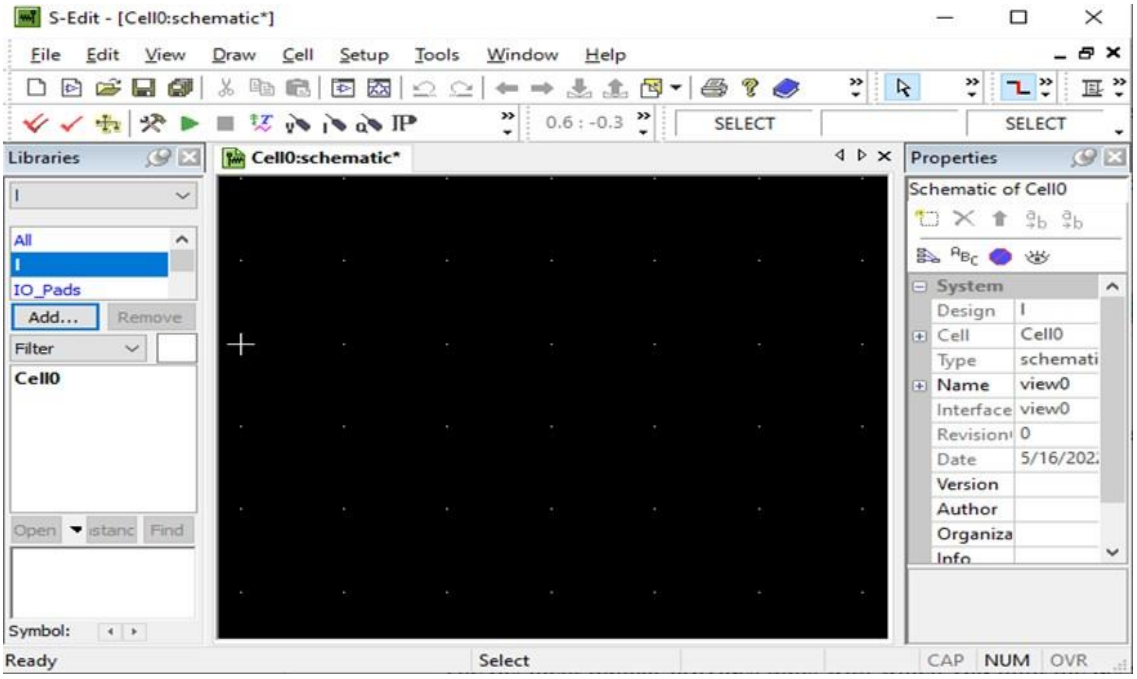

Fig.17: Window represents cell view to design schematic

To make any circuit schematic.

Inverter, for example.

a) To access all devices, go to >>libraries and afterwards press enter on device.

b) Choose the certain device, for illustration, NMOS Device, and then click “, instance. Similarly, for PMOS

c) At this instant, we can change the properties of device as per our requirement.

d) DRAG the chosen component into the cell then place where ever you need it to appear before pressing DONE. After that, press ESC or click DONE.

e)  click on this symbol to connect through wire between devices

f)  Provide Input & Output by connecting In port & Out port

g) In the dialogue box, you may now name the port as you desire. Click OK after that.

h) After you've finished these processes, connect the voltage (VDD) and grounded (GND).

i) For that Go to libraries>> MISC >>Select VDD or GND

j) Finally, the schematic design is created.

By following these steps, we can draw any type of schematic through instantiations.

CHAPTER 6

SIMULATION RESULTS

CHAPTER 6

SIMULATION RESULTS

6.1 Simulation Procedure:

After you've completed your schematic design, check to see if it meets the requirements of the Specification. That is why pre-layout simulation is necessary.

For simulation go to>> tools>> T-spice>> ‘ok’

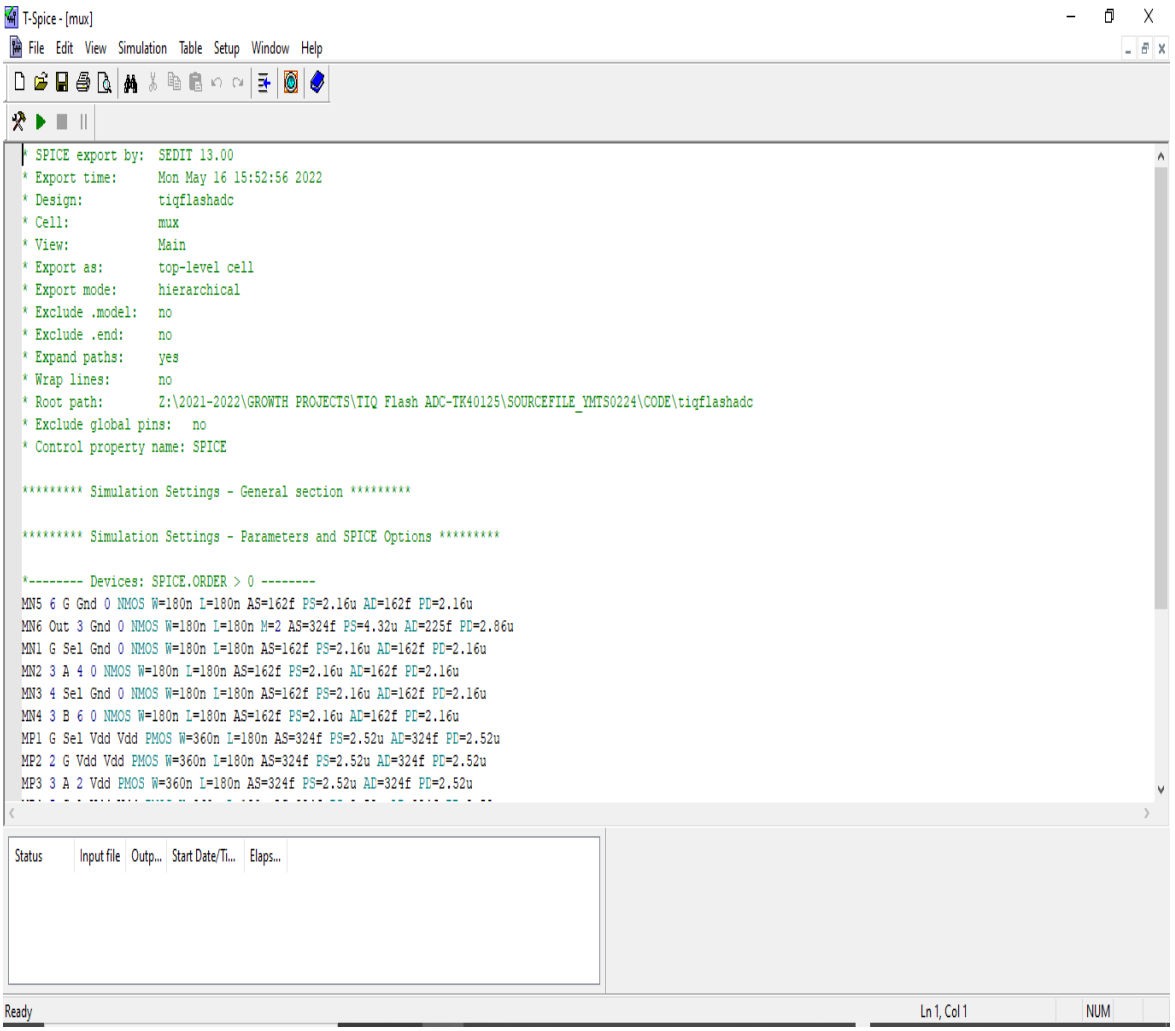

Fig. 18: T-spice window displays

 Then click on this symbol.

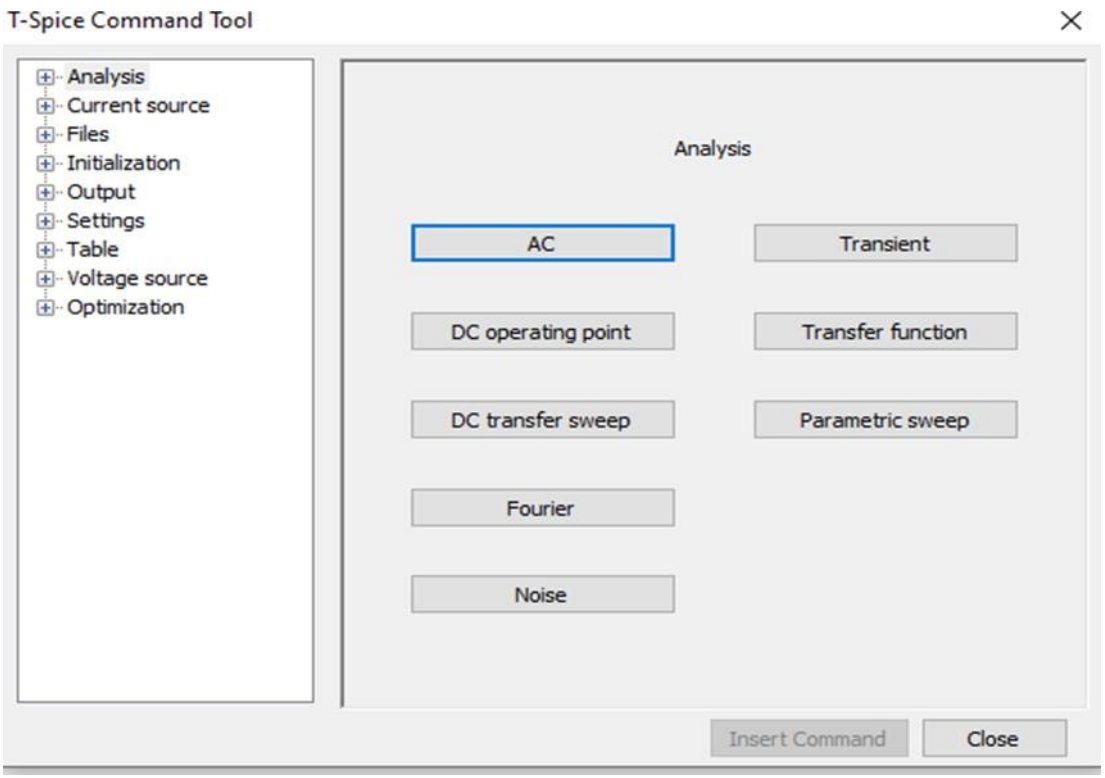

Fig.19: Window for inserting commands

Let's get started with the transient analysis of Inverter.

Phase 1: TSMC 0.25m Technology code must be included.

For that

Go to >> T-spice command tool >> Files >> Include >> browse TSMC .25µm files

>> Insert command.

Phase 2: Then to give Input

T-spice command tool >> Voltage source >> select type of input you want to give (lets

Take bit) >> Insert command

Phase 3: Analysis

T-spice command tool >> Analysis >> select type of analysis you want to give (let's take

Transient) >> Insert command

Phase 4: Output

T-spice command tool >> Output >> which output you want to see >> Insert Command

```
v2 CLK 0 BIT ({01} pw=50n on=2 off=0 delay=0)
.lib "T:\A VIJAYA  LAKSHMI\Nanometer Technology Files\TSMC018.md"

v5 Vdd GND 2
.print tran V(vin) v(b0) v(v1) v(s4) v(m8) v(t16)
.measure tran delay trig v(vin) val=1 rise=1 targ v(m8) val=2 rise=1
.power v5
.tran 1n 1u
.end
.end
```

Fig. 20: Final Net list commands

In the Net list commands .lib command indicates the location of library file in our system which represents the technology used to draw the schematic. Here, the technology we used is 180nm technology.

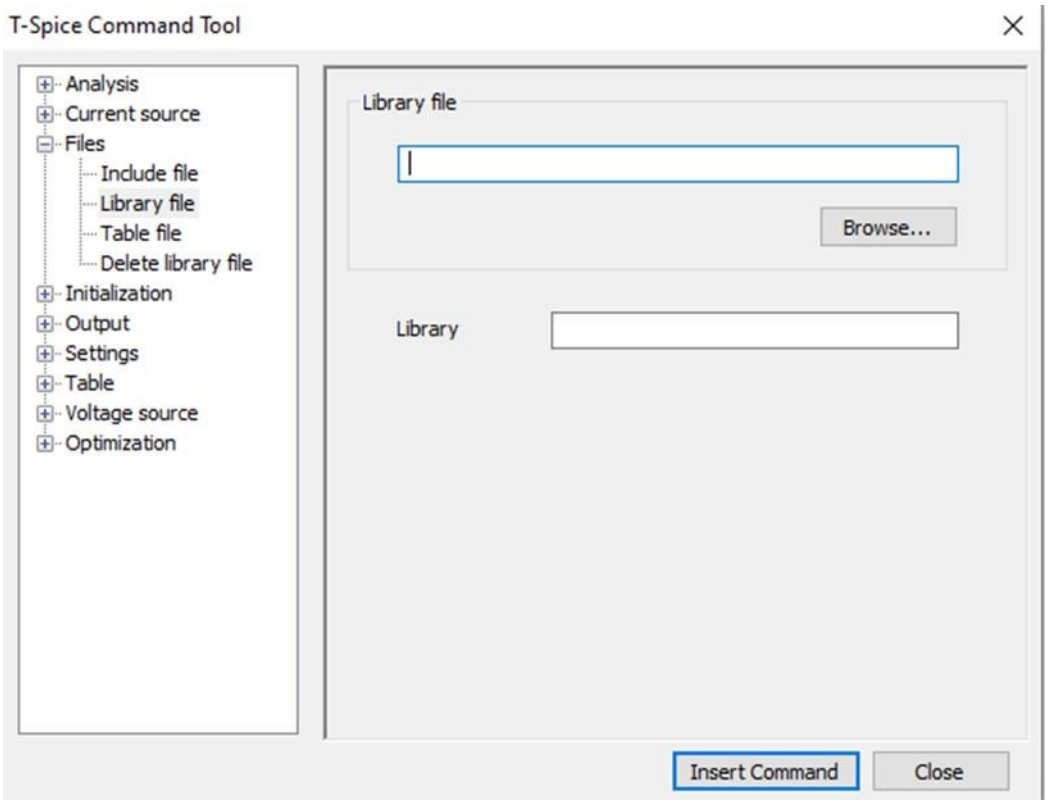

Fig.21: Window to add Library file

Here, we have to browse the location of library file in our system and need to click on Insert command then automatically that particular .lib command is inserted in T-spice file.

There are many types of voltage sources such as BIT, Constant, Pulse and so on. We mostly prefer to use Bit, Constant, Pulse and Sinusoidal types of voltage supply.

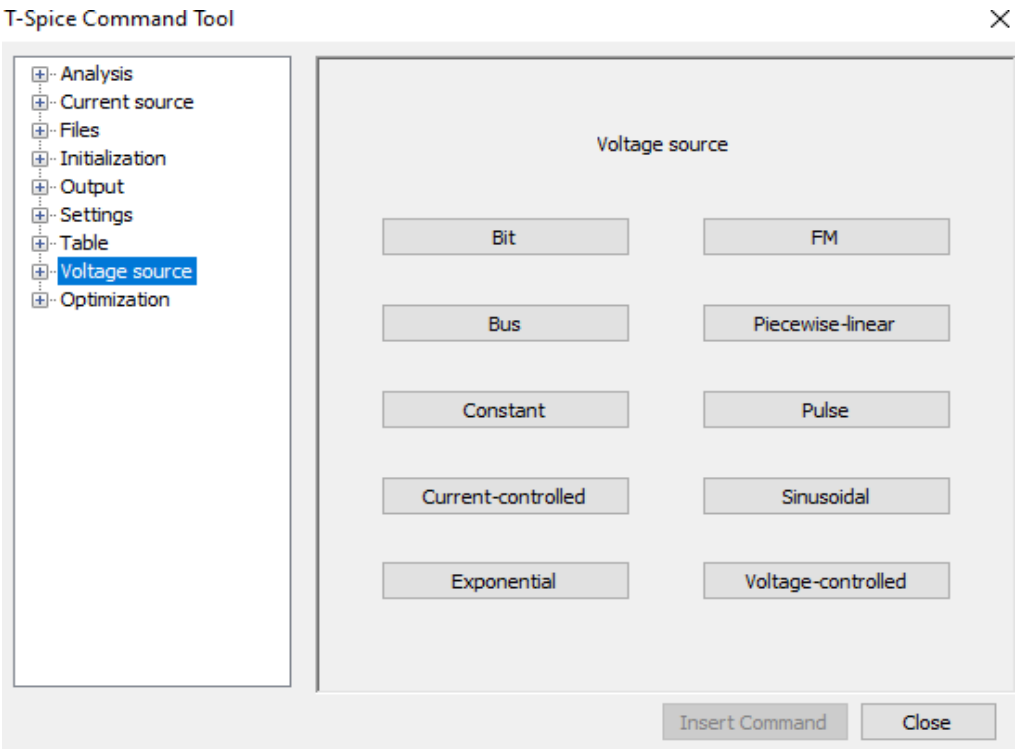

Fig.22: Window displays the types of voltage sources

Two Voltage sources provided as input, one is constant voltage and the other is the BIT type of voltage.

The syntax of voltage source for constant supply is as shown:

Syntax for constant type of voltage:

[Voltage source name] [+ve pin connection] [-ve pin connection] [Value]

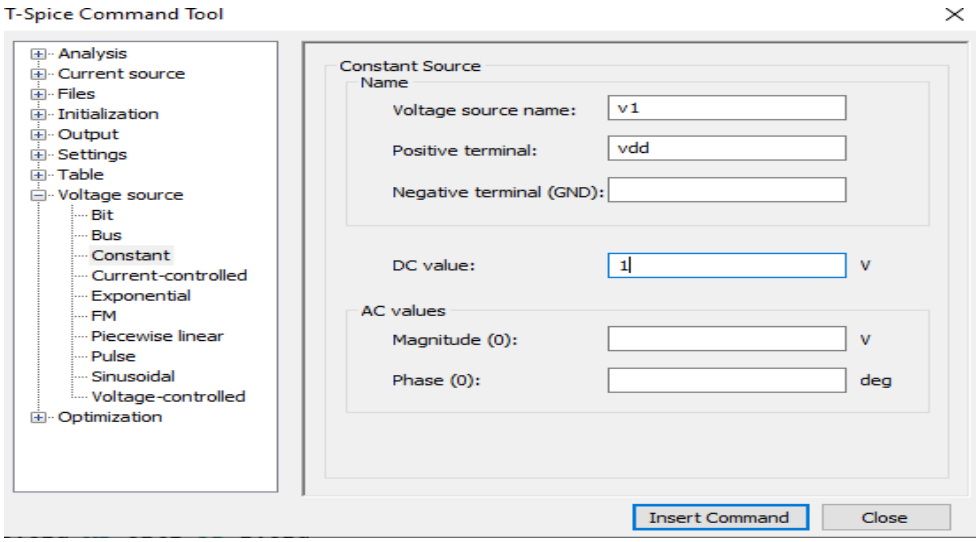

Fig.23: Screen displays the insertion of values for constant type source

From the above syntax, the voltage source name will be an indication for us to notify, we can name it as v1, b1 ... etc., anything we can mention as per our convenience. As we know that, Voltage source has two connections, one is positive and the other is negative. The positive pin connection represent to which port it is linked to. For suppose, the positive pin is connected to Vdd (symbol) then we can mention Vdd or if it is connected to some input say A, then we have to mention A. The negative pin connection is almost connected to Ground. Therefore, it represents 0 or GND in the syntax. And finally, the value we have to mention should be a constant value. Let it be 5V.

Syntax for BIT or other type of voltage:

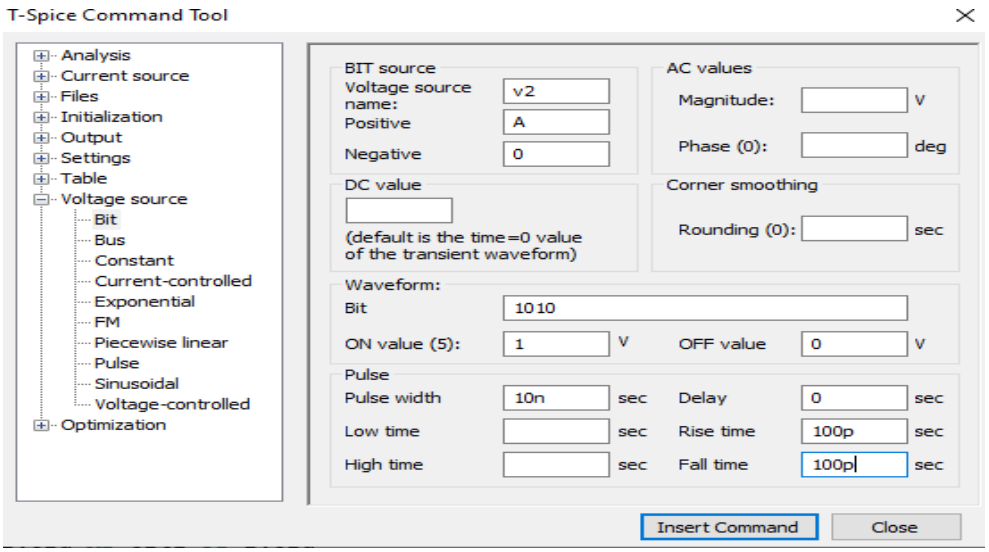

Fig.24: Window posturizes the values allotment for Bit type source

From the above fig, we can avoid the mentioning of values for Pulse Width, Rise time, fall time, Delay time, on value and off value. Then the syntax will be shown as mentioned below.

[V_name] [+ve pin] [-ve pin] [Type] [(Input values or pattern)]

For the syntax of Type of voltage, additionally, we have to mention what type of voltage we will provide and the input values or pattern representations are different for different types of voltage sources. For an instance, considering the Bit type of voltage, it consists of Bit pattern, on & off condition voltage values. For Pulse, it consists of Initial voltage level, Peak voltage level, delay, rise time, fall time, pulse width and Period.

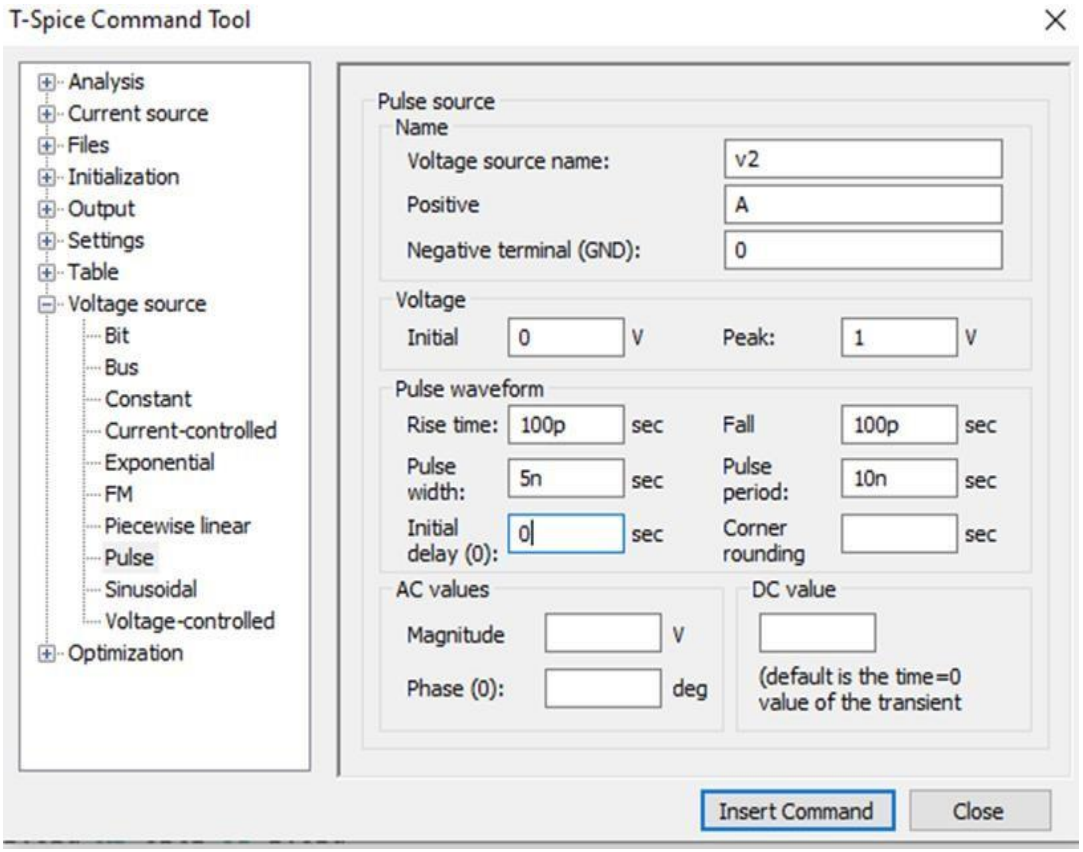

Fig.25: Window displays the values provided for the Pulse type of Source.

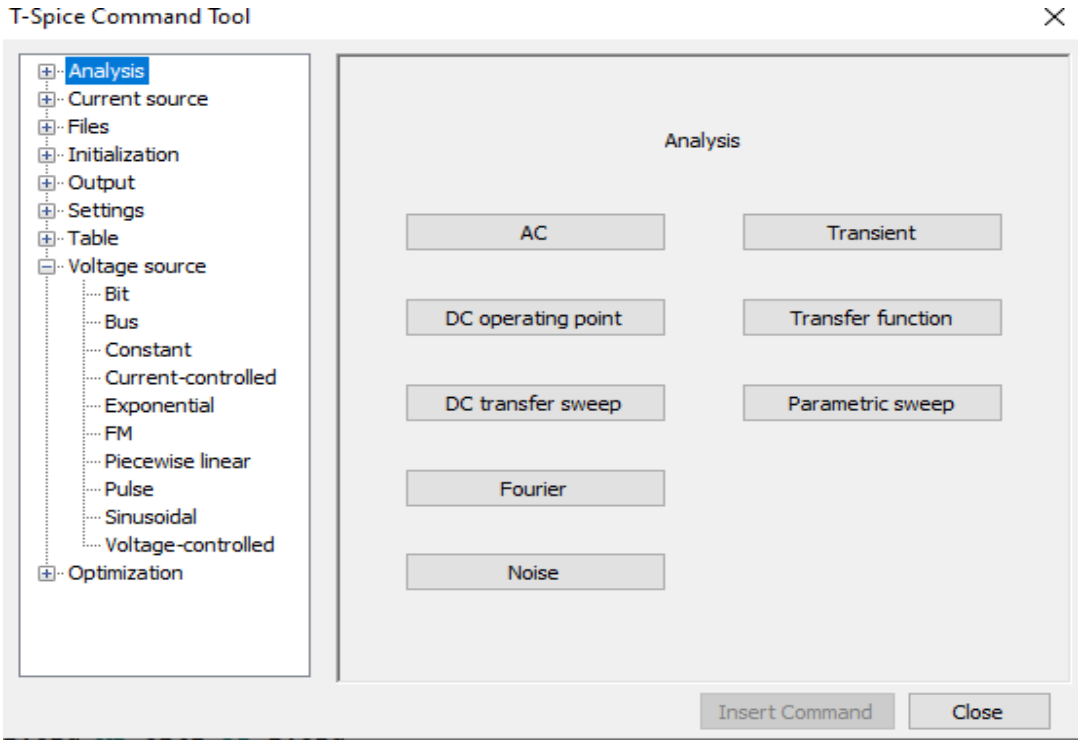

Fig.26: Window shares the screen for different types of Analysis

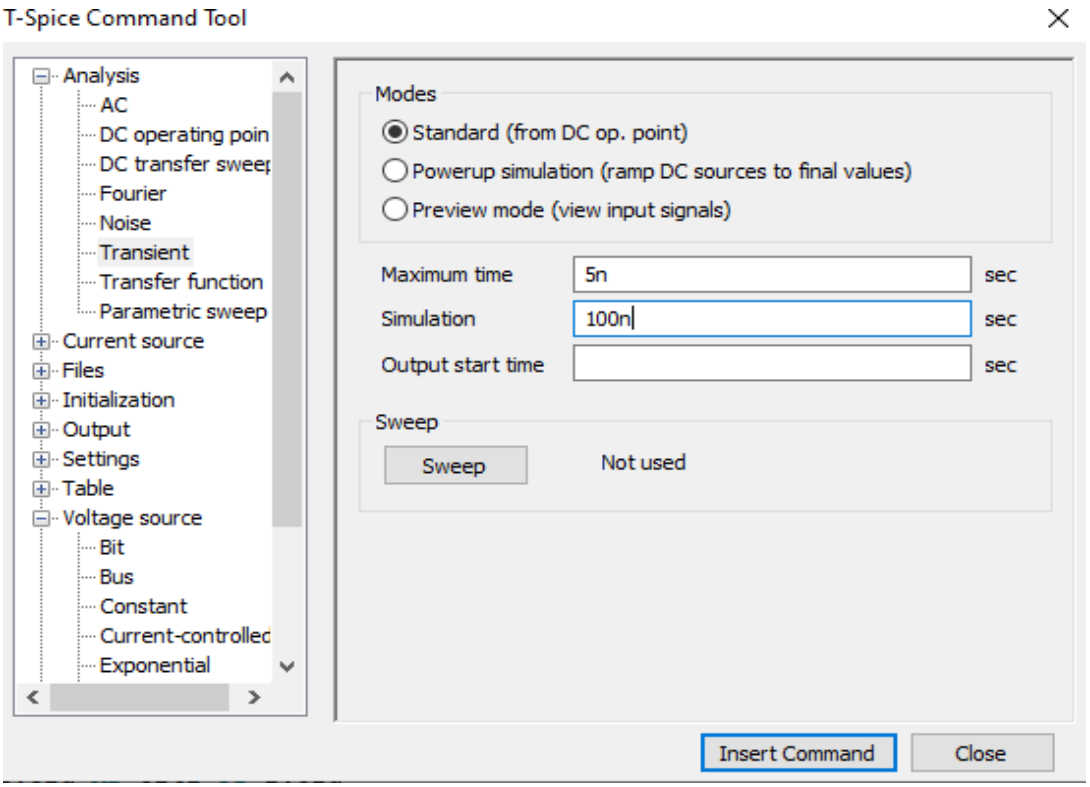

Fig.27: Window displays the command for Transient Analysis

Here .tran command relates to the type of analysis. .print command relates to the output. And .power command is used to measure power. There are few ways to calculate power. One is to calculate the power from Vdd source and directly get the average power value. The other is to calculate the power from many sources such as Vdd, Input ports and so on, then we have to calculate the average power consumed from all individual average power values of each source.

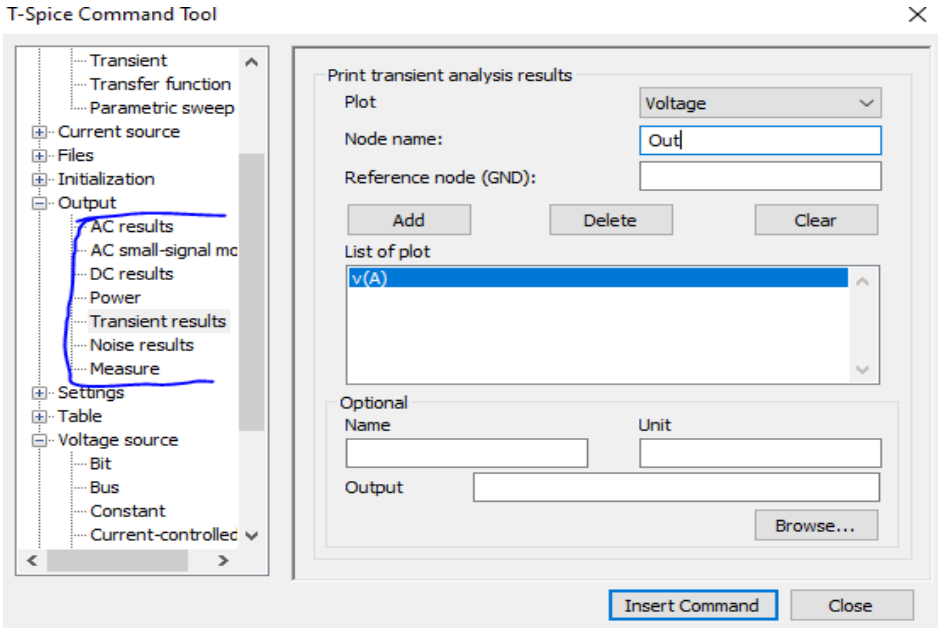

Fig.28: Procedure to print transient results

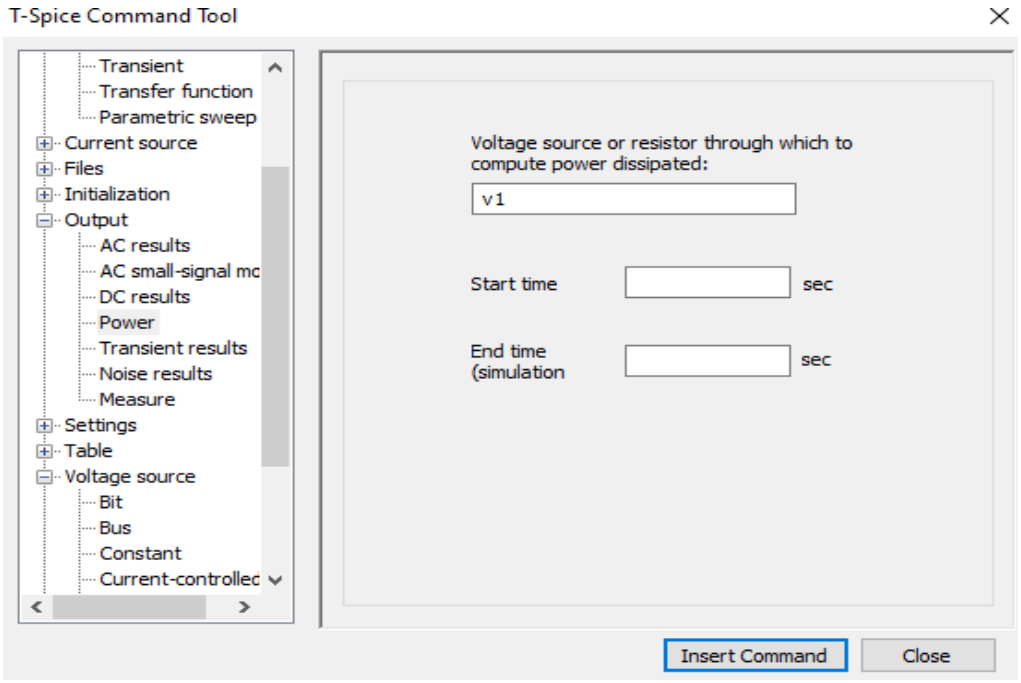

Fig.29: Procedure to Calculate Output Power

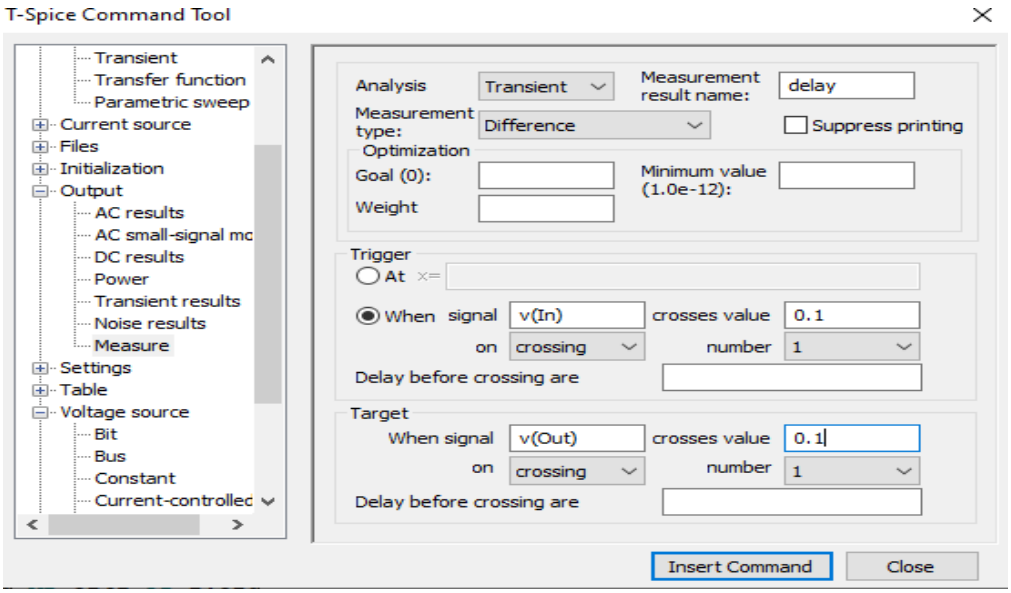

Fig.30: Values provided to measure delay

Here also mentioned .measure command which is applied to calculate delay measured between input & output. From the observation of syntax for delay measurement, we can say that tran represents type of analysis, delay represents the name of measuring quantity, trig represents the input source v(In) indicates the input value val represents the value of voltage, rise/fall represents the number of rise/fall of input signal and targ represents targeting value, v(out) represents the output signal, val represents the value of output voltage, rise/fall represents the number of rise/fall of output signal.

Then, in the upper left corner, click the run icon. Pre-layout inverter simulation output.

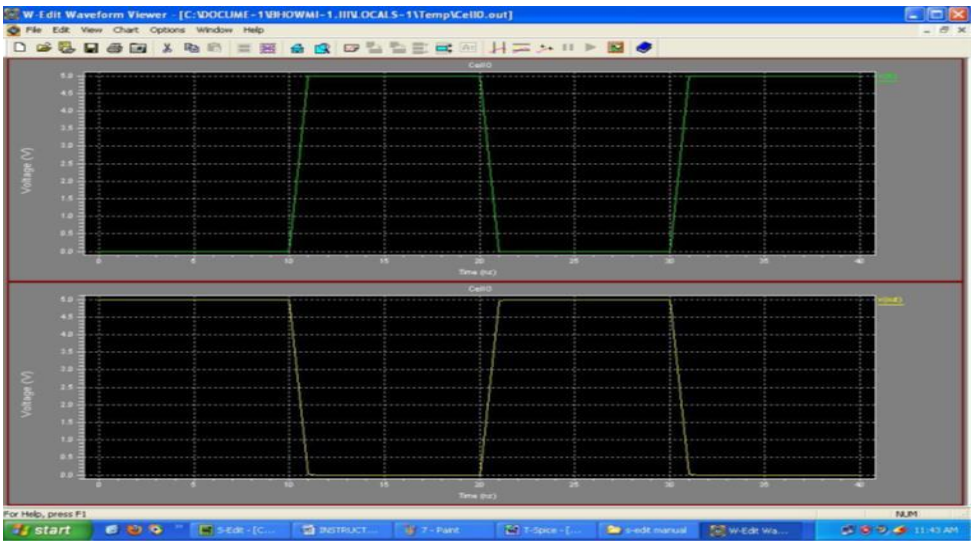

Fig. 31: Output waveform appears in W-edit

In W-edit window, there is an expand chart icon in the tool. This is used to split the output waveforms. Observe the waveforms and then close the waveform window as well as W-edit window.

There will be the finished status which is high-lighted in blue color.

After that, give a Right click on the finished line and there we will get the results of parameters generated by the net-list. Then an Output window will opened. As we know that, Area is nothing but the count of MOSFETs. In Tanner EDA, the power calculated would be Average power consumed during the simulation time. And the delay measured is the difference between the triggering and targeting destinations of the particular signals provided in the delay command line.

```
Device and node counts:
          MOSFETs - 632
```

Fig.32: Area

```
Power Results
v5 from time 0 to 1e-006
Average power consumed -> 7.132766e-003 watts
```

Fig.33: Average power consumed

```
delay = 2.0062e-009
   Trigger = 1.6667e-007
   Target  = 1.6867e-007
```

Fig.34: Delay measured

6.2 Project Results:

In this paper, the proposed circuits are Modified TIQ comparator, Modified MUX based encoder and implementation of Flash ADC. Here the entire design is simulated using Tanner EDA software by employing 180nm technology file. The schematic designs and waveforms for particular schematic is mentioned below. And finally, a comparison table for both existing as well as proposed works is also listed below in terms of Power dissipation, Area and Delay.

6.2.1 Modified TIQ Comparator:

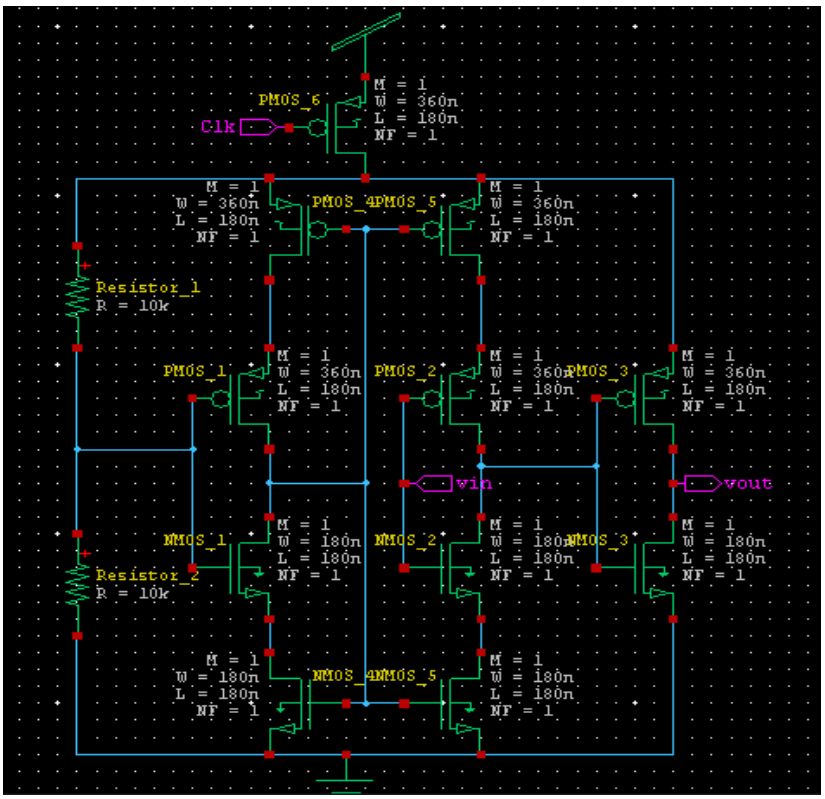

Fig.35: Schematic of proposed TIQ Comparator.

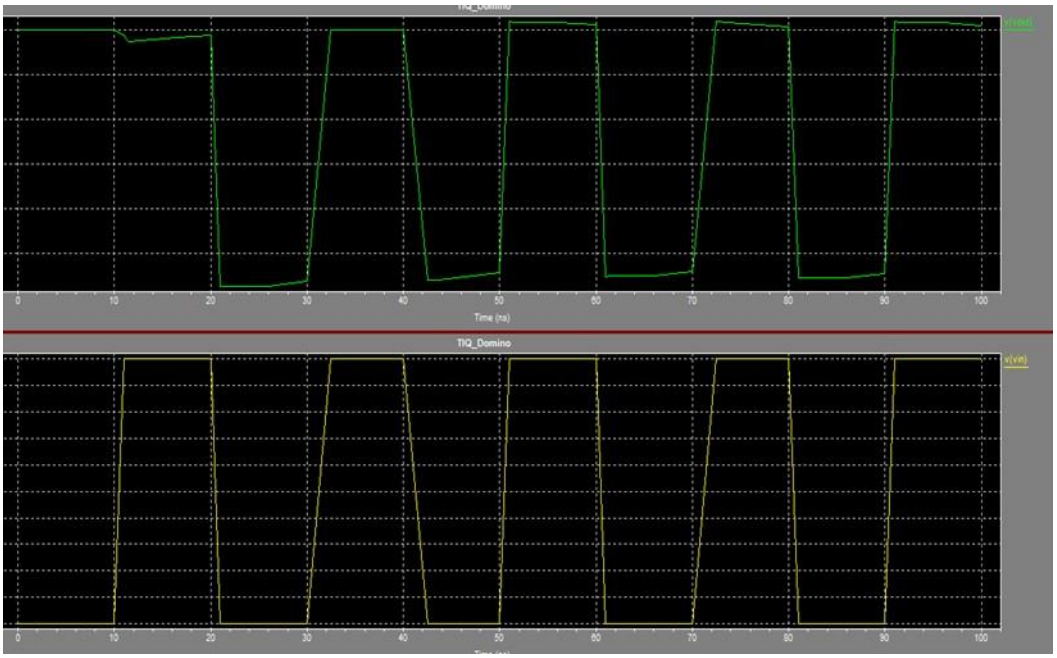

Fig.36: Waveforms for proposed TIQ comparator

6.2.2 Modified MUX based Encoder:

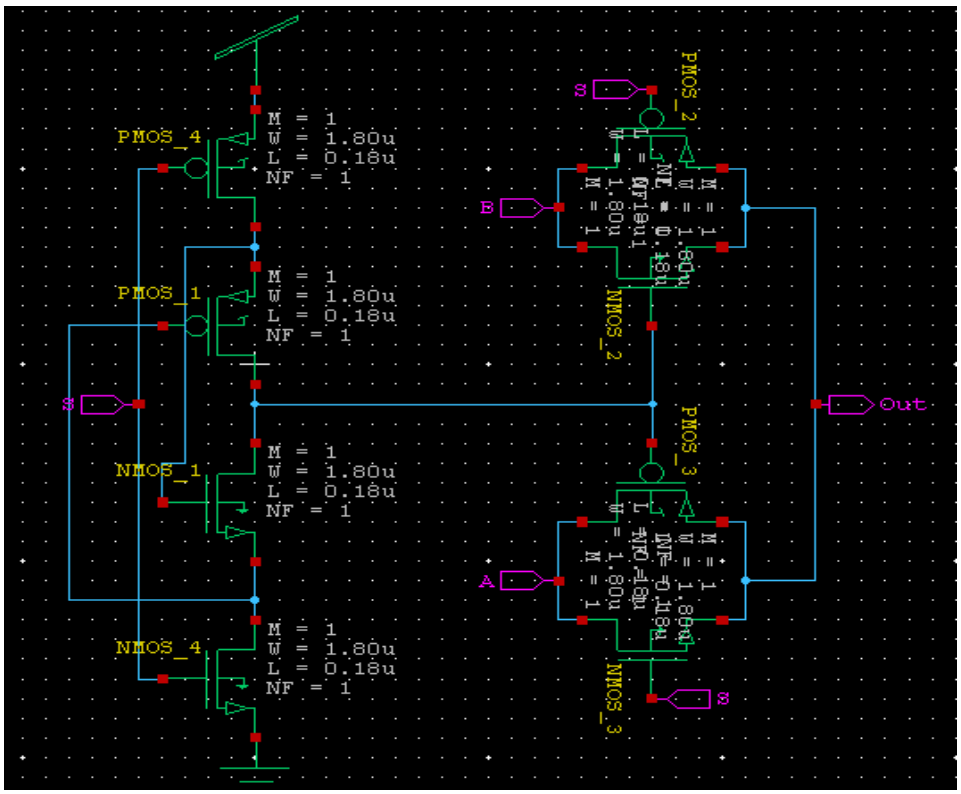

Fig.37: Schematic of MUX using TG adopting Lector Approach

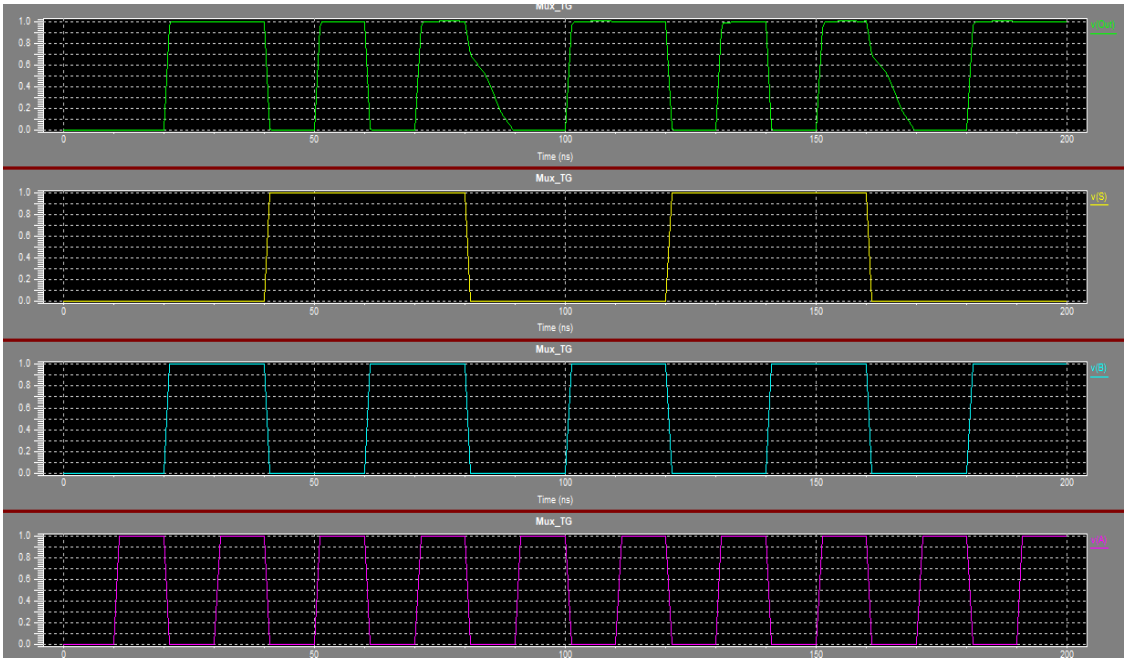

Fig.38: Waveforms for the schematic of MUX

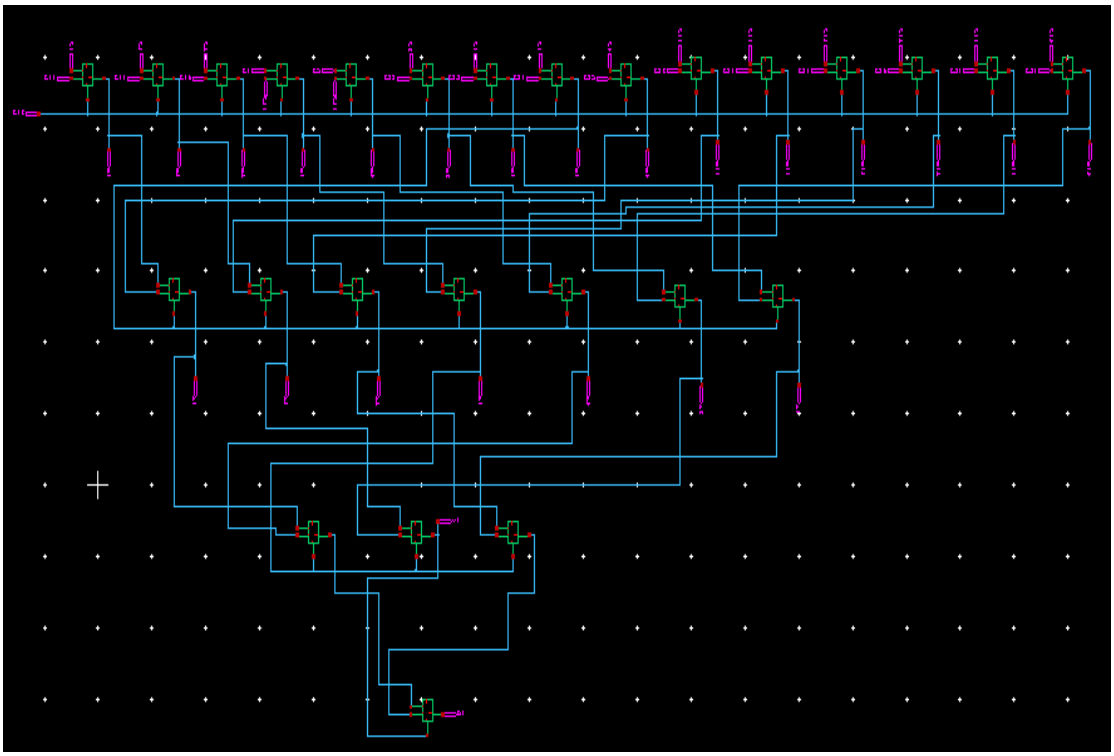

Fig.39: Schematic of Mux based encoder

6.2.3 Proposed Flash ADC

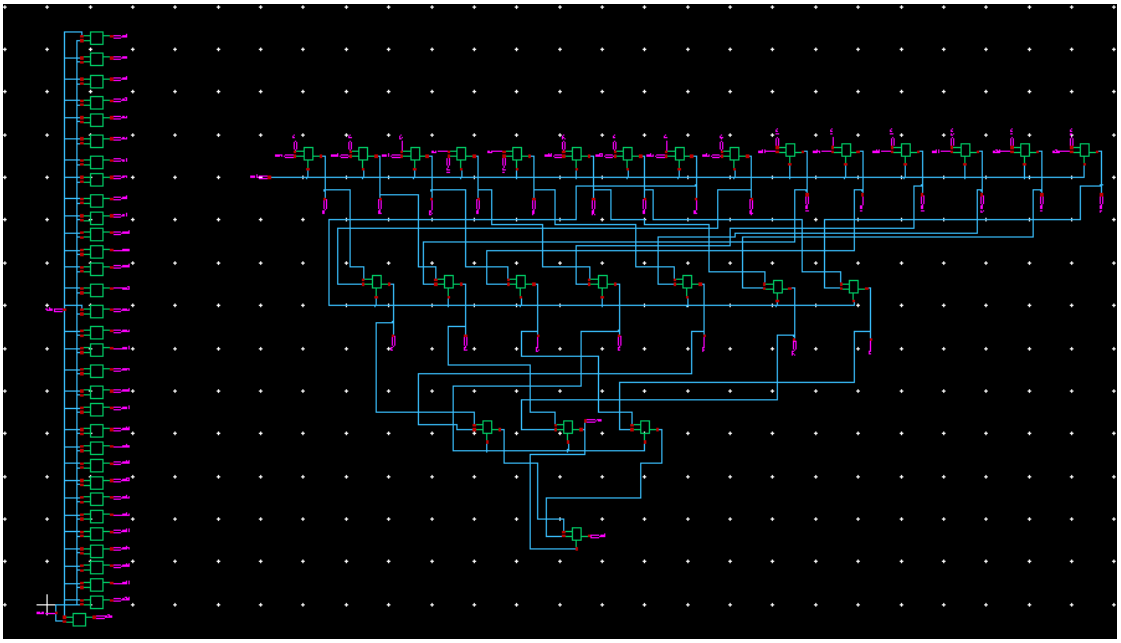

Fig.40: Schematic of Proposed Flash ADC

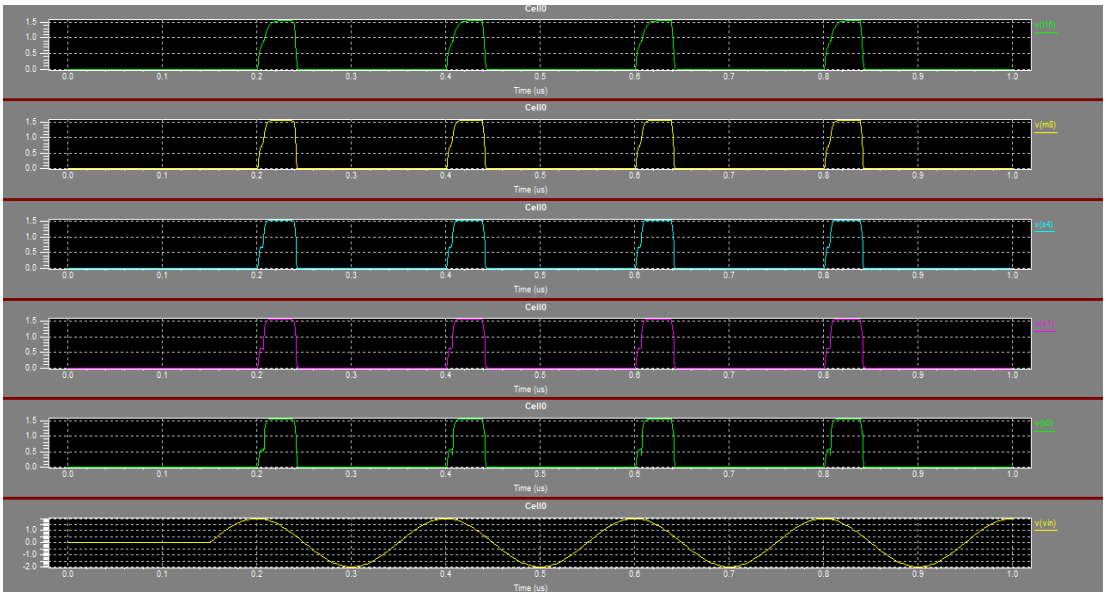

Fig.41: Output Waveforms for Flash ADC

6.2.4 Comparison between existing and proposed methods

	Area	Power	Delay
Existing	632	7.1327mw	2.0062ns
Proposed	560	2.639mw	36.29ns

Table-1: Comparison of Performance parameters among existing & proposed work

Table-1 mention the comparisons of Area, Delay and Power among Existing TIQ Flash ADC as well as Modified Flash ADC. From the observations of simulation results, we can conclude that Area as well as Power consumed is better in Proposed Flash ADC contrasted to Existing work.

CHAPTER 7

CONCLUSIONS AND FUTURE SCOPE

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7.1 Conclusion

In this thesis work, Flash A/D Converter using modified Threshold Inverted Quantizer comparator and Mux oriented encoder protocol is designed. It is simulated using T-spice simulation by employing 180nm Technology file. Here individual systems are interfaced to design a Flash ADC which are TIQ comparator as well Mux based encoder in TG logic adopting Lector approach. There are also having individual applications for TIQ comparator as well as Mux based encoder. These two modified systems which will provide better results interfaced for the implementation of flash ADC to achieve better resolution and outputs along with performance parameter evaluation.

A 5 bit flash Analog to Digital Converter is modelled using an array of 32 TIQ comparators and a threshold compensation technique. To reset the threshold level of voltage for each comparator in the array, depend on the magnitude of resistances R0 or R1 individually or else both simultaneously. To evaluate the reliance of inverter threshold level of voltage on the tunable resistor, a parametric sweep is performed on the magnitude of the resistance (whether R0 as well as R1) in the range of approximately 1 k to 100 M.

As a proof of concept, a 5-bit flash Analog to Digital Converter is modelled using threshold adjusted TIQ comparators. A MUX oriented encoder for thermometer data to binary transition is also modelled.

The encoder will then be used to change the 32-bit thermometer code from the Threshold Inverted Quantizer array result to binary code. This is carried out in two phases by the encoder in this Analog to digital converter. The 32-bit thermometer data is initially transformed to 5-bit grayscale data during the primary level. The 5-bit Gray formatted data is translated into 5-bit binary format which used a typical conversion circuitry comprising two inputting XOR operation.

The overall circuit latency is one of the most critical elements in determining Analog to digital converter effectiveness. The encoder circuit's latency was geometrically computed and was found to be in the tens of nanoseconds range.

A flash ADC with self-generated reference voltage is shown that can be built in a typical CMOS technology and offers stable performance over a wide temperature range. The circuit has been evaluated for static and dynamic efficiency and has been shown to be stable over a wide range of temperatures (-20 to 120°C). The use of resistors, on the other hand, adds to the complexity of the operation, raising cheval expenses. As a result of this restriction, future work could include a new resistor-less or MOSFET-only architecture.

7.2 Future work:

To extend this work of Flash ADC, we can replace the TIQ comparator with Dynamic comparator, Two stage op-amp, Telescopic Op-amp, Magnitude comparator etc., And we can change the configurations of the comparators by switching P-type and N-type Mosfets in the schematic. And also further we can also apply any Low power techniques for that work such as Power Gating, Transistor Stacking, Multi-Threshold Technique, Lector approach. We can also modify the TIQ comparator by inserting current limiters in order to reduce power consumption. There may also be possible to change the configuration of MUX used for encoder design. We can design MUX based on GDI Logic & Domino Logic. It is also possible to do voltage scaling and body biasing of transistors. There is also possibility to design the flash ADC using sample and hold circuit and also we can employ discrete comparator.

Either by changing the configurations of comparator as well as MUX or by modifying those designs by adopting any low power techniques. We can achieve better results in terms of performance parameters such as Area, Power and Delay. We can also optimize the flash ADC structure using Low technology files and also by changing the W/L ratios of the Mosfets.

From the observations of individual performance of different types of comparators and encoders in terms of latency, transistor count and power dissipation. The architecture of flash ADC is built using power efficient comparator and fast performance encoder. We can also design Flash ADC based on Low technology files such as 22nm, 16nm to attain better chip area and fast performance in the following decades.

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