DESIGN AND ANALYSIS OF MODIFIED VOLTAGE BASED SENSE AMPLIFIER FOR LOW POWER APPLICATION

A DISSERTATION REPORT

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SUBMITTED BY:

DIVYA

2K20/VLS/04

UNDER THE SUPERVISION OF

Dr. POORNIMA MITTAL

PROFESSOR

ELECTRONICS & COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

MAY 2022

ELECTRONICS & COMMUNICATION

ENGINEERING

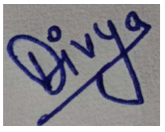
DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, Divya, Roll No. 2K20/VLS/04 student of M. Tech (VLSI & Embedded systems), hereby declare that the project Dissertation titled **"Design and Analysis of Modified Voltage Based Sense Amplifier For Low Power Application"** which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillmentof the requirement for the award of the degree of Master of Technology is unique and has not been copied without proper citation. This work has never before been used to give a degree, diploma associateship, fellowship, or other equivalent title or recognition.



Place: Delhi Divya

Date: May 24, 2022

ELECTRONICS & COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(Formerly Delhi College of Engineering)

Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled **"Design and Analysis of Modified Voltage Based Sense Amplifier For Low Power Application"** which is submitted by **Divya, 2K20/VLS/04**, to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the prerequisite for the award of the degree of Master of Technology, is a documentation of the student's project work completed under my supervision. To the best of my knowledge, this work has never been submitted in part or in full for any degree or diploma at this university or anywhere else.

Place: Delhi

Date**:** May 24, 2022,

Prof. Poornima Mittal

Supervisor

Professor

Department of ECE, DTU

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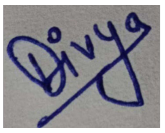


Divya

2K20/VLS/04

MTech: VLSI Design and Embedded System

(2020-2022)

ABSTRACT

In memories and peripheral circuits, the sense amplifier has taken center stage. Longer battery life has become a major challenge for high-speed memories as the need for portable devices grows. In the age of digital technology and VLSI circuitry. SRAM, or static random-access memory, is critical for low-power and high-speed performance. CMOS memory contain sense amplifiers (SA). The saved information is read using SA. Because the sensing amplifier (SA) is a critical component of the read circuitry for both volatile and non-volatile memories, like as FLASH, their performance has a substantial impact on memory performance. The four key performance parameters of SA are access time, energy, power, and area. This thesis describes a sense amplifier with a modified design that includes a dual-voltage dual-tail level restoration voltage latch sense amplifier (DVDTLR-VLSA). The sensing amplifier (SA) is a fundamental component of SRAM and memory systems. In the publications, the voltage mode sense amplifier (VMSA) is found to perform better than the current mode sense amplifier. Many designs have been offered in the literature, each with its own set of benefits. The standard 6T SRAM serves a critical role in cross coupled sense amplifiers. The voltage variations that must be measured are provided by SA.

The major classifications of SA have been discussed and compared in this thesis, with the best of the two being explored and explained in sub parts. There have been eight various varieties of VMSA researched, studied, and simulated. All these SAs are differential and cross-coupled SRAM-based SAs. The basic forms of SA structures are the first four differential SAs, while the advanced cross coupled topology of SA is the final four differential SAs. Current, Power, Energy, Transistor Count, and Delay are important SA characteristics that describe the overall performance of SA. On the LT spice simulator, all sense amplifier structures were simulated on the 180 nm technology node and then compared based on parameter and topology.

Sense Amplifiers are broadly used in the periphery of Static Random Access Memory (SRAM). Sense amplifiers (SA) are used to fulfills the demand of high speed and low power and act on access time. In this thesis a modified improved Double switch level restoration access transistor sense amplifier (DVDTLR-VLSA) is reported. The design has been simulated in 180 nm technology node with 1.8V operative voltage. The results

of DSLRA-SA are compared with most known sense amplifier topologies based on power, energy, delay, and current parameters in which DVDTLR-VLSA performing admirable. The improved SA is found suitable after examining all the analysis, The design takes a very small amount of power and energy while also improving delay. This thesis excellently finds perfect solution that prove more superior for low power CMOS SRAM.

Finally, the performance of DVDTLR-VLSA is superior to that of all other SA topologies. A modified sense amplifier design has been reported based on this assertion, which includes a level restoration circuit (LRC) approach, dual switch (sleep transistors), feedback inverter, and access transistors coupled to bit lines. A modified design is studied and simulated at the 180 nm technology node and compared to current SA in the literature to determine its workability. Propagation delay, power, PDP, and current are the four main parameters that are calculated. The performance of DVDTLR-VLSA is noticeably superior. When compared to a typical cross coupled voltage latch SA (CCVLSA), the enhanced circuit uses half the power. Energy and delay results are also improved. Various analysis such as Dimensional analysis, Temperature analysis and effect of sleep transistors are done for improved SA to examine the performance. A modified cell with sleep transistors has least power, delay and energy and have better.

CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

S. No.	Abbreviation	Full Name
1.	BDSA	Basic Differential Sense Amplifier
2.	BL	Bit Line
3.	BLB	Bit Line Bar
4.	CCLSA	Cross Coupled Latched Sense Amplifier
5.	CCVLSA	Conventional Cross Coupled Voltage Latch Sense Amplifier
6.	CLVMSA	Current Latched Based Voltage Mode Sense Amplifier
7.	CMSA	Current Mode Sense Amplifier
8.	DSCVMSA	Double Switch Cross Coupled Voltage Mode Sense Amplifier
9.	DSTGVMSA	Double Switch transmission Gate Voltage Mode SA
10.	DTGVSA	Dual Switch Transmission Gate Voltage Latch Sense Amplifier
11.	DVDTLRVLSA	Dual-Voltage Dual-Tail Level Restoration Voltage Latch Sense Amplifier
12.	E	Energy
13.	EN	Enable
14.	HSVSA	High Speed Voltage Sense Amplifier
15.	IC	Integrated Circuit
16.	LRC	Level Restoration Circuit
17.	P	Power

18.	SA	Sense Amplifier
19.	SRAM	Static Random Access Memory
20.	TGVLSA	Transmission Gate Voltage Latch Sense Amplifier
21.	VMSA	Voltage Mode Sense Amplifier
22.	VLSI	Very Large-Scale Integration
23.	WL	Word Line

CHAPTER 1

INTRODUCTION

In modern memory circuits, the interest in sense amplifiers has been raised due to the growing concern about low power and high-speed concerns in current memory circuits, and the interest in sense amplifiers has increased. Faster memory is embedded in static random-access memory (SRAM or Static RAM). Data is kept when power is applied and lost when power is disconnected. The system on Chips (SOCs) has SRAMs built in. SRAMs are commonly utilized in latch and cache circuits. The cache is a term used to describe an array of SRAM bit cells. The major problem of SRAM circuits is the engagement between the write and read equilibrium. As suggested in the works of literature, the cell ratio should be enough significant to permit the read access aside from changing the data. Power, area, and other components of enhanced SRAM bit cells. Low power, area, and delay demand is increasing day by day, which is largely dependent on SA.

The primary function of SA is to read the contents of CMOS memory and to detect information stored in bit cells. The speed and power of SA can be reduced by using high speed, lower delay, and low power techniques such as adiabatic logic and VTCMOS, etc. one of the known techniques for better consequences are used in this thesis is the level restoration circuit (LRC) technique or a level shifter. It is the combination of PMOS latch transistors point to output. LRCs are used between I/O and core circuits, they are also an important part of the multi-voltage circuit. Another aspect of SRAM bit cells and SAs are small areas with high speed and low power. So, to design a SA with the lowest transistor for a small area used is a real challenge. For reducing power and propagation delay, the bit lines voltage swing should be lower than the supply voltage. One more feature that influences the operative results concerning the order of voltage levels is the aspect ratio. The aspect ratio of PMOS and NMOS transistors of SA should be conventional and correct. This dimensional analysis has been done for several decades for actual pull-up and cell ratio. The analysis is examined in supplanting section of this thesis.

There is a different classification of SA in the literature such as single-ended SA, double-ended SA, voltage mode, charge transfer, current mode, latch type SA, etc. Among all SAs, Cross coupled voltage mode SA (VMSA) is best. The reason for the choice of cross coupled latch SA due to there is no static current passed through it and is

used to identify bit line voltage differences during a read operation. So, the design and analyses with proper circuit operation and output of best performing VMSA for SRAM is a provocation for low power application. The main parameters for best design considerations are power, area, speed, aspect ratio, transistor count, etc. generally, for lesser area requirements, a smaller number of transistors are used in the cell. For this, the effect of sleep transistors has been examined while removing or adding head and foot switch sleep transistors. The above-mentioned parameters may affect the occupied area of the SA and the SA with low power, energy, and area with high speed can be considered the best performing SA.

In this work, an LRC-based double switch level restoration access transistor sense amplifier (DVDTLR-VLSA) is reported. The design is made based on a single supply circuit. LRCs provide the required short circuit dissipation positive feedback network. also, the performance of DVDTLR-VLSA is compared with well-known existing SAS.

1.1 Motivation

Nowadays, the requirements for digital systems and electronic appliances increasing, and electronic circuits have appropriate memory. Among whole memory circuits present in the very-large-scale integration (VLSI) industry, CMOS memories are the most known due to their authentication. where power consumption is the main concern in each field. Low-power, high-speed, high-area and high-energy utilization are all priorities. The sensing amplifier block is primarily responsible for memory speed. The sensing amplifier oversees accessing the memory and turning bit line voltage variations into output data. Sensing techniques for memory have undergone extensive development, resulting in memory that is small, quick, low-power, and efficient. Due to the demand for these durable and portable gadgets in everyday life, the evolution of low-voltage, low-power technologies are critical today. As a result, a great deal of research is focused on this area, which can be accomplished by reducing feature size, modifying existing topologies, lowering power supply voltage, and so on. Therefore, in today’s modern technologies, low-power and high-speed design techniques are desirable.

A SRAM is a fundamental of sense amplifier. A SA is an active analog cell which lowers the time it takes for a signal to travel from an accessed memory cell to the logic circuit at the array's edge. It's used to detect minor variations on memory bit lines and generate large voltage swings. SA’s are critical to the memory circuit's functioning, performance, and durability. The use of a sensing amplifier in memory circuits allows for

a reduction in delay and power. The developed sense amplifier should be industry standard and capable of supporting conventional SRAM designs without negatively impacting other SRAM appliances.

This thesis follows the pattern by presenting a low-power level restoration circuit technology-based sense amplifier with high speed and increasing energy with low power supply. The SA is made up of an optimized modified structure that leads to better performance.

1.2 Objective

An in-depth assessment of information makes room for new questions, ideas, and understandings to emerge. The primary goal of research is to uncover new possibilities by exploring the unexplored.

Primary objectives of this research project are as follows:

- To Compare multiple Sense amplifier designs for the same technology nodes, power supply, and transient time. This is also helped to determine the trend of SA being used for low-power applications.
- To understand the working of sense amplifiers and which ones perform the best, a comparison is done between existing SA structures and modified SA structure. For PDP analysis, a mathematical calculation is also performed. To establish which circuit had the best performance, SAs are compared, and their findings are tabulated.
- To design and analyze a modified sense amplifier structure that includes a back-to-back inverter, dual switch, and level restoration. For optimal performance, temperature analysis, dimensions analysis, and the influence of sleep transistor analysis are all performed.

The emphasis of this research is to create a up-to-date better sense amplifier structure that uses low-energy and low-power components and may be used in low-power applications. Multiple sense amplifier topologies on the same technology node, with the same aspect ratios and transient times, were compared for this. Then, for the best performance, the existing SA design is compared to the changed SA design. The new design is examined. Bit-lines display significant capacitance and are speedier since modern memory systems.

1.3 Methodology:

Comparative performance of the two basic Classifications of SA structure named Voltage Mode SA and Current Mode SA is verified over the same technology and aspect ratios. Thereafter, out of two the best SA is further studied with its different topologies and analyzed the performance based on different parameters such as power, energy, current, and delay. After this, a modified design is implemented and analyzed with several analyses. The updated SA design has 10 transistors, five PMOS and five NMOS, and is divided into three stages: access transistors, driver transistors, and load transistors, as well as two PMOS latch transistors connected to Vdd and two sleep transistors. The LRC approach was used to modify the design. This thesis focuses into the standard sense amplifier structures. In addition, the structure of a modified sense amplifier known as the "Dual-Voltage Dual-Tail Level Restoration Voltage Latch Sense Amplifier" is presented, and it is reported that the LRC approach take part in an important function in the effectiveness of the sense amplifier. As a result, the changed structure offers the best performance. A variety of sense amplifier parameters have also been defined and researched.

1.4 Thesis Organization:

This thesis is divided into six chapters. A sense amplifier is defined in Chapter 1 as an introduction to the sense amplifier. The motivation, objective, approach, and thesis organization are also included in Chapter 1. The literature review and the technology gap are discussed in Chapter 2. The third chapter examines a significant classification of sense amplifiers as well as assessments of the best-classified sense amplifiers. Chapter 4 examines four advanced sense amplifier architectures, as well as their parameters and performance. Chapter 5 depicts the redesigned sense amplifier design, its analysis, and many performance analyses. The conclusion and future scope are presented in Chapter 6.

- CHAPTER 1- Provides a basic overview of SRAM and sense amplifiers, as well as how they operate at low power and low voltage. This chapter discusses the thesis's objective, motivation, methodology, and thesis organization.
- CHAPTER 2- The prior research on SRAM and sense amplifier was detailed in this chapter. According to published work, power dissipation and PDP are slightly higher. In the literature, various types of SA topologies have been reported. Negative-positive feedback, LRC, dual switch, transmission gate, and

other approaches and devices have all been utilized in SA to improve its performance.

- CHAPTER 3- This chapter covers the two most common SA classifications, as well as their functionality, operation, and parameters. The best of two major classification systems is investigated further. We looked at the four existing VMSA topologies. At 180nm technology nodes and 1.8V supply, all four SA were examined. Then, depending on their structures, their parameters were compared.
- CHAPTER 4- This chapter covers the description and parametric analysis of 6T SRAM-based advanced cross couplings SA. Simulations and calculations are used to examine the metric extraction of these circuits.
- CHAPTER 5- This chapter illustrates the modified design. This chapter describes the design, how it works, and compares the previously reported SA from Chapter 4 with a modified design to demonstrate the higher action of the modified designed sense amplifier. For the modified SA design, major factors such as PDP, propagation delay, power dissipation are determined. For the best performance of the improved SA, numerous analyses were performed, including the effect of sleep transistors, dimensional analysis, and temperature analysis.
- CHAPTER 6- This chapter contains the important outcomes of every chapter along with the future work.

Finally, the list of publications contingent to the work carried out in this thesis is attached. Afterword, the detailed list of references is presented which is used to refer and site the previous research work to explore the directions for our present work.

CHAPTER 2

LITERATURE REVIEW

Reviewing the reported work is always necessary. The aim of a literature review is to: Establish a foundation of knowledge about the topic. Identify areas of previous expertise to minimize repetition and to give credit to other scholars. Recognize previous studies' contradictions, research gaps, main research conflicts, and unsolved concerns.
This chapter is categorized into two sections: (1) previous reported work, and (2) technical gaps.

2.1 PREVIOUS REPORTED WORK:

S. Yadav, N. Malik, A. Gupta, S. Rajput [1], Presented the design and analysis of Static Random-Access Memories (SRAMs) is presented, with a focus on minimizing delay and power consumption. Also, implemented the 6T SRAM cell which has a Read and write time, power consumption and delay have all been lowered. Bit-line parasitic capacitance increases as memory capacity grows, delaying voltage sensing. To prevent this problem, apply efficient scaling approaches and further improve design performance.

B. Rawat, P. Mittal [2], Proposed a seven-transistor static random-access memory (SRAM) bit cell with a single bit line architecture. Its performance is validated by Monte Carlo analysis and temperature variation analysis. When compared to other single-ended 5T, 6T, 7T, 8T, 9T, and 10T SRAM cells, the cell is proven to perform better. In comparison to the other cells, the ION/IOFF ratio is high since the leakage current is low.

A. K. Gundu, M. S. Hashmi, A. Grover [3], Proposed a latch type SA. Then a statistical study is performed to show that it outperforms the traditional latch type SA. In terms of offset voltage and sensing delay, the results imply that the suggested SA has the potential to compete with the standard latch type SA. The influence of driver transistor sizing on sensing delay was also examined.

M. R. Garg, A. Tonk [4], Describe the many types of voltage and current sensing amplifiers. The review goes discusses the working of sense amplifiers, as well as their benefits and drawbacks. It is also describing the size of Various transistors in sense amplifiers. The paper focuses on certain performance parameters that should be taken into account while developing sense amplifiers.

T. Kobayashi, K. Nogami, T Shirotori, Y. Fujimoto [5], Describe two new power-saving strategies for high-performance VLSIs with a large-scale memory and numerous interface signals. One is a current-controlled latch sense amplifier, which minimizes power consumption. In comparison to the traditional current-mirror sense amplifier, this sense amplifier reduces power without reducing access time. The other is a static power-saving input buffer (SPSIB), which lowers DC current in interface circuits with TTL high input levels.

R. Jain, K. Gupta, N. Pandey [6], Hybrid Dynamic Current Mode Logic with Modified Current Source is a low-power MOS Current Mode Logic (MCML) concept proposed in this study (H-MDyCML). The functionalities of circuits are accomplished utilizing complementary pass transistor logic, which helps to address the problem of multiple-level transistor stacking. improved power and delay are also presented.

B. Rawat, P. Mittal [7], A single bit line, seven-transistor static random-access memory (SRAM) bit cell was proposed. For temperatures, Monte Carlo analysis and temperature variation analysis support its performance. The performance of the cell is compared to that of other single-ended SRAM cells, and it is shown to be superior. The bit cell's power consumption is also determined to be minimal in all modes of operation.

H. Chun-Lung, H. Mean-Horn [8], This research produced a high-speed sensing amplifier that can be used in static random-access memory (SRAM) applications. The sense amplifier can be utilized in memory units, as a line receiver, and as a restoring element for small-swing logic. Simulated findings demonstrate that the suggested sense amplifier improves the speed of traditional sense amplifiers.

T. Na, S. H. Woo, J. Kim, H. Jeong, S. Jung [9], Depicts the detection of dead zones of the two most common latch-type SAs, voltage- and current-latched SAs, are examined in this brief. In terms of sensing delay, power consumption, and PDP, an appropriate latch-type SA technique is also provided for various SA input voltages. When a sense amplifier's input voltage difference exceeds the offset voltage, the SA identifies it correctly and outputs a large signal.

B. Mohammad, P. Dadabhoy, K. Lin, P. Basset [10], A complete study of the Voltage Latched Sense Amplifier (VLSA) and Current Latched Sense Amplifier (CLSA) design is presented. The results show the two sense amplifiers behave for two different design topologies: one for low power (LP) process technology designed for mobile low leakage applications, and the other for high performance (HP) applications. For active power,

leakage power, speed, and area, a detailed Spice simulation with statistical models and Monte Carlo simulations is used to compare the two systems. Our research reveals that VLSA outperforms CLSA.

A. Chrisanthopoulos, Y. Moisiadis, Y. Tsiatouhas, A. Arapoyanni [11], There is a comparison of different current mode sense amplifiers. The current sensing sense amplifiers under consideration are ideal for SRAM and flash non-volatile memory. The sensing delay time for various power supply voltages and bit-line capacitance values is simulated and the results are presented. The energy dissipated per sensing operation is also compared, as well as worst-case and high temperature scenarios.

N. Kumar, P. Mittal [12], In terms of latency, average power dissipation, and Power delay product, a comparison is done between FINFET based Gate Diffusion Input and Pass Transistor based 2:1 Multiplexers. The power dissipation of a GDI-based mux is relatively low. GDI-based Mux has superior performance and lower power consumption. Because multiplexers can be employed in a variety of combinational circuits, improving the performance of the multiplexer is increase the overall performance of the circuit.

E. Seevinck, P. J. V. Beers, H. Ontrio [13], Proposed a simple four-transistor current-sense amplifier. The circuit creates a virtual short circuit between the bit lines, lowering the sensing delay and making the bit-line capacitance practically irrelevant. Furthermore, the virtual short circuit assures that bit-line voltages are equal, removing the requirement for bit-line equalisation during read operations.

B. D. Yang, L. S. Kim [14], Proposed a low-power SRAM (HBLSA-SRAM). To lower both capacitance and write swing voltage of bit lines, it employs a hierarchical bit line composed of a bit line and sub-bit lines with local sensing amplifiers. The HBLSA-SRAM decreases write power consumption in bit lines without reducing noise margin by using a modest swing signal on the high capacitive bit line and a full swing signal on the low capacitive sub-bit line.

C. Kishore, A. Kumar [15], The delay and power measurements on transmission gate voltage mode sense amplifiers and voltage mode sense amplifiers are presented in this study. In comparison to VMSA, the proposed circuit is a transmission gate voltage mode sense amplifier (TGVMSA). When compared to TGVMSA and VMSA, the result exhibits less delay and power dissipation. The TGVMSA has a larger cell area, but its power dissipation and delay are reduced.

2.2 TECHNICAL GAP

There is a technical gap after observing and reviewing all the reported work. Most of the literature includes comparisons between SA classifications, Voltage, current, and charge transfer SA's are examples. However, the qualities of all these sense amplifiers differ, and in all the literature, voltage mode sense amplifiers seem to be the most effective. As a result, the comparison of voltage mode and current mode SA is examined in this thesis, and the results are reported. The best of the two is then studied further for the best results. Sense amplifiers are a broad field of research with numerous classifications and subcategories in the literature.

However, the goal of all research is aimed at achieving the performance requirements required for all vlsi circuits, namely speed, power, and area. As a result, the best categories are examined in this thesis based on these requirements. Cross coupled sense amplifiers are the optimum result of voltage mode sense amplifiers. Due to design difficulties, the described sense amplifiers in the literature had higher power dissipation. Additionally, some early reports of sense amplifiers have a longer delay and slower operation. Although, according to early accounts, the number of transistors is minimal. Furthermore, SA experiments presented in published literature demonstrate that they have lower accuracy, higher compliance voltage, and improper aspect ratios that cause problems in low power, low voltage applications. For proper aspect ratios dimensional analysis of modified SA has been done in this thesis.

CHAPTER 3

Characteristic Comparison for Different Voltage and Current Sense Amplifiers

A sense amplifier is an active circuit used to detect minor fluctuations on memory bit lines and produce full voltage swing by limiting the time it takes for a signal to travel from an accessed memory cell to the logic circuit at the array's edge. It translates the arbitrary logic levels on a bit line to the peripheral Boolean circuits' digital logic levels. Sense amplifiers, which are employed with memory cells, are critical components in determining CMOS memory performance and environmental tolerance. Sense amplifiers have grown in popularity because of their usefulness in memory designs. The developed sense amplifier should be standard and capable of supporting the present Static random-access memory (SRAM) design without influencing the other devices considerably. Understanding SRAM and its circuitry is required to develop the sense amplifier.

This chapter is organized in seven sections:

- The heart of the sense amplifier is an SRAM, which is defined in section 3.1.
- The working of a sense amplifier is outlined in part 3.2, and the major classifications of sense amplifiers are defined in section 3.3.
- The performance of the SA is examined in section 3.4. Differential sense amplifier topologies are discussed in section 3.5, and their performance is compared in section 3.6.
- considering these challenges, section 3.7 summarizes the conclusions of the chapter as well as the chapter's important outcomes.

3.1 Static Random Access Memory

SRAM (static random-access memory) is a volatile memory that operates at the same speed as logic circuits while consuming very little power in standby mode. SRAM is utilized to offer a high-speed link with central processing units or the CPU that is not possible with DRAM. As a result, a memory that consumes extremely little power and runs quickly is required [1]. This section is covering the SRAM, which is the most basic component of the SA. The heart of Sense Amplifier is SRAM (SA). Comparative examination of 6T SRAM based Cross coupled sense amplifiers is explored and simulated in this dissertation. To understand the sense amplifier, you must first

understand the concept and operation of SRAM. Basic 6T SRAM structure is presented in Fig. 3.1.

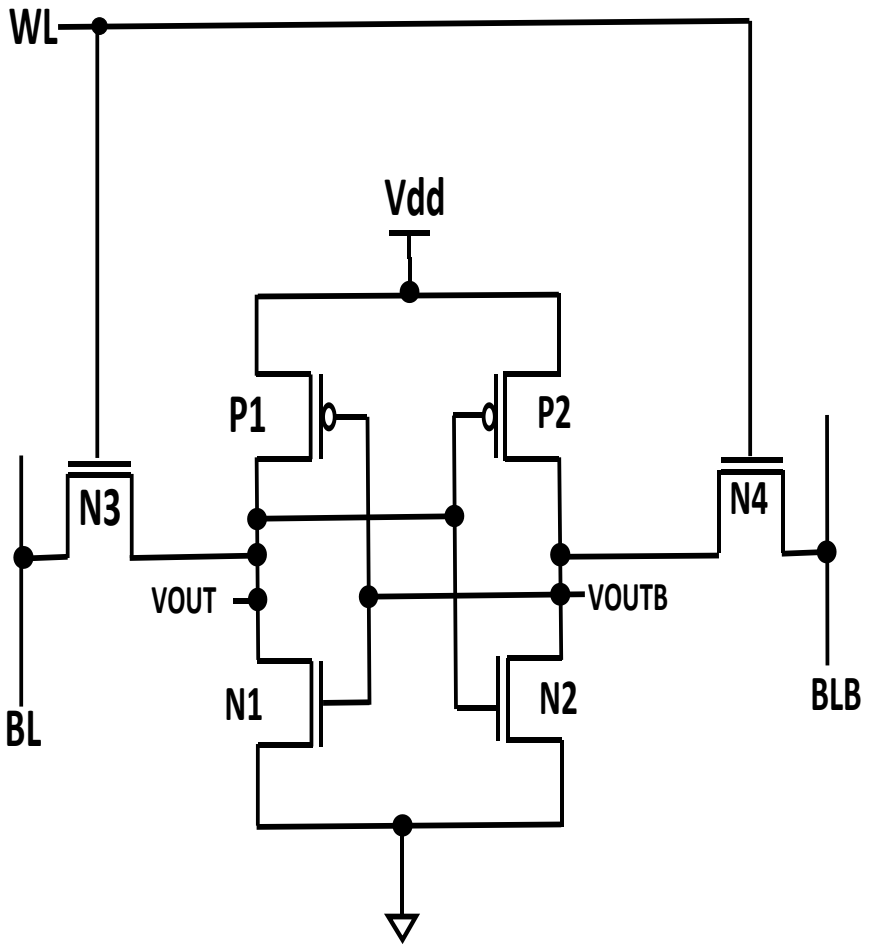


Fig. 3.1 Schematic of 6T SRAM

The SRAM cell is just a flip flop. Binary data "0" or "1" is stored on the internal or storage nodes of this flip flop [2]. Six MOSFETs make up the 6T SRAM cell, with four of them acting as CMOS inverters to store bits as 1 or 0, and the other two acting as pass transistors to operate the SRAM via the bits line. The SRAM circuit can be accessed when the WL (word line) is high.

3.2 Sense Amplifier

The semiconductor memory integrated circuit (IC) chip's important component is sense amplifier (SA). It is a component of the read circuitry. This is used to read information from memory. SRAM is capable of high-speed operations with low power consumption. However, its peripheral circuit might have a significant impact on the system's speed and power [3].

The struggle between read and write stability is the main design issue in the SRAM cell. The primary function of SA is to detect data stored by amplifying minor voltage differences to desirable logic levels depending on discharge in bit line voltages [4]. From the fundamentals to sophisticated sensing circuits, the sense amplifier circuits were investigated in detail. The Current Mode Sense Amplifier (CMSA) also known as non-differential SA serves the differential output voltages to the output line pair of SA. The Voltage Mode Sense Amplifier (VMSA), also known as differential SA, is connected to the SA output line pair to enhance the differential output voltages. The voltage SA is turned on after the CMSA has been turned on. As a result, the VMSA is commonly employed because no static current passes through it after the SA locks, resulting in a power reduction.

In this chapter, two major classifications of SA are explored. VMSA are genuine and straightforward. Differential sensing, on the other hand, deals with most of the Silicon. Despite this, most of the architecture relies on differential SA to connect exceedingly dense packing.

3.3 Major Classification of Sense Amplifier

Different Sense Amplifier topologies are classified in this section. SRAM is capable of high-speed operations with low power consumption. However, its peripheral circuit might have a significant impact on the system's speed and power [5-6]. Memory performance is mostly influenced by SA characteristics like as latency and power dissipation [7]. Memory size is shrinking while storage capacity is increasing in today's world. The time effect of reading and writing data from the memory would be exceedingly rapid as storage efficiency improves. As a result, several SAs are used to attain this goal [8].

Double Switch transmission Gate Voltage Mode SA (DSTG-VMSA) and Current Mode latch sense Amplifier (CMSA) are two basic SRAM-based VMSA (Differential) and CMSA (Non-Differential) topologies that were employed in the early stages of research.

3.3.1 Voltage Mode Sense Amplifier (VMSA)

In 2013 Na *et al.* [9] reported DSTG-VMSA. To depreciate the leakage current while standby mode, the double switch transmission gate voltage Mode SA (DSTG-VMSA) is designed. The head switch transistor M1 and foot switch transistor M6 relates to enable pin (EN) to avoid

leakage current. The (DSTG-VMSA) is depicted in Fig. 3.2. The cell comprises of five PMOS and four NMOS transistors where transistor M9 and M10 are combined with transistor M7 and M8 to make transmission gate as it is combination of pmos and nmos transistor. The M2-M5 transistors created a cross couple inverter.

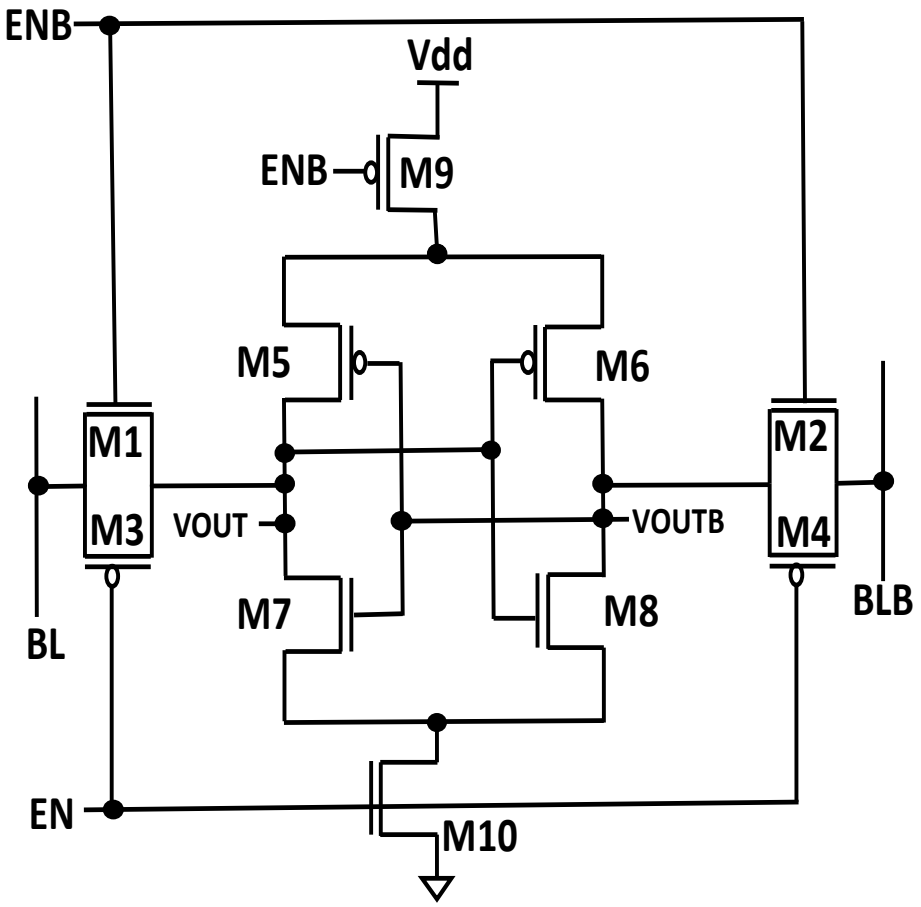


Fig. 3.2 Circuit Diagram of Voltage Mode Sense Amplifier

The switching transistors M1 and M6 turned on when enable bar pin (ENB) was "0" and pin (EN) was "1." Assume that when ENB is 1 and EN is 0, BLB is "0" and BL is "1," which turns off the tail transistors and turns on the transmission gate transistors (M7, M8, M9, M10). So that the output node BL is charged at the same rate as BLB. Power and energy are saved, also the SA's speed is boosted, due to the double switch and reduced leakage current.

3.3.2 Current Mode Sense Amplifier

The voltage mode sense amplifier is used in the Current Latch Sense Amplifier. It's also a voltage sensing amplifier of the differential type. Two cross-coupled inverters are employed in this amplifier to provide positive feedback, similar to a latch type sense

amplifier. However, by inserting two additional nmos transistors, the bit line is isolated from its output. As a result, the input impedance is extremely high.

In year 2012, current mode latch sense amplifier (CMSA) has been described by B. Mohd. *et al.* [10]. The current mode sense amplifier may have more advantages because of no extra intermediate voltage.

The design for the CMSA is shown in Fig. 3.3. This SA comprises of six PMOS (M1, M2, M8, M9, M10 And M11) and five NMOS (M3, M4, M5, M6 and M7. The inputs of Bit line BL and BLB are connected to column bit lines. The cross coupled inverter formed in the SA is used for full swing at the output. Bit line BL and BLB operates the gate of transistor M5 and M6. The transistor M8, M9, M10 and M11 are precharge transistors.

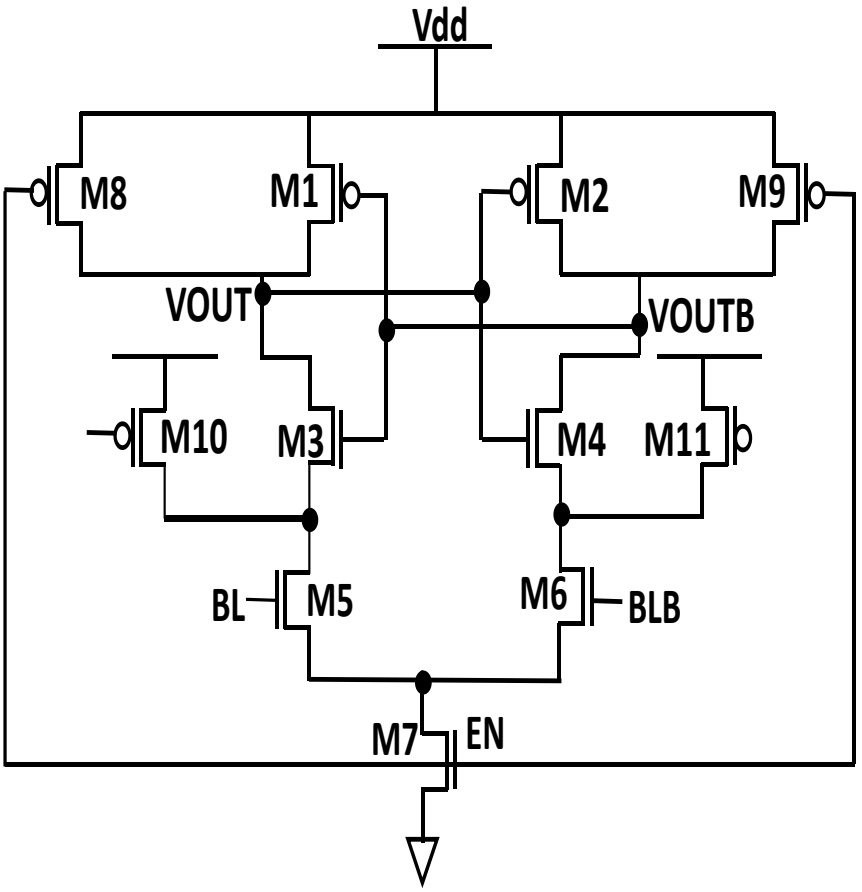


Fig. 3.3 Current Mode Sense Amplifier

Here, Transistor M1, M3, M2, and M4 formed cross coupled network. When enable pin (EN) is high, transistor M7 turned ‘ON’ and precharge transistors turned ‘OFF’. Since M5 and M6 differs their channel currents are different and the current on either output node VOUTB or VOUT is faster than other node. So, by this SA this difference is set on.

The Table 3.1 shows the Comparative Properties of both Voltage and Current Mode Sense amplifiers.

Table 3.1 – Comparative properties of voltage and current SA

S. NO.	VMSA	CMSA
1.	Na *et al.* [9] reported double switch transmission gate voltage latch SA in 2013.	B. Mohd. *et al.* [10] reported a current mode latch sense amplifier in 2012.
2.	Voltage mode Sense amplifiers are used to identify bit line Voltage differences.	CMSA are used to observe the bit line current differences to evaluate the stored data into the memory cell is either a '0' or '1'.
3.	Voltage mode sense amplifiers (VMSA) are devices that detect voltage variations on the bit line.	CMSA are operated to minimize the delays of SA as they produce low common I/O impedances. Advantage of CMSA is it is not suffering from additional complexity of design.
4.	During read operation of cell, some small voltage swing arises on the bit lines that is used to drive digital logic and moreover amplified by differential couple. Although the voltage swing of bit lines is being reduced and is achieving the similar extent even so bit line, the VMSA become unusable.	The purpose for using CMSA in SA circuits is small input impedances of them. Perquisites of small output and input impedances are decrements into, cross talking, voltage swings, substrate voltage and current modulations.

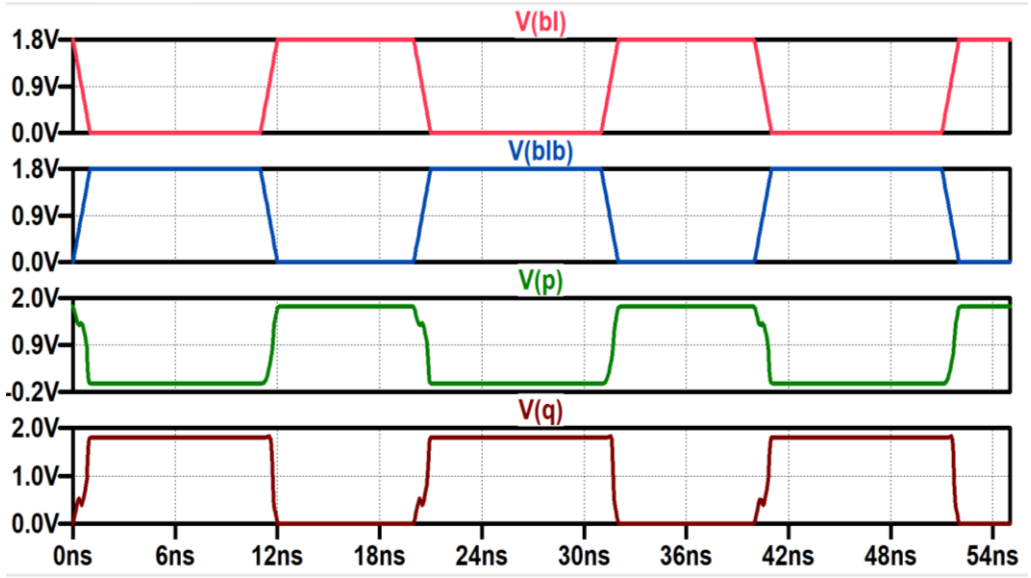
It can be surmise with table 3.1 that both the VMSA and CMSA have their own properties and applications. By applying these SAs in VLSI design performance can enhance and can reduce the power consumption for integrated circuits.

3.4 Performance Analysis of SA Classifications

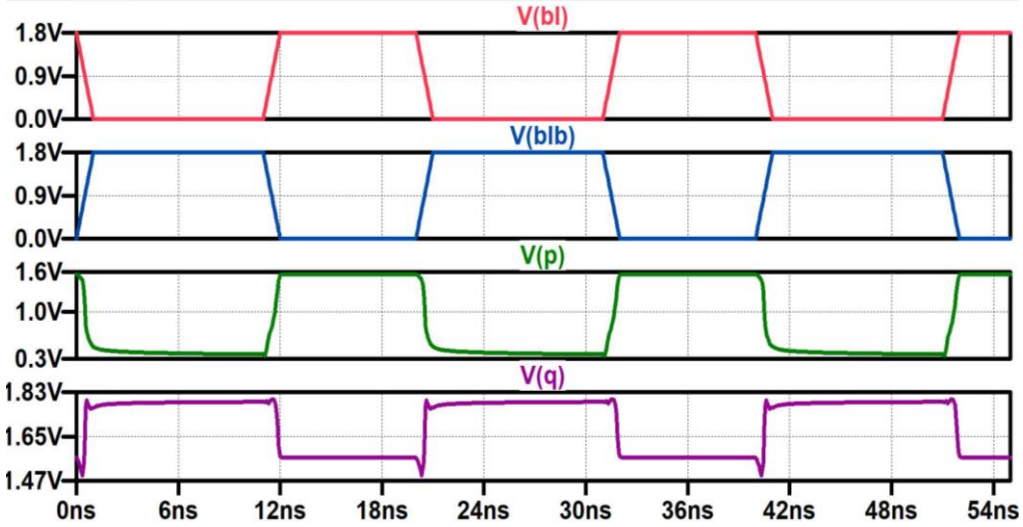
Illustrated Sense Amplifiers in Fig. 3.2 and Fig. 3.3 are simulated on 180 nm technology node employing the supply voltage of 1.8 V. To achieve parameter performance for; power, current and energy, the optimized simulation results of designed VMSA and CMSA are analyzed in this division. The simulations are performed using LT SPICE. The simulation results obtained are clarified in the following subdivision. Aspect ratios of nmos both the SAs is 4:1 and for nmos of both the SAs is 2:1 and L = 180 nm and W = 360nm respectively. The simulation findings are presented in the sections below.

3.4.1 Output Characteristics

Performance of characteristics such as energy, power, and current are vital to achieve excellent performance while developing memory cells [11]. The plots are observed over a period of 55ns. The output Waveform for VMSA circuit functionality is illustrated in Fig. 3.4 (a), here v(q) i.e., OUTB is follows same as bit line bar BLB and v(p) i.e., OUT is following bit line BL. Thereby confirming the working of VMSA. The "W" and "L" values of nmos transistor is W is equal to 0.36um and L is 0.18um and for PMOS, "W" is 0.72um and "L" is 0.18um respectively.



(a)



(b)

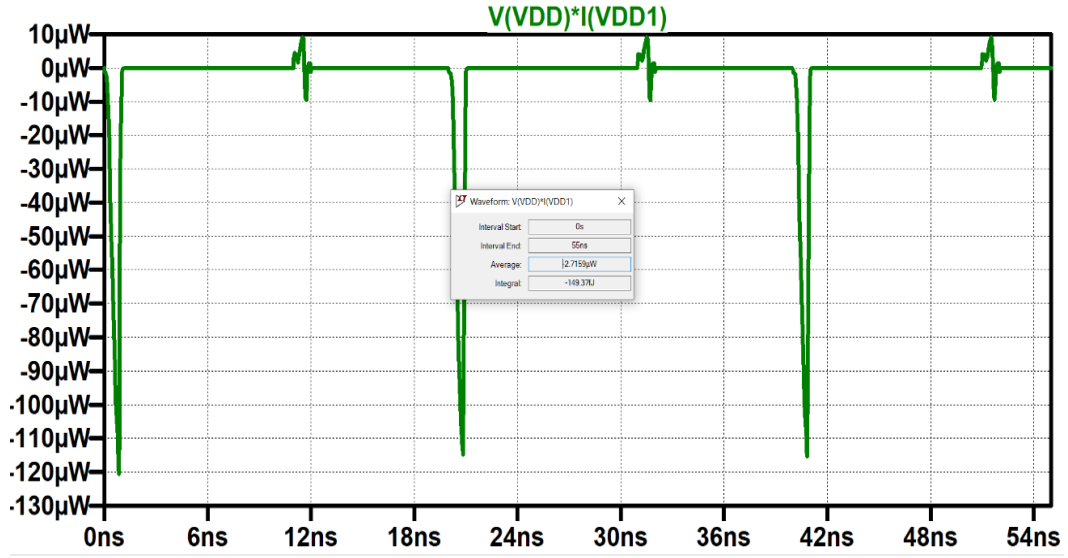
Fig. 3.4 Output Characteristics of (a) VMSA and (b) CMSA

Waveform of CMSA circuit functionality is depicted in Fig. 3.4 (b). Here v(q) i.e., OUTB is follows same as bit line bar BLB and v(p) i.e., OUT is following bit line BL.

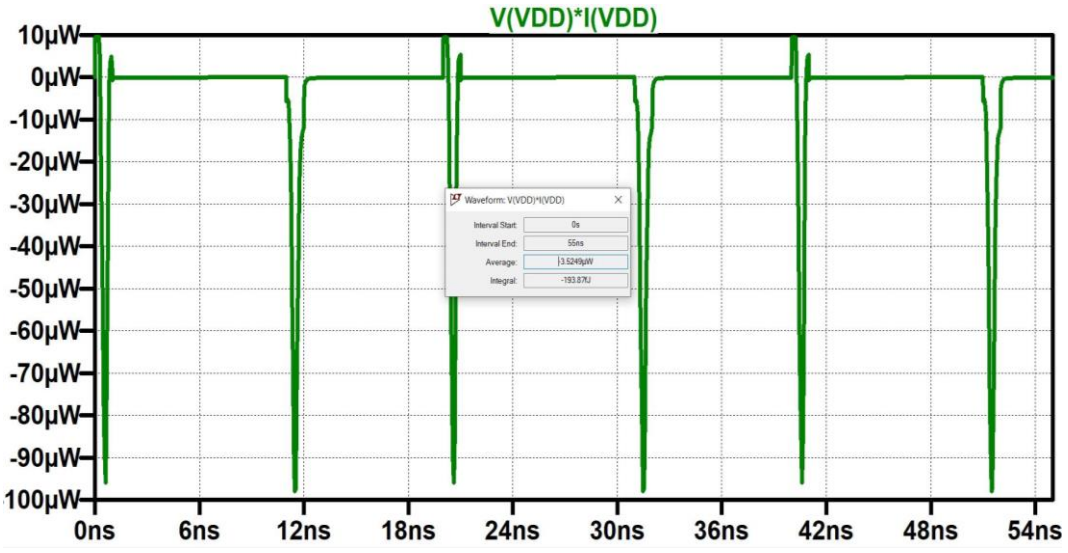
This confirms the working of CMSA. The “W/L” ratio of CMSA is same as “W/L” ratio of VMSA for both Pmos and Nmos transistors.

3.4.2 Power and Energy Analysis

The amount of power dissipated by a circuit is an important factor to consider. Because batteries have a certain amount of power, the device should only utilize that much [12-13]. The low power is important to avoid supplementary system required for cooling. Also, they created portable problem [14-15].



(a)



(b)

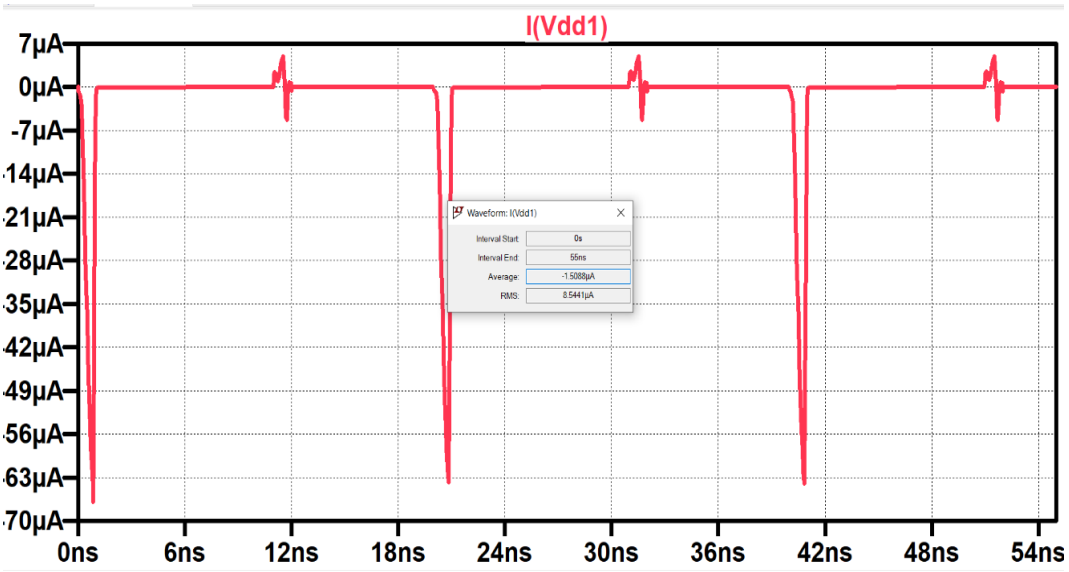
Fig. 3.5 Power and Energy of (a) VMSA and (b) CMSA

Because of the additive system, the cost of the systems has increased. With the growing demand for low-power gadgets [16], it's becoming important to investigate SA's power dissipation. Power dissipation should be kept to a minimum when designing the SA [17]

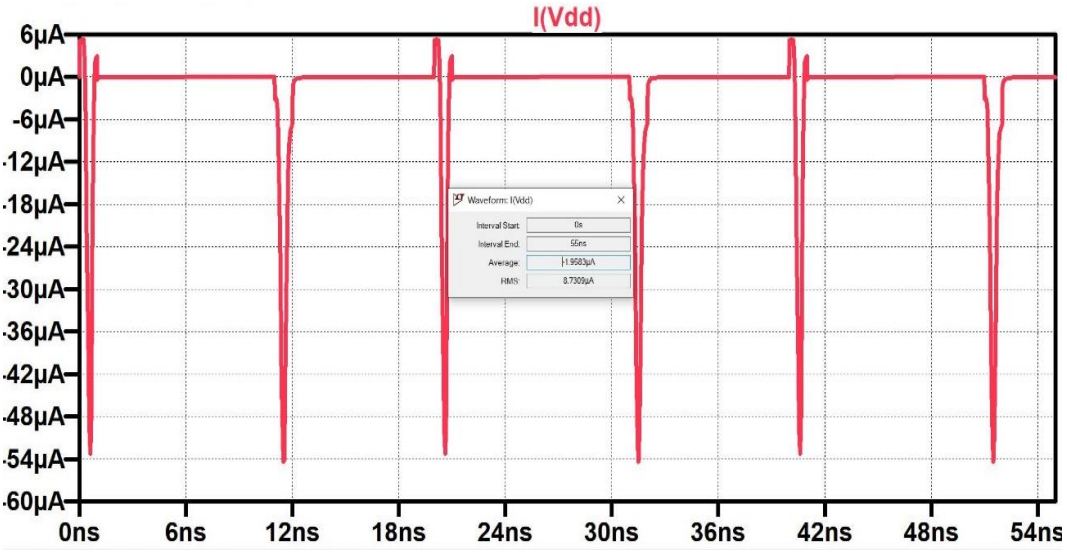
The overall power consumption within the circuit is shown in Fig. 3.5 (a) and Fig. 3.5 (b). Power obtained for VMSA and CMSA is 2.715 uW and 3.524 uW respectively.

3.4.3 Current Analysis

Fig. 3.6 (a) and Fig. 3.6 (b) shows the output waveform based on current analysis of both the SA configurations. It can be inferred from the figure that VMSA has the low current i.e., 1.5088 uA and CMSA has the high current i.e., 1.9583 uA. This is due to design and transistor sizing.



(a)



(b)

Fig. 3.6 Current analysis of (a) VMSA and (b) CMSA

It can be inferred from the figure that VMSA has the low current i.e., 1.5088 uA and CMSA has the high current i.e., 1.9583 uA. This is due to design and transistor sizing.

Current (I) equals to power divided by voltage. (V=1.8)

$$I = P/V \tag{3.1}$$

The Table 3.2 surmise the result comparison of various parameters the two sense amplifiers.

Table 3.2 - Comparative result for VMSA and CMSA

Sense Amplifier	Power (µW)	Energy (fJ)	Current (µA)	Transistor-Count
VMSA	2.715	149.37	1.5088	10
CMSA	3.524	193.87	1.9583	11

*Overall Performance; [a] At Supply Voltage=1.8V

It can be surmise from Table 3.2 that CMSA has more power dissipation i.e., 3.524 uW approximately half as compared to VMSA i.e., 2.715 uW respectively. Consequently, among the two circuits, VMSA has very less energy 149.37fJ which is less than that of CMSA i.e., 193.87fJ while the transistor count of both the transistors are approx. near and w/l ratio and other parameters for both designs are same. It indicates that between these two circuits VMSA is the right choice for low power applications. The result demonstrates that power and energy of VMSA is less as compared to CMSA. Therefore, VMSA are an ideal fit for low power integrated circuits; while the power consumed by CMSA is higher so more suitable for circuits with not much power constraints such as power plants and large power sources. By applying these SAs in VLSI design performance can enhance and can reduce the power consumption.

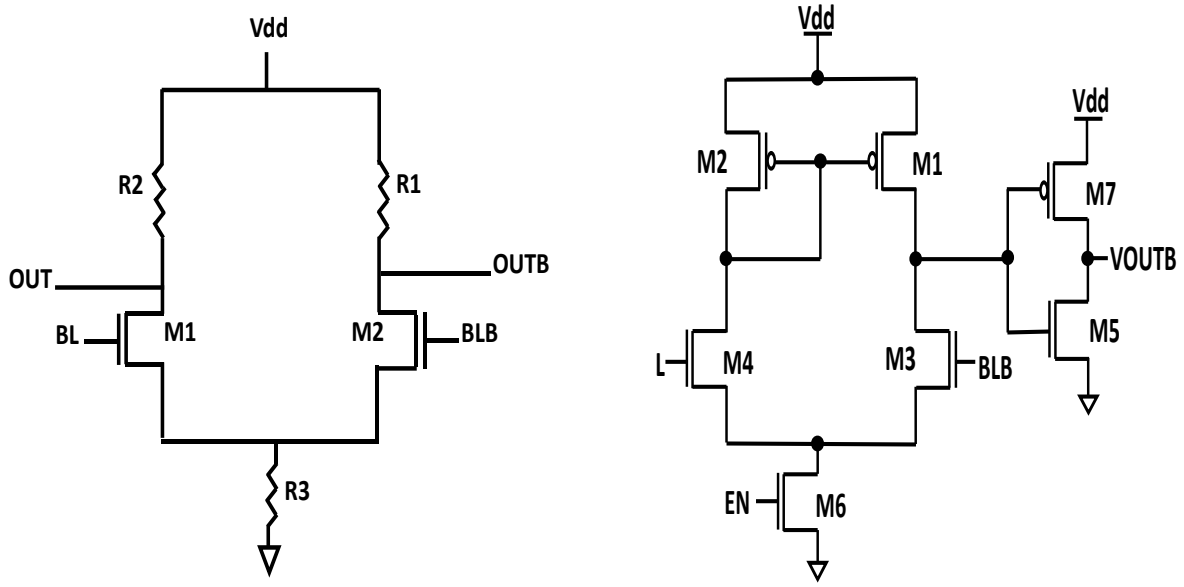
3.5 Differential Sense Amplifier Topologies

Most CMOS memories, including all SRAM, DRAM, many ROM, and other memory architectures, use differential sense amplifiers. The primary criterion for memory design is the design of sensing amplifiers [18]. The sense amplifiers are connected to a pair of identical bit lines in such devices. Single ended amplifiers, differential amplifiers, latch type SAs, and cross coupled sense amplifiers are examples of voltage mode SAs. Various varieties of SAs are employed in a variety of memory cells, depending on the memory cell's design and performance needs [19]. As the VMSA are an ideal fit for low power integrated circuits it is important to analyze various differential SA (VMSA).

3.5.1 Basic Differential Sense Amplifier (BDSA)

Multiple SA topologies and their working analyses has been presented in this section.

Fig. 3.7 recorded diverse SA cells proposed over the decades in literature. In 2019, Selvakumar *et al.* [20] presented basic differential sense amplifier (BDSA) depicted in Fig. 3.7 (a). Differential SAs have been familiar for a long interval. This amplifier contains all necessary elements for sensing. The SA is made up of two transistors (M1 and M2) and three resistors (R1, R2 and R3). It takes small input signal and amplifies to large output signal. These circuits are used in noise rejection. The most basic circuit is not used in all application due to its low speed. Small difference at bit lines BL and BLB are amplified to full swing output node.



(a) (b)

Fig. 3.7 Schematic diagram of (a) BDSA and (b) HSVSA

Its capability to discard common noise and amplifying true variation present between the signals characterize the effectiveness of amplifier. Due to its slow speed of reading data, considerably high-power dissipation, and intrinsic high offset, basic VMSA is not used in SRAMs.

3.5.2 High Speed Differential Sense Amplifier (HSVSA)

In 2016, Pathrikar *et al.* [21] depicted the basic High-speed voltage Latch SA (HSVSA) design shown in Fig. 3.7 (b). In this circuit, there are three NMOS transistors (M3, M4, and M6) and two PMOS transistors (M1 and M2), and a CMOS inverter. The operation starts with an active enable signal (EN), the bit line voltage difference "BL" and "BLB" is being detected by SA, and the output voltage is carried out. The suitable design of Sense amplifier is the first objective for designing SRAM based circuits [22]. The SA senses the point variation between the BL and BLB voltages as quickly as EN

goes high and produces a desired output voltage A CMOS inverter is attached additionally with SA output to amplify the magnitude. Due to high gain of inverter the output achieved VOUT is high and the cost of HSVSA is high.

3.5.3 Current Latched Based VMSA (CLVMSA)

W. jin-shyan *et al.* [23] in 2014 reported a current latched based VMSA (CLVMSA). The schematic is shown in Fig. 3.8 (a). The circuit provides strong feedback. The enable bar signal (ENB) activates the M4. Transistors M2, M3, M5 and M7 forms an inverter. Through bit lines BL and BLB, internal nodes are pre charged. When M4 is active low, the pass transistors M1 and M6 are "ON", and full swing output is amplifying the differential voltage.

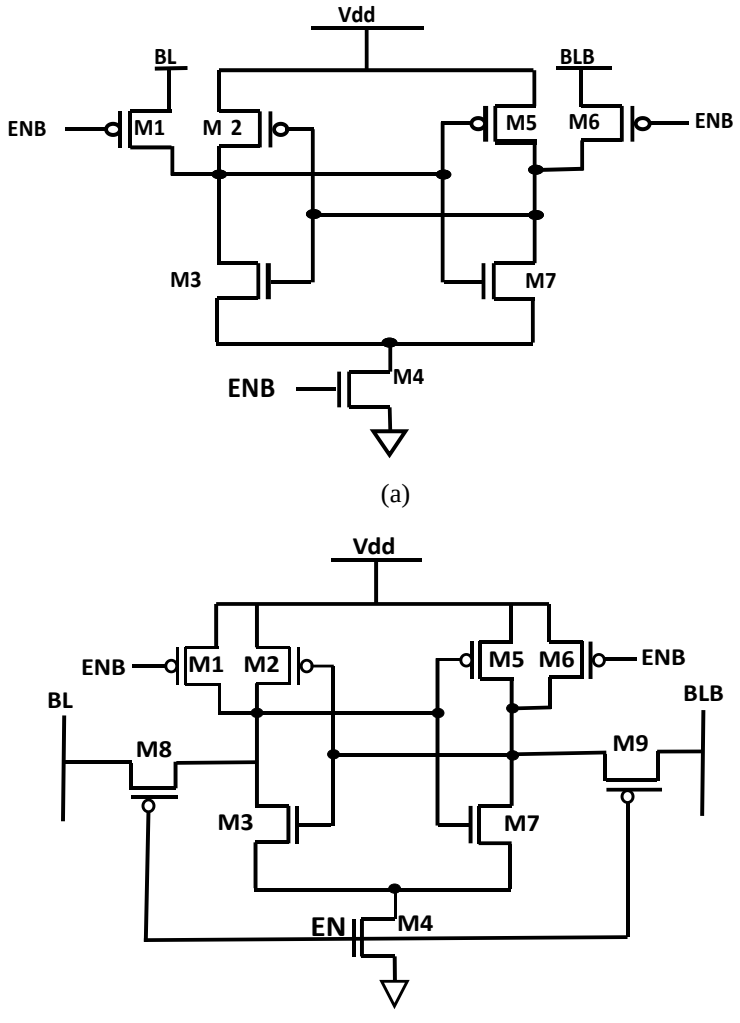


Fig. 3.8 Schematic diagram of (a) CLVMSA and (b) CCLSA

3.5.4 Cross Coupled Latch Sense Amplifier (CCLSA)

In 2016, Gundu *et al.* [24] introduced a cross coupled latch sense amplifier (CCLSA) depicted in Fig. 3.8 (b). Here transistor M2, M3, M5 and M7 form a cross coupled

inverter hence named as cross coupled SA. Two additional pre charging transistors M1 and M6 are present in the circuit. The reason for choice of this SA is its high-speed functionality due to pre-charging nodes. For proper separation of internal and output nodes EN should be controlled carefully in these SAs. The SA is good in speed prospective but not worth for power consumption. The other drawback of CCLSA is current leakage from output node to input node between drain and source of M7 and M8 when EN is active high.

3.6 Performance Comparison of Differential Sense Amplifier Topologies

Design objectives for sense amplifiers that combine specified environmental tolerance, Due to the contradictory effect of circuit complexity and transistor sizes on individual design goals, achieving sufficient amplification, low power consumption, restricted layout area, and good reliability is difficult. In this section the performance comparison of differential sense amplifier topologies is presented.

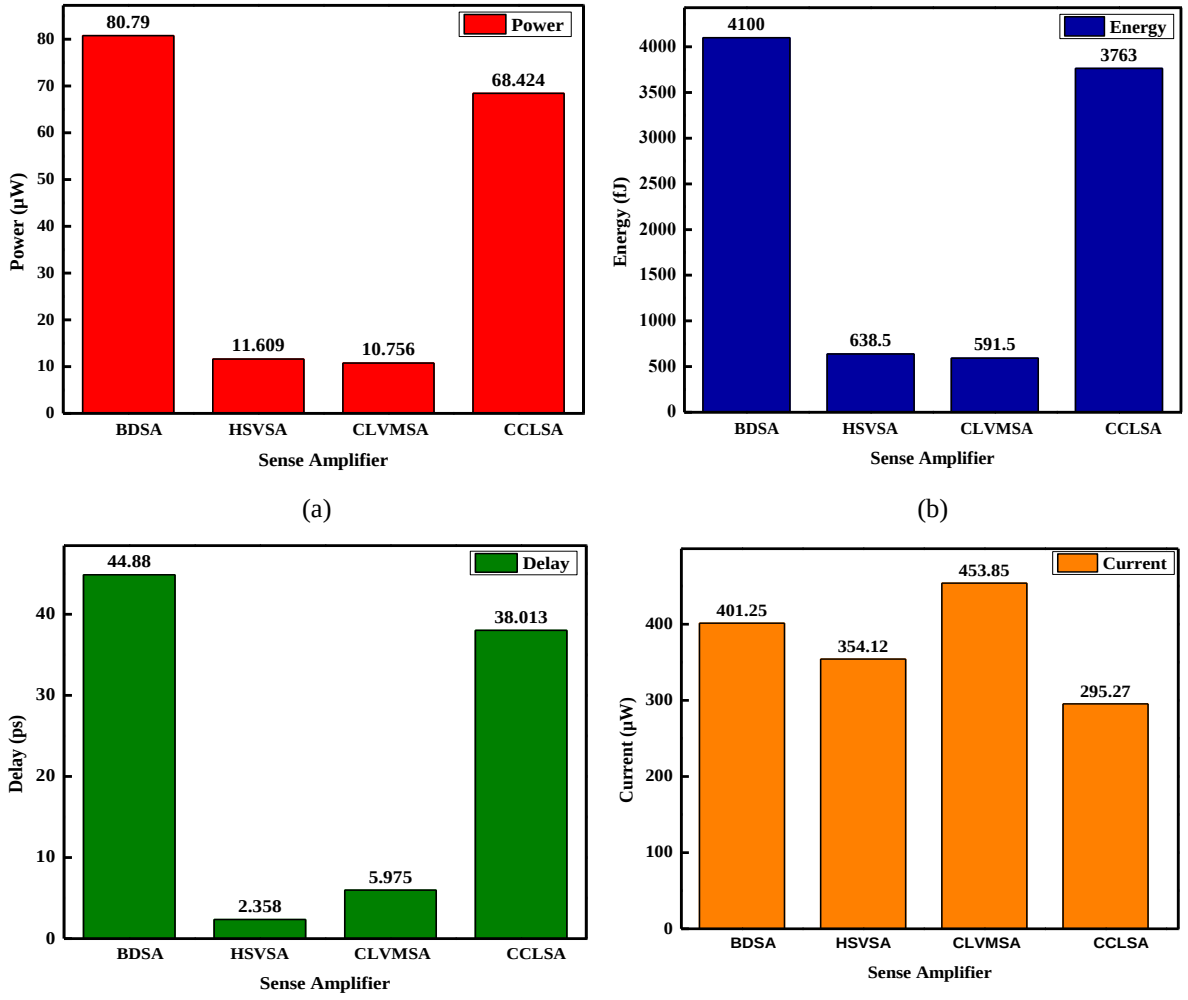


Fig. 3.9 Comparative results of (a) power, (b) energy, (c) delay and (d) current

In Fig. 3.9 comparative results of differential SA topologies are shown. Fig. 3.9 (a), (b),

(c) and (d) shows the power, energy, delay, and current comparison respectively. Also, the comparative data are tabulated in table 3.3. The Table 3.3 shows the result comparison of four differential amplifier topologies described in section 3.5.

Table 3.3 - Comparative result for Sense Amplifier topologies

Sense Amplifiers	Power (µW)	Energy (fJ)	Delay (ps)	Current (µA)	No. of Transistors
BDSA	80.79	**4100**	**44.88**	401.25	2
HSVSA	11.609	638.5	**2.358**	354.12	7
CLVMSA	10.756	591.5	**5.975**	453.85	7
CCLSA	68.424	3763	38.013	295.27	9

It can be inferred that the BDSA consume maximum power i.e., 80.79 µW with least transistors used and CLVMSA perform best in terms power, energy, and transistor count.

3.7 IMPORTANT OUTCOMES:

The major classifications of sense amplifiers, Voltage mode and Current mode sense amplifiers, are simulated and analyzed in this chapter. Both designs' properties are compared. Finally, the excellent is examined in further depth.

- Designing and analysis of major classification of SA - Voltage mode and Current mode SA by simulating the same with the help of LTSPICE tool in 180nm CMOS technology with a voltage supply 1.8V.
- The comparability and properties between these two circuits are analyzed to identify the best of the two amplifiers, CMSA consumes approximately double power than VMSA. The result comparison of various parameters of the two topologies is shown in Table 3.2.
- Properties of both voltage and current sense amplifiers are depicted in Table 3.1. From analyzed simulation result VMSA found to be the best choice.
- For best SA, differential sense amplifier topologies are analyzed. Too much difference between results of four topologies, and as CLVMSA perform best then review of cross coupled amplifier is important for best performance.

CHAPTER 4

PARAMETRIC EXTRACTION AND COMPARISON OF DIFFERENT VOLTAGE-MODE BASED SENSE AMPLIFIER TOPOLOGIES

The design of CMOS cross-coupled inverter sense amplifiers is discussed in this chapter using an analytical method. Different sense amplifiers are employed in different types of memory cells based on their design and performance. As a rapid and reliable sense amplifier, the CMOS cross-coupled inverter pair is often utilized. The differential couple is the simplest voltage sense amplifier [25].

The following is the arrangement of this chapter:

- The basic circuit of a cross coupled sense amplifier is described in Section 1.
- Advanced cross coupled sense amplifier structures are constructed and investigated in section 4.2.
- In section 4.3, simulated analytical results are presented, followed by a performance comparison of cross coupled SA topologies in section 4.4.
- Finally, important chapter outcomes are reported in section 4.5.

4.1 Cross Coupled Sense Amplifiers

Basic circuit of cross coupled sense amplifier is depicted in Fig. 4.1. A slight voltage swing happens on the bit line when a cell is read, which is amplified by differential coupling and used to operate digital logic. The voltage sense amplifier becomes ineffective as the bit line voltage swing decreases and approaches the same magnitude as bit line noise. [26-27]. The positive feedback is exploited to achieve a fast-sensing operation. Basic circuit of cross coupled voltage sense amplifier is shown in Fig. 4.1. M1-M4 constitute cross-coupled inverters in the circuit depicted in Fig. 4.1, whereas M5 is the driver transistor. When the read operation is initiated, voltage is charged and discharged on BL and BLB, which are coupled to this sense amplifier.

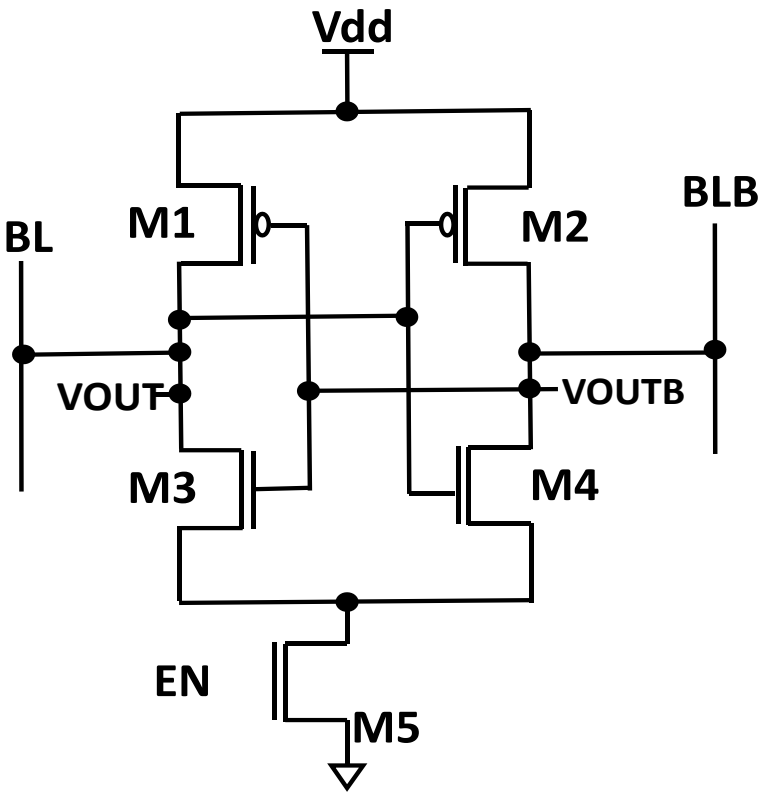


Fig. 4.1 Basic Circuit of Cross Coupled Sense Amplifier

Positive feedback causes the upper voltage level to go to VDD and the lower voltage level to go to zero. The nodes BL and BLB are input and output terminals at the same time in the basic cross-coupled SA.

4.2 Advanced Cross Coupled Voltage Mode Sense Amplifier Topologies

This section is describing the advance Voltage Mode Sense Amplifier Topologies with enhancing performance. Many identical and distinctive SA concepts have been recognized to meet the design goals that a SA may face. Design goals include low power, low energy, and low delay, as well as high speed, small area, and low power supply. This section contains some of the most notable SA cells created in the last decade. SA is a necessary component of semiconductor memory IC chips [28-29]. It's the read circuitry factor. This is necessary for reading data from memory. There are various topologies of Single ended, double ended, latch type SA, and cross coupled sense amplifiers are examples of differential mode sense amplifiers (VMSA). Different varieties of SAs are used in various memory cells, depending on the memory cell's design and performance needs.. Among all SAs, Cross coupled voltage mode SA (VMSA) are best. The reason for choice of cross coupled latch SA due to there is no static current passed through it and are used to identify bit line voltage differences during read operation. So, the design

and analyses with proper circuit operation and output of best performing VMSA for SRAM is provocation for low power application. The main parameters for best design considerations are power, area, speed, aspect ratio, and transistor count etc. Major classifications of VMSA are discussed within the work [30]. Latch type SAs are common to all of the SAs mentioned in this chapter. For all PMOS and NMOS transistors, the aspect ratios of all SAs are the same.

4.2.1 Conventional Cross Coupled Voltage Latch SA (CCVLSA)

It is necessary to use a latch type cross-coupled voltage mode sensing amplifier because the current flow stops automatically once the choice process is accomplished. Because of the powerful positive feedback, this sense amplifier is used to read the contents of many forms of memory. Kishore *et al*. [31] in (2019) reported the most favored and known SA in the industry is conventional cross coupled voltage latch SA (CCVLSA) depicted in Fig. 4.2.

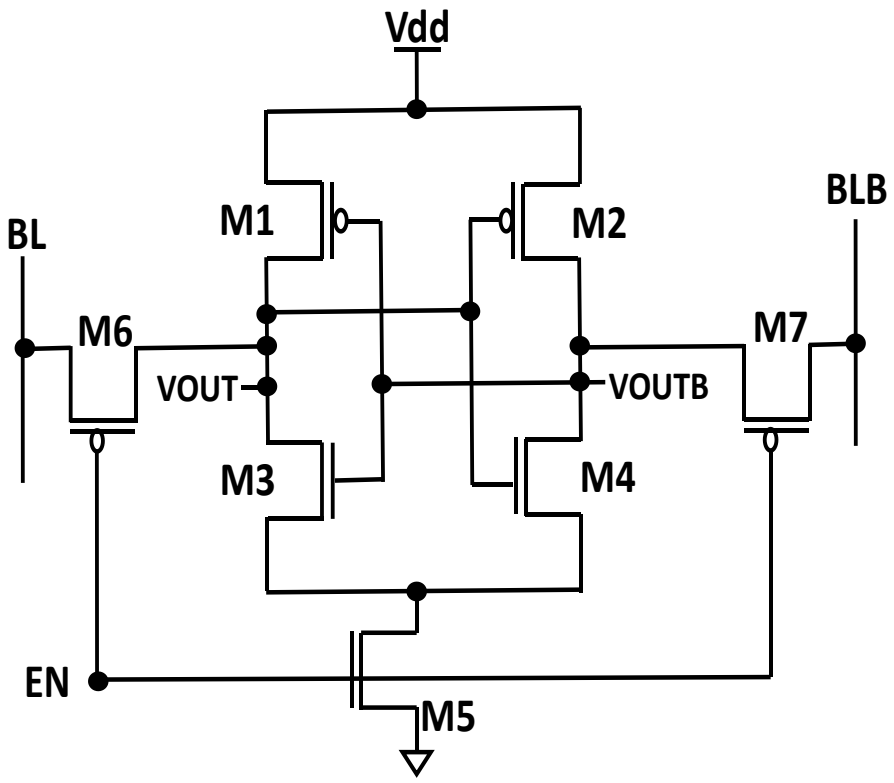


Fig. 4.2 Schematic Design of CCVLSA

Access transistors, driver transistors, and load transistors are the three primary components of SA. The SA detects the voltage difference between bit lines BL and BLB. Single ended, VMSA, and cross coupled SAs are examples of SAs. For different memory cells, different SAs are practiced [31]. Because the output nodes of these types of SA also act as input nodes, enable (EN) must be managed carefully.

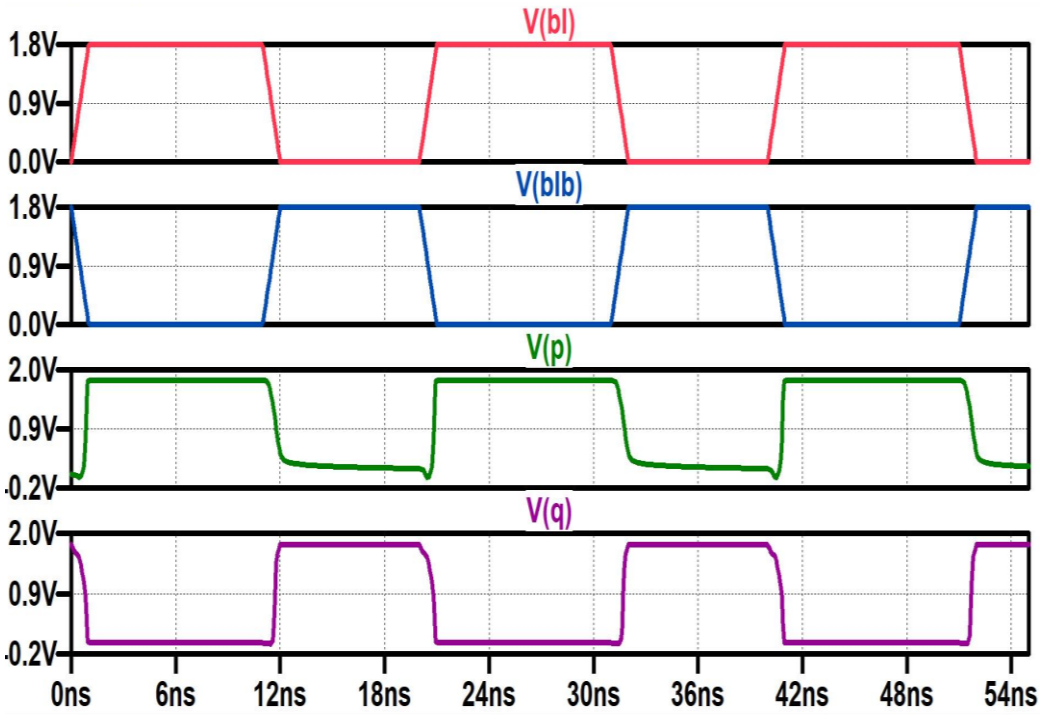


Fig. 4.3 Output Waveform of CCVLSA

To reduce the leakage current while in standby mode, a transistor M5 (footswitch) is necessary. Assume that the bit line (BL) has a higher voltage than the reference voltage, but the BLB has a lower voltage. The SA brings active by using enable (EN). Output waveform of CCVLSA is shown in Fig. 4.3 where, OUT P follows BL and OUT Q follows BLB.

4.2.2 Double switch cross coupled VMSA (DSCVMSA)

The performance and current path in conventional cross coupled voltage latch SA is improved by modifying it with a Double switch cross coupled VMSA (DSCVMSA) is reported by Na *et al.* [9] in 2013. By introducing additional head switch and correspondent enable (ENB) signal as shown in Fig. 4.4. the head switch limits the weal latching transistors from being active during idle period, therefore the infirm current path is restricted and enable (EN) must be activated before ENB to transistor M1 and M3 remain turned OFF.

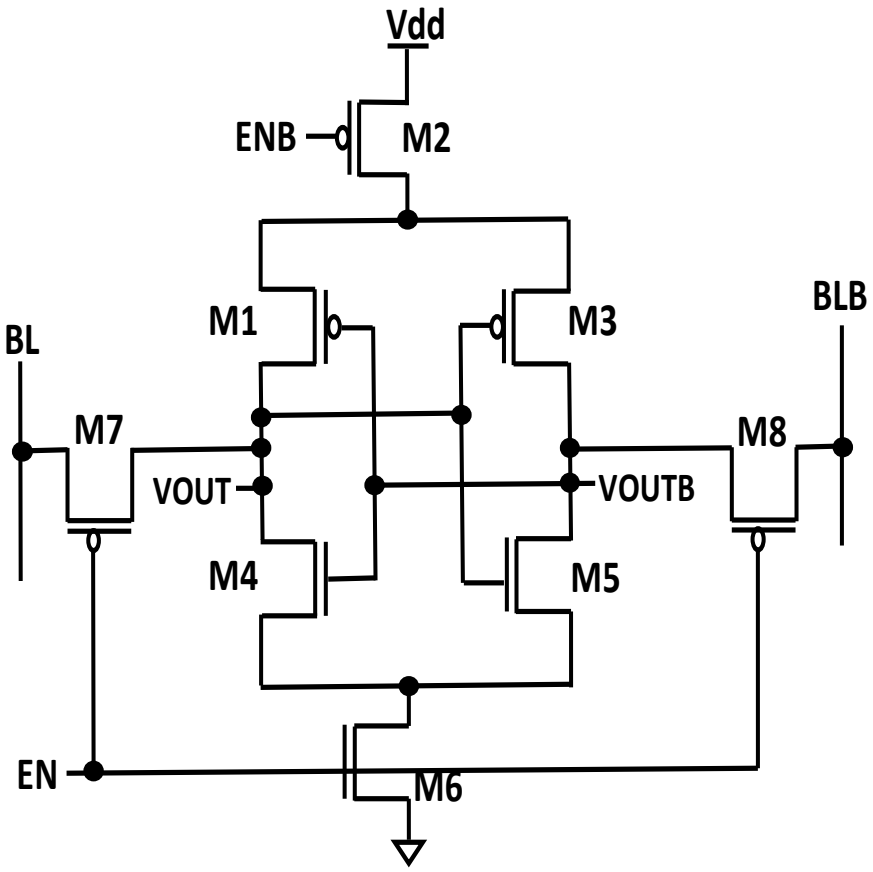


Fig. 4.4 Schematic Design of DSCVMSA

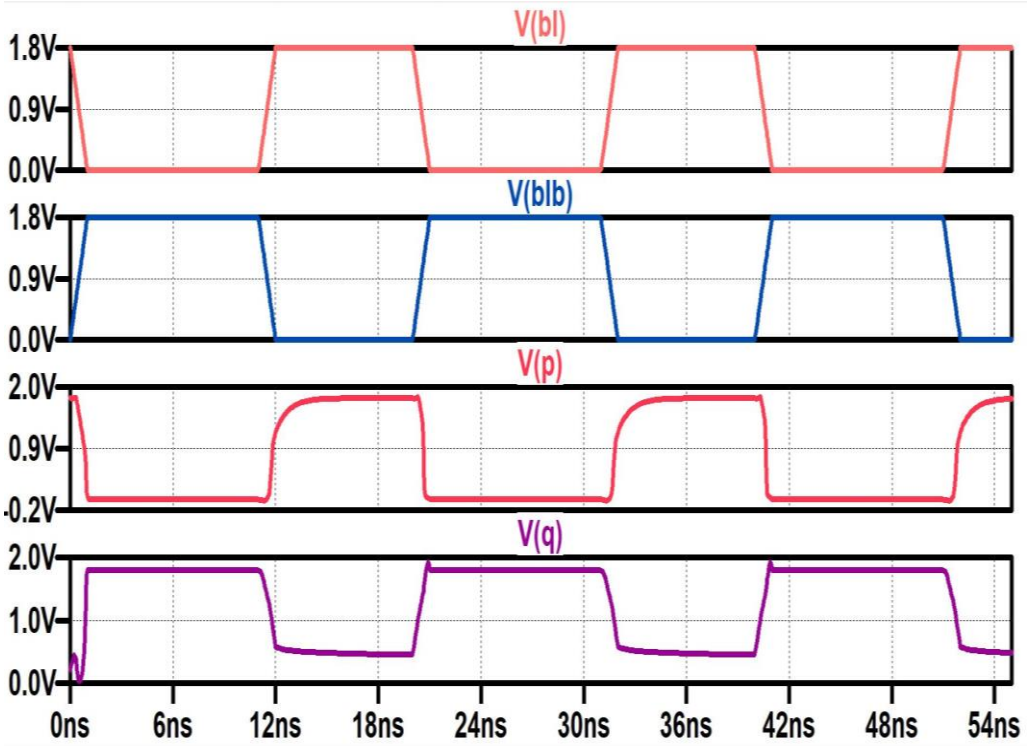


Fig. 4.5 Output Waveform of DSCVMSA

The Enable Bar turns “ON” the transistors M7 and M8. The output nodes charged equal to voltage of BL and BLB. When EN is active and ENB is inactive the access transistors

M7-M8 turned OFF. Then node at the source of head switch M1 is pick up to Vdd and node at drain of bottom switch M6 takeout to ground level. Thus, the output towards BL be identical to power supply (vdd) and output towards BLB be equal to zero. The output Waveform for DSCVMSA circuit functionality is illustrated in Fig. 4.5. Here, v(q) i.e., OUTB is follows same as bit line bar BLB and v(p) i.e., OUT is following bit line BL. Thereby confirming the working of VMSA.

4.2.3 Transmission Gate Voltage Latch SA (TGVLSA)

In 2019 Kishore *et al*. [31] reported the design of transmission gate voltage latch SA (TGVLSA) depicted in Fig. 4.6. The design consists of four PMOS (M6, M8, M1 and M2) and five NMOS (M3, M4, M5, M7 and M9) TGVLSA works same as CCVLSA only two additional transistors M5 and M7 are added by two PMOS transistors M6 and M8 and formed a transmission gate. The transmission gate transistors are attached to BLB and BL.

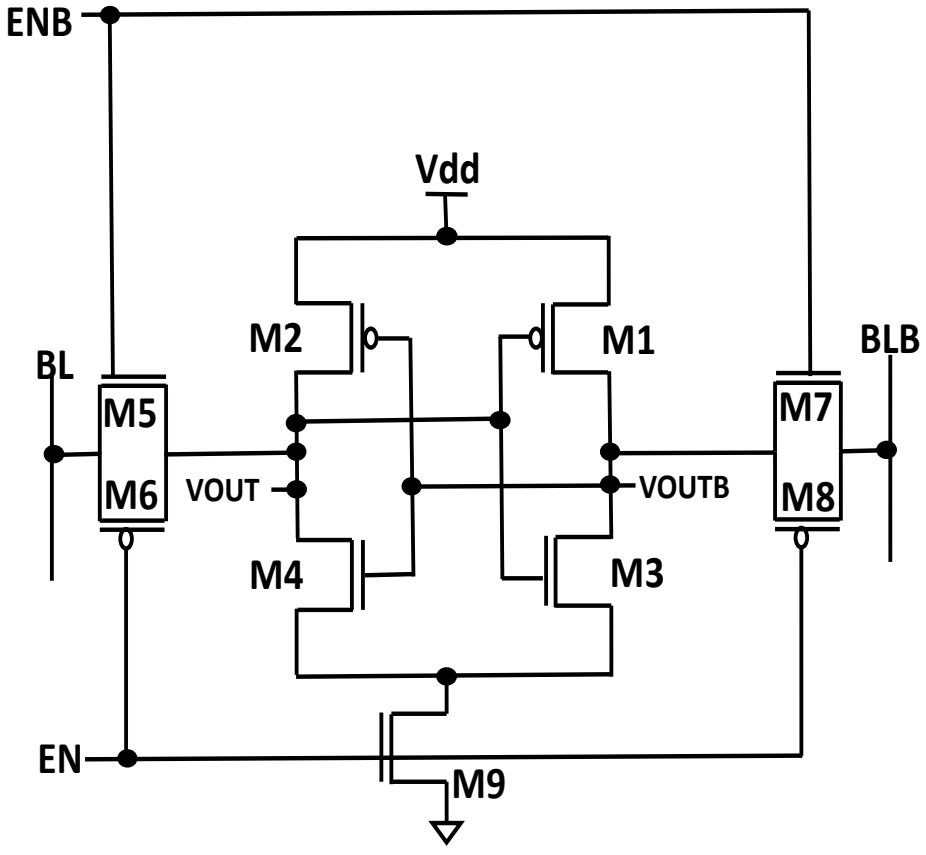


Fig. 4.6 Schematic Design of TGVLSA

The delay and power of TGVLSA is improved as compared to CCVLSA. Therefore, Transmission gate is the combination of PMOS and NMOS also known as analog or CMOS switch. Also, they have the property to conduct in both the directions and reject by any potential. TGVLSA is used to allow or reject a signal towards output [31]. The

transmission gate is used to control gate signal and acts as a bi-directional switch. The "W" and "L" values of nmos transistor is W is equal to 0.36um and L is 0.18um and for PMOS, "W" is 0.72um and "L" is 0.18um respectively.

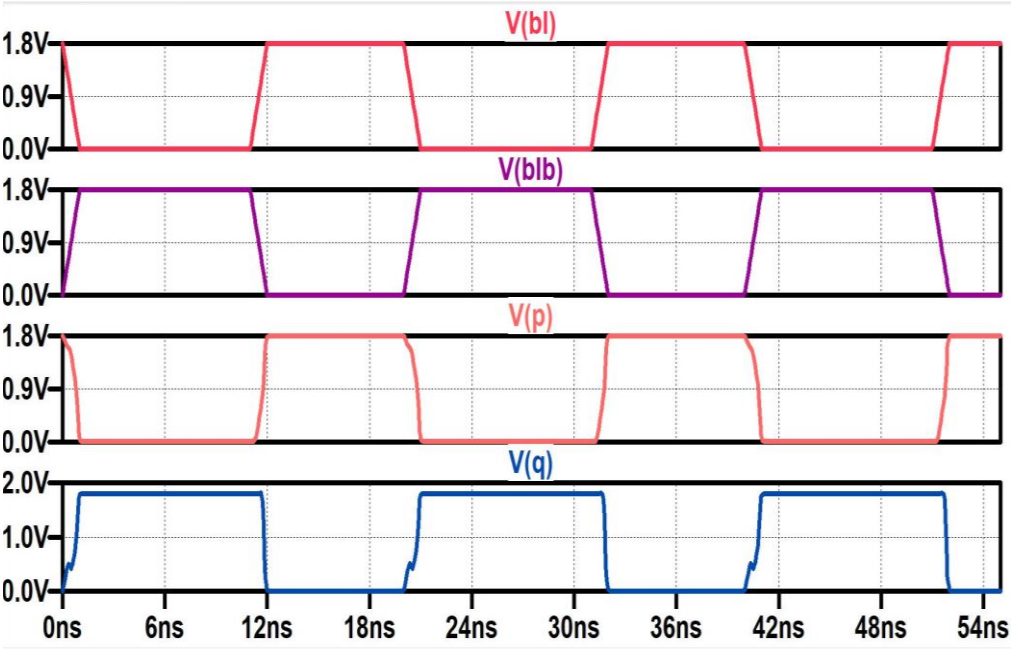


Fig. 4.7 Output Waveform of TGVLSA

The output Waveform for TGVLSA circuit functionality is presented in Fig. 4.7. Here, v(q) i.e., OUTB is follows same as bit line bar BLB and v(p) i.e., OUT is following bit line BL. Thereby confirming the working of VMSA.

4.2.4 Dual Switch Transmission Gate Voltage Latch SA (DTG-VSA)

Na *et al.* [9] reported dual switch transmission gate voltage latch SA DTG-VSA. To depreciate the power consumption and to remove the leakage current the (DTG-VSA) is designed. The head switch transistor M10 and foot switch transistor M10 relates to enable EN respectively in the SA to avoid leakage current. The (DTG-VSA) is depicted in Fig. 4.8. Uses of sleep switches are used to decrease leakage current [9]. The SA comprise of five PMOS and four NMOS transistors where transistor M5-M8 used to make inverter circuit, transistor M3 and M4 are access transistors. When enable (EN) is "high" and (ENB) is "low", the sleep transistors M9 and M10 Turned "ON". Assuming BL is "high" and BLB is "low". When EN is equal 0 and ENB is 1, M9 and M10 gets Turned "OFF" and transmission gate transistors [M1, M3, M4, M2) is Turned "ON". By this output node charge equals BL and BLB.

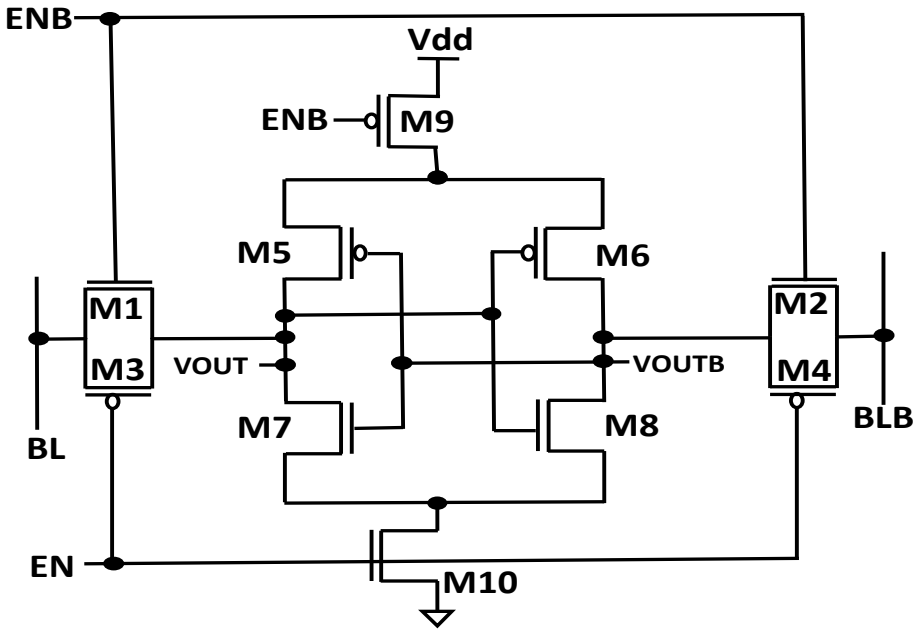


Fig. 4.8 Schematic Design of DTG-VSA

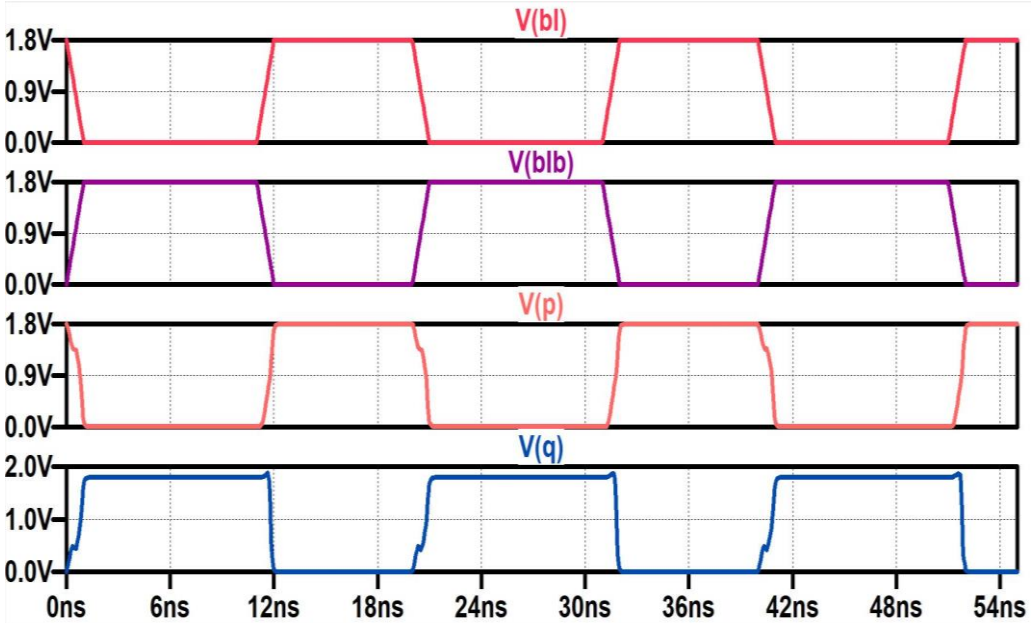
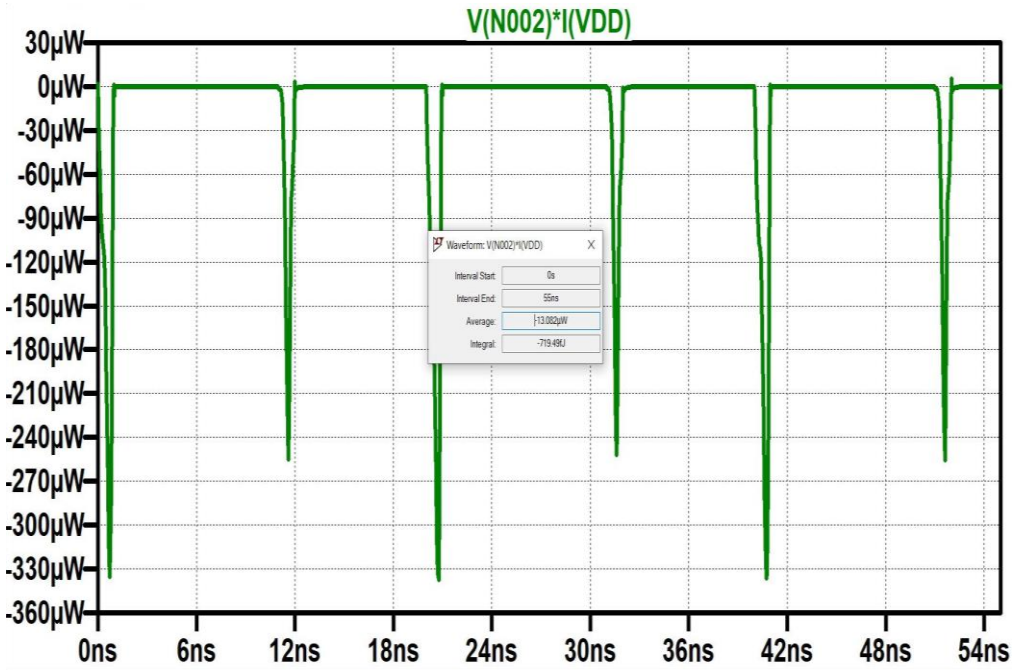


Fig. 4.9 output waveform of DTG-VSA

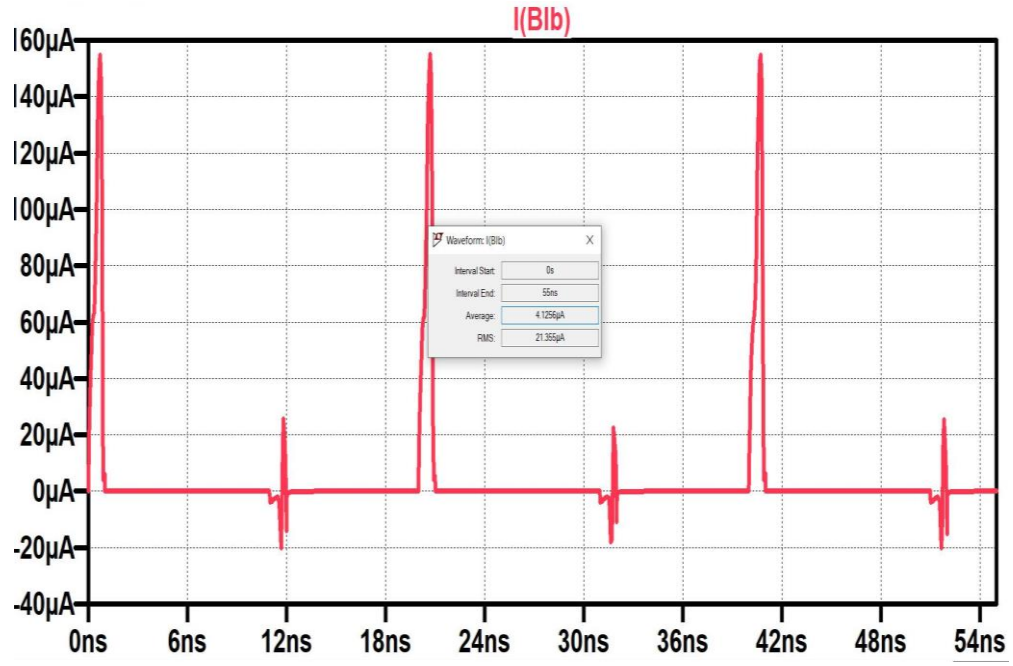
Due to dual switch and decreased leakage current the speed is expanded. Output waveform of DTG-VSA is presented in Fig. 4.9.

4.3 Simulated analytical results of Cross Coupled Voltage Mode SA topologies

The Simulated results of the existing Cross coupled Voltage mode Sense amplifier topologies are examined in this section. All the simulations have been performed using LT SPICE tool. Output waveform of power and current analysis of existing cross coupled SA topologies is shown in Fig. 4.10, 4.11, 4.12 and 4.13 sequentially.



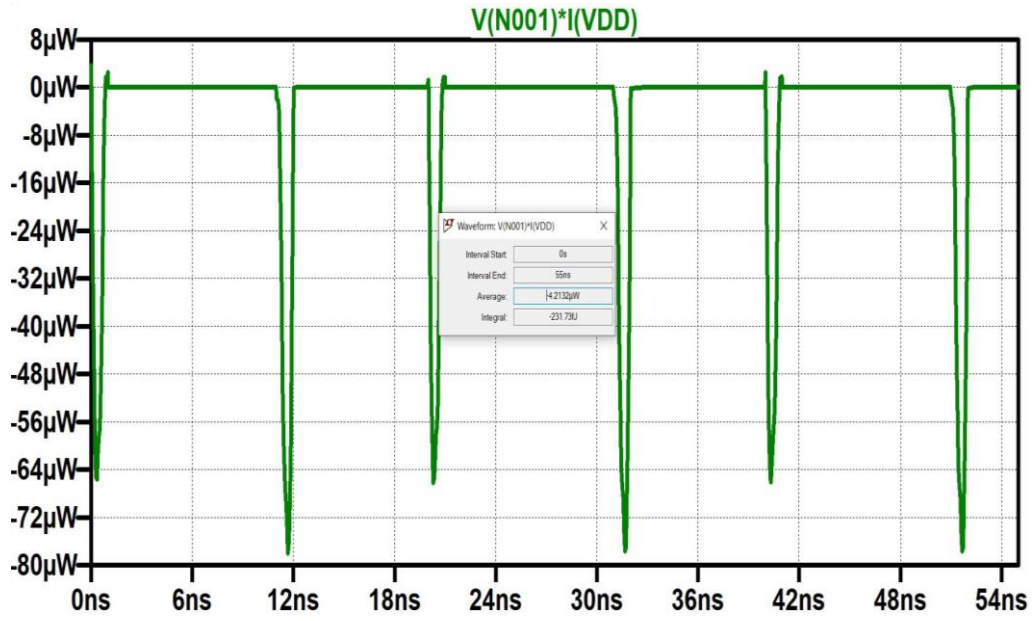
(a)



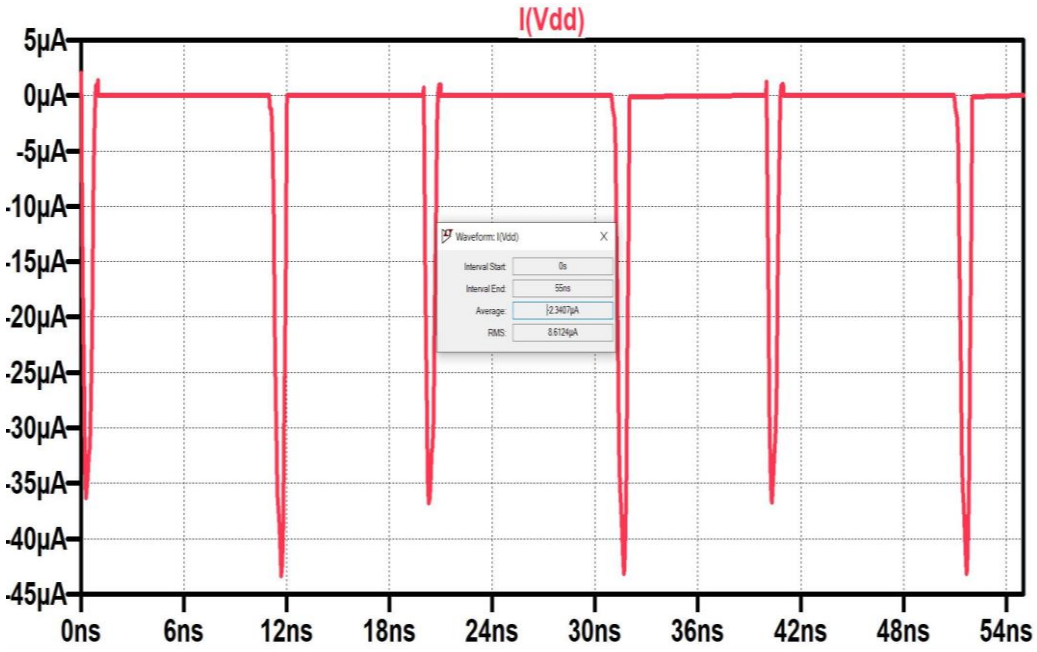
(b)

Fig. 4.10 waveform of CCVLSA (a) power and (b) current

It can be inferred from Fig. 4.10 (a) and (b) that obtained power and current for SRAM based cross coupled voltage latch SA (CCVLSA) is 13.083 µW and 4.126 µA respectively which is extremely high. So, to improve the performance the power and current analysis of DSCVMSA is examined and depicted in Fig. 4.11.



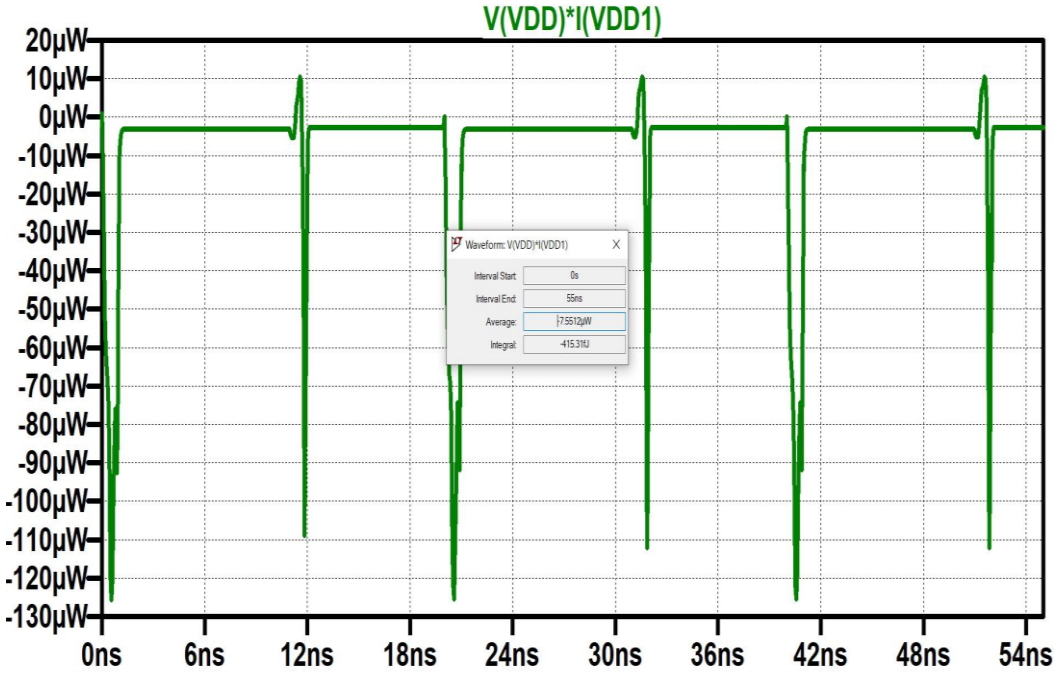
(a)



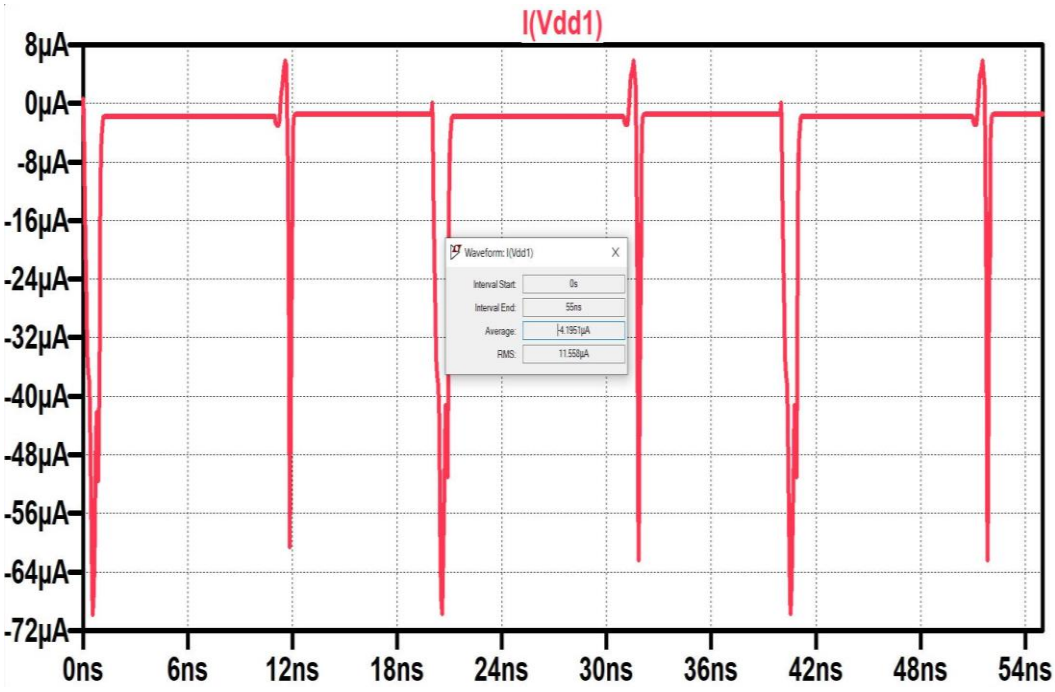
(b)

Fig. 4.11 waveform of DSCVMSA (a) Power and (b) Current

Fig. 4.11 (a) and (b) is showing that simulated power and current evaluated at 1.8V power supply for SRAM based Double switch cross coupled based VMSA (DSCVMSA) is 4.213 µW and 2.3407 µA respectively which is better as compared to CCVLSA.



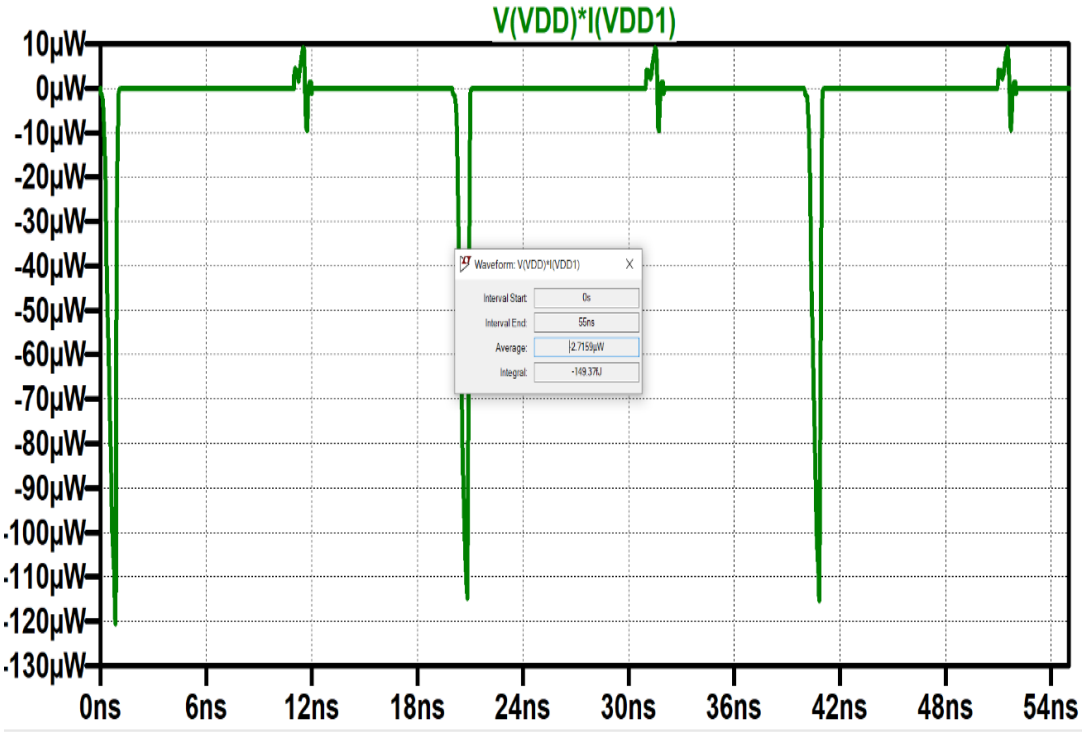
(a)



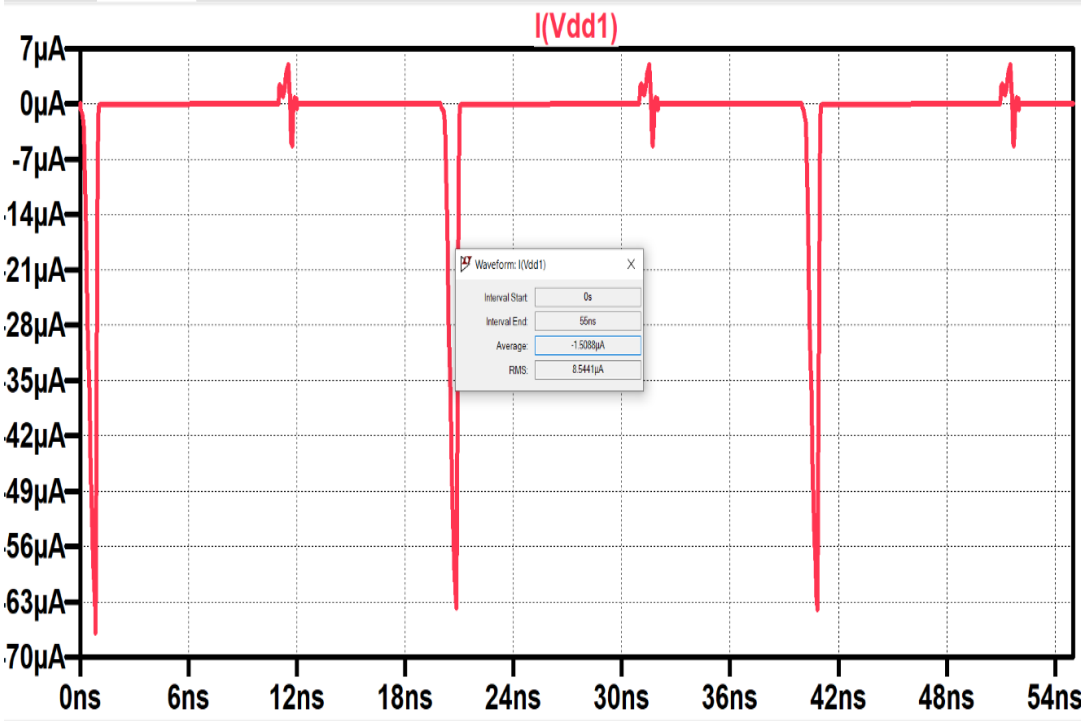
(b)

Fig. 4.12 waveform of TGVLSA (a) Power and (b) Current

Performance of characteristics like as energy and power are critical for better results while constructing memory cells. Power dissipation should be kept to a minimum when designing the SA. The circuit's overall power usage is displayed. The supply voltage is V_{dd}, and the average current is I_{blb}. [32].



(a)



(b)

Fig. 4.13 waveform of DTG-VSA (a) Power and (b) Current

For obtaining the better power and current of TGVLSA and DTG-VSA. Simulated waveform of power and current of TGVLSA and DTG-VSA is depicted in Fig 4.12 and Fig. 4.13. Power is improved in DTG-VSA.

4.4 Performance comparison of SA topologies

To obtain performance for parameters, power, current, delay and energy. The cross coupled SA topologies are simulated at 180 nm technology node with the power supply of 1.8V. The simulation results obtained are clarified inthis section.

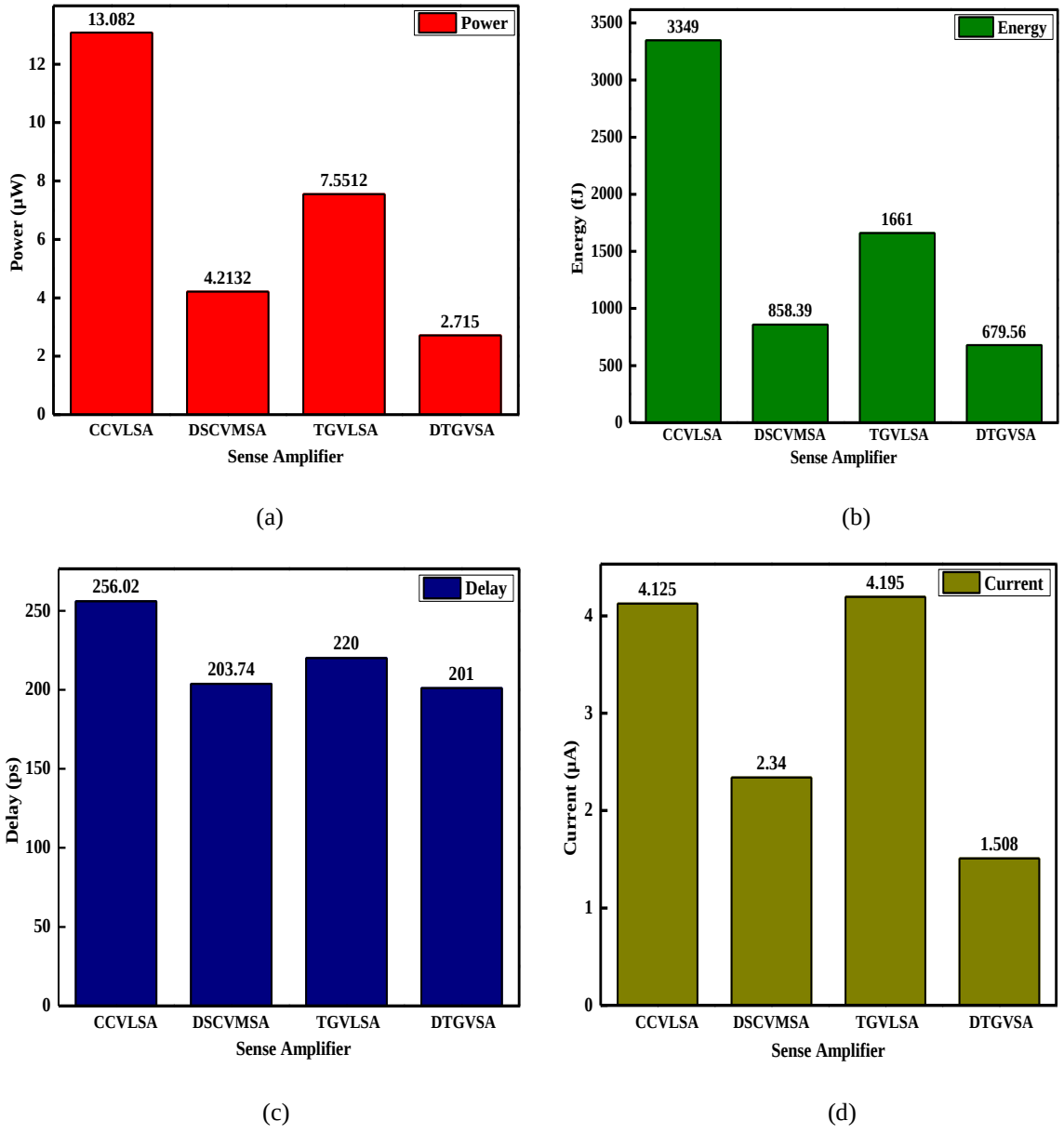


Fig. 4.14 Comparative results of SA (a) Power (b) Energy (c) Delay and (d) Current

Waveform of power, energy, current and delay is depicted in Fig. 4.14 (a), (b), (c), and (d). DTG-VSA demonstrates outstanding performance due to the dual switch and rejection of leakage current.

The Table 4.1 shows the result comparison of four differential amplifier topologies described in section 3.5.

Table 4.1 - Comparative result for cross coupled SA topologies

Sense Amplifiers with Power Supply 1.8V	Power (µW)	Energy (fJ)	Delay (ps)	Average Current (µA)	No. of Transistors
CCVLSA	13.082	**3349**	**256.02**	4.125	7
DSCVMSA	4.2132	858.39	**203.74**	2.340	8
TGVLSA	7.5512	1661	220.00	4.195	9
DTG-VSA	2.715	679.56	201.00	1.508	10

It can be surmise from the table 4.1 that DTG-VSA shows the least amount of power and delay. CCVLSA, on the other hand, has 10% higher outcomes in terms of power and latency. DSCVMSA also outperformed CCVLSA and TGVLSA, because its power is around half that of TGVLSA. According to these findings, double switch sleep transistor circuits performed better.

4.5 IMPORTANT OUTCOMES:

In this chapter the design and analyses of cross coupled SA topologies are simulated and compared to find best choice for best performance.

- Designing and analysis of cross coupled sense amplifier topologies – CCVLSA, DSCVMSA, TGVLSA, DTG-VSA with the help of LTSPICE tool in 180nm CMOS technology with a voltage supply 1.8V.
- Comparative results of all the cross Coupled SA topologies are depicted in Table 4.1. From analyzed simulation result DTG-VSA found to be the best choice.
- For best SA, differential sense amplifier topologies are analyzed. Too much difference between results of four topologies, and as DTG-VSA performed best due to double switch then modified design with dual switch is a good idea of research.

CHAPTER 5

MODIFIED SENSE AMPLIFIER

The primary function of SA is to detect data stored based on the discharge in bit line voltages; it amplifies the small voltage difference to acceptable logic levels, allowing the data to be displayed suitably by logic apart from the memory. The basic MOS differential voltage sense amplifier circuit has all of the parts required for differential sensing. A differential amplifier amplifies small signal differential inputs into a big signal single ended output.

This chapter is organized in following sub-sections:

- The basic design concept and functioning of a Level Restoration Circuit (LRC) are discussed in Section 5.1.
- In section 5.2, the design of the modified sense amplifier is detailed, as well as performance analyses and comparisons.
- The modified sense amplifier's results and discussions are found in section 5.3.
- The important outcomes of the improved sense amplifier are discussed in Section 5.4.

Both memory access time and overall memory power dissipation are influenced by the performance of sensing amplifiers. As memory capacity grows, bit line capacitance grows as well, making memory slower and more energy hungry. A sensing amplifier is an active circuit that lowers the time it takes a signal from an accessed memory cell to reach the logic circuit at the memory cell array's edge and transforms arbitrary logic levels on a bit line to the digital logic levels of peripheral Boolean circuits. The ability of a differential amplifier to reject common noise and increase actual signal distinctions determines its efficacy. Basic differential voltage amplifiers are not employed in memories because of their poor working speed at high power. [35-37].

The differential SA is typically used since no static current passes through it and is present after the latches, resulting in a power reduction. They are also genuine and straightforward. Differential sensing, on the other hand, covers the majority of silicon area. Nonetheless, it is largely about designs. Using differential SA, it is possible to combine exceptionally high packing density with low power consumption and a reasonable access time. The CMOS cross-coupled inverter pair is frequently used as a fast and reliable sensing amplifier. To achieve a quick sensing operation, positive

feedback is used. The offset of the cross-coupled pair used as a sense amplifier has been thoroughly investigated. A research that considers these devices can provide various design insights into how to minimize their impact on the performance of the sense amplifier. So, to achieve the best performance, in this chapter a modified Cross coupled Differential sense amplifier with double switch and based on level restoration circuit technology is analyzed [38].

5.1 Level Restoration Circuit

A level restoration circuit (LRC) serves a voltage swing from a low to high valid logic level. When a typical CMOS inverter is used to convert the low-swing signal to a full-swing signal, the stand-by power consumption keeps rising. As a result, a Level Restoration Circuit (LRC) must be employed as a receiver to properly convert the low-swing signal to a full-swing signal without causing excessive short-circuit DC current. The circuits aren't fast enough, and there's a lot of short-circuit dissipation, despite their widespread use due to their simplicity. Fig. 5.1 presents basic level restoration circuit with pass transistor logic [39].

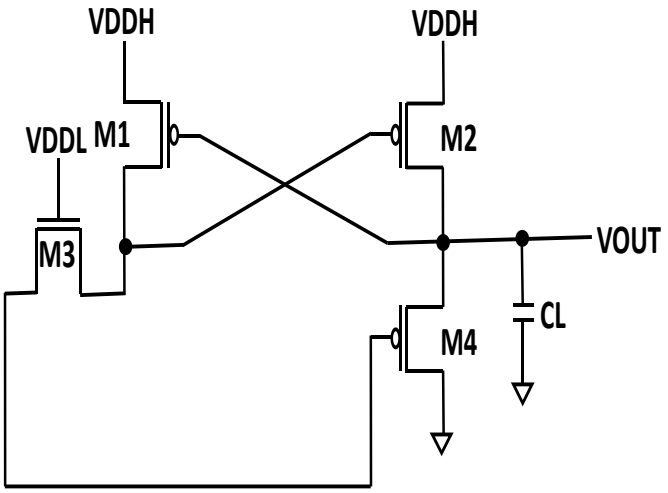


Fig. 5.1 Basic LRC with Pass Transistor Logic

These circuits are generally adopted due to their severity and presents a valid volume of short circuit dissipation because of positive feedback transistor M1. Level restoration circuits are used in MOS logic designs as they supply low to high valid logic level of Voltage swing in reaction towards an input signal in distinct to high voltage signal to low logic signal range. Dual voltage with swing restoration logic is used.

5.2 Modified Sense Amplifier

A dual-voltage dual-tail level restoration voltage latch sense amplifier (DVDTLR-VLSA) including two sleep transistors is reported in the chapter. The schematic design of modified SA consists of ten transistor is depicted in Fig. 5.2. The circuit designing of modified SA is same as double switch cross coupled VMSA, only two additional PMOS transistors M1 and M2 are attached. Also, there are two division of circuit connected to VDD. The DVDTLR-VLSA amplified the bit line voltage difference ΔVBLB and ΔVBL. Use of level restoration circuit and double switch inn voltage latch sense amplifier forms the improved modified design of sense amplifier as presented in Fig. 5.2. The working of access transistor, driver transistor and load transistor are same as conventional cross coupled VMSA.

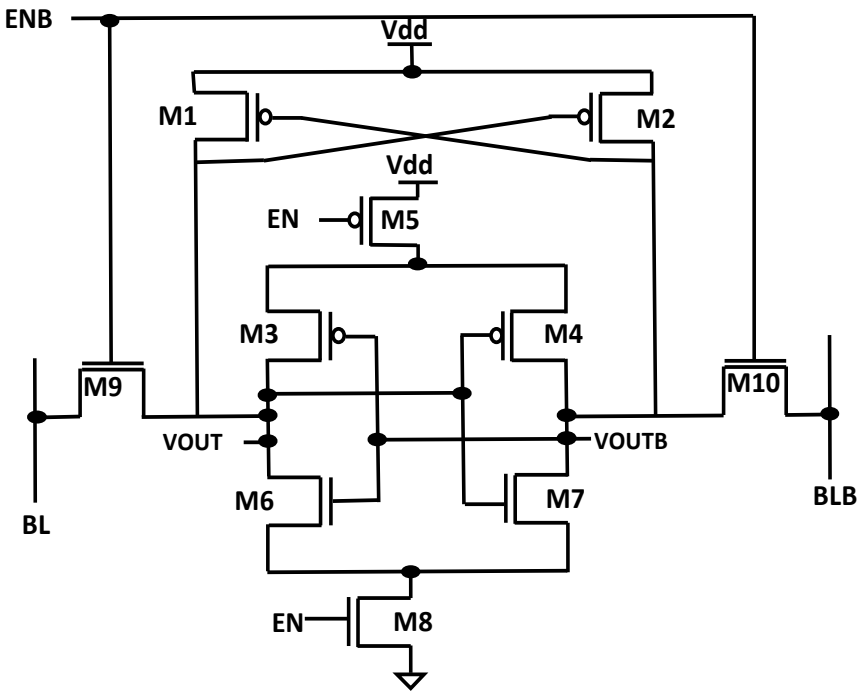
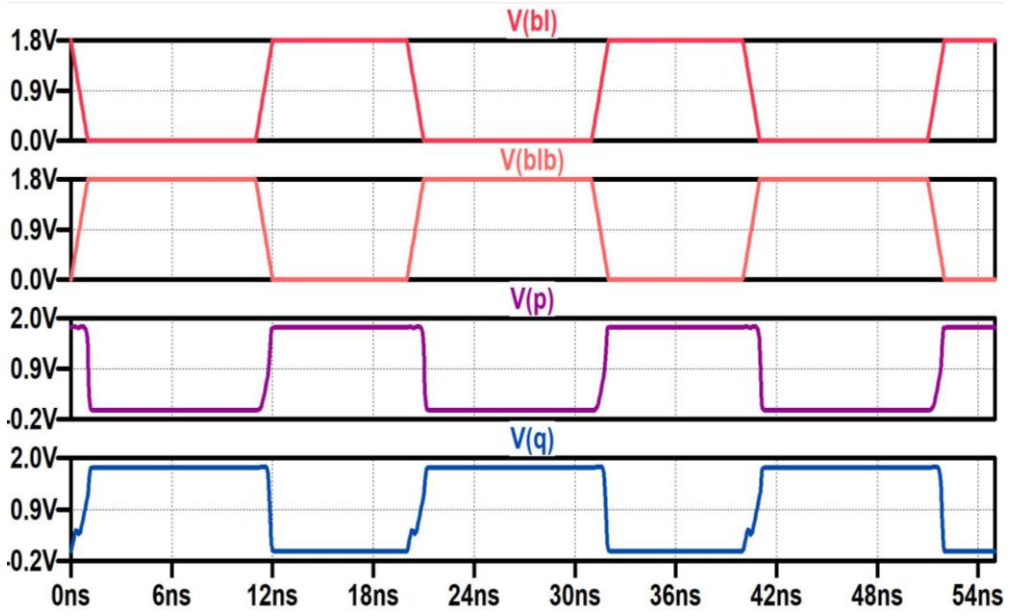


Fig. 5.2 Schematic Diagram of Modified Sense Amplifier

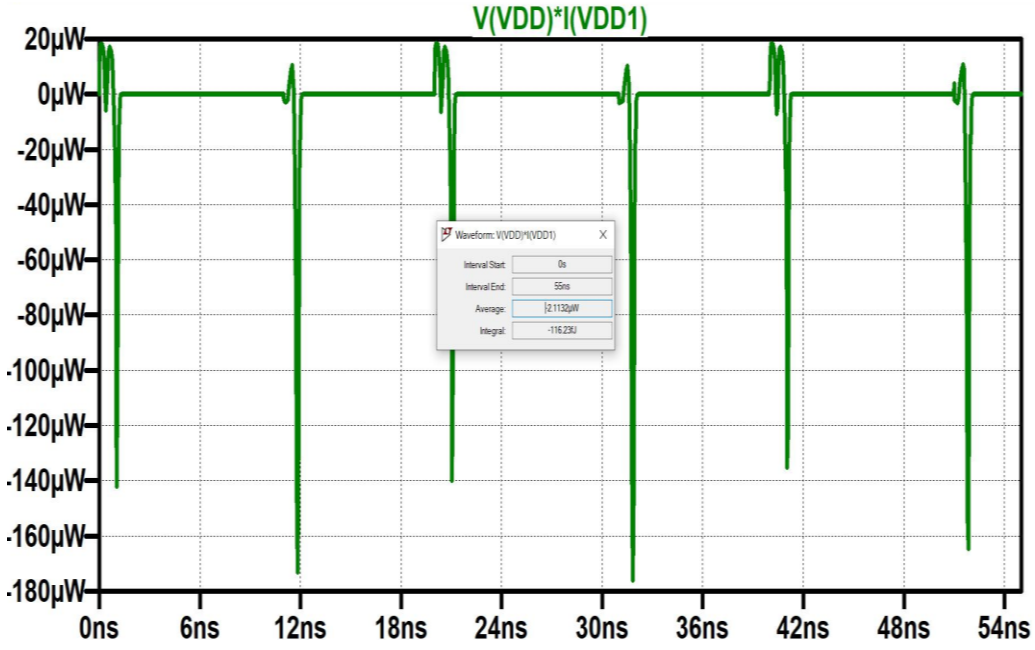
When EN is “1” and Enable bar signal ENB is “0”, the enabling transistors M8 and M5 Turned “ON”. Assuming (BLB = “0”) and (BL = “1”). While ENB = 1 and EN = 0 and sleeping transistor gets turned “OFF”. This is used to charge output nodes.

5.2.1 Performance Analysis of modified Sense Amplifier

Section 5.2 examined the Simulated results of the modified SA. All the simulations have been performed using LT SPICE tool in this section. In Fig. 5.3 (a) output functionality of modified SA is presented. When Enable signal is high and bl is also high then output out p follows the bl. Similarly, when ENB is active low and bit line bl is high the output out q act in accordance with blb. By this waveform working of SA is being confirmed. In Fig. 5.3 (b) and 5.3 (c) power and current waveforms are presented respectively. Power dissipation is an important and emerging field nowadays. The main complexity is not power dissipation, but the appropriate operation and output of the circuit. The low power is significant because if the power is too high, a cooling system will be required.



(a)



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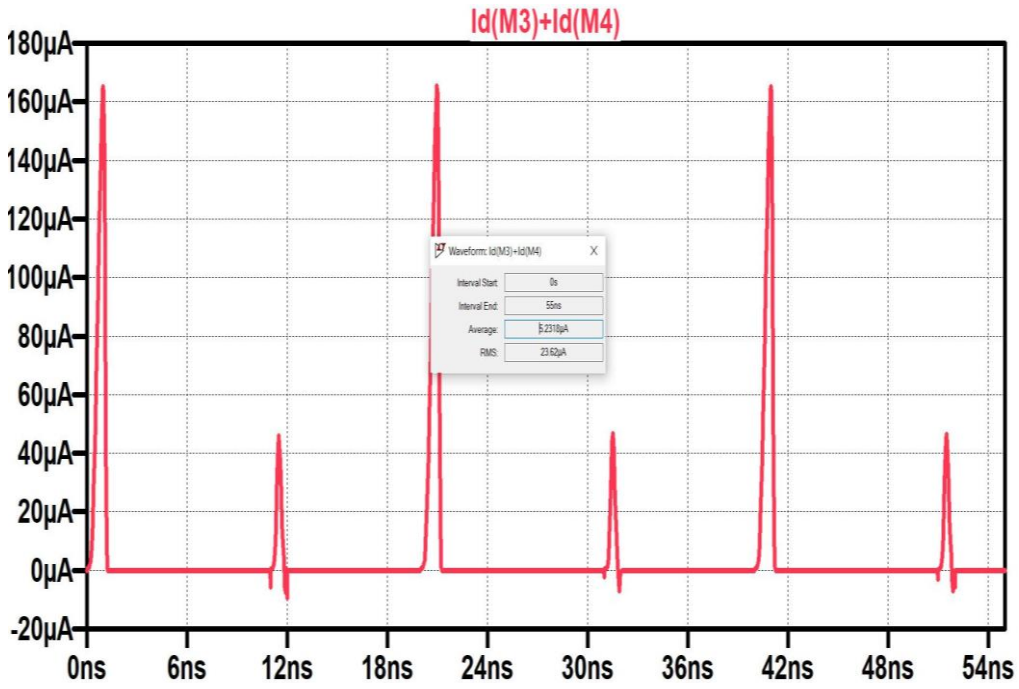

(c)

Fig. 5.3 Output Analysis of Modified SA (a) Functionality (b) Power (c) Current analysis

Power is a critical parameter nowadays. The low power is important to avoid supplementary system required for cooling. Also, these are created portable problem [40]. Thus, cost of the systems is raised due to additive system.

5.2.2 Effect of sleep Transistors on Modified SA

One among the low power technique used for vlsi circuits is power gating. A sleep transistor is a high Vth PMOS or NMOS transistor that connects the permanent power supply to the circuit power supply, also known as the power supply and “virtual power supply” or connected to ground. It is used to save the power by turned off the switch of the unused portion of circuit. A power management unit controls the sleep transistor, which turns on and off the circuit's power supply. PMOS and NMOS transistors are used as power switch. Another name of power switches is sleep transistors. NMOS and PMOS are used as power supply rails as Vss and Vdd respectively. Even though sleep transistor concept is simple, designing and developing an optimal sleep transistor is difficult due to the numerous consequences that the sleep transistor and its implementations have on design performance, area, overall power dissipation.

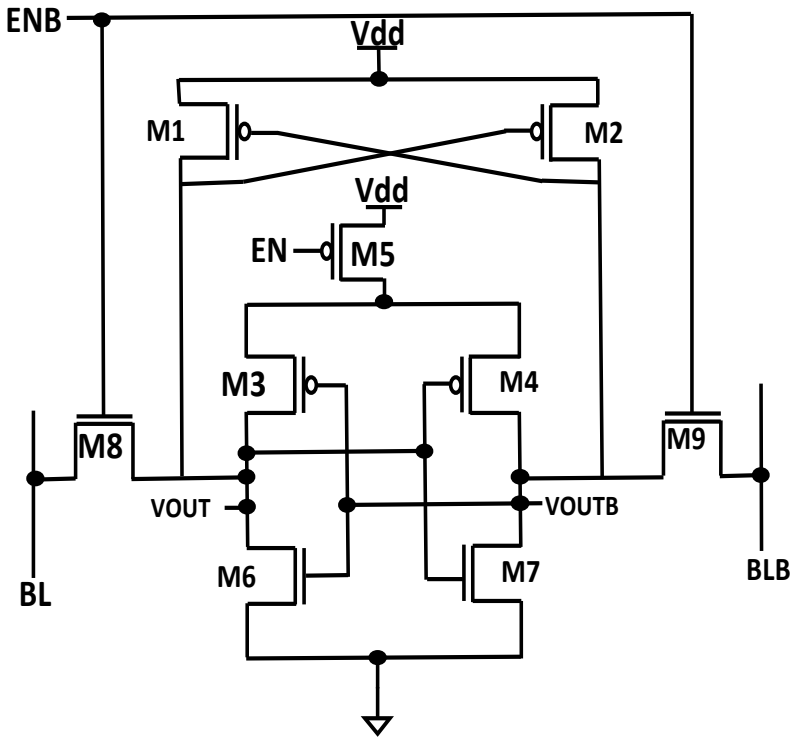

Fig. 5.4 Modified SA without Bottom Sleep Transistor

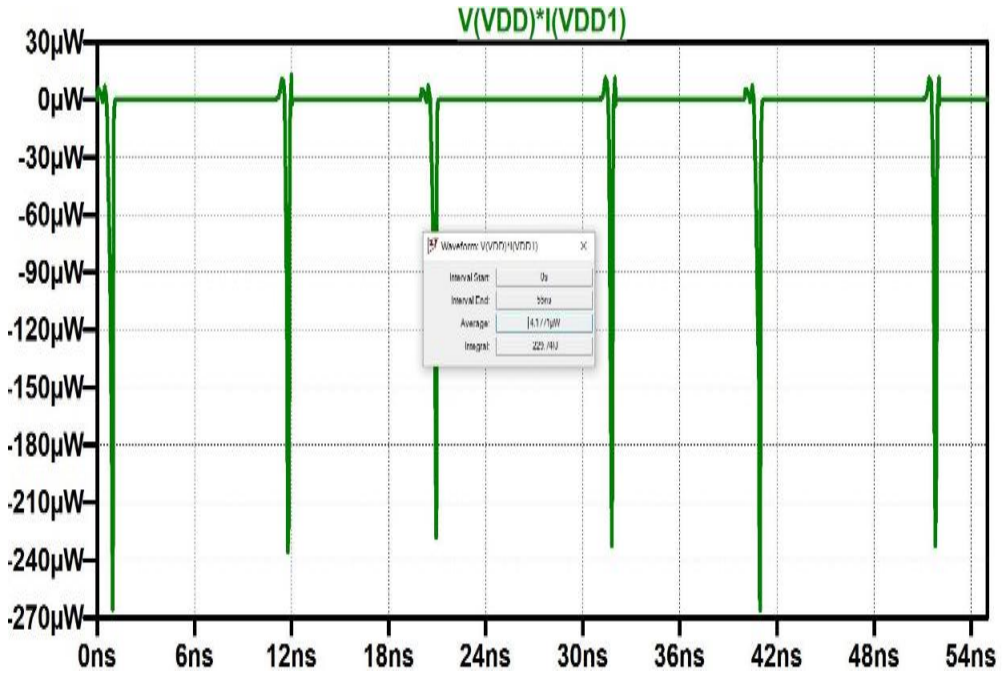

Fig. 5.5 Power of Modified SA without bottom sleep transistor

Kanika *et al.* [42] reported impact of sleep transistor on SRAM. In Fig. 5.4 and Fig. 5.5 shows the bottom sleep transistor is removed from the modified SA and power of modified SA without bottom sleep transistor. After removing bottom sleep transistor, we get power and delay as 3.7 µW and 256.78 ps respectively.

Table 5.1 shows the comparative result of SA with or without sleep transistor.

Table 5.1- Effect of Sleep Transistor

	Power (µW)	Delay (ps)
Modified SA	2.113	262.03
Modified SA without sleep transistor	3.7	256.78

It is shown in table 5.1 that SA with sleep transistor is consuming low power i.e., 2.16 µW than that of SA without sleep transistors i.e., 3.7 µW while there is not too much variation in delay results. It is due to reduction of leakage. The NMOS transistor is attached with circuit and ground. Hence called footer transistor.

5.2.3 Dimensional Analysis of Modified SA

Speed performance of any SA can be recognized by knowing how fast the output nodes become charged. Therefore, correct designing is necessary to charge output nodes through precharge transistors in minimum time.

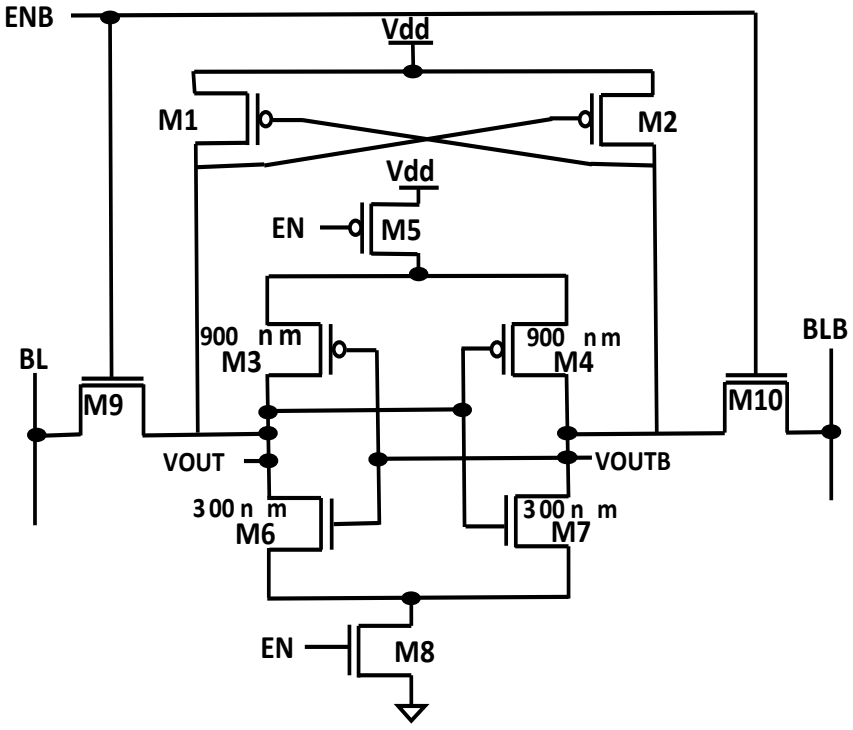

Fig. 5.6 Schematic of Modified SA with labelled aspect Ratio

In Fig. 5.6 the aspect ratio of driver transistors and load transistors is arranged to attain perfect pull-up ratio and cell ratio. Length of all driver and load transistors is 180nm.

While the w of transistors M3, M4, M6 and M7 are 900nm, 900nm, 300nm and 300nm respectively. The design is analyzed for low power, Energy, and satisfactory speed operation. SA is being proposed in such a way to store and amplify the low voltage difference to desire logic level and by shorting the time to charge output nodes.

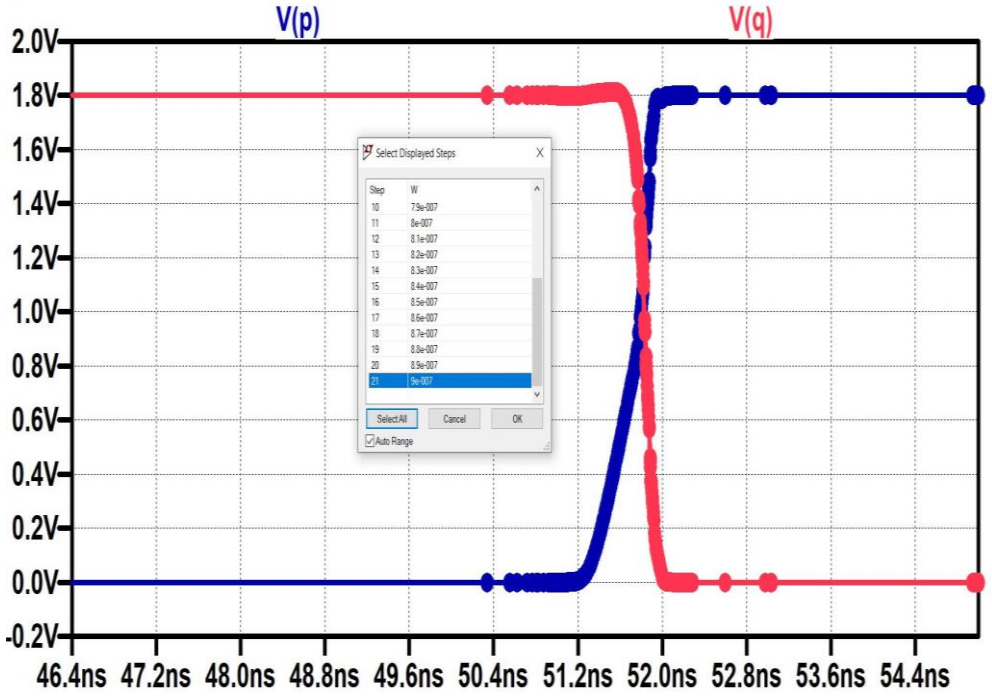

Fig. 5.7 Output Waveform When width is varying - pmos w =900nm

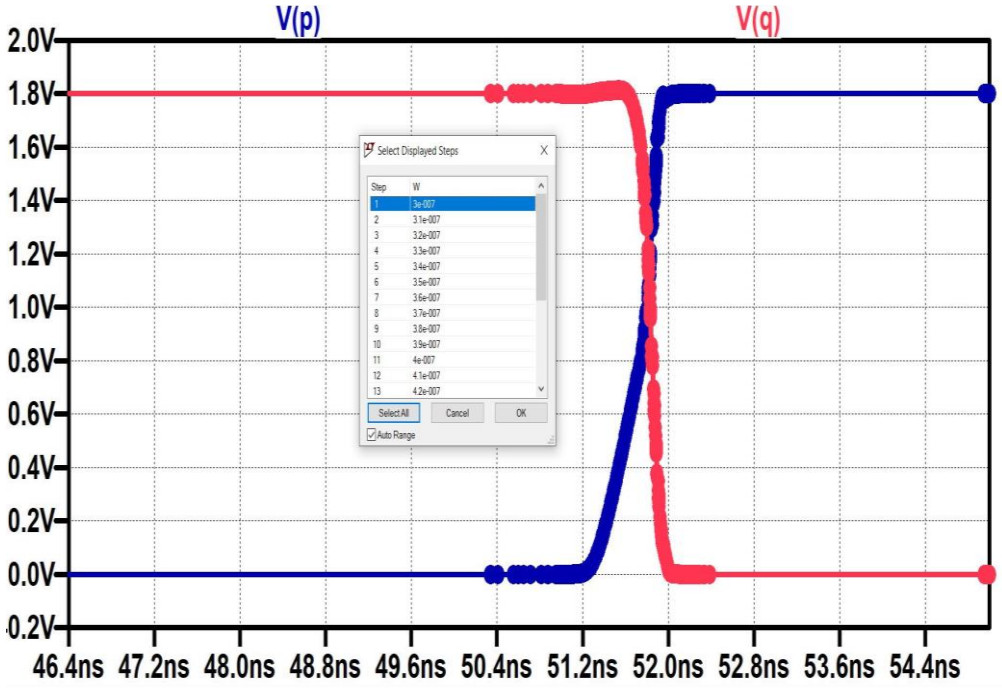

Fig. 5.8 Output Waveform When width is varying - Nmos w =300nm

It can be surmise from Fig. 5.7 and Fig. 5.8 that when the aspect ratio of driver and load transistor are 900/180 nm and 300/180 nm, the best output results are achieved by this ratio as the output node charged fast. By this method the speed of SA can be improved.

5.2.4 Temperature analysis

Sense amplifier are the heart of CMOS memories in Very large-scale integration (VLSI) industry. All VLSI circuits are designed to perform well in all temperature ranges. Temperature is an important parameter in all fields of science and technology as well as in daily life aspects. As the portable devices can be carried everywhere and used in all environmental conditions [42]. The temperature of devices can possibly surge. Hence, to examine the variation in temperature of these devices, a temperature variation analyses is analyzed to identify the possible variation for the modified SA. This is skilled to make sure the performance dependability of the cell. The temperature analysis is executed for temperature ranging from 27 º C to 120 º C shown. The output for the evaluation is shown in Fig. 5.9 and Fig. 5.10.

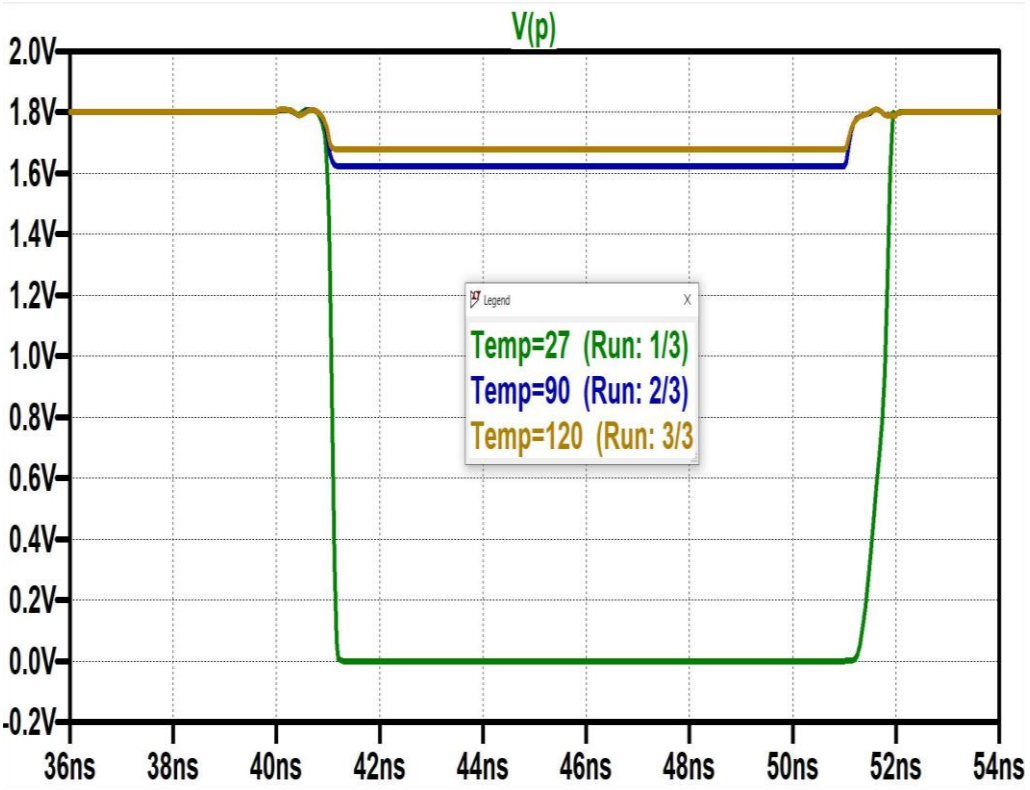

Fig. 5.9 Temperature of output P at 27º, 90º and 120º Celsius

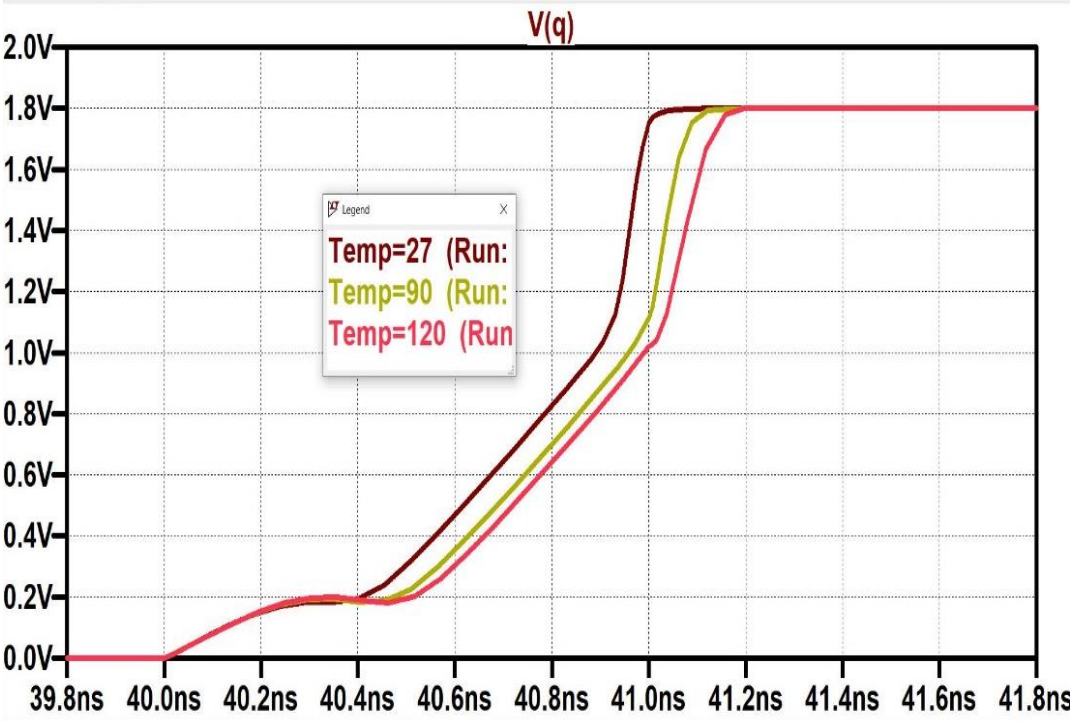

Fig. 5.10 Temperature of output Q at 27º, 90º and 120º Celsius

It can be analyzed from the above waveform; the temperature performance of the SA is showing very high variation of deflection, the best results are achieved at default temperature range i.e., 27º C so that it is showing good variation range for working in different temperature. The output voltage level of SA runs between 0V to 1.8V, which is the normal functioning range.

5.3 Results and Discussions of modified SA

Comparative performance analysis of various cross coupled voltage mode SAs with modified SA is presented in this section. The four main designs aimed in the VLSI industry are speed, delay, power, and area. chapter is summed up based on the design extent to analyze the stability within these parameters. Low power is necessary for portable devices.

5.3.1 Energy and power performance

Power consumption is a principal parameter of entire VLSI circuits. With the rising request of low power appliances, research on the power techniques of sense amplifier get popular [43]. It may be surmise from Fig. 5.3 (b) that between existing SAs present in Chapter 4, DVDTLR-VLSA has the low energy as well as lowest power i.e., 567.81fJ and 2.167 µW.

$$\textbf{Power (P) = V*I} \quad \textbf{(5.1)}$$

The product of delay and power also known as switching energy is used to calculate the energy.

$$\textbf{Energy (E) = P*D*P} \quad \textbf{(5.2)}$$

5.3.2 Delay Analysis

As the interest of high-speed circuit increases delay factor become important factor in VLSI circuits. HSVLSA has the least delay therefore the SA is best choice. Also, there is a tradeoff between other topologies presented in Table 5.2.

$$\tau_{p} = (\tau_{phl} + \tau_{plh})/2 \quad \textbf{(5.3)}$$

Propagation delay of logic circuit is defined as time needed for output voltage to hold out the midway between the 0 and 1 logic levels. i.e., half (50%) of Vdd. Results are obtained by assuming Aspect ratios of PMOS's are 4:1 and NMOS's are 2:1.

5.3.3 Current Analysis

In Fig. 5.3 (c), result analysis of current of modified Sense Amplifier is presented. Current (I) equals to power divided by voltage (I=P/V). Here we have calculated the average current passing towards the output nodes. Average current of modified SA is 6.231 µA. The output current of this design is the highest. However, in SA, electricity usage and energy consumption are the lowest. Low-power approaches such as VTCMOS and adiabatic logics, for example, can further reduce delay.

Table 5.2- Comparison of SA configuration designed at 180nm technology node and evaluated for 1.8V supply

Sense Amplifiers with Power Supply 1.8V	**Power (µW)**	**Energy (fJ)**	**Delay (ps)**	**Average Current (µA)**	**No. of Transistors**
CCVLSA	13.082	**3349**	**256.02**	4.125	7
DSCVMSA	4.2132	858.39	**203.74**	2.340	8
TGVLSA	7.5512	1661	220.00	4.195	9
DTG-VSA	2.715	679.56	201.00	1.508	10
Modified SA	2.113	553.72	262.03	6.231	10

Comparative performance analysis of various cross coupled voltage mode SAs with modified SA is presented in this section. The four main designs aimed in the VLSI

industry are speed, delay, power, and area. Results are summed up based on the design extent to analyze the stability within these parameters. Low power is necessary for portable devices.

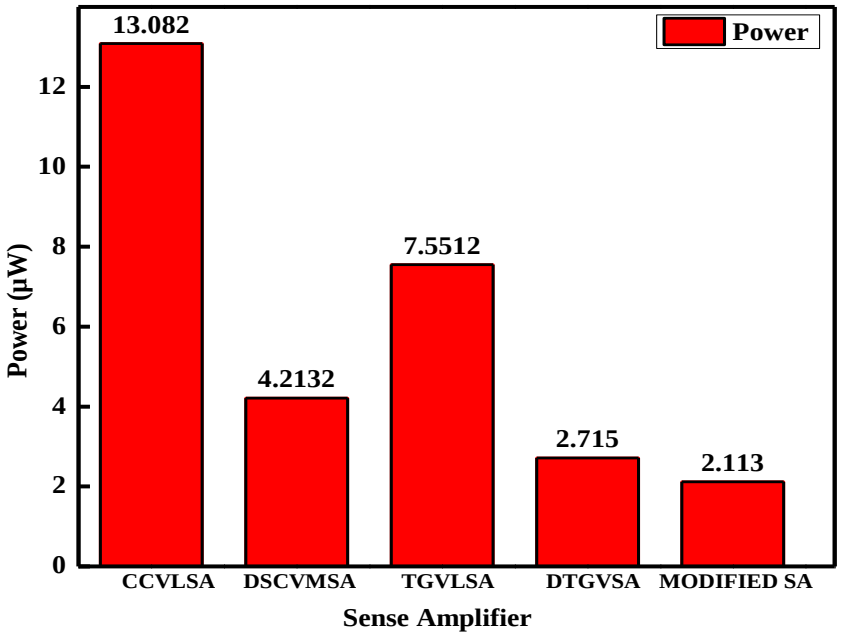

Fig. 5.11 Comparative power analysis

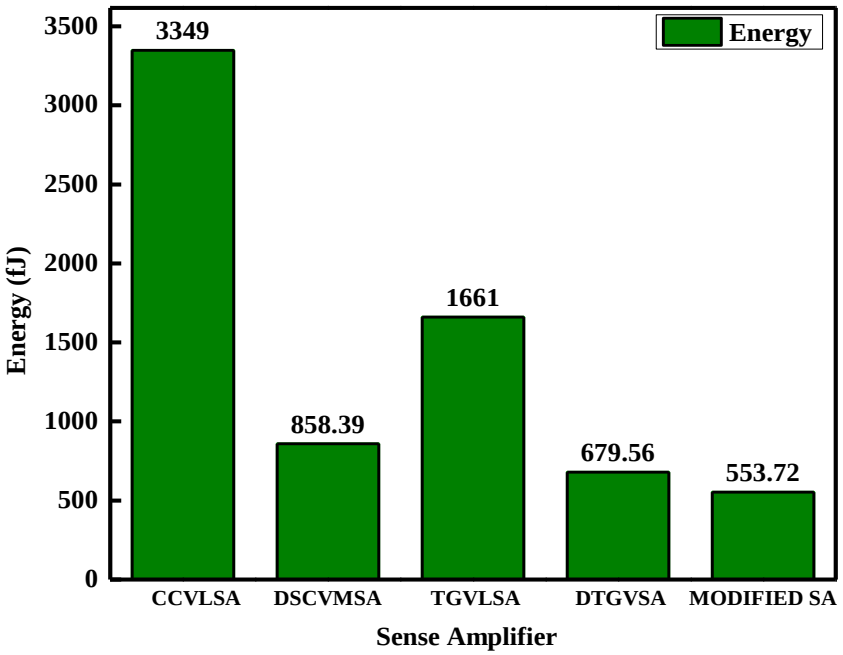

Fig. 5.12 Comparative Energy analysis

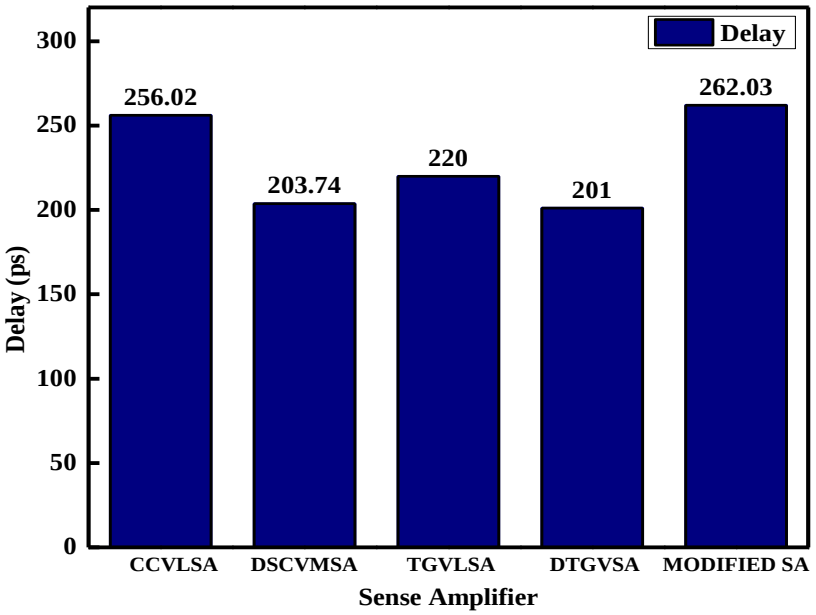

Fig. 5.13 Comparative Delay analysis

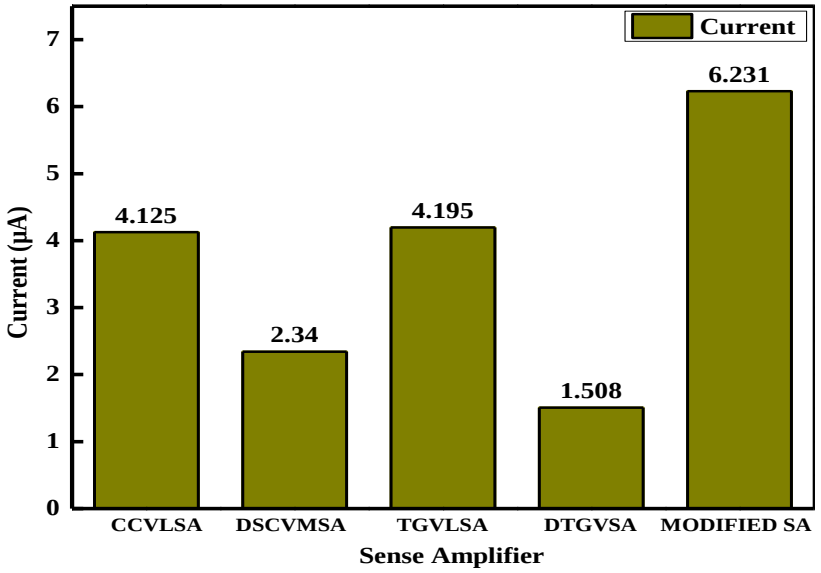

Fig. 5.14 Comparative Current analysis

Figures 5.11, 5.12, 5.13, and 5.14 show comparison data for power energy delay and current, respectively. A comparison of the current of the improved SA with existing cross coupled SA topologies is depicted in Fig. 5.14. The improved SA has a power of 2.113 W. The output current of this design is the highest. The SA has the lowest energy and power consumption. Because the modified SA's delay is like that of the CCVLSA, the modified SA performs similar in terms of speed. However, in terms of energy and delay, the modified SA performs outstanding. From this it can be said that the modified design

performed better among all existing SA. The comparative data of parameters; power, switching energy delay and current of each SA evaluated for 1.8V.

5.4 IMPORTANT OUTCOMES:

In this chapter, basic vlsi parameters such as power, energy, current, and delay are used to construct and analyze a modified sense amplifier. The performance of SA is also compared to that of other topologies.

- The modified sense amplifier has been analyzed and simulated.
- Power, delay, current and PDP have been calculated and plotted.
- Effect of sleep transistors on modified SA is analyzed. Also, temperature analysis and dimensional analysis is done for modified SA to achieve best performance.
- Our modified design shows superior performance over the existing sense amplifiers analyzed in chapter 4.

CHAPTER 6

CONCLUSION AND FUTURE SCOPE

6.1 CONCLUSION

In this thesis, the basic SA classifications of voltage mode and current mode SA have been investigated, their attributes studied, and the differences between their results provided. The topologies of the best SA between the two categories, VMSA or differential SA, are investigated further. On a 180 nm CMOS technology node, BDSA, HSDSA, HSVSA, and CLVMSA are simulated. CLVMSA has the lowest power, energy, and current of the four differential sensing amplifier topologies, with values of 10.7 µW, 591.5 fJ, and 453.85 µA, respectively. Although BDSA's performance is the worst of the four known topologies, it takes up the least amount of space due to its least transistor count. After obtaining the optimum CLVMSA (differential cross coupled sense amplifier) result. Cross coupled sense amplifiers are being investigated further to find the best outcomes among the SA currently available in the literature.

CCVLSA, DSCVMSA, TGVLSA, and DTG-VSA are four existing cross coupled VMSA topologies that have been further examined for power, energy, current, and delay at supply voltage 1.8 V, 180 nm. DTG-VSA demonstrates outstanding performance due to the dual switch and rejection of leakage current. DTG-VSA shows the least amount of power and delay. CCVLSA, on the other hand, has 10% higher outcomes in terms of power and latency. DSCVMSA also outperformed CCVLSA and TGVLSA, because its power is around half that of TGVLSA. According to these findings, double switch sleep transistor circuits performed better. This thesis reports a modified better design for the best performance based on this concept.

The performance of a sense amplifier has been improved using a modified dual-voltage dual-tail level restoration voltage latch sense amplifier (DVDTLR-VLSA). The SA is built on a 180nm technology node with a 1.8V supply. Comparative Each changed SA undergoes a transient examination with a pulse width of 55ns. Throughout the thesis, the transient time, aspect ratios, supply voltage, and technology node are all the same. The (DTLR-VMSA) has been modified primarily for high speed. The improved SA has the lowest power, exactly 2.1132 µW, the current obtained for modified SA is 6.231 µA

which is significantly improved by all other existing SAs taken into consideration. Transistor sizing is also an important way to attain delay reductions, but there is a trade-off between delay and current as reported for some SAs. according to the simulation findings. This is a significant improvement over the previous SAs examined in the thesis. Additional analyses for the DVDTLR-VLSA have been performed, including the effect of the sleep transistor on the modified SA, dimensional analysis, and temperature analyses, all of which suggest that the updated design is the best case. The power is enhanced, same as it is with sleep Transistors. The DTLR-VMSA is best approach for a low-power circuit design.

6.2 FUTURE SCOPE

The performance of a SA has been improved utilizing a modified dual-voltage dual-tail level restoration voltage latch sense amplifier, according to the analysis (DVDTLR-VLSA). The (DTLR-VMSA) has been optimized for low power and high speed. The data suggest that the modified SA's delay outcomes have not improved. Although this design has fulfilled certain aspects of the goal, a better Sense Amplifier can yet be built with additional circuit design improvements.

The following points can be used to extend and modify the SA. Improved circuit design can further reduce delay.

- The impact of process corner changes on the results of the suggested SA is not considered. As a result, proper circuit design and precise simulations eliminate the consequences of these variances.
- Yield measurements are possible.
- The layout can also be developed with the Tanner tool's L-Edit, which calculates the area for chip production.
- The Body Bias Voltage Latch Sense amplifier is made to work quickly. We employed 180 nm technologies in our design, however newer technologies such as 28 nm and beyond can be applied to improve design and analysis.
- The layout analysis can also be developed with the Tanner tool's L-Edit, which calculates the area for chip production.

There may be a lot to do in the future to improve performance.

LIST OF PUBLICATIONS

SCOPUS INDEXED, INTERNATIONAL JOURNAL

1. Divya, Poornima Mittal. "A low-power high performance voltage sense amplifier for static RAM and comparison with existing current/voltage sense amplifiers", Int. j. inf. tecnol. 2022 (ISSN: 2511-2104), Apr 2022 (Published by Springer, Scopus Indexed).
2. Divya, Poornima Mittal. "Design and Performance Analysis of High-Performance Low Power Voltage Mode Sense Amplifier for Static RAM", Advances in Electrical and Electronic Engineering, 2022 (ISSN 1804-3119 (Online), (Accepted by AEEE, Scopus Indexed).

SCOPUS INDEXED CONFERENCES

1. Divya, Poornima Mittal. "Parametric Extraction and Comparison of Different Voltage-Mode based Sense Amplifier Topologies", 3rd International Conference on Advances in Computing, Communication Control and Networking (ICAC3N), Dec 2021, (Accepted, published by IEEE, Scopus Indexed).

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