MILLER COMPENSATION USING CMOS OP-AMP EMPLYOING CURRENT BUFFER

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE
OF

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Submitted by:

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I **TANUSHRI BHAGAT** student of MTech (Signal Processing and Digital Design), hereby declare that the project Dissertation titled "**Miller Compensation using CMOS OP-AMP employing Current Buffer**" which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Report titled "**Miller Compensation using CMOS OPAMP employing Current Buffer**" which is submitted by **TANUSHRI BHAGAT**, **2K20/SPD/14** of Electronics and Communication Department, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi
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ABSTRACT

The title of the project “Miller Compensation using CMOS OPAMP employing Current Buffer” comprises of a technique in which the existing circuits of current buffer have good efficiency but because of the presence of the roots of the transfer function, its frequency response is compromised. Miller compensation is a technique for stabilizing op-amps that involves connecting a capacitance C with respect to the steps responsible for supplying the gain, often the second stage, in a negative-feedback mode. Operation amps are adaptable, certainly, yet their scope of uses is confined by their yield current restrictions. A regular operation amp can be anticipated to ceaselessly sink or source not more than 30 or 40 gain , however a few sections can deal with more like 100 gain ratio, and others will battle to give you 10. There is an extraordinary class of high-yield current enhancers, with current capacity drawing closer or in any event, surpassing 1000 as the gain. The plan strategy of the two-stage CMOS functional intensifiers utilizing Mill operator capacitor related to the current buffering circuit is introduced. Plan illustration of the proposed strategy is given. This thesis will analyze the circuits of CMOS and operational amplifiers. After which the importance of principle of Miler Compensation is evaluated and the circuit employing Miler Compensation is proposed.

The compensating capacitance in the compensation transistor falls between Vdd and the operational amplifier output in this technique, thus Moscap serves the role without the need for a metal capacitor. 10pF capacitor and 20K compensating resistor are used in this design. When we consider noise with respect to the frequencies at the higher range in the power supplied will have very less or no capacitance or inductance path at the end of the receiver, whereas miler Vdd noising figures out a way via the second step transistor CGS and the compensating capacitor $C_{c.}$ A functional enhancer, or op-amp as called, is an amplification circuit at the voltage taking into considerations the components in the outside circuit using the feed back elements like resistances and capacitances which are joined between the input and the output sides of the circuit. The elements used for feed back are the ones which are responsible for the main way how the circuit would be drawn and hence its name as "operation," and all the different types of feed back used in the circuit, using the resistance, capacitance, else considering all of them, are responsible for performing the set of applications.

For our work, we proposed this technique which uses the Miller Capacitance in a circuit which takes into account the Current Buffer circuit and this circuit has been developed with the help of LTSpice Software Version XVIII and the circuit output for the frequency response has been analysed in the results and hence, we have concluded that circuit is stable and also has a good frequency response for all the frequencies.

ACKNOWLEDGMENT

A successful project can never be prepared by the efforts of the person to whom the project is assigned, but it also demands the help and guardianship of people who helped in completion of the project. I would like to thank all those people who have helped me in this research and inspired me during my study.

With profound sense of gratitude, I thank **Mr. Rahul Thakur**, Assistant Professor, Electronics and Communication Dept, DTU, my Research Supervisor, for his encouragement, support, patience and his guidance in this research work. Furthermore, I would also like to thank all my professors, who gave me the permission to use all required equipment and the necessary format to complete the report.

I owe my deepest thanks to my family - my mother and father who have always stood by me and guided me through my career, and have pulled me through against impossible odds at times. Words cannot express the gratitude I owe them. My friends here at Delhi Technological University have been a crucial factor, without whom the thesis would have been complete one month earlier.

Tanushri Bhagat

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List of Abbreviations

CMOS- Complementary Metal Oxide Semiconductor

Op-Amp- Operational Amplifier

NMOS- N channel Metal Oxide Semiconductor

PMOS- P channel Metal Oxide Semiconductor

RHP- Right hand Plane

LHP- Left hand Plane

PSRR- Power Supply Rejection Ratio

MOM- Metal Oxide Metal

SOC- System on Chip

Cc- Compensating Capacitor

TF- Transfer Function

Chapter 1: Introduction

Functional Enhancer (operation amp) is one of the significant structure blocks in simple transmission handling and information change just as remote interchanges. In enhancement and separating applications, operation amps are utilized in regrettable input arrangement and are important to have high voltage gain. To keep away from shut circle unsteadiness, recurrence remuneration is vital in op-amp plan.

1.1 Overview

Operational Amplifiers, whose basic design has been shown in Figure.1.1, are the prime elements in today's integrated systems, and they're employed in a wide range of circuit topologies, starting from the basic calculations which can include plus, minus, multiplication and divide to complex applications which are data converters, references, filters, clocks, and data recovery circuits. The accepted notions for operational amplifier (op-amp) design have been continually challenged by continued scaling in CMOS techniques[1]. The feature size of CMOS devices is reducing, allowing for even quicker processing.

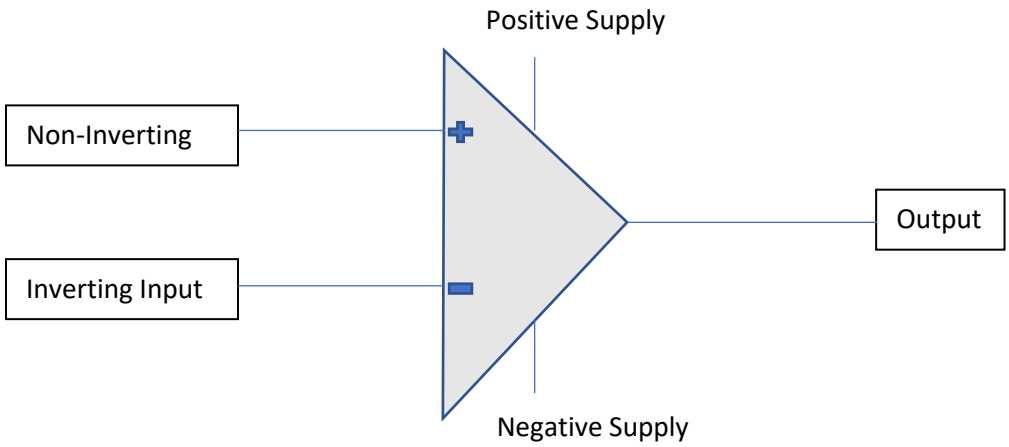


Figure 1.1: Operational Amplifier

The main aim of using the negative feedback in the circuit is to decrease the potential difference between the amplifier inputs mainly the non-inverting and inverting, which causes the output that is limited within the DC voltage and its boundaries, biasing the operational amplifier's internal transistors to operate in the forward active mode[2]. A small content of the voltage output signal V_{out}, is diverted back to the non-inverting (+) terminal of the input with the use of the feedback resistor, Rf, which leads to the positive feedback control of the op-amp. This behavior is employed in electronics to achieve an extremely

quick response of the switching application to a condition or signal, despite the fact that it is typically seen as undesirable. Bi-stability is a term used to describe the behavior of devices which show switching characteristics like multi-vibrators and gates which are used to perform the logical operations in our circuits.

The probability of instability and gain in the system which arises due to the non-inverting or regenerative feedback causes the gain to increase in a system, potentially leading to regenerative-oscillation or undamped oscillations[3]. This is one of the very important use of the positive feedback in our day to day circuits which are used for circuits maintain the timing of the circuit and maintaining the oscillation. The operational amplifier with both the types of feedback are depicted in the Figure 1.2.

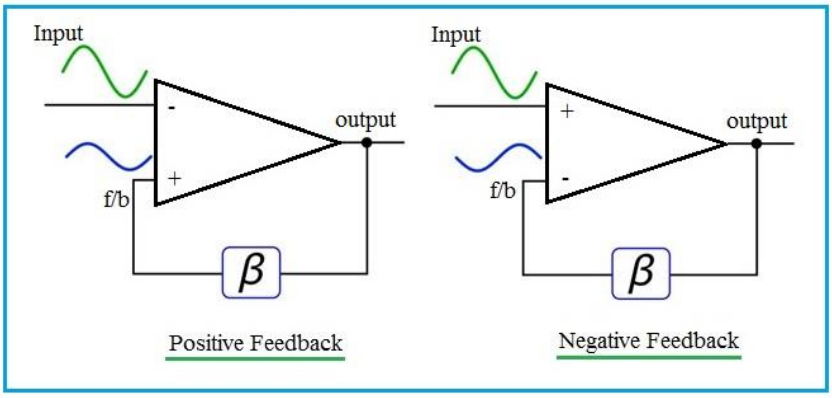


Figure 1.2: Types of Feed back[32]

Functional Enhancer (operation amp) is one of the significant structure blocks in simple transmission handling and information change just as remote interchanges. In enhancement and separating applications, operation amps are utilized in regrettable input arrangement which are very necessary for creating the need to have high voltage gain. To keep away from shut circle unsteadiness, recurrence remuneration is vital in opamp plan. For bi-stage operational amplifier which uses CMOS, the easiest pay method is to change the high addition stage with the help of a capacitor across it. This outcomes in the pole dividing peculiarities which further develops the shut circle security essentially [5]. To accomplish the increase prerequisite which causes high gain, bi-stage operation amplifier design, which has a separate addition differential stage after informational differential stage, is broadly utilized. Be that as it may, two-stage operation amp configuration is normally convoluted by the requirement for recurrence pay.

Compensation which uses the principle of Miller capacitor, which is refined by interfacing the high addition stage with the addition of a capacitor, is the most straightforward strategy to make up for a bi-stage CMOS operation amplifier. Sadly, the incorporation of Mill

operator capacitor which will likewise make a bothersome plane on the right-hand side of the plane (RHP) zero[6]. Out of these strategies, the best one is to drop this zero on the right-hand side of the plane is by embedding an invalidating n series resistor with the Mill operator capacitor. Then again, scratch-off of the bothersome zero on the right-hand side of the plane can be accomplished by taking into account a current support associated between one finish of the Mill operator capacitor and the information hub of the increase stage. Current cushion pay is a proficient procedure for both increase transfer speed item and PSRR execution when contrasted with the zero valued resistor and potential difference support strategy which utilizes a low worth remuneration capacitor[7].

Albeit the execution of the operation amp with current compensation of buffer has been accounted for and the plan methodology has been proposed, the total plan system which is applicable for the operational amplifier of this sort has not been introduced. In this Mtech thesis, we endeavor to bridge this gap by bring forward the plan method for the operational amplifier using CMOS with Mill operator pay related to the current cradle. It ought to be called attention to that dissimilar to the technique proposed in, which results in the opamp with a couple of intricate form shafts and one limited zero, the idea which has been brought forward with this methodology depends on the system which would hypothetically result in the opamp with only one genuine non-predominant post[8]. The distinctions of the shut circle conduct between these two pay conditions will be considered in the following segment.

1.1 Contribution of Thesis

This work which I have proposed in my Mtech thesis investigates the use of multi stage amplifier and how they can be modified and used for high frequency applications. This thesis compares the current buffer technology with the existing technology and it is found that it results in an open loop pole on the plane which is one the right side of the plan which makes the system unsteady. To overcome this problem which we encounter in these circuits, we propose a technique using the Mill capacitor keeping in mind that it will help stabilize the system on the right-hand side by the poles which are being of the plane and also it will provide better results at high frequency.

The technique for designing bi-stage operational amplifiers using the CMOS technology, that use a capacitor based on the Miller Compensation principle in parallel with a common-gate current buffer is described. Unlike the previously described design technique for this sort of opamp, which yields an operational amplifier based on complex conjugate poles of 2 non-dominant nature and zeros which are finite, the procedure that has been brought forward employs a design strategy that yields an operational amplifier which has only single pole which shows dominant behavior[9]. All the work that has been proposed is done using designing the circuits on LtSpice and then the design parameters and process

parameters are specified using the modules in the Spice portal and then the output graphs are obtained and the stability and positioning of the poles are verified.

The main aim of this thesis is to contribute to this domain of research which will improve the system performance for high frequency circuits and also stabilize the system as the main concern nowadays is the efficiency of a circuit and its ability to work for a wider range of frequency with no compromise. The current buffer which we use in the circuit helps us in the reaching the standard product of the desired Gain-Bandwidth, but this result is restricted to low frequencies only. To improve response of the circuit in terms of the frequency of the system we proposed the use of Miller capacitor in the circuit which will help in shifting the right hand pole of the circuit, hence stabalising the system at higher frequencies and hence making the system more reliable and efficient[10].

1.2 Outline of the Thesis

This thesis which is submitted in the fulfilment of my Master's Degree aims to contribute to this area of CMOS technology with my latest findings. Initially, I started with polishing my basics about each and every component used in this area. Since, my main aim was to work on a new technology which is more efficient and has a greater frequency response. The Chapter 2 of the thesis starts with the studying the main multi stage amplifier which is one of the most important components in our circuits nowadays and its applications are distributed over various domains. Along with explaining the circuit, focus is also laid on all the elements which are useful in the circuit and also the types of coupling which are used in the circuit. These coupling have different effects on the circuits and these applications are explained in this work.

Later on, in this chapter we focused on the Current buffer and Current amplifier circuits and their working. We also noted the basic difference in the functioning of both these types of circuits and also focused on their applications in different fields. Finally, in this chapter we studied about the Miller effect and the capacitance produced according to this effect. We derived the mathematical formula of this capacitance and the importance that it possesses in the circuits. Also, we focused on its applications in practical circuits. The thesis of this work explains the methodology of the thesis in which primarily, we focused on the Miller Compensated circuit which we have taken into consideration. We performed the small signal analysis of this circuit and calculated the Miller Capacitance[11] with the help of Miller effect and the capacitance value is changed to the miller capacitance of the circuit. Also, we noted the pole zero plot of the circuit and then plotted the poles and zeroes on the plane. Then, we analyzed the shortcomings of the circuit and the main aim of the thesis is to work on the circuit hence, improving its frequency response

Further, we discuss the working of current buffer operational amplifier and the need of using this circuit in our analysis. We discuss the main reason for using the circuit and then

we explain our wish to integrate the miller capacitance with this current buffer circuit to combine the advantages of both these circuits hence, improving the reliability of our circuit for practical applications. We discuss the Frequency compensation consideration of the circuit by analyzing the transfer function. Then we try to calculate the gain and phase of the circuit and plot it across the different range of frequencies. Also, the magnitude response of the function is plotted and the phase is calculated with the mathematical formula.

We propose an operational amplifier current buffer employing the Miller capacitance. We also compared the process and design parameters across different research papers and then the values of the CMOS parameters used in the circuit are fixed. We also discuss the need for compensation in our circuits and compare the output of the circuit with and without the Miller compensation. Finally, we reach a point where we understand the importance of compensation in the circuit and this design is proposed with the Miller compensated capacitor. The proposed technology is studied taking into consideration the magnitude response of the uncompensated and the compensated circuits and the frequency responses of the circuits. Finally, we wish to incorporate this proposed technology through the simulation on LTSpice[12]. Later on, we depict the original circuit on LTSpice and then the Miller compensated circuit. Parallelly, we analyse the outputs of both the circuits and suggest that the circuit which we proposed is better and have a good frequency response over the bandwidth. Finally, we conclude the thesis with our findings and then propose some changes which can be carried out in the further analysis. We have included all the references which were of great support throughout the project and without this contribution we couldn’t have completed this research.

Chapter 2: Literature Survey

The circuit which is proposed through this paper considers the Operational Amplifier as the core element. This op-amp is utilized in the development of different components like Multi-stage amplifiers using the different types of MOSFET. Through this section, we discussed the Multi-stage amplifiers, current buffer and current amplifier circuits. The applications of all these components and circuits are compared with the existing uses and then the new methodology has been proposed.

2.1 Multi-Stage Amplifiers

The applications which we are having in the day to day lives require an amplifier which amplifies the voltage and power into consideration, sometimes this amplification is not good even because of the use of only the single state and hence does not suffice our needs in the practical day to day uses. Finally, amplifiers which considers stages which uses multiple amplifiers and various stages are more prominent nowadays. The second stage input is coupled with the pre-stage output using a device in multi-stage amplifiers which is called as a coupling device. The common coupling devices used in a circuit are usually a capacitor or a transformer [13]. The process of joining the different stages of amplifier with the help of a coupling device is called as Cascading.

In particular applications we can use cascading to give us the accurate impedances at both the transmitting and the receiving end of the amplifier for the applications used by us. The categories in which these amplifiers are divided into different types on the basis of the amplifier categories deployed in every stage. An amplifier which takes into consideration multiple amplifiers connected together forming different stages are known as cascaded amplifier.

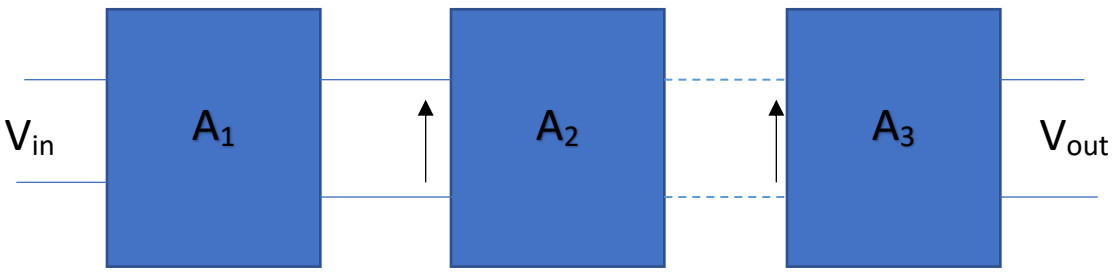


Figure 2.1: Multistage Amplifier

The mathematical equation for the above Multistage amplifier shown in the Figure 2.1 can be calculated using the formula which is derived below. This formula can be extended to the n-stages of the amplifier [14].

Output of the final stage is V_0 which can be calculated by-

$$A_n = \frac{Vn}{Vn-1} \tag{2.1}$$

$$V_0 = A_n * V_{n-1} \tag{2.2}$$

Here, in our circuit-

$$A_1 = \frac{V1}{Vin} \qquad A_2 = \frac{V2}{V1} \qquad A_n = \frac{V0}{Vn-1} \tag{2.3}$$

Finally, the circuit gain of the final stage can be mathematically depicted as-

$$A = A_1 * A_2 * \ldots\ldots * A_n \tag{2.4}$$

$$A = \frac{V1}{Vin} * \frac{V2}{V1} * \ldots\ldots * \frac{V0}{Vn-1} \tag{2.5}$$

$$A = \frac{V0}{Vin} \tag{2.6}$$

The equations 2.1 to 2.4 is the derivation of the Multi-stage amplifier which can be used to calculate the circuit gain of the circuit. At the end, this circuit gain is a ratio of the output voltage to the input voltage at the first stage of the amplifier. This current gain can also be evaluated as the product of the gains of all the stages in the multi-stage amplifier. While multiplying the gains of all the stages, the final gain reduces to the ratio of the final output to the first input[16].

2.1.1 Roles of Capacitor used in Multi Stage Amplifier

There are different types of capacitor present in the case for multi-stage amplifier. The purpose of different capacitor with their positioning in the circuit diagram is explained in this section. Figure 2.1.1 is a circuit diagram showing the circuit of a multi-stage amplifier using a capacitor[17].

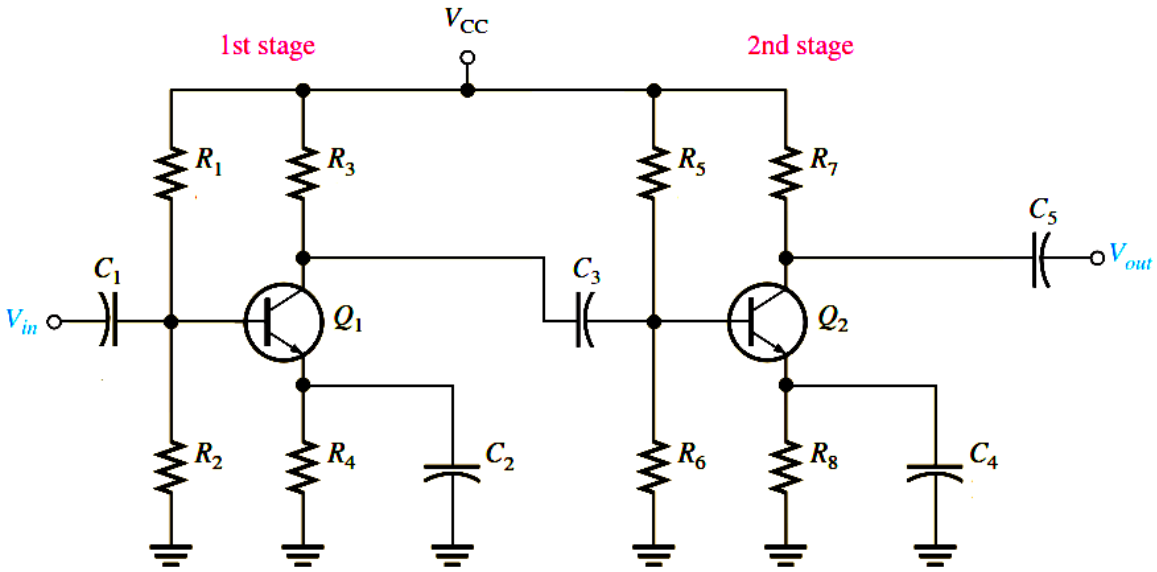


Figure 2.1.1: Multi-stage amplifier with capacitor

In the circuit we have 4 types of capacitor which have different purposes-

a) Input Capacitor, C_{in} which is placed right after the AC source in the circuit which is responsible for maintain the bias conditions.
b) Emitter Capacitor, C_E which is in parallel to the bypass capacitor.
c) Coupling Capacitor, C_C which is responsible for connecting the multiple stages in the case of a multi-stage amplifier.

Input Capacitor

The capacitor present at the input of the circuit Cin, takes an AC signal into account at the base of the transistor by coupling in the pre-stage of the amplifier is coupled to the transistor's base by the input capacitor. Suppose this capacitor Cin has become non-existent, the resistor R2 will be parallel to the source of the signal and the voltage bias of the base region will be changed. Henceforth, through the source of the AC signal Cin, will flow through the circuit present at the input which will maintain the bias conditions of the input circuit[18].

The Capacitor with bypass Emitter, Ce

The resistor at the emitter side is connected in the parallel combination to the by-pass capacitor Ce. This helps in creating a channel with minimum component of AC in the signal and helps in boosting of the channel. The feedback circuit is made with the use of R_e on the transmitting side of the circuit and in the absence of the capacitor at this stage, the voltage at the output of the circuit will reduce significantly[19]. Thus, the emitter capacitor will help in the generation of the AC signal which is having better SNR to flow at the output side.

Coupling Capacitor Cc

The coupling capacitor, C_c, is responsible for joining different circuits, in our case helps in connecting both the stages and reduces or nullify the intervention part of the DC component in the signal which helps in disturbing the movement of the point of operation in the graph and hence keeps the system stable. The reason why it is called as blocking capacitor is because of its ability to stop the DC part of the signal voltage from surpassing from it[20]. If the capacitor in the circuit is in dearth, the product of the resistance and the capacitance, i.e. the RC component tries to get in the circuit in which the resistance is present in the opposite and this will cause distortion in the upcoming stages of the circuit by disturbing the network and its connection.

2.1.2 Types of Coupling:

There are 4 types of coupling devices which are used in multi-stage amplifier. These are the methods which are used for coupling to gain better results. They are listed on the basis of the elements which are used for coupling.

Capacitance Resistance Coupling

When we talk about the types of coupling, we generally want to the start with the easiest and the famous one. As the name of this type of coupling suggests, it is very unique and basic combination of the capacitor which is present in series with the resistor. This pair is useful because of the ability of the capacitor to block the DC component of the signal and to let the AC component pass through it.

The coupling capacitor is responsible for transferring the AC from the previous stage's output to the next stage's input. To care about the subsequent stages, block the DC components from DC bias voltages[21]. In the following chapters, we'll go over the specifics of this coupling mechanism. The Resistance coupling has been shown in the Figure.2.1.2(a).

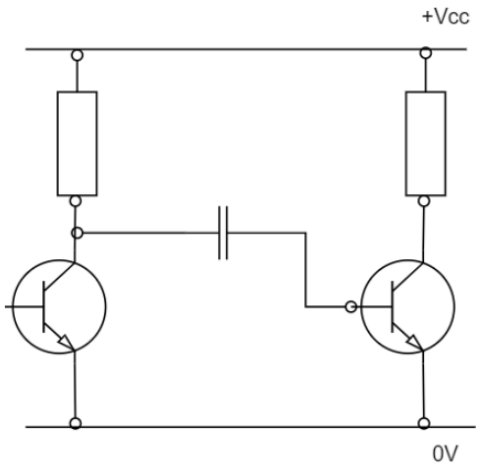


Figure 2.1.2(a): Resistance Coupling

Coupling using the Impedance

The second type of coupling is also used in practical applications, as shown in Figure 2.1.2(b) and since we know that impedance of a circuit is referred to as the combination of the inductor and the capacitor together as the elements which form the basis of coupling in this category. The inductance of this circuit is very much used for figuring out the coil which is to be used in coupling and the Z, impedance. The imaginary part of the frequency component of the signal, namely jwL, is the method in which we do the coupling of the impedance[22]. We are not referring to this one method because of its difficulty in calculation and ease of usage.

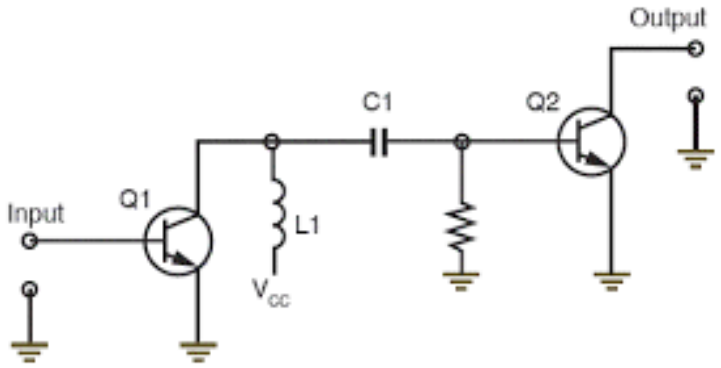


Figure 2.1.2(b): Impedance Coupling[21]

Coupling with the use of Transformer

This type of coupling in which we use the transformer as the main element for the method of coupling. According to the property of the transformer, it has the ability to surpass the AC component in the voltage of the circuit and it has to submit the output into the bi-stage input. The main use of this type of coupling is that it can perform this type of coupling without the requirement of the capacitor as an element[23]. The core which are present in the receiving end of the transformer's serves as a return for the base channel, hence neglecting the need for resistance at the base. The method of coupling is widely utilised because of its efficiency and impedance matching properties and is shown in Figure 2.1.2(c).

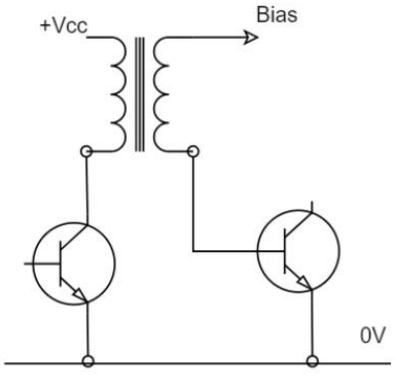


Figure 2.1.2(c): Transformer Coupling

Directly Coupling

This type of coupling as the name suggests means that we directly connect all the last stages to the next stages in the amplifier circuit as shown in Figure 2.1.2(d). When these stages are connected with each other the most important thing is that the segregation of the DC component of the signal should be connected significantly with every stage of the amplifier keeping in mind the settings for the bias of the circuit[24]. When the load is linked in continuation with the other components present in the circuit at the receiving end of the circuit, we realise that we start using this approach because of its ease in connections. For instance, headphones, loud speakers, and so on.

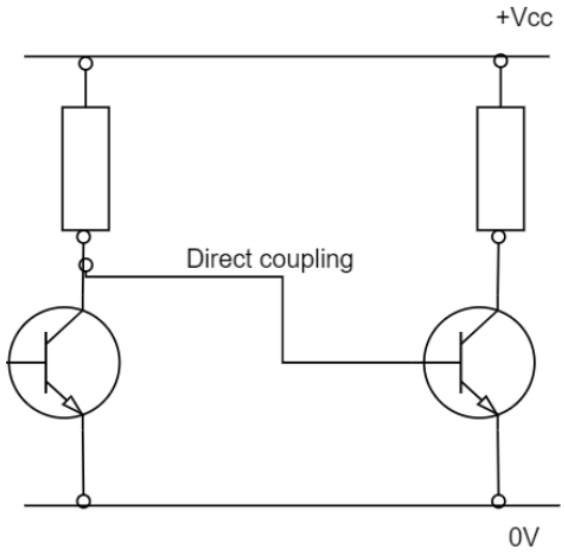


Figure 2.1.2(d): Direct Coupling[25]

2.1.3 Applications of Multi-Stage Amplifier

This type of amplifier which has multiple stages in it has applications which can be found in a variety of sectors and environments, including:

a) This type of amplifiers is also used to isolate DC signals.
b) Implementation that require more gain and flexibility
c) Increased bandwidth
d) MOSFET-based multiple stage amplifiers are also utilized in significant areas of applications.

e) These are typically used when we require them to function at an excessive speed application and also requiring voltage which high values, amplifier with multiple stages the cascading is used[26].
f) Audio Receivers.
g) Improve the signal strength and beneficial for extremely weak signals.
h) To improve the SNR of the signal and minimize the distortion.

2.2 Current Buffer and Amplifier

The circuit which makes use of a current buffer, transfers the value of I, current in a circuit with the value of impedance at the input side to be less to one where the value of the impedance at the output side is more[27]. This circuit that connects different circuits helps in keeping the following circuit from overloading the previous circuit. When the impedance of this circuit is unlimited the impedance at the receiving end is negligible, great linear response, and fast response are all characteristics of circuit with current buffer shows a behavior of ideality. A unity gains current buffer or circuit where the current behaves a follower is a circuit which buffer circuit with one gain (B=1). The current at the receiving end simply tracks or follows the input current in this case. Transistors can be used to create a current buffer (BJT or MOSFET)[28].

Its purpose is to protect signal sources from being harmed by variations on the account of the load at the output side and noting the value of current which is found at the receiving end. In maximum cases, this circuit serves a important link in the middle of low-power signals at the transmitting end (such as those maintained by the sensors) and higher-current load at the receiving end[29]. An ideal current buffer is depicted in the Figure 2.2.1 for reference.

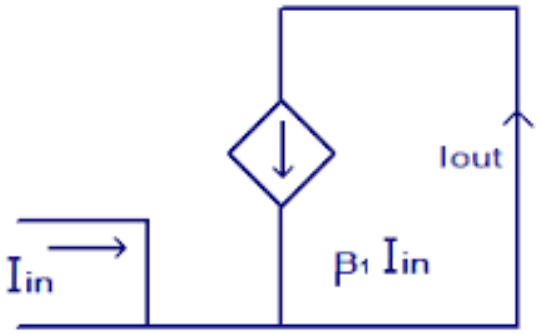


Figure 2.2.1: Current Buffer[27]

The circuit which takes into account the amplification of the current is a circuit which uses electronic components in the circuit and are responsible for the multiplication of the components of the value of current at the transmitting end and then passes it to the successive ends of the circuit. The main application of these types of circuit is amplifying the value of current hence its name[30].

A signal which is steady or an unsteady signal with respect to the constraint of time and this plot of the signal is the main criterion for use at the transmitting end. The amplification of the current in the circuit is supposed to keep a check at the other variables of the circuit mainly voltage and note that these remain constant and unchanged. This is the foremost principle of this circuit which should be followed and the circuit diagram is explained below, this deriving the formula of the output current. A current amplifier's gain is defined as the ratio of the value of the current at the transmitting end flowing through the value of current at the receiving end[31]. It is represented by the denotion Ai and has no units because it is a quotient.

$$\text{Current Gain } (A_i) = \frac{Output\ Current}{Input\ Current} \tag{2.6}$$

The circuit of a current amplifier highly relates to that of the buffer using the voltage with the slight change of the buffer voltage which is believed to have ideal characteristics and this is gonna fulfil the requirements of current that is needed by the load thus noting that the voltages at the transmitting and the receiving end remains the same. Also, noting that the circuit responsible for current amplification passes the desired current to all the following stages present in the circuit [33]. This circuit contains two transistors. Q1 and Q2 have current gains of 1 and 2. The input current which can be Iin, and Iout is often referred as the current at the load, and the voltage of the collector of the transistor T2 is +Vcc. So, with the reference to the circuit below in the Figure 2.2.2, we can derive the mathematical formula for the current at the output to be-

The value of current at the receiving end is given by-

$$I_{output} = \beta 2 * \beta 1 * I_{input} \tag{2.7}$$

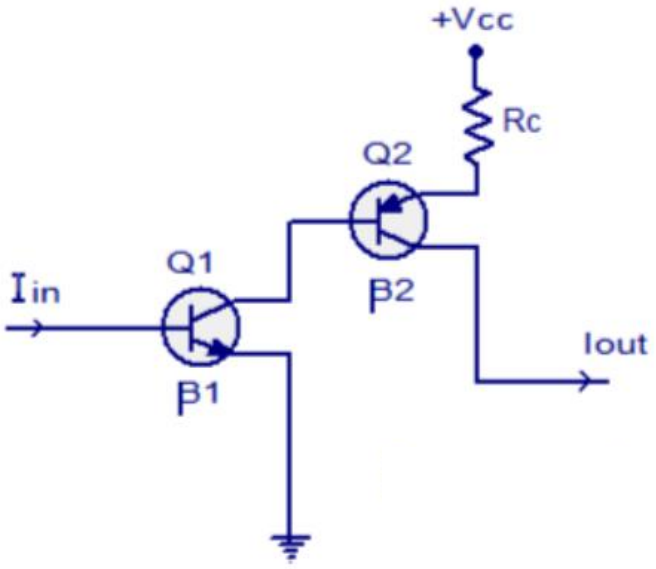


Figure 2.2.2: Current Amplifier[28]

2.2.1 Applications

The current buffer and current amplifier have different applications based on the requirements. Some of them are-

a) Current amplifier circuits are used in the sensor systems for increasing the strength of the weak signals when the signals are to be used in subsequent circuits[34].
b) The variable gain current amplifiers are used n many manufacturing systems in the industrial sector.
c) Current amplifier circuits are used to increase the signal strength of the output. E.g. the speakers are used for getting better bass as the output.

d) Current Buffers are generally used for isolating the succeeding circuits from the input current.
e) Current Buffers are also used for fluctuations in the voltage and current which are caused to the varying impedances at the output.
f) They can be used in various motor circuits.

2.3 Miller Capacitor

The functional enhancers (op amp) is a critical component in analogue processing of signals, data conversion, and wireless communications [35]. Functional enhancers are utilised in circuits utilizing the use of feedback which have a negating in amplification with addition filtering applications and require a greater increase at the voltage. A bi-stage functional enhancer layout with a imbalance distinct gaining stage post the difference stage at the side of the input is often employed to attain such a high gain need. The need for frequency adjustment, however, complicates two-stage op amp construction. Miller compensation, which involves placing a capacitor in accordance with the high increase in the transmitting stage. This is by far the more useful way for the process of compensation for a bi-stage CMOS operational amplifier.

Sadly, this method which works using introduction with the capacitor using the Miller process will result in the process of unwanted RHP zero. Enclosing the resistor having the characteristics of nulling in coordination with the use of Miller capacitor, as depicted as Figure, is one way to cancel this RHP zero. Alternatively, the buffer of current placed by the ends of the Miller capacitor with the gain stage's end of transmission side at the input is parallelly utilized for removing the unwanted zero at right hand side of the plane.

Miller capacitance is a typical approach for frequency compensation in operational amplifiers. Miller frequency compensation is the most often used frequency compensation technique today. Miller compensation, that can be refined through the process of interfacing the element C (capacitor) in co-ordination with the higher addition step, passing with the most straightforward strategy for make up for a bi-stage CMOS operation amp. Sadly, due with incorporation using the Mill operator capacitance will likewise make a bothersome zero at the right side of the plane.

The most popular strategy is for dropping this zero on the right-hand side of the plane is by embedding an invalidating resistance in coordination via a Mill operator capacitance. Then again, scratch-off of the bothersome zero on the right-hand side of the plane and this can be accomplished with the help of a currentI support associated in the middle of one finish side at Mill operator capacitance and the information hub of the increase step. Current cushion pay is a proficient procedure for both increase transfer speed item and PSRR execution[36] when contrasted with the help of a resistance having null characteristics and voltage support methodology while utilizing a less worthy remuneration capacitance value.

Albeit with execution of the operation amp with current compensation of buffer has been accounted for and the plan methodology has been proposed, the total plan system which has been carried with the use of an operational amplifier with this sort, is a new thing which has been brought forward through this paper. In this thesis, the aim is to endeavor to bridge this hole by bringing forward the plan method for operational amplifier using the CMOS with Mill operator pay related to the current cradle. It ought to be called attention to that

dissimilar to the technique which has already been discovered in, whose solutions in the operational amplifier with a couple of intricate form poles and one limited zero, the proposed plan methodology depends on the system which would hypothetically result in the opamp with only one genuine non-predominant post[37]. The distinctions of the shut circle conduct between these two pay conditions will be considered in the following segment. The following figure 2.3.1 shows the conversion of a capacitor in the feedback of an operational amplifier using the Miler theorem.

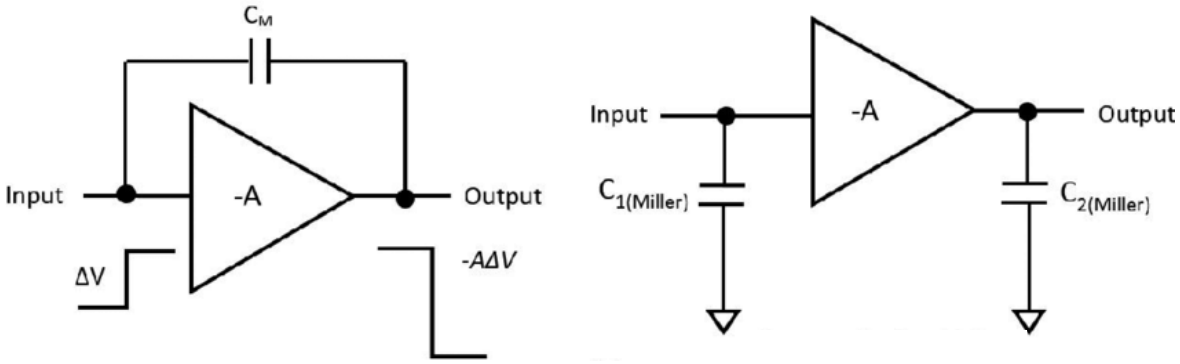


Figure 2.3.1: Miller Capacitor Circuit[23]

The Miler capacitances can be calculated from the above figure, using the formula derived in the equations 2.8 and 2.9 -

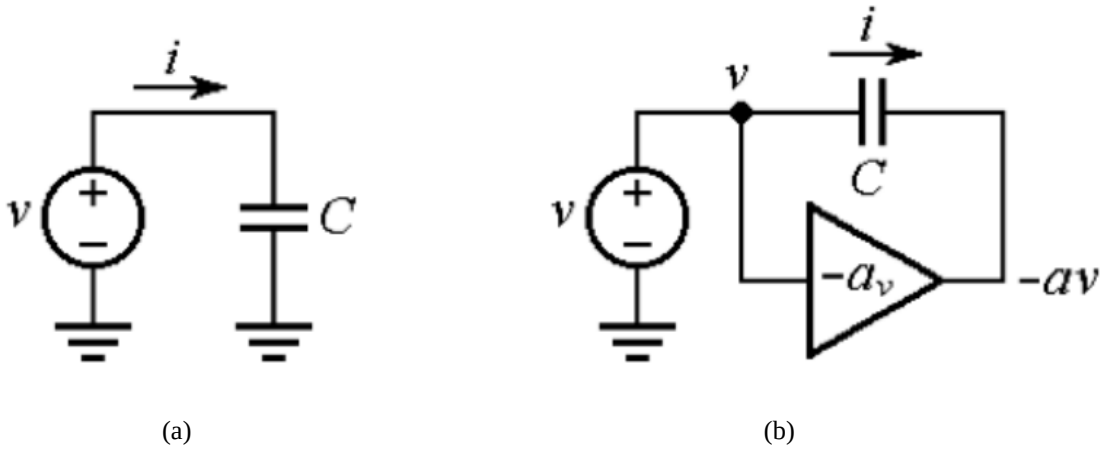
$$C_{1(Miler)} = C_M (1+ |A|) \quad (2.8)$$

$$C_{2(Miler)} = C_M (1+ (1/|A|)) \quad (2.9)$$

2.3.1 Miller Effect and Capacitance

The miller effect which was discovered by the efficient contribution of John Milton Miller's work. The capacitor which is issued for the equivalence circuit of an negating voltage amplification can be improved using the miller theorem by levelling up more capacitor or inductor in the middle of the transmitting and the receiving parts of the system. According to this Miller theorem, a system with an impedance (Z) connecting two nodes with voltage values V1 and V2 has an impedance (Z).

When this impedance is replaced with two different impedance values and linked to the identical transmitting and receiving sides to the ground, the response with respect to the frequency of the amplifier could easily be analysed with the input capacitance can be increased [38]. The Miller effect is the name for such an effect. Only inverting amplifiers exhibit this effect.



(a) (b)

Figure 2.3.2: Miller Effect and Capacitance[21]

As per the circuit (a) in Fig. 2.3.2, the current which will be generated in the circuit will be dependent on the voltage and capacitor and can be written as-

$$i = C\frac{dv}{dt} \tag{2.10}$$

Now, as per the circuit shown in Fig. 2.3.2 (b), if we try to connect the capacitor as a feedback element for the voltage amplifier with a inverting gain of $-a_v$ then the current

equation can be defined by substituting the value of voltage in the above equation and the voltage in our case would be the difference among the voltages present at the output and the input of the circuit and can be calculated the Voltage amplifier as –

$$i = C\ \frac{d[v-(-a_v v)]}{dt} = C\frac{dv(1+ a_v)}{dt}\ =\ C_M\ \frac{dv}{dt} \tag{2.11}$$

The C_M which is denoted in the above equation is termed as the Miller Capacitance and its value is –

$$C_M = (1+ a_v)C \tag{2.12}$$

$1 + a_v$ multiplies the feedback capacitance C reflected to the input. This allows enormous capacitances to be synthesized using physical capacitors that are relatively small.

Chapter 3: Methodology

The circuit proposed works on the principle of Miller theorem with the implication of the current buffer circuit. This method of compiling the properties of both the circuits is utilized in this paper to remove the shortcomings of both the circuits and then compensating the advantages of these circuits. Hence, we wish to improve the overall output characteristics of the circuit.

3.1 Working Principle of Miller Compensated Circuit

Miller compensation is quite possibly the most famous technique that is utilized to expand the steadiness of the Multistage speaker. The plan that is displayed in Fig. is the setup of Mill operator remuneration[39]. The main phase of this Operation Amp comprises of NMOS differential contributions with a P-type MOSFET using the concept of mirroring in the current load, though the subsequent step is again a P-type MOSFET normal source intensifier along a NMOS current mirror load. The remuneration capacitor is associated between the yield of these two phases, so this Pay Capacitor Cc is likewise called a Mill operator Capacitor.

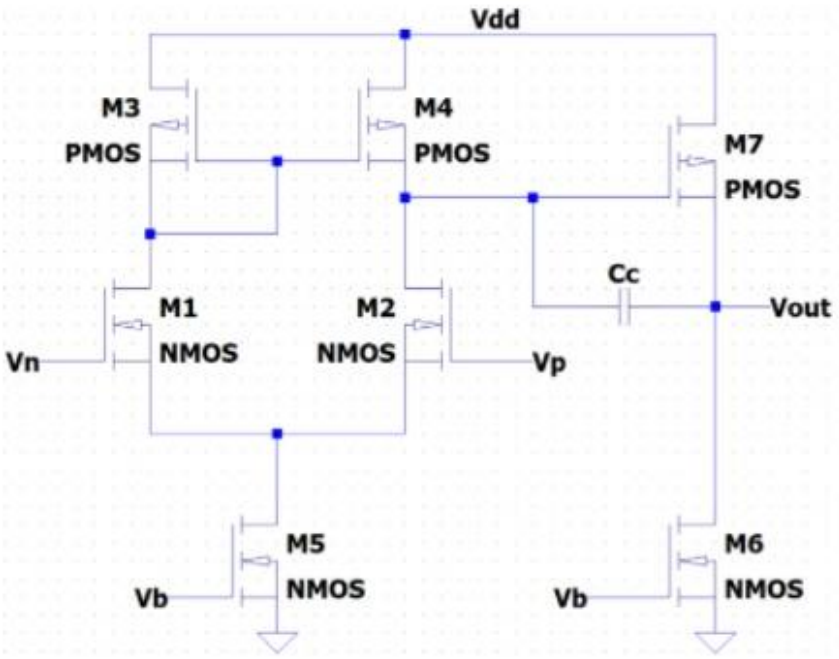


Figure 3.1.1: Miler Compensated Circuit

The circuit in the Figure 3.1.1, describes the design of a bi-stage complementary mosfet operational amplifier using a Miller capacitance and a current buffer circuit. Sadly, we forgot that one of the presuppositions drawn by us during the designing approach in [9]-[10] states the worth of the gain-bandwidth product can approximate the value of the operational amplifier's gain at the unity frequency. With respect to the data in [11], we are not accomplished to make such approaches and is invalid considering the pole which is present in the transfer function but isn't dominant enough to be considered for the frequency and substantially greater as compared to the multiplied result of the bandwidth with the gain of the system. As a result, the process in[8] must be modified in a way so the attributes of the frequency component of the constructed operational amplifier are considerably nearer to the intended digits in the comparison.

The functioning rule of Mill operator pay is to divided the posts so a higher stage edge can be reached at the solidarity gain recurrence. Be that as it may, lead to a zero on the right side of the plane (RHP) was formed because of a feed forward current caused due to the yield of the principal step to the yield of the subsequent step[40]. After the execution of the Mill operator Capacitor, the predominant post and non-prevailing shaft are accomplished because of the post parting. By utilizing nodal examination at both info (V1) and yield (V2) hubs of the normal source stage, the framework gain condition can be created, where the new places of posts and zeros can be found.

The circuit above depicts a miller adjusted bi-stage operational amplifier with a robust biasing circuit. It has a bi-stage operational amplifier and a steady transconductance biasing circuit. The primary step is commonly a difference amplifier consisting of a high gain. The amplifier having the source as the common terminal usually meets the next step's requirements, with a moderate gain. The input step of a bi-stage op-amp is preferably a difference amplification circuit, and the next step is a higher gian step driven by the amplification circuit working on the difference of the previous stage's output. With the finding in the researches held till now, it is evident that the gain of the circuit without the feedback in the case of a bi-stage functional enhancer is 2 poles underneath the value of unit. For this case, our phase shift is less than 45 degrees when the benefits of this bi-stage functional enhancers equals with the gain at the unit margin of the component of frequency. The main consequence of this circuit, a two-stage op-amp must be corrected to achieve stability. Pole splitting with the Miller effect is the most extensively utilised compensatory methodology in analogue structure circiut and its designing. Miller compensation becomes the efficient way of dealing for this method.

By lowering one pole down in frequency, the outcome of the Miller theorem results in the creation of pole whose characteristics are superior than the other ones, while shifting the other denominator up in frequencies makes the other denominator roots less effective (pole splitting). We intend to shift the pole of the system making it a system which is dependent only on the most dominant pole by removing the less one and then enhancing the TF of the system, this step is focused to get the much-desired margin in terms of phase of the system. A compensating capacitance value is summoned in the middle of output for previous step

(differential amplifier) and before the beginning of op-am in the Miller compensation technique. We can analyse the Miller Compensated principle in the system by performing the small signal analysis on the circuit shown in Figure 3.1.2.

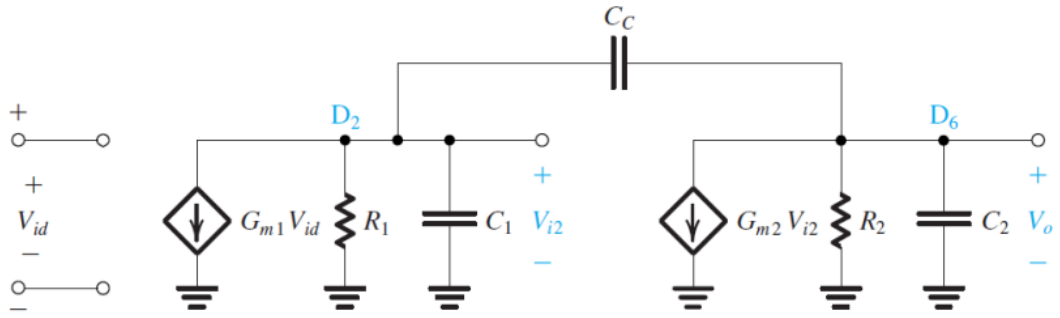


Figure 3.1.2: Small Signal Comparison of Miler Compensated circuit

Noting of equations for small signal model are-

$$\frac{V_{i2}}{\frac{1}{sC_1}} + \frac{V_1}{R_1} + G_{m1}V_{id} + \frac{V_{i2}-V_0}{\frac{1}{sC_c}} = 0 \tag{3.1}$$

$$\frac{V_0}{\frac{1}{sC_2}} + \frac{V_0}{R_2} + G_{m2}V_{i2} + \frac{V_0-V_{i2}}{\frac{1}{sC_c}} = 0 \tag{3.2}$$

$$\frac{V_0(s)}{V_{id}(s)} = \frac{G_{m1}R_1G_{m2}R_2(1-s\frac{C_c}{G_{m2}})}{S^2[R_1R_2(C_1C_2+C_1C_c+C_2C_c)]+s[R_1(C_1+C_c)+R_2(C_2+C_c)]+G_{m2}R_1R_2C_c]+1} \tag{3.3}$$

$$\frac{V_0(s)}{V_{id}(s)} = \frac{A_{DC}\,(1-\frac{s}{z_1})}{\left(1-\frac{s}{p_1}\right)(1-\frac{s}{p_2})} \tag{3.4}$$

$$z_1 = \frac{G_{m2}}{c_c} \tag{3.5}$$

$$p_1 \cong -\frac{1}{G_{m2}R_1R_2C_c} \tag{3.6}$$

$$p_2 \cong -\frac{G_{m2}C_c}{C_1C_2 + C_1C_c + C_2C_c} \cong -\frac{G_{m2}}{C_1 + C_2} \tag{3.7}$$

The equations from 3.1 to 3.7 are derived using the small signal analysis on the circuit which is considered in Fig. 3.1.2. From the small signal analysis, we have depicted the location of the poles on the plane while deriving the relation between the impedances under consideration in the circuit.

If between the desired results for the initial with the successive stages if the compensating capacitor is not present, then poles of this amplifier can be written as-

$$p_1 = \frac{1}{R_1C_1} \tag{3.8}$$

$$p_2 = \frac{1}{R_2C_2} \tag{3.9}$$

The equation 3.8 and 3.9 are the representation of the poles when the compensating capacitor is removed. This occurs due to the use of the Miller capacitance we have proposed for the existing circuit.

Because the Miller principle is capable of significantly improving the increase the continual with respect to the timing related to the compensating capacitor, a zero which is introduced on the right hand side of the plane in the bi-stage operational amplificationer due to the feedback issued in the forward loop gain of the current with the starting steps of the output and the functional enhancer's as a result of the Miller compensation technique [4]. This is an undesired result since it reduces the phase margin, restricting the two-stage

operational amplifier's maximum bandwidth. The compensating capacitor on the bi-stage operational-amplifier is substantial for certain conditions.

The pole zero plot for the above circuit is shown in the Figure 3.1.3. This plot consists of the case in which we have considered normal conditions and also the conditions using the Miler Capacitances.

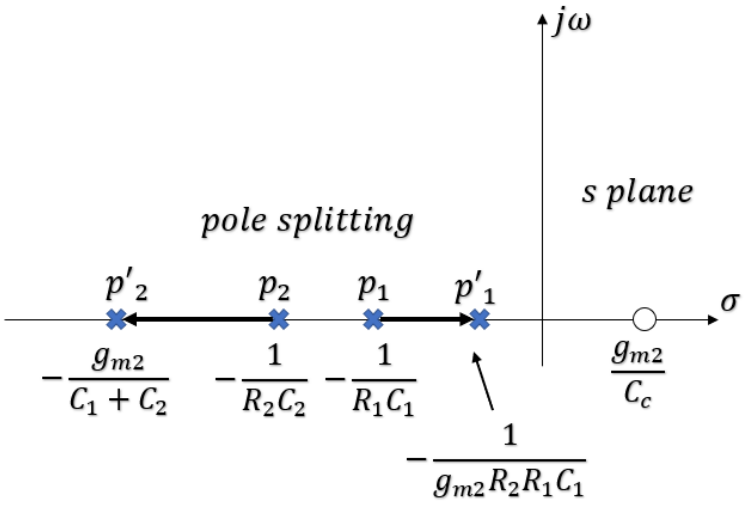


Figure 3.1.3: Pole Zero plot for Miler effect on Functional Enhancer

The denominator roots of the transmitting (in) and the receiving ends(out) are divided into categories such that, resulting in preceding and non-preceding poles, resulting in the circuit whose functioning as a system where only one root is important, as indicated on the pole-zero plot. To overcome the RHP zero generated by the Miller effect, many innovative approaches have been devised. Advanced frequency compensation approaches include the use of the value of resistance which have a nullifying effect on the principle of compensation[5]. As stated in the previous section, the goal of this thesis is to figure out the benefits of employing a compensating feedback such that it does not directly affect[7] the circuit we are dealing with but parallelly helps in dividing the multi pole system into a system which is solely dependent on only one root in the denominator of the transfer function[6].

3.2 Working Principle of Current Buffer Operational Amplifier

The compensating behavior of the circuit which uses the buffer nature of current is provided in for the purpose of correcting the pole on the right hand side of the plane in order to achieve stability and acceptable phase margin. In comparison to use of the value of resistance which has the nullifying effect and voltage bufffer approaches with the value of capacitance as a typically less number, currrent bufffer compensating technique is a very useful strategy for consideration of the product of the range of frequencies with respect to the increase in the magnitude and also the growth in terms of the performance. Various two-stage opamp design approaches are discussed.

The current buffer compensation technique is used to create a bi-stage complementary mosfet which can be utilized for all the needs with this. With a single 3.3V supply, the developed opamp achieves better gain, better UGBs, and lower voltage at the offset side with a significant reduction in the power we are consuming through its working. For stability, a bi-stage functional enhancer uses miler compensating technique, which results in a zero at the right-hand side of the plane in the circuit which is constructed without any feedback and hence the current can flow in line and cross the compensating capacitance, lowering the maximum gain-bandwidth (GBW).

Nullifying Resistance, Current Bufer, Voltage Bufer, and combination of the two with the Buffer are among the strategies used to reduce the problem and let the current to flow though the straight path. The Nullifying Resistance approach is the most popular and straightforward. MOS transistors were used to create a zero at the left side of the plane with enhanced product of the gain with respect to the range of frequencies. In contrast, the Voltage Bufer technique has a larger gain-bandwidth, whilst the Common-Gate Current Buffer technique has a remarkable gain-bandwidth efficiency and PSRR performance.

Furthermore, by using a cascode differential stage instead of a conventional differential stage, the Current Buffer technique can be improved. The successive pole, is believed to be dependent on the value of the capacitance in the nearby path and hence, limits the maximum gain-bandwidth. The figure below 3.2.1, shows the circuit diagram for a current buffer circuit which uses the operational amplifier in its circuit.

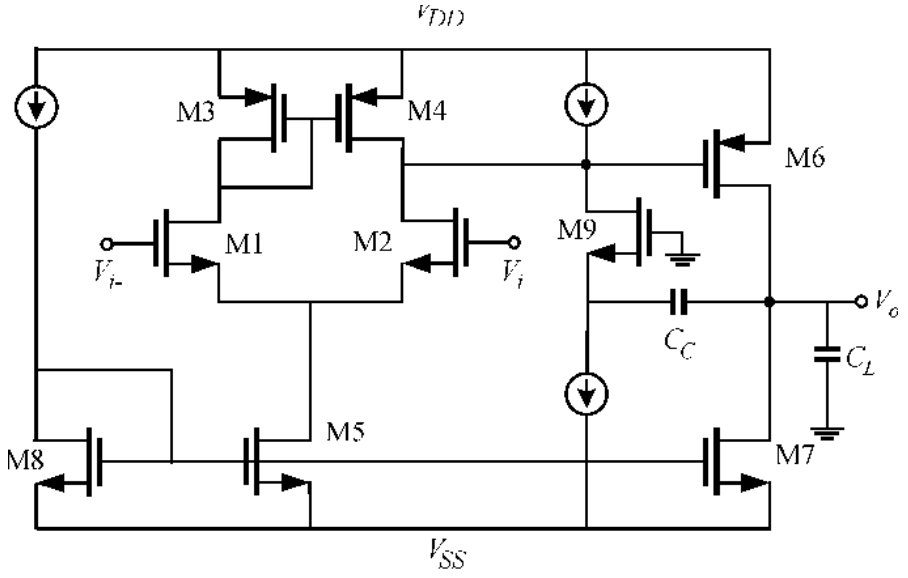


Figure 3.2.1: Current Buffer employing Operational Amplifier

This strategy improves the product of the gain along with the range of frequencies and PSRR rate of improvement. Moreover, this is also used for addressing the voltage bufer's shortcoming of reducing the amplifier output swing. This design method provides for a considerably lower CC value. The option to employ smaller CC allows for more flexibility in balancing noise performance and power consumption. Keeping into consideration the advantages of both these compensation techniques, we intend to improve the frequency response for the system we are dealing with and hence enhances the stability and reliability of the circuit.

3.3 Frequency Compensation Consideration

When endeavoring to settle a speaker with ample no of stages, the presentation of a Mill operator capacitance might make a circuit with no feedback way and zeroes at the right hand side of the plane (RHP) zero, thus putting a risk strength to the controlling circle[5]. Notwithstanding a resistor with nullifying characteristics, either a voltaage cushion is useful otherwise we can go for a support using the current which could be set in line along the Mill operator capacitance to hinder the straight-forward way with the presence of a zero on the left side of the plane (LHP). A zero on the left side, when kept in the appropriate area, could be responsible for dropping the impact of the pole and additionally a zero at the right side, supporting the stage edge, and working on huge sign strength.

For the most part, the exchange capacity of our functional enhancer with 3 roots on the denominator and one limited root on the numerator can be communicated with the transfer function,

$$T(s) = \frac{T_0\ (1-\frac{s}{z_0})}{\left(1-\frac{s}{p_0}\right)\left(1-\frac{s}{p_1}\right)(1-\frac{s}{p_2})} \tag{3.10}$$

If p0 is non-imaginary we can re-write it,

$$T(s) = \frac{T_0\ (1-\frac{s}{z_0})}{\left(1-\frac{s}{w_{p0}}\right)\left(1-\frac{s}{w_0}+\frac{s^2}{{w_0}^2}\right)} \tag{3.11}$$

Here p1 = - p1, has been a post recurrence related by the genuine shaft p1 and and are, individually, the factor at which we can calculate the rate of its dampen and the normal undamping recurrence comparing to the non-prevailing posts p2 and p3[6]. By meaning t the solidarity gain recurrence and m = 180° - A(jt), the stage edge of the opamp, the connection between the boundaries o, t, m and z can be displayed in Eq.3.12.

$$w_0 = \frac{w_t b}{\varepsilon-\sqrt{\varepsilon^2+b^2}} \tag{3.12}$$

Where b is the phase and is denoted by Eq.3.13.

$$b = \tan(\Phi_m + \tan^{-1}\frac{-z_0}{w_t} \tag{3.13}$$

Following which the frequency responses were plotted for different angles to gain theoretical understanding-

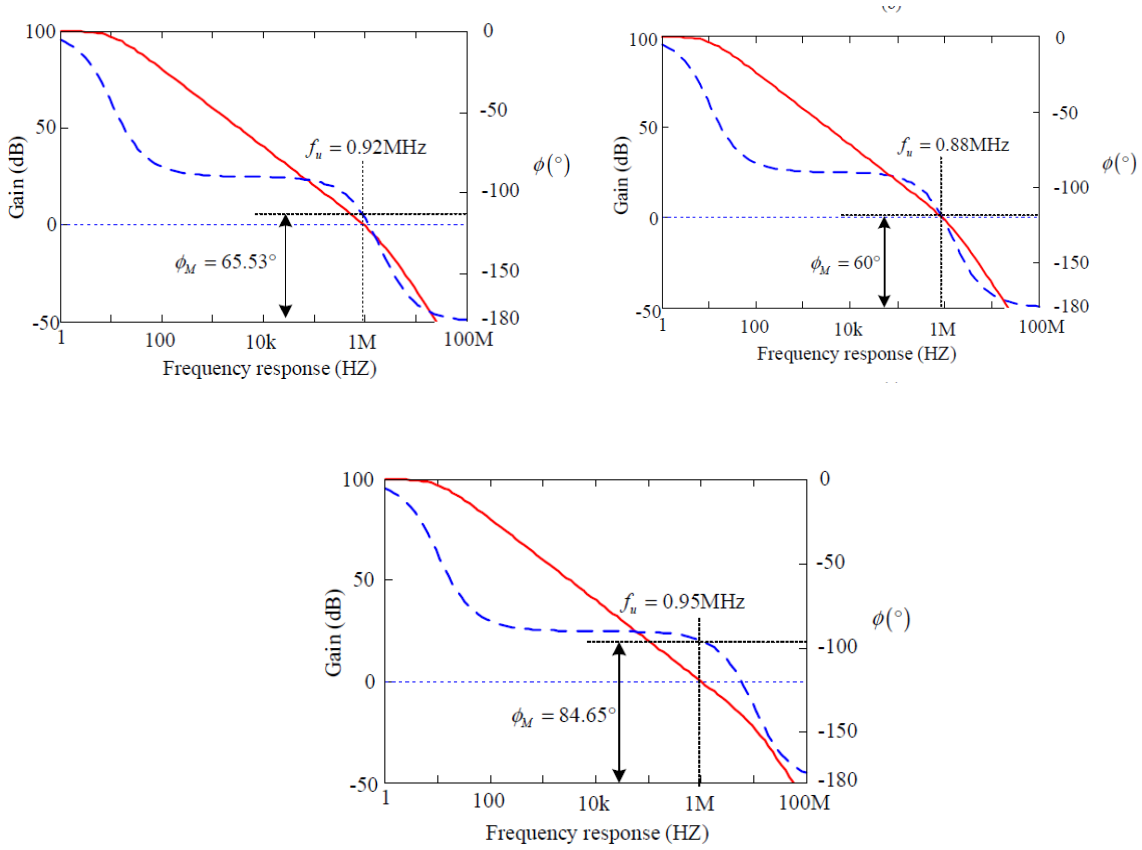


Figure 3.3.1: Frequency Responses for different Gains

Therefore, the necessary stage edge can be gotten if the worth of and are picked appropriately [7]. Notwithstanding, as portrayed in Fig. 3.3.1, the close loop response of the operation amp with criticism association can't be dictated by the stage edge alone. The damping factor of the non-predominant posts additionally assumes a basic part in molding the shut circle reaction of the opamp.

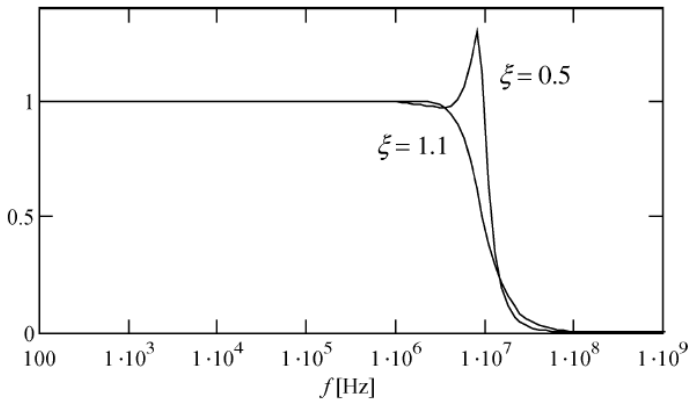


Figure 3.3.2: Magnitude Response

As indicated by the figure above, 3.3.2, for θ_m, signifies is the state that outcomes with our poles p2 and p3 converting into intricate form pairs, the cresting inside the shut circle reaction is clear. The pay circumstances that outcomes in complex poles having no or very little effect, posts ought to in this manner be circumspectly utilized [8]. As indicated by the principal condition the non-prevailing poles p1 and p2 are genuine if θ_m. It was tracked down that under such a condition, the upsides of p2 and z can be made equivalent if the underneath relationship is fulfilled[36].

3.4 Operational Amplifier Designing and Variables

The bi phase functional enhancer in Figure.3.4 is planned utilizing a prototype boundary using the 35nm Complementary Mosfet processing. The cycle boundary depicted in the Table 3.4.1 and plan boundary in Table 3.4.2 are utilized for planning the protoype for achieving the desired determination. The following values of the process and the design parameters which are shown are used while using the mosfet in our circuits simulated in LTSpice.

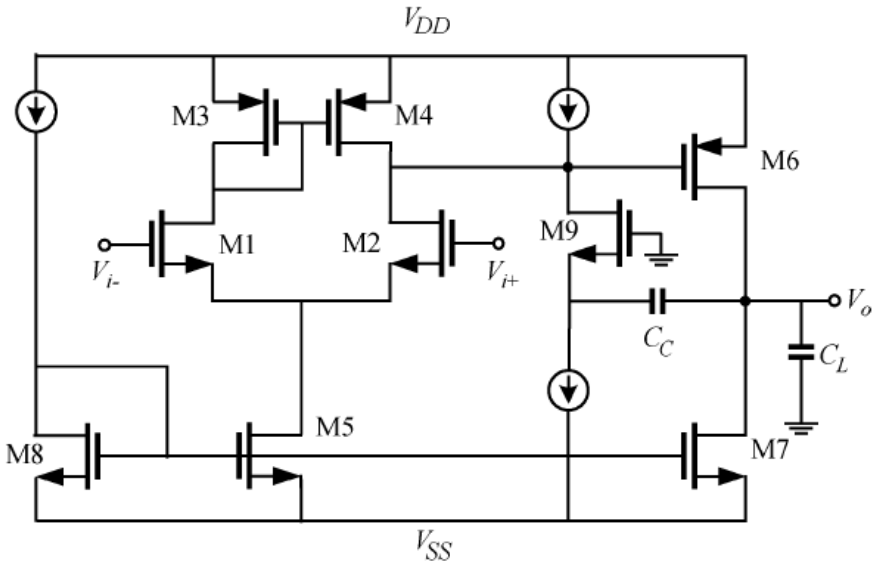


Figure 3.4 Design of Existing Op-Amp Current Buffer in consideration

The table below gives a brief about the process and design parameters of the CMOS used in the simulation process [9].

Process Parameters	PMOS	NMOS
T_{ox} (m)	7.8e -9	7.8e -9
μ (cm^2/Vsec)	155.52	421.38
Vt_0 (volt)	-0.68	0.549

Table I: Process Parameters

Devices	Width/Length (μm)
MN1, MN2	0.9
MN3, MN9	3
MP1, MP2	0.834
MN4, MN5	10
MN6, MN7	4
MN8	22.5
MNP3, MP4	1.78
MP5	13
C_C	0.5pF
Cl	5pF

Table II: Design Parameters

The design parameters and process parameters which are specified in the above tables are the values which have been taken into consideration after reviewing various Journal Papers in this domain and these parameters have been selected such that the output response is expected with the best possible stability based on the specifications of the MOSFET and all the different elements taken into consideration.

3.5 Need for Compensation

Planning a course with scaling of the voltage which is used for supplying and maintaining the electric field continuous in the semiconductor is cumbersome, so speakers using the multiple stages are the one required fix we can have. Despite this, each stage only has one post, so the input architecture becomes shaky as it falls through numerous steps. Following that, a multistage enhancer should be created for a transitory reaction that has been damped [10]. Broadly comprehended and approved compensating strategies are Miler operator remuneration, Cascode compensation, compensating circuit using forward feedbacks and a lot much subsidiaries taking into use such methods. Since of its pole splitting nature, the compensating method using the Miler is used for compensating the frequency because it can increase bandwidth to a higher frequency by moving non-dominant poles. Although several miller compensation strategies were presented in the past for enhancing the product of the gain for all the range of frequencies, severity of the circuit was increased as more steps were added and the no of amplifiers and capacitances were added. The use of a nulling resistor to compensate for Miller creates a zero on the right hand side of the plane (RHP), which degrades the steadiness of the system.

To cancel the pole on the right hand side of the plane, a compensating value of capacitance is applied in line with bufer of the current element which can be employed, although the presence of poles having the real and imaginary parts in the closed system loop is a drawback of this strategy. A correction based on damping stages is also offered, although the approach has a bad rate of rejection at the side of the supply from the power (PSRR)[11]. If we introduce cascade compensation, we can construct a capacitance or inductance node with a typically low value inside the functional enhancer that requires too much amount of power to eliminate RHP zero by connecting a compensation capacitor at a very less rate of impedance at the node. Similarly, in-direct way of compensating can be achieved by dividing the transistor to create an impedance which may appear to be less for the case of the operational amplifier. Adding a zero with the help of a feedback circuit using only straight path method[12] has also been described, but it suffers from a combination caused in the completed circuit due to the presence of the zero and pole present at the same time causing problem with sluggish settling transient response, making it unsuitable for all applications, and it has limited output swing. A floating capacitor is used in all of the procedures outlined above (in between drain and gate positioning of compensation capacitor always for the 2nd stage). The utilisation of a capacitance which used the combination of metal oxide (MOM) using the amount of silica in the chip tradeoff is required for a floating capacitor in modern CMOS technology. A compensation strategy based on a capacitance which is ground, could be implemented using a capacitance having the characteristics of a mosfet, has been brought forward in the current approach. The suggested method is impervious to noise which is generated by the voltage supplying the power, that becomes critical in huge SOC designs[13].

3.6 Proposed Compensation Technique

The proposed architecture of compensated two-stage opamp is shown in Figure 3.6.1. MN1, MN2 act as differential pair input transistors in the first stage, whereas Mn3, Mn4, Mn6 serve as transistors used for bias. A composite transistor is a 1st-step P-type mosfet source using the current as the main transistor for the loading that is been separated by multiple sections (MP2, MP3)[14]. Mp2 gate is connected straught to Mp1 gate, while Mp3 gate is switched via a filter that allows only lower frequencies to pass. As a result, the sum of gmp2 and gmp3 at low frequencies, and gmp2 at all lower frequencyes greater with respect to the cut-off frequency of the filter, is composite transistor transconductance (gm)[15].

Thus, composite semiconductor trans-conductance (gm) is the amount of gmp2 and gmp3 at low recurrence and gmp2 at all lower frequencies higher than the channel remove recurrence[41]. The miller compensation was compared with the uncompensated method and then the compensation method was proposed and then the ideal gain characteristics are shown.

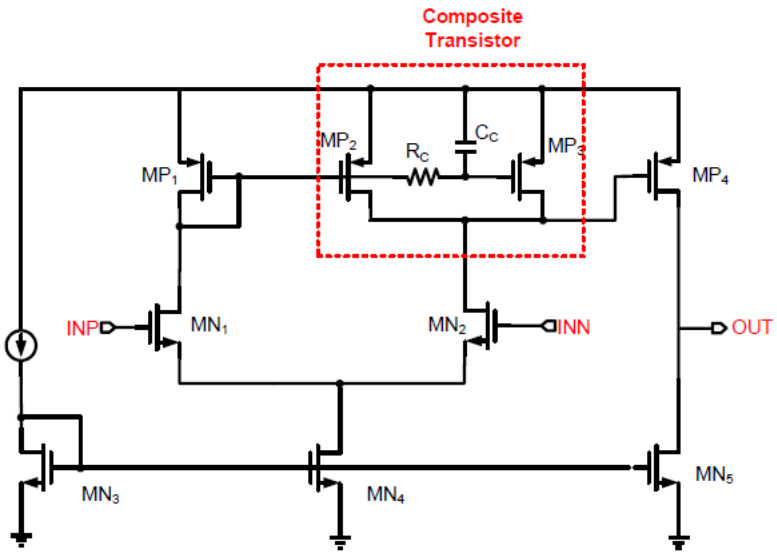


Figure 3.6.1: Proposed Compensation Technique

We might improve stability by positioning Zcomp precisely at the dominating pole of the uncompensated op amp; this type of compensation is also known as lag compensation [16]. The bode plot of the non-compensated, Miler compensation circuit, suggested compensated operational amplifier is shown in Fig. 3.6.2.

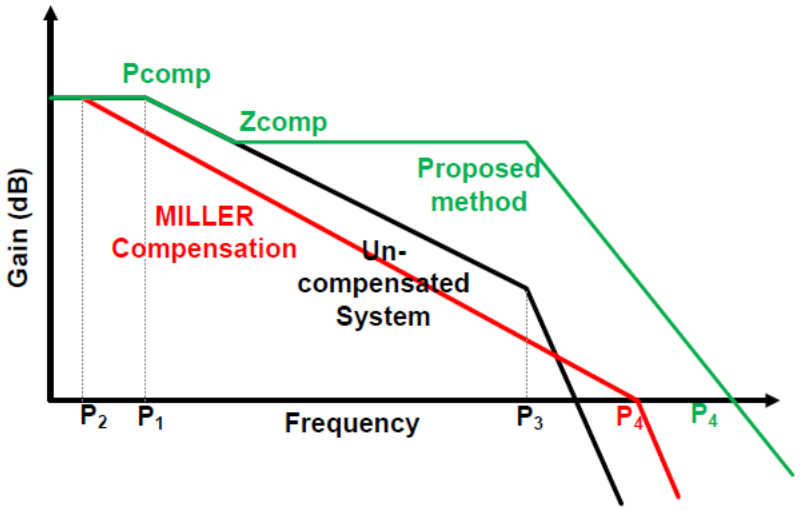


Figure 3.6.2: Magnitude Frequency Comparison

Clearly, the suggested solution achieves a significantly larger product of gain at the unit frequencies maintaining the power as the constant, or it might save substantial power considering the product of the gain at various frequencies as constant. The compensating capacitance in the composation transistor falls between Vdd and the operational amplifier output in this technique, thus Moscap[27] serves the role without the need for a metal capacitor. 10pF capacitor and 20K compensating resistor are used in this design. When we consider noise with respect to the frequencies at the higher range in the power supplied will have very less or no capacitance or inductance path at the end of the receiver, whereas miler Vdd noising figures out a way via the second step transistor CGS and the compensating capacitor C_c[18]. At 1MHz, simulations reveal a -30dB PSRR, whereas the miller approach has a -16dB PSRR, resulting in a 14dB greater supply rejection[42].

Chapter 4: Result and Discussion

The reproduction was performed on LTspice and first we played out the current buffer in 2-stage Operational Amplifier and the outcomes are displayed beneath in the circuit 4.1[19].

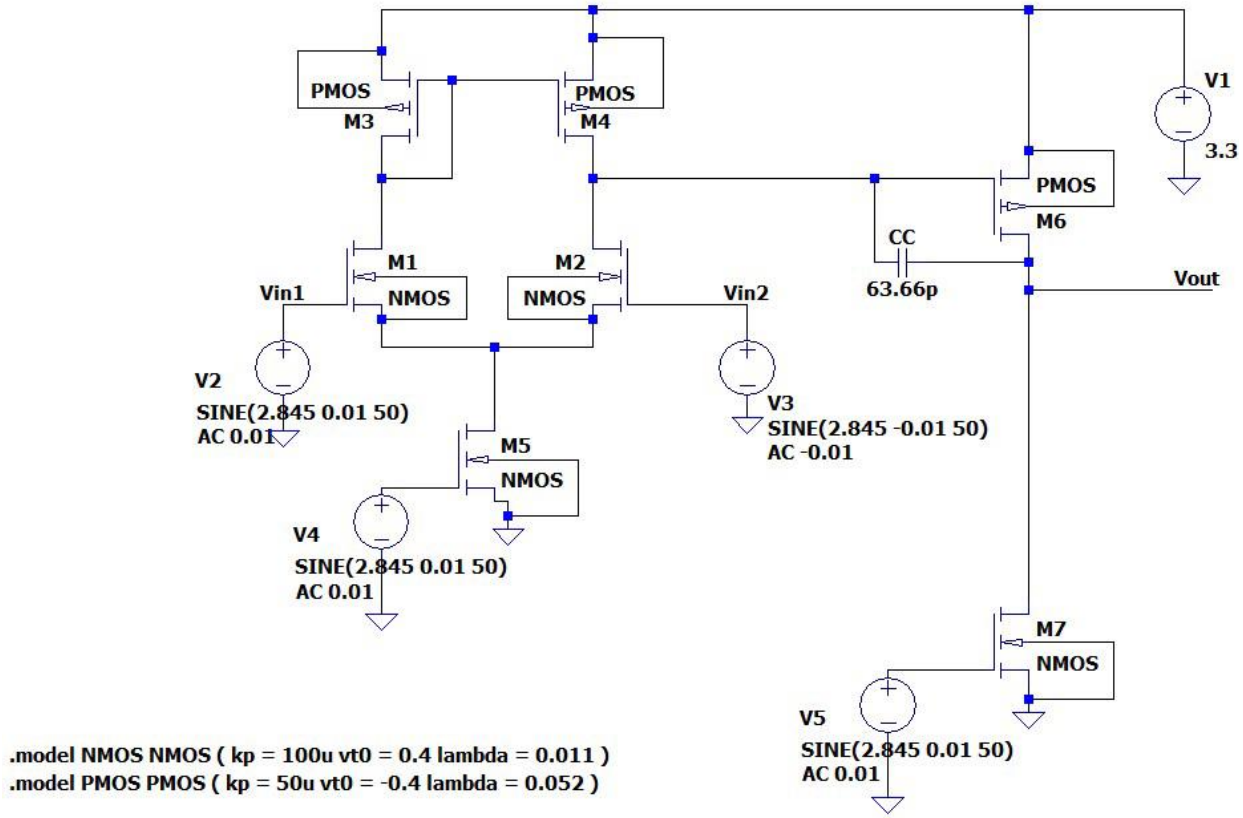


Figure 4.1: Current Buffer Two Stage Operational Amplifier

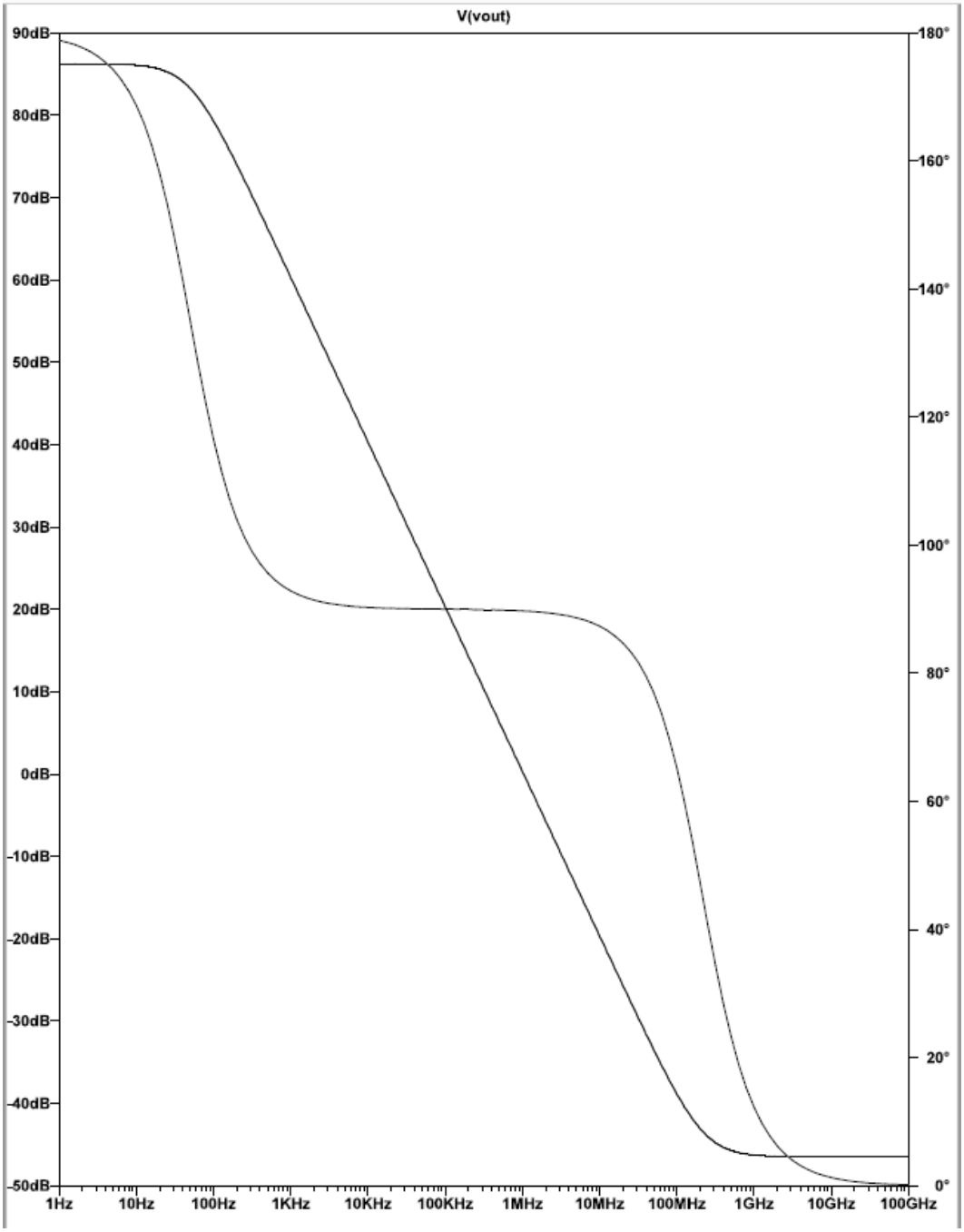


Figure 4.2: Output Frequency and Phase Response for Current Buffer Circuit.

The above output in the Figure 4.2, is achieved by drawing the schematic on LTSpice and specifying the design parameters as described in the paper above. But, due to this overlapping sequence at certain instances, the system is not stable. So, we proposed the Miler Capacitance in this particular circuit and observe the results.

Noticing the consequences of this current buffer circuit it was understood that to balance out a multiple-stages enhancer, the presentation with the Mill operator capacitance might make a feed forward way and zero on the right hand side of the plane (RHP), endangering the strength of the controlling circle and thus, the yield got was adjusted by altering the circuit boundaries according to the boundaries characterized in this paper and afterward the Mill operator Compensated Current buffer[20] was acquired The changes in the circuit made in LTSpice are depicted in Figure 4.3.

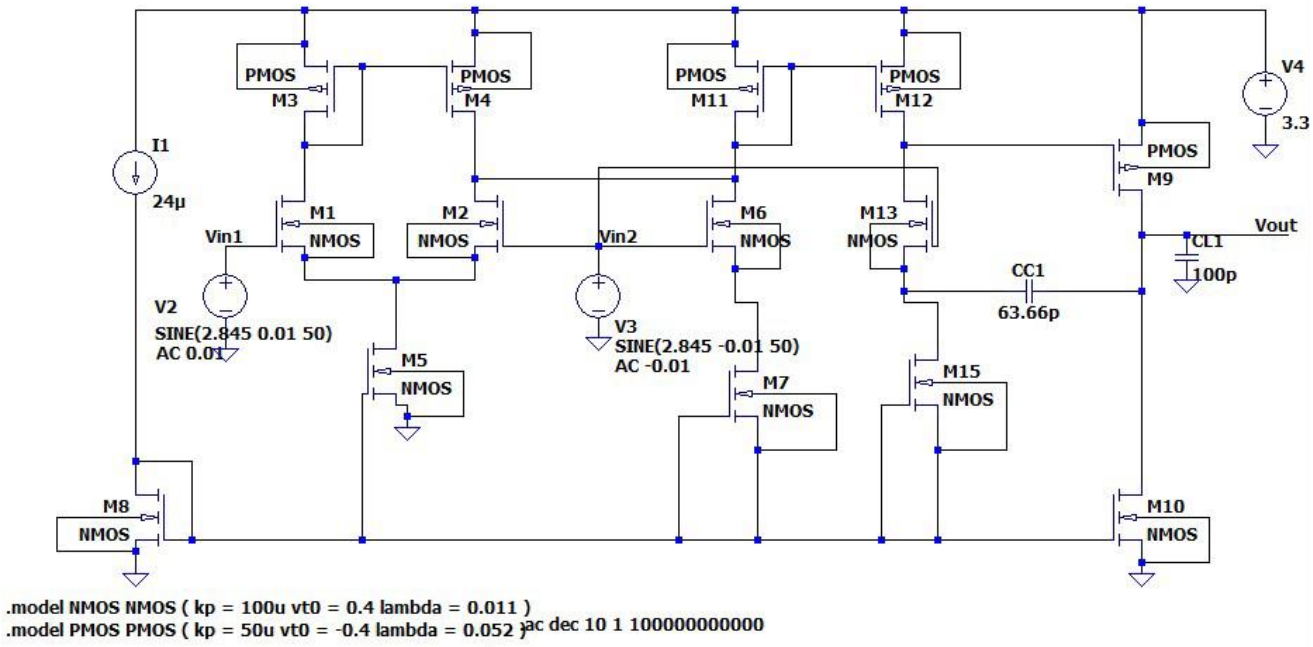


Figure 4.3: Miller compensation employing Current Buffer.

Comparing the final output frequency response for this technique, we observe that the overlapping has been removed successfully which was due to the presence of the pole on the right-side of the plane. This has eventually improved the stability and the frequency response of the system and is proved in the output in the Figure 4.4.

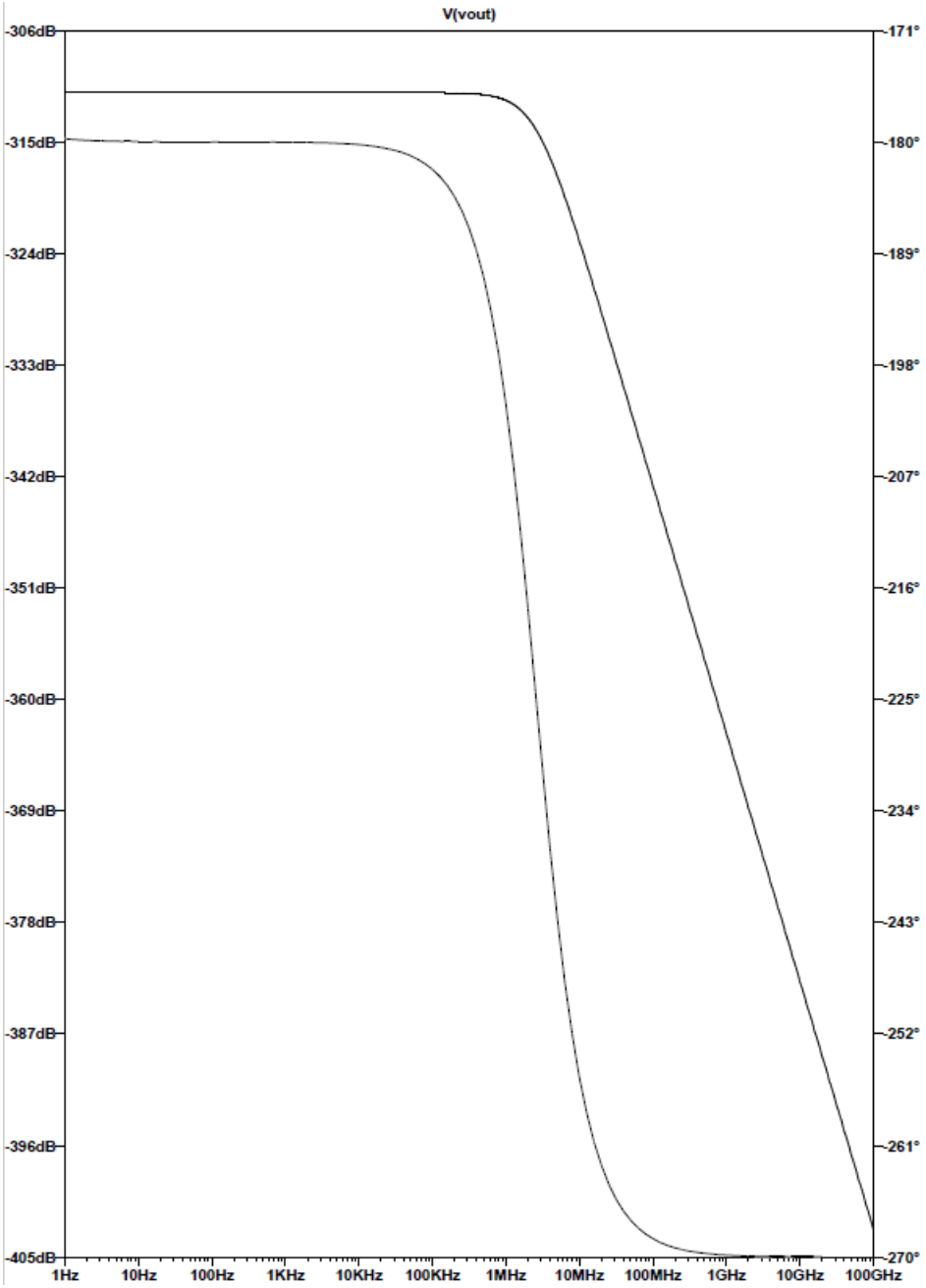


Figure 4.4: Miller Capacitor simulated output response

Chapter 5: Conclusion

After comparing the results of the Current Buffer circuit, it was clearly visible that when we try to balance the circuit of a multi-stage operational amplifier, with the help of the Miler Capacitance, we can achieve a feed-forward path in the circuit and also add a zero to the right hand side of the plane but in the end, it lead to endangering the control circle which ultimately affected the stability of the system. This problem which emphasized the gain of the circuit based on the existence of the roots of the transfer function were resolved with the help of the Miler compensated circuit employing the current buffer circuit. Hence, this is the best solution, as it helped us achieve stability without having to compromise with the frequency response of the circuit at higher frequency ranges.

Recreation results affirm that the proposed plan system could easily utilized for planning the functional enhancer thus meeting each and every one of the pre-defined determinations. Here all the brought forward methodology along with the procedure proposed to utilize the Mill operator capacitance current support remuneration. Be that as it may, while the technique resulted in the functional enhancer with un-dominant posts having real and imaginary part in the roots, which show topping in close loop recurrence reaction, the suggested plan method resulted in the operational enhancer with only 1 un-dominant genuine pole, which displays level shut circle recurrence reaction[21].

Examination between the proposed methodology and different systems are summed up underneath.

a) This proposed circuit in this thesis contrasted with the methodology dependent on the invalidating resistor remuneration: The worth of Cc of the proposed strategy can be made a lot more modest. The more extensive scope of the passable worth gives a higher adaptability to commotion power tradeoff.

b) Also, it also, contrasted with the methodology in remuneration technique: The two strategies depend on post zero undoing. Nonetheless, the proposed methodology is less delicate to the precision of change in the voltage at the input of the fact that the post zero doublet is set a lot higher than the non-prevailing poles which significantly affect the system stability[38].

c) This circuit is implemented on the 35nm CMOS and is capable to work with a voltage of 1.2V at the input side. With these conditions, we are able to have better efficiency of the functional enhancer along with a better frequency response.

d) The main advantage of using this in comparison to the other circuits is its capability with work for low-power circuits. Due to the 35nm technology, the space between the

different elements fabricated on the chip has significantly reduced. Hence, reducing the overall SOC size.

For the future work, we wish to work on the 14nm technology and wish to extend our compensation theory to these circuits. Since, the fabrication distance, has been reduced to half in this case. We have to work on the characteristics of the capacitances and inductances in the circuit which may affect each other's behavior. The stability of the circuits is to be checked with the compensation technique first and then the response of the circuit at different ranges of the frequency needs to be evaluated. At, the end the circuit characteristics and the minimum supply voltage need to be considered to propose the compensation for this technology.

Chapter 6: References

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Chapter 7: Appendix

7.1 List of Publication

The Paper “Miller Compensation using CMOS OPAMP employing Current Buffer” has been accepted for IEEE INCET,2022 which is Technically Co-Sponsored by IEEE Bangalore Section and IEEE USA, to be held in Belgaum, India and organized by the JGI Group. This is scheduled on 28th May,2022.