DESIGN OF A TERNARY DIGITAL TO ANALOG CONVERTER USING 3R-4R-6R LADDER NETWORK

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I, UTKARSH GUPTA, Roll No. 2K19/VLS/21 student of M.Tech. (VLSI Design & Embedded Systems), hereby declare that the Project Dissertation titled "Design of A Ternary Digital To Analog Converter Using 3R-4R-6R Ladder Network" which is submitted by me to the Department of ELECTRONICS AND COMMUNICATION ENGINEERING, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma, Associateship, Fellowship or other similar title or recognition.

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CERTIFICATE

I hereby certify that the Project Dissertation titled "Design of A Ternary Digital To Analog Converter Using 3R-4R-6R Ladder Network" which is submitted by Utkarsh Gupta, Roll No. 2K19/VLS/21, Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or fully for any Degree or Diploma to this University or elsewhere.

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ABSTRACT

It was proven very early in the year 1964 that instead of base 2, the natural base (given by e=2.71828...) is the most efficient radix for the implementation of switching systems. The research also showed that base 3 rather than base 2 is the most efficient integral base for the implementation of digital systems. But despite that, binary technology (base 2) dominated the implementation of digital systems all over the world until recently. During the early 2000s it became clear that new methodologies were required to sustain the Moore's law and keep up the growth of processing power without increasing the number of transistors. This led to the recent implementations of ternary logic systems which had been neglected till now. The new ternary logic systems offered substantial power saving, reduced no. of transistors, increased processing power, reduction in delay and reduction in area. In this project we are going to design a Ternary Digital To Analog Converter Using 3R-4R-6R Ladder Network. We further implement a 10 Trit ternary DAC using this technique which has a 57 times better resolution than a binary 10-bit DAC. Simulation results of this circuit also indicate a very low total unsettled error of 0.047% of the Full Scale Reading. All simulations were performed using SYMICA DE software.

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LIST OF ABBREVIATIONS

Abbreviation	Full Form
DAC	Digital to Analog Converter
ADC	Analog to Digital Converter
CNTFET	Carbon Nanotube Field Effect Transistor
T-DAC	Ternary DAC
T-ADC	Ternary ADC
NTI	Negative Ternary Inverter
STI	Standard Ternary Inverter
PTI	Positive Ternary Inverter
T-OR	Ternary OR gate
T-AND	Ternary AND gate
T-NOR	Ternary NOR gate
T-NAND	Ternary NAND gate
T-NOT	Ternary NOT Gate
VLSI	Very Large Scale Integration
MVL	Multiple Valued Logic
CMOS	Complementary Metal Oxide Semiconductor
MWCNT	Multi Wall Carbon Nanotubes
SWCNT	Single Wall Carbon Nanotubes
LST	Least Significant Trit
FSR	Full Scale Reading
DNL	Differential Nonlinearity
INL	Integral Nonlinearity
SPDT	Single Pole Dual Throw

CHAPTER 1: INTRODUCTION

1.1. INTRODUCTION

Today one of the major creative challenges faced by the VLSI circuit and system engineers is to design a new generation of VLSI products which consume minimum power without compromising on minimum area constraints. The concern of power dissipation in the form of heat has been part of the design process since the 1970s but it was only towards the end of the century that it became the main design concern [1].

In any modern VLSI circuit, about 70 per cent of the chip area is occupied only by the interconnections [2]. The large number of nodes and interconnections in modern binary circuits lead to enormous levels of power consumption and many restrictions in fabrication which can be a source of failures. Thus, the interconnection complexity and other issues of binary circuits paved way for the research in multiple-valued logic (MVL) alternatives i.e. technologies using bases other than base 2. Among all the MVL technologies it has been proven mathematically by the authors of [3] that ternary logic (base 3) is the most efficient in circuit complexity and cost compared to other bases.

On the device level, many devices and techniques such as Carbon Nanotube FETs, Single-electron devices, Spin wave architecture, Quantum electronics and Quantum Computing etc. were developed in order to replace the

CMOS technology. Among these new techniques CNTFETs operate satisfactorily and provide the best trade-off in terms of energy efficiency and circuit speed [4]. Further, the property of CNTFETs to manifest different threshold voltages at different nanotube diameters make them the ideal candidate for implementing MVL technologies [2].

These new devices and techniques enabled the efficient design of Ternary Combinational and Ternary Sequential circuits. While design of ternary digital systems can mitigate most of the above challenges faced by the VLSI designers, the main problem remains that the physical world is made up of analog signals. So in addition to creation of ternary combinational and sequential circuits we require a ternary A/D and D/A Converters to convert these digital values to analog signals and vice versa.

The first design of a Ternary DAC using a 3R/4R ladder network was proposed very early in the year 1986 in [15]. But this design incorporated the use of triple throw switches which were hard to fabricate. An improvement has been suggested in [16] which uses SPDTs instead of triple throw switches and a differential ladder network. But fabricating large resistances could cause increased chip area and parasitic capacitances [17]. In order to avoid that a new implementation of a T-DAC using current mirror sources has been suggested in [17]. A drawback of the circuits suggested in [16, 17] was that they needed additional circuitry for Ternary to Binary Conversion of their input signals. In [18] a new resistive ladder network has been proposed which doesn't require any ternary to binary conversion circuitry. This circuit has 2 different ratios of resistors for the least significant trits and most significant trits. In [19], a binary weighted ternary DAC has been proposed. Each of these designs, its merits and drawbacks have been discussed in a later chapter.

In this project we are going to design a Ternary Digital To Analog Converter Using 3R-4R-6R Ladder Network which is a modification of the design proposed in [15]. This new design uses also uses a voltage follower at the output of the resistive ladder network as proposed in [18]. We further implement a 10 Trit ternary DAC using this technique which has a 57 times better resolution than a binary 10-bit DAC. Simulation results of this circuit also indicate a very low total unsettled error of 0.047% of the Full Scale Reading. All simulations were performed using SYMICA DE software.

The rest of this project report has been organized as follows - Chapter 2 gives an introduction to the Ternary Logic. Chapter 3 provides an overview of the previous works and Chapter 4 explains the adopted methodology. Chapter 5 consists of the Simulation results, comparison with previous work, conclusion and future scope of this work.

CHAPTER 2: TERNARY LOGIC

2.1. INTRODUCTION

Even though it had been shown in 1964 that instead of base 2, the natural base e=2.71828... is the most efficient radix for the implementation of switching systems and base 3 is the most efficient integral base for the implementation of switching systems, binary technology (base 2) dominated the implementation of all switching systems throughout the world for many years. It was only during the early 2000s that it became clear that new methodologies were required to sustain the Moore's law and keep up the growth of processing power without increasing the number of transistors. Over the last decade, ternary logic was extensively investigated and it has been shown that ternary logic has superior characteristics compared to binary circuits, making it a compelling alternative. These characteristics include a lower count of active devices on the chip, an increased capability to process data per unit area, higher flexibility, higher processing speed and a lower power dissipation and lower interconnection complexity[2].

There are two ways to represent the Ternary logic systems: balanced ternary logic (-1,0,1) which corresponds to ($-V_{dd}$,0,V_{dd}), and standard/unbalanced ternary logic (0,1,2) which corresponds to (0,V_{dd}/2,V_{dd})[6]. The T-DAC developed in this project uses standard ternary logic (0,1,2) but a similar approach can be used to construct a T-DAC which uses the balanced ternary logic (-1,0,1).

The basic switching elements used for the implementation of ternary logic are diodes, bipolar transistors, JFETS, MOSFETs and Resonant Tunneling Devices (RTDs) and CNTFETs. Most of the recent implementations of Ternary logic employ CNTFETS due to their unique properties which make them highly suitable for implementing MVL. CNTFETs have been discussed in detail in next section.

2.2. CARBON NANOTUBE FET (CNTFET)

Design of Ternary logic was simplified greatly by the advent of the CNTFETs. Carbon nanotubes are made from very narrow strips of minuscule sheets of graphite which are rolled into a tube shape. The relatively small dimensions and unique morphologies of the CNTs have made them a focus of nano-electronics engineers and scientists. If a single graphite sheet is used, the CNT formed is called single-wall (SWCNT) type and if the number of sheets is more than one, then it is called a multi-wall (MWCNT) [5].

The three dimensional arrangement of the carbon atoms in any CNT sheet is specified with by it's chiral vector which is given by $ch=nXa+ mXb$, where a and b are two vectors for the hexagonal lattice of the CNT and the two indexes (n, m) are determined according to the orientation of the graphite sheet. There are 3 different SWCNT types based on the chirality vector -

- The zigzag CNT (when n=0 or m=0)
- The armchair CNT(when n=m)
- The chiral CNT (when $n \neq m \neq 0$)

The electrical conductivity of a SWCNT is also dependent on the

above chiral vector. A SWCNT will behave like a semiconductor if it's indexes 'n' and 'm' follow the equation n-m≠3k (where k is any integer value) [5]. The diameter D_{CNT} of a CNTFET is calculated through the equation-

$$D_{CNT} = \frac{a\sqrt{n_1^2 + n_1 n_2 + n_2^2}}{\pi} \tag{2.1}$$

where a is the inter-carbon atom distance which is approximately equal to 0.249 nanometers [5]. The threshold voltage V_{th} is determined by the equation-

$$V_{th} = \frac{aV_\pi}{\sqrt{3}\, eD_{CNT}} \tag{2.2}$$

where, V_π is a constant (with value of 3.033 eV) and it determines the inter atom carbon π-π bond energy in a tight bonding lattice [5]. The dependence of V_{th} on D_{CNT} makes CNTFETs an ideal candidate for use in MVL.

The following table lists four commonly used chiralities alongwith their corresponding CNT diameters as well as threshold voltages –

Table 2.1: Commonly used Chiralities of CNTFET

Chiral Vector (n_1, n_2)	Threshold Voltage (V)	Diameter (nm)
(8,0)	0.7	0.63407
(10,0)	0.56	0.79259
(19,0)	0.3	1.50592
(29,0)	0.2	2.29851

2.3. Basic Ternary Logic Gates

There are a few basic operations which every logic system should be able to perform irrespective of it's complexity. These basic operations are NOT, OR, AND, NAND and NOR. Ternary gates which can perform these functions are denoted as T-NOT, T-OR, and T-AND etc.

A ternary inverter is a circuit that inverts the input signal and gives it as the output. In ternary logic we have three inverter operations – Positive ternary inverter (PTI), Negative Ternary Inverter (NTI) and Standard ternary inverter (STI). The behaviour of these inverters is described by the given below equations-

$$\text{NTI-} \quad \begin{cases} 2, & if\ x = 0 \\ 0, & if\ x \neq 0 \end{cases} \qquad (2.3)$$

$$\text{STI-} \quad \bar{x} = 2 - x \qquad (2.4)$$

$$\text{PTI-} \quad \begin{cases} 0, & if\ x = 2 \\ 2, & if\ x \neq 2 \end{cases} \qquad (2.5)$$

The truth-table of all three ternary inverters is given below-

Table 2.2: Truth Table of PTI, NTI and STI

Input (X)	NTI (Y0)	STI (Y1)	PTI (Y2)
0	2	2	2
1	0	1	2
2	0	0	0

A simple transistor level design of the PTI, NTI and STI was given in [5] and is shown in Fig. 2.1. These are the simplest and most efficient implementations of the ternary inverters. In comparison the STI implementation given in [6] uses 5 CNTFETs. The STI proposed in [8] is even more inefficient as it uses 6 transistors to implement the same STI which has been implemented using only two CNTFETs in [5]. This clearly shows that the use of appropriate chiralities and diameters of CNTFETs is very crucial for the design of an efficient ternary logic device.

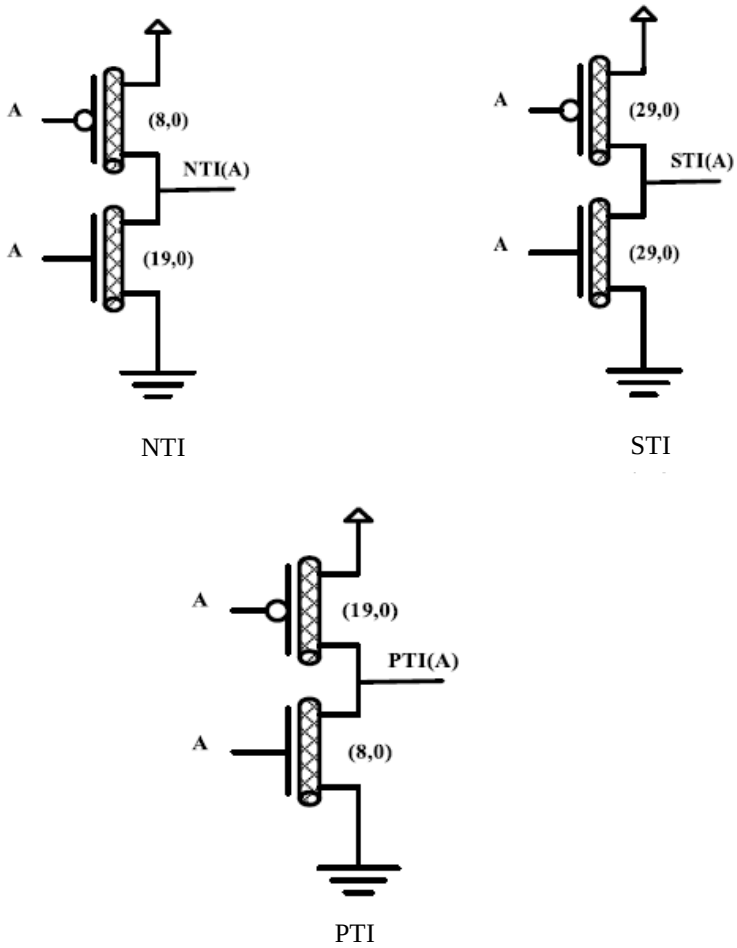

Fig. 2.1: Transistor level of NTI, STI and PTI

The equations of the other basic ternary functions are given below –

$$Y_{AND} = X_i.X_j = min\{X_i, X_j\} \quad (2.6)$$

$$Y_{NAND} = \overline{min\{X_i, X_j\}} \quad (2.7)$$

$$Y_{OR} = X_i + X_j = max\{X_i, X_j\} \quad (2.8)$$

$$Y_{NOR} = \overline{max\{X_i, X_j\}} \quad (2.9)$$

where Xi and Xj are ternary variables having values 0,1 or 2. As we can see Ternary OR operation basically returns the input with the maximum value as it's output. Similarly the Ternary AND operation returns the input with the minimum value as it's output. Further, we can see that the T-NOR and T-NAND operations

return the standard ternary inversion of the corresponding T-OR and T-AND operations respectively. The Truth table of these functions is given below-

Table 2.3: Truth Table of T-OR, T-NOR, T-AND and T-NAND

Input A	Input B	T-OR	T-NOR	T-AND	T-NAND
0	0	0	2	0	2
0	1	1	1	0	2
0	2	2	0	0	2
1	0	1	1	0	2
1	1	1	1	1	1
1	2	2	0	1	1
2	0	2	0	0	2
2	1	2	0	1	1
2	2	2	0	2	0

2.4. Ternary Combinational Circuits

A ternary combinational circuit can be defined as a circuit which uses of a combination of ternary logic gates to transform ternary input signals into ternary output signals. The output of a Ternary combinational circuit depends only on the current inputs i.e. there is no memory element in the circuit. Several ternary combinational circuits have been proposed in [2, 5, 6].

In [5] a systematic methodology has been given which can be used to design any required ternary combinational circuit with the help of CNTFETs. This method [5] incorporates the use of a Ternary to Binary Decoder at the input end and a binary to ternary encoder at the output end. After conversion of input ternary signals to binary signals, they are fed to an intermediate stage which separately generates two binary outputs corresponding to logic 1 and logic 2 output. Finally these two binary outputs are encoded into a single ternary output

using the binary to ternary encoder presented in [5]. Using this technique a Ternary Half Adder and a ternary 1-digit multiplier have been implemented in [5].

2.5. Ternary Sequential Circuits

A ternary Sequential circuit can be defined as a circuit whose output depends on the present input as well as the past input. In other words a ternary sequential circuit is one which consists of a ternary memory cell. The biggest advantage of creating a ternary memory device is the increased memory capacity. The storage capacity of a ternary device versus a binary device rises exponentially by a factor of $(3/2)^n$ where 'n' is the no. of ternary digits (or trits) or the no. of devices. For instance, the storage capacity of a 2 trit memory cell is $(3/2)^2 = 2.25$ times of a 2-bit memory cell. Another way to see this is that the storage capacity of a 2 trit memory cell is more than a 3-bit memory cell. So with ternary memories we can have increased storage capacity with fewer number of devices.

The most basic ternary memory element is a ternary flip flop or a flip flap flop. It has three stable states (0, 1 and 2). A flip flap flop can be easily constructed from a binary flip flop by just replacing the binary logic gates with Ternary logic gates as shown in Fig. 2.2. At first the circuit appears exactly like a binary D-latch constructed from four NAND gates and one inverter. But in reality, it is a ternary D-latch constructed using four T-NAND gates and one T-NOT gate. An important thing to note over here is that the enable signal is a binary signal and can have only two values logic 0 or logic 2. The output of the ternary D-latch is not known for the intermediate (logic 1) value of EN.

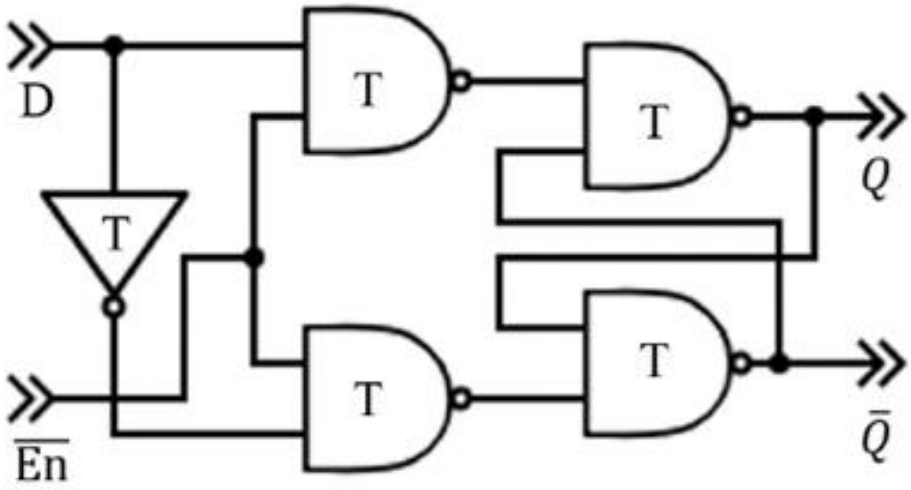

Fig. 2.2: Ternary D-Latch using T-NAND and T-NOT (STI) gates

The authors of [8] have proposed a ternary master slave D-flip flop implemented using CNTFETs. The circuit is shown below –

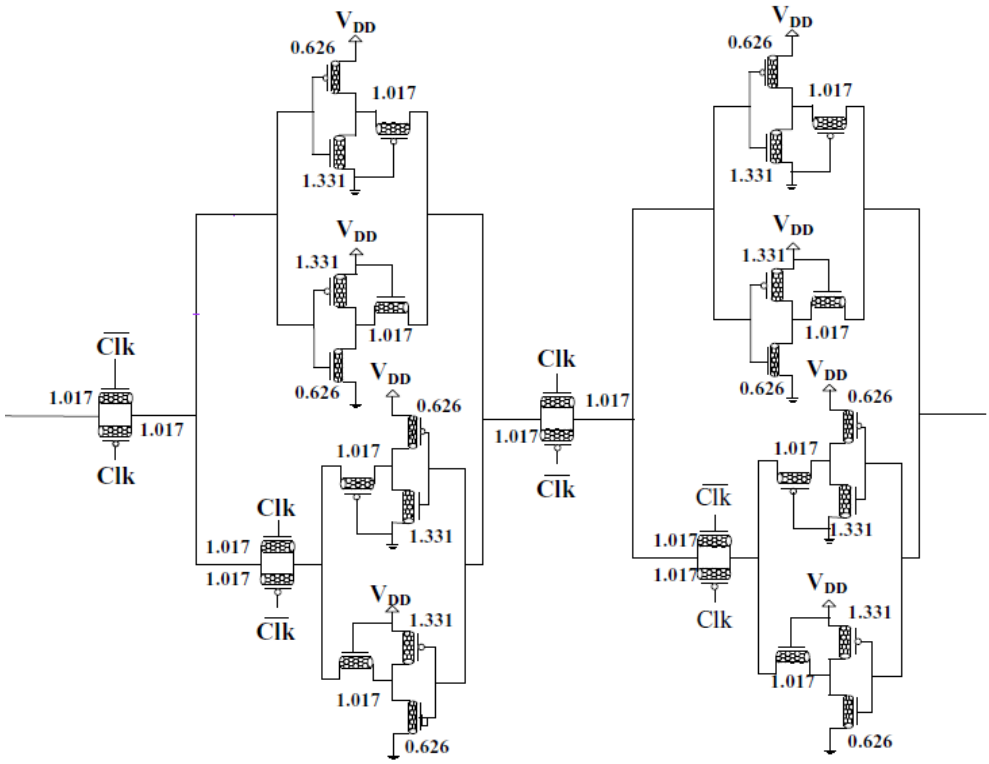

Fig. 2.3: Ternary Master slave D-Flip Flop proposed in [8]

A simplified version of the above circuit is shown below-

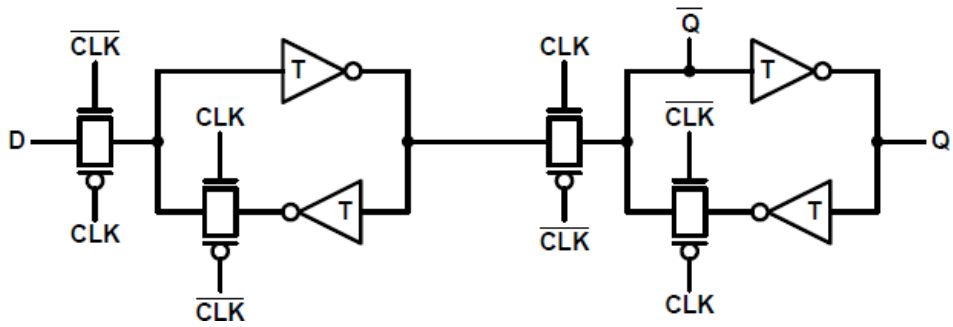

Fig. 2.4: Simplified version of Ternary Master slave D-Flip Flop proposed in [8]

The truth table of the above ternary Master slave D flip flap flop is given below-

Table 2.4: Truth Table of Master Slave Ternary D-Flifp Flap Flop

CLK	D	Q_{n+1}
↓	X	Q_n
↑	0	0
↑	1	1
↑	2	2

Once we create a ternary memory element we can use it to design more sophisticated circuits like shift registers, counters, data encoders and decoders etc.

2.6. Ternary Data Converters

In our day to day life we use several digital electronic appliances for various purposes like communication, entertainment, transportation and security etc. By implementing these digital systems using ternary logic we can greatly improve their performance and reduce the size of these digital systems. But since most real world signals are analog in nature, we need an interface to convert these the analog signals into ternary digit signals and ternary digital signals into analog

signals. Consider the Audio Processing example given below-

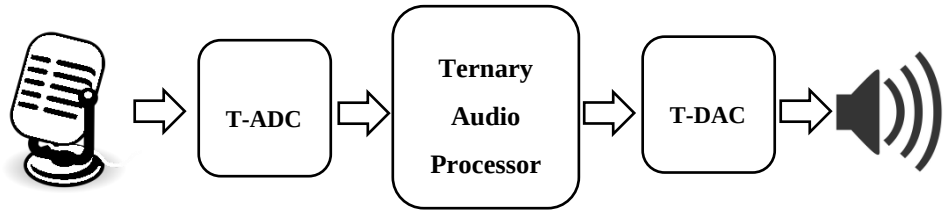

Fig. 2.5: Theoretical Ternary Audio Processing System

In this example, the ternary ADC converts the speech signal (analog) received from the audio input device (mic) into a ternary digital signal so that it can be fed to the ternary Audio processing equipment. Thereafter, the processed ternary digital signal is converted back into an analog signal by the ternary DAC so that it can be used by the audio output device (speaker).

A DAC is an electronic circuit which converts a digital code into an analog code. The biggest advantage of using a ternary DAC at place of a binary DAC is the increased performance, higher resolution and reduced size. The resolution of a ternary device versus a binary device rises exponentially by a factor of $(3/2)^n$ where 'n' is the no. of ternary digits (or trits) in the digital code. In this project we develop a ternary 10-trit DAC which has a resolution of $(3/2)^{10}$, i.e. approximately 57 times the resolution of a 10-bit binary DAC. Alternatively, if use a 7-trit ternary DAC, it gives a resolution which is slightly higher than the resolution of a 11-bit binary DAC. Thus according to the design goal we can either increase the resolution or decrease the area/power requirements of a DAC by using ternary logic.

The 2 most common architectures for a binary DAC are the binary weighted DAC and the R-2R ladder DAC. In this project we will develop a

ternary DAC by slightly modifying the R-2R architecture to create a 3R-4R-6R ladder network.

2.7. Performance parameters of a T-DAC

In accordance with [20-25], the various performance parameters of a ternary digital to analog converter can be defined as follows-

- **Resolution**- The resolution of Ternary Digital to Analog Converter can be defined as the number of different analog output voltage values that can be provided by the DAC or the different number of codes that can be written to the T-DAC [22, 23, 25]. For a n-Trit T-DAC, the resolution is 3^n
- **Least Significant Trit (LST)**- The LST of a T-DAC is defined as the smallest change that can be produced at the analog output (in volts) corresponding to a change in the least significant trit of the input ternary code. For a n-trit T-DAC, the LST is equal to $Vref/3^n$
- **Gain error –** The Gain error of a T-DAC can be defined as the difference between the expected value of the Full scale reading and the actual value of the full scale reading [20].
- **Differential Nonlinearity (DNL) error**- The DNL error of a T-DAC can be described as the difference between the actual step height of a T-DAC and the ideal value of the LST of a T-DAC [20, 24].
- **Integral Nonlinearity INL error**- The INL error of T-DAC can be defined as the deviation of all values on the actual transfer function from a straight line representing the ideal transfer function [20, 24]. It can be calculated as the summation of all differential nonlinearities for each step [20,24].

CHAPTER 3: METHODOLOGY USED

3.1. PREVIOUS WORK-

In the recent years, several designs of different ternary logic circuits have been proposed which include some primary arithmetic operations like the half adder and 1-digit multiplier presented in [5]. The main focus of these implementations was efficiency in terms of the delay, number of transistors and power. But most of the previous work has been focused on implementing only combinational and sequential ternary circuits and there has been very little work in the implementation of ternary data converters (T-ADCs and T-DACs) despite the many advantages of ternary circuits.

One of the earliest designs of a ternary DAC was proposed in [15] in 1986 and is shown in Fig. 3.1. This was the first ternary DAC to use a ladder network with resistances in the ratio of 3R, 4R and 6R. The values of resistances are picked such that the value of the equivalent resistance to the left of each node principle node is 6R. The detailed network analysis is given in [15] and has been skipped here for the sake of brevity. A major drawback of this circuit was that it required the fabrication of Triple Throw switches which are hard to implement.

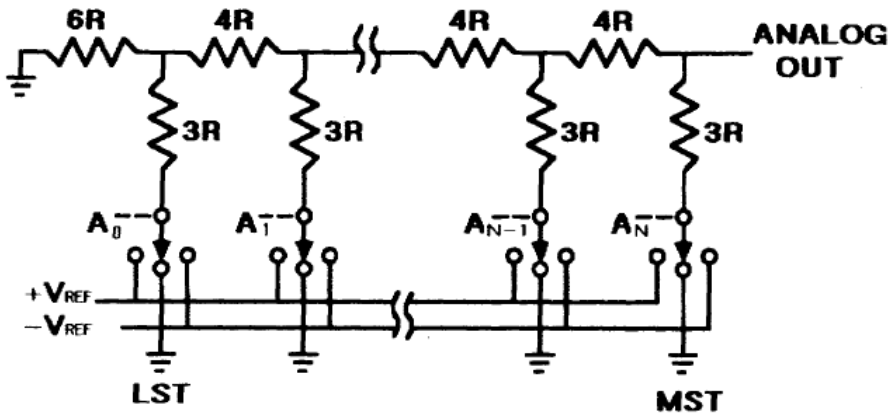

Fig. 3.1: Ternary DAC design proposed in [15]

To mitigate these problems, the authors of [16] have suggested a new circuit which uses SPDT (Single Pole Dual Throw) switches instead of Triple throw Switches and a single power supply line instead of two. This circuit [16] uses SPDTs in conjunction with a differential ladder network. The circuit is shown in the Fig. 3.2 below-

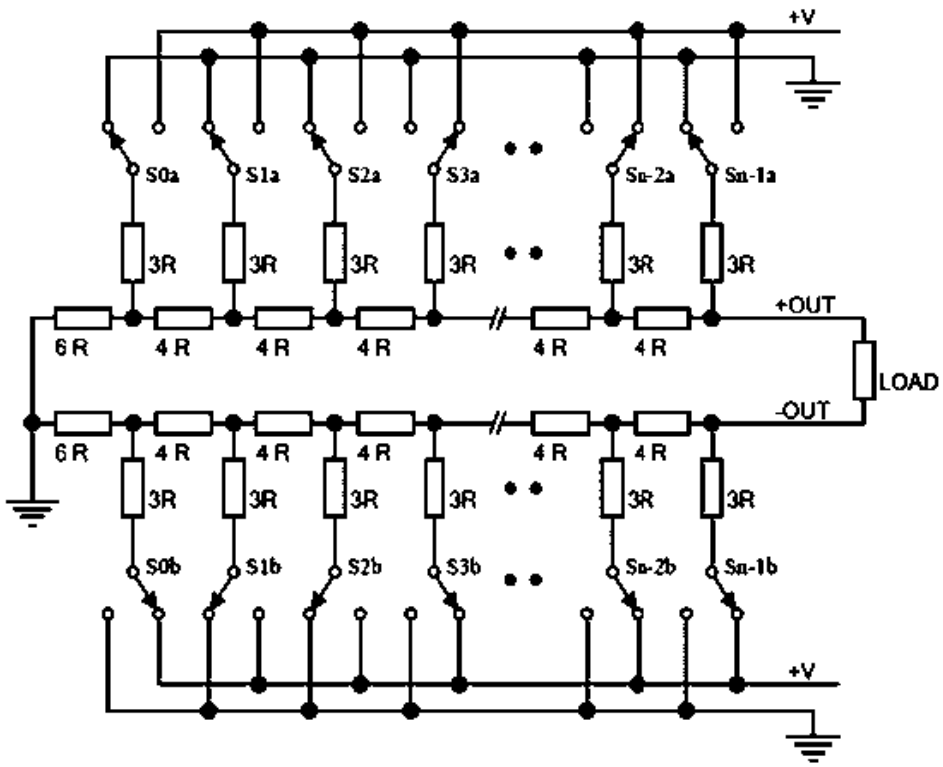

Fig. 3.2: Ternary DAC design proposed in [16]

While this circuit presented in [16] mitigated the above problems, it had it's own drawbacks. Firstly, this circuit uses a differential ladder which doubles the number of required resistors and increases the design complexity as well as power consumption. Further, this T-DAC is not truly a ternary DAC as it requires the conversion of ternary signals to binary signals for it's negative and positive value coding branches. This means that we require additional circuitry in the form of a ternary to binary decoder in order to utilize this DAC.

A very different approach for the construction of a ternary DAC has been proposed in [17] and is shown in Fig. 3.3 below. In this circuit the use of current mirror sources has been proposed instead of a resistor ladder network. This is done to avoid the challenges faced in the fabrication of resistor lines in the range of a few kΩ [17].

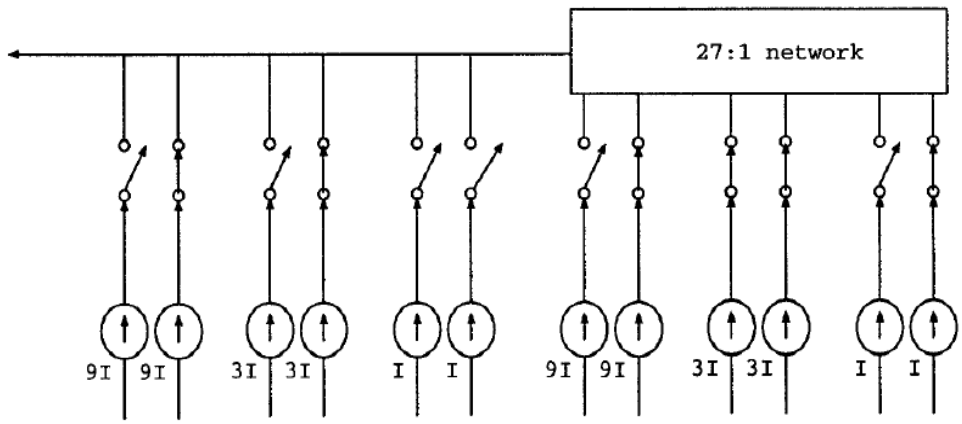

Fig. 3.3: Ternary DAC design proposed in [17]

But this circuit again requires conversion of ternary signals to binary signals which means it also requires additional circuitry in the form of a ternary to binary decoder. Further, even though the resistive ladder network has been removed, the circuit still requires a 27:1 current divider network which has been realized using MOS transistors. The MOS transistor current divider network may reduce the area and parasitic capacitance of the chip but the large number of MOS transistors in the current divider network and all current mirror sources increase

the design complexity and increase the number of steps in the fabrication process, thereby increasing the fabrication costs.

Another disadvantage of the above circuits is that in all of these circuits the digital inputs have been connected indirectly through a triple throw switch in [15] or an SPDT in [16,17]. This problem has been resolved in [18] which presents a completely new resistive network for the Ternary DAC. The circuit is shown in Fig. 3.4 below-

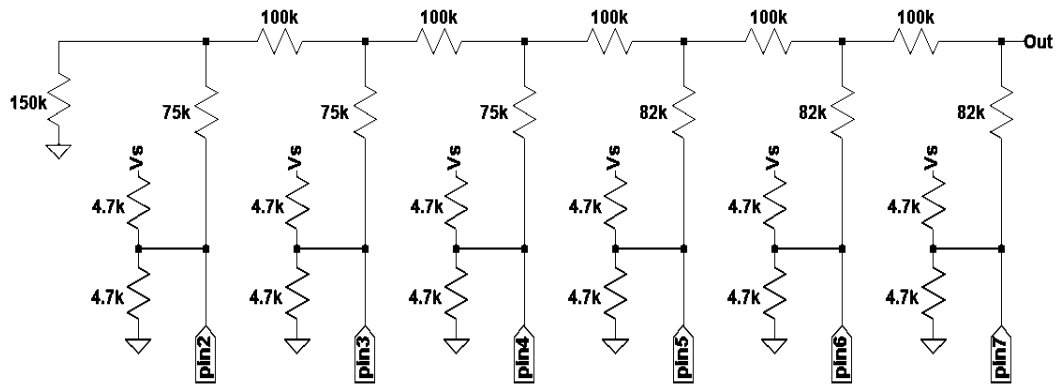

Fig. 3.4: Ternary DAC design proposed in [18]

This circuit uses a potential divider, which in this case is a pair of 4.7kΩ resistors. This holds the pin at Vs/2 when a pin is configured as High impedance input. The main ladder resistors are much stronger so that the normal pin drive remains unaffected [18]. This circuit also uses an output buffer (voltage follower) at the output end (shown in Fig. 3.5). The output of a DAC has a variable impedance due to the resistor network and it becomes non-linear if connected directly to the load. Therefore the output is connected to a Voltage follower.

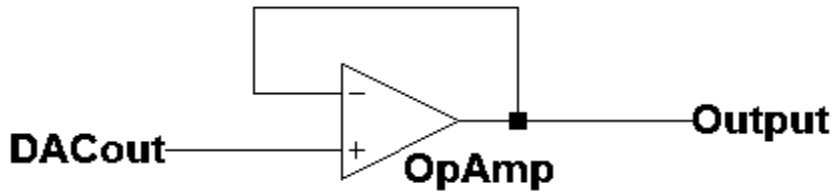

Fig. 3.5: Output Buffer (Voltage follower) from [18]

Since the above circuit uses too many different values of resistances, it can quickly increase the design complexity and fabrication costs. Further, this circuit uses large values of resistances and as mentioned in [17], the fabrication of resistances which are even a few kΩs can lead to large chip area and high parasitic capacitances. Therefore fabrication of a large number of resistors of large values can quickly increase the total size of the chip and the total parasitic capacitances of the circuit.

Another approach for creating a ternary DAC using the weighted resistance architecture has been proposed in [19] and is shown below in Fig. 3.6-

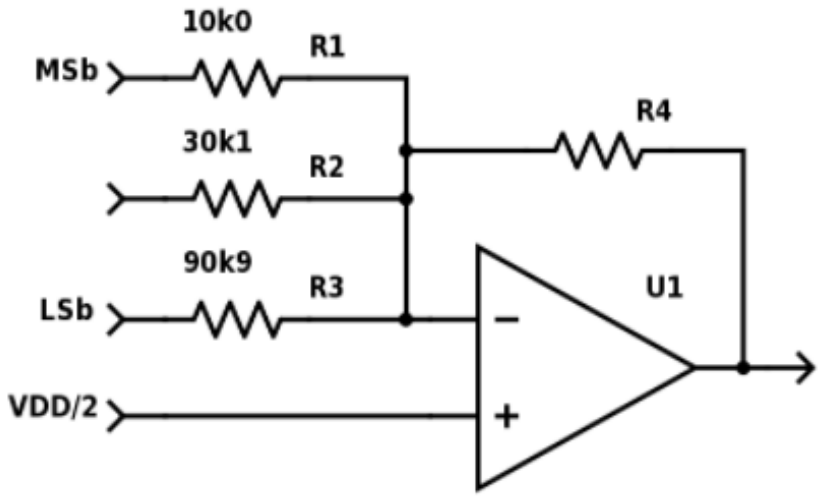

Fig. 3.6: Ternary DAC design proposed in [19]

Upon careful observation we can see that this design [19] is unfavorable for the same reasons as for the circuit proposed in [18] i.e. larger chip area, large parasitic capacitances, multiple different values of resistors to be fabricated etc.

3.2. PROPOSED DESIGN-

In this project we design a simple ternary DAC by modifying the 3R-4R-6R ladder network proposed in [15]. This circuit uses only three different values of resistors and doesn't require large resistances of the order of tens or hundreds of kΩ as in [18, 19]. Further, the proposed circuit doesn't require the usage of triple throw switches or SPDT as in [15-17] because the digital signals are directly connected to the input lines of the T-DAC. In order to avoid any non-linearity caused by this direct connection, we use a output buffer (voltage buffer) as in [18, 19]. In addition to that the proposed circuit is a truly ternary DAC in the sense that it does not require any additional Ternary to binary conversion circuitry as in [16, 17]. The proposed design for an n-Trit Ternary DAC is given in the Fig. 3.7 below-

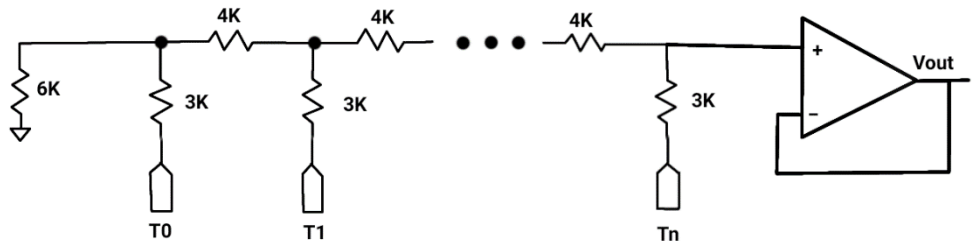

Fig. 3.7: Proposed n-Trit Ternary DAC

It is a simple infinite ladder network with a combination of the resistances 3K, 4K, 6K. The ternary digital inputs T0, T1, … Tn are directly applied at the inputs of the DAC. The output of the resistive ladder network is fed to a voltage follower. Using this technique the following circuit was implemented in Symica DE (shown in Fig. 3.8 on next page). The ten boxes labeled "signal" at the bottom are ternary staircase wave generators which generate a waveform with a time period equal to 3^{n+1} nanoseconds for the nth input.

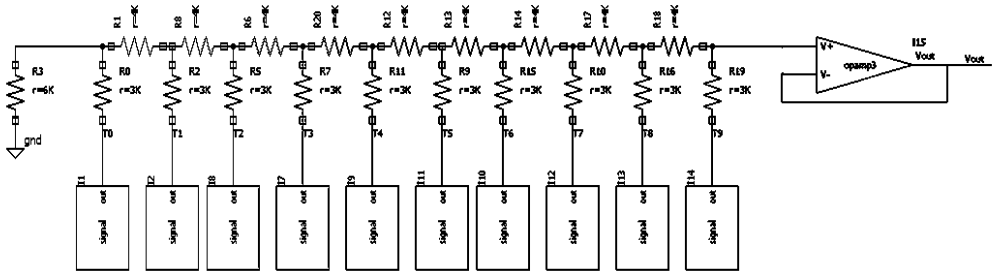

Fig. 3.8: 10-Trit Ternary DAC simulated in Symica DE

It is a 10-Trit Ternary DAC with a resistive ladder network of 3K, 4K and 6K. The ten ternary inputs (T0, T1, … T9) are applied directly to the input of the ADC. The ternary input signals are of unbalanced type i.e. (0,1,2). For the sake of simplicity, we have kept the Vs at 2 Volts which means that logic level 2 (Vs) corresponds to 2 Volts, Logic level 1 (Vs/2) corresponds to 1 Volts and logic level 0 (GND) corresponds to 0 volts respectively. For simulation purposes we have used an ideal opamp to implement the voltage follower at the output end. Another advantage of using this circuit is that we can control the gain of the circuit by adding a couple of resistors in the feedback loop of the Op-amp. This might help in scaling up/down the output voltage for certain applications.

Another advantage of using the 4R/3R implementation is that the ratio accuracy and thermal tracking of these resistors might be improved in comparison to R/2R networks because of the nearly equal values of these resistances.

CHAPTER 4: RESULTS

4.1. SIMULATION RESULTS-

A 10-Trit ternary Digital to Analog Converter has been implemented and simulated using Symica DE software. A staircase waveform with varying Time period was applied as the input signals (T0, T1, T2… T9) to the T-DAC circuit. The following table lists the Time period of all input signals-

Table 4.1: Time Period of Ternary Input Signals (T0, T1,… ,T9)

S. No.	Name of Signal	Time Period (ns)
1.	**T0**	3 ns
2.	**T1**	9 ns
3.	**T2**	27 ns
4.	**T3**	81 ns
5.	**T4**	243 ns
6.	**T5**	729 ns
7.	**T6**	2,187 ns
8.	**T7**	6,561 ns
9.	**T8**	19,683 ns
10.	**T9**	59,049 ns

The simulation results of the 10-trit T-DAC are shown in the following figures (Fig. 4.1 to 4.4)-

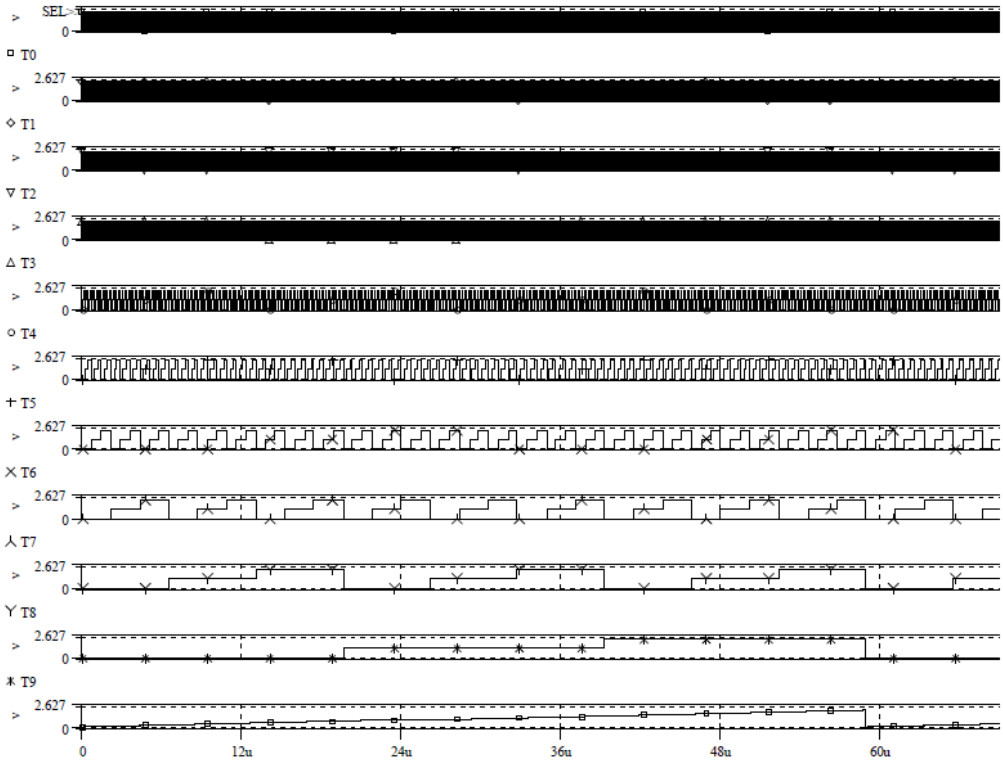

Fig. 4.1: Input Vs. Output characteristics of the 10-trit DAC

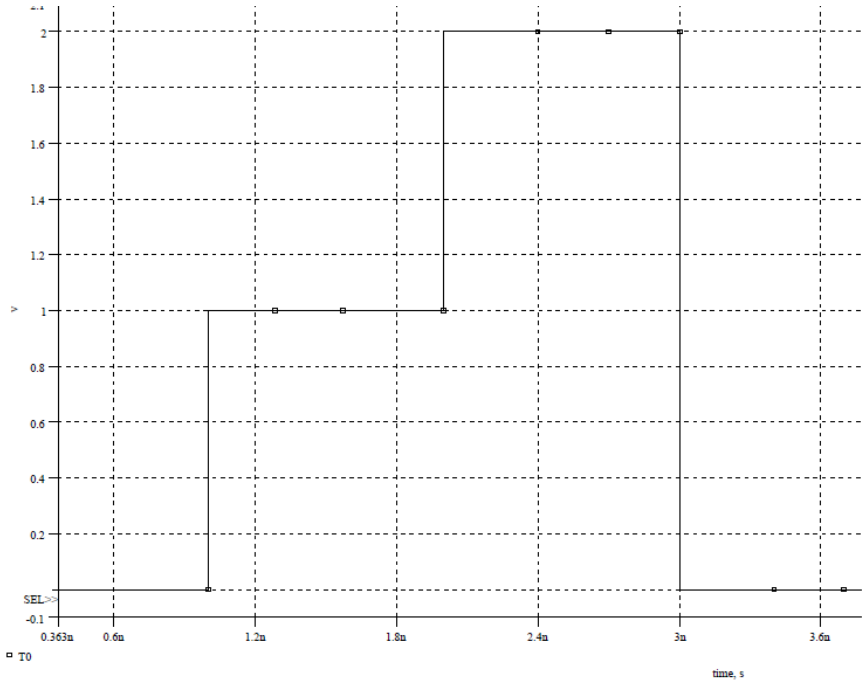

Fig. 4.2: Zoomed section of the input T0 to show waveform

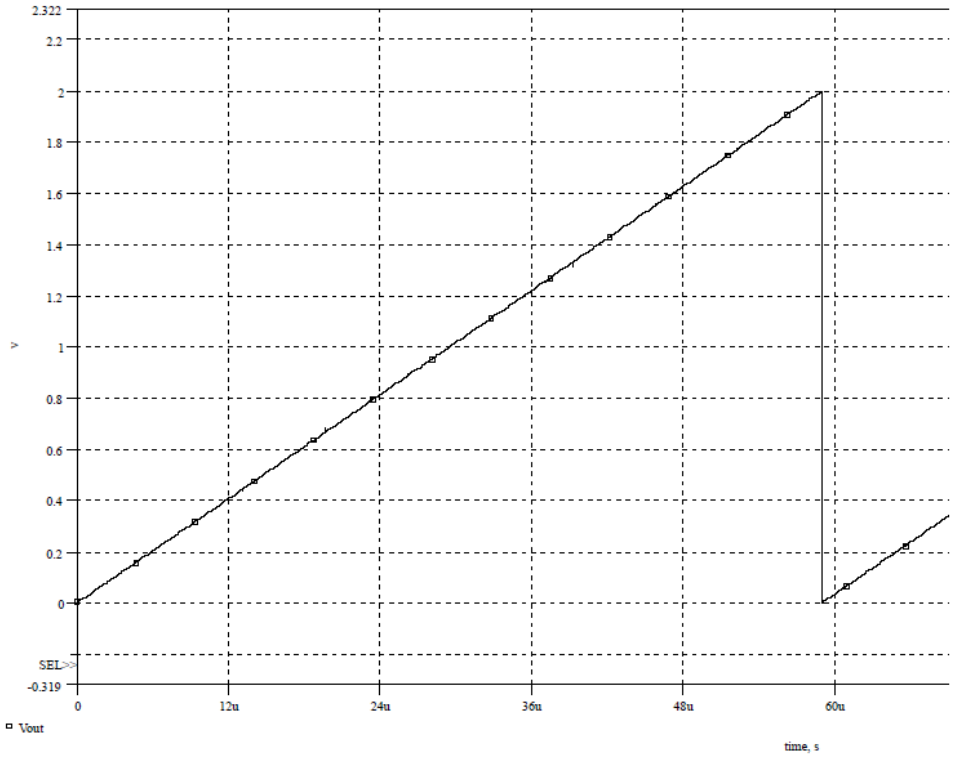

Fig. 4.3: Output characteristics of the 10-trit DAC for a staircase input

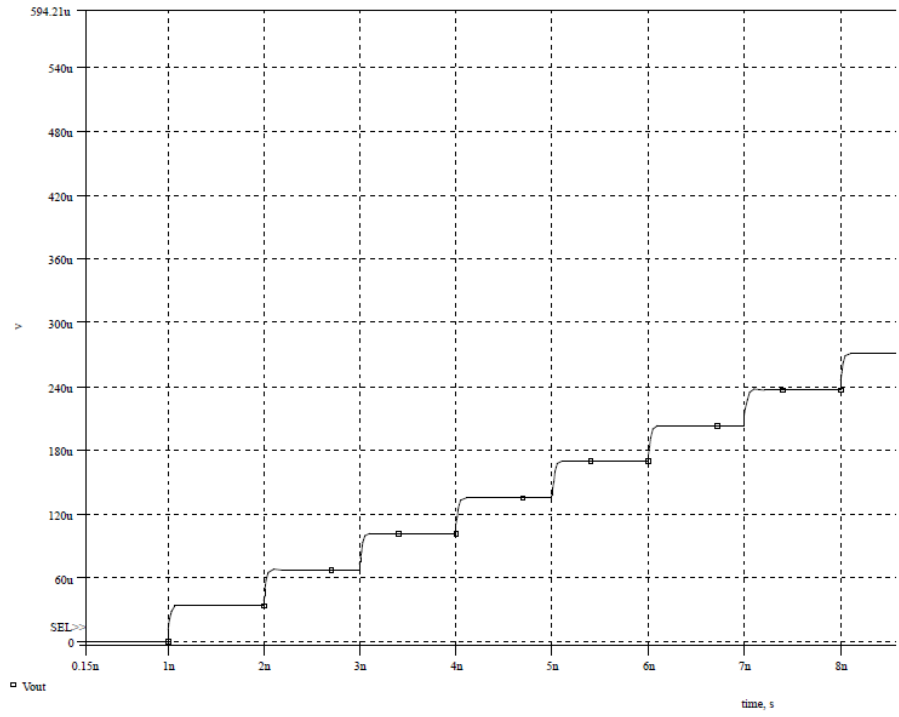

Fig. 4.4: Zoomed section of the output Vout to show waveform clearly

The zoomed section of the input signal T0 (Fig. 4.2) shows that the LST of the digital code applied on our 10-trit T-DAC changes every one nano second. The zoomed section of the output signal Vout (Fig. 4.4) shows that for every change in the input digital code, there is a corresponding change in the output signal Vout at intervals of 1 nano second. The output characteristics of the 10-trit DAC (Fig. 4.3) show that the time period of the DAC output is the the same as the time period of the MST of the DAC input i.e. 59049 nano seconds.

4.2. PERFORMANCE PARAMETERS OF THE T-DAC –

The following table gives a list of the performance parameters of the 10-trit ternary DAC that was simulated in this project-

Table 4.2: Performance Parameters of the T-DAC

S. No.	Characteristic	Proposed Design
1.	Resolution (no. of output levels)	**59049**
2.	Least Significant Trit (Volts)	**33.87017µV**
3.	Gain Error (Volts)	**4.00006µV**
4.	DNL Error (Volts)	**-16.0376nV**
5.	INL Error (Volts)	**-946.952µV**
6.	Settling time (sec)	**22.3592ps**
7.	Total Unsettled Error (Volts or % of FSR)	**946.960µV or 0.047% of FSR**

4.3. CONCLUSION & FUTURE SCOPE-

In this project a ternary Digital to Analog converter has been designed and a 10-trit T-DAC was implemented using this methodology. The new circuit solves several problems encountered in the previous circuits proposed in [15-19]. The performance analysis of the circuit shows a 57 times higher resolution than a

10-bit binary DAC. Further, the circuit has a very low total unsettled error of 0.047% of the FSR. The simulation results indicate a substantial improvement over the existing binary DACs. As an extension of this work, DACs of other bases (other than 2 or 3) can be developed using a similar approach for specific applications. The N-ary DACs of higher bases could provide an even higher resolution as well reduce the ladder stages thereby reducing the circuit complexity, fabrication costs and power consumption. Another area of research could be integration of ternary logic gates, memory cells and T-DACs and T-ADCs to create new Ternary microcontrollers and microprocessors.

REFERENCES

[1] Abdellatif Bellaour, Mohamed I.Elmasry “Low-Power Digital VLSI Deign: Circuits and Systems”. Springer Science + Business Media LLC

[2] S. Lin, Y.-B. Kim, and F. Lombardi, ``CNTFET-based design of ternary logic gates and arithmetic circuits," IEEE Trans. Nanotechnol., vol. 10, no. 2, pp. 217225, Mar. 2011.

[3] S.L. Hurst, “Multiple-valued logic its status and its future,” IEEE Transactions on Computers, vol. 133, no. 1, pp. 1160–1179, December 1984, 10.1109/TC.1984.1676392.

[4] G. Hills, M.G. Bardon, G. Doornbos, D. Yakimets, P. Schuddinck, R. Baert, D. Jang, L. Mattii, S.Y. Sherazi, D. Rodopoulos, R. Ritzenthaler, C.-S. Lee, A. Thean, I. Radu, A. Spessot, P. Debacker, F. Catthoor, P. Raghavan, M. Shulaker, H.-S. Philip Wong, and S. Mitra, “Understanding energy efficiency benefits of carbon nanotube field-effect transistors for digital VLSI,” IEEE Transactions on Nanotechnology, vol. 17, no. 6, pp. 1259-1269, Nov. 2018, 10.1109/TNANO.2018.2871841.

[5] A. D. Zarandi, M. R. Reshadinezhad and A. Rubio, "A Systematic Method to Design Efficient Ternary High Performance CNTFET-Based Logic Cells," in IEEE Access, vol. 8, pp. 58585-58593, 2020, doi: 10.1109/ACCESS.2020.2982738.

[6] R. A. Jaber, A. Kassem, A. M. El-Hajj, L. A. El-Nimri and A. M. Haidar, "High-Performance and Energy-Efficient CNFET-Based Designs for Ternary Logic Circuits," in IEEE Access, vol. 7, pp. 93871-93886, 2019, doi: 10.1109/ACCESS.2019.2928251.

[7] Z. T. Sandhie, F. Uddin Ahmed and M. H. Chowdhury, "Design of Ternary Master-Slave D-Flip Flop using MOS-GNRFET," 2020 IEEE 63rd International Midwest Symposium on Circuits and Systems (MWSCAS), Springfield, MA, USA, 2020, pp. 554-557, doi: 10.1109/MWSCAS48704.2020.9184618.

[8] Mohammad Hossein Moaiyeri, Molood Nasiri, Nooshin Khastoo, "An efficient ternary serial adder based on carbon nanotube FETs", Engineering Science and Technology, an International Journal, Volume 19, Issue 1, 2016, Pages 271-278, ISSN 2215-0986, https://doi.org/10.1016/j.jestch.2015.07.015 (http://www.sciencedirect.com/science/article/pii/S2215098615001214)

[9] Predictive Technology Model, *Post-Silicon Devices,* Nanoscale Integration and Modeling (NIMO) Group, Feb. 28, 2008. Accessed on Aug. 3, 2021. [Online]. Available: http://ptm.asu.edu/postsi.html

[10] Team PSpice, *How to resolve convergence error,* Cadence Design Systems, Aug. 10, 2016. Accessed on Aug. 3, 2021. [Online]. Available: https://www.pspice.com/how-resolve-convergence-error

[11] S. Garg, *Convergence error in Transient Analysis,* Cadence Design Systems, (2014). Accessed on Aug. 3, 2021. [Online]. Available: https://community.cadence.com/cadence_technology_forums/f/custom-ic-design/29141/convergence-error-in-transient-analysis

[12] F. Rider, *Convergence issue with verilogA model,* Cadence Design Systems, (2014). Accessed on Aug. 3, 2021. [Online]. Available: https://community.cadence.com/cadence_technology_forums/f/custom-ic-design/30535/convergence-issue-with-veriloga-model

[13] Intusoft, *Solving SPICE Convergence Problems,* Intusoft. Accessed on Aug. 3, 2021. [Online]. Available: http://www.intusoft.com/articles/converg.pdf

[14] MIT, *VerilogA Reference Manual,* MIT, Accessed on Aug. 3, 2021. [Online]. Available: https://lost-contact.mit.edu/afs/cnf.cornell.edu/windows/Program%20Files/LEdit/program%20files/Tanner%20EDA/Tanner%20Tools%20v13.0/Docs/VerilogA_Reference.pdf

[15] F. G. Reinagel, "Trinary Logical Operations and Circuitry with Communication Systems Applications", In Proc. of IEEE Military Communication Conference, 1986.

[16] Stolfi, Guido. (2012). A Ternary Digital to Analog Converter with High Power Output and 170-dB Dynamic Range. https://arxiv.org/ftp/arxiv/papers/1210/1210.6338.pdf

[17] S. Nooshabadi, G. S. Visweswaran and D. Nagchoudhurhi, "Current mode ternary D/A converter," Proceedings Eleventh International Conference on VLSI Design, 1998, pp. 244-248, doi: 10.1109/ICVD.1998.646611.

[18] J. Bowman, *A 9-bit microcontroller DAC using a ternary resistor-ladder,* Blogger, Apr. 19, 2015. Accessed on Aug. 3, 2021. [Online]. Available: http://idle-spark.blogspot.com/2015/04/a-9-bit-microcontroller-driven-dac.html

[19] M. Dunn, *Ternary DAC: Greater resolution, less bits,* EDN, AspenCore Inc., Oct. 2, 2017. Accessed on Aug. 3, 2021. [Online]. Available: https://www.edn.com/ternary-dac-greater-resolution-less-bits/

[20] Texas instruments, *Understanding Data Converters,* Texas Instruments, (1995). Accessed on Aug. 3, 2021. [Online]. Available: https://www.ti.com/lit/an/slaa013/slaa013.pdf

[21] K. Duke, *DAC Essentials: How accurate is your DAC,* Texas instruments, Oct. 9, 2013. Accessed on Aug. 3, 2021. [Online]. Available:

https://e2e.ti.com/blogs_/b/analogwire/posts/dac-essentials-how-accurate-is-your-dac

[22] K. Duke, *DAC Essentials: The pursuit of perfection*, Texas instruments, Mar. 8, 2013. Accessed on Aug. 3, 2021. [Online]. Available: https://e2e.ti.com/blogs_/b/analogwire/posts/dac-essentials-the-pursuit-of-perfection

[23] Ques10, *Performance Parameters of DAC*, Ques10, (2019). Accessed on Aug. 3, 2021. [Online]. Available: https://www.ques10.com/p/36764/performance-parameters-of-dac-1/

[24] S. Arar, *What Are the DNL and INL Specifications of a DAC? Non-Linearity in Digital-to-Analog Converters*, All About Circuits, EETech Media, LLC, Mar. 13, 2019. Accessed on Aug. 3, 2021. [Online]. Available: https://www.allaboutcircuits.com/technical-articles/understanding-dnl-and-inl-specifications-of-a-digital-to-analog-converter/

[25] Wikipedia, *Digital-to-analog converter*, Wikipedia, May. 26, 2021. Accessed on Aug. 3, 2021. [Online]. Available: https://en.wikipedia.org/wiki/Digital-to-analog_converter