STUDY AND IMPLEMENTATION OF THRESHOLD TYPE BINARY MEMRISTOR EMULATOR

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS FOR THE AWARD OF THE DEGREE OF

MASTER OF TECHNOLOGY

IN

VLSI DESIGN & EMBEDDED SYSTEMS

Submitted by:

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

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I, Juli Kumari Roy, Roll No. 2K19/VLS/07 student of MTech (VLSI & Embedded systems), hereby declare that the work presented in this thesis designated "**Study and implementation of Threshold Type binary memristor emulator"** is done by me and submitted to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in fractional fulfillment of the prerequisite for the award of the degree of Master of Technology.

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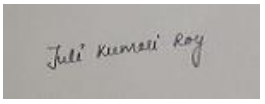

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CERTIFICATE

I hereby certify that the Project Dissertation titled "**Study and implementation of Threshold Type binary memristor emulator**" which is submitted by **Juli Kumari Roy, 2K19/VLS/07**, to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the prerequisite for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date**:**

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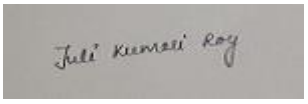

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ABSTRACT

Memristor is a fourth basic circuit element which depicts the relationship between charge (q) and flux (ϕ). There is a lean presence of fabricated memristors in the market due to complexities involved in its processing. Therefore, significant research efforts are made towards presenting emulators that mimic memristor behaviour.

In this project, new memristor emulator circuit has been designed based on DVCC and CFOA. The emulator consists of subtractor, inverting amplifier, integrator, bistable circuit, inverting summing amplifier, multiplier and voltage into current to ensures floating characteristic of the emulator. The subtractor senses the memristor voltage. The diodes in anti-parallel configuration provides threshold sensitive behaviour of the emulator which may be adjusted by resistor ratio. The integrator ensures the dependence of memductance on history state. The bistable circuit provides non-volatility and bistable properties of the emulator. The proposed circuit uses lesser number of resistor than the available binary memristor circuit. The proposal has been verified through Pspice simulations.

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LIST OF ABBREVIATIONS

CCII	Second-generation Current Conveyor
OTA	Operational Transconductance Amplifier
VDCC	Voltage Differencing Current Conveyor
VDTA	Voltage Differencing Transconductance Amplifier
CBTA	Current Backward Transconductance Amplifier
CFOA	Current Feedback Operational Amplifier
DVCCTA	Differential Voltage Current Conveyor Transconductance Amplifier
DVCC	Differential Voltage Current Conveyor

CHAPTER -1

INTRODUCTION

1.1 Background

MEMRISTOR is a circuit element with excellent features memory and neuromorphic application characteristics. It is non-volatile and has a very small size of just a few nanometres, making it suitable for memory applications. It also has pulse-based operation and adjustable resistance, which are required for regulating the synaptic weights of neuromorphic cells for neuromorphic applications. Chua proposed the memristor (memristor+ resistor) as a new passive circuit element in 1971, which offers the needed fundamental relationship between charge and flux linkage [1]. Due to their particular behaviour and properties, the memristors created by Hewlett-Packard (HP) Laboratories in 2008 by Strukov et al. [2] with TiO2 are well known. The pinched hysteresis loop in the current versus voltage plane under sinusoidal excitations is a common property of both the memristor and the memristive device. As a result of these occurrences, the devices resistance is dependent on the input current or voltage history, and it can therefore act neural network synapses. Despite the high level of interest in the memristor among scientists, commercially available memristors are unlikely to appear in the near future due to the high cost and technical challenges of fabricating nano-scale devices. To develop real world application circuits that use memristors properties, various circuit substitutes that behave like memristors are required. SPICE macro models [3–6] have been presented by numerous research groups and are suitable for simulating memristor. Macro models, on the other hand, are not hardware and cannot be utilised to create physically implementable memristor application circuits. As a result, emulators that can emulate the behaviour of real memristors are required. The processing difficulties in the production at memristor at nanoscale has directed research in making memristor emulators based on active blocks. Floating and grounded memristor emulators are the two forms of memristor emulators, based on their architectures. The analogue active blocks of floating-type memristors are identical to a second-generation current conveyor (CCII), a multiplier, and an Op-amp [7-8]. CCII and operational transconductance amplifiers (OTAs) [9] can be used to create a memristor emulator that is electronically controllable but has a restricted frequency response. A charged controlled memristor emulator based on DVCCTA has been presented in [10]. [11] describes a memristor emulator utilizing the IC AD844AN

and an analogue multiplier, however the number of active and passive parts necessary to create this type of emulator circuit is greater. In [12] proposes a memristor emulator with four CCIIs and one multiplier, as well as various passive components, in an incremental design. One DDCC and one multiplier were utilized as active elements in the construction of a memristor emulator in [13], and the circuit performed well up to 1 MHz. Using CCTA as an active element and a few passive components, a floating/grounded type memristor [14] has been presented. In [15] employed two CFOAs as active elements and one diode as a nonlinear element to build an emulator circuit, and it was updated again in [16], however this time an OTA was used instead of a diode. The emulator circuit illustrated in [17] is made up of two AD844ANs with an analogue multiplier and can operate at a frequency of up to 160 kHz. [18] describes a modification of this emulator that can operate at up to 860 kHz. A grounded memristor emulator has been built in [19] that can be programmed in both incremental and decremental modes utilising one VDTA and one capacitor. In [20], describes a flux-controlled grounded/floating-type memristor emulator with two OTAs and one capacitor that can function at up to 8 MHz. One CCTA and one CCII were used as active elements in [21] to create a floating-type memristor emulator that can work at up to 5 MHz.

Memristor, a passive circuit element, featuring relationship between Charge and Flux [2], having applications in circuit designs like memory [22], digital circuits [23-24], neuro network [25], chaotic systems [26-27] and analog circuits [28-29]. Memristor is still not available as a commercial component due cost and technical difficulties in fabricating nanoscale devices. However, memristor emulators are cost-efficient and easy to implement. Analog building blocks are used to emulate memristor behavior in [7,13,14,30,31,32,33] while microcontroller-based emulator circuits are presented in [34-36]. Recently there is an interest in design binary memristor. These are based on low pass filter [37]and thresholding concept [38]. Thus, there is limited literature available for threshold type memristor emulator.

1.2 Objective

The main objective of this project is to present new structures for threshold-type binary memristor emulator based on CFOA and DVCC.

1.3 Organization of Thesis

In Chapter 1, there is a basic introduction of Project

In Chapter 2, current feedback operational amplifier and its basic circuits application are given.

The Chapter 3 presents an overview of DVCC.

In Chapter 4, the proposed memristor emulator circuit based on DVCC and CFOA are detailed and verified through simulations. All simulation results for evaluating the properties of the proposed memristor emulators circuit are included.

Chapter 5 describes Conclusion & Future Scope of this project.

CHAPTER-2

CURRENT FEEDBACK OPERATIONAL AMPLIFIER

This chapter describes current feedback operational amplifier. Some of the CFOA based applications such as inverting voltage amplifier, non-inverting amplifier, summing amplifier, subtractor amplifier, integrator and bistable circuit are explained. Their characteristics have been simulated and verified by Pspice.

2.1 The CFOA

The CFOA uses a second-generation current conveyor followed by a voltage buffer. A simplified symbolic diagram is shown in Fig. 2.1[39] and its characteristics equations are given by (2.1).

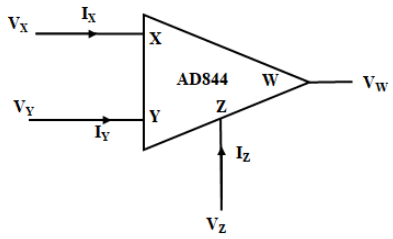


Fig. 2.1 Symbolic diagram of AD844 [39]

$$I_Y = 0$$

$$V_X = V_Y$$

$$I_Z = I_X \qquad (2.1)$$

$$V_W = V_Z$$

2.2 Basic Circuit Applications of CFOA

This section describes the basic circuit applications of CFOA which have been used in this project.

2.2.1 Inverting Voltage Amplifier

The inverting voltage amplifier shown in Fig. 2.2. it consists of an CFOA and two resistances R_1 and R_2, has a finite input impedance given by R_1 which must be taken much larger than the input resistance of the CFOA which is typically of the order of 65ohm.

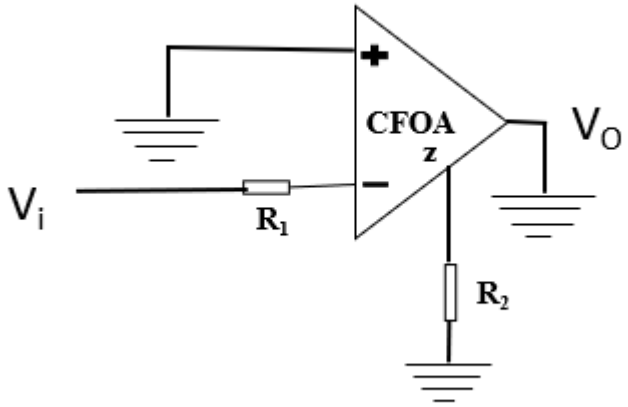


Fig. 2.2 Inverting Voltage Amplifier [40]

the transfer function can be computed as

$$\frac{V_O}{V_i} = \frac{-R_2}{R_1} \tag{2.2}$$

2.2.2 Non-Inverting Amplifier

A non-inverting amplifier consist of a CFOA and two resistances R_1 and R_2 as shown in Fig.3.3.

The resulting transfer function as

$$\frac{V_O}{V_i} = \frac{R_2}{R_1} \tag{2.3}$$

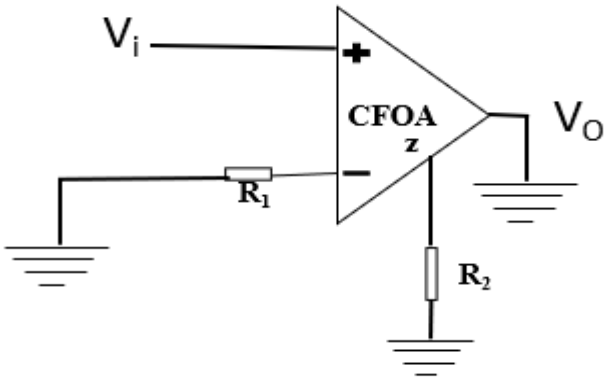


Fig. 2.3 Non-Inverting Amplifier [40]

2.2.3 Summing Amplifier

An CFOA based summer is shown in Fig. 2.4 and this circuit makes use of a single CFOA.

The output voltage Vo can be written as:

$$\text{Vo} = -\left(\frac{R_3}{R_1} V_i + \frac{R_3}{R_2} V_s\right) \tag{2.4}$$

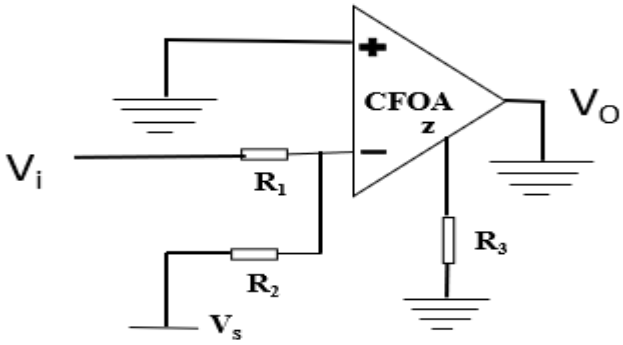


Fig. 2.4 Summing amplifier

2.2.4 Subtractor Amplifier

Considering the CFOA to be ideal the output voltage for the circuit shown in Fig. 2.5 can be expressed

$$V_O = -\frac{R_2}{R_1}(V_1 - V_2) \quad (2.5)$$

The circuit of Fig. 2.5 can also be used as a subtractor if R_1 = R_2 = R and the voltage at the output can be written as

$$V_O = -(V_1 - V_2) \quad (2.6)$$

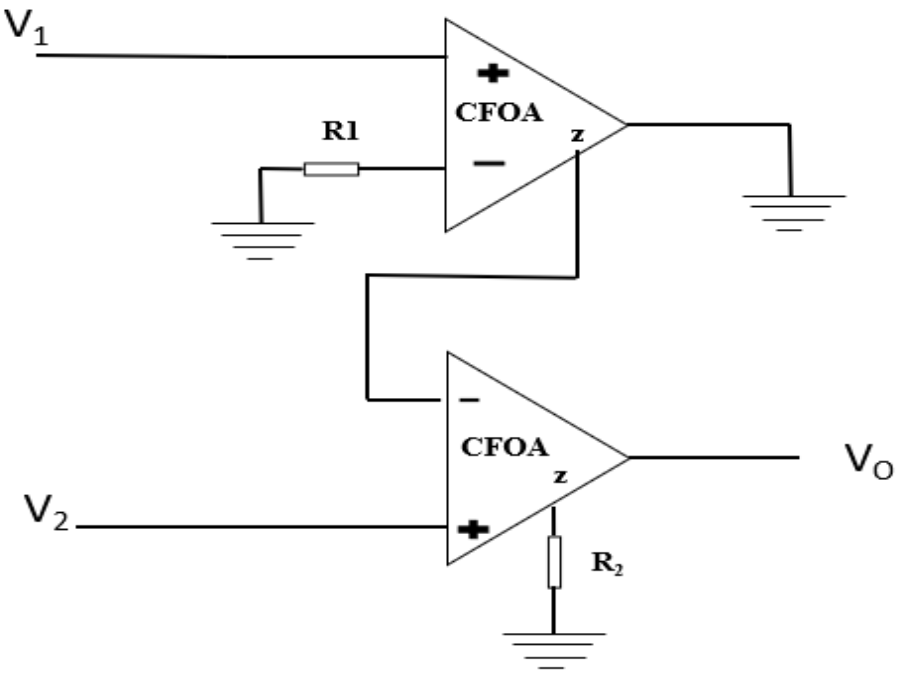


Fig. 2.5 Subtractor Amplifier

2.2.5 Integrator

The circuit shown in Fig. 2.6 represents an inverting integrator. Assuming the CFOA to be ideal.

The output voltage V_O is calculated as follows:

$$V_O = -\frac{\omega_O}{S}V_i \quad (2.7)$$

Where $\omega_O = \frac{1}{CR_1}$

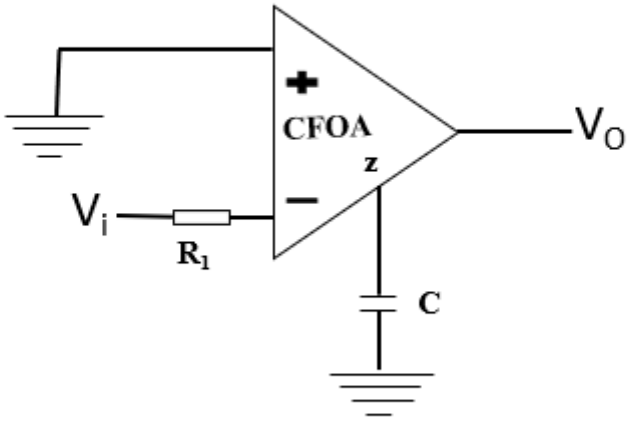


Fig. 2.6 The inverting integrator

2.2.6 Bistable Circuit

A bistable circuit Fig 2.7 is needed next to add non volatility and bistable properties to the emulator. Its output is given by (2.8).

$$\mathrm{Vsc} = \begin{cases} V_{ss} & V_{TH} < V_{int} \\ \text{hold} & V_{TL} \leq V_{int} \leq V_{TH} \\ V_{DD} & V_{int} < V_{TL} \end{cases} \tag{2.8}$$

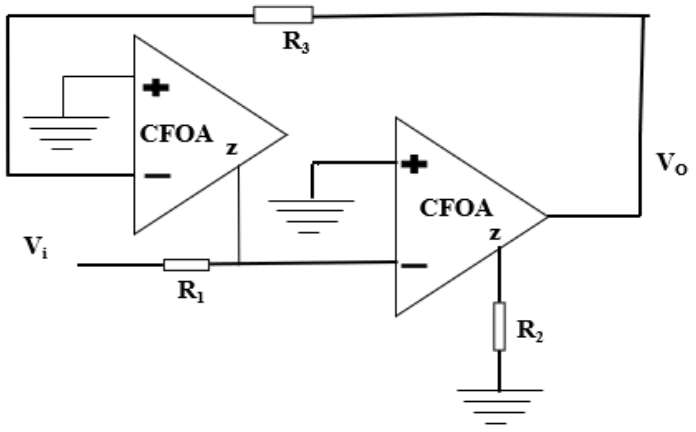


Fig. 2.7 Bistable Circuit

where V_{TH} and V_{TL} correspond to upper and lower threshold voltages of bistable circuit and are related by (2.9)

$$V_{TH} = -V_{TL} = \frac{R_1}{R_3} V_{DD} \quad (2.9)$$

Other symbols in (2.8) have their usual meaning.

2.3 Simulation Results

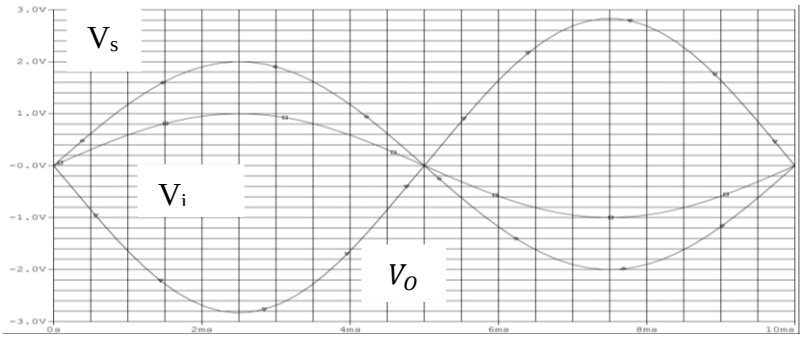
The CFOA based applications such as summing amplifier, subtractor amplifier, integrator and bistable circuit are simulated and verified by Pspice. The power supply of V_{DD} = - V_{SS}=10V is taken.

An input Voltage V_i = 1sin(2000πt) and V_s = 2sin(2000πt) is applied to the summing amplifier. The performance of summing amplifier is verified for (a) R_1=R_2=R_3 =1kΩ, (b)R_1= 1kΩ, R_2=R_3 =2kΩ and (c)R_1=1kΩ, R_2=R_3 =4kΩ, its transient waveform shown in Fig. 2.8.

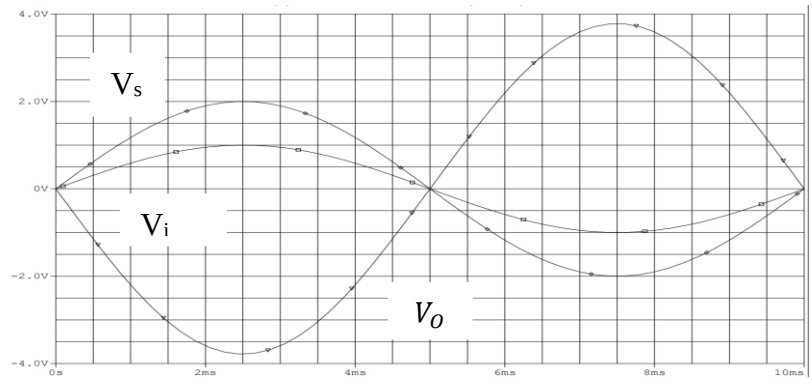
An input Voltage V_1 = 5sin(2000πt) and V_2 = 2.5sin(2000πt) is applied to the subtractor amplifier. Functionality of subtractor can be verified from the Transient response presented in Fig. 2.9 for (a) R_1=R_2=1kΩ (b) R_1 =1kΩ, R_2 =2kΩ (c) R_1 =1kΩ, R_2 =1.5kΩ.

The simulation waveform is depicted in Fig. 2.9 verify the functionality of inverting integrator for R_1 = 100 kΩ and C = 10nF and input Voltage V= 5 sin(1000πt) is applied to the integrator circuits.

An input Voltage V= 8 sin(1000πt) is applied to the bistable circuit. The characteristic of bistable circuit is verified for R_1=5 kΩ, R_2=500kΩ and R_3=10kΩ. The simulation waveform is depicted in Fig. 2.10 which is in tune with theoretical prediction.



(a)



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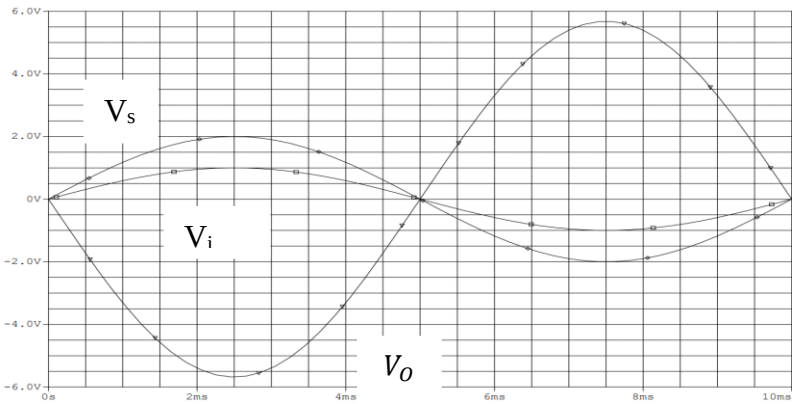
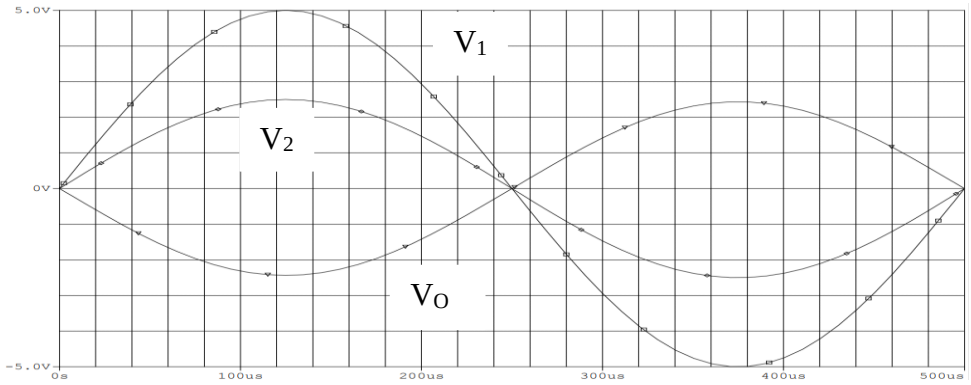
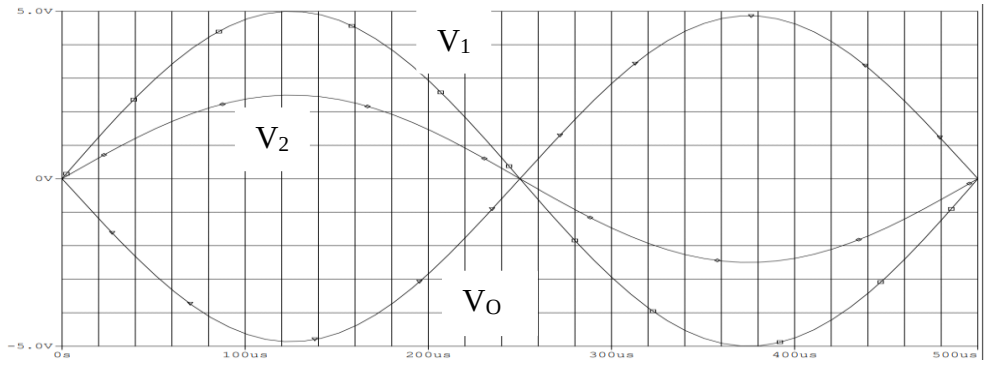


(c)

Fig. 2.8 Transient waveforms of summing amplifier for (a) R_1=R_2=R_3 =1kΩ, (b) R_1= 1kΩ, R_2=R_3 =2kΩ and (c)R_1=1kΩ, R_2=R_3 =4kΩ



(a)



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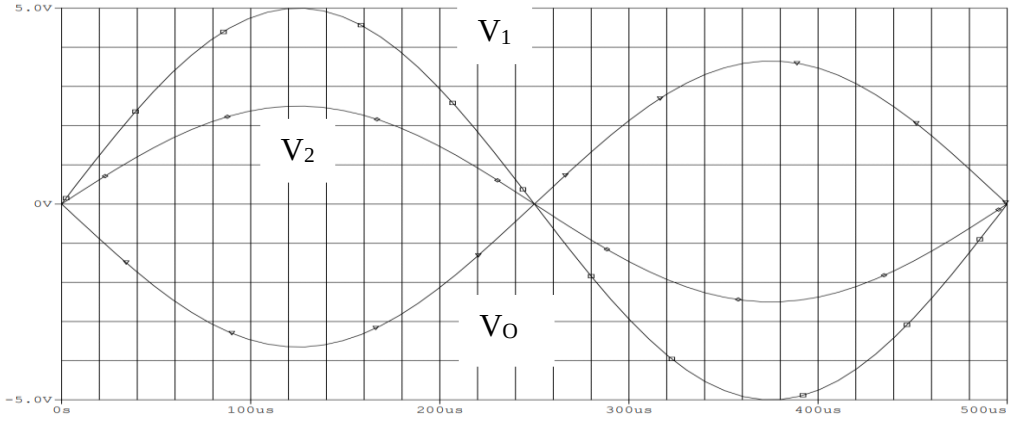


(c)

Fig. 2.9 Transient waveforms of subtractor amplifier for (a) R_1=R_2=1kΩ, (b) R_1= 1kΩ, R_2 =2kΩ and (c)R_1=1kΩ, R_2=1.5kΩ

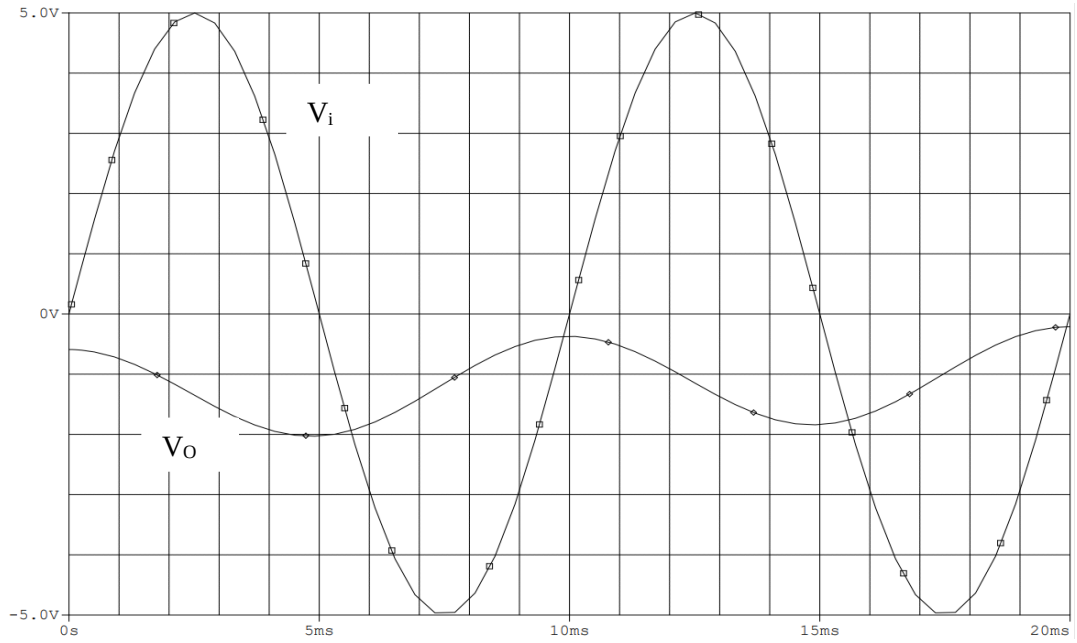


Fig. 2.10 Transient waveform of inverting integrator

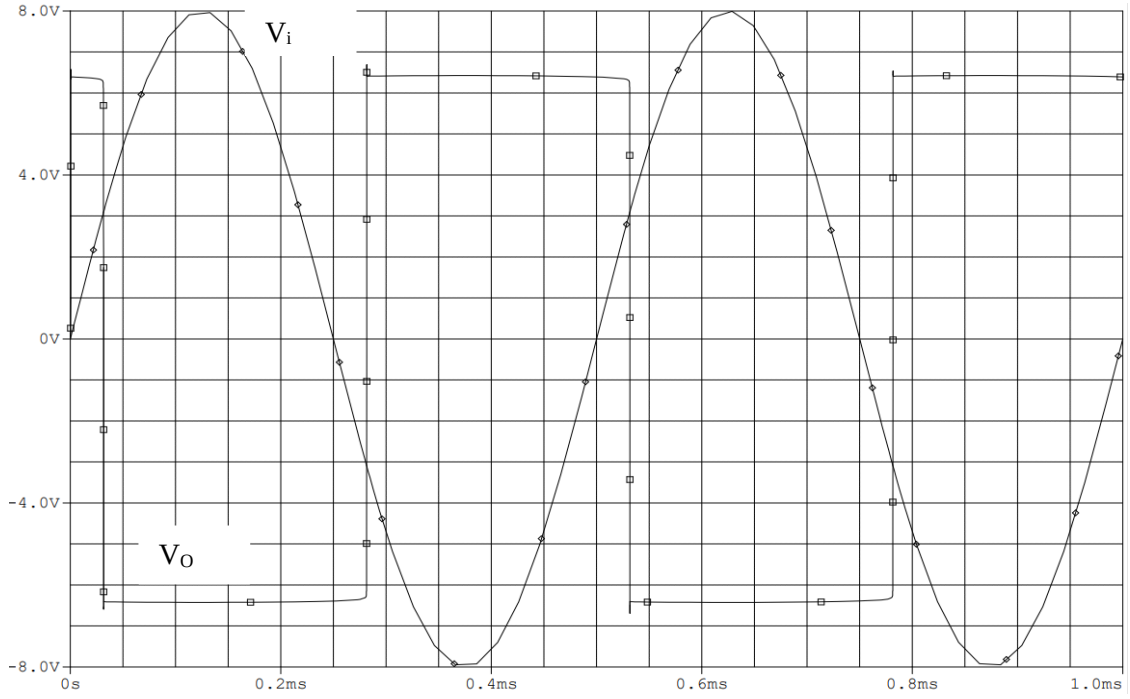


Fig. 2.11 Transient waveform of bistable circuit

According to the above Simulation results the characteristics of CFOA and its applications have been simulated and verified using Pspice.

CHAPTER- 3

DIFFERENTIAL VOLTAGE CURRENT CONVEYOR

Having seen the circuit and applications of CFOA in previous chapter, this chapter explains another block Differential Voltage Current Conveyor (DVCC) which is designed to work with differential signals.

3.1 The DVCC

The Differential Voltage Current Conveyor is capable of processing difference of voltages and also possesses current conveying capability. The DVCC finds wide applications in analog signal processing circuits namely filters [41-42], oscillator [43-44], multivibrator [45] etc.

Fig. 3.1 shows a symbolic representation of DVCC. It has four terminals namely Y_1, Y_2, X and Z. Its principle of operation can be explained by the set of characteristics equations as given in equation (3.1)

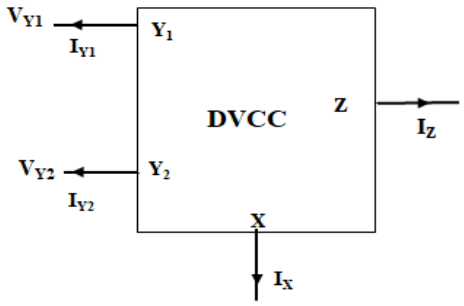


Fig. 3.1 Symbolic diagram of DVCC [46]

I_{Y1}=0
I_{Y2}=0
$V_X = V_{Y1} - V_{Y2}$
$I_Z = I_X$ (3.1)

From equations (3.1), it can be concluded that the difference of voltages applied at Y_1& Y_2 terminals is conveyed to voltage at X terminal while the injected current at X terminal is the conveyed to terminal Z. Since input terminals Y_1 & Y_2, have high input impedances, hence no current flows through these terminals.

3.2 Bistable Circuit based on DVCC

The bistable circuit depicted in Fig. 3.2 uses a single DVCC and two resistors. The connection Y_1 to Z provides the positive feedback of bistable circuit. Loop gain of the positive feedback is greater than unity.

The voltage at output node of the bistable circuit varies from high to low and low to high. When the input voltage given by equation (3.2).

$$V_{in} = V_{Y1} - V_X \tag{3.2}$$

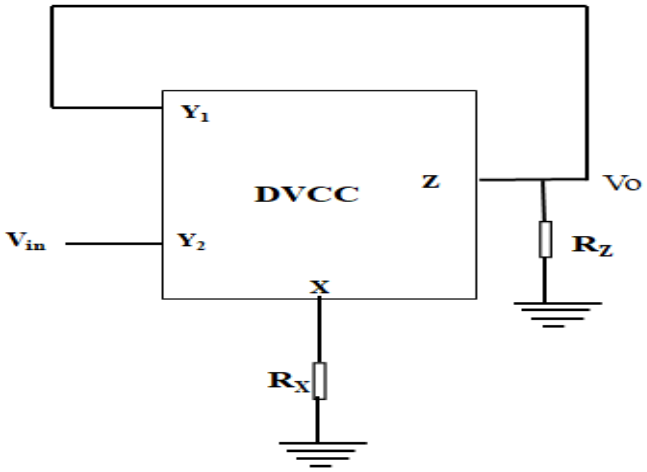


Fig. 3.2 DVCC based Bistable circuit [47]

Where V_{TH} and V_{TL} related to upper and lower threshold voltage of bistable circuit given by (3.3) and (3.4) respectively.

$$V_{TH} = V_{DD} - V_{XDD} \tag{3.3}$$

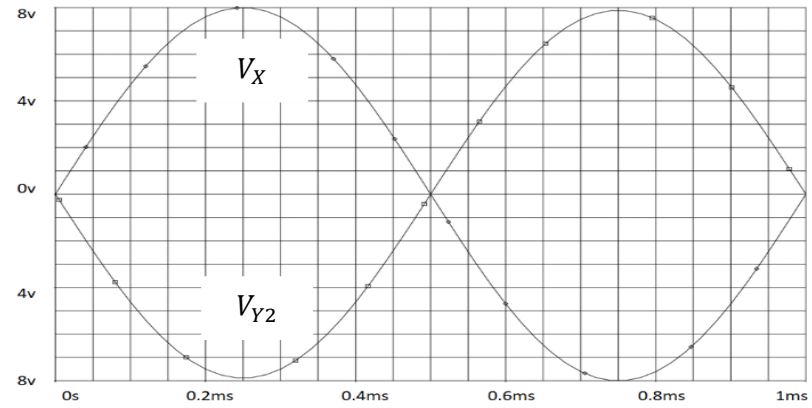
$$V_{TL} = V_{SS} - V_{XSS} \tag{3.4}$$

Where V_{XDD} and V_{XSS} saturated voltage at X terminal.

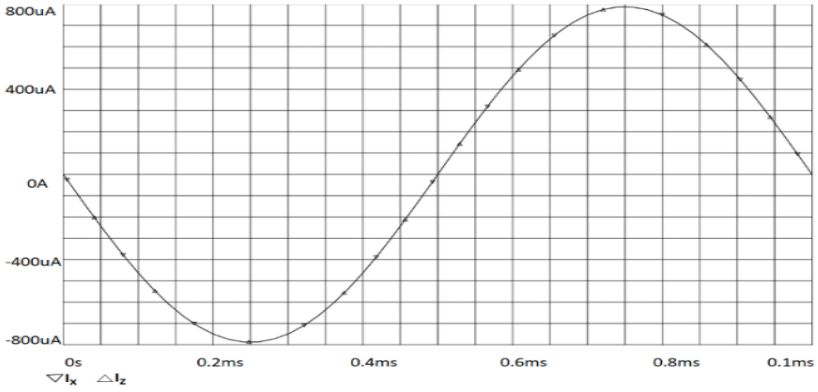
3.2 Simulation Results

The operation of the DVCC is examined through Pspice simulations. The realization of DVCC based on IC AD844.The power supply of V_{DD} = - V_{SS}=10V and R =10kΩ are used. An input Voltage V= 8 sin(2000πt) is applied at Y_2 terminal and Y_1 is connected to ground

in the circuit shown in Fig. 3.1. The output was taken at the Z and *X* terminal of DVCC. The simulation waveforms are depicted in Fig. 3.3 which are in tune with basic characteristics of DVCC and fig 3.4 verified the functionality of bistable circuit which is based on DVCC.



(a)



(b)

Fig. 3. 3 Time domain waveform a) V_X and V_{Y2} and b) I_Z and I_X

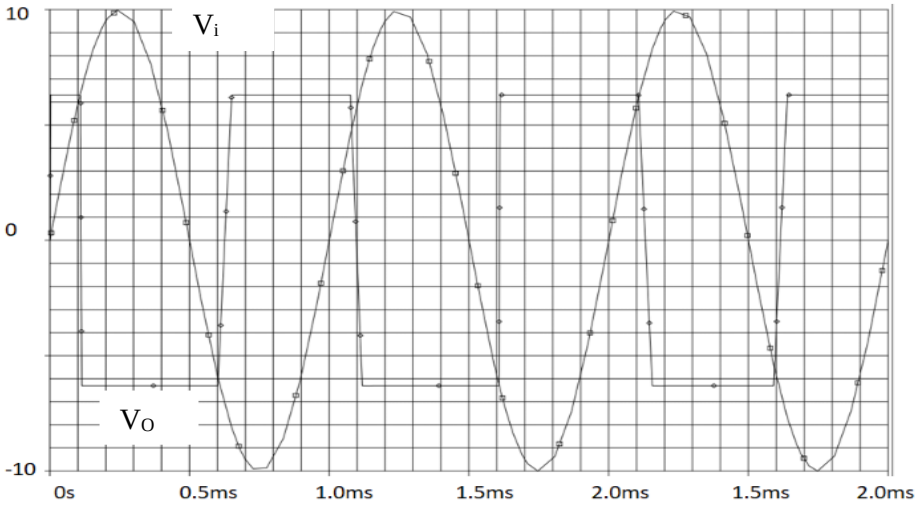


Fig. 3.4 Transient waveform of bistable circuit

The Characteristics of DVCC and its applications have been simulated and verified using PSpice.

CHAPTER- 4

PROPOSED MEMRISTOR EMULATOR CIRCUITS

This chapter presents CFOA and DVCC based binary memristor emulator. The proposed threshold type memristor emulator has the ability of threshold type switching which ensure the basic logic operations essential for non-volatile storage property, on which all its applications are based.

4.1 Mathematical Model

The behaviour of threshold type memristor [47] is briefly reviewed in this section. The current i through voltage controlled memristor is product of memconductance G and voltage v where G is function of time (t), state variable x and voltage v and is given by (4.1).

$$i = G(x, v, t)\, v \tag{4.1}$$

Additionally, the following equation for derivative of state variable x also needs be satisfied

$$\frac{dx}{dt} = f(x, v, t) \tag{4.2}$$

The threshold phenomenon [48] is modelled by (4.3)

$$\frac{dx}{dt} = \beta v + 0.5(\alpha-\beta)\,[|v + v_{th}|-|v - v_{th}| \tag{4.3}$$

Here coefficients α and β characterize the rate of change in state variable and v_{th} corresponds to threshold voltage.

Further, the binary memristor has low resistance and high resistance states which are abbreviated as LRS and HRS. Assuming threshold voltages as Y1 and Y2 the value of resistance is LRS if state variable is less than Y1 and HRS if state variable is greater than Y2. In case the state variable lies in between Y1 and Y2, the memristor holds the state.

4.2 CFOA based Threshold Type Binary Memristor Emulator

The proposed emulator uses 9 CFOAs, one multiplier, two diodes, 14 resistors and one capacitor against 2 CFOAs, 7 opamps, one multiplier, two diodes, 17 resistors and one capacitor. Thus, proposed circuit use lesser number of resistors.

The proposed emulator corresponds to floating memristor, therefore a voltage subtractor circuit is required CFOA 1 and CFOA 2 serve this purpose the output V_{diff} is given by

$$V_{diff} = -\frac{R_2}{R_1}(V_A - V_B),\ V = V_A - V_B = -A_1(V_A - V_B) \tag{4.4}$$

$$\text{where } A_1 = \frac{R_2}{R_1}$$

with the selection $R_2 = R_1$, V_{diff} reduces to

$$V_{diff} = -(V_A - V_B) \tag{4.5}$$

The diode D_1 and D_2 are used to model threshold voltages. Assuming cut in voltage of both the diodes as v_γ, (v_γ may be interpreted as v_{th}) in equation (4.3) to the next stage (comprising of diodes and CFOA 3) is

$$V_d' = A_1V - 0.5[|A_1V + A_2v_\gamma| - |A_1V - A_2v_\gamma|] \tag{4.6}$$

$$\text{where } A_2 = \frac{R_4}{R_3}$$

with $A_2 = 1$, (4.6) reduces to (4.7)

$$V_d' = V - 0.5[|V + v_\gamma| - |V - v_\gamma|] \tag{4.7}$$

It may be noted that for input voltage $\leq |v_\gamma|$ the output is zero. Further the threshold voltage may be varied by changing the value of A_1.The threshold increases with $A_1 < 1$, remains same as diode cut in voltage for $A_1 = 1$and decreases with $A_1 > 1$.

To satisfy (4.1), an integrator is to be placed next. The CFOA 4 performs this function. Its output is given by

$$V_{int} = -\frac{1}{R_5 C}\int V_d' \, dt \tag{4.8}$$

The operating frequency of memristor is decided by the product R_5C i.e., a higher value will yield lower frequency and a lower value result in higher frequency.

A bistable circuit is needed next to add non volatility and bistable properties to the emulator. The CFOA 5 and CFOA 6 provide the functionality of bistable circuit. Its output is given by (4.9).

$$Vsc = \begin{cases} V_{ss} & V_{TH} < V_{int} \\ hold & V_{TL} \leq V_{int} \leq V_{TH} \\ V_{DD} & V_{int} < V_{TL} \end{cases} \tag{4.9}$$

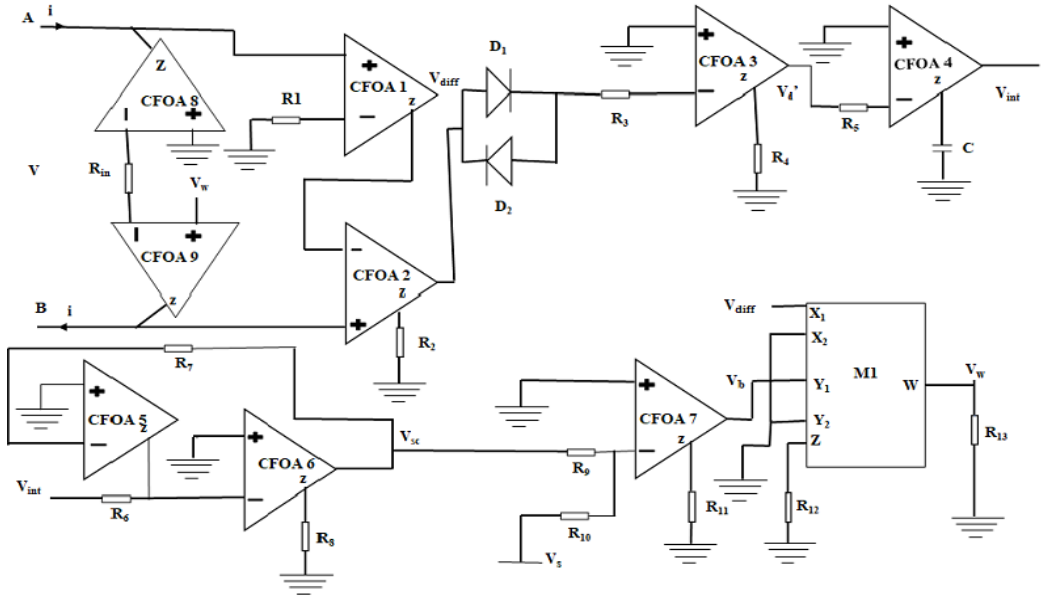


Fig. 4.1 CFOA based proposed threshold binary type emulator

where V_{TH} and V_{TL} correspond to upper and lower threshold voltages of bistable circuit and are related by (4.10)

$$V_{TH} = -V_{TL} = \frac{R_6}{R_7} V_{DD} \tag{4.10}$$

Other symbols in (4.9) have their usual meaning.

The output of bistable circuit passes through an inverting summing amplifier formed by CFOA 7 so that output voltage V_b has single polarity (V_s is used for shifting the voltage level).

A multiplier is necessary to provide voltage proportional to memristor current. AD633 is used for this purpose. It multiplies signals V_{diff} and V_b and uses resistors R_{12} and R_{13} to adjust multiplication coefficient.

$$V_w = R_{in}\, i \tag{4.11}$$

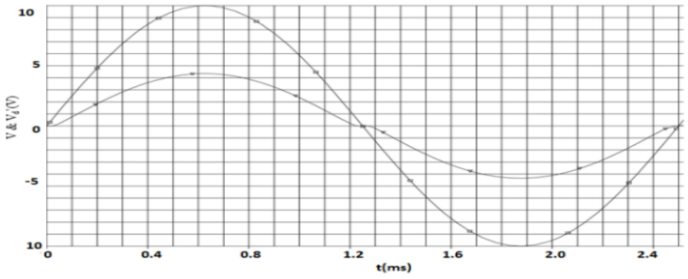
The CFOA 8 and CFOA 9 are used to convert the voltage V_w to memristor current i. The current flowing through R_{in} is given by

$$i = \frac{V_w}{R_{in}} \tag{4.12}$$

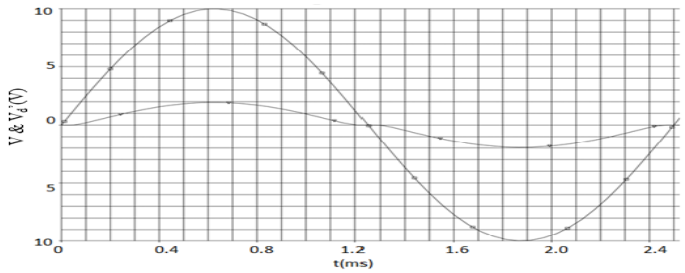
According to the above analysis the proposed circuit emulates threshold type memristor.

4.2.1 Simulation Results

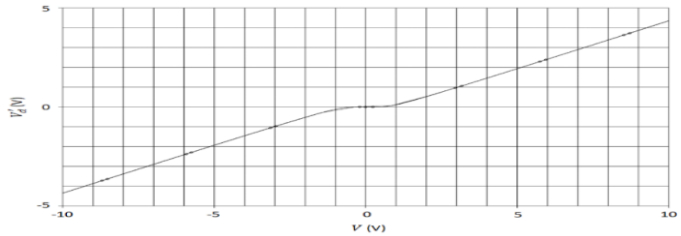
The operation of the proposed emulator is examined through PSPICE simulations. The power supply of V_{DD} = - V_{SS}=10V is taken. An input Voltage V= 10 sin(1000πt) is applied to the circuit Fig. 4.2 depicts the time domain waveforms for V and V_d' for A_1=1 (R_1=R_2=R_3=R_4=10kΩ) and A_1=0.5 (R_1=5kΩ, R_2=2.5kΩ, R_3=10kΩ, R_4=20kΩ). A decrease in threshold voltage is observed which corroborates with theoretical prediction.



(a)



(b)



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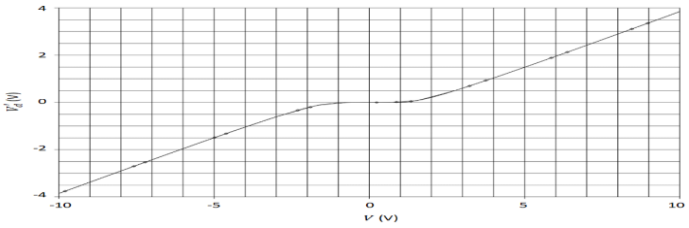


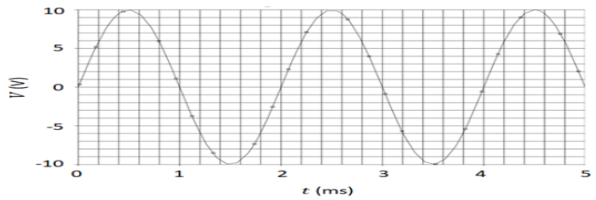
(d)

Fig. 4.2 Transient waveforms of the V and V_d' signal at (a) A_1=1, (b) A_1=0.5, Transfer characteristics of V and V_d' curve at (c) A_1=1, (d) A_1=0.5.

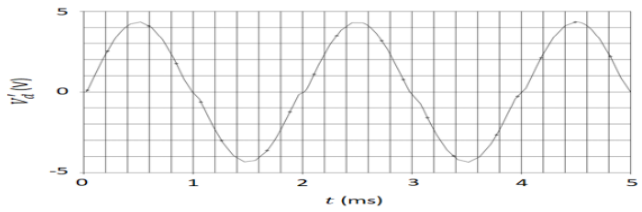
Table 4.1 Component Setting CFOA Based Memristor Emulator

Component	Value
R_3= R_4 =R_5= R_6 = R_7=R_{13}=R_{in}	10kΩ
R_8	500kΩ
R_9	20kΩ
R_{10}	2.1kΩ
R_{11}	7kΩ
R_{12}	5.6kΩ
C	10nF

The functionality of complete circuit is verified for A_1=1 (R_1=R_2=R_3=R_4=10kΩ) and V_s =2.1V. The component settings are listed in Table 1 and for diode D_1 and D_2 D1N4148 is used. The simulation waveforms are depicted in Fig. 4.3 which are in tune with theoretical prediction.



(a)



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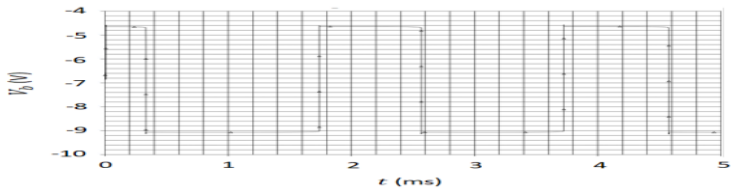

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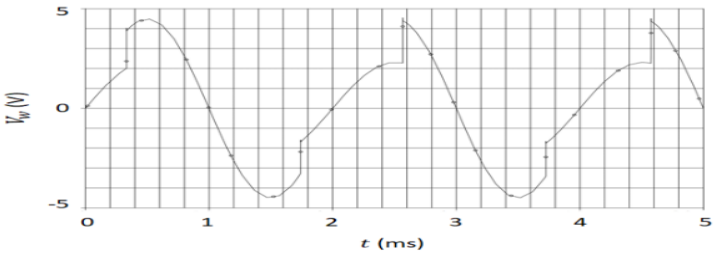
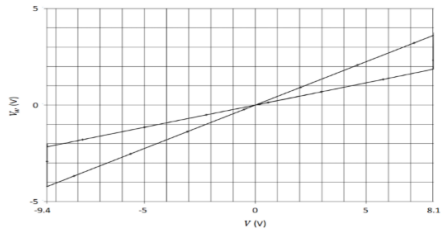
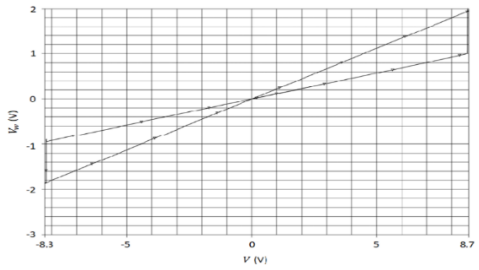


(d)

Fig. 4.3 Time domain waveform (a) V, (b) V_d', (c) V_b, (d) V_w.



(a)



(b)

Fig. 4.4 V versus V_w characteristics of the emulator (a) at A_1=1 (b) at A_1=0.5

The plot of V versus V_w are shown in Fig. 5.4 for A_1=1 (R_1=R_2=R_3=R_4=10kΩ) and A_1=0.5 (R_1=5kΩ, R_2=2.5 kΩ, R_3=10 kΩ, R_4=20kΩ) while keeping another component setting same as given in Table 4.1. The plots correspond to pinched hysteresis loop confirming the functionality of memristor.

4.3 Threshold Type Binary Memristor Emulator based on DVCC

The proposed emulator uses 5 DVCC, two diodes, 9 resistors, one capacitor, and one multiplier against 2 CFOAs, two diodes 7 opamps, 17 resistors, one capacitor and one multiplier. Thus, proposed emulator circuits use lesser number of resistors.

The proposed floating emulator circuits consists of subtractor, integrator, bistable circuit, inverting summing amplifier, multiplier and voltage into current to ensures floating characteristic of the emulator. The subtractor senses the memristor voltage, therefore a voltage subtractor circuit is required DVCC 1 serve this purpose the output V_{SUB} is given by (4.13)

$$V_{SUB} = (V_A - V_B)$$

$$V = V_A - V_B \tag{4.13}$$

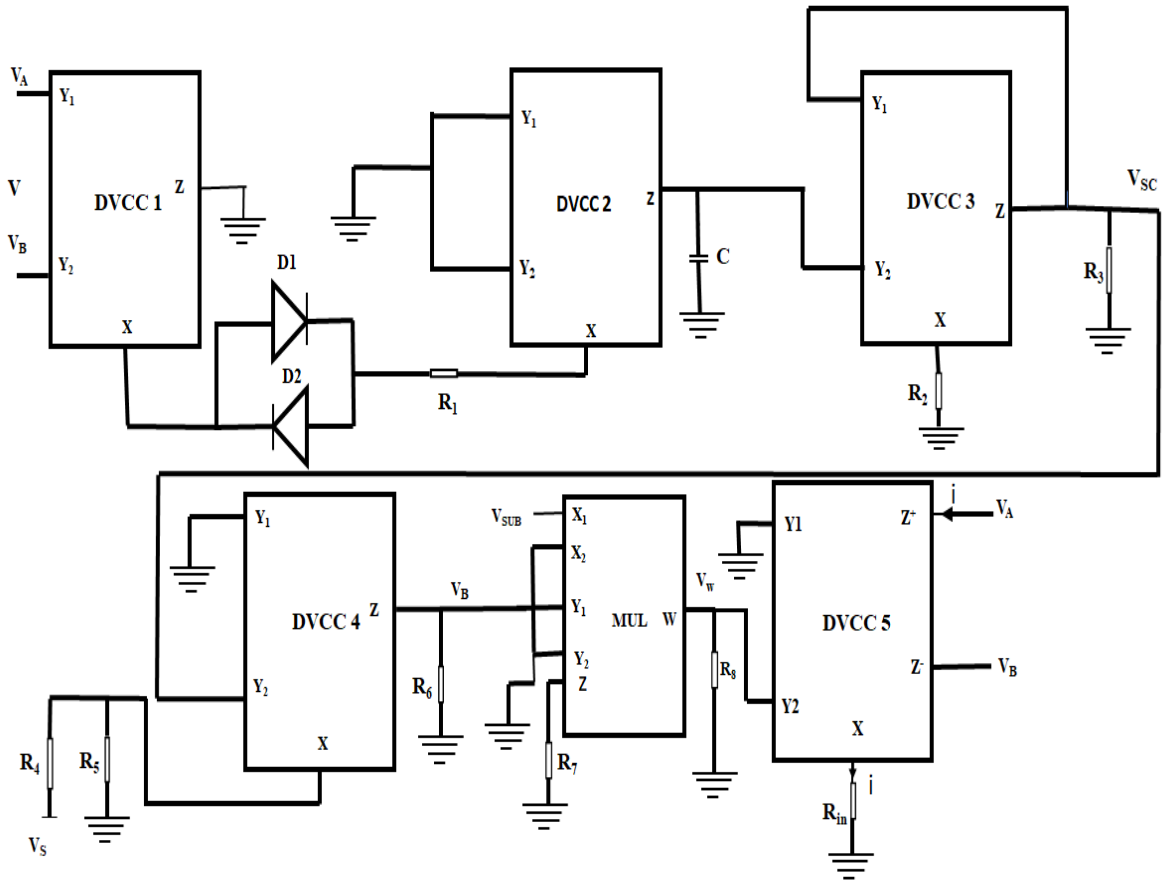


Fig. 4.5 DVCC based proposed threshold binary type memristor emulator

The diode D1 and D2 in anti-parallel configuration provide threshold sensitive behaviour of the emulator which may be adjusted by resistor ratio of DVCC. Assuming cut in voltage of both the diodes as v_{th}, in equation (4.14).

$$V_d' = V - 0.5[|V + v_{th}| - |V - v_{th}|] \tag{4.14}$$

It may be noted that for input voltage ≤ |vth| the output is zero. The threshold voltage remains same as diode cut in voltage, however, by introducing block with gain (G_1) before integrator formed by DVCC2. In presence of gain, (4.14) modifies to

$$V_d' = V - 0.5[|V + G_1 v_{th}| - |V - G_1 v_{th}|] \tag{4.15}$$

It may be noted that the threshold voltage increases when G_1 is less than unity while a decreasing trend is observed for G_1 is greater than unity.

An integrator circuit is needed next to add the dependence of memductance on history state. The DVCC 2 provides the functionality of integrator circuit.

The product of RC performs the operating frequency of memristor emulator, for higher value will produce lower frequency and a lower value result in higher frequency.
For bistable and non- volatility properties to the memristor emulator, a bistable circuit is needed. The DVCC 3 deliver the functionality of bistable circuit. Its output is given by (4.16)

$$\mathrm{Vsc} = \begin{cases} \mathrm{V_{ss}} & \mathrm{V_{TH}} < \mathrm{V_{int}} \\ \mathrm{hold} & \mathrm{V_{TL}} \leq \mathrm{V_{int}} \leq \mathrm{V_{TH}} \\ \mathrm{V_{DD}} & \mathrm{V_{int}} < \mathrm{V_{TL}} \end{cases} \tag{4.16}$$

Other symbols in (4.15) have their usual meaning
The bistable circuit employing a single DVCC and two resistors which shown in Fig. 4.5. The connection Y_1 to Z provides the positive feedback of bistable circuit. Loop gain of the positive feedback is greater than unity.
The voltage at output node of the bistable circuit varies from high to low and low to high. When the input voltage given by equation (4.17).

$$V_{in} = V_{Y1} - V_X \tag{4.17}$$

Where V_{TH} and V_{TL} related to upper and lower threshold voltage of bistable circuit given by (4.18) and (4.19) respectively.

$$V_{TH} = V_{DD} - V_{XDD} \tag{4.18}$$
$$V_{TL} = V_{SS} - V_{XSS} \tag{4.19}$$

The output of bistable circuit passes through an inverting summing amplifier formed by DVCC 4 so that output voltage V_S (V_S is used for shifting the voltage level).

A multiplier is necessary to provide voltage proportional to memristor current. AD633

is used for this purpose. It multiplies signals V_{SUB} and V_S and uses resistors R_7 and R_8 to adjust multiplication coefficient.

$V_W = R_{in}\, i$ (4.20)

The DVCC 5 is used to convert the voltage V_W to memristor current i. The current flowing through R_{in} is given by

$$i = \frac{V_w}{R_{in}} \quad (4.21)$$

The proposed circuits, according to above analysis, emulates a threshold type memristor.

The proposed emulator uses 5 DVCC, two diodes, 9 resistors, one capacitor, and one multiplier whereas the existing counterpart [47] uses 2 CFOAs, two diodes 7 opamps, 17 resistors, one capacitor and one multiplier.

4.3.1 Simulation Results

Pspice simulations are used to verify the proposed emulator circuit functionality. The power supply of V_{DD} = - V_{SS}=10V is taken. An input Voltage V= 10 sin(2000πt) is applied to the circuit shown in Fig. 4.5.

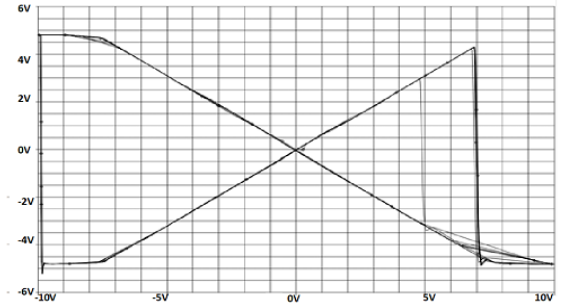
Table 4.2 Component Setting DVCC Based Memristor Emulator

component	***value***
$R_1 = R_2 = R_4 = R_5 = R_6 = R_7 = R_8 = R_{in}$	10 kΩ
C	10nF
R_3	100 kΩ

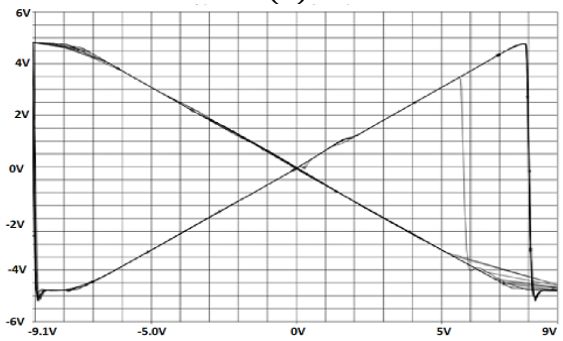
The functionality of complete circuit is verified for G_1=1 and V_S =2.1V. The component settings are listed in Table II and for diode D1 and D2 D1N4001 is used.

The plot of V versus V_W are shown in Fig. 4.6 for G_1=1 and while keeping another component setting same as given in Table 4.2. The plots correspond to pinched hysteresis loop confirming the functionality of memristor.

Simulations are done to examine the frequency-dependent pinched hysteresis loop of the proposed design for different frequencies. The input voltage (V) versus V_W characteristics of the proposed emulator at different input frequencies, i.e.,7kHz, 9kHz, 10kHz and 15kHz are observed and are shown in Fig. 4.7. It is noted that the area of the hysteresis loop is dependent on the frequency of the input signal. The enclosed area of the pinched hysteresis loop decreases monotonically with the increase in frequency of the input.



(a)



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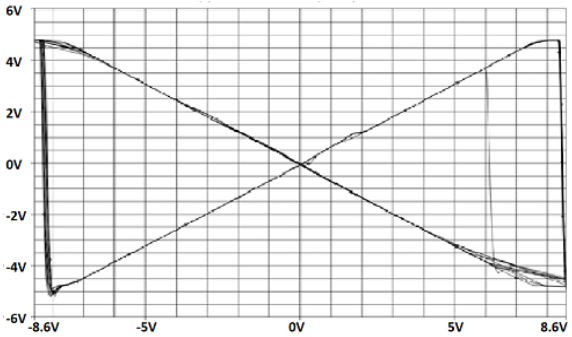

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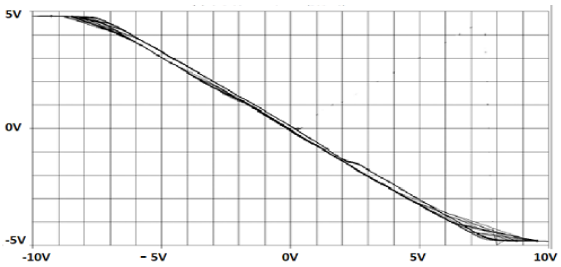

(d)

Fig.4.6 V versus V_W characteristics of the emulator (a) at f=7kHz (b) at f=9kHz (c)at f=10kHz (d) at f= 15kHz

Memristor emulator based on both CFOA and DVCC have been presented in this chapter. The Characteristics of memristor emulator have been simulated and verified.

CHAPTER-5

CONCLUSION AND FUTURE SCOPE

In this thesis, new threshold type binary memristor emulator circuit based on DVCC and CFOA has been proposed. The proposed emulator consists of subtractor, diode, inverting amplifier, integrator, bistable circuit, inverting summing amplifier, multiplier and voltage into current to ensures floating characteristic of the emulator. The diodes in anti-parallel configuration provides threshold sensitive behaviour of the emulator which may be adjusted by resistor ratio. The proposed circuit uses lesser number of resistor than the available binary memristor circuit.

The emulator circuits in this thesis, implemented by using of CFOA and DVCC. The CFOA uses a second-generation current conveyor followed by a voltage buffer and DVCC which is capable of processing difference of voltages. The proposed circuit consists of subtractor, inverting amplifier, integrator, bistable circuit and inverting summing amplifier can be implemented by DVCC as well as CFOA, which reduces number of resistors.

Simulations are done to examine the frequency-dependent pinched hysteresis loop of the proposed design for different frequencies. It was noted that the area of the hysteresis loop is dependent on the frequency of the input signal. The enclosed area of the pinched hysteresis loop decreases monotonically with the increase in frequency of the input. The threshold voltage can be varied by changing the value of gain of the subtractor.

Memristor having applications in circuit designs like memory, digital circuits, neuro network, chaotic systems and analog circuits. The proposed circuit possess adjustable thresholds. Hence, this circuit can be used in multiple applications requiring logical based operations. With these features and components, the proposed circuit can be helpful in further study, simulations and design of memristor.

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List of publications

Paper	Author list. Title. Conference	Status
[1]	Juli Kumari Roy, Neeta Pandey, **"CFOA based Threshold Type Binary Memristor Emulator"** First International Conference on Emerging Trends in Industry 4.0 (2021 ETI 4.0)	Accepted
[2]	Juli Kumari Roy, Neeta Pandey, "**Threshold Type Binary Memristor Emulator based on DVCC"** 8th International Conference on Signal Processing & Integrated Networks (SPIN 2021)	Accepted