IMPLEMENTATION OF OTA USING DIFFERENT METHODOLOGY

A DISSERTATION

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MASTER OF TECHNOLOGY

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Submitted by:

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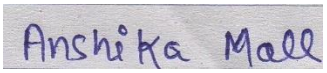
I, Anshika Mall, Roll No. 2K19/VLS/02 student of M.Tech (VLSI & Embedded systems), hereby declare that the work presented in this thesis designated "**IMPLEMENTATION OF OTA USING DIFFERENT METHODOLOGY**" is done by me and submitted to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in fractional fulfillment of the prerequisite for the award of the degree of Master of Technology. This is an original research work and not copied from any source without acknowledging them with proper citation and has not previously published anywhere for the award of any Degree, Diploma Associateship, Fellowship, or other similar title or recognition.



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CERTIFICATE

I hereby certify that the Project Dissertation titled "**IMPLEMENTATION OF OTA USING DIFFERENT METHODOLOGY**" which is submitted by **Anshika Mall, 2K19/VLS/02**, to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the prerequisite for the award of the degree of Master of Technology, is a record of the project work carried outby the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

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ABSTRACT

Manufacturers and designers are looking for methods to construct Smaller-sized high-performance devices with reduced power consumption, and are lighter in weight in today's competitive market. Low static power consumption, complete rail dynamic range, and simplicity of scaling combine to make the ideal mix for high-performance integrated circuits (IC). In many applications, analog integrated circuits, the Operational Transconductance Amplifier (OTA) is the block with so much power consumption. The importance of low power consumption in phone devices is growing, therefore designing a low-power OTA is a problem. For an OTA design, Between speed, power, and gain, there is a trade-off, because these metrics are frequently contradictory.

Two-stage OTAs, cascode OTAs, and folded cascode OTAs are the three types of OTAs that I have implemented in this project work. We discuss different types of OTA that include Single-stage OTA, Two-stage OTA, cascode OTA, Folded cascode OTA.

Also, The comparative analysis of the design and performance of an operational transconductance amplifier using CMOS and FinFET is presented. Active filters and other devices make use of the operational transconductance amplifier (OTA), which needs low power consumption and high gain, and OTA based on FinFET is proposed for this reason. The application of FinFET in analog circuits is a crucial area of study. A simple analysis of various multigate FETs and their advantages over current technology, as well as the need for us to improve such transistors, is presented. The ability to shrink the physical size of such technologies is the driving force behind their growth. The OTA has been implemented using CMOS and 18 nm FinFET models, with all simulations performed in Cadence Virtuoso.

An operational amplifier may not be adequate to be used for an active element in many analog or mixed VLSI applications. For instance, when designing integrated high-frequency active filter circuitry, an OTA, is often used which is a much simpler building block. The term "operational" refers to the fact that the difference of two voltages is used as the input for the current conversion. The size of transistors is decreasing and the power supply is also decreasing as a result of recent advancements in VLSI technology

Most analog circuits with linear input-output characteristics use the OTA as a basic building element. The OTA is commonly utilized in analog circuits such as neural networks, instrumentation amplifiers, ADCs, and filter circuits.

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LIST OF ABBREVIATIONS

VLSI:	Very Large Scale Integrated Circuits
OTA:	Operational Transconductance Amplifier
FET:	Field Effect Transistor
CMOS:	Complementary Metal Oxide Semiconductor
ICS:	Integrated Circuits
OPAMPS:	Operational Amplifiers
MOSFET:	Metal Oxide Semiconductor Field Effect Transistor
RF:	Radio Frequency
EDA:	Electronic Design Automation
SOI:	Silicon On Insulator
SCE:	Short Channel Effects
UGB:	Unity Gain Bandwidth
PM:	Phase Margin

CHAPTER-1

INTRODUCTION

1.1 BACKGROUND

VLSI design (IC design) is a branch of electronics engineering that encompasses the Techniques for logic and circuit design needed to design integrated circuits. Small electronic components are embedded in an electrical network on a monolithic semiconductor to make upintegrated circuits (ICs). The two basic types of integrated circuit design are digital and analogIC design. The goal of digital design is to achieve logical correctness, maximizing circuit density, and effectively route clock and timing signals. Operational amplifiers, linear regulators, phase-locked loops (PLL), oscillators, and active filters are all designed using analog integrated circuits. Gain, matching, power dissipation, and resistance are all aspects of analog design that are primarily concerned with the physics of semiconductor devices. Because the fidelity of analog signal amplification and filtering is frequently crucial, analog ICs use bigger area active components and are typically less dense in circuitry than digital designs.

Prior to the introduction of the design tools based on software and microprocessor, analog integrated circuits (ICs) were developed using parts for the processing kit. Less-complexity circuits, such as op-amps, were used in these ICs, which typically had no more than 10 transistors and few connections. In the 1970s, when computers were first made available, computer programs were created to simulate designs of the circuit with more accuracy than could be achieved by human computation.

SPICE was the first circuit simulator for analog integrated circuits. Using computerized circuit simulation tools, more complex IC designs can be created than hand calculations can achieve, making the design of analog ASICs (Application-specific integrated circuits)

practical. Computerized circuit simulators, such as Cadence Virtuoso, also allow for early detection of design flaws before a physical device is fabricated.

There is a basic study of different multigate FETs and their advantages over existing technology and the need for us to develop such kinds of transistors. This Project will also inform us in implementing OTAs using CMOS & FinFETs in a simulation environment so that we can successfully put forth our proof about the advancement of transistors. We also looked under the scope up to which our concerned technology can be extended. Their immense potential for improving and revolutionalizing the electronic market as we know. These 3D FETs have emerged out from the rest of the transistor technologies currently in development because of their better gate control and overcoming abilities from short channel effects.

The main reason for the development of such technologies is their scope for reduction in their physical size. The circuitries implementing these transistors will have so many advantages over so many factors that will have an astonishing effect on the devices we see today. I have made OTA using CMOS & 18 nm FinFET models.

1.2 OBJECTIVE

The main objective of this project is to present structures for different topologies of Operational transconductance amplifier (OTA) and comparison between them in terms of gain, bandwidth, settling time, speed, size.

The supply voltages are dropping as CMOS technology advances, while the threshold voltages in transistors remain relatively constant. To make things worse, Nano-CMOS transistors' inherent gain is decreasing. In sub-100nm technologies, Traditional vertically stacking (i.e. cascoding) transistors solutions for achieving high gain become less useful.

Horizontal cascading (multistage) is required to realize op-amps or OTA in processes with low supply voltage. This project addresses innovative design strategies for multi-stage OTA realization. When low power, small VDD, and fast speed are needed, both single- and fully differential OTA are provided. The suggested, and experimentally validated, OTA offers significant speed benefits over typical op-amp designs while also requiring a smaller layout area.

1.3 ORGANIZATION OF THESIS

In Chapter 1, there is a basic introduction to the project.

Chapter 2, explains the Literature survey of different topics that, I have implemented in my project.

Chapter 3, presents the comparative analysis of OTA using CMOS & FinFET.

Chapter 4, explains a comparative analysis of different topologies of OTA.

Chapter 5, summarises the project's conclusion and future scope.

CHAPTER-2
LITERATURE SURVEY

2.1 OTA

Analog integrated circuit design with high performance, such as operational transconductance amplifier (OTA) in CMOS technology, has become a major problem in recent years due to increased demand for system on chip (SoC) manufacturers. In an open-loop configuration, the OTA circuit is well-known for its high bandwidth. Bluetooth, Global System for Mobile (GSM) Communication, and Ultra Wide Band (UWB) are employed in multimode transceivers, making them suitable for a wide range of applications [1] [2].

The Operational Transconductance Amplifier (OTA) is similar to traditional Operational Amplifiers in that they both have Differential inputs. The main distinction between an OTA and a traditional operational amplifier is that an OTA's output is in the form of current, whereas a traditional op-amp is in the form of voltage [1].

Operational Transconductance Amplifiers (OTA) are crucial components in a wide range of analog circuits and systems that have traditionally relied on OPAMPs. Recently, work has begun on developing OTA circuits that are extremely linear, require less power, and operate at lower supply voltages [1].

An operational transconductance amplifier (OTA) is like OP-AMP in a lot of aspects. The only difference is the OTA circuit uses an outside bias current Ibias, which is accountable for its flexibility and tunability.

A voltage-controlled current source active system is known as an OTA. It's a device that uses a differential input voltage to produce an output current. A voltage is normally provided as an additional input to regulate the amplifier's transconductance. OTAs are commonly used in the

absence of external feedback (although it is possible and allowed). We may think of the OTA feature as a more or less ideal transistor with finite transconductance [1] [2] [3].

Its primary application is in the implementation of electronically driven applications that are more challenging to incorporate with traditional op-amps, such as variable frequency oscillators and filters, as well as variable gain amplifier levels. OTA is a crucial active component of analog signal processing and signal production [1].

Operational Transconductance Amplifiers (OTA) are important components in a wide range of analog circuits and systems that have previously been introduced using OPAMPs. Recently, work on designing highly linear OTA circuits that consume less power and run at lower supply voltages has begun.

The higher frequency OTA can be used in a number of RF and microwave applications as a basic building element, whereas previous OTAs rarely worked over 200MHz [1]. This project's main goal is to analyze the performance of traditional OTA approaches and proposea topology based on improved process technology that can shatter the prior frequency barrier. Different OTA topologies have been studied and analyzed. It is recommended that you use a topology that strikes the perfect balance between complexity and its performance. The study examines and compares OTA topologies in terms of how technology scaling affects several performance characteristics such as transconductance, gain, bandwidth, supply voltage, powerconsumption, frequency range, and so on.

Figure 2.1 depicts the OTA symbol. The following formula is used to measure the current output Io:

$$Io=\pm g_m[(V_P)-(V_n)]$$

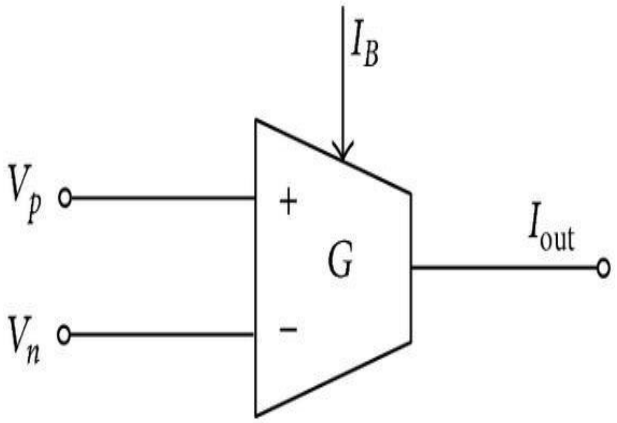

Fig 2.1:OTA symbol [1]

where gm denotes the transconductance gain. In the above Equation, the polarity of the current output is indicated by the sign "±".

Figure 2.2 depicts an OTA with MOS transistors.

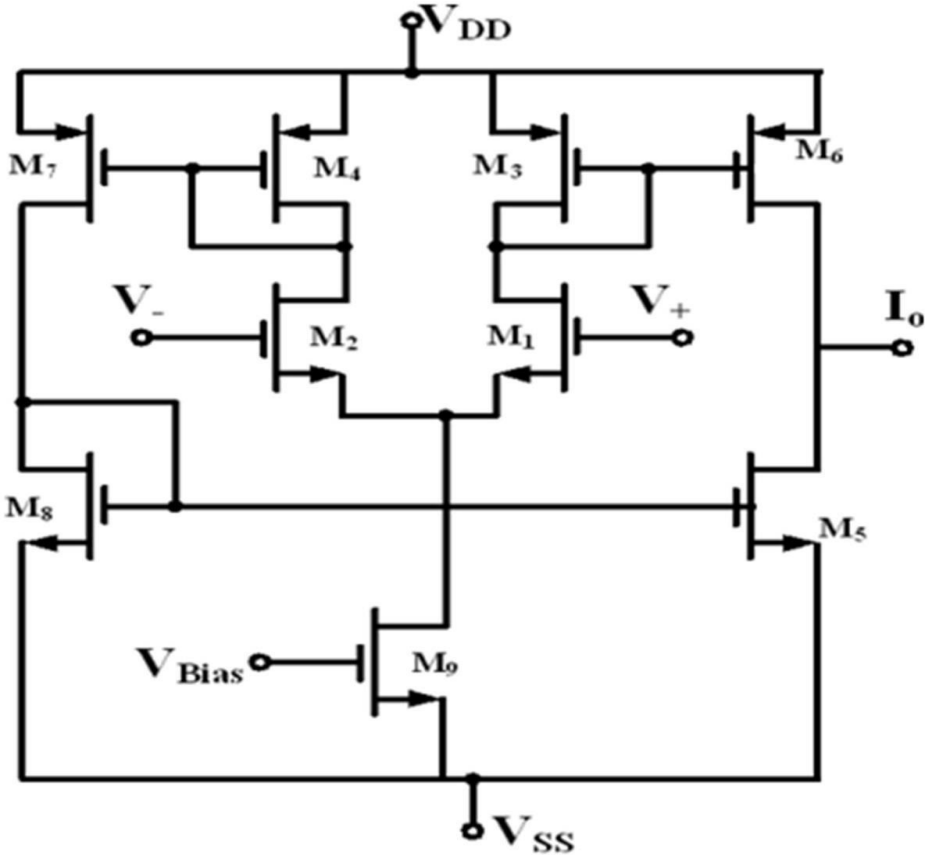

Fig 2.2: OTA with MOS transistor [1]

The transconductance gain is defined as:

$$g_m = \sqrt{\mu_n C_{ox} \frac{W}{L} I_b}$$

2.2 DIFFERENT STRUCTURES OF OTA

The operational transconductance amplifier (OTA) is a form of amplifier in which, All nodes are low impedance, with the exception of the input and output nodes [4]. Figure 2.3 shows a simple OTA example of a diff-amp with a current mirror load.

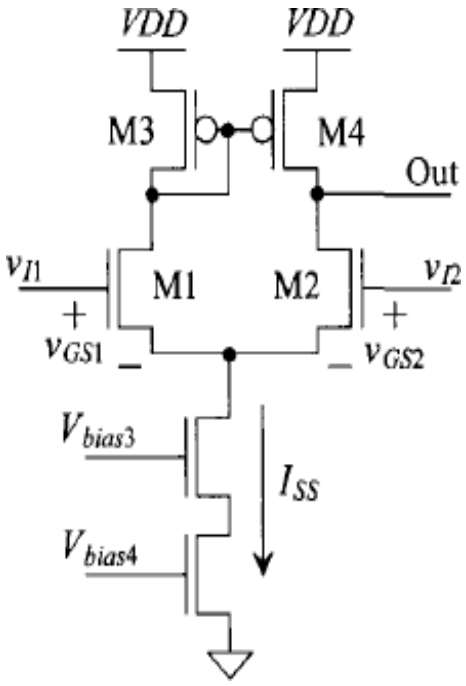

Fig: 2.3 Creating a diff-amp with a current mirror load [4]

Without the use of a buffer, an OTA can only drive capacitive loads. A resistive load will eliminate the OTA's gain (Unless the resistance is quite large). Figure 2.4 shows an example of an OTA.

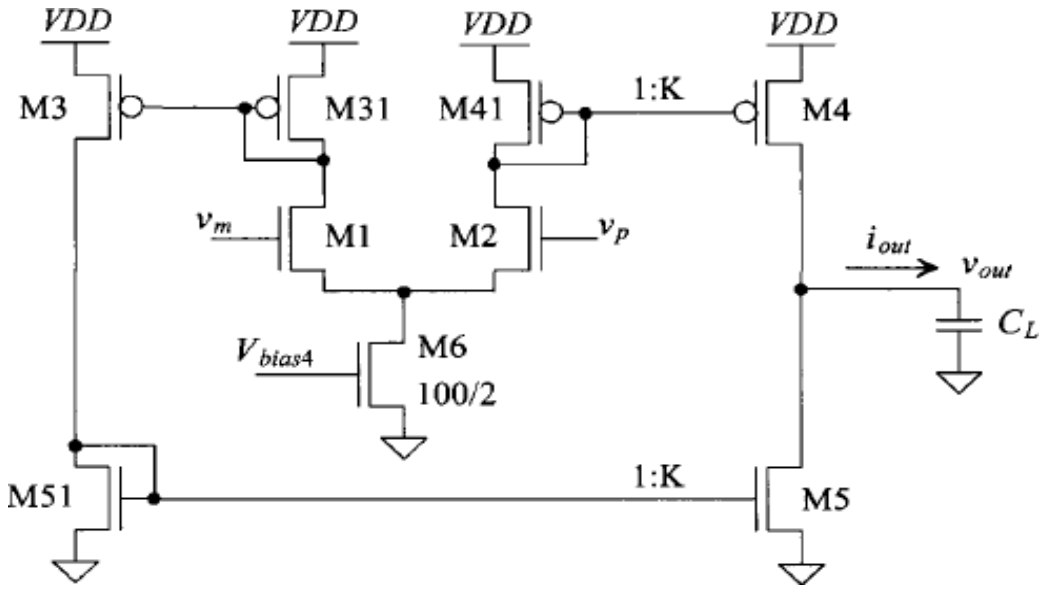

Fig 2.4: Example of an operational transconductance amplifier (OTA) [4]

The simple op-amp in Fig. 2.5 is not regarded as an OTA since M4's drain is a node with a high impedance, not the input or output of the amplifier.

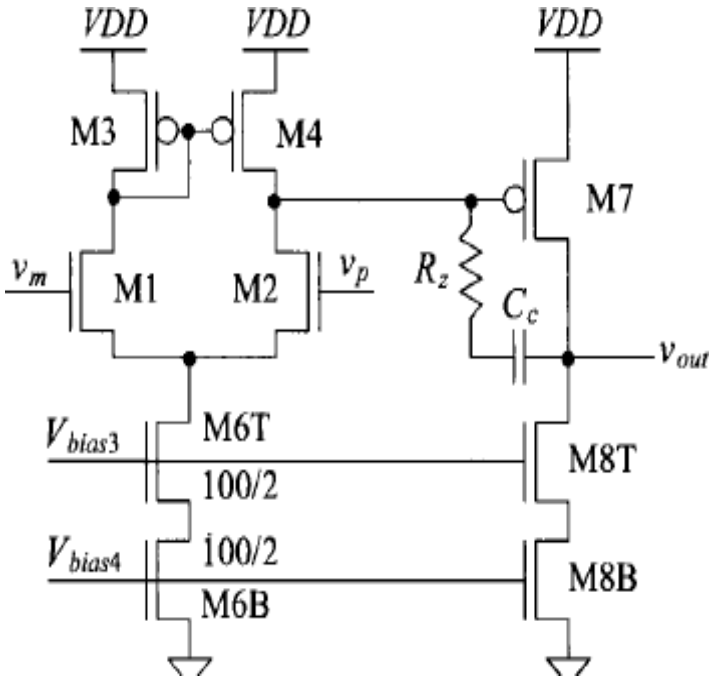

Fig 2.5: Basic two-stage op-amp [4]

Except for the input and output nodes, all nodes are coupled to a gate or drain or a source, as shown in Fig. 2.3. The M4 and M5 MOSFETs can be greater than the other MOSFETs in the circuit by k times(K > 1), as indicated by the "1: K" terminology [4].

It's important to keep in mind that the non-inverting input is the gate for OTA. While the derivation is fascinating, we are more interested in the transconductance of the OTA. If the impedance of the capacitor is low as compared to the OTA's output resistance, we can write it at higher frequencies [4].

A POINT TO REMEMBER

When the load capacitance is raised, the unity-gain bandwidth decreases, which makes the OTA more stable. Unlike two-stage op-amps, which can become unstable as the load capacitance increases, the OTA will be more stable as the load capacitance increases. In addition, the phase margin approaches 90 degrees as the load capacitance increases. The step reaction of the OTA is of the order of first form (just the same as in an RC circuit) [4]. The OTA works very well as an "operational amplifier (op-amp)" in a closed-loop configuration because the load in many on-chip applications is simply capacitive. (we'll refer to OTAs as op-amps). We obtain a (two-stage) op-amp like the ones we discussed earlier when we add a second stage to the basic OTA. Using the methods already presented, we may adjust the resulting structure (However, using these two-stage designs to drive a load capacitance that is too large can cause instability) [4].

2.2.1 : CASCODE OTA:

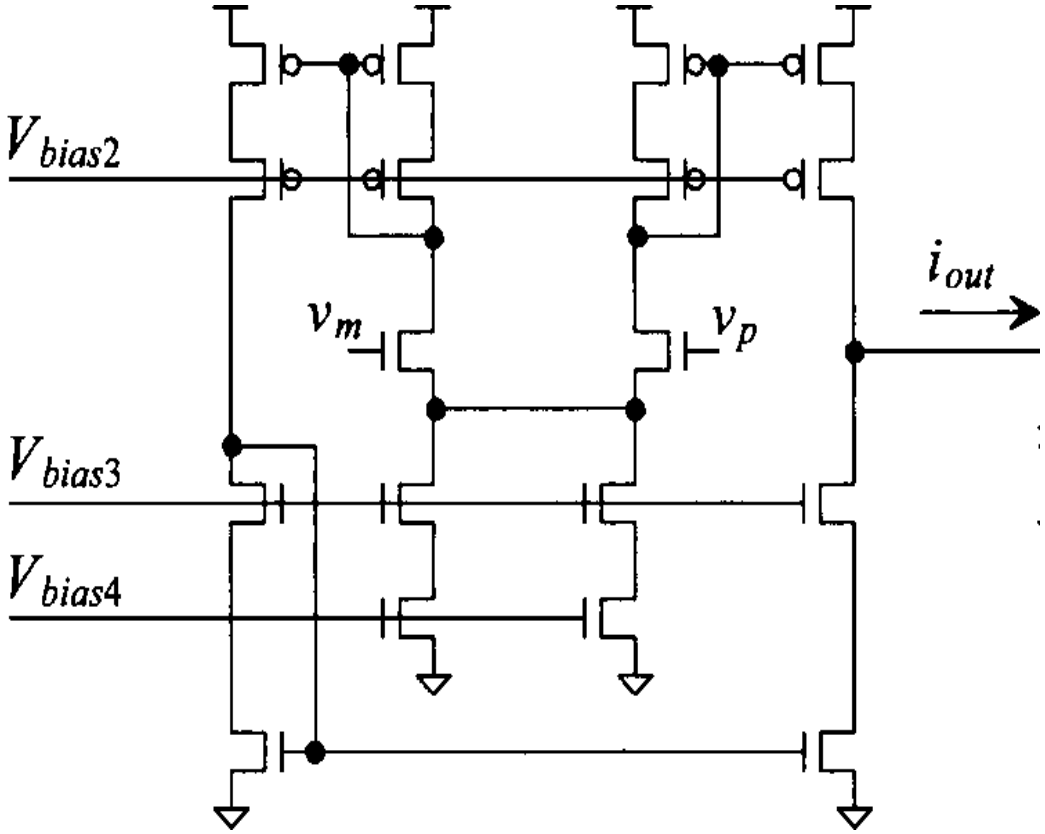

Fig 2.6 Basic structure of Cascode OTA [4]

In an ideal operational transconductance amplifier (OTA), the output resistance is infinite. None of the Iout flows in the OTA's own output resistance and all of it flows in the external capacitive load (which is *r04\r05* in the OTA of Fig. 2.3). In order to improve the OTA's output resistance, consider the configuration as seen in Fig. 2.4. The OTA is the foundation for this topology in Figure 2.3 except that now we have cascoded the circuit of current mirrors. Note how we have drawn the tail current source of the differential amplifier instead of two MOSFETs, four MOSFETs with twice the width (This is how we would set it up as well). The OTA now has a higher low-frequency gain [4].

2.2.2 FOLDED CASCODE OTA:

The following illustration depicts an NMOS differential amplifier-based folded cascode OTA. We have constructed the schematic in Figure 2.7 with MOSFETs which are parallel in the branches that supply or sink greater current to avoid identifying MOSFETs with twice the width (we can take an example as, the differential amplifier's tail current). All MOSFETs in Figure 2.7 maintain a steady flow of current [4] [5].

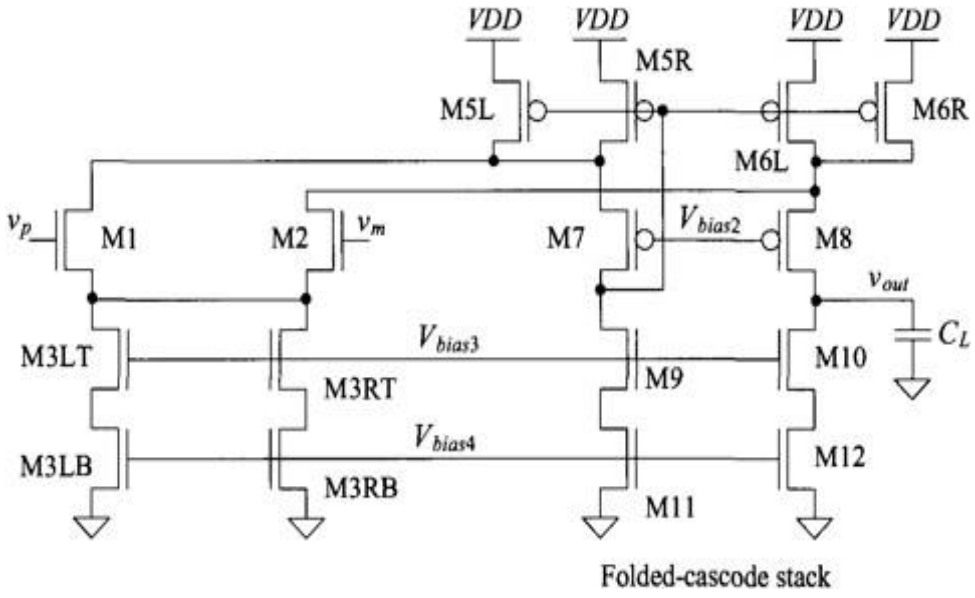

Fig 2.7 Folded Cascode OTA [4]

2.3 CMOS

The complementary metal-oxide-semiconductor (CMOS) fabrication process is a type of fabrication technique for MOSFET (metal-oxide-semiconductor field-effect transistor) that employs p-type and n-type MOSFETs in complementary and symmetrical pairs for its operations.

Integrated circuit chips (ICs), microprocessors, microcontrollers, memory chips, and other digital logic circuits are all built using CMOS technology. CMOS technology is also employed in analog applications, in addition to digital ones. Instead of signal relays, transmission gates can be utilized as analog multiplexers.

In mixed-signal (analog+digital) applications, the technology of CMOS is also frequently employed for RF

circuits up to microwave frequencies. For various types of communication, Image sensors (CMOS sensors), converters of data, RF circuits (RF CMOS), and highly integrated transceivers are all examples of analog circuits that use CMOS technology.

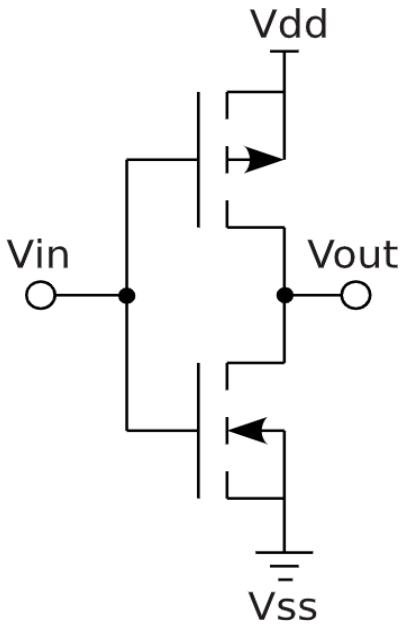

Fig 2.8: Basic CMOS circuit [2]

CMOS electronics have two important characteristics: high noise immunity and low static power consumption.

2.4 FinFET:

It took a quarter-century for the multi-gate transistor to go from research to manufacture a 22nm technology node microprocessor in 2012. Due to their vastly enhanced electrostatics,

FinFETs outperform incumbent planar devices. Most electronic design automation (EDA) tools must be updated for FinFET designs in the FinFET design environment. This process is nearly complete, and tools from important vendors are now available (Synopsis, Mentor Graphic, and Cadence) [9].

Foundries that make the best semiconductors are capable of offering their customers with full EDA support. FinFET Technology is now available on the market. This device has been adapted with high-performance logic and will be used for several generations to come. This decade will likely see the introduction of new fin materials into products. FinFET has brought significant improvements to the realm of circuit design, and the design environment is fast maturing as tools are updated [9] [10].

2.4.1 Brief history of FinFET

About a quarter-century ago, in the late 1980s, the most significant era of multi-gate MOSFET discoveries occurred. In 1987 probably invented the first multi-gate transistor.

The authors discovered that by reducing the body bias effect, the entire body which is depleted because of this narrow tri-gate bulk based on Silicon transistor aids enhance switching [3]. Two years later, researchers showed the DELTA, the first double gate transistor in bulk silicon, which was a precursor to the FinFET. A decade later, the first FinFET on SOI substrate was published.

SOI also allowed for the creation of a horizontal gate-all-around (GAA) transistor, paving the way for silicon-based nanowire devices. When two or more than two nanowires is stacked on top of each other, the driving current capability of a transistor is improved for a given footprint size [10] [13].

The FinFET transistor was invented by Chenming Hu and colleagues of him at the University of California in Berkeley in an attempt to solve the worst effect called as SCE (Short Channel

Effect). FinFET was created with Silicon-On-Insulator in mind (SOI). Intel is the first company to use FinFET in 2011 production, describing it as the most significant advancement in semiconductor technology in more than 50 years.

By 2015, FinFET processors were used in all of the top servers, computers, Android, and iOS phones. A non-planar, double, triple, or multi-gate transistor is referred to as a "FinFET" & based on the single gate transistor design, it is designed either on an SOI substrate or on a silicon wafer. A thin Si "fin" surrounds the conducting channel which forms the device's body, which is an essential feature of FinFET. The effective channel length of the unit is determined by thickness.FinFET is divided into two types-SOI FinFET & Bulk FinFET. FinFETs are nothing more than the "Base" on which they are built [10].

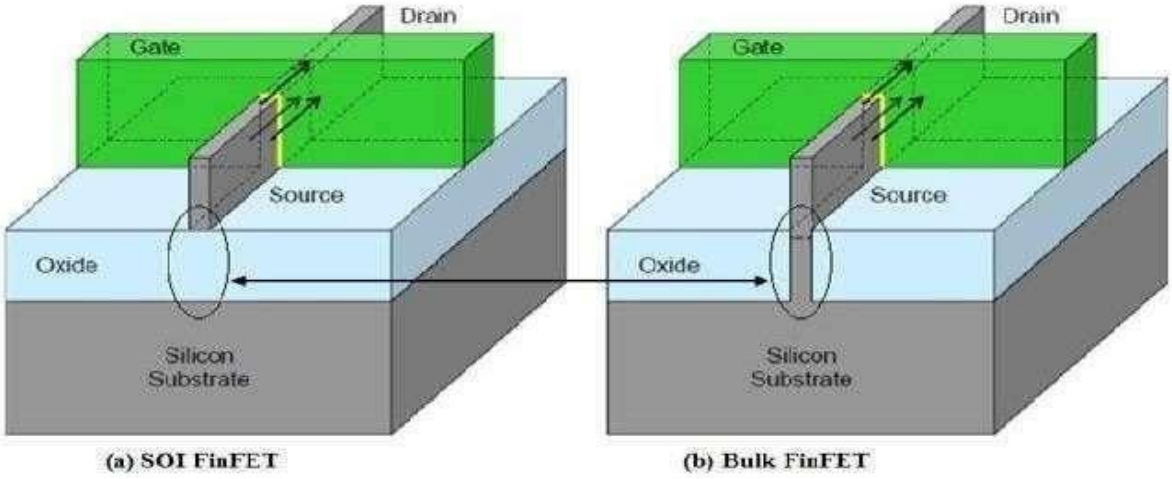

Fig 2.9: SOI FinFET and Bulk FinFET [10]

SOI FinFETs with thin oxide on the sides of the fin is known as

a) Double-Gate FinFETs,

while those with thin oxide on the top and sides of the fin are known as

b) Triple-Gate FinFETs, as shown in fig.2.10 :

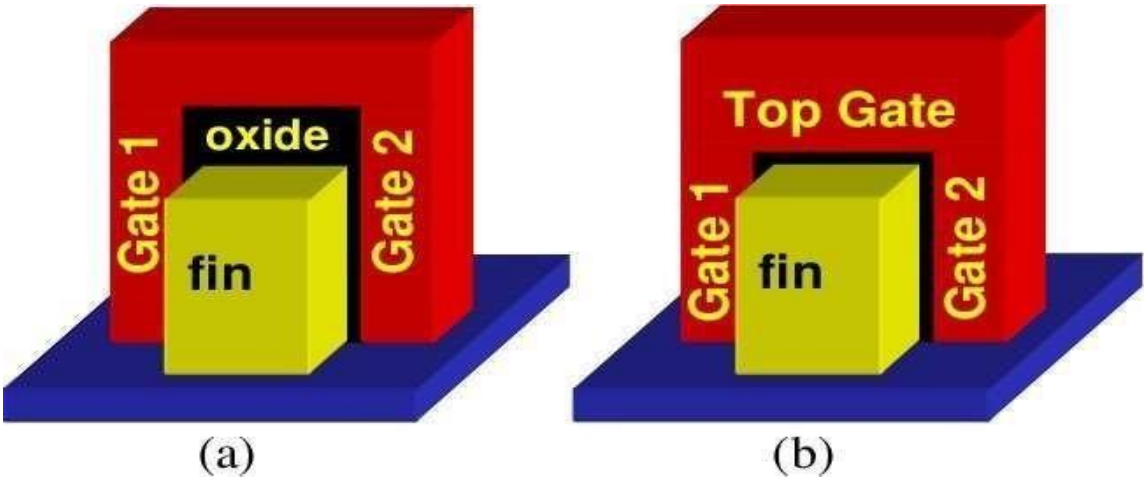

Fig.2.10. Double-Gate & Triple Gate FinFET [11]

A FinFet works in the same way as a traditional MOSFET. When the circuits are idle, the second gate can be used to regulate the device's threshold voltage, allowing for easy switching on one side and lower leakage currents. Finally, for simpler logic gates, separate access to both gates may be used [11].

2.4.2 : Why do we need FinFET today?

Nowadays we can see the new technologies like latest mobile phone have so many features & these features requires lots of transistors, we can say millions or billions of transistors and to adjust a large number of transistors on a single chip requires scaling of transistors & when we scale down the size of the transistor then it reduces the distance between source & drain due to which short channel effect occurs so to overcome this problem we use FinFET**.**

Since the invention of MOSFETs, the device's channel length has been steadily decreasing in order to manufacture small and fastest devices. The following factors related to MOSFET underline the need for the smaller, much compact devices and explain why the MOSFET is not an appropriate solution. The length is the shorter section of the gate electrode, while the

width is the longer section. Short-channel effects rise when the channel length of a MOSFET decreases [14].

Two physical phenomena are thought to be responsible for the short-channel effects:

a. The channel's electron drift characteristics have been limited.

b. The shrinking of the channel length causes a change in the threshold voltage.

There are five different types of short-channel effects:

A.Drain-induced barrier lowering

Due to the depletion region which is surrounding the drain, and extends to the source, the two depletion layers mix. Punch through develops as a result of this. Thin oxides layer, higher substrate doping, shallow junctions, and wider channels can all aid to limit punch-through.

B..Surface scattering

Due to the depletion region which is surrounding the drain, which is extended to the source, the two depletion layers mix. Punch through develops as a result of this. Thin oxides layer, higher doping of substrate, junctions which are shallower, and wider channels can all aid to limit punch through. The longitudinal electric field component grows as the channel length decreases, and the surface mobility becomes dependent on the field. In a MOSFET, carrier transport is restricted to the inversion layer which is narrow. The mobility is reduced due to surface scattering. It's tough for electrons to migrate parallel to the contact. This is required so that the average mobility of the surface is approximately half of that of bulk mobility.

The collisions that electrons experience as they accelerate toward the interface are known as surface scattering.

C. Velocity saturation

In saturation mode, velocity saturation lowers transconductance. Carrier velocity goes to its maximum value when a stronger electric field is applied, which is known as saturation velocity. The transistor's state is known as velocity saturation when this happens. A high scattering rate of extremely energizing electrons, mostly owing to optical photon emission, causes velocity saturation. This effect lengthens the time it takes for carriers to pass across the channel.

D. Impact ionization

This is mainly caused by high electron velocity in the presence of larger longitudinal fields, which can form electron-hole pairs by impact ionization. The Impact ionization happens when an object collides with silicon, causing electron-hole pairs to ionize. It normally works like this: the drain attracts the majority of the electrons, while holes will enter into the substrate and will become part of the substrate current. The area in between the drain and the sourcecan also function as the NPN transistor's base. The source acts as an emitter, while the drain acts as a collector. The usually reversed-biased substrate-source P-N junction will conduct if, with the help of the source, holes are collected, and the accompanying current in the hole results in a voltage drop in the substrate material on the order of 6V. Then, similarly to the injection of electrons from the emitter to the base, electrons can be injected from the source to the substrate. As they go towards the drain, they can gather enough energy to form new eh pairs. If some electrons generated by high fields leave the drain field and penetrate into the substrate, the situation can deteriorate, causing problems for other devices on the chip.

E. Hot electron effect

trapped in certain parts of a device, causing unfavorable device behavior and deterioration, resulting in hot carrier Effects. The electric field of the channel grows as the size of the devices is reduced. As a result, the high field zone at the drain terminal takes up a significant amount of channel length. This causes the hot-electron effect, which causes the device parameters degradation with time. This effect always creates problems during the scaling down of the device.

MOORE'S LAW In 1965, Gordon Moore drew a diagram showing his prognosis for the development of the speed of silicon technology. Moore's Law still holds true decades later. Gordon Moore is one of Intel's co-founders. Since the advent of the integrated circuit (IC), the number of transistors per square inch on an IC has doubled every year. In the semiconductor sector, this law is critical for setting targets and planning for the long term. Moore's law is a projection or observation rather than an actual law. It refers to the force that propels technological, economic, social, and technological progress.

2.4.3 Working & Principle of FinFET:

A FinFET operates similarly to a conventional MOSFET. Both p-channel and n-channel Both p channel and n channel MOSFETs can function in two modes: enhancement and depletion mode. When there is no voltage on the gate terminal, the channel has the most conductivity. The channel's conductivity decreases when the voltage shifts from positive to negative.

When a MOSFET in enhancement mode has no voltage applied to the gate, due to which it will not conduct. In contrast to depletion mode, the device conducts better in enhancement mode when the gate terminal voltage is higher.

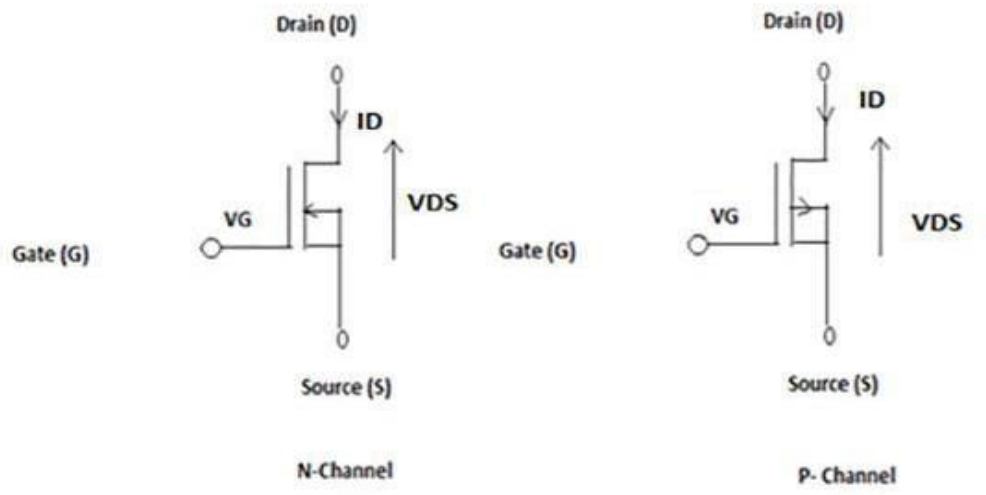

Fig 2.11:Showing FinFET's working principle based on MOORE'S Law [19]

The MOSFET's primary function is to regulate the voltage and current flowing between terminals of source and drain. The gate terminal creates a capacitor of very high quality. The gate is made of the silicon oxide layer, p-body silicon, gate metallization, and p-body silicon. The most important component is the capacitor. The surface of the semiconductor beneath the layer of oxide, between the terminals of source and drain. By giving a positive or negative gate voltage, inversion from p-type to n-type will take place. A depletion region is generated when a small amount of voltage is given to this structure (the capacitor) while keeping the terminal of the gate positive with respect to the source. The contact between the silicon and the SiO2 forms this depletion zone.

The source terminal, drain terminal, and n+ source all attract electrons when a positive voltage is supplied. The electron reach channel is formed as a result of this. Current will flow between the source and drain terminals if the voltage is applied between the source and drain terminals. The gate voltage regulates the concentration of electrons (Vg) [20]. A hole channel will form under the oxide layer when a negative voltage is applied. The conduction of current between the source and the drain is now controlled by the source to gate voltage. Only when the gate voltage passes a certain threshold does conduction

Commence [19] [20].

2.4.4 Construction of FinFET

The two varieties of FinFets are constructed differently. A standard MOSFET's basic layout and method of operation are comparable to this one. The fin, a three-dimensional bar atop the silicon substrate, is the only distinction.

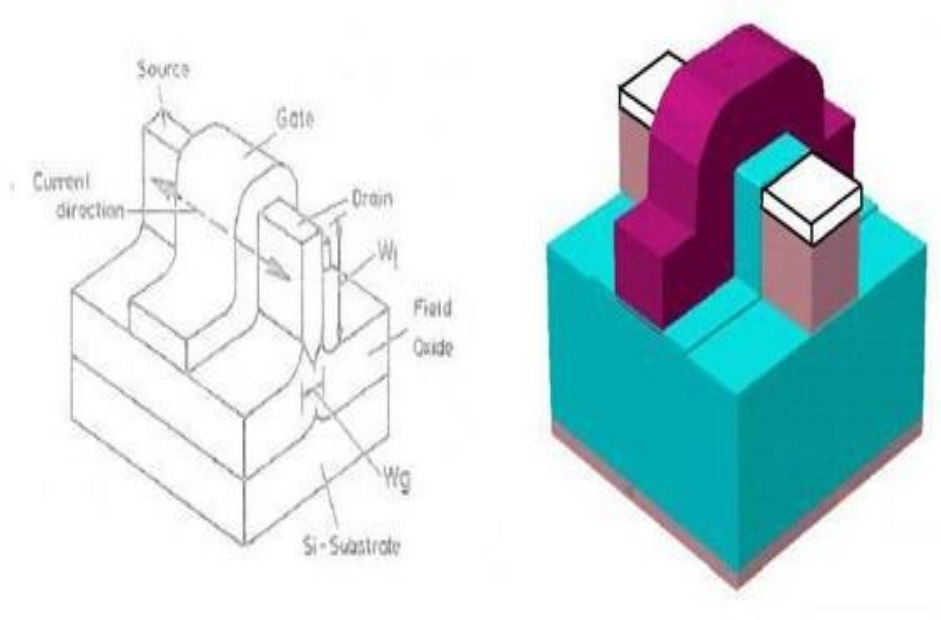

Fig 2.12: Construction of silicon Based bulk FinFET [19]

2.4.5 Construction of silicon Based bulk FinFET

FinFets are made of silicon. The channel which is conducting is wrapped by a thin Si fin, which is one of FinFet's most notable features. The device's body is made up of this. The fins are a three-dimensional canal that connects the terminal of the source and drain. They're constructed on a silicon substrate. The channel is wrapped around the gate terminal. This enables the creation of many gate electrodes, which reduces leakage current while increasing drive current.

A. Substrate: A weakly p-doped substrate with a hard mask on top serves as the foundation of a FinFET. A patterned resist layer is included as well.

B. Fin etches: A highly anisotropic etching procedure is used to create the fins. Due to the lack of a stop layer, the process of etching must be based upon time. The SOI models have this layer.

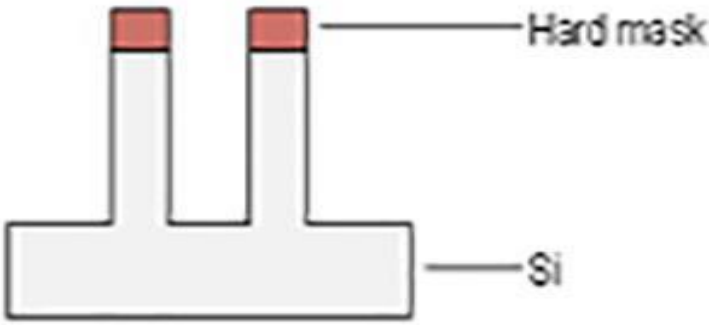

Fig 2.13:Showing the Deposition of n+ doped Poly Silicon Layer

C. Oxide deposition: To separate the fins from one another, deposition of oxide with an aspect ratio of high filling behavior is required.

D. Planarization: Chemical mechanical polishing is used to planarize the oxide. The hard mask serves as a stop layer in this case.

E. Recess etch: This procedure is required in order to recess the oxide coating and create lateral fin isolation.

F. Gate oxide: To isolate the gate electrode and the channel, the gate oxide is formed on the uppermost i.e. top of the fins using thermal oxidation. Because of this reason, fins are connected beneath the oxide, a high-dose angled implant at the fin's base generates a dopant junction, which completes the isolation.

G. Gate Deposition: On the very top of the fins, a heavily doped polysilicon layer is next placed. As a result, around the channel three gates are wrapped: one on either side of the fin,

and one above. The gate oxide thickness on top of the third number gate determines how it is wrapped.

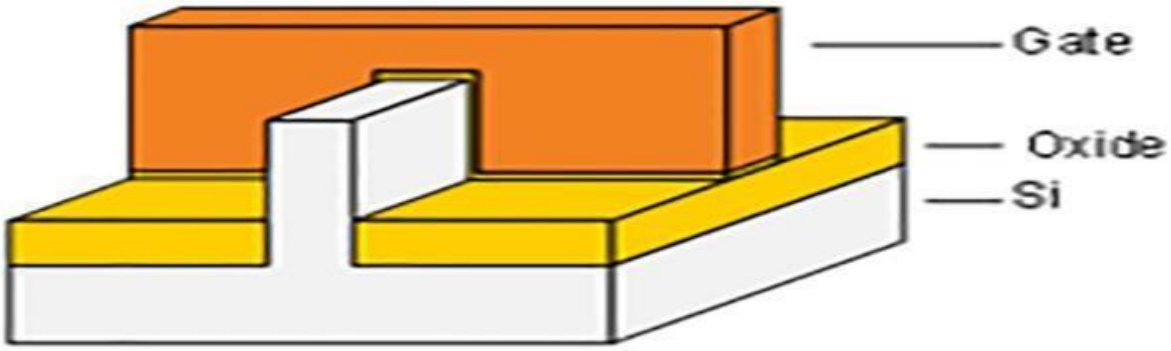

Fig 2.14: 2-D View of Layers of FinFET [19]

The top gate's influence can likewise be reduced by depositing a layer of nitride on the top of the channel. The channels on an SOI wafer are already segregated from each other because of the presence of a layer of oxide. The etching of the fins is also simplified as a result of this. Because of reason that the process may be stopped on the oxide, this is done.

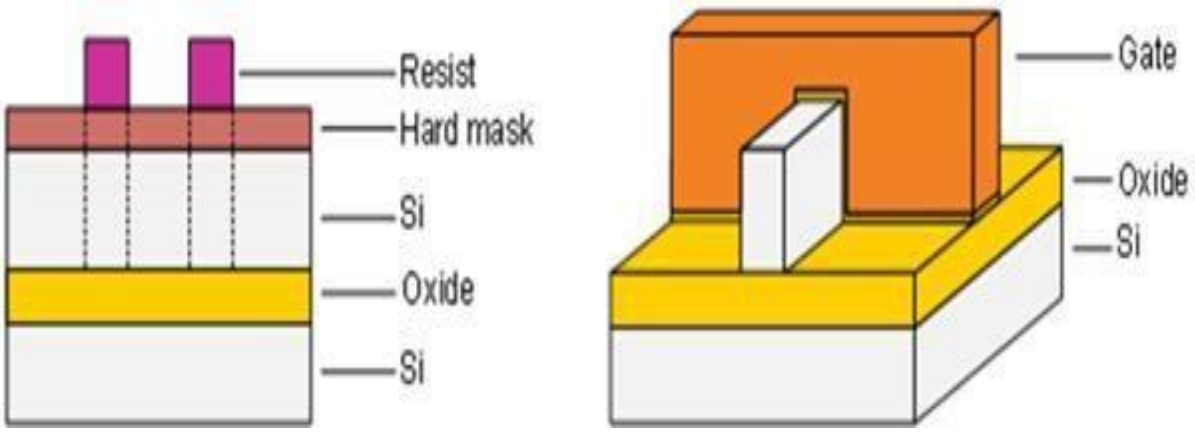

Fig 2.15: 3-D structure FinFET [19]

2.4.6 Advantages of FinFET:

- Short channel effect (SCE) is reduced.
- The driving current is improved.
- The device is more compact.
- The cost is low.

2.4.7 Disadvantages of FinFET:

- The mobility of electrons is reduced.
- Resistances of source and drain are higher.
- Reliability issues.

CHAPTER-3

COMPARATIVE ANALYSIS OF OTA USING CMOS & FINFET

3.1 CMOS based OTA:

The OTA with MOSFET transistors is shown in Figure 3.1

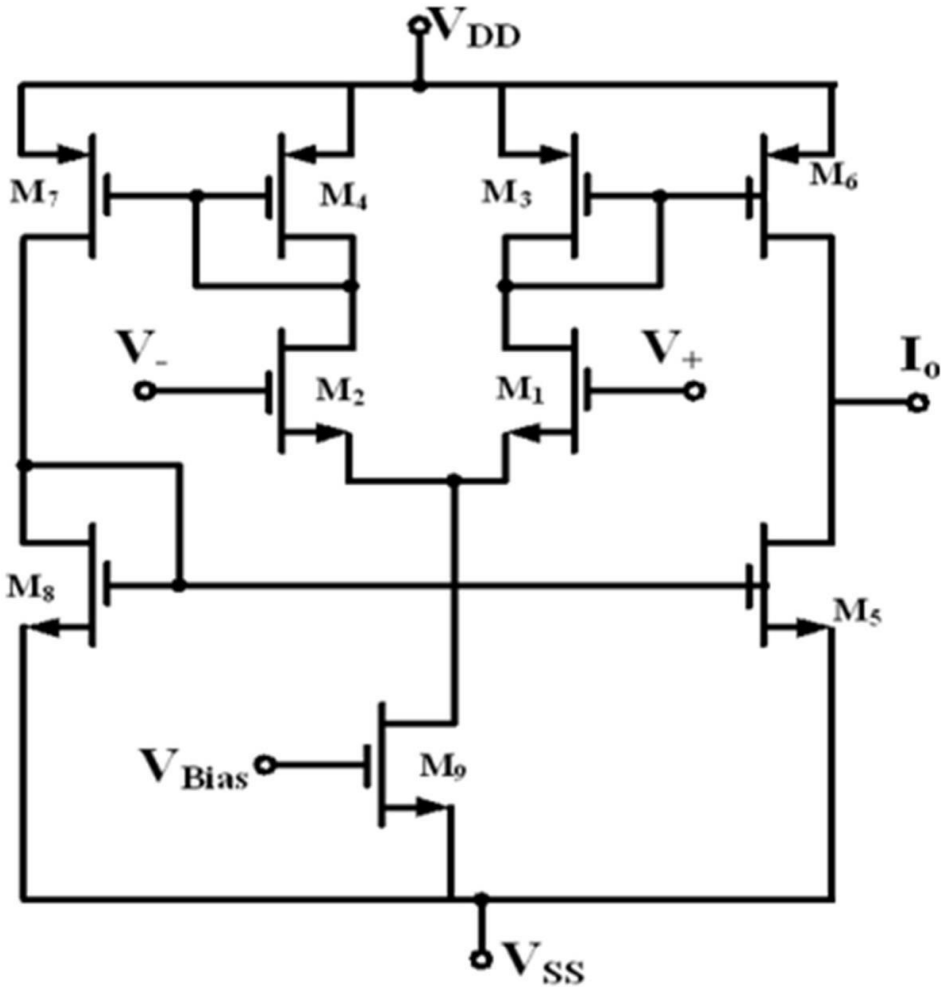

Fig 3.1:OTA based on CMOS[1].

Four types of aspect ratios are used in this combination [1]. The aspect ratios of all ten MOSFETS are given in Table 3.1.

Table 3.1. Aspect Ratios of N-MOSFET and P-MOSFET of Figure 3.1

MOSFET Transistors	Aspect Ratio(W/L)
M1 & M2	3.6/0.36
M3,M4,M5& M8	1.44/0.36
M6 & M7	2.88/.36
M9	5.4/0.36

The width (W) and length (L) specified for MOSFET technology mean the minimum length bandwidth of the gate of MOSFET. The W/L ratio is determined by the multiplicity factor m, as well as transconductance and current capability. Varying the W/L ratio directly changes the transconductance of the circuit. Thus it is very important to specify the W/L ratio of the MOSFET if it is used in the circuit.MOSFETS' small size, ease of fabrication, and low power dissipation allow for extremely high levels of logic and memory circuit integration.

3.2 SCHEMATIC OF CMOS BASED OTA

We make a schematic diagram of CMOS-based OTA using 180nm technology in the cadence virtuoso. The Schematic is made with the help of basic elements required for the circuit i.e., for making schematic of OTA PMOS and NMOS are arranged in the connection as shown in the figure. The schematic of OTA in cadence virtuoso can be made as shown below:

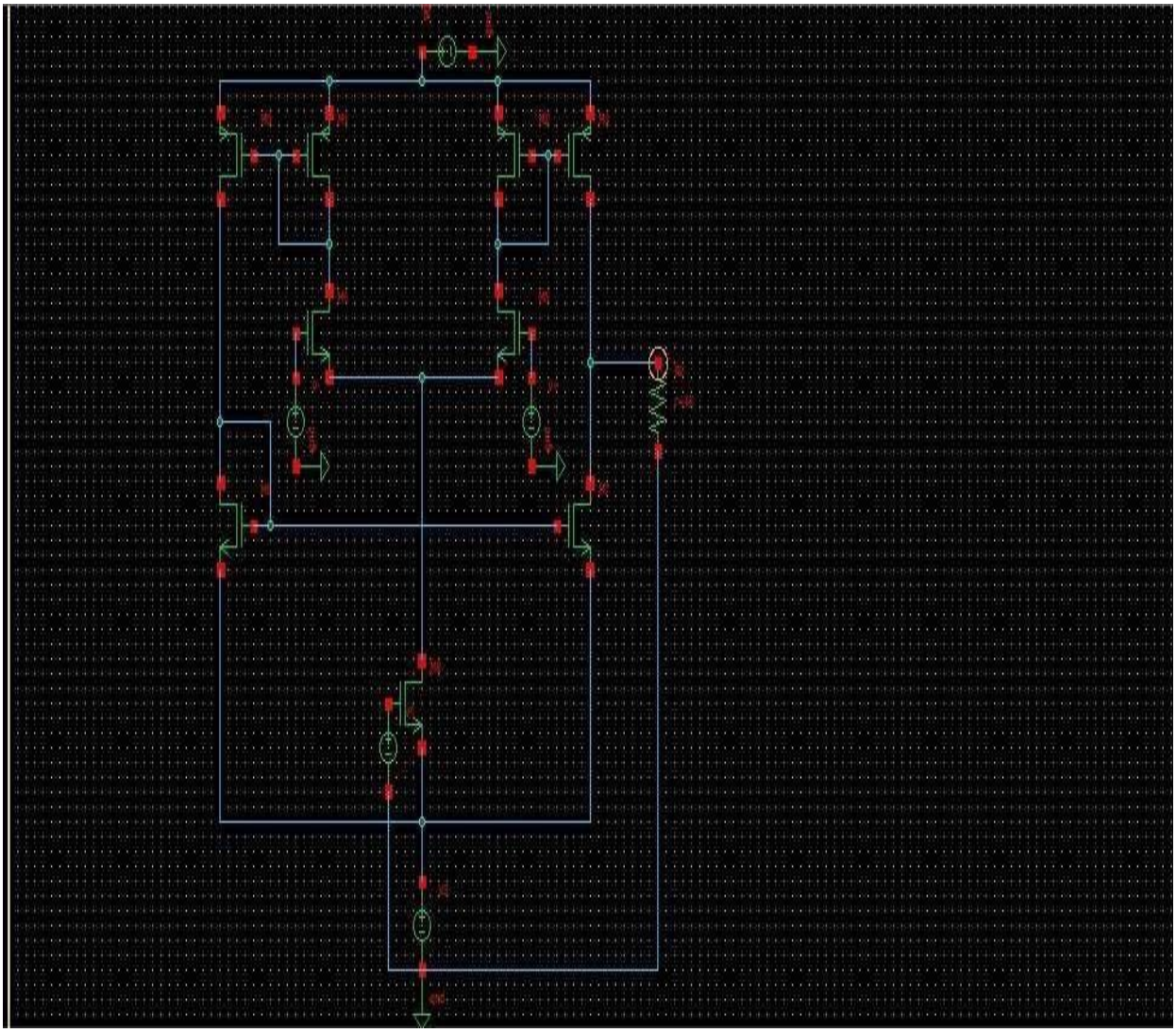

Fig.3.2.Schematic Diagram of CMOS based OTA

3.3 FINFET BASED OTA

We make a schematic diagram of FinFET based OTA in the cadence virtuoso. The Schematic is made with the help of basic elements required for the circuit i.e., for making a schematic of FinFET based OTA we used 18nm length of FinFET.The schematic of OTA in cadence can be made as shown below:

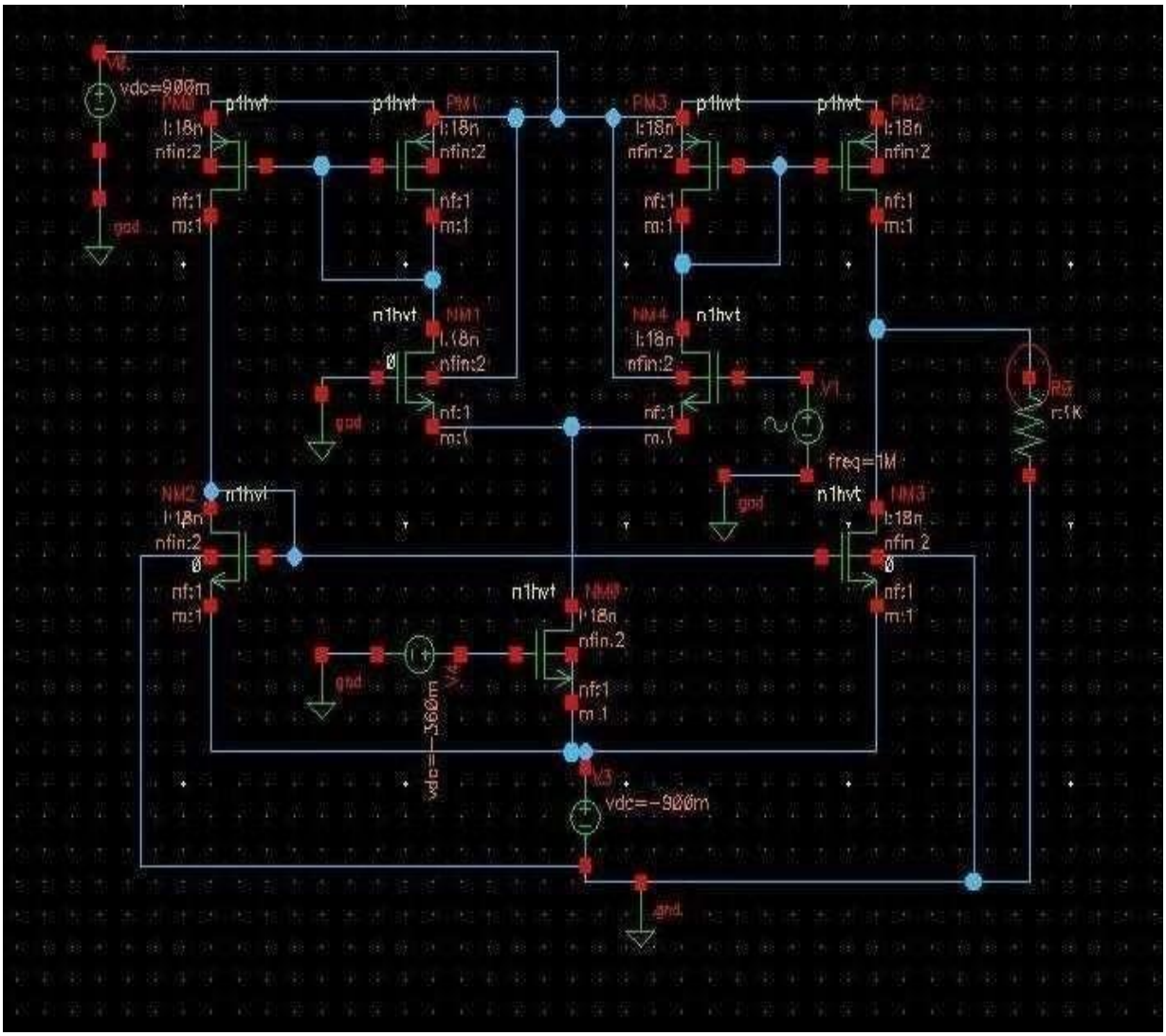

Fig.3.3.Schematic of FINFET based OTA

3.4 SIMULATION RESULTS:

There is three analysis to characterize the OTA and they are DC analysis, AC analysis & Transient analysis.

3.4.1 :DC analysis

To characterize the OTA in terms of linearity we have done a dc analysis. For this analysis, we have swept input voltage (V+) from -1V to 1V.

The biasing voltage of -360 mV is applied at the gate terminal of M9. The DC power supply used was ± 0.9V. The dc response has been plotted between the input voltage and output current.

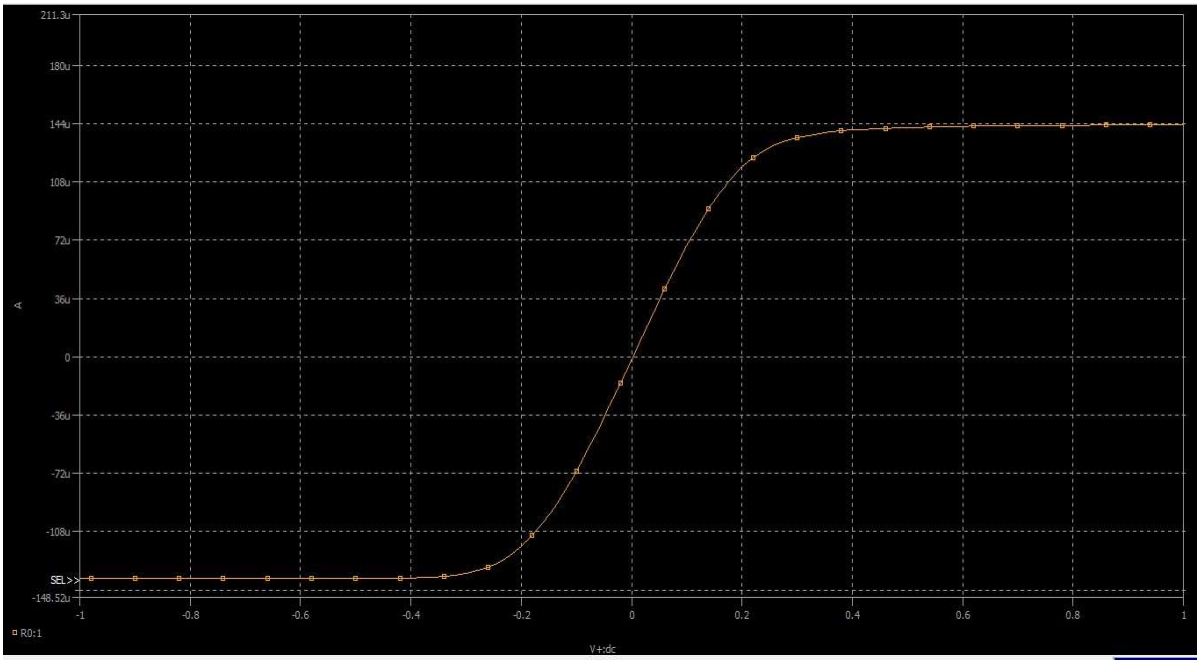

Fig.3.4. DC Response of CMOS based OTA

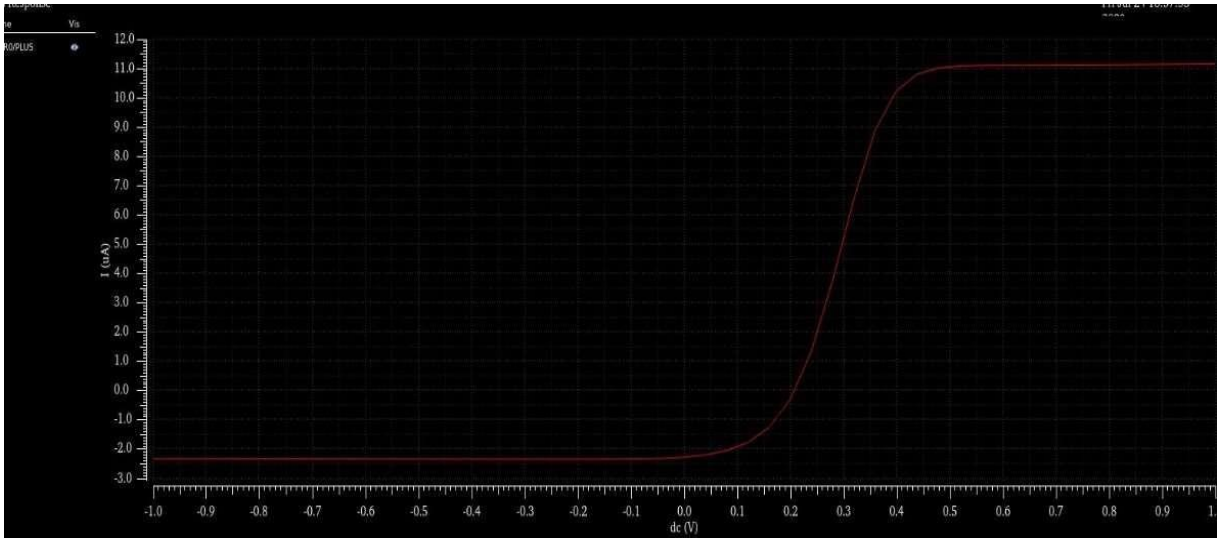

Fig.3.5.DC Response of FINFET based OTA

Table 3.2.Input voltage & output current range

	CMOS based OTA	**FINFET based OTA**
Input common mode range (voltage)	-0.2v to +0.2v	0.15v to 0.45v
Output Current	-108 µA to +108 µA	-0.2 µA to +11 µA

3.4.2 :AC analysis

The AC analysis enables us to determine what happens to our circuit when AC signals are applied to its input. It helps us to measure the bandwidth & transconductance gm. We have obtained the frequency response of the circuit in ac analysis. We have given 50 mV as the input voltage at (V+) varying the frequency range from 1 kHz to 10 GHz on the x-axis and keeping the y-axis as a varying range of transconductance $gm=Iout/Vin$. The DC power supply used was ± 0.9V.

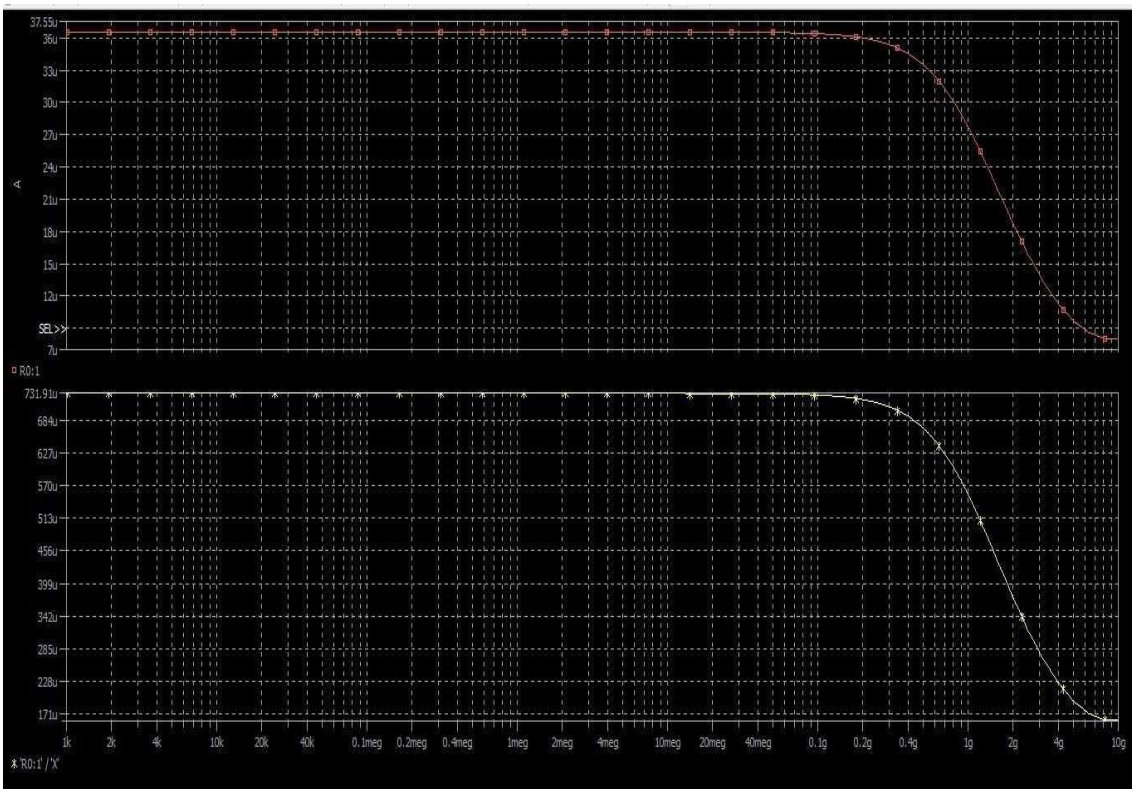

Fig.3.6.AC Response of CMOS based OTA (current & voltage w.r.t frequency)

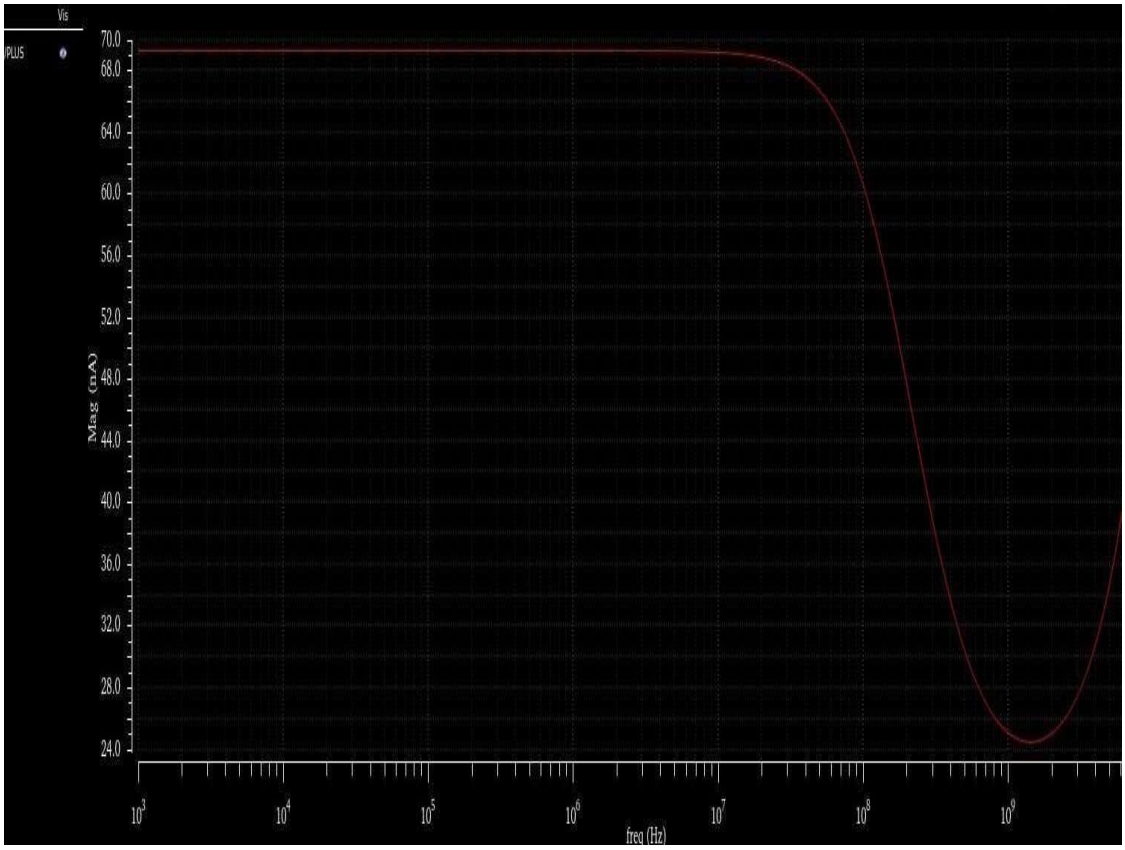

Fig.3.7.AC Response of FINFET based OTA (current w.r.t frequency)

Table.3.3.Input voltage,Output current & Transconductance

	CMOS based OTA	**FINFET based OTA**
Iout	36 µ A	69 µ A
Vin	50Mv	50 mV
Gm	0.72 mA/V	1.38 mA/V

3.4.3 :Transient analysis

The time-domain waveforms generated by the transient analysis are plots of voltage or current versus time. It calculates the circuit's response over a period of time. For transient analysis of the above OTA circuit, we have given the sinusoidal signal of 10 kHz frequency and 50 mV of amplitude for the time span of 2ms. We have kept output and input as Y-axis and time as X-axis. The transient response obtained is in-between

time vs current or voltage graph for 2ms.

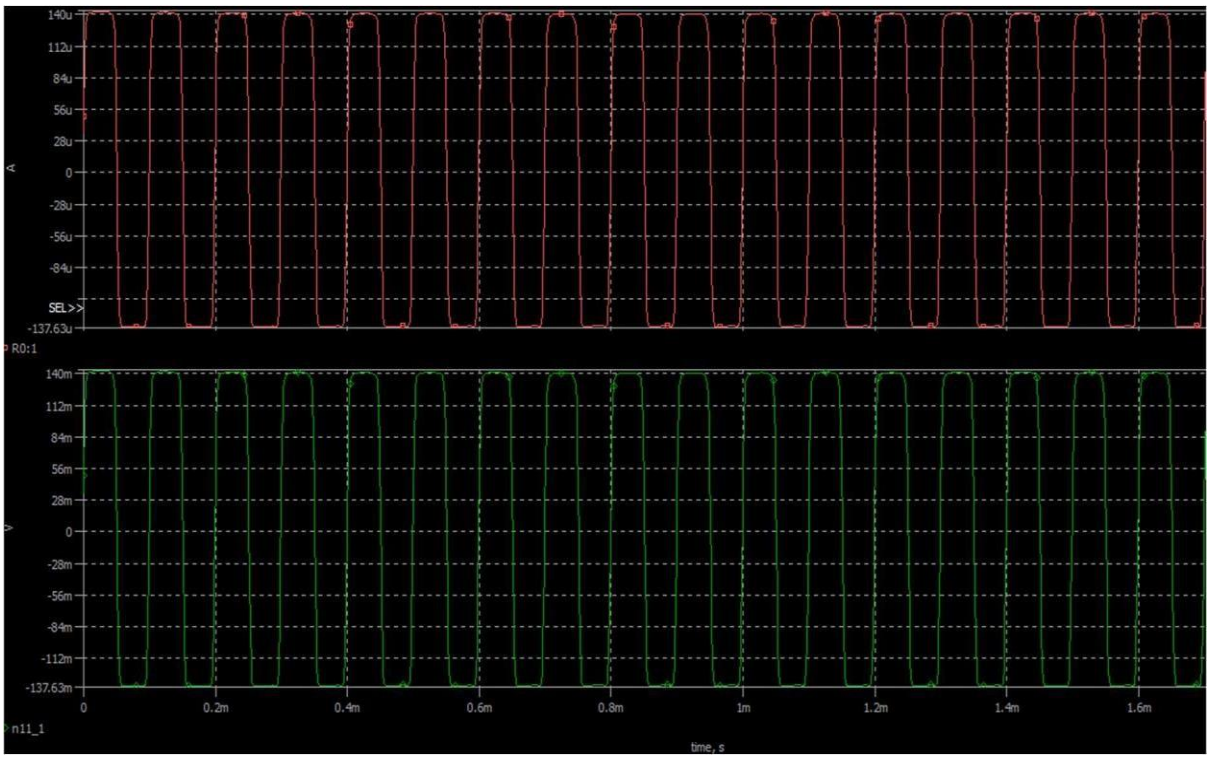

Fig.3.8.Transient analysis of CMOS based OTA(current & voltage w.r.t time)

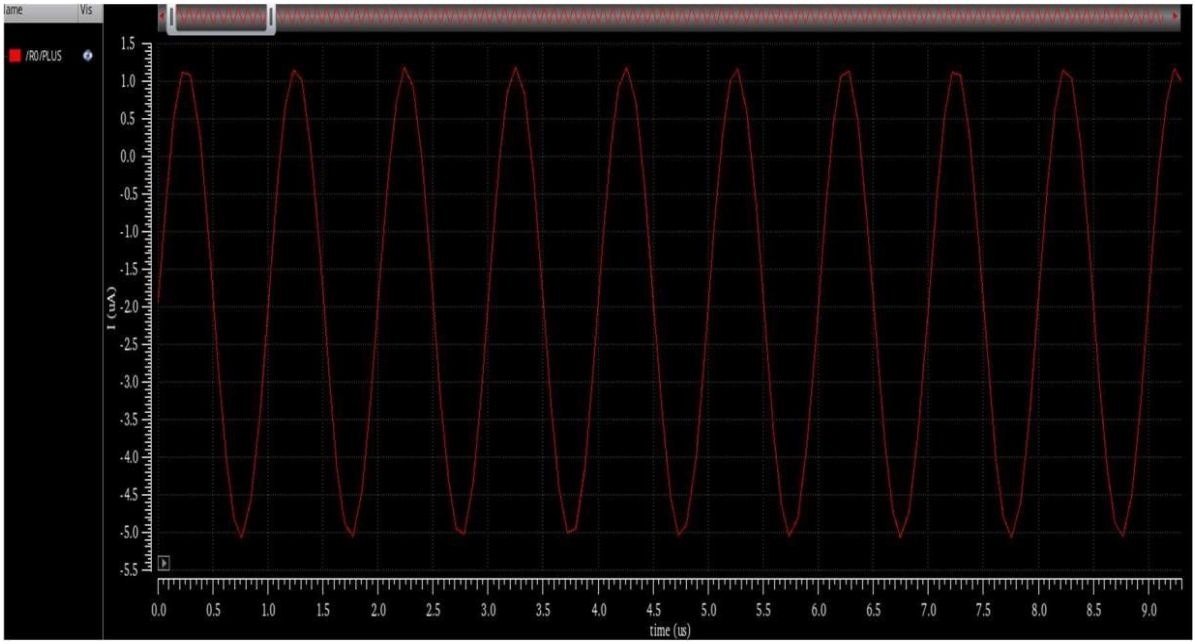

Fig.3.9.Transient analysis of FINFET based OTA (current w.r.t. time)

CHAPTER-4

COMPARATIVE ANALYSIS OF DIFFERENT TOPOLOGIES OF OTA

4.1 TWO-STAGE OTA:

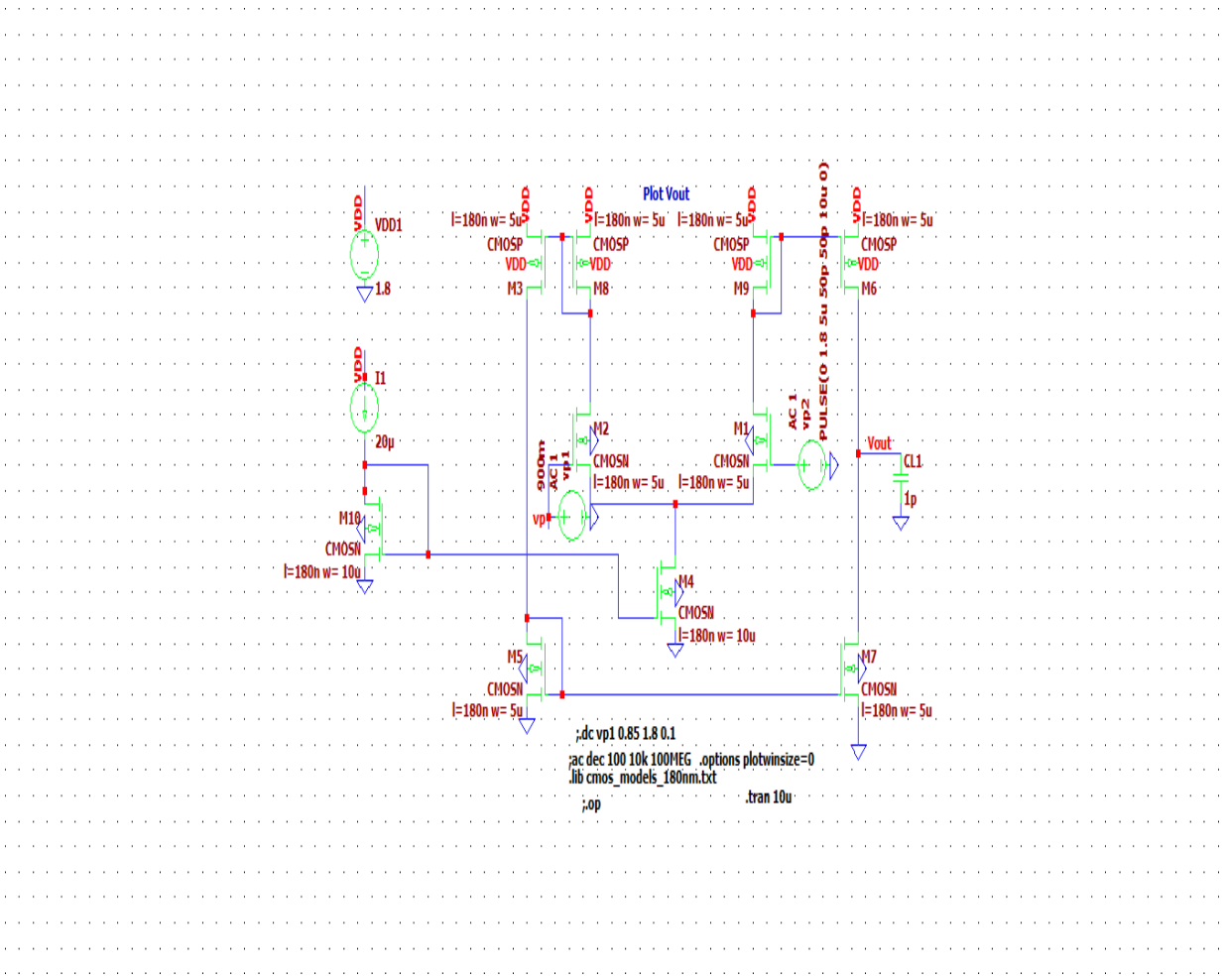

Fig 4.1:Schematic of two-stage OTA

4.1.1 Frequency Response:

The circuit is implemented on 180nm technology in a spice simulator. For frequency response inputs are given with AC 1 and with command .ac dec 100 10k 100MEG. From frequency, we calculate Unity gain frequency and Phase Margin.

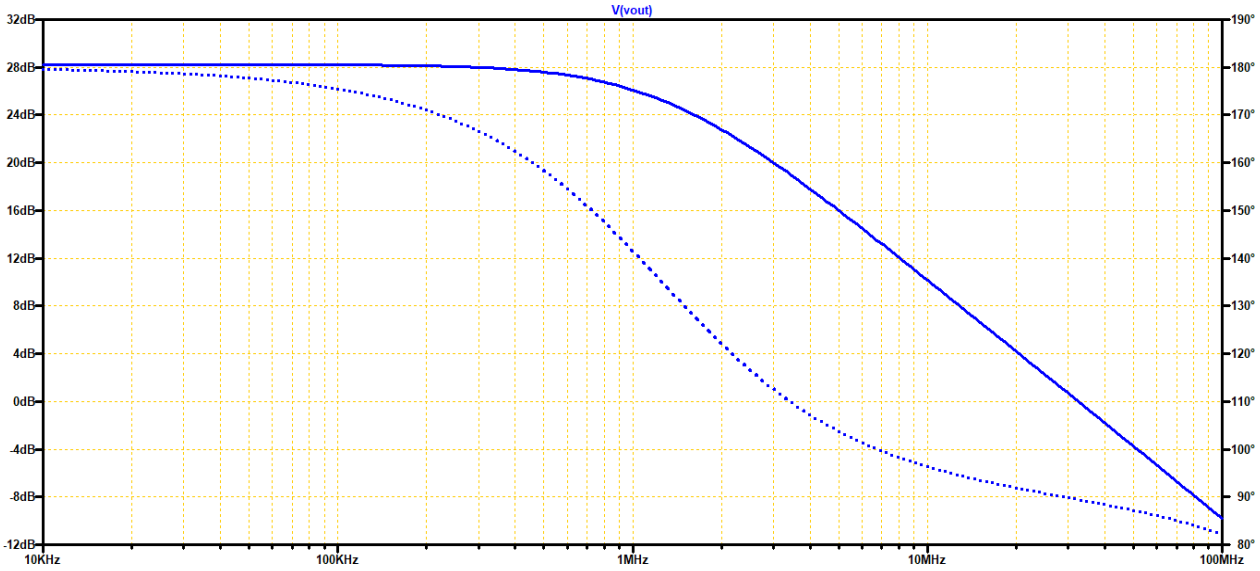

Fig 4.2 Gain and Phase plot of two-stage OTA

Gain=28dB

Unity gain frequency(frequency at 0dB)=32.70 MHz

4.1.2 DC ANALYSIS:

DC Characteristics are obtained by sweeping the DC input from 0.1V to 1.8V Where all transistors of the two-stage op-amp are in saturation. DC analysis is done with the command:

dc vp1 0.85 1.8 0.1

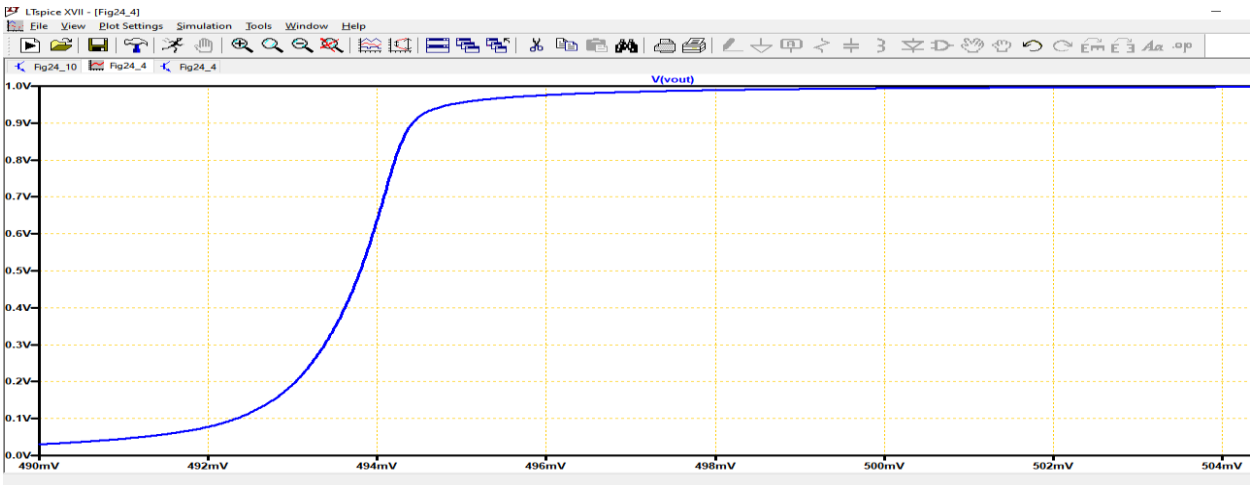

Fig 4.3: Vout versus Vin plot

4.1.3 Transient Analysis:

The step response is given to the input 0 to 1.8v and the output response is plotted with the command: .Tran 10u. Settling time is calculated with a 2% error.

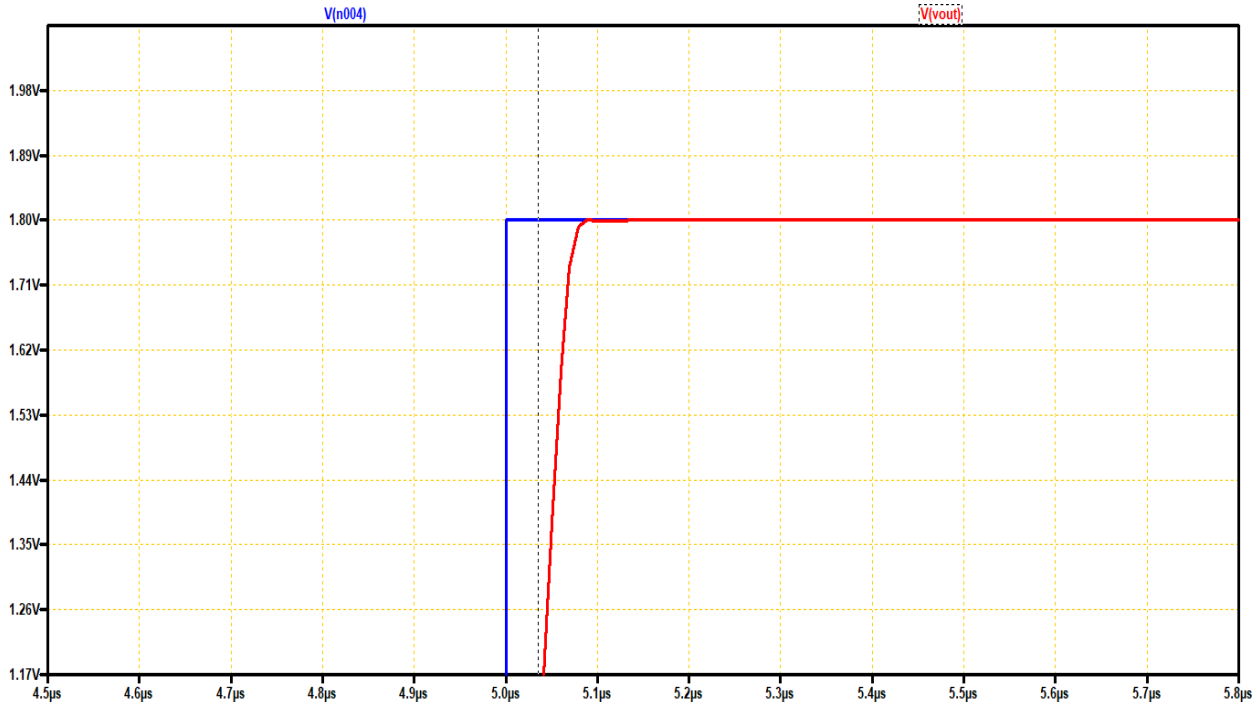

Fig 4.4: Step Response for Two-stage OTA(calculation of settling time 2% error)

Settling time:

The settling time is the time it takes for the response to reach and stay within the defined range (2 % to 5%) of its final value.

In above fig 2 % of 1.8 v is 1.76 v.

And time delay i.e. settling time at 1.76 v = (5.0732-4.998) µs

= 0.0752 µs

Power calculation:

Power $=\{I_d(M4)+ I_d(M7)\}\times 1.8v$

$=\{1.7859+1.02\}\times 10^{-5}\times 1.8v$

= 50.49 µwatt

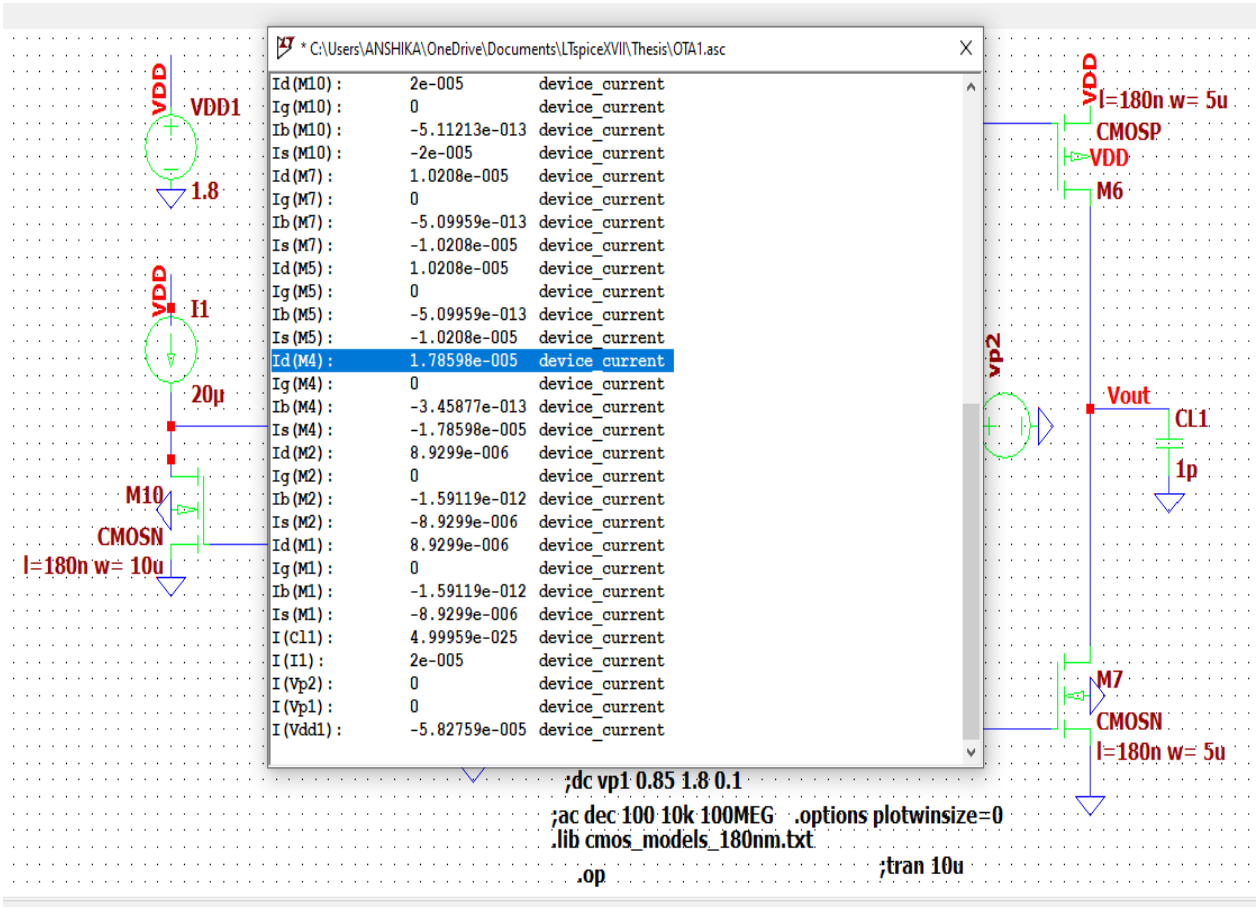

Fig 4.5: Showing Value of current (I_d) flows through M4 & M7

4.2 The Folded-Cascode OTA :

Figure 4.5 shows an example of an NMOS differential-amplifier-based folded cascode OTA. Let's look at what happens when VP is high in order to describe the OTA's working qualitatively (above Vm). Ml will turn ON and M2 will switch OFF as a result of this. When Ml is turned ON, it pulls M5's drain down, turning OFF M7. M9 and Ml pull the gate of M5 down as M7 shuts down. The current in M6 grows when the gate of M5 is lowered. Simultaneously, as the current in M2 decreases, the current in M8 increases, and the voltage atoutput rises.

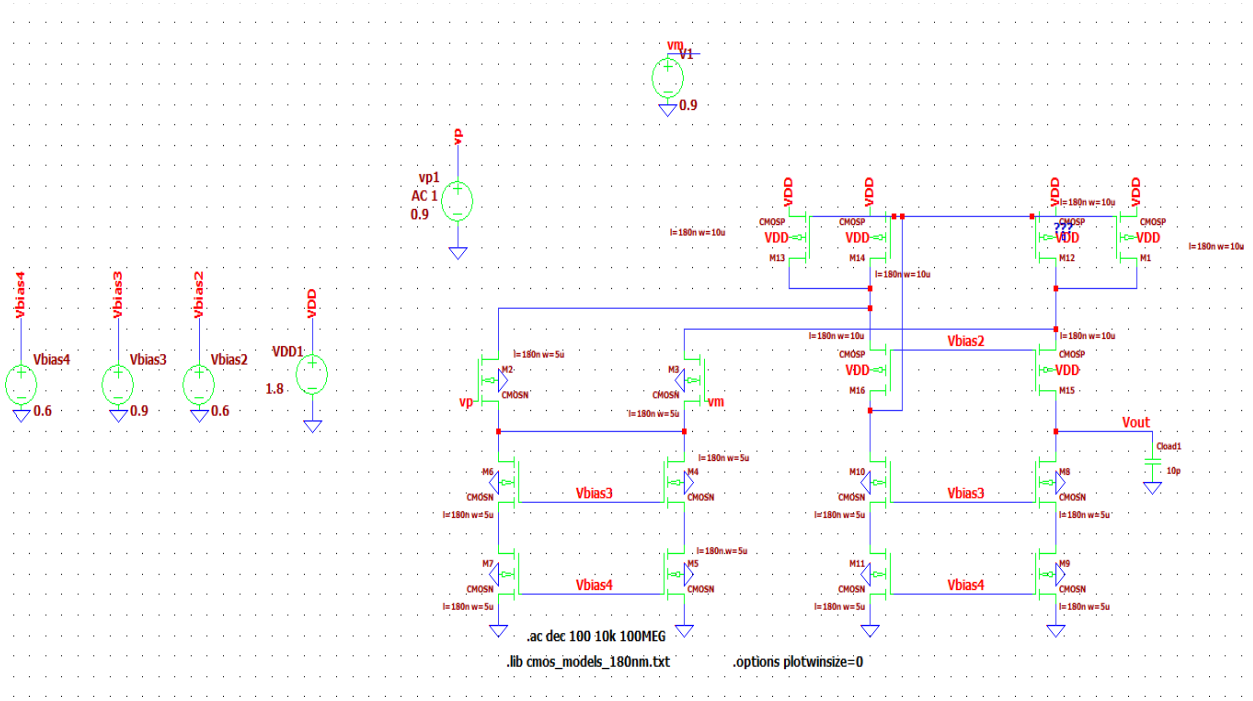

Fig 4.6: Schematic of folded cascode OTA

4.2.1 Frequency Response:

For frequency response inputs are given with AC 1 and with command .ac dec 100 10k 100MEG. From frequency, we calculate Unity gain frequency and Phase Margin.

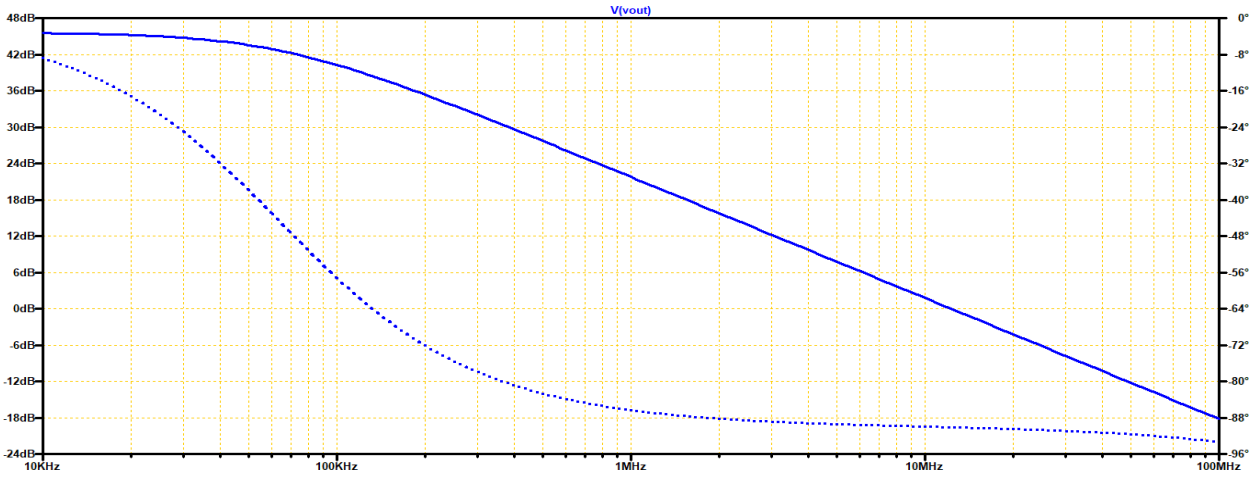

Fig 4.7: Gain and Phase plot of two-stage OTA

Gain=45.68dB
UGB=12.44MHZ

4.2.2 : DC Analysis:

DC Characteristics are obtained by sweeping the DC input from 0.1V to 1.8V Where all transistors of the two-stage op-amp are in saturation. DC analysis is done with the command:

dc vp1 0.85 1.8 0.1

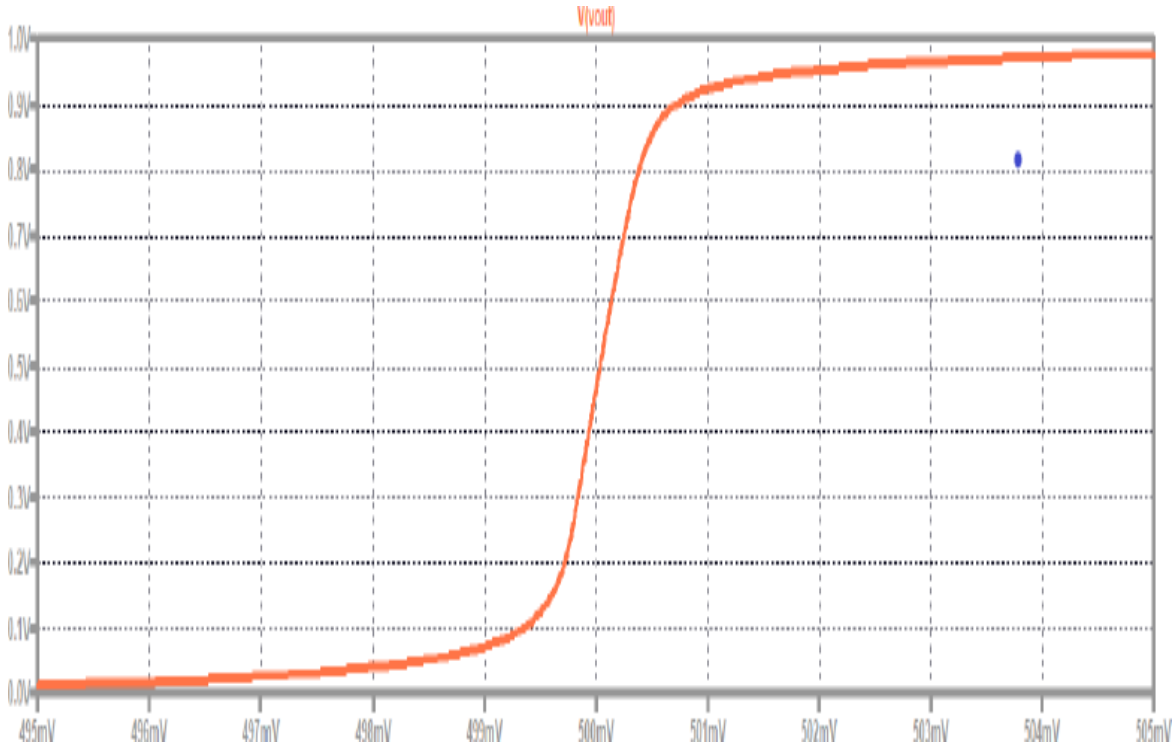

Fig 4.8: Vout versus Vin plot

4.2.3 Transient Analysis:

The step response is given to the input 0 to 1.8v and the output response is plotted with the command: . tran 10u. Settling time is calculated with 2% error.

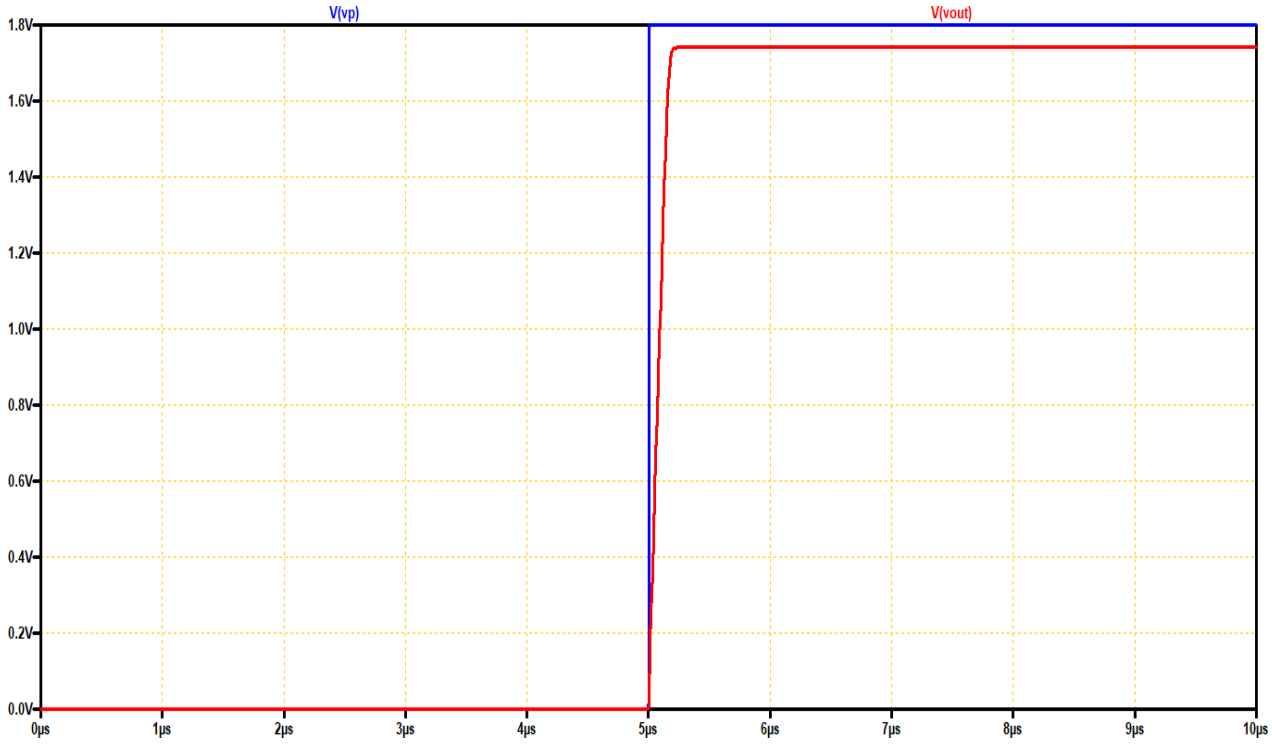

Fig 4.9: Step Response for Two-stage OTA(calculation of settling time 2% error)

In above fig 2 % of 1.8 v is 1.76 v.

And time delay i.e. settling time at 1.76 v = (5.29-5.02) µs

= 0.27 µs

Power Calculation:

Power $=\{I_d(M8)+ I_d(M6)\}\times 1.8v$

$=\{1.7859+1.02\}\times 10^{-5}\times 1.8v$

= 192.96 µwatt

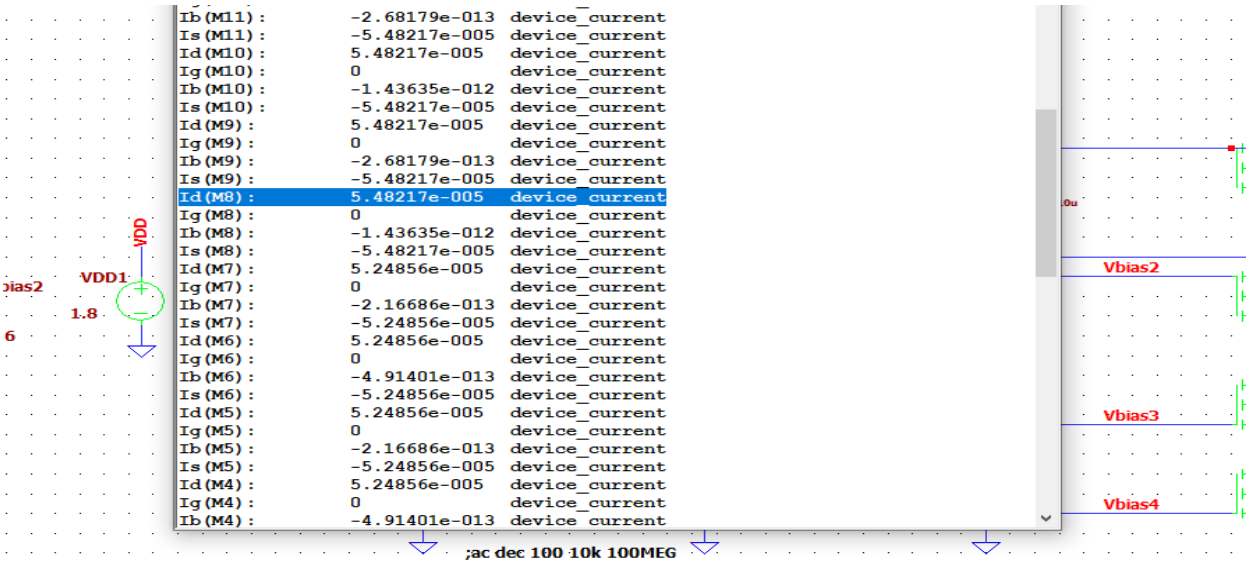

Fig 4.10: Showing Value of current (I_d) flows through M6 & M8.

4.3 Cascode OTA

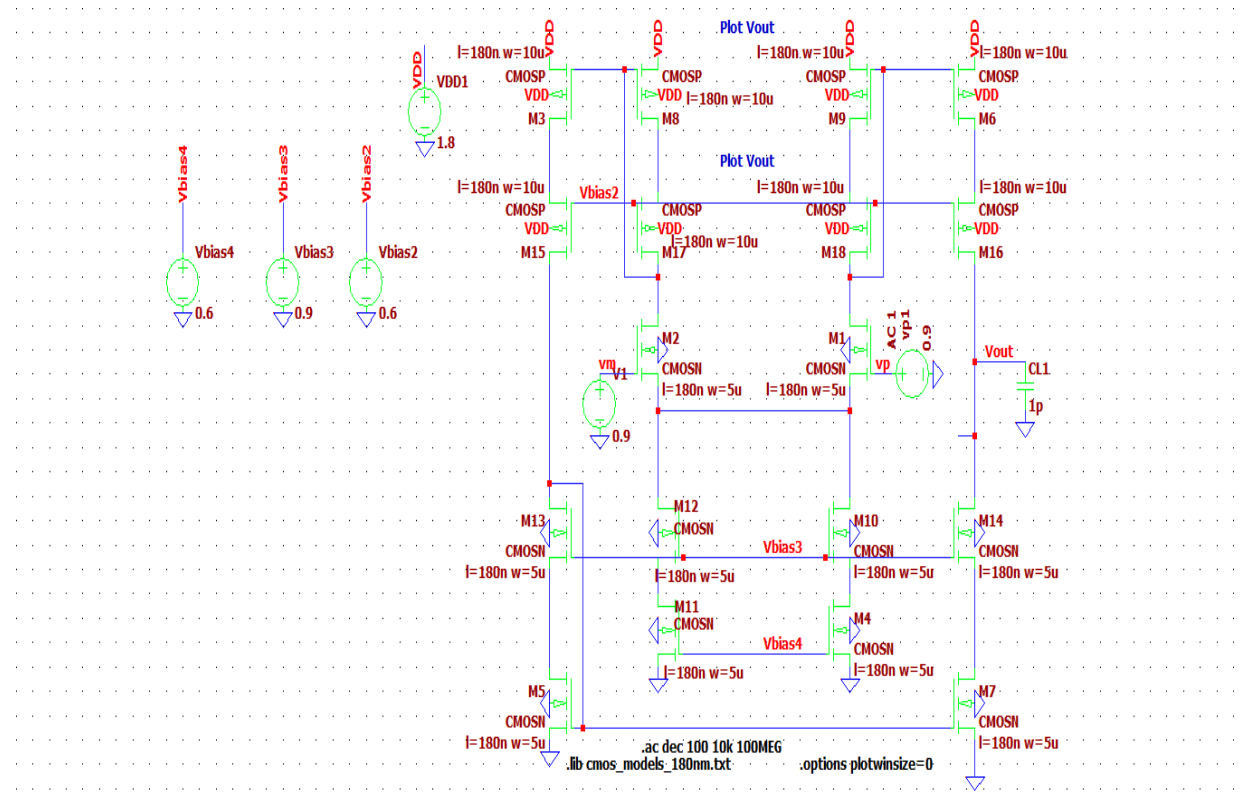

Fig.4.11:Schematic of Cascode OTA

4.3.1 Frequency Response:

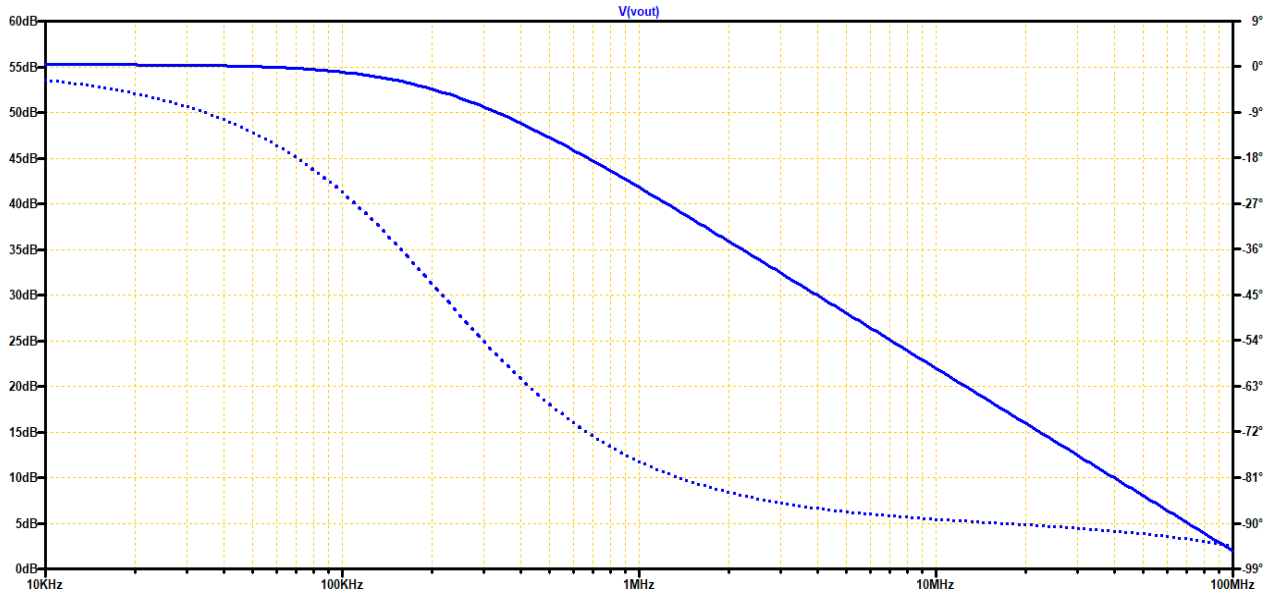

Fig 4.12: Gain and Phase plot of Cascode OTA

Gain=55dB

Unity gain frequency=13.883MHZ

4.3.2 DC Analysis:

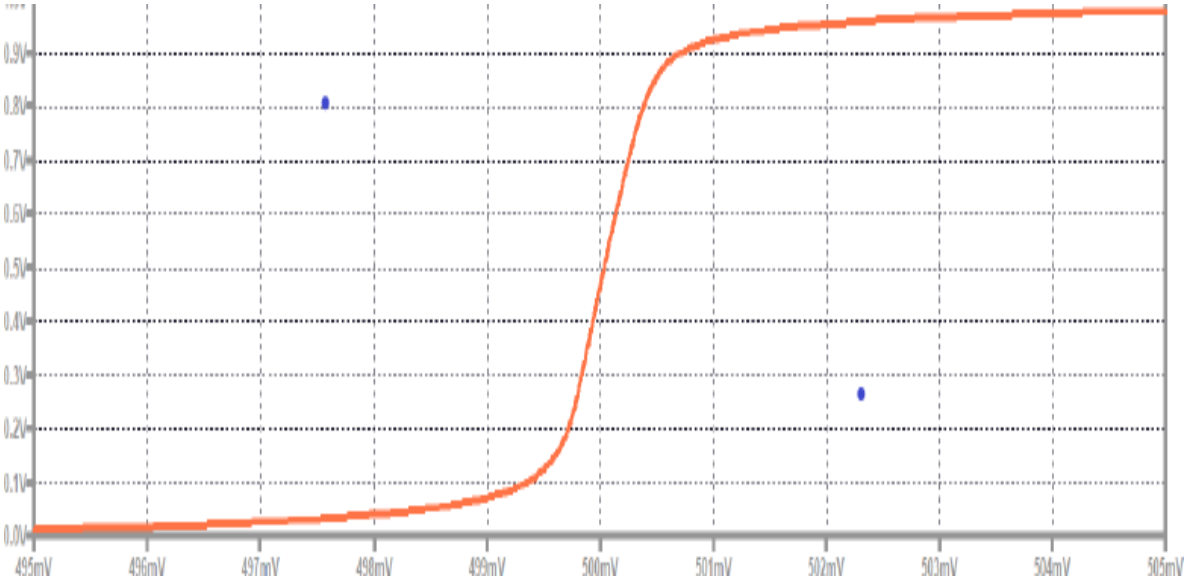

Fig 4.13: Vout versus Vin plot

4.3.3 Transient Analysis:

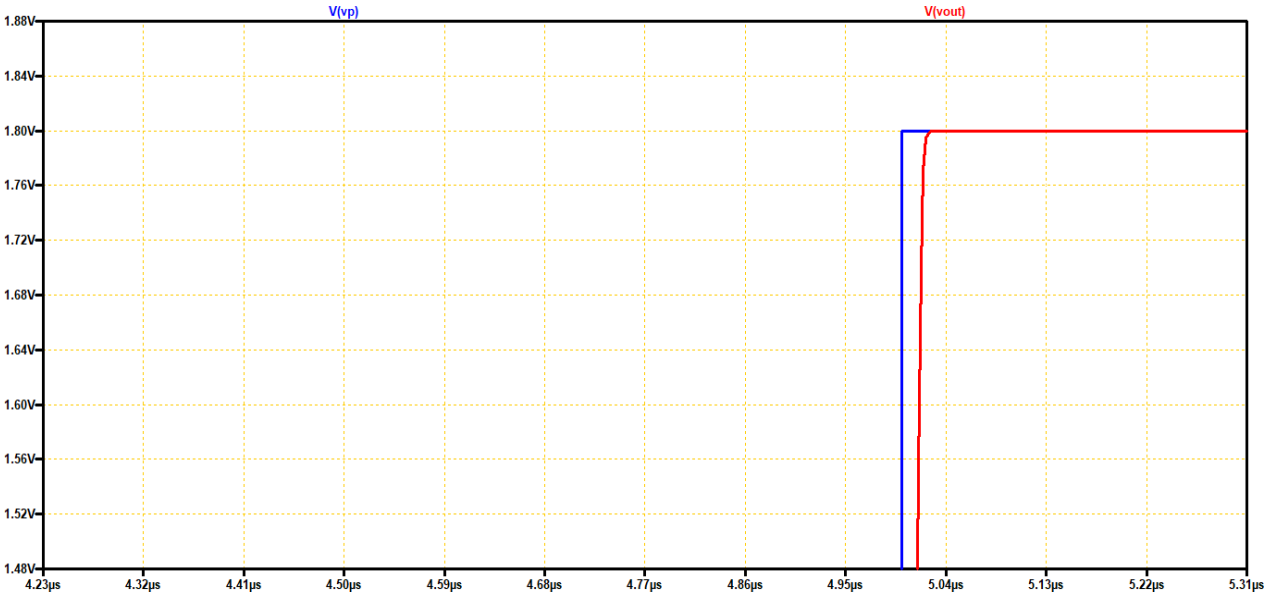

Fig 4.14: Step Response for Two-stage OTA(calculation of settling time 2% error)

Settling time = (5.0219-5.0037) µs

Power Calculation:

Power ={I_d(M14)+ I_d(M10)}× 1.8v

={5.25+5.23}× 10^{-5}× 1.8v

= 188.64 µwatt

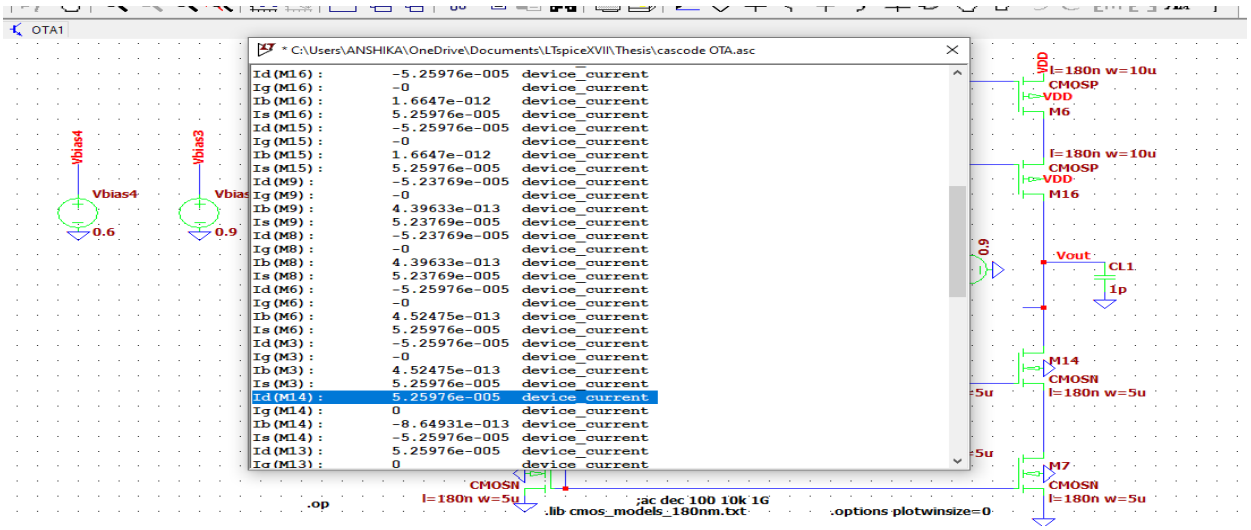

Fig 4.15: Showing Value of current (I_d) flows through M10 & M14

The next chapter will summarize the main conclusions and proposals obtained in this work and at the same time will propose suggestions in order to improve or expand this work.

4.4 Comparison & Analysis:

	OTA	**Cascode OTA**	**Folded Cascode OTA**
Gain	28 dB	55 dB	45.68 dB
Unity gain frequency	32.70 MHZ	13.88 MHZ	12.44 MHZ
Phase at 0 dB (PM)	70.036˚	79.89˚	59.98˚
Settling time	0.0752 µs	0.0182 µs	0.027 µs
Power	50.49 µwatt	188.64 µwatt	192.96 µwatt

CHAPTER-5
CONCLUSION AND FUTURE WORK

The previous chapters have provided important information about how analog design can remain in nanometer technologies. There are the two main concerns in nanometer technologies: the transistors in this type of technology are not suitable to develop useful specifications in analog circuits like amplifiers; with smaller sizes on transistors, the uncertainty in fabrication processes, environmental conditions and second-order effects, the variability in the circuit specifications raises significantly. Considering the above two concerns, the below summarizes the main contributions of this work and how they can be expanded upon and improved.

5.1 CONCLUSION:

This work proposed and also exposed some circuits, criteria, and considerations, in order to obtain robust and useful specifications for OTA'S. However, the propositions made can easily be expanded and applied to different circuits, to improve behavior, regardless of technology type and scale, as outlined below.

The circuit was developed by taking into account a variety of non-ideal situations that can influence parameters, and methods of circuit output were used to mitigate their effects in order to increase the circuit's performance and efficiency.

FinFET is the most advantageous platform because it provides high gain, high bandwidth, and a reduction in the short channel effect, as well as a variety of dimensions in which researchcan be conducted. As a result, an operational transconductance amplifier based on FinFET hasbeen chosen. The cadence tool was used in this proposed work to compare FinFET and CMOS-based

OTA circuits at 18nm. Except in some cases where research is underway to boost performance using FinFET, The parameter of performance of all built configurations shows that the OTA circuit based on CMOS outperforms the OTA circuit based on FinFET. In the two-stage OTA that has been implemented using FinFET, gain and bandwidth are increased while the circuit size is reduced, resulting in improved overall efficiency. In addition, as compared to CMOS-based OTA, some of the performance parameters in FinFET- based OTA are not up to scratch.

5.2 FUTURE WORK

With the development of this work arises new interesting topics to complement and enhance the current work. On the other hand, some tasks, simulations, and analyses must be done to finish the design flow for analog circuits in nanometer technologies. These are:

- .Due to the technology restricted sizing the layout stage represents a big concern. This is due to the technology incorporating many more layers than conventional technologies and the use of matrix transistors, which raises the complexity in the layout stage. However, the restrictions over the sizing could allow the automation of the layout in a similar way to that of digital circuits.
- Establish some criteria in other types of circuits that allow the making of a robust design in a clearer way.
- The most common way to try to compensate analog circuits is through biasing, for this reason, it is desirable to develop a variety of biasing circuits widely characterized in order to make easy and fast compensations in any design.
- Incorporate some techniques in order to reduce the circuit offset, and try to reduce the power consumption without losing robustness

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