ANALYTICAL MODELING AND SIMULATION OF DOUBLE GATE TFET FOR LOW POWER DESIGN AND PERFORMANCE ANALYSIS OF CNWFET

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT FOR THE AWARD

OF

MASTER OF TECHNOLOGY

IN

VLSI DESIGN & EMBEDDED SYSTEM

Submitted by

ANUPRIYA SRIVASTAVA

(2K19/VLS/03)

Under the supervision of

Dr. DEVA NAND

Assistant Professor

(ECE)

DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY

(FORMERLY DELHI COLLEGE OF ENGINEERING)

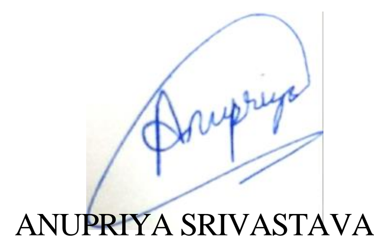
BAWANA ROAD, DELHI -110042

ELECTRONICS & COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, Anupriya Srivastava, Roll No. 2K19/VLS/03, student of MTech (VLSI Design & Embedded System), hereby declare that the Project Dissertation titled **"Analytical Modeling and Simulation of Double Gate TFET for Low Power Design and Performance Analysis of CNWFET"** which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not derived from any source without appropriate citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate-ship, Fellowship or other similar title or recognition.



Place: Delhi ANUPRIYA SRIVASTAVA

Date: 9th October, 2021

ELECTRONICS & COMMUNICATION ENGINEERING

DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled **“Analytical Modeling and Simulation of Double Gate TFET for Low Power Design and Performance Analysis of CNWFET”** which is submitted by Anupriya Srivastava, Roll No. 2K19/VLS/03, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Dr. DEVA NAND

Date: 9th October, 2021

SUPERVISOR

ASSOCIATE PROFESSOR

ABSTRACT

With the semiconductor industry scaling down to the nanoscale regime, the three factors come hand in hand that are namely the speed, power and the area. These three factors are inter-relatable and furthermore the power is classified as power consumed and the power dissipated. As we reduce the size of the Integrated Circuits (ICs), the power consumed by the circuit should also be reduced, and at the same time some effects become prominent at the nanoscale and therefore need to be considered. At the nanoscale, as these effects became prominent, this led to the modification in the structure of the devices to be used for the low power applications.

Moore's law has been the backbone of the VLSI industry which says that the transistors on the chip doubles every eighteen months and this has been followed up till now. The designing of the devices and the circuits on the EDA tools provided by the industry reduces the cost of manufacturing by a large scale as the fabrication of the devices is costly process.

This work proposes about the modelling of the TFET (Tunnel Field Effect Transistor) device that finds out the surface potential of device using the mathematical models. The work has been carried out using the TCAD Tools (Technology Computer Aided Design). This device proposes a good ON current for a device to operate and also the lower subthreshold swing than that of the conventional MOSFET device. The work done here is based on a 2D model of the Poisson's equation that is solved using the Parabolic approximation method and also certain conditions that limit the boundaries of the device called the boundary condition for a device and the conditions differ from region to region of the TFET device. Finally, the results have been simulated and compared with the previously work done on the Analytical modelling of the TFET device for a nanoscale regime.

TABLE OF CONTENTS

	Certificate	*ii*
	Declaration	*iii*
	Acknowledgement	*iv*
	Abstract	*v*
	List of Figures	*9*
	List of Tables	*10*
	List of Abbreviations	***11***
	CHAPTER 1	**12-15**
	Introduction	
1.1	Over view	12
1.2	Motivation	14
1.3	Literature Review	15
1.4	Tools Used	15
1.5	Organization of Work	15
	CHAPTER 2	**16-19**
	Literature Survey and Objective	
2.1	Literature Review	16
2.2	Research Gap and Motivation	18
2.3	Objectives	19
	CHAPTER 3	**20-30**
	Field Effect Transistors	
3.1	Transistors	20
3.2	Metal Oxide Semiconductor Field Effect Transistor	20
3.3	Enhancement MOSFET	21
3.4	Threshold Voltage	23
3.5	Region of Operations	24
3.6	Output Characteristics	25
3.7	Transfer Characteristics	26
3.8	Transconductance	27

3.9 Second Order Effects 27
3.9.1 Body Effect 27
3.9.2 Channel Length Modulation Effect 27
3.9.3 Subthreshold Slope 28
3.10 Limitations 28
3.10.1 Hot Electron Effect 28
3.10.2 Drain Induced Barrier Lowering 28
3.10.3 Mobility Degradation 29
3.10.4 Subthreshold Conduction 29
3.10.5 Punch Through Condition 30
3.10.6 Leakage Current 30
3.11 Nanowire Field Effect Transistors 31
3.12 Cylindrical Nanowire Field Effect Transistors 31

CHAPTER 4 **37-43**

Tunnel Field Effect Transistors

4.1 Alternative to MOSFET 37
4.2 Tunnel Field Effect transistors 37
4.2.1.1 Structure 37
4.2.1.2 Operation 40
4.2.1.3 Transfer Characteristics 41
4.2.1.4 Ambipolar Current 42
4.2.1.5 Advantaged of TFET 42
4.2.1.6 Limitations of TFET 42

CHAPTER 5 **43-48**

Device Design and Simulation Methodology

5.1 Introduction 43
5.2 Silvaco TCAD Tool 45
5.2.1 ATLAS Framework 45
5.2.2 Common Models 47
5.2.2.1 CONMOB 47

5.2.2.2 SRH 47
5.2.2.3 FERMI 47
5.2.2.4 BQP 47
5.2.2.5 Non-Local BTBT 47
5.2.3 Numerical Method 48
5.2.4 Estimation of Results 48

CHAPTER 6 50-69

An Approach to Analytical Modeling of TFET

6.1 Introduction 50
6.2 Model Development 51
6.2.1 Gate Regulation in channel's surface potential 54
6.2.2 Drain Regulation in channel's surface potential 56
6.3 Modeling for the Surface potential 57
6.3.1 Gate controlled region surface potential 57
6.3.2 Surface potential under drain control region 58
6.3.3 Surface potential for all operating regions 59
6.4 Drain Current Modeling of Double Gate TFET 67

CHAPTER 7 69-70

Conclusion and Future Scope

7.1 Conclusion of Analytical Model of DG-TFET 69
7.2 Future Scope 70

References 71-74

LIST OF FIGURES

Figure No.	Figure Description	Page No.
3.1	Device Structure of N-MOSFET	21
3.2	Output characteristics of the simple MOSFET	21
3.3	Transfer characteristics of the simple MOSFET	26
3.4	2D cut plane of the device	32
3.5	Simulated Cylindrical Nanowire FET Structure	33
3.6	Variation of the subthreshold slope with channel Radius	34
3.7	Variation of the subthreshold slope with channel length	34
3.8	Variation of the threshold voltage with channel Radius	35
3.9	Variation of the threshold voltage with work function	35
3.10	Transfer characteristics of the device with varying channel radius	36
3.11	Transfer characteristics of the device with varying work function	36
3.12	Transfer characteristics of the device with varying channel length	37
4.1	Device structure of single gate conventional TFET	38
4.2	Device structure of double gate conventional TFET	40
4.3	Energy Band Structure of double gate conventional TFET	40
5.1	Shortcuts of the tool involved in Silvaco ATLAS TCAD tool	45
5.2	Block diagram of design of device and its characterization	46
6.1.	Modeled Double Gate TFET Structure	52
6.2.	EBD during ON and OFF state.	54
6.3.	Transfer Characteristics for OFF state and ON-state current.	54
6.4.	Surface potential variation w.r.t gate biasing voltage, comparing our model to TCAD simulation results	55
6.5.	Surface potential variation w.r.t drain biasing voltage, comparing our model to TCAD simulation results	57

6.6. The device surface potential w.r.t lateral distance, comparing our proposed model and TCAD results 64

6.7. Surface potential w.r.t dielectric constant and comparing our model to TCAD simulation results.. 65

6.8. Surface potential w.r.t gate work function and comparing our model to TCAD simulation results. 65

6.9. Surface potential w.r.t materials used for and comparing our model to TCAD simulation results.. 66

6.10. Transfer characteristics of the DG_TFET device at a constant V_ds= 0.5 V with the comparison to TCAD simulation results with the modeled one. 68

LIST OF TABLES

Table	Table Name	Page
Table 6.1	Device Parameters	52

LIST OF ABBREVIATION

MOSFET	Metal Oxide Semiconductor Field Effect Transistor
IC	Integrated Circuit
CMOS	Complementary Metal Oxide Semiconductor
SCE	Short Channel Effects
HCE	Hot Carrier Effects
ITRS	International Technology Roadmap for Semiconductor
DIBL	Drain Induced Barrier Lowering
CNTFET	Carbon Nano Tube Field Effect Transistor
TFET	Tunnel Field Effect Transistor
BTBT	Band to Band Tunneling
AVSS	Average Subthreshold Swing
DG-TFET	Double Gate Tunnel Field Effect Transistor
VLSI	Very Large Scale Integration
FET	Field Effect Transistor
PVT	Process Voltage Temperature
CONMOB	Concentration Dependent Field Mobility Model
SRH	Shockley Read Hall Recombination
BQP	Bohr Quantum Potential Model
TCAD	Technology Computer Aided Design

CHAPTER-1

Introduction

This research is focused on the analytical modeling of a novel TFET architecture. The modeling is performed using the MAPLE software and is then simulated and verified using Silvaco ATLAS TCAD Tool. This chapter gives an introduction to the existing MOSFET technology and the challenges faced by it are presented along with the literature survey for the research carried out on the device for low power applications and its applications are discussed. Thesis organization is also included in this chapter.

1.1 Overview

Over the era of two decades, the CMOS technology has revolutionized the semiconductor industry whether we talk about the Analog Integrated Circuits or the Digital Integrated Circuits and the EDA tools have reduced the cost of manufacturing by a huge amount. The silicon and the compound semiconductors including III-V compounds still finds the niche applications [36]. The fabrication cost of the circuits is the major part including the minute steps of lithography and others similar steps in the fabrication. The CMOS technology still serves as the basic technology to design electronic circuits and will continue as it is. For the property of controlled conduction the semiconductors have been explored and this has led to the various experiments performed including the material engineering which performs the experiments on the different material that can be used to improve the conducting properties of the device. The effects at different-different scale are the reason to find a novel device which can carry the legacy of CMOS technology further. Finding the good properties (electrical) of the device with the reducing channel length is the first objective of the research in the VLSI Industry [9]. The electrical properties include the ON current of, OFF current, subthreshold swing of the device and mitigating the effects that come into the picture while we minimize the channel length. The effects such as the hot electron effect, second order effects and the fringing effects from the electric field at gate. The whole story of the VLSI industry revolves around the three parameters speed, power, and area of the chip or the Integrated circuit designed [9]. Reducing power or low power techniques are

being implemented at different level that could be at device level, circuit level or a system level.

The physics behind the working of the device involves some important properties that are to be focused upon, are the material properties that is being used for analyzing the device characteristics, carrier distribution, charge transport mechanism and junction physics and the effects at the nanoscale. For the recent time, 3 materials are being focused, these are Si, Ge, and the GaAs and certain other III-V compound semiconductors are being explored. High Electric field's impact on the carriers due to heavy doping at the junction which in turn causes tunneling of carriers at the respective junctions [28]. The interface or the surface between the semiconductors also classify them further, for example the interface of semiconductor with the metal is a Schottky barrier, then comes the semiconductor interface with an insulator is termed as Insulated Gate Field Effect Transistor (IGFET).

All the electronic equipment's that we use in our daily life has the semiconductor component inside it. Study of the semiconductor devices involves the solid state physics and the bandgap engineering now a days has become the essential part of semiconductor industry so as to find the appropriate material for the construction of the semiconductor device which can give a better or improved performance than the silicon based semiconductor devices. The significance in the electronic design will have to shift to the devices that are becoming increasingly capable [28]. Countless innovations by large number of scientist have helped the Moore's law to sustain since decades. Some of the great innovations are listed below that have played a vital role for the advancement of the IC technology in the past five decades.

1. Invention of the Complementary Metal Oxide Semiconductor (CMOS) in the year 1963 by Chih Tang Sah and Frank Wanlass at the Fairchild Semiconductor enabled extremely dense and high performance circuit.
2. Invention of Integrated circuit was one of the main contribution itself by the Robert Noyce at Fairchild Semiconductor and equally credited to Jack Kilby at Texas Instruments in the year 1959.

3. The invention of FAMOS memory in the early 1970's by the Frohman-Bentchkowsky post the invention of the Floating gate FET.

Some of the recent advances in the industry are listed as:

1. In the year 2010, a major breakthrough in the development of transistor took place which was the design and fabrication of the first Junction-less Transistor was announced.
2. In the year 2011, the development of the SET (Single Electron Transistor) which was 1.5nm in diameter was announced and was made out of oxide based materials.

The need of the Analog design engineer will always be there even of the digital circuits have acquired the major portion in the industry as the daily signals that we encounter are in the analog form, it may be the signals generated by the human body or any other communication signal that needs to be processed by an analog engineer [36], that is it must be first amplified using an amplifier circuitry and the further the digital parts comes into the picture that includes the Analog to Digital Converter (ADC) that is further processed.

1.2 Motivation

Moore's law being followed since five decades and can continue for the next decade in the designing of the Integrated Circuits which says that the number oftransistors on a chip doubles almost every 18 months. The recent trends of research in the semiconductor device motivated me to contribute some in this field in any way that could be helpful for me and also for the society through the practical solutions.

The Tunnel Field Effect Transistor (TFET) can be promising candidate for the semiconductor industry for the CMOS technology to proceed and therefore a lot of research or you can say work is going on the TFET device development as it shows some promising properties for the device to work in the Integrated Circuit Technology as it has low subthreshold swing but with also less ON current. The Analytical modelling of the TFET device has been carried out to procure the surface potential of device. The TFET's electrical properties shows some promising properties as a successor to the CMOS Technology.

1.3 Literature Review

This is one of the crucial part of the research in any field, where we should be known of the facts what's happening in the field, by this I mean that one should be aware of the latest research been carried out by the different researchers not only across the country but globally. What work can be extended from the previous research on the topic to extract some more beneficial information for the betterment of the society. Will talk about the literature survey as complete section in the chapter No.2 where we will discuss about the research paper reviewed before starting my work.

1.4 Tools Used

This thesis work has been carried out on the MAPLE platform version 2018 and the compilation of the results has been carried out using the Origin Pro tool and also the Mendeley tool for the literature survey.

1.5 Organization of Work

The thesis work has been organized in the following manner:

Chapter 2: Describes the Literature survey of done during and before carrying out the work and also the Research gap and the Objective of the work carried out.

Chapter 3: Describes the existing MOSFET, its structure, mechanism of the conduction of current in the device and the Nanowire FET.

Chapter 4: Describes the Tunnel Field Effect Transistor, its structure, mechanism of the conduction of current in the device.

Chapter 5: Explains the methods to model and simulate the semiconductor device and the important features of the Tool used.

Chapter 6: Focuses on an approach to the Analytical Modeling of the TFET device.

Chapter7: This chapter talks about the work that can be done in future and the conclusion of the work that has been carried out.

CHAPTER-2
Literature Survey and Objective

In this thesis work our focus is to Model a Double Gate TFET for the device's surface potential and the drain current of device to achieve better higher on-off current ratio (I_{ON}/I_{OFF}) which is the only point that puts the TFET device into doubt as a replacement for the existing CMOS technology. Our focus in this chapter will be to discuss the work that has been reviewed before to know about the findings that have been achieved by the researcher in this field. This chapter presents the literature survey of research papers based on DG-TFET (Double Gate Tunnel Field Effect Transistor) and Modeling paper related to the DG-TFET structure. Research gap and objectives are also included in this chapter.

2.1 Literature Review

Lining Zhang et al. [1] have proposed a model for Double Gate TFET in which the novelty of the model is in term of considering the capacitances of the device accurately. Further the device is modeled with the perspective of designing the low power circuits such as they have presented an application of SRAM and the basic logic circuits using the modeled TFET device. This paper was reviewed with the perspective of extending the research work to the circuit level.

Zhijun Lyu et al. [2] this paper by the authors have presented their work on the DG-TFET device in which the full analytical modeling has been done using the basic 2-D poisson's equations to obtain the equations for the surface potential and the current of the device at the drain terminal. This work considers the charges at the source depletion region. The results procured after the modeling are on the 100nm technology that mean the channel length is 100nm of device and further the results obtained match with the TCAD simulation results.

Chunlei Wu et al. [3] proposed work by the author presents their work with novelty by considering the dual modulation effects and for studying this effect the paper has been reviewed for carrying out the work. But the work has been carried out on device

dimension with gate length of 200nm and the surface potential has been obtained for all regions of the device. This paper also uses the basic 2D poisson equation for deriving the model of surface potential. And for the current model it uses the generation rate concept of charge carriers using Kane's model to predict the accurate drain current model of the device.

Sangwan Kim et al. [4] This paper also presents the same surface potential's analytical model only and was reviewed to get through the basics of how to start the modeling of the device. The paper also has the same dimension of the device with gate length of 100nm and with some concept of the fringing capacitances both the inner and outer fringing capacitances.

Boucart et al. [9] has proposed the DG-TFET and showed that the characteristic and execution of a DG-TFET has improved as compared to single gate TFET. With the help of different high-k gate dielectric material in DG-TFET device they have shown the improvement in ON current as 0.23mA at gate voltage 1.8V and OFF current less than 1fA. They have achieved an AVSS of 57mV/decade and minimum point slope of 11mV/decade. They also achieved the ION/IOFF current ratio more than 2e11 for a channel length of 50 nm [9].

Vandenberghe et al. [14] have proposed a new structure with full length and short length gate of the DG-TFET. With the help of Kane's generation model, he proposed an analytical ON current model for this DG-TFET. ON current is depends on the band gap of material, oxide thickness, doping level of source and drain. In the proposed short gate DG-TFET ON current flows with the help of point tunneling and line tunneling mechanism of the charge carriers. The small oxide thickness improves the ON current [14].

Menka Yadav et al. [16] proposed a model for the symmetric and asymmetric 3-terminal and 4 terminal double gate n-TFET. Modeling has been performed in subthreshold regime, where no Quantum Mechanical (QM) study has been considered.

The device consists of HfO2 as a gate dielectric material. The proposed model showed that the Vth of the device can be adjusted with the help of appropriate gate work function. It also has an advantage of volume inversion. Due to the use of 4T the device has a flexibility of adjusting the threshold voltage as per the requirement. The analytical modeling is robust in terms of scaling [16].

Bhowmick et al. [17] Proposed a DG-TFET with hetero material at gate dielectric and low band gap material at source side. The I_{ON}/I_{OFF} ratio has been improved with the help of low-k dielectric at source side and high-k dielectric at drain side. Also, they have used Germanium at source side to increasethe tunnelling probability hence the ON current. They have developed the analytical model for DG-TFETs electric field with the help of basic Poisson's equation and which is helpful for determining the subthreshold swing, output conductance, trans-conductance, and gate threshold voltage and the drain threshold voltage parameters. A hetero gate material dielectric DGTFETs have 53 mV/decade subthreshold swing and mA range ON current and better immunity of the short channel effects [17].

Prabhat et al. [20] proposed a novel of analytical modeling for surface potential and drain tunneling current for the DGTFET. The tunneling width at the drain and source junctions are calculated by the surface potential. The width of the tunneling junctions at source-channel and channel-drain are used as limits in the integration of the BTBT rate for calculation of the drain tunneling current. Ambipolar current is measured in the DG-TFET considering the BTBT (Band-2-Band Tunnneling)in both source and drain junction. The modelled results were verified by simulation results of the device by SILVACO TCAD tool [20].

2.2 Research Gap and Motivation

A conventional MOSFET suffers from short channel effects and it does not deliver the adequate performance in the nanometre technology (existing and future technology). For the technology innovation perspective, we have chosen the research work in the

Nano scale technology and a silicon semiconductor based TFET, which has high ON current to OFF current ratio, low leakage current and steeper Subthreshold slope as compared to the MOSFET [9]. Further, we have developed the model for surface potential and the drain current of the device. the work that could be done on the DG-TFET device was to model for the reduced device dimensions so that the modeled device could be compatible with the ongoing/existing technology for the designing of the circuits for the low power applications. The conventional TFET have an surface potential's analytical model, electric field, ON current, OFF current, transconductance, drain tunnelling current and leakage current etc. so the work proposed here has the device dimensions reduced to channel length of 40nm, so it is proposed for a Future electronic device which is used in high performance and low power application. The modeled results are verified with the simulation result of the device by SILVACO TCAD tool.

The current-voltage (I_D-V_G) characteristics (transfer characteristics) of the conventional Metal Oxide Semiconductor FET shows the subthreshold slope of 60 mV/decades i.e. the Boltzmann distribution limits, which cannot be reduced further for the MOSFET. From this subthreshold slope we infer that to increasethe drain current by a decade then the gate voltage shoould be increased by 60 mV. In a MOSFET there is a ratio in on current and off current by at least 10^6, so for all devices, the supply voltage is at least 1 Volt. To decrease the subthreshold slop below 60 mV/decade of the device or a device which switching characteristics are much faster.

2.3 Objectives

The aim of this work is to design a model for the surface potential of the device and also for the drain current of the device and the work carried out is done with channel length of 40nm. This work is divided into following two objectives.

- Design and analysing the Cylindrical NWFET for the cardinal elements such as the Subthreshold slope, threshold voltage and transfer characteristics with variation of channel radius, length, and workfunction.
- Developing the analytical model for surface potential and also the drain current of the Double Gate TFET structure for reduced dimensions (channel length of 40nm).
- Comparison of the simulated and modeled Double gate TFET structure results.

CHAPTER-3
Field Effect Transistors

In this chapter, we discuss the concept of Field Effect Transistors and the advantage of using them is discussed. This chapter mainly focuses on the MOSFET and the working of this device, various operating regions, operation modes and some of the advantages have been discussed.

3.1 Transistors

The word transistor is derived from the two words that are 'trans' meaning transfer and 'resistor' meaning resistance in total meaning the transfer of the resistance. Transistor is basically a 3 terminal device in which the important feature is that the current through the two terminal is controlled by current or the voltage at third terminal. If the current is controlled by the current it is then classified as Bipolar Junction Transistor and if the controlling parameter is the third terminal voltage then it is Field Effect Transistor [28]. This controlling feature of the transistor helps us to amplify small signals of our importance or to work as a switch. The operation of the Field Effect Transistor device depends on the electric field intensity produced in the channel. It is being preferred over the bipolar junction transistor for designing the Integrate Circuits as the current in the device is because of the majority carriers and has less noise and leakage current than the MOSFET.

3.2 Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

In these transistors the current at the two terminal is controlled by voltage at the third terminal that is the Gate terminal here. These transistors have been the backbone of the Integrated circuit technology, in the digital Integrated circuit technology MOSFET is the most widely used electronic device in which the gate electrode isolated from the channel by using an insulator. Since most of the semiconductor devices are being fabricated using the silicon technology so we use SiO_2 as the insulator or the gate oxide to isolate the gate electrode from the channel of the MOSFET or any other (IGFET) Insulated Gate Field Effect Transistor.

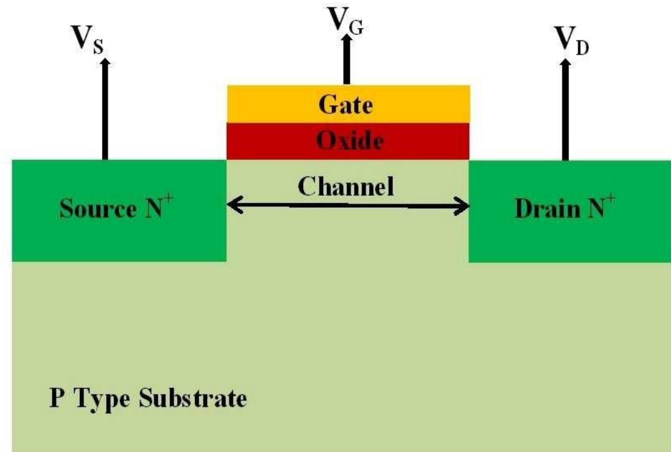


Fig. 3.1 Device structure of N-MOSFET [5]

MOSFET is basically classified into two types that are the depletion-type and the enhancement-type MOSFET, generally we use the enhancement type MOSFET because the channel is formed when we apply the bias at the gate terminal and the conduction of the current takes place in the device. Based on the bias applied at the gate and also the drain terminal the operating regions of the MOSFET are defined [28]. MOSFET can operate in the 3 regions mainly that are the (i) Cut-off Region (ii) Linear or Triode Region and the (iii) Saturation Region. The equations for the above operating regions can be given as:

For Triode or Linear Region of operation:

$$Vds < (Vgs - Vth)$$

$$Vgs > Vth$$

For Saturation region of operation:

$$Vds \geq (Vgs - Vth)$$

$$Vgs > Vth$$

3.3 Enhancement MOSFET

The Enhancement MOSFET is operated under the strong inversion channel and is sometimes called inversion layer. In this the channel is called as induced channel because it is induced from the large electric field intensity developed in the channel.

This MOSFET is designed using the planar technology. In the gate region, a parallel plate capacitor is created with metallic plate (gate plate) and induced channel as the second plate of the capacitor and the SiO_2 insulating layer work as a dielectric between the two plates of the capacitor. Because of the high input impedance the gate current or the input current of the device is ideally zero. The high input impedance of the device is due to the SiO_2 dielectric present at the gate terminal. Earlier the gate terminal was made using the metallic plate or the aluminium plate, but now it has been replaced by the polycrystalline silicon material.

For the enhancement-mode n-channel type device formed on p-type silicon substrate. The source and the drain regions are diffused with the n^+ impurity with a relatively lightly doped substrate of p-type impurities and also the thin oxide layer between the metallic gate and the silicon substrate. For the device to conduct the current there should be some channel formed between the source and the drain regions and for the n-type enhancement-mode MOSFET the channel should be of n-type only [36].

When we talk about the band diagrams of the MOSFET, the fermi level is close to the conduction band for the n^+ type source or the drain, and it is closer to valence band for the p^+ type semiconductors. Due to this potential barrier between the materials the flow of electrons is restricted and requires some potential so that the electrons get excited and crosses this potential barrier from the influence of the electric field. When we apply a positive voltage at the gate in comparison to the substrate, the positive charges are accumulated on the gate metal and due to this the negative charges also get accumulated in the substrate region near the Si-SiO_2 interface and this accumulation of negative charges near the interface give rise to a depletion region which is a thin layer of mobile charges, and as the potential is increased this layer gets inverted and the flow of carriers from the source region to the drain region starts giving rise to the flow of drain current in the device [28]. As the majority carriers are flowing in from source region to the drain, the current flows from drain to source. The gate voltage affects the conductance of the induced channel and this relation between the gate voltage and the drain current

is termed as the transfer characteristics of the MOS device, this defines that how our input voltage changes the drain current flowing in the device.

3.4 Threshold Voltage

The transfer characteristics of this device also defines a voltage called the device's Threshold voltage. Threshold voltage is the cardinal element required for turning the transistor ON or OFF. Its minute adjustment according to design specifications is of utmost priority in order to match our device with other circuits.. Now when the interface potential reaches a sufficient positive value, the flow of carriers start from source to the drain region through the interface or the channel formed. We now say that the interface is inverted and this value of voltage for which the channel is inverted is termed as the threshold voltage of the device. Now if we increase the gate potential further the charge in the depletion region remains somewhat constant but the charge density in the channel continues to increase, thus providing more current from source to drain. According to semiconductor physics, the threshold-voltage of the MOSFET can be defined as voltage for which the interface is as much n-type as the substrate is p-type [36].

The threshold voltage of the device can be expressed as:

$$Vth = \varphi ms + 2\varphi f + \frac{Qdep}{Cox}$$

The threshold voltage of the device can be adjusted by doping in the channel at the time of fabrication and this alters the doping concentration near the interface.

Now after a sufficient gate voltage, the negative charge carriers are induced in the p-type substrate region and in the channel the p-type impurity reduces thus the valence band moves down and the fermi level and valence band gap increases. The barrier

between the source-channel-drain reduces and thus the electrons can flow easily from the source region to the drain region [28].

The definition of threshold voltage for the depletion mode MOSFET changes because the channel is already formed in this type of MOSFET and we need to deplete the channel to turn OFF the device. Let say, for n-channel device the channel is existing for the zero gate voltage and then we apply negativevoltage at the gate terminal to turn the device OFF.

3.5 Region of Operations

1. **Linear or Triode Region:**. When the voltage at gate is increased the current increases linearly in the starting, and the potential in the channel varies from source to the drain due to the Ohmic voltage drop. Now as the voltage at the drain terminal increases the channel formed starts getting pinched off from the drain side and then some constant current flows in device. The MOSFET operates a resistor which is controlled by gate voltage, and theequation for the drain current is given by:

$$I_d = \frac{\mu_n C_{ox} w}{2L}(2V_{DS}(V_{GS}-V_{TH})-(V_{DS})^2)$$

2. **Saturation Region:** As we keep on increasing the gate voltage, at some point we see that the channel formed starts getting pinched from the drain side as the drain voltage also increases and at this time only some of the carriers are able to jump to the drain region and this continues till a particular voltage and the constant current flows in device. The carriers flow continues because of the high electric field in the channel. The term L in the equation considers the (CLM) channel length modulation effect in the device [36]. This effect depicts the dependence of drain current on the drain voltage, this is similar to the early effect in the bipolar junction devices. The MOSFET in the saturation region can be used as a current source connected between drain and the source. The current source injects current into ground or draws current

from the supply Vdd. In other words only one terminal of each current source is floating. The equation of the current in saturation region is given by:

$$I_d = \frac{\mu_n C_{ox} W}{2L}(V_{GS}-V_{TH})^2 (1+ \lambda(V_{DS}-V_{DSsat}))$$

3. **Cut-off Region:** Below threshold-voltage, device is OFF state. Ideally, he drain current as zero but possibility of leakage current in device and this is e subthreshold leakage current.

$$V_{GS} < V_{TH}$$

4. **Deep Triode Region:** The MOSFET operates in this region when the Vgs ≥ Vth and Vds ≪ 2(Vgs-Vth). While working in this range it acts as a linear resistor and is regulated by overdrive voltage..

3.6 Output Characteristics

The output characteristics of the MOSFET is the relation between the current at drain terminal and the drain voltage or it can also be called as drain characteristics. When the voltage at gate terminal becomes greater than device's threshold voltage, then the current is represented by the drain current equation of the linear region as the channel works as a linear resistor depending on Vgs. Now as we increase the drain voltage the voltage near the drain terminal across the oxide decreases and the charge there becomes smaller and therefore the channel starts pinching off from the drain side and the current flowing in the device saturates. The saturation current flows for the large drain voltage. The output characteristics of a n- channel MOSFET lies in the first quadrant and for the p-channel MOSFET it lies in the third quadrant. The characteristics have been displayed below from the simulation.

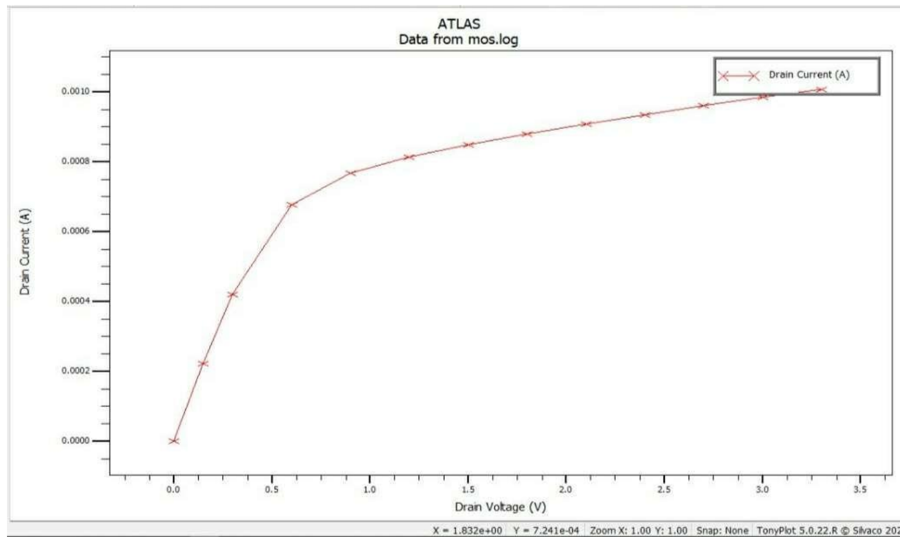


Fig. 3.2 Output characteristics of the simple MOSFET device

3.7 Transfer Characteristics

Transfer characteristics of a device is the plot between the output parameter and the input parameter. For MOSFET, the transfer characteristics is the plot relating the output drain current and input gate terminal voltage for a constant bias at the drain terminal. In linear region the plot is linear function of the input voltage and is therefore a straight line. But at the higher gate biasing the current increases somewhat sub-linearly. The transfer characteristics in saturation has the quadratic dependence on the gate voltage. The characteristics have been displayed below from the simulation.

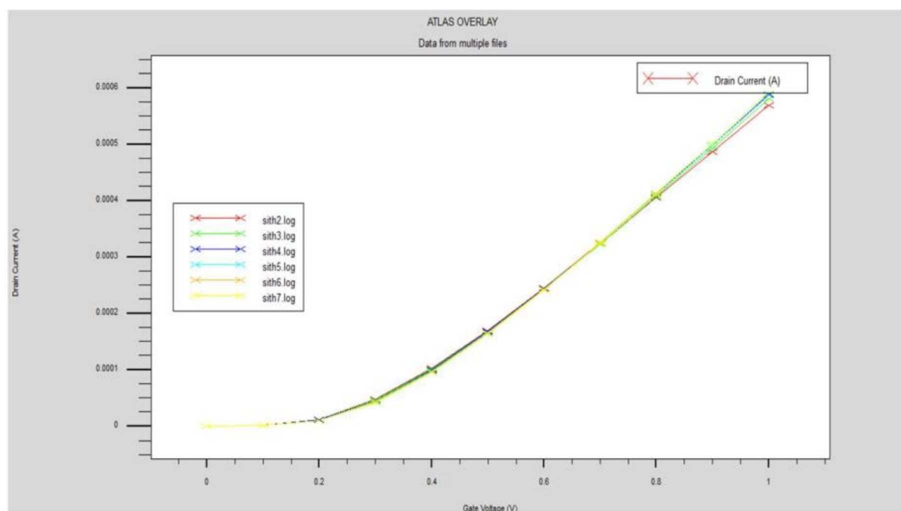


Fig. 3.3 Transfer characteristics of the simple MOSFET device

3.8 Transconductance

This is the most important parameter of the MOSFET and is defined as a figure of merit that tells how well a device transforms the voltage to current. The change in the current at the drain terminal to the change in voltage at the gate-source terminal is defined as the transconductance. It is also said as the current driving capability of the device. So, we can say that for a high transconductance (g_m), a minute change in the gate voltage results in the huge change in drain current [36]. And we prefer a device with a higher transconductance value. In the saturation region the value of transconductance is inverse of the ON resistance in the deep triode region.

$$g_{\mathrm{m}} = \frac{\partial I_{\mathrm{D}}}{\partial V_{\mathrm{GS}}}$$

3.9 Second Order Effects

The analysis done up till now has excluded the effects that affects the practical performance of the device. Here we talk about the 3 second order effects:

3.9.1 Body Effect: This effect is also termed as backgate effect because the substrate or the body terminal also start working as the second gate. Initially we assumed that body and the source terminal were connected to ground but this is not the case practically, as when the voltage at the body terminal drops below the voltage at source terminal. This effect can understood by assuming the voltage at the drain and the source terminal to be zero and the as the body voltage is less than the source voltage, depletion layer formed near the interface becomes more wider and thus the device's threshold voltage increases, thereby affecting the performance of the device. Therefore we tie the body terminal of NMOS to the lowest potential and that of PMOS to the highest potential in the circuit [28].

3.9.2 Channel Length Modulation: When the channel pinch –off occurs, we see that the actual length of the channel is different from the channel length that we assume as it decreases when the difference between the bias at the drain and the gate terminal increases and this channel length becomes the function of the bias voltage

at the drain terminal. This is effect is denoted by the term L in the drain current equation.

3.9.3 Subthreshold Conduction: Till now we have assumed that as soon as the voltage at gate drops below the threshold voltage, the device goes to the OFF state and thus the drain current becomes zero. But practically this doesn't happens as still there exists a weak inversion layer which conducts some current and this current has exponential dependence on the gate voltage. This conduction of the device is called as the subthreshold conduction [36].

3.10 Limitations

As the technology is scaling down rapidly, certain parameters have become more essential, these are power, area and the speed of the circuit. With the scaling of the device, certain effects become prominent at the nanoscale and thus this results in the limitation of the existing MOSFET. Some of the effects are briefed below that the MOSFET triggers.

3.10.1 Hot Electron Effect

In the MOS device when the electron moves from source to the drain terminal, the electric field increases towards the drain terminal because of the drain biasing and the electrons moving get excited and have high kinetic energy. This effect becomes more prominent when the device dimensions comes to the nanoscale and as the electrons can easily be trapped in the interface at the gate terminal or it can tunnel through the gate terminal thus affecting the drain current of the device that is the drain current reduces because of the reduction in the carrier concentration in the channel [28]. To overcome this effect, we use Halo doping in the device according to which the doping is denser near the junctions and the uniform along the rest of the device area. There is no Hot hole effect as the effective mass of the proton is higher than that of the electron so the tunneling of the protons through the gate terminal becomes somewhat difficult and therefore we only say that there is Hot electron effect in the device.

3.10.2 Drain Induced Barrier Lowering

This effect comes into the picture due to three reasons, first one being because of the inappropriate scaling of device and the second reason is because of the less concentration of the doping in the channel region & the third one being because of the width of the source and the drain regions, these issues in the device results in the unpredicted electrostatic interactions in between the source and the drainregions which is termed as DIBL [28]. These issue further results in widening of the drain depletion region which widens towards the source side and that results in the punch through condition in the device. To overcome this, the doping profile of the channel region should be made sufficiently high.

3.10.3 Mobility Degradation

Drain current of the device is because of the flow of the charge carrier and the mobility of the carriers affects the current. Therefore the variation in the mobility of the carrier needs to be considered. The degradation in the mobility is largely because of two reasons:

- Lateral field effect:. Source to drain carrier flow causes them to go through the roughness at the junction of $Si\text{-}SiO_2$ and this results in the scattering and finally in the mobility degradation [6].
- Vertical field effect: Is a consequence of Vgs. With increase in this voltage, the terminal increases this results in the charges coming near the oxide-substrate interface resulting in scattering thus decreasing mobility, which leads to velocity saturation [6].

3.10.4 Sub threshold Conduction

In an ideal MOSFET device, we examine that the drain current abruptly becomes zero as soon as the voltage between the gate to source (V_{GS}) reduces to below V_{TH}. But practically, still there exists some amount of conduction at drain terminal below threshold-voltage due to weak-inversion layer formed in the channel, which allows charges to move from source terminal to the drain terminal, this type of conduction of drain-current is termed as sub-threshold conduction.

3.10.5 Punch through Condition

When the biasing voltage at the drain terminal (V_{DS}) increases then the drain depletion region widens towards the source region and this condition results in a single depletion region in the device. This results in the very high electric field as the electric field then becomes a solid function of voltage at drain. Equation (1.2) shows the punch -through voltage[7]

$$V_{TH} = \frac{qN_A L^2}{2s_S} \tag{1.2}$$

q, Na, L, and ε_s are the electronic charge, doping concentration, length of channel and dielectric constant of the silicon.

3.10.6 Leakage Current

The power consumption of the MOSFET depends heavily on the supply voltage of the circuit and is proportional to square of supply voltage, and as we reduce the supply voltage the leakage current of the devices increase. This is because the threshold voltage will also be reduced which results in less noise margin of the device and the transition region between the ON and the OFF state becomes less and thus the metastability of the device increases which affects the operation of the device for some applications. This can also result in the conduction of the device even in the OFF state because of the weak inversion region formed.

$$I_{sub} = I_0 e^{\left(\frac{V_{GS}-V_{TH}}{\eta V_T}\right)}\left(1 - e^{-\frac{V_{DS}}{V_T}}\right) \tag{1.3}$$

$$I_0 = \frac{W\mu_0 C_{OX} V_T^2}{L}\,(\eta - 1) \tag{1.4}$$

$$V_T = \frac{KT}{q}$$

Where, W, L, V_{GS}, V_{TH}, V_{DS}, Cox, and μ_o are the width, and the length of the channel, gate-biasing voltage, threshold-voltage, oxide-capacitance and mobility of the charge carriers of the device, respectively.

3.11 Nanowire Field Effect Transistor

Any design of the device below the 100nm range comes in the nanoscale regime. This technology is under the research as an alternative to existing MOS technology. Under the nanoscale technology various structure modifications are being studied [37]. Nanowire field effect transistor is a rod shaped structure and in that the source drain and gate regions are specified. It can be further studied in Gate all around NWFET. Then under the nanoscale different structure were proposed and some are used commercially such as the FinFET technology. The FinFET was named from its shape as it has structure like that of a fin of fish and due to double gate and tri gate structure it has more control on the device electrical characteristics. The nanowire transistors are effective in reducing the short channel effects in the devices, leakage currents and but the nanowire transistors suffers one major drawback ofreliability issues.

3.12 Cylindrical Nanowire Field Effect Transistor

This work started with the design and analysis of the Nanowire FET specifically Cylindrical Nanowire FET, in which we focused on the cardinal elements of the device that are the threshold voltage, subthreshold conduction and also the transfer characteristics of the device designed. The designed device was analyzed by varying device structural parameters such as the radius of the channel, channel length and work function of the material used at gate terminal.

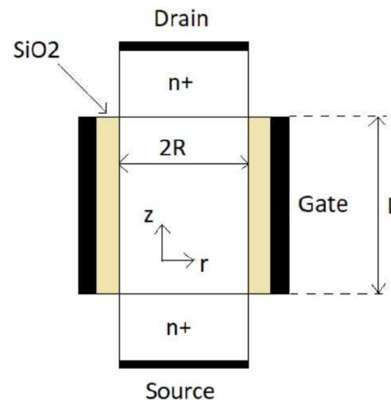


Fig. 3.4 2D Cut plane of the device

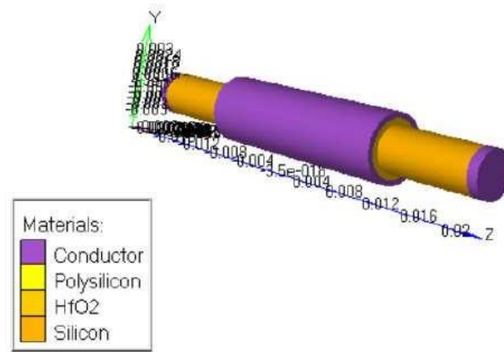


Fig. 3.5 Simulated Cylindrical Nanowire FET Structure

The designed device showed up some extra-ordinary results for the sub-threshold-slope of the device which make it suitable to be used for low-power circuits applications [Figure 3.4, Figure 3.5]. Few of the other important parameters that are kept in mind while designing the device are the short channel effects, threshold voltage and the ON current of the device.

As Mentioned above, we carried out work on three parameters of the device and we will be taking about them in detail from now. First of all we will see how the subthreshold slope of the device varies with channel radius, channel length and also the work function at gate terminal.

Subthreshold Slope: From the drain current equation we can observe that as when the gate voltage is reduce to threshold voltage, the drain current theoretically becomes zero but practically it doesn't happens and some amount of current is flowing in the device and this is the subthreshold conduction of the device. From the analysis of the device designed we concluded that if we increase the channel radius then the subthreshold slope increases and this is due to the reason that as the channel radius increases then channel formed is weakened which adds to the diffusion current in the sub-threshold regime [Figure 3.6, 3.7]. The channel radius for which the device has been analyzed are 2nm, 3nm and 5nm. And with the channel length increasing the subthreshold slope decreases because the carriers have to travel more distance therefore the current flowing decreases and the channel length taken into account are 20nm and 30nm respectively.

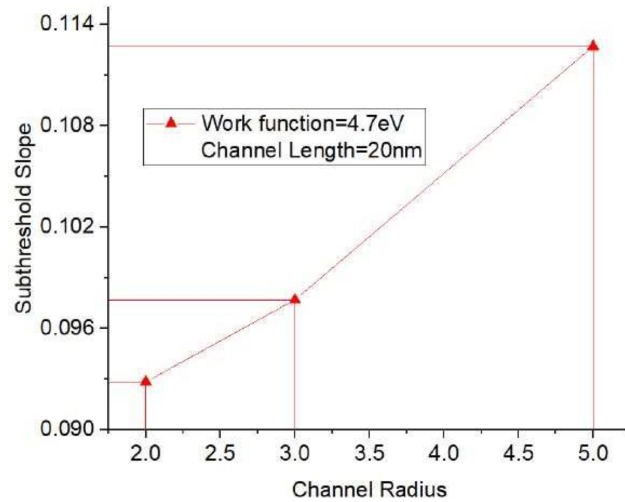


Fig. 3.6 Subthreshold slope with respect to channel radius

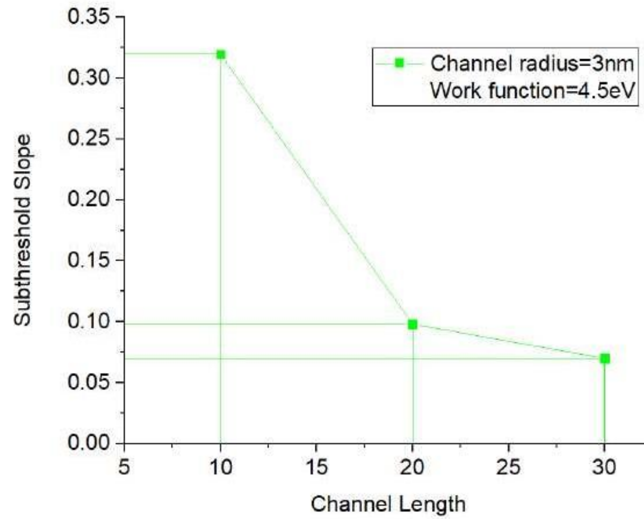


Fig. 3.7 Subthreshold slope with respect to the channel length

Next come the dependence of the threshold voltage on the channel radius, length and work function. As the channel radius is increased the barrier between source and channel is reduced and more carriers can be freely injected into the conducting channel. The work function upon which the analysishas been done are 4.5eV, 4.7eV and 4.9eV [Figure 3.8, 3.9].

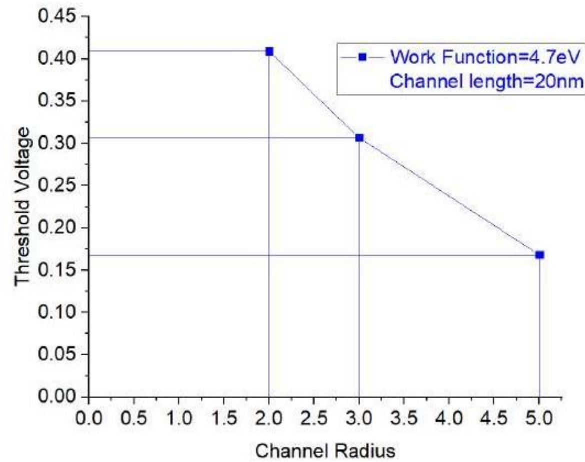


Fig. 3.8 Threshold voltage with respect to the channel radius

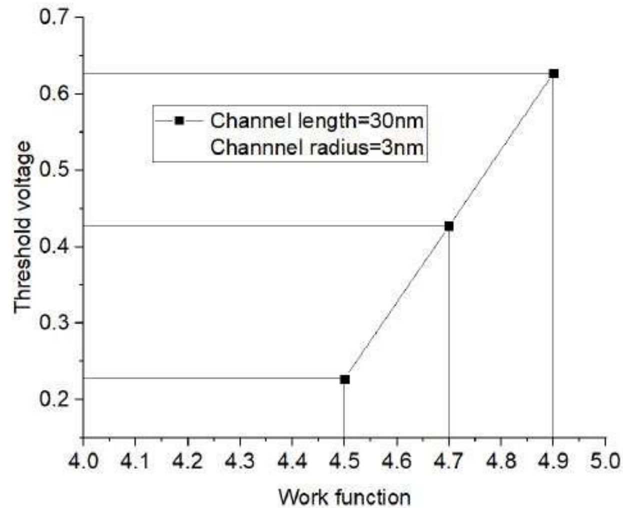


Fig. 3.9 Channel radius with respect to the wok function

Finally the most important characteristics of the device is the transfer characteristics that depicts how the input signal is transferred to the output. In this analysis we mainly focus on the ON current of the device and it can be seen that channel radius is directly proportional to the CNWFET ON current. While for the work function the graph goes the other way [Figure 3.10,3.11,3.12].

Whole of the above analysis has been performed on the n-type CNWFET and results procured have been picturized.

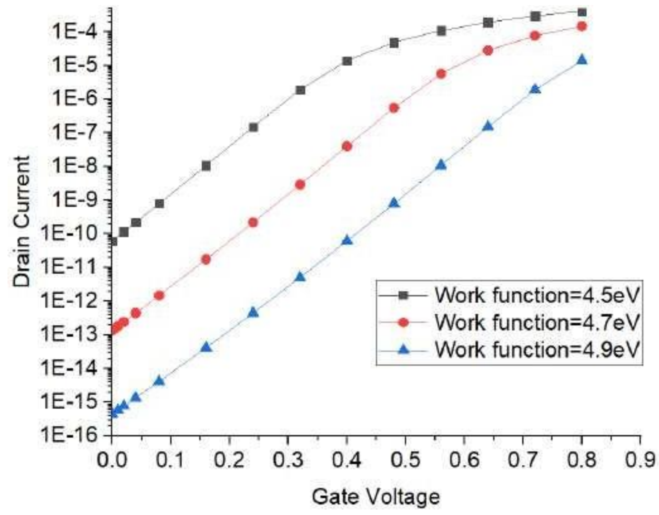


Fig. 3.10 Transfer characteristics of the device for varying work function

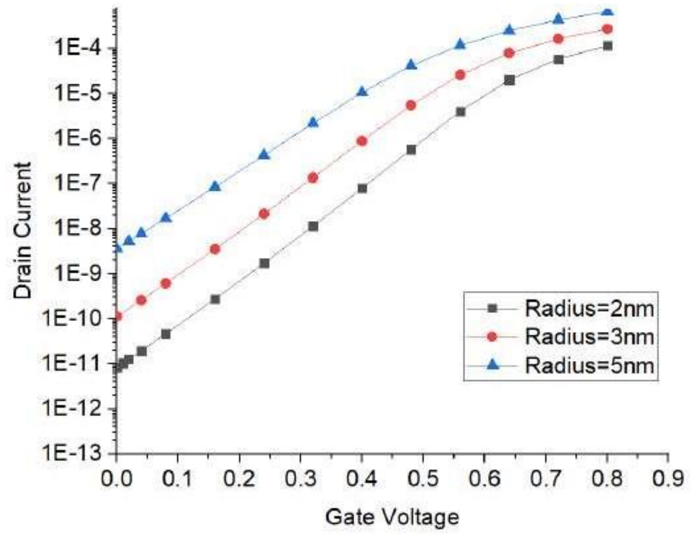


Fig. 3.11 Transfer characteristics of the device for varying channel radius

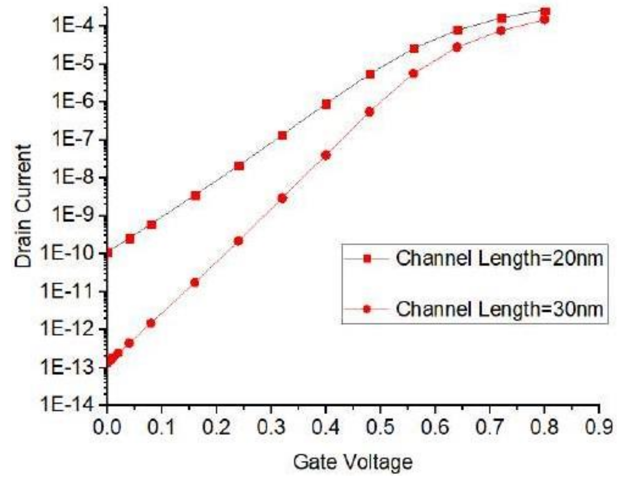


Fig. 3.12 Transfer characteristics of the device for varying channel length

CHAPTER-4
Tunnel Field Effect Transistors

In this chapter, we discuss the basic concepts of Tunnel FET which has a different mechanism for current flow and some of the other major differences from the conventional FETs. We also discuss the importance of certain device parameters for it to be an promising candidate as a successor of MOSFET technology.

4.1 Alternative to MOSFET

As the device size is reducing, there are short channel effect and thus the performance of the MOSFET also reduced also because of the second order effects. In return the leakage currents increase and so does the OFF current. Also we require high ON current to OFF current ratio for low power applications circuits. For the requirements to match with low powerapplications, different devices and their structure modification are being studied and explored for different applications [37]. Currently FinFET, CNWFET (Carbon Nanowire FET), High Electron Mobility Transistor(HEMT), CNTFET (Carbon Nanotube FET), TFET (Tunnel FET), DLFET (Doping Less FET), JLFET (Junction Less Field Effect Transistor).

4.2 Tunnel Field Effect Transistor (TFET)

All these experiments of finding a new device is just because of keeping the consumption of power within the acceptable limit of operating of the circuit. TFETs have a different mechanism for current transport due to which it exhibits some interesting electrical characteristics which will be described in further sections. In this chapter we describe the structure of TFET [15], the current transportation model, an approximate model for the tunneling current.

4.2.1. Structure

The structure of TFET is similar to that of reverse biased PIN diode structure. The structures for the n-type and also the p-type TFET have been shown below. One of the identifiable feature of TFET from other FETs is the type of the doping profile in the device in the source and the drain region. Both the regions have opposite type of doping while the normal FETs have the same type of doping in the regions.

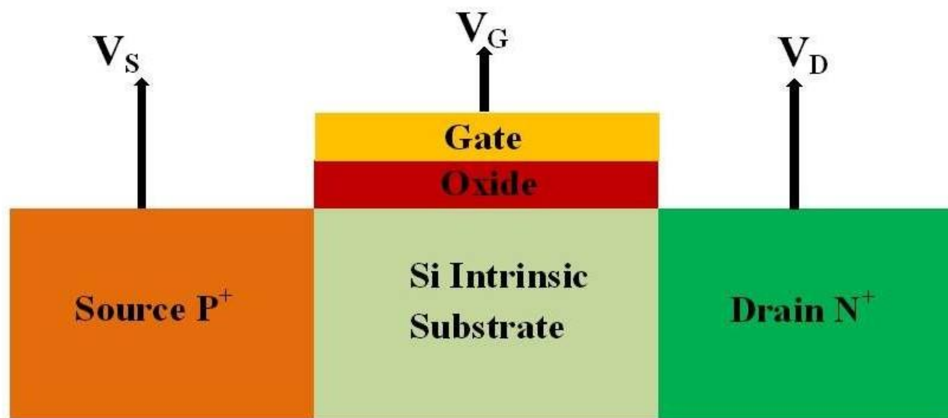


Fig. 4.1 Device structure of single gate conventional TFET [30]

The major benefit of TFET is impart a sharply vertical subthreshold slope as it has distinguishable current transport technique, Band to Band Tunnelling (BTBT).This also really low leakage current thus benefits of such kind of the TFET makes it more suitable option of the MOSFET. There is significant disadvantage of less ON current also of the device. The advantages of this device are favourable for the low power applications [15].

For n-type TFET, the doping profile of drain region is of n-type and that of source is p-type, similarly for p-type TFET the drain is doped with impurities of p-type and source with n-type and for both channel is lightly doped n-type or p-type accordingly. Gate terminal is separated from channel in a similar fashion to conventional MOSFET. The TFET is classified as n-type or the p-type on the basis if the dominant carriers in the channel, that is when the dominant carriers are electron in channel then it is n-type, otherwise it is p-type and also to note that the terminals are also named on basis of whether the carriers are entering or leaving the channel. If the carriers are entering the

channel then that region from which the carriers are coming is called source region and the other one is called drain into which the carriers are entering. The mechanism here used for transportation of carriers is Band to Band Tunnelling [26]. This structure of TFET suffers from one major drawback that is that the device has a low ON current. Many structure modifications have been proposed ameliorating the problems that have been observed in the simple TFET structure. Different structure implementation of TFET have their peculiarities, but the basis of operation remains the same for every TFET structure implementation. The electrical characteristics of device that are of important aspect of different structures vary with the various parameters of the device such as the body thickness, gate-dielectric thickness, dielectric constant, workfunction of the polysilicon and also the drain source doping concentration. The doping of the drain and source region is of main importance because the TFET shows the ambipolar nature which says that due to the symmetry in the device the carriers can also start to flow from the drain terminal for example for n-type TFET when we apply the positive voltage at the gate terminal, the electrons from the source tunnels into the channel region and further flow to drain terminal but when we put the negative bias at the gate terminal then also the carriers can flow from drain terminal into channel region resulting in the ambipolar nature of the device. Therefore we need a sharp doping profile of the source region and of that drain it should be lesser than the drain doping [30]. If we use a single gate TFET then we see that the ON current in very less and therefore we modify our structure to Double Gate TFET (DGTFET) which has more control over the drain current as it will have more control on the channel region and ideally we expect our current to double as compared to the single gate.

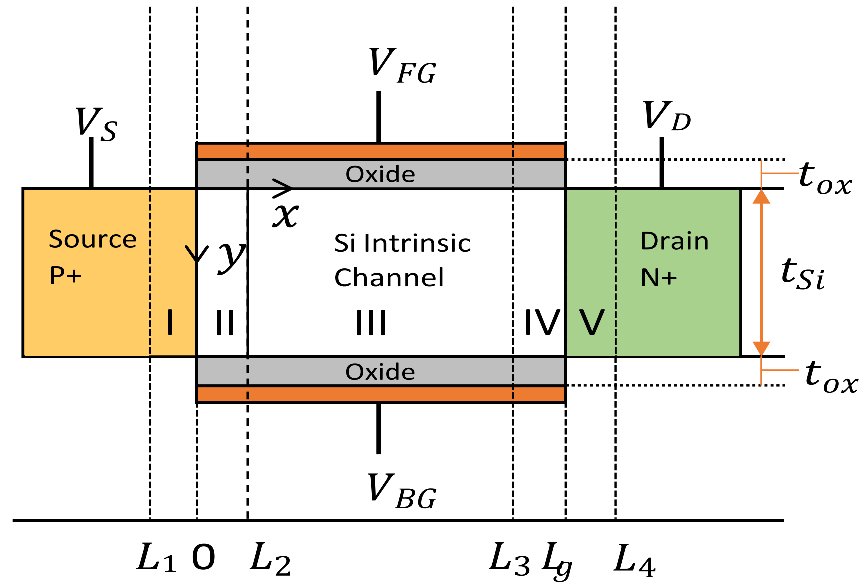


Fig. 4.2 Double gate TFET (traditional)

4.2.2. Operation

Operation meaning the mechanism behind the working of the device. The TFET uses band-2-Band Tunneling (BTBT) concept according to which the carriers tunnel from the source region into the channel region that is from the valence band of the source to the conduction band of channel for an n-type TFET when we apply the positive bias at the gate.

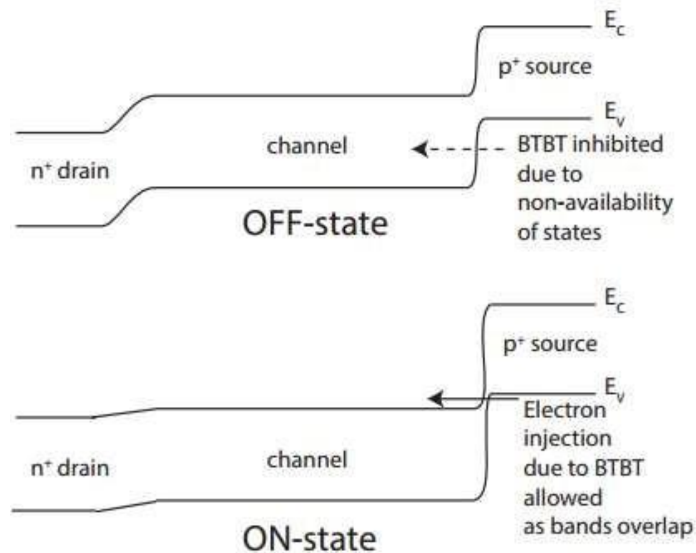


Fig. 4.3 Energy Band Structure of double gate conventional TFET

The above figure shows the band diagram for the n-type TFET in the ON and OFF state. In the OFF state the valence-band of the source lies below the conduction band of the channel region and therefore the Band to Band Tunnelling (BTBT) is inhibited and thus no conduction in the device takes place [26]. Due to this reason the OFF current of the TFET is very low, which is an important feature for a device to be used in the low power applications. As we increase the gate bias voltage, conduction band of channel is moved down and the valence band of source and conduction band aligns due to band bending and the TFET is now in the ON state because of the carrier flow due to the tunnelling of carriers from source to channel, device now conducts current. For n-type TFET the majority carriers flowing are the electrons and therefore named as n-type TFET, similarly for p-type TFET the majority carriers are holes and thus named as p-type TFET.

4.2.3. Transfer Characteristics

Transfer characteristics explains how the drain currentvaries with the change in the gate voltage, the transfer characteristics of TFET can be divided into three phases:

(i) OFF State: when the V_{GS} is less than the V_{OFF}, the current in the device is very low and the as explained from band diagrams the Band to Band Tunneling is inhibited. V_{OFF} is the minimum gate voltage at which currents starts to take off.

(ii) Subthreshold Region: when the $V_{OFF} < V_{GS} < V_T$, then the drain current increases rapidly and the V_T is threshold voltage of TFET.

(iii) Super Threshold region: when $V_{GS} > V_T$, then the drain current increases but not that as in the subthreshold region that is at a reduced rate.

4.2.4. Ambipolar Current

In a TFET, there are 2 tunneling junctions one is the between the source-channel and the other one is between the drain-channel. For the normal working of TFET we want tunneling of carrier to take place at the source channel tunneling junction and the

tunneling at the other junction is suppressed by high doping of source region and comparatively lesser doping of drain. Ambipolar behavior means that a TFET device shows both type of behavior with electrons as majority carrier in n-type TFET and holes as majority carrier for p-type TFET.

4.2.5. Advantages of TFET

(i) **Subthreshold Slope**: This explains that how much change in the gate voltage is required to change the drain current by a factor of 10 or by a decade. The subthreshold for a TFET can be calculated by the average subthreshold slope and is given by [31-33]:

$$SS_{AVG} = \frac{V_{TH} - V_{OFF}}{\log\ (I_{DS}(V_{TH}) - I_{DS}(V_{OFF}))}\ mV/decade \qquad (1.8)$$

Where V_{TH} is the device's threshold voltage of TFET and is determined using constant current methodology & V_{OFF} is deviation of the gate from source voltage during the OFF state while the I_{DS} (V_{TH}) is device's drain current at threshold voltage and $I_{DS}(V_{OFF})$ is the drain current at OFF state.

(ii) **Drain Current:** TFET has a lower ON current but the ration of the ON current and OFF current is very good for low power applications, and also for different structures proposed the ON current also improves significantly. TFET is also immune to the short channel effects and also the speed of device improves.

(iii) **DIBL:** This effect is explained as the ratio of the threshold voltage difference at 2 different drain voltage to the difference of drain bias voltage and is given by the equation: [33]

$$DIBL = \frac{V_{TH}(V_D{=}1V) - V_{TH}(V_D{=}0.1V)}{V_{DS}(V_D{=}1V) - V_{DS}(V_D{=}0.1V)} \qquad (1.9)$$

4.2.6. Limitations of TFET

Being the most promising candidate as a successor to the existing MOSFET technology, it has some limitations:

- In a conventional MOSFET, the drain and source are formed from the silicon semiconductor with help of ion implantation or diffusion process, here we cannot attain same doping concentration in different devices. This random dopant fluctuation is undesirable for TFET because in increases the OFF current, thus the ratio decreases.
- The abrupt junctions traditional TFETs are needed for the carrier tunneling from Valance Band (VB) to Conduction Band (CB). Since this is a high temperature phenomena thus it is not made for traditional TFET at functional temperatures [33]
- The conventional TFET requires high manufacturing cost. Because of the diffusion and ion-implantation techniques are being used in making of the TFETs [33].
- A conventional TFET device also requires costly thermal-Annealing techniques in manufacturing process.

CHAPTER-5

Device Design and Simulation Methodology

In this Chapter, we discuss the work methodology with the help of the block diagram and tool used to simulate and model the device and obtained the result. Silvaco Atlas TCAD tool is used to obtaining the result and the MAPLE software has been used for modeling the required parameters of the device..

5.1 Introduction

With the advancement in the technology, tools for designing and simulating the circuits are available nowadays and the availability of these Computer Aided Design tools have reduced the cost of preparing a circuit by an enormous amount. Various CAD tools are available for simulating the device such as the SILVACO, Sentaurus these tools can be used for designing any device with the finite dimensions. These tools basically work on the basis of finite element method. These tools provides device fabrication and its parameters assessment by physical mechanism not through the electrical processing. This provides the facility of virtual fabrication thereby reducing the cost of fabrication by a huge amount [35]. The modeling of the device plays a crucial role in the circuit designing as if we want to design the circuit using our own proposed device then firstly we need to model that device using some software for mathematical simulation then using the model file of the device it is further used in designing circuits like for example we can use in analog circuit design for which we have the EDA tool as Cadence Virtuoso. Through modeling of the device we develop the mathematical relations of the potential or the current whichever parameter we want of the device using boundary conditions and also the effects that the device and accordingly the equations for the device changes as we change the dimensions also. We develop model for surface potential of the device, drain current, carrier density for any device, and this thesis work include the modeling of the TFET device with scaled dimensions. The modeling of the device can be done using the mathematical tools but we preferably use MAPLE or MATLAB software for the same.

5.2 SILVACO TCAD Tool

It is an industry standard tool which can be used for simulation purposes and also for virtual fabrication. This tool also provides an accurate device characteristics of the proposed device which can further be used accordingly. The Silvaco tool provides two type of framework one is the ATHENA and the other one is ATLAS [35]. ATHENA is used as a process simulator in which one can perform the complete fabrication process virtually for a device and ATLAS is design simulator which provides all the parameter insight of the device like the electron-hole concentration, doping profile, surface potential, energy band diagram, electric field, mobility, conduction and valence bands, carrier density, these parameters can be obtained from the tool along with the characteristics of the device that are the output and transfer characteristics.

5.2.1 ATLAS Framework

Atlas is a tool designed for the physical realization of two dimensions as well as three-dimensional (2D, 3D) virtual prototype of semiconductor devices. Atlas tool is outlined in such a manner that it can be utilized with Virtual Wafer Fabrication (VWF) interactive Tools [34]. The VWF Interactive Tools involve the accompanying: Mask Views, Editor, Deck Build, and Tony Plot, Tony Plot 3D and Deceit, which is shown in Fig. 4.2 [35].

Fig. 5.1 Shortcuts of the tool involved in Silvaco ATLAS TCAD tool

Now we are analyze the designing of the any architecture in ATLAS Silvaco TCAD tool. The designing portion includes the three parts, first one is INPUT statements, another is MODELS, NUMERICAL Methods and ANALYSIS Portion and last one is OUTPUT files. INPUT statements includes the meshing, meshing is used for creating the node points for the calculation. There are two type of meshing includes in ATLAS TCAD tool one is normal mesh and other is quantum tunneling mesh (QT mesh), which

is defined in Tunnel Field effects Transistors where tunneling is occur. Region formation is used for defines the region that which portion is work as source, drain, channel or work as insulator. After defining the region, material selection and doping will be done and at last we provide the electrode. Designing of device and its characteristics will be understood by the Fig. 4.3 [35].

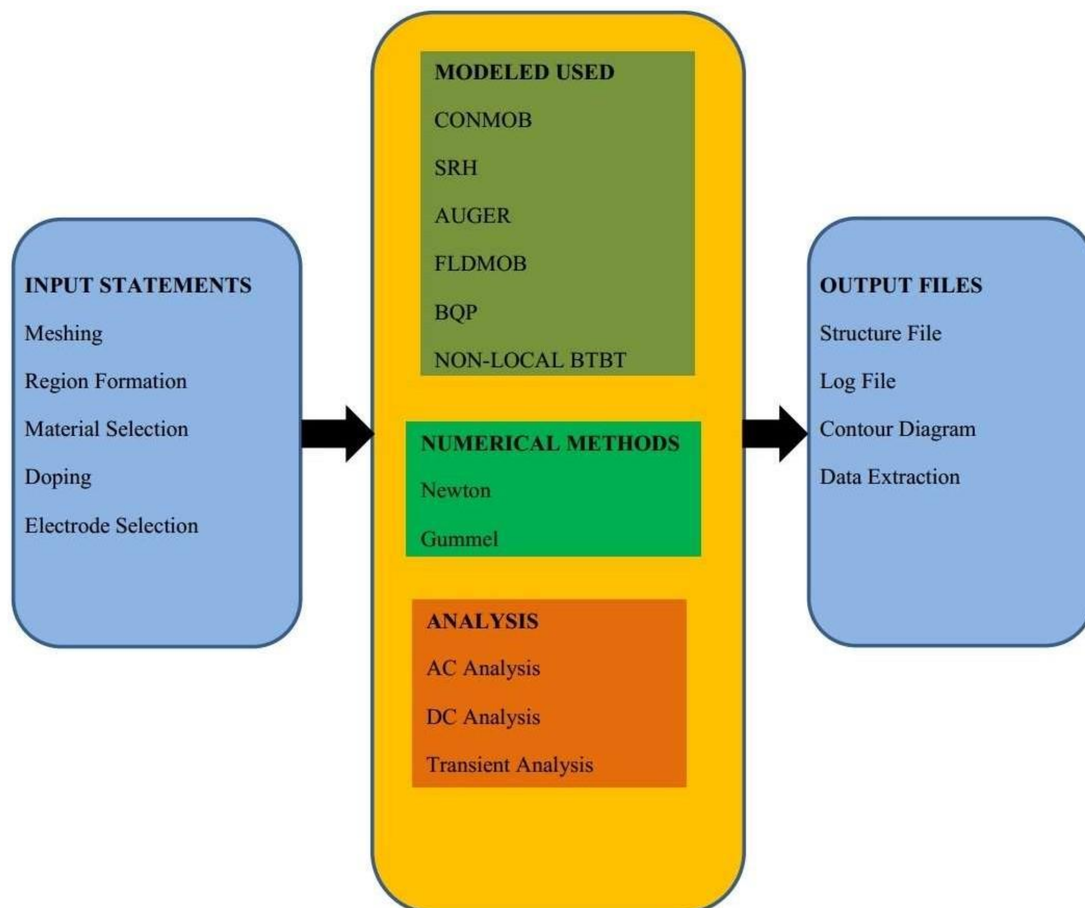


Fig. 5.2 Block diagram of design of device and its characterization.

There are different models used to obtain the device characterization, which are CONMOB, SRH, AUGER, FLDMOB, BQP and Non-Local Band to Band Tunneling (Non-Local BTBT). AC analysis, DC analysis and Transients analysis will be done in ATLAS TCAD tool to obtain the results. The results will be shows in Tony Plot tool. Output files have structure file and log file, structure shows the structure of the device and log file shows the characterization of the device like current capability [35].

5.2.2 Common Models.

5.2.2.1 Concentration-dependent Low-Field Mobility Model (CONMOB):

For this type, CONMOB is made use of as a section of MODELS statement. The current type tells about low field mobility of electrons and holes at 30 degree Celsius for Si and GaAs [35].

5.2.2.2 Shockley- Read Hall Recombination Model (SRH):

The SRH parameter is utilized as a part of the MODELS articulation for initiating this model. There are a couple client quantifiable parameters that utilized as a part of the MATERIAL proclamation, as TAUN0 and TAUP0 the electron and hole lifetime parameters. This type tells us about the recombination of electron as well as holes via Shockley- Read-Hall recombination within the device [35].

5.2.2.3 Fermi- Dirac Model (FERMI):

Fermi-Dirac measurements are used here. This model is used in those regions which are degenerately doped yet with decreased convergences of carriers [35]. To initiate this model FERMI is utilized as a part of the MODELS articulation.

5.2.2.4 Bohr Quantum Potential Model (BQP):

BQP model is utilized for the hydrodynamic models and Energy balance, where the semi-classical potential is changed by the quantum potential. The Bohr quantum potential model has two benefits over the density gradient model first it has better convergence and second it has better calibration to the Schrodinger-Poisson model [35]. The BQP.NGAMMA and BQP.NALPHA allows setting γ and α parameter for electrons respectively. Similarly BQP.PGAMMA and BQP.PALPHA allows setting γ and α value for holes respectively.

5.2.2.5 Non-Local Band to Band Tunneling Model (Non-Local BTBT):

Non-Local band to band tunneling model (Non-Local BTBT) is used for tunneling mechanism of the device. In TFETs current is due to tunneling phenomena so this model is used for obtaining the current. In tunneling region special type of meshing is required

which is known as quantum tunneling meshing (QT meshing) in both lateral and longitudinal direction [35].

5.2.3 Numerical Methods.

ATLAS uses the METHOD statement to define numerical methods [34]. To find the solution there are three distinct types of systems [35]

1. Gummel
2. Newton
3. Block

The Gummel and Newton iteration methods are used for 3D simulations, whereas Gummel, Newton, and Block are all used for 2D simulations [34]. The main technique finds solutions for one obscure variable while others being constant. This procedure will proceed until a steady solution is gotten. Not at all like the Gummel technique, newton technique solves and finds every one of the problem in the meantime [35]. Block technique is in the middle of newton and Gummel technique as it understands a couple of questions in the meantime.

5.2.4 Estimation of results:

The yield records of Atlas are of three unique types [35]. They are:

1. Run-Time Output:

The run time output is seen at the base of the Deck Build Window. Any errors happening amid this yield will be shown in the run-time window.

2. Log Files

Log files contain the characteristics curve of the device after simulation. These include the variation of Drain current (I_{DS}) w.r.t. variation in the gate voltage (V_{GS}). AC analysis is possible by mentioning the frequency [35].

3. Extraction of parameters in Deck build

To extract the various parameters of the device there is the need to mention EXTRACT statements in the deck build command line after the generation of log file i.e. threshold

voltage, subthreshold slop, I_{ON}/I_{OFF} ratio can be extracted by using the extract statement. Finally output file will generate containing the various parameter+

rs [35].

CHAPTER-6

An Approach to Analytical Modeling of TFET

6.1 INTRODUCTION

The fast rate of technology growth, the dimension reduction, other changing standards are critical segment of research. In such cases nanotechnology is gaining popularity [1,2]. Now the size reduction can't be done further rapidly. Thus novice techniques, devices, technologies are to be suggested for high frequency, reduced power consumption and improved area after scaling for good circuit operation [2]. The Tunnel FET don't consume large power besides that is doesn't let the short-channel consequences effect its functioning. This also has reduced sub-threshold swing [3]. The model that we talk about here is established from the 2D Poisson equation [4]. There current in this model is due to the BTBT, it is extremely intricate band bending at the junction. We shall also consider efficiency here. Inversion charges should also be considered here at higher voltages because there is the channel will be depleted. The model that we have proposed here has taken into consideration of the device's discrete bias, thus taking into consideration dual-modulation effects in TFET (an integral feature of TFET) [21-22].

We have used the Silvaco ATLAS 3D simulator to verify our model. We have considered an uniform doping profile in both the drain (having $1x10^{18}$ cm^{-3} concentration) as well as the source (having $1x10^{18}$ cm^{-3} concentration), while channel doping is 10^{15} cm^{-3}.

6.2 MODEL DEVELOPMENT

The device structure of TFET is shown in Fig. 1. The parameters for simulation and modeling have also been shown below:

TABLE 6.1: PARAMETERS

PARAMETERS	VALUES
Length of Channel	40nm
Length of Source	50nm
Length of Drain	50nm
Gate oxide material	HfO_2
Oxide thickness	2nm
Channel concentration	10^{15} cm^{-3}
Source concentration	$5x10^{20}$ cm^{-3}
Work function (Gate)	4.5eV
Drain Concentration	10^{18} cm^{-3}

For the inclusion of every effect in the nanoscale techniques and devices, we have made the usage of BQP (Bohr Quantum Potential) model in the ATLAS simulator due to the fact that the convergence properties and improved in this [3,5]. The Bohr Quantum Model has two positive reason to be considered (i) Convergence features (ii) We can calibrate it, compared to the results from Schrodinger and Poisson equations while we consider little flow of current.

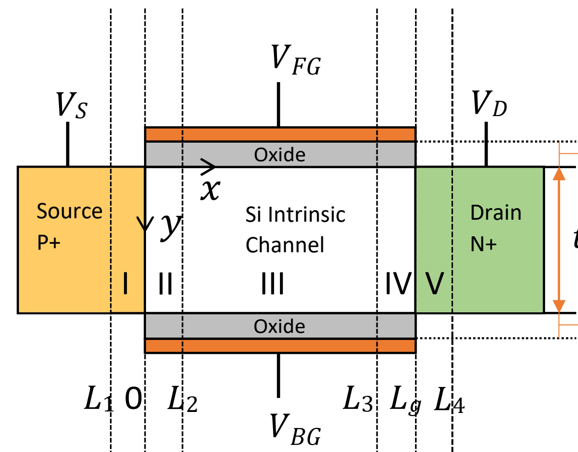


Fig.6.1. Modeled Double Gate TFET Structure

Here we discuss about the n-type DG-Tunnel Field Effect Transistors structure as shown in Fig.1.

Channel length is 40nm (<100nm), thus it comes under nanotechnology[6]. The regions I & II marked in Fig. 1. are the depletion regions in the source and the channel regimes respectively, which is also the tunneling region of the TFET device. Region III in the device is area of channel and during the modeling we also contemplate the charges in the channel. Similarly, IV and V regions represent the channel drain region. L_1, L_2, L_3, L_4 are the depletion lengths forthe device's Source-Channel-Drain regimes respectively. $L_2 > L_1$ due to the source density being more than drain density thus depletion width Li is less. Similarly, L3 >L4. Source doping density is $5x10^{20}cm^{-3}$ p-type impurities, Channel density is $10^{15}cm^{-3}$ and drain doping density $10^{18}cm^{-3}$ n-type impurities. TFET has two operating regions (i) in this gate bias regulates the channel surface potential and, (ii) drain terminal regulates the surface potential. Here dual modulation effect is applicable in TFET. This effect is a major property of TFETs. The transfer characteristics are shown in Fig. 3.

The Fig. 2 shows energy band diagrams of double gate TFET (scaled down) in ON and OFF state.

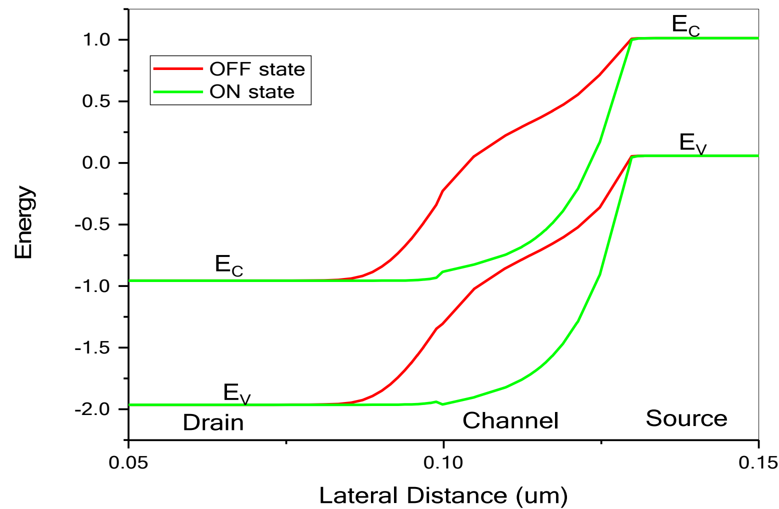


Fig. 6.2. Energy Band Diagram during the ON and OFF state.

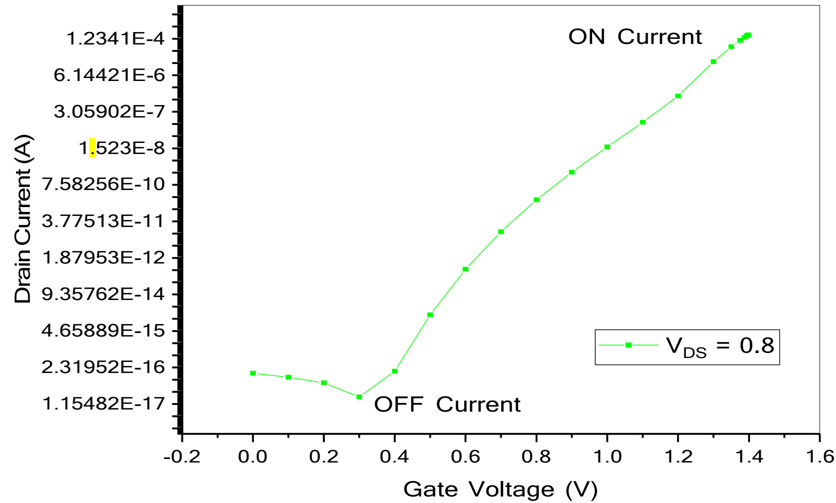


Fig. 6.3. Transfer Characteristics for OFF state and ON-state current.

6.2.1 GATE REGULATION IN CHANNEL SURFACE'S POTENTIAL

The dependence of potential along channel because of the gate terminal voltage can be seen in the results shown in Figure 4. The drain voltage is kept constant at 0.5V and the gate voltage is being varied from 0.55V to 0.8V. Initially i.e at small gate terminal voltage, potential in channel has linear relation with gate terminal voltage, as we can see in the graph, it increases linearly. Later on, when the voltage is high, channel potential saturates, shown in the graph because of inversion it becomes independent. This happens because the inversion charge screens the potential from the curve further in bias region, same as MOSFET in strong inversion mode.

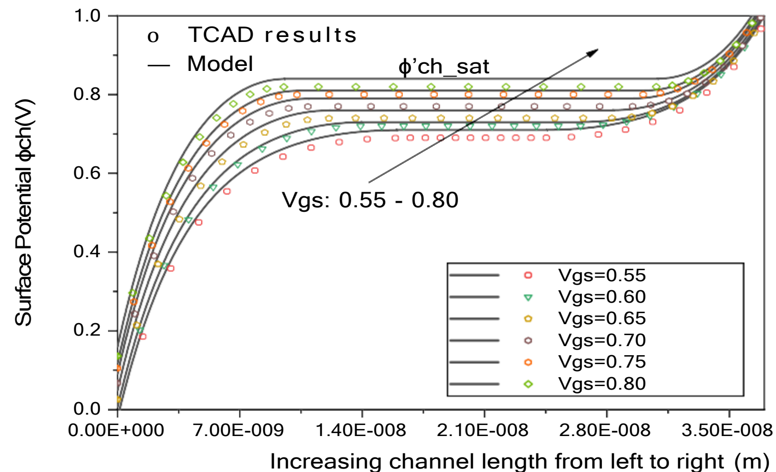


Fig. 6.4. Surface potential variation w.r.t gate biasing voltage. The gate biasing voltage at V_{ds}= 0.5 V comparing our model to TCAD simulation results .

The inversion charge density and channel doping at the $2\phi_{fp}$ potential, are equal as the channel doping, is also pretty low so as to optimally screen the gate modulation. In such case, the $\phi'_{chs} = \boldsymbol{\phi}$ which is $2\phi_{fp}$, inside MOSFET, where $\boldsymbol{\phi}$ is actually the potential required for enough inversion charges while considering the screening gate modulation

$$\phi = \left(\frac{KT}{q}\right) \ln \left(\frac{\text{NchNinv}}{n_i^2}\right) \quad (1)$$

Where n_i is the intrinsic carrier concentration, N_{ch} is doping concentration of channel and N_{inv} is the required inversion charge density for screening gate modulation.

6.2.2 CONTROLING THE CHANNEL SURFACE'S POTENTIAL WITH HELP OF DRAIN

The saturation of surface potential has relation with potential at the drain. on the drain biasing potential.

$$V_{tran} = \phi + \gamma\sqrt{V_{ds} + \phi} + V_{fb} + V_{ds} \qquad (2)$$

Where γ is body $\sqrt{2Esiq\mathrm{Nch/Cox}}$ factor and V_{FB} I s flatband voltage.

Fig. 6.5 shows the surface potential changing with drain bias voltage. Here the gate bias is taken to be 0.8 volts and voltage at drain end is varied from 0.45 volt to 0.7 volt. This, thus gives modulation effect at the drain.

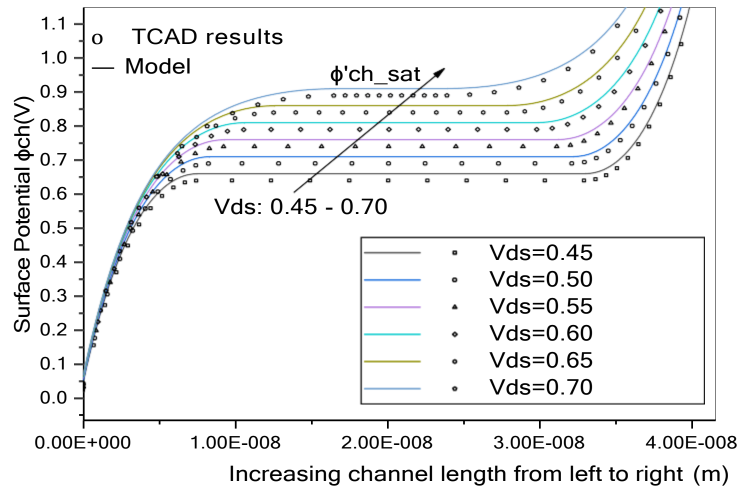


Fig. 6.5. Surface potential variation w.r.t drain biasing voltage. The drain biasing voltage at V_{gs}= 0.8 V comparing our model to TCAD simulation results .

Thus, we can infer from the above results that gate terminal voltage (V_{gs}) or drain terminal voltage (V_{ds}) can impact the surface potential according to the regions they are being operated at. Thus, this is how we come at the term called dual modulation effect as we switch between the 2 regions.

6.3 SURFACE POTENTIAL MODELLING REQUIREMENT

6.3.1 Gate Controlled Region Surface Potential

The surface potential for this particular regime is given as :

$$\phi'_{chs} = \left[\sqrt{\frac{\gamma^2}{4} - \frac{\gamma}{2} + V_{gs} - V_{fb}}\right]^2 \tag{4}$$

6.3.2 Surface Potential Under Drain Control Region

The equations for the finding out the surface potential equations in IV and V regimes functions similar to the region I and II. The only difference is the potential change thus modifying the depletion length. The equations are :

$$zs_4(x) = V_{g2} - (V_{g2} - \emptyset_{dg}) \cosh\left(\frac{(x - L_g + L_3)}{\omega_2}\right) \tag{5}$$

T

$$zs_5(x) = -\frac{qN_{deff}(x - L_1 - L_4)^2}{2\varepsilon_{si}} - \emptyset_{f1} (6)$$

$$N_{deff} = \frac{2\varepsilon_{si}}{q}\left(\frac{qN_d}{2\varepsilon_{si}} - \frac{C_{ox}V_{g2}}{\varepsilon_{si}t_{si}}\right) \tag{7}$$

$$\emptyset_{f1} = V_{th}\, ln\left(\frac{Nd}{Ni}\right) \tag{8}$$

For equations (5) and (6) $x = L_g$ since the same procedure is used for region I and II boundary condition. This criteria will vary accordingly as depletion length changes. Likewise L_3 and L_4 length of depletion region is computed.

6.3.3 Surface Potential for all Operating Regions

Generation rate of the carrier for BTBT procedure is relying on tunneling junction electric field [18-19]. The 2D poisson equation is shown below:

$$\frac{6^2\varphi_i(x,y)}{6x^2} + \frac{6^2\varphi_i(x,y)}{6y^2} = \frac{qNa}{s_{si}} \tag{9}$$

Here 'φ' is potential, ε_{si} is dielectric constant. We'll solve the equation with the parabolic equation, in the following way:

$$\varphi_i(x, y) = c_0(x) + c_1(x)y + c_2(x)y^2 \quad (10)$$

'y' sweeps from '0' to t_{si} while $\varphi_i(x, y)$ is device's surface potential that we need to find out. The also have constants that we need to figure it out first using the y- axis boundary condition.

The first thing is that the boundary condition is because of the potential at the junction of semiconductor and oxide, that happens to be the same as surface potential $\varphi_i(x)$, thus giving us:

$$\varphi_i(x, 0) = \varphi_i(x) \qquad (11)$$

The next thing is the other boundary arises from displacement vector which is continuous over the junction of oxide and semiconductor. The equation is shown as :

$$\frac{\partial \varphi_i(x,y)}{\partial y} = -\frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}}(V_{g1} - \varphi_i(x, 0)) \qquad (12)$$

Here, it is evaluated at y =0. The gate fringing electric field effect on surface potential and V_{g1} is given by the difference of gate to source potential and also the flatband voltage.

$$V_{g1} = V_{gs} - V_{fb} \qquad (13)$$

$$\frac{\partial \varphi_i(x,y)}{\partial y} = \frac{\varepsilon_{ox}}{\varepsilon_{si} t_{ox}}(V_{g1} - \varphi_i(x)) \qquad (14)$$

This is evaluated at $y = t_{si}$, here t_{si} is Si body thickness.

The third boundary conditions arises due to the electric field being null at $y = t_{si}/2$.

The boundary conditions mentioned above are useful to find the equation 6 constants. The constants are found as follows :

$$c_0(x) = \varphi_i(x) \qquad (15)$$

$$c_1(x) = -(V_{g1} - \varphi_i(x))\frac{C_{ox}}{\varepsilon_{si}} \qquad (16)$$

$$c_2(x) = (V_{g1} - \varphi_i(x))\frac{C_{ox}}{2\varepsilon_{si}t_{si}} \qquad (17)$$

This equation has taken into aspect the fringing capacitances (C_f), these are then split into inner (C_{inf}) and outer fringing capacitance (C_{outf}) [20]. This is mentioned in equation below:

$$\frac{d^2 zs_1(x)}{dx^2} - \frac{zs_1(x)}{\omega_1^2} = -\frac{(V_{g1} - \frac{qN_a t_{si}}{2C_f})}{\omega_1^2} \qquad (18)$$

$$\omega_1 = \sqrt{\frac{t_{si}\varepsilon_{si}}{2C_f}} \qquad (19)$$

where, $$C_f = C_{inf} + C_{outf} = \frac{\varepsilon_{ox}}{t_{ox}} \qquad (20)$$

The $zs_1(y)$ is basically the surface potential of region I while $zs_2(y)$ is the region II surface potential. The equations are:

$$C_{inf} = C_{inf,max}\exp\left[\left(\left(\frac{V_{g2} - \emptyset_{dg}/2}{3\emptyset_{dg}/2}\right)\right)^2\right] \qquad (21)$$

$$C_{inf,max} = \frac{2\varepsilon_{si}}{\pi(t_{si}/2)}\ln\left(1 + \frac{t_{si}}{2t_{ox}}\right) \qquad (22)$$

$$C_{outf} = \frac{2\varepsilon_{ox}}{\pi t_{ox}} \ln\left(1 + \frac{h_g}{t_{ox}}\right) \qquad (23)$$

The stack height h_g is derived with the use of conformal map procedure.

$$zs_1(-L_1) = -\emptyset_f \qquad (24)$$

$$\frac{\partial z_{\ 1}(x)}{\partial x} \approx 0 \qquad (25)$$

We are evaluating the above criteria at x $=-L_1$.

Thus we have a surface potential of region I and it is dependent on L_1

The surface potential is shown as follows:

$$zs_1(x) = -\frac{qN_{seff}(x+L_1)^2}{2\varepsilon_{si}} - \emptyset_f \qquad (26)$$

$$N_{seff} = \frac{2\varepsilon_{si}}{q}\left(\frac{qN_a}{2\varepsilon_{si}} - \frac{C_{ox}V_{g1}}{\varepsilon_{si}t_{si}}\right) \qquad (27)$$

$$\emptyset_f = V_{th}\, ln\left(\frac{Na}{Ni}\right) \qquad (28)$$

So same is for surface potential of region II as follows :

$$zs_2(x) = V_{g2} - (V_{g2} - \emptyset_{dg}) \cosh\left(\frac{(x-L_2)}{\omega_2}\right) \qquad (29)$$

$$\omega_2 = \sqrt{\frac{t_{si}\varepsilon_{si}}{2C_{ox}}} \qquad (30)$$

Equating region I & II equations keeping x =0 and find L_1 and L_2 .

$$zs_1(x) = zs_2(x) \equiv \varphi(0)(31)$$

And,

$$\frac{\partial zs_1(x)}{\partial x} = \frac{\partial z\ _2(x)}{\partial x} \qquad (32)$$

We have kept x = 0 in order to find the undetermined terms. Where $\varphi(0)$:

$$\varphi(0) = (V_{gs} - V_{fb1} + \emptyset) - \left((V_{gs} - V_{fb1} - \emptyset_{dg})^2 + 2(V_{gs} - V_{fb1})\emptyset + \emptyset^2\right)^{0.5} \qquad (33)$$

$$\emptyset = \frac{qN_{seff}\omega_2^2}{\varepsilon_{si}} \qquad (34)$$

Which gives,

$$L_1 = \sqrt{\frac{2\varepsilon_{si}(\varphi(0) - \emptyset_f)}{qN_{seff}}} \qquad (35)$$

$$L_2 = \omega \cosh^{-1}\left(\frac{V_{gs} - V_{fb1} - \varphi(0)}{V_{gs} - V_{fb}\ - \emptyset_{dg}}\right) \qquad (36)$$

At the end we'll derive the device channel, we call it X here. Since the transition from gate regulated to drain regulated region (dual modulation effect), is biasing it is not discrete function but a continuous one, The function X can be shown as follows :

$$X = \frac{1}{2}\left[V_{ds} + \varphi + \varphi_{chd} - \sqrt{(-V_{ds} - \varphi + \varphi_{chd})^2 + \alpha^2}\right] \tag{37}$$

$$\varphi_{chd} = \left(\sqrt{V_{gs} - V_{fb} + \frac{\gamma_1^2}{4}} - \frac{\gamma_1}{2}\right)^2 \tag{38}$$

$$\varphi = V_{th} ln\left(\frac{N_a N_i}{n_i^2}\right) \tag{39}$$

$$\gamma_1 = \frac{\sqrt{2\varepsilon_{si} q N_i}}{C_{ox}} \tag{40}$$

We are considering that α = 0.04 is a tiny factor [12]. Thus, we derive the channel surface potential of region II as follows :

$$\varphi_{chc} = V_{th} ln\left(\frac{1}{V_{th}}\left(\frac{1}{2}\left(-\frac{\gamma_1(X-2)}{2\left(\sqrt{X}+\gamma_1\right)^3} + \frac{X}{\left(\sqrt{X}+\gamma_1\right)^2}\right)\left(V_{gs} - V_{fb} - X\right)^2 + V_{th} + \frac{\sqrt{X}}{\sqrt{X}+\gamma_1}\left(V_{gs} - V_{fb} - X\right) + \right)\right) + X \tag{41}$$

3

In order to see how good and accurate our results of equation (26), (29) and (41) are, we shall see the contrast with help of the TCAD results by using Silvaco tool.

Fig. 6, shows that model and the simulated results are matching ideally after we examined the region I, II and III. We can see a linear relation of source and drain potential our model. As we can see so far from our derived device, gate and source potential is directly proportional to the device while drain saturates.

Thus, low power applications have devices that have high output resistance [13, 15].

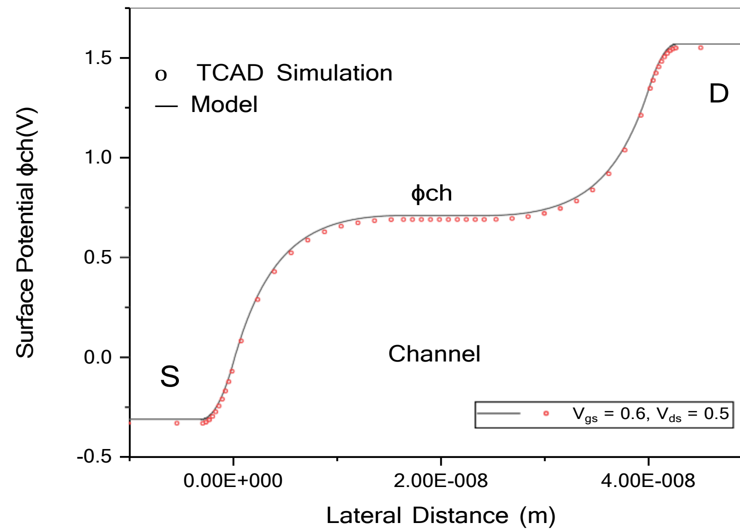


Fig. 6.6. The device surface potential w.r.t lateral distance, comparing our proposed model and TCAD results.

In order to boost the ON current, we have changed various parameters like the dielectric material. The surface potential is will change linearly as the tunneling current has a logarithmic dependency on dielectric constant [9]. Fig. 7 shows the result. The dielectric constant has inverse relation with the thickness while no effect on oxide thickness. But after a certain point, the leakage current will cause hot electron carriers.

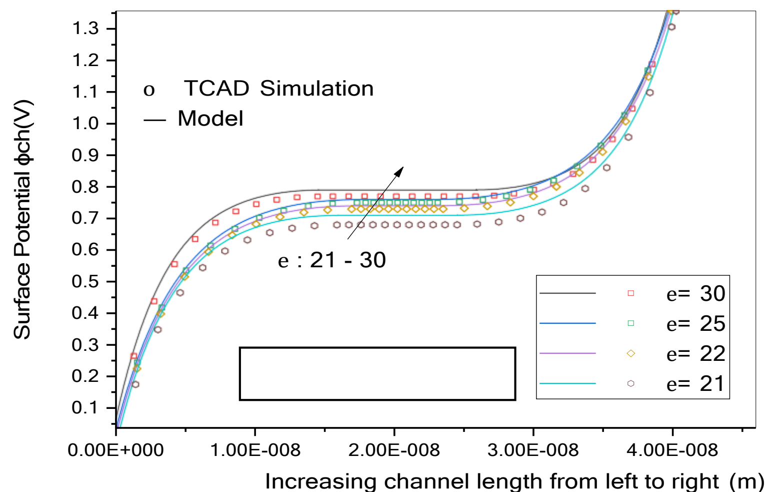


Fig. 6.7. Surface potential w.r.t dielectric constant and comparing our model to TCAD simulation results.

Fig. 8 shows that the workfunction of device grows from 4.1 eV to 4.4eV, hence the surface potential decreases.

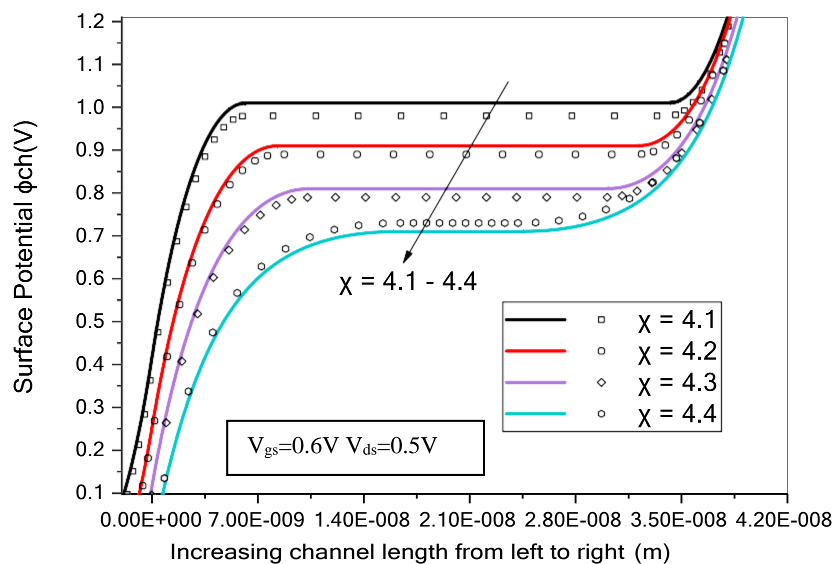


Fig. 6.8. Surface potential w.r.t gate work function and comparing our model to TCAD simulation results.

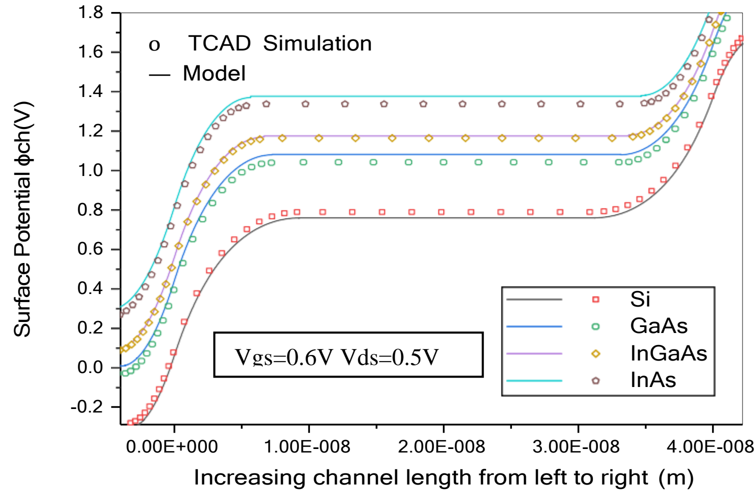


Fig. 6.9. Surface potential w.r.t materials used for and comparing our model to TCAD simulation results.

The research so far in the domain have suggested that the Silicon devices have low ON current [6-8]. In order to increase the tunneling current we will use the compound combination semiconductor and thus band gap is reduced of tunneling current, assuming that the OFF current wouldn't arise to leakage current. This is possible because of direct bandgap material used. The device that we are discussing here are GaAs, InAs and InGaAs devices and their simulations are analyzed for performance.

6.4 Drain Current Modeling of DG-TFET

The length the ele,,ctrons moved tunneling VB in the source region to CB in channel is denoted by d_t. The d_t is computed at the tunneling intersection using the equations for surface potential. The least tunneling distance is computed utilizing mathematical theories, using the peak tunneling probability.

The drain current is given by the following equation

$$I_D = \iint G_{BTBT}\, dxdy \qquad (42)$$

Correlation of the generation rate of tunneling is utilizing the Kane's model and is

given by equation (43).

$$G_{BTBT} = A \frac{|E^2|}{E_G^{0.5}} e^{(-B\frac{E_G^{1.5}}{|E|})} \quad (43)$$

E_G here is energy bandgap for Si, E is electric field, defined as
$|E| = (E_X + E_Y)^{0.5}$ and A & B factors are used in finding generation rate, also the values of B = 1.9 x 10^7 V/cm and A = 4 x 10^{14} $cm^{-3}s^{-1}$ [26]. The electric field is the differentiation of surface potential.

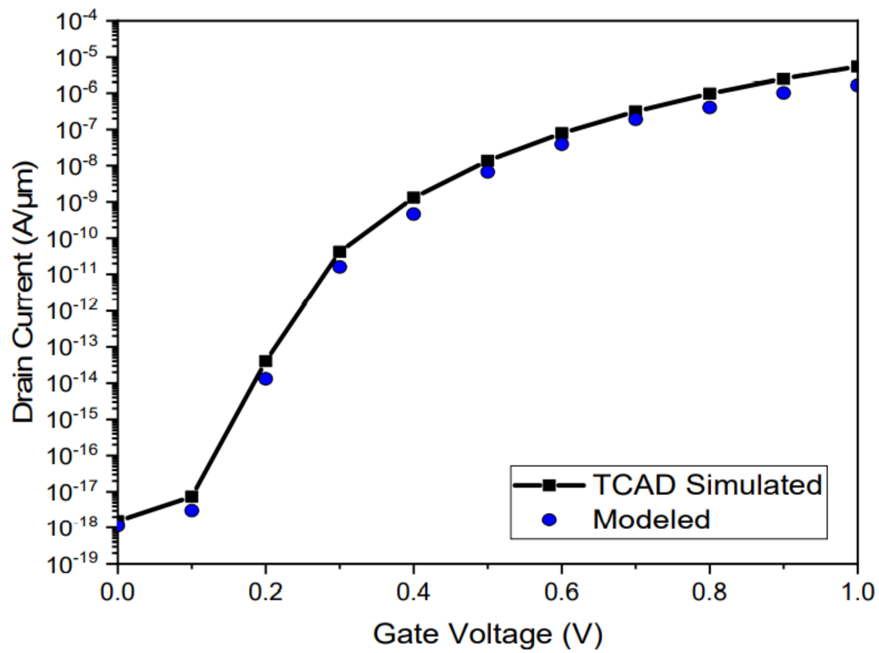


Fig. 6.10. Transfer characteristics of the DG_TFET device at a constant V_{ds}= 0.5 V with the comparison to TCAD simulation results with the modeled one.

The equation 42 is obtained by the results of Fig. 10, alongside the simulation of TCAD. These results were obtained while keeping V_{ds}=0.5V. The graph above also shows that the ON current is of the order of 10^{-5} A. This thus tells us that the TFET devices are giving good result of TFET, and can be used as substitute of MOSFET.

CHAPTER-7
Conclusion and Future Scope

In this chapter, Conclusion of Double Gate TFET structure modeled has been discussed and what work could be done in future to better optimize the results have been discussed. Here we also talk about the conclusions derived from the modeled device.

7.1 Conclusion of Analytical Model of Double Gate TFET (DG-TFET) and from the Analysis of the Cylindrical Nanowire FET

In the present work, the device that we have discussed here shows that it's matching well with TCAD simulation results. All the derived and modeled equations have been mentioned in the above section. The depletion lengths that we obtained at V_{gs}= 0.6V, V_{ds}= 0.5V are optimized. The L1(region I) and L2(region II) have been derived to be 2.942 nm and 8.011 nm. Also the L_3 (region IV) & L_4 (region V) are 8.67 nm and 3.38 nm. Since the doping profile of channel is lesser than the doping profile of drain as well as source, depletion width will be come out to be more. The OFF state current in this device is less than femto amperes (~10^{-16}). This is really useful feature for devices that are supposed to be used for low-power usage. The ON current in the range of milliamperes (~10^{-5}).

Also here, we have simulated the double gate TFET device architecture using TCAD ATLAS device simulator tool. By doing that we have also analyzed several features of theis structure.

The designed device structure of the Cylindrical Nanowire FET has been analyzed for the cardinal elements such as the subthreshold slope, threshold voltage and the transfer characteristics of the device. So these variation in these parameters has been analyzed on the structural parameters. Finally the results that we have obtained show us that the channel radius equal to 2nm and channel length equal to 20nm and work function of 4.9eV give most optimized subthreshold slope that is equal to 41.4 mv/decade and as we know this is equivalent to the standard FET's subthreshold slope.

7.2 Future Scope

In this research work of modeling a TFET structure and simulation of the DG-TFET has been carried. The performance of DG-TFET structure modeled can further extended for low power applications. Mentioned below are the points one can consider for research in future

- Development of low power memory circuits such as SRAM.
- Development of digital logic circuits.

We are in opinion that the results that we have procured can put to use in scientific research. Besides that, the device has a scope of usage in low power devices and techniques because nowadays minimizing the power consumption by device is the industry treand.

REFERENCES

1. J. W. Yang and J. G. Fossum , "On the feasibility of nanoscale triple-gate CMOS transistors," IEEE Trans. Electron Devices, Vol. 52, No. 3, pp. 1159-1164, 2005.
2. D. Nagy, G. Indalecio, A. J. Garcia-Loureiro, M. A. Elmessary, K. Kalna, N. Seoane, FinFET versus gate-all-around Nanowire FET: Performance, Scaling and Variability, IEEE Trans. Electron Devices, Vol. 6, pp. 332-340, 2018.
3. S. K. Sharma, B. Raj and M. Khosla, "A Gaussian approach for analytical subthreshold current model of cylindrical nanowire FET with quantum mechanical effects", Microelectronics Journal, Vol. 53, pp. 65-72, 2016.
4. P. Ghosh "An analytical drain current model for dual material engineered cylindrical/surrounded gate MOSFET", Microelectronics J., Vol. 43, pp. 17-24, 2012.
5. H. *Guang-Xi, W. Ling-Li, I. Ran, T. Ting-Ao, Q. Zhi-Jun, "Quantum-mechanical study on surrounding gate metal oxide semiconductor FET", Commun. Theor. Phys. Vol. 54 (4), pp. 763, 2010.*
6. H. Iwai, "Roadmap for 22 nm and beyond," Microelectronic Engineering, Vol. 86, pp.1520-1528, Jul-Sep 2009.
7. Y. Cui, Z. H. Zhong, D. L. Wang, W. U. Wang, and C. M. Lieber, "High performance silicon nanowire field effect transistors," *Nano Lett.*, Vol. 3, no. 2, pp. 149–152, Jan. 2003.
8. A. Singh, M. Khosla, B. Raj, "Circuit Compatible Model for Electrostatic Doped Schottky Barrier CNTFET," *Journal of Electronic Materials, Springer,* Vol. 45, Issue 12, pp 4825-4835, 2016
9. M.T. Bohr, "Nanotechnology goals and challenges for electronic applications", IEEE Trans. Nanotechnology. Vol. 1 (1), pp. 56-62, 2002.
10. Yadav, M., Bulusu, A. and Dasgupta, S. Two dimensional analytical modeling for asymmetric 3T and 4T double gate tunnel FET in sub-threshold region: Potential and electric field. *Microelectronics Journal*, *44*(12), pp.1251-1259, 2013.
11. Kim S, Choi WY. Improved compact model for double-gate tunnel field-effect transistors by the rigorous consideration of gate fringing field. Japanese Journal of Applied Physics;56(8):084301, 2017 Jul 6.

12. Zhang L, He J, Chan M. A compact model for double-gate tunneling field-effect-transistors and its implications on circuit behaviors. In2012 International Electron Devices Meeting, (pp. 6-8). IEEE, 2012 Dec 10.
13. Wu, C., Huang, R., Huang, Q., Wang, C., Wang, J. and Wang, Y.. An analytical surface potential model accounting for the dual-modulation effects in tunnel FETs. *IEEE Transactions on Electron Devices*, *61*(8), pp.2690-2696, 2014.
14. Lyu, Z., Lu, H., Zhang, Y., Zhang, Y., Lu, B., Cui, X. and Zhao, Y. A Fully Analytical Current Model for Tunnel Field-Effect Transistors Considering the Effects of Source Depletion and Channel Charges. *IEEE Transactions on Electron Devices*, *65*(11), pp.4988-4994, 2018.
15. I. A. Young, U. E. Avci, and D. H. Morris, “Tunneling field effect transistors: Device and circuit considerations for energy efficient logic opportunities,” in IEDM Tech. Dig., Washington, DC, USA, pp. 22.1.1–22.1.4, doi: 10.1109/IEDM.2015.7409755, Dec. 2015.
16. C. Shen, S. L. Ong, C. H. Heng, G. Samudra, and Y. C. Yeo, “A vari- ational approach to the two-dimensional nonlinear poisson’s equation for the modeling of tunneling transistors,” IEEE Electron Device Lett., vol. 29, no. 11, pp. 1252–1255, doi: 10.1109/LED.2008. 2005517, Nov. 2008.
17. W. G. Vandenberghe, A. S. Verhulst, G. Groeseneken, B. Soree, and W. Magnus, “Analytical model for a tunnel field-effect transistor,” in Proc. MELECON, pp. 923–928, doi: 10.1109/MEL- CON.2008.4618555, May 2008.
18. N. Cui et al., “A two-dimensional analytical model for tunnel field effect transistor and its applications,” Jpn. J. Appl. Phys., vol. 52, no. 4R, pp. 044303-1–044303-6, doi: 10.7567/JJAP.52.044303, 2013.
19. M. G. Bardon, H. P. Neves, R. Puers, and C. Van Hoof, “Pseudo- two-dimensional model for double-gate tunnel FETs considering the junctions depletion regions,” IEEE Trans. Electron Devices, vol. 57, no. 4, pp. 827–834, doi: 10.1109/TED.2010.2040661, , Apr. 2010.
20. M. Gholizadeh and S. E. Hosseini, “A 2-D analytical model for double- gate tunnel FETs,” IEEE Trans. Electron Devices, vol. 61, no. 5, pp. 1494–1500, doi: 10.1109/TED.2014.2313037, May 2014.

21. Y. Yang, X. Tong, L.-T. Yang, P. Guo, L. Fan, and Y. Yeo, "Tunneling field-effect transistor: Capacitance components and modeling," IEEE Electron Device Lett., vol. 31, no. 7, pp. 752–754, Jul. 2010.

22. S. Kumar and B. Raj, "*Compact channel potential analytical Modeling of DG-TFET based on Evanescent–mode Approach*," Journal of Computational Electronics, Springer Vol. 14, No. 2, pp.820-827, July 2015.

23 S. Sharma, B. Raj, Mamta Khosla, "A Gaussian Approach for Analytical Subthreshold Current Model of Cylindrical Nanowire FET with Quantum Mechanical Effects, Microelectronics Journal, Elsevier, Vol. 53, PP. 65-72, April 2016.

24 A. Singh, Dinesh Kumar Saini, Dinesh Agarwal, Sajal Aggarwal, Mamta Khosla, B. Raj, "*Modeling and Simulation of Carbon Nanotube Field Effect Transistor and its Circuit Application ,*" Journal of Semiconductors (JoS), IOP Science, Vol.37, PP. 074001-6, July 2016.

25 B. G. Streetman and S. Banerjee, "Solid state electronic devices" (Vol. 4). Englewood Cliffs, 1995, NJ: Prentice Hall.

26 Short channel effects of MOSFET NPTEL [Online Content]

27 K. Boucart and A. M. Ionescu, "Double-Gate Tunnel FET with High-k Gate Dielectric", IEEE transactions on electron devices, 2007 54(7), pp.1725-1733.

28 S. Saurabh and M. J. Kumar, "Novel attributes of a dual material gate nanoscale tunnel field-effect transistor", IEEE transactions on Electron Devices, 2011, 58(2), pp.404-410.

29 S. Anand and R. K. Sarin "Analog and RF performance of doping-less tunnel FETs with $Si_{0.55}Ge_{0.45}$ Source". Journal of Computational Electronics, 2016, 15(3), pp.850-856.

30 S. Anand, S. I. Amin and R. K. Sarin, "Performance analysis of charge plasma based dual electrode tunnel FET", Journal of Semiconductors, 2016, 37(5), p.054003.

31 V. Prabhat and A. K. Dutta "Analytical surface potential and drain current models of dual-metal-gate double-gate tunnel-FETs", IEEE Transactions on Electron Devices, 63(5), 2016, pp.2190-2196.
32 I. SILVACO, "ATLAS User's Manual", 2011 Santa Clara, CA, Ver, 5
33 B. Razavi, "Design of Analog CMOS Circuits", 2000: McGraw Hill.
34 D. Garg and B. Raj "Design and Analysis of Cylindrical Nanowire FET for Low Power Circuit Power Applications", IE Conference 2019.