ACTIVE FILTER IMPLEMENTATION USING CURRENT MODE BLOCK

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VLSI DESIGN & EMBEDDED SYSTEM

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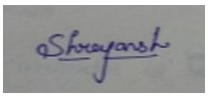
I, **SHREYANSH**, Roll No. **2K19/VLS/17** student of M.Tech. VLSI Design & Embedded Systems, hereby declare that the project Dissertation titled "**Active Filter Implementation Using Current Mode Block**" which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.



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CERTIFICATE

I hereby certify that the Project Dissertation titled "**Active Filter Implementation Using Current Mode Block**" which is submitted by **Shreyansh**, Roll No **2K19/VLS/17** to the Department Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology/Bachelor of Technology, is a record of the project work carried out by the students under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

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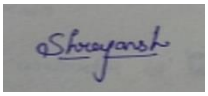

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ABSTRACT

One of the famous and fundamental building block that may be utilised in a variety of ways to perform various analog processing function is a Current Conveyor abbreviated as CC. Till date various researches has been made in this regards and various functionality like amplifier, filters etc can be achieved by using these devices. A Current Conveyor is a minimum three terminal devices but not limited to it. CC's can be classified according to their generation. The current conveyor (CC) concept was first released in 1968 this is called as first generation of current conveyor and after two years in 1970 second generation has been developed and later on third generation of current conveyor is also developed, we will discuss about this in greater details in upcoming chapters..

Various other analog processing block also uses current conveyor as these primary block. The CFOA (current feedback opamp) & CCII (second-generation current conveyor) are considered adaptable building blocks in analog current mode signal processing. One of the famous novel five-port analog building block that combine these two CFOA & CCII is OFCC (operational floating conveyor) and this may be used for a variety of applications. It combines the functions of a current feedback op-amp & a current conveyor in one package.

This thesis shows the implementation of OFCC block as universal current mode device which can be used in realization of various functions where earlier an operational amplifier were used. Further it also shows the implementation of active biquad filter using new OFCC Block in a) TAM (Trans Admittance Mode) b) VM (Voltage mode) c) TIM (Trans Impedance Mode) d) CM (Current Mode). The OFCC block and amplifier is implemented in CMOS 90nm and 130nm technology node and later filter has been implemented on CMOS 130nm technology node by using software Symica DE. For low voltage applications and to minimize power consumption it uses single supply of 0.4 V. Various plots for OFCC block, amplifier and filter are also present in this thesis.

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LIST of ABBREVIATIONS

IC - Integrated Circuit

CC - Current Conveyors

CCI - First Generation Current Conveyor

CCII - Second Generation Current Conveyor

CCIII - Third Generation Current Conveyor

OFCC - Operational Floating Current Conveyor

CFOA - Current Feedback Operational Amplifier

CFA - Current Feedback Amplifier

OTA - Operational Trans Conductance Amplifier

CCCCTAs - Current Controlled Current Conveyor Trans-Conductance Amplifiers

VM - Voltage Mode

CM - Current Mode

TIM - Transimpedence Mode

TAM - Trnasadmittance Mod

CHAPTER 1: - INTRODUCTION

1.1 IC Design Introduction

Electronics engineering is divided in to various subfields, IC design known as Integrated circuit design is one of its subfield that encompasses the various techniques for logic and circuit design used in the manufacturing of ICs. Integrated circuits are made up of microelectronic components embedded on a monolithic semiconductor with electrical network. Digital and Analog integrated circuit design are the two different categories of IC design.

Implementation of Digital ASICs, Microprocessors, Memory and FPGA are all made via digital IC design. Digital IC Design give majority of its emphasis on circuit optimization, maximizing the uses of allotted chip area by incorporating maximum number of device, logical correctness of digital block, device placement on chip to ensure that timing and clock signals are transmitted effectively. On the other hand, Analog IC design consists of Power & Radio Frequency integrated circuits design. Current Conveyor, Oscillators, active filter, opamp linear regulators and phase looked loops are part of analog IC design. Analog design focuses on the device physics of semiconductor devices (example like how transistor is going to behave in its different region of operation), resistance, gain of active devices, power dissipation, matching condition etc. As compared to analog ICs, digital ICs uses smaller area active devices and are usually more dense in circuitry also in some cases digital ICs are technology independent.

Back in 90s analog ICs were developed using hand calculations, before the introduction of high performance computers and electronics design automation tools. Low-complexity circuits, such as op-amps, were used in these ICs, which typically had no more than 10 transistors and few connections. In the 1970s when computers became accessible, computer programmes were built to simulate circuit designs with better precision than could be achieved by human computation. SPICE was the first circuit simulator for analogue integrated circuits which stands for Simulation Program with Integrated Circuits Emphasis. Analog ASICs (application-specific integrated circuits) may now be designed using computerised circuit modelling tools, which allows for more IC design complexity than can be achieved with hand calculations. Computerized circuit simulators, such as LTSpicce, Cadence Virtuoso, Symica, and others, allow for early detection of design flaws before a real device is built. Furthermore, this circuit simulator can include more complex device models and circuit analyses that would be too time consuming to do by hand.

The usage of electronic design automation tools in the designing of ICs has increased due to the complexity of present IC design, scaling of transistors and market demand to generate designs at a faster rate than before. In a nutshell, electronic design automation is the process of designing, testing, and verifying the instructions that the IC will execute.

1.1.1 A Brief Introduction to Design Steps

The steps in a IC design cycle are as follows [33]: -

(a) System Specification

In this customer gives its reequipments like what kind of functionality he wants from chip to to the task. This stpes involves different levels of discussions between customer and chip maker

(b) Architectural or System-Level Design

(c) Logic Design

RTL based logic designs happens in this phase which requires any hardware descriptive language to make the different digital block for desired Ips.

(d) Circuit Design

(e) Physical Design

From this point onwards everything comes under backend part which involves place & route, floor planning, parasitic device extraction etc.

(f) Physical Verification and Signoff

STA (Static Timing Analysis), CTS (Clock Tree Synthesis) comes under this section

(g) Wafer Fabrication

GDS formed in above steps is now send to the foundry for wafer manufacturing.

(h) Packaging

(i) Chip Development

Fig.1.1 shows the flowchart for above described IC design process flow: -

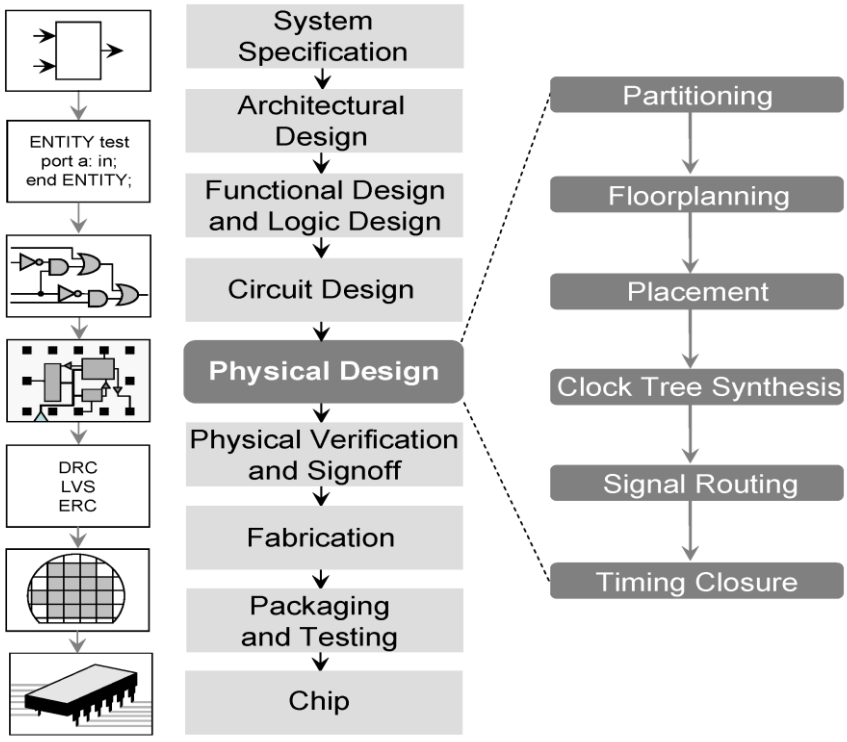


Fig1.1 Flow chart of integrated circuit design [32]

1.2 Introduction to General Signal Processing

In real word majority of the signals are present in analog form like speech, voice etc. to process these analog signal we require analog processing block. Modern chip comprises of both analog along with digital processing circuits. Voltage and current are the two important parameter in which are required by analog circuits. Despite the fact that many of the signals handled by analog circuits are really currents in their original state, analog and digital designers began to think and calculate primarily in terms of voltages over time. Fig.1.2 shows the block diagram for general signal processing system. By inspecting the analog routes of the signal processing system, the sensors output, which were generally charges or currents, the I/V converter converts these output signal to voltages before being processed by the voltage signal processing circuits shown in Fig 1.3. On the output side also similar situation occurs, where the D/A converter's output current was first altered to voltage, then post processed the voltage signal before being converted to current and used to power a physical transducer. [1].

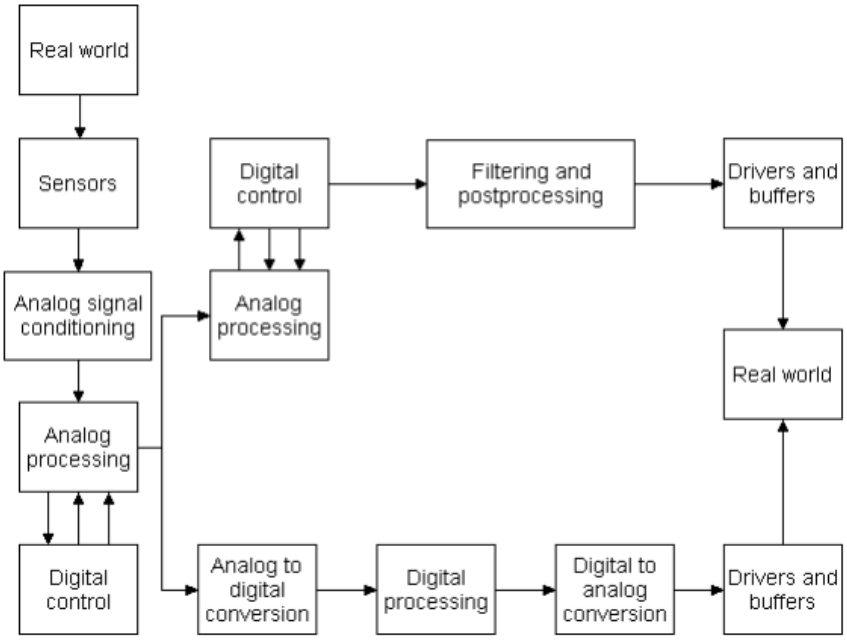


Fig.1.2 Block diagram of signal processing system [1]

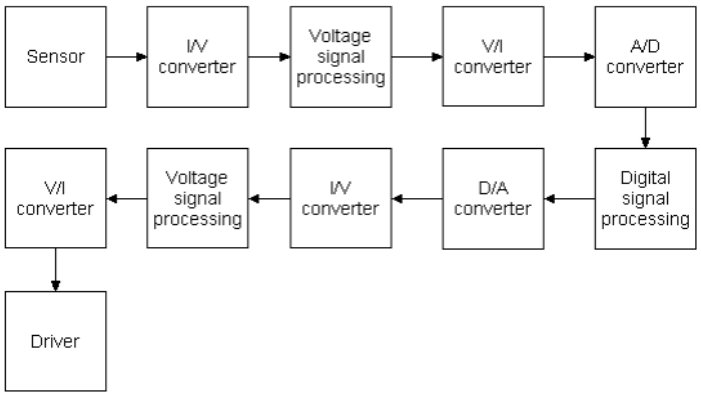


Fig.1.3 Voltage Signal Processing System [1]

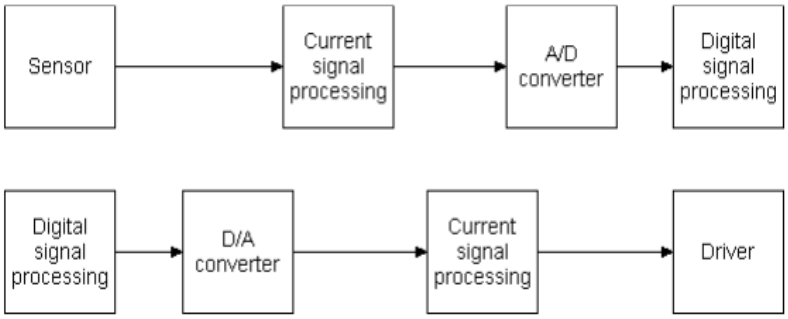


Fig.1.4 Current signal processing system [1]

The better way to implement is to use that analog circuitry which processes the signals directly in form of currents as shown in Figure 1.4. By that type of implementation, we no longer require the V/I and I/V converters.

The lack of high-performance current processing circuits was the explanation behind why current signal processing circuits could not begin itself till today [1]. Op-amps, comparators, etc. these are some well-known building blocks for voltage processing circuits, but on the other hand, in designing of basic current processing blocks or circuits less attention has been dedicated.

One of the important current processing block is Current Conveyor. It's a versatile construction block that includes voltage and current sub-blocks. [Smith and Sedra], they are one of the first persons who introduced the current conveyors in the late 1960s and early 1970s.

In their early development, the performance of conveyors was severely constrained due to the limitations of existing technologies. Now many analog designers have been interested in the current conveyor or current processing system as technology has advanced. Thanks to recent advancements current conveyors have evolved into highly valuable analogue electronics building blocks, with their primary use in high frequency, high speed circuits for both current as well voltage signal processing [2]. Except for some specific varieties, a conveyor is usually a three port device that operates largely in the current mode but also in various other modes too. The general block diagram of a current conveyor consists of two main components these are voltage follower VF and a current CF follower as shown in Fig 1.5.

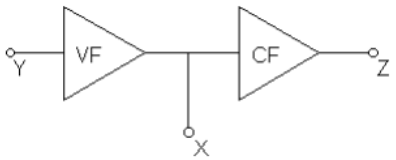


Fig.1.5 Current Conveyor [2]

1.3 AIM of Dissertation

The AIM of this thesis is to implement the different amplifier configuration and also implementation of filter in different modes by using new current mode block which is OFCC stands for Operational Floating Current Conveyor. Functioning of block and amplifier is implemented on CMOS 90nm and also on 130nm technology node and filter is implemented on CMOS 130nm technology node. This new OFCC block has been already designed in []. This thesis uses this new block in designing of amplifier as well as filter then differentiator followed by integrator.

1.4 Organization

After giving brief introduction to IC Design and also brief introduction on signal processing block the rest of the content of thesis is as follows: -

In Chapter 2 we will see the various filter implementation proposed by different authors and we will try to find out their advantaged and short-coming of different filter configuration.

Chapter 3 gives insight on Current conveyors, starting from introduction to current conveyors then their division, how are they different from one another and so on and so forth.

Chapter 4 tells about the OFCC block, its implementation and simulation results are also present here.

Chapter 5 consists of amplifier configuration and their simulation results.

Chapter 6 has simulation results for filter in different modes like a) TAM (Trans Admittance Mode) b) VM (Voltage mode) c) TIM (Trans Impedance Mode) d) CM (Current Mode).

In Chapter 7 we will see the implementation of differentiator and integrator using the OFCC Block.

Chapter 8 consist of conclusion and future scope of thesis.

CHAPTER 2: - LITERATURE REVIEW

The current conveyor (CC) is one of the most fundamental building blocks of current mode analog signal processing. Before the development of current conveyor, since the late 1940s the most extensively used concept is of opamps, making it difficult for any other similar concept to gain widespread acceptance [3]. In recent decades, current-mode design techniques have gotten a lot of attention because they have a broader gain independent bandwidth than their voltage equivalent. Current-mode circuits also have greater precision, linearity and dynamic range than traditional circuits [11,12].

Current conveyors can be used in designing of the filters or other electronics devices due to above mentioned advantages. As a result of scaling of technology node and increasing demands of portable electronics product, which requires low voltage devices and low power circuitry or blocks in analog processing systems which encourages the use of current conveyors [34], more about current conveyors will be discussed in chapter 3. Modern days analog IC design is so connected together that it requires both current mode and voltage mode of operation and sometimes this mode of operation of circuit are connected together in a single silicon chip. These types of need can be addressed by using Transimpedance mode (TIM) & Transadmittance mode (TAM) filter structures as an interface, allowing for distortion-free interaction. As the advancements in analog design increased, enough literature can be found which can shows the various implementations of filter design by using the different mode like TIM, TAM, VM, CM, but there is less available literature which can implement all possible filter by using the same circuit in different modes. The advantages of having this type of circuits can be found in terms of area and power requirement.

After the introduction of CCCII (Current Controlled Conveyor) author [M. T. Abuelma'atti] [35] proposed the mixed mode biquad filter based on current controlled second generation of current conveyor with dual output. The filter proposed by author uses 4 blocks of CCCII and two capacitors as shown in Fig.2.1, both the capacitors value are put at 0.5µF, from this circuit author is able to obtain the lowpass, high pass, bandpass and notch filter responses. By the same author, the filter circuit presented by [Abuelma'atti et al] [24] consists of 7 CCII+ blocks along with 7 CCII+ active block it also uses 8 resistors and 2grounded capacitors as shown in Fig.2.2, it's a mixed mode current conveyor based filter which can realize all the filter responses and they are LP, HP, AP, BP and the responses of the filter can have independent electronic tunability. As, the filter proposed by [24, 35] may able to realize all the filter responses but it uses quite a number of active and passive components which can take up large silicon area and as well as large power consumption and dissipation which is avoided in modern days IC design.

[S. Maheshwari et al] [25] proposed a low voltage (with power supply voltage of $\pm$1 V) mixed mode filter based upon 3 active block these blocks are CCCCTAs (Current Controlled Current Conveyor Trans-Conductance Amplifiers) and 2 capacitors as shown in Fig.2.3 which makes it as the biquad filter and the proposed circuit is electronically tuneable. Circuit uses a supply voltage of $\pm$ 1 V. The filter proposed by author, can implement LP, BP, HP responses in these four possible modes which are TIM, TAM, VM, CM. This filter uses BJT transistors in implementation of CCCCTAs block but as per industry standard CMOS based implementation

is used in modern IC design due to various advantages of CMOS based implementation. As per author [25] above proposed filter can be used in modern microelectronics IC design.

[Jiun-Wei HORNG] [26] proposed a circuit which can implement the high order universal filter in only two modes and these modes are transimpedance mode and current mode. Without component matching condition, from this circuit author is able to realize LP, HP, BP, AP and NP filter response in both mentioned modes. Proposed circuit is based upon CCII and MOCCII. For second order universal filter block, it uses 3 resistors, 2 capacitors as their passive elements and for active block it uses 2 CCII, 1 MOCCII which has two outputs. MOCCII block uses the supply voltage of $\pm$ 1.25 V with a biasing voltage of -0.65V. The proposed 2nd order active filter implemented by author is shown in Fig.2.4. As compared to other available literatures filter proposed is able to realize BP, HP, NP, AP from same structure in both current as well as voltage mode. Proposed filter in not realized in Voltage and Trans admittance mode. HSPICE simulations and CMOS implementation of MOCCII block and proposed filter at 180nm technology node from TSMC can be found in [26].

As per [Neeta Pandey et al] [27] majority of the work done on filter by using current controlled conveyors is either in current or voltage mode. As per circuit designers mixed mode circuit design have wide variety of application in IC design and this type of circuit can be easily adapted by the IC designers. [27] proposed a mixed mode active filter which uses 2 capacitors and 2 resistors as their passive elements and 2 active blocks, based on CCCIIs or MOCCCII for multiple output. Circuit uses the bias voltage of $\pm$ 2.5 V. Proposed circuit is able to realize all the filter responses and these responses are LP, BP, HP, NP and AP all the 4 mode which are VM, CM, TIM, TAM that's why proposed circuit is mixed mode active filter, block diagram of proposed circuit is shown in Fig.2.5.

CFOA (Current Feedback Opamp) are also the choice for the active filter design. Comlinear Corporation [13] was the first to create the current feedback amplifier (CFA) based on the CCII+. The initial CFA circuit was a BJT. Any closed-loop design in which the error signal utilised for feedback is in the form of a current is known as current feedback. Before [V. K. Singh et al] [28] there is no CFOA based active universal biquad filter has been realised which can give all the generic filter response in all the 4 modes and those modes are VM, CM, TAM, TIM. [V. K. Singh et al] [28] proposed a circuit which can implement the second order active universal filter in all 4 modes. From this circuit author is able to realize LP, HP, BP, AP and NP filter response in all mentioned modes. Proposed circuit uses 9 resistors and 2 capacitors as their passive elements and filter implementation is completed by using 4 CFOA block as active element. CFOA circuit uses the bias voltage of $\pm$ 12 V. Proposed active biquad filter block is shown on Fig.2.6. Simulation results and hardware implementation can be found in [28].

2.1 Block Diagram Represenation of Various Filter which are Discussed Above

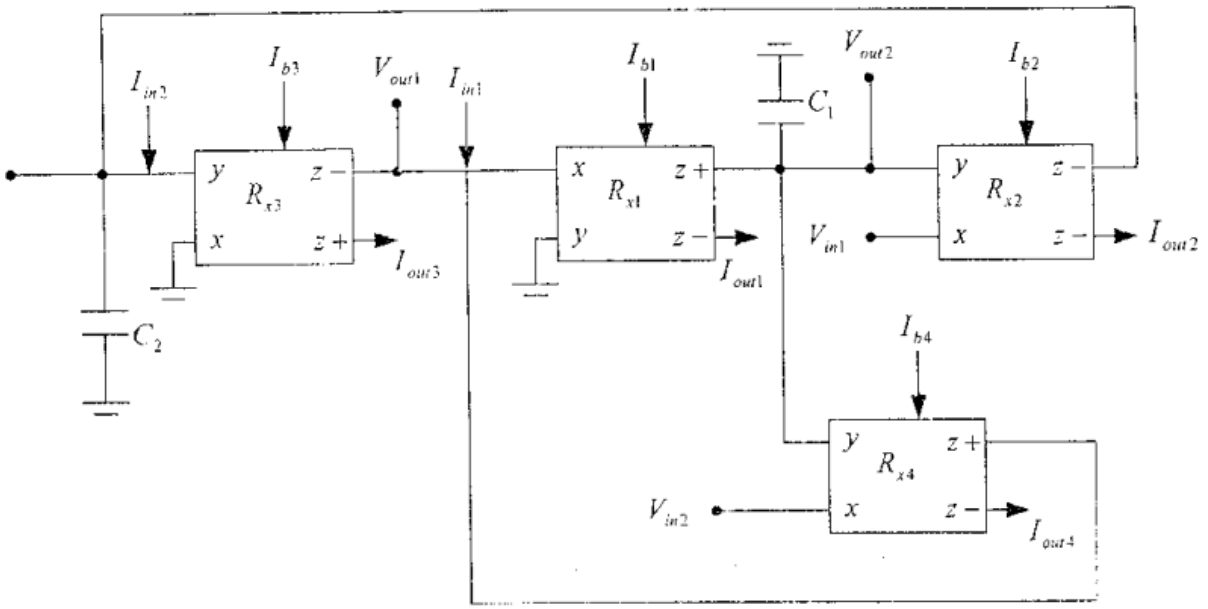


Fig.2.1 Block Diagram of Filter Circuit proposed by [35]

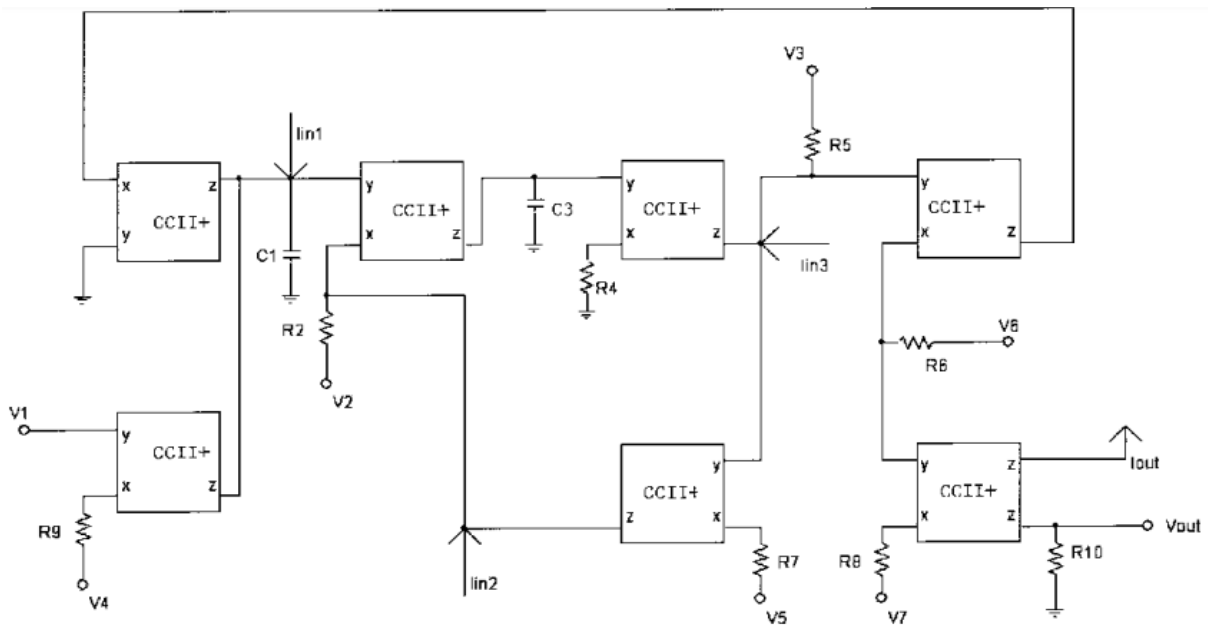


Fig.2.2 Block Diagram of Filter Circuit proposed by [24]

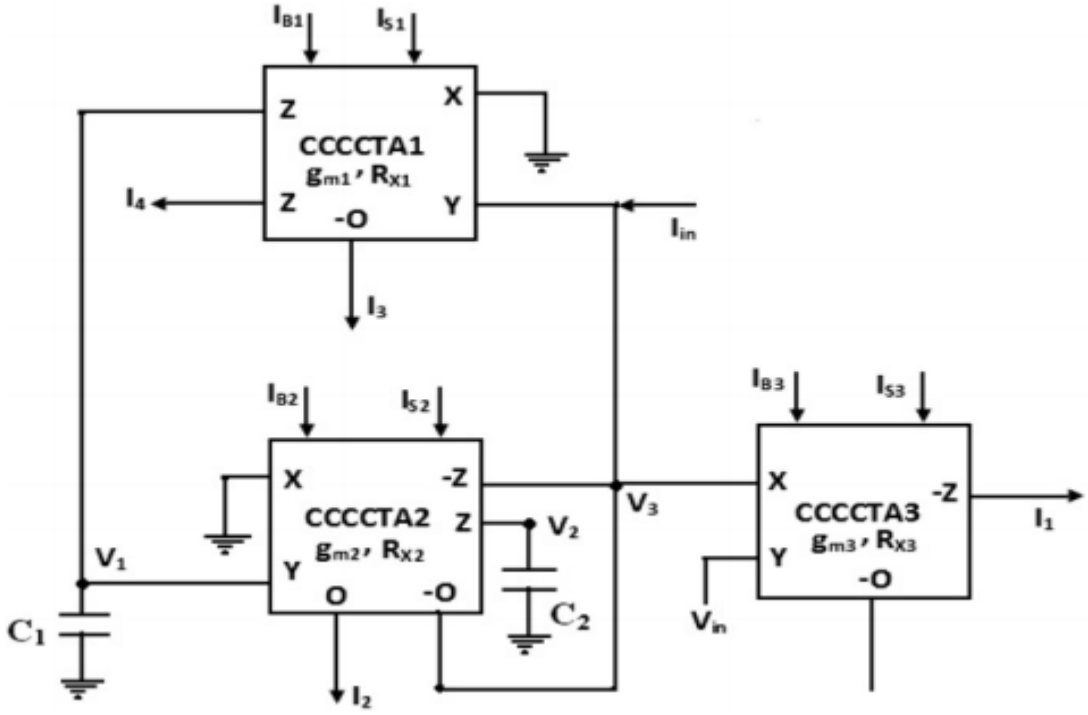


Fig.2.3 Block Diagram of Filter Circuit proposed by [25]

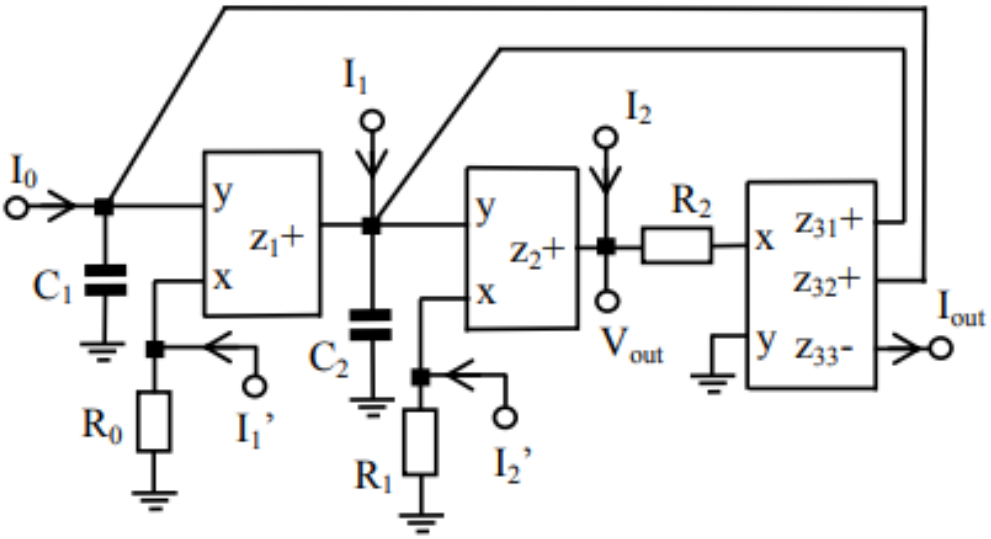


Fig.2.4 Block Diagram of Filter Circuit proposed by [26]

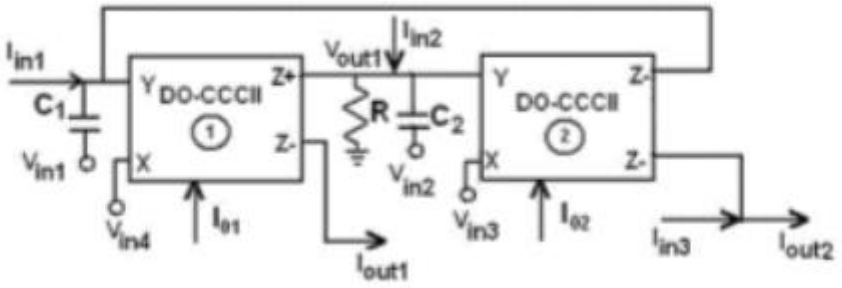


Fig.2.5 Block Diagram of Flter Circuit proposed by [27]

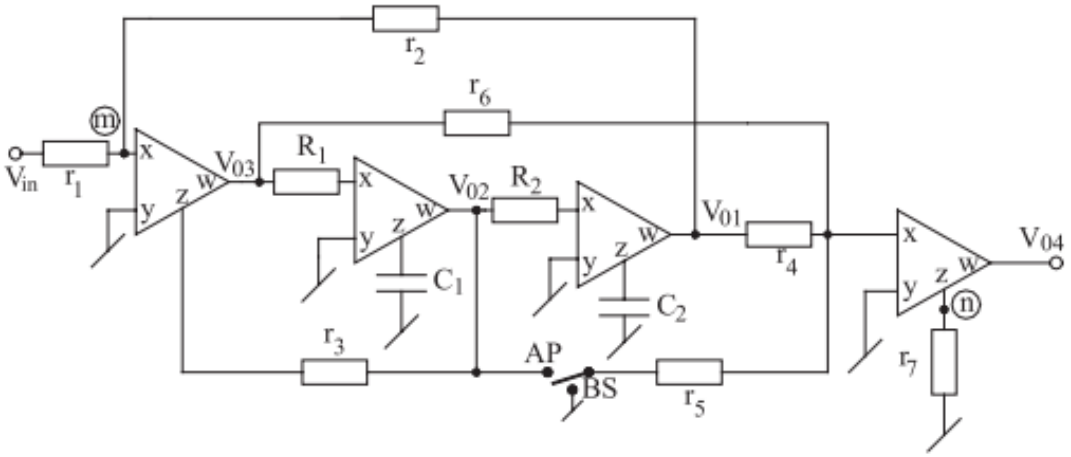


Fig.2.6 Block Diagram of Filter Circuit proposed by [28]

Table 2.1 summarize the above discussions about the various analog filters that are being proposed by different author.

Table 2.1 Comparison of different analog filters

Reference	Various Mode with their Filter Response				Name & No. of Active Block	No. of resistors & capacitors	
	VM	CM	TAM	TIM		R	C
[35]	LP, BP, HP, NP	LP, BP, HP, NP	LP, BP, HP, NP	LP, BP, HP, NP	CCCII & 4	0	2
[24]	All Five	All Five	All Five	All Five	CCII & 7	8	2
[25]	LP, BP, HP	LP, BP, HP	LP, BP, HP	LP, BP, HP	CCCCTA & 3	0	2
[26]	Not Realized	All Five	Not Realized	All Five	CCII & 2, MOCCII & 1	3	2
[27]	All Five	All Five	All Five	All Five	CCCII & 2	2	2
[28]	All Five	All Five	All Five	All Five	CFOA & 4	9	2
Thesis	LP, HP, NP	LP	LP, HP	LP	OFCC & 2	5	2

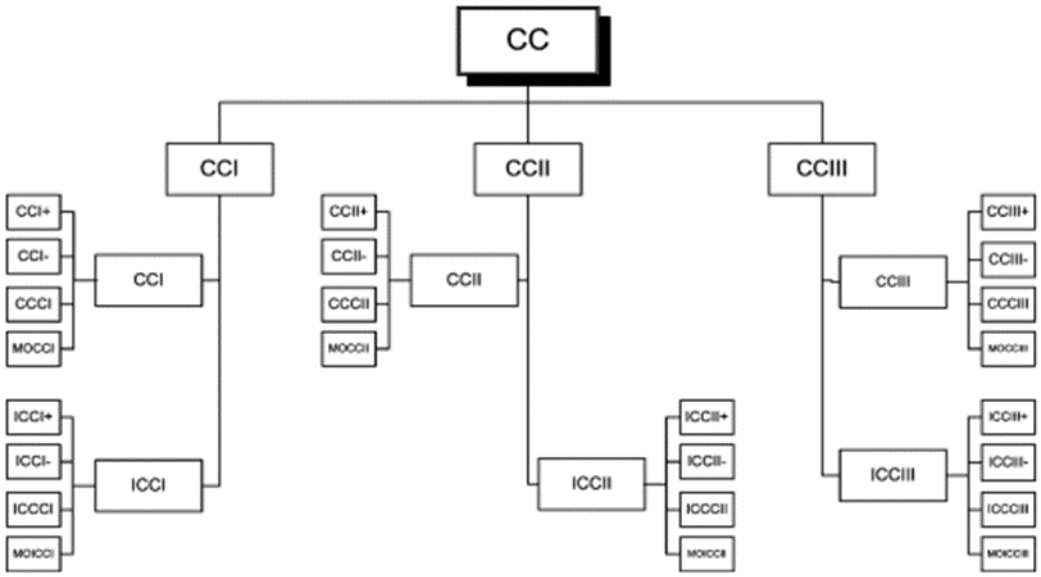
2.2 Summary

In this chapter we have seen and studied the various implementation of active biquad filters by using different active blocks. We have also studied the various merits and demerits of these block. Above studies also shows that how the current mode device can be used in implementation of filter due to their various advantages as compared to voltage mode counterpart. We have also seen the various literatures which can shows the various implementations of filter design by using the different mode like TIM, TAM, VM, CM. Filter circuits proposed by [35, 24, 28] consists of more than 4 active block the main disadvantages of sing these filter blocks in modem days IC design as industry as technology is scaling we try to incorporate more no of blocks in same semiconductor chip, these filter will requires large area to implement these functionality in modern chip. In above study we have also seen that the power supply required by all of these active filter blocks is greater than 1 V which reduces their chances to get included in modern IC design because in low power design we require those blocks which requires less power consumption and less supply voltage. This thesis tries to implement filter design in all four modes by using the low power and low supply voltage block of OFCC which is already designed in [11] so that this circuit can be used in low voltage applications. The OFCC (Operational Floating Current Conveyor) combines CCII± (second generation current conveyor) and CFOA (current feedback amplifier) [11] and which makes it flexible analog block. The other parts of this thesis through some more light on this.

CHAPTER 3: - CURRENT CONVEYORS

The current conveyor (CC) is one among the most popular fundamental building blocks of analog current mode signal processing. In 1968 the concept of CC (current conveyors) is developed by Smith & Sedra and later on in 1970 it evolved in to second generation of current conveyor. Before the development of CCs, since in the late 1940s the utmost extensively used concept is of opamps, making it difficult for any other similar concept to gain widespread acceptance [3]. When current conveyor came into existence it can be observed that it helps in simplifying the circuit design similar to normal opamp. The CC provides an alternate method of abstracting difficult circuit operations, making it easier to create novel and effective implementations. Furthermore, CC is a miscellaneous mode general building block that may be used to replace traditional opamps in voltage mode applications. The rest of the chapter describes the classification of the current conveyors based on their generation which are First, Second and Third generation of current conveyor, also each generation is further divided in to current controlled, multiple output, direct, inverse, positive type and negative type. For better understanding, Fig.3.1shows the tree representation of current conveyor.

Fig.3.1 Different types of CCs [4]



3.1 History of Current Conveyor (First Current Conveyor)

A. Sedra was working on his Master's thesis research at the University of Toronto in 1966, under the guidance of Prof. K. C. Smith. His first assignment was to create a voltage-controlled waveform generator, but he ended up creating a new circuit in which the control variable was current rather than voltage. The circuit designed by him is shown in Fig.3.2, in which Q1 transistor is the current source transistor and its emitter is coupled to a control voltage Vc through a resistor R. The emitter of diode compensating transistor Q2, is connected to ground. Current mirror is formed by the combination of transistor Q5, Q4 and Q3. transistor Q1 and Q2 also forms the combination of a current mirror due which the current flowing in Q2 is equal to that of flowing through Q1, and according to the property of current mirror if they have equal

current then their Base-Emitter voltage (V_{EB} in case of pnp transistor) should also have to be equal, as their base is shorted to each other due to which their base voltage should be equal which leads to, voltage at emitter of Q1 transistor equals to zero. Result of this is that the current flowing through Q1 is equals to Vc/R, neglecting the base current the same current flows through the transistor Q3, and transistor Q3 and Q5 form the current mirror which leads to same Vc/R currents flows through collector of Q5. From above discussion it's pretty evident that the circuit provide the precise voltage to current converter. As, the transistor Q3, Q4, Q5 are having same property but they are discrete transistor so in order to match their properties and implement good current mirror characteristics emitter resistance is added to the transistor in order to achieve same emitter base voltage(V_{EB}) for the npn transistor.

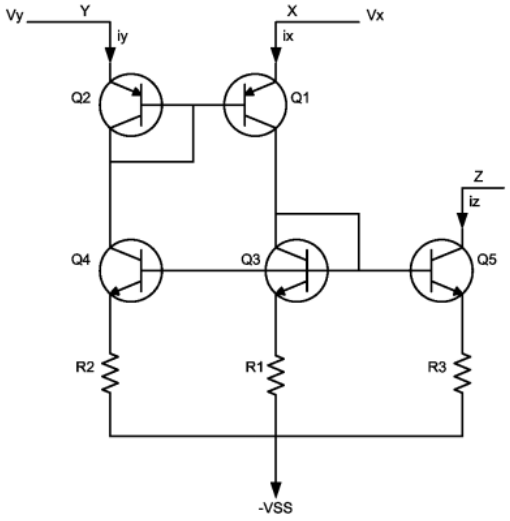


Fig.3.2 First Bipolar Current Conveyor [5]

As already discussed, transistor Q1, Q2 and transistor Q5, Q4 and Q3 are matched and on the other hand resistor R1, R2, R3 are matched to obtain better current mirroring property. Author observation from above circuits are as follows: -

1. The Y-terminal didn't have to be grounded, and it could be linked to a voltage V y, resulting in an identical voltage in the X-terminal regardless of the current delivered to that terminal, resulting in a virtual short.

2. The current supplied to the terminal X is same as of the current flowing through the terminal Y and it's independent of voltage applied at terminal Y.

3. And finally, the current which flows through the output terminal Z is conveyed form the current supplied to the terminal X and also at terminal Z, impedance level is very high.

As a result of above discussion, the First Current Conveyor was born [5].

A CC is a minimum 3-terminals device, when paired with different electronic components like resistor, capacitor, transistor etc. in a circuit, it can perform a number of beneficial analog signal processing jobs. The current conveyor, like the opamp, makes circuit design easier. Furthermore, a current conveyor's real behaviour closely resembles its ideal behaviour, meaning that a designer can employ current conveyors that perform at levels close to their

projected theoretical performance [6]. There are different ways for the classification of current conveyor but majorly they are classified on the basis of their generation which goes as follows: -

(a) CCI or First Generation current conveyor

(b) CCII or Second Generation current conveyor

(c) Third Generation current conveyor commonly named as CCIII

Further each of above generations of current conveyor are divided as follows: -

(a) Positive or Negative Current Conveyor

(b) Direct or Inverted CC

(c) Current Controlled CC

(d) Multiple outputs CC

For visual understanding of division/bifurcation of current conveyor, the tree representation of it is already shown in Fig.3.1.

3.2 First Generation Current Conveyor (CCI)

The block depiction of first generation of CC's is shown in Figure 3.3, it's shown as a three port device. As previously said, in 1968 first current conveyor appeared and it is developed by Sedra and KC Smith [7] and its behaviour/functioning is described as: -

If voltage is supplied at Y terminal, then the terminal named as X has the same potential as of Y. The current driven into terminal X has no effect on voltage in X terminal, which is generated by the voltage in terminal named as Y. In the same way, if the input current flowing through X causes an equal current to flow into the terminal Y, and another equivalent current to flow into the output terminal Z and also the voltage delivered at the terminal Y has no effect on the current through the terminal Y, which was established by the current via the terminal X. Now due to above mentioned facts, the current through Y terminal and voltage at terminal X are processed by a current follower and voltage follower respectively. In conclusion we can say that the, current conveyor has a property of dual virtual open circuit input and a virtual short circuit input characteristic at the terminal Y & Y respectively [6].

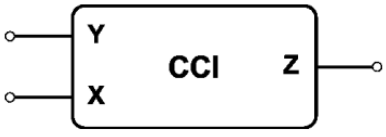


Fig.3.3 First Gen current conveyor

Now after having theoretical understanding of first generation of current conveyor lets us move our focus in understanding of equations of current conveyor which is derived from above discussion and represented in matrix form below: -

$$\begin{bmatrix} iy \\ vx \\ iz \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} vy \\ ix \\ vz \end{bmatrix} \quad (3.1)$$

From matrix equation 3.1 it's clear that the, current going through the terminal Y is the same as that flowing through the terminal X i.e. $i_y = i_x$. the second equation obtained from the matrix states that $v_x = v_y$, i.e. X's terminal voltage is equal to the voltage at terminal names as Y, and from the last column of matrix shows that $i_z = \pm i_x$ which means that the current flowing in terminal named as Z is same in magnitude that flows through terminal X and as previously discussed current conveyor are of two types i.e. positive and negative so depending upon the configuration Z terminal can take respective direction.

3.2.1 Positive and Negative type first generation current conveyor

As mentioned earlier, one of the classifications of CC is centred on positive and negative type so let's look in to that in detail. This type of classification just depends upon the direction of current that flows into terminal Z of current conveyor. As discussed earlier the third column of matrix equation describes the direction of flow of current in terminal Z. The CCI is called Positive First Generation CC or CCI+ if both currents in the terminals X and Z enter or leave i.e. from equation 3.1 if condition is $i_z = i_x$, on the contrary if the equation of current is $i_z = -i_x$ then the current conveyor is Negative First Generation of CCs or simply CCI- i.e. current flowing through the terminal named as Z has the opposite direction as the current which is flowing through the terminal named as X [6]. Figure 3.4. shows the block diagram representation of both CCI- & CCI+.

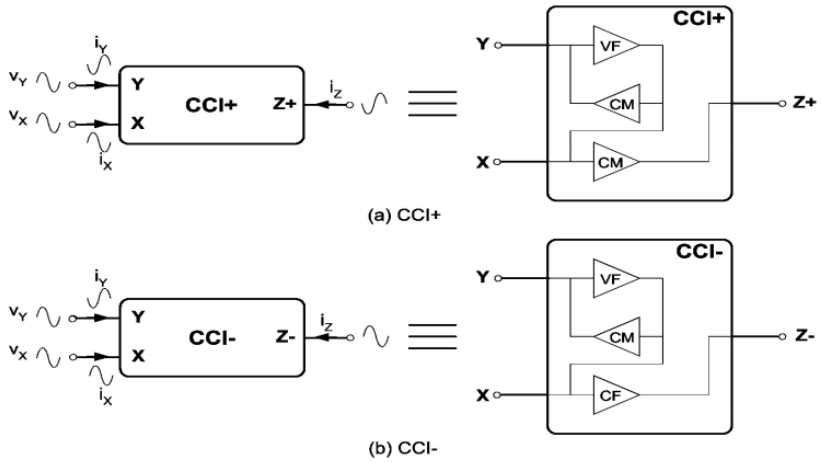


Fig.3.4 Block diagram of (a)CCI+ (positive type) (b) CCI- (negative type) [4]

In a CCI+, the current flows through the terminal Z has a phase of 180 degrees relative to the current that flows through the terminal X. So, to implement this and satisfy the equation 3.1 between terminal Y and terminal X there should be a Voltage Follower (VF) which helps in achieving $v_x = v_y$. and to satisfy the current equation of equation 3.1 there is a requirement for two current mirror which make sure that the equations $i_y = i_x$ and $i_z = i_x$ follows. Similarly, for CCI-, the current flows through the terminal Z has a phase of 0 degrees relative to the current that flows through the terminal X. It also requires Voltage follower and current mirror to achieve $v_x = v_y$ and $i_y = i_x$ respectively and to achieve $i_z = -i_x$ we require current follower instead of current mirror in previous case, shown in Fig.3.4.

3.2.2 Direct and Inverse Current Conveyor

According to the polarity of voltage present at terminal Y, the current conveyor is classified as Direct or Inverse. In Direct first generation of CCs (CCI) the polarity voltage of terminal X & Y are same. On the other hand, if they have opposite polarity then they are called as Inverse first generation of current conveyor (ICCI). Matrix eq.3.2 describes the relation between input/output current and voltages [6].

$$\begin{bmatrix} iy \\ vx \\ iz \end{bmatrix} = \begin{bmatrix} 0 & 1 & 0 \\ \pm 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} vy \\ ix \\ vz \end{bmatrix} \tag{3.2}$$

From above matrix equation we can say that if vx = vy then we get direct CCI, on the other hand, if vx = -vy then we get Inverse CCI. and from same equation the third row is also showing that both direct and indirect current conveyor can be further divided in to positive and negative types which is already discussed in previous section. The only difference can be observed in case of Inverse CCI is that in direct CCI voltage follower is replaced by voltage mirror to satisfies the condition of inverse CC which is vx = -vy and all other concepts will be same which are described in detail in previous section. Figure 3.5 shows the block diagram for Inverse CC in both positive and negative type.

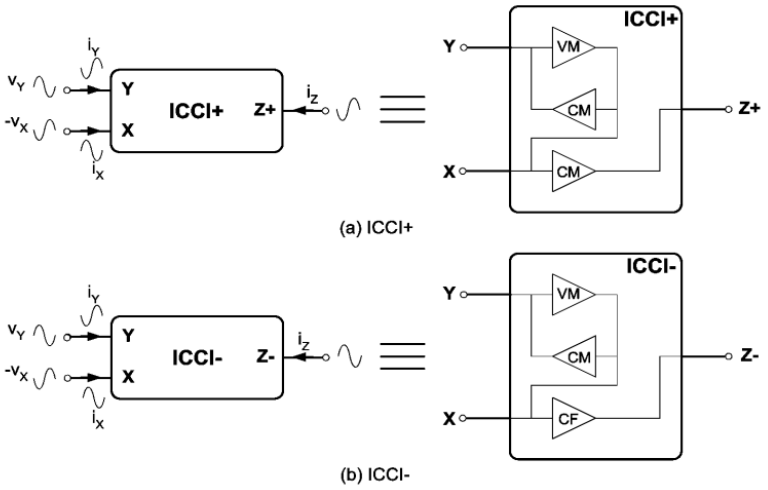


Fig.3.5 Block Diagram of (a) ICCI+ (positive type) (b) ICCI- (negative type) [4]

3.2.3 Multiple Output Current Conveyor

As the name suggests, the current conveyor having more than one output terminal i.e. terminal Z is said to be Multiple Output Current Conveyor. It's abbreviated as MOICCI for Inverse Multiple Output Current Conveyor and Direct Multiple Output Current Conveyor for MOCCI. Negative & Positive both type of output can be present in MOCCI and also they can be implemented in both direct and inverse form. The block diagram representation of Multiple Output Current Conveyor in both direct and inverse form with positive and negative type output is shown by Fig 3.6 . The concepts will remain the same which are discussed earlier in this chapter.

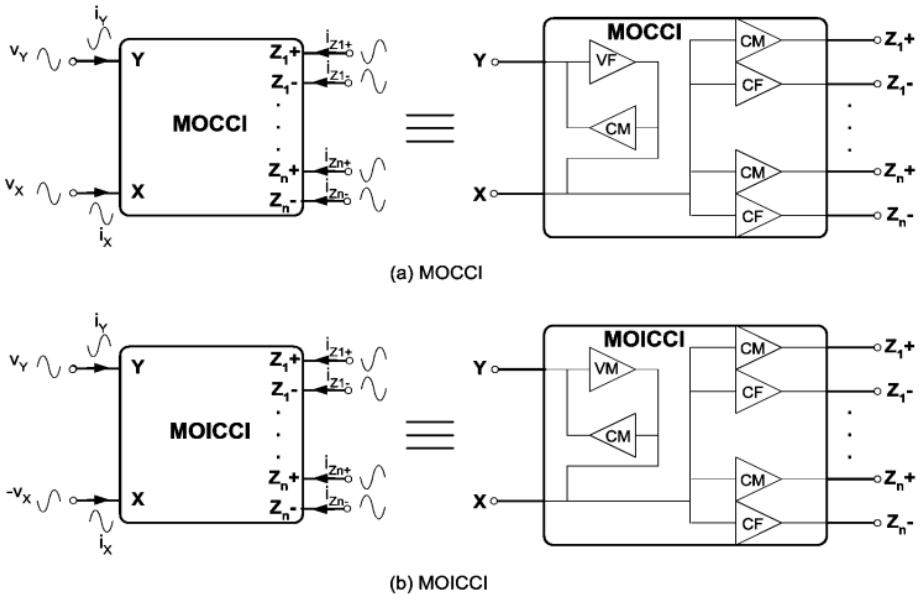


Fig.3.6 Block diagram of (a) MOCCI (b) MOICCI [4]

3.2.4 Current Controlled Current Conveyor

This type of current conveyor follows similar concepts which are described in earlier section except that in this their biasing current can be manipulated externally by a biasing current Iref. Block diagram for different combination of Current Controlled Current Conveyor is shown by below Fig.3.7.

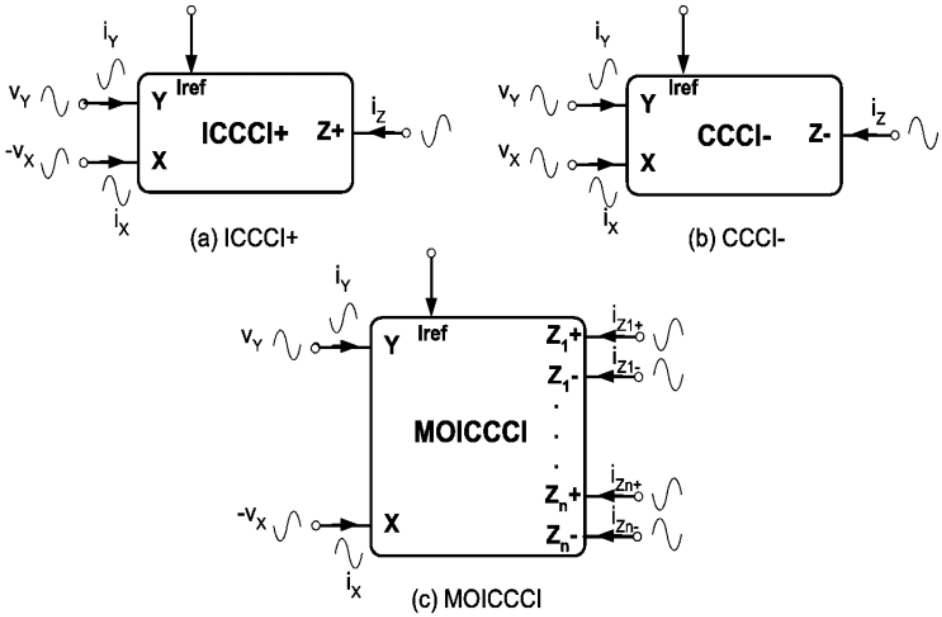


Fig.3.7 Block Diagram of different CCCC (a) Positive type Inverse Current Controlled CC (b) Negative type Direct Current Controlled CC (c) Multiple Output Current Controlled CC[4]

3.3 Second Generation Current Conveyor (CCII)

In 1970's same author Sedra and KC Smith [8] proposed the second version of current conveyor which increases the versatility of first generation of CCs. In first generation of CCs, the current going through terminal Y is the same as that flowing through the terminal X i.e. $i_y = i_x$, in this generation it has been modified that the current flows through terminal Y is zero i.e. iy = 0 and due to this, terminal Y will now acts as high (almost infinite) input impedance terminal and all other parameters are same, now due to this (iy = 0), the impedance seen from terminal named as X is zero, because the voltage at terminal named as Y & terminal X are same. The input current flowing via the terminal X causes an equal current to flow into the terminal Z [6]. Now let us look at the matrix equation of second generation of CCs which is shown by equation 3.3.

$$\begin{bmatrix} iy \\ vx \\ iz \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} vy \\ ix \\ vz \end{bmatrix} \tag{3.3}$$

From matrix equation 3.3 it's clear that the, current going through the terminal Y i.e. iy = 0, the second equation obtained from the matrix states that $v_x = v_y$, i.e. the voltage at terminal named as X is equal to Y's terminal voltage and the last column of matrix shows that $i_z = \pm i_x$ which means that the current that flows through terminal named as Z is same in magnitude that flows through terminal X and as previously discussed current conveyor are of two types i.e. positive and negative so depending upon the configuration Z terminal can take respective direction.

3.3.1 Positive and Negative Type Second Generation Current Conveyor

As deliberated in section 3.2.1, similar concept is followed in second generation of current conveyor too except the changes mentioned in section 3.3. So let us briefly study the positive and negative type second generation current conveyor with their block diagrams.

This type of classification just depends upon the direction of current that flows into terminal Z of current conveyor. The CCII is called Positive Second Generation of CC or CCII+ if both currents in the terminals X and terminal named as Z enters or leaves i.e. from equation 3.3 if condition is $i_z = i_x$, on the contrary if the equation of current is $i_z = -i_x$ then the CC is called Negative First Generation of CC or simply CCII- i.e. current flowing through the terminal named as Z has the opposite direction as the current i.e. flowing through the terminal X . Fig.3.8 shows the block diagram of both CCs.

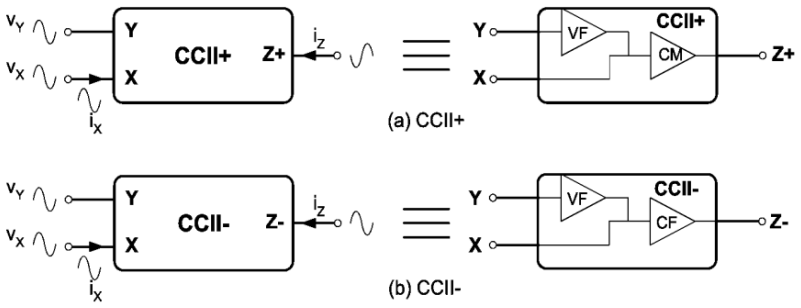


Fig.3.8 Block Diagram of (a) CCII+ (positive type) (b) CCII- (negative type) [4]

From the Fig.3.8 it is evident that the block diagram of CCII differ from CCI, as there is no requirement of current mirror which earlier (in CCI) requires for making iy = ix, because in CCII iy = 0. And functionality of remaining block is exactly same as discussed in section 3.2.1.

3.3.2 Direct and Inverse Second Generation CC

Depending upon polarity of voltage at Y terminal, the second generation of CC can also be classified as Direct or Inverse. In Direct second generation of CC (CCII) the polarity of voltage of terminal named as X & Y are same. On the other hand, if they have opposite polarity then they are called as Inverse second generation of current conveyor (ICCII). Matrix eq.3.4 describes the relation between input/output current and voltages: -

$$\begin{bmatrix} iy \\ vx \\ iz \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \pm 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} vy \\ ix \\ vz \end{bmatrix} \tag{3.4}$$

From above matrix equation it we can say that if vx = vy then we get direct CC, on the other hand, if vx = -vy then we get Inverse CC. and from same equation the third row is also showing that both direct and indirect current conveyor can be further divided in to positive and negative types which is already discussed in previous section. The only difference can be observed in case of Inverse CC is that in direct CC voltage follower is replaced by voltage mirror to satisfies the condition of inverse CC which is vx = -vy and all other concepts will be same which are described in detail in previous section. The block diagram for Inverse CC in both positive and negative type is shown by Figure 3.9.

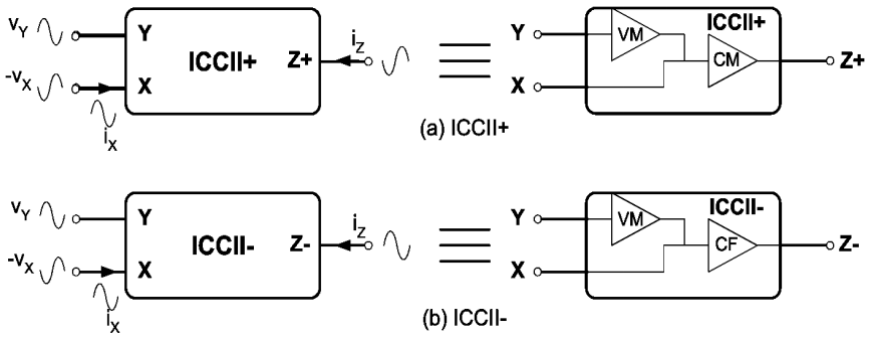


Fig.3.9 Block Diagram of (a) ICII+ (positive type) (b) ICCII- (negative type) [4]

3.3.3 Multiple Output Second Generation Current Conveyor

Again, similar concept, already explained in section 3.2.3. Block diagram for the same can be found in Fig.3.10.

3.3.4 Current Controlled Second Generation Current Conveyor

Again similar concept, already explained in section 3.2.4. If an external current bias is applied to current conveyor, then its knows as Current Controlled Second Generation CC. Block diagram for the same can be found in Figure 3.11.

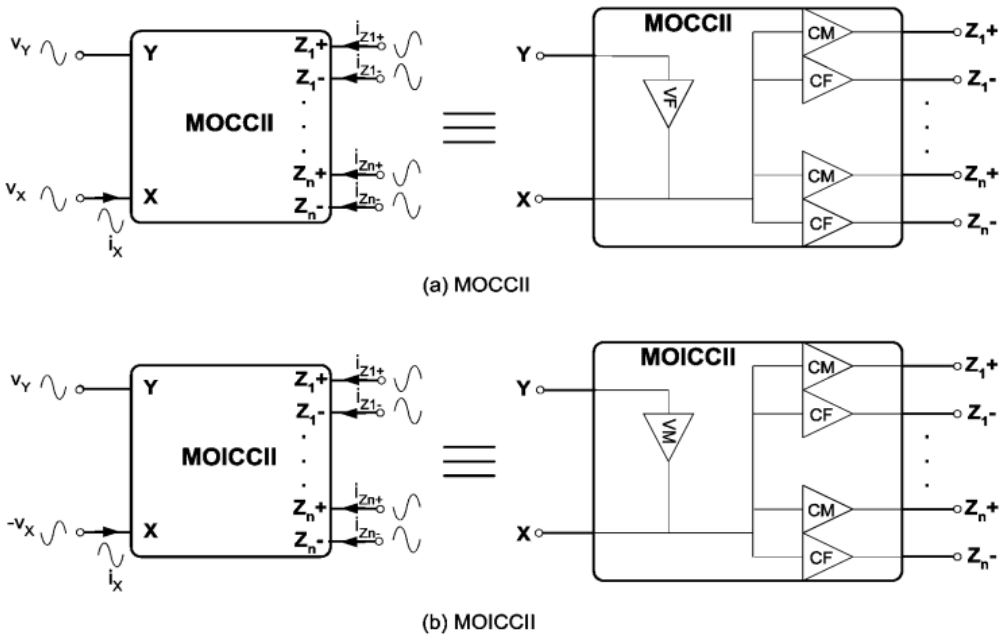


Fig.3.10 Block Diagram of second gen. (a) Multiple Output Second Generation CC (b) Multiple Output Inverse Second Generation CC [4]

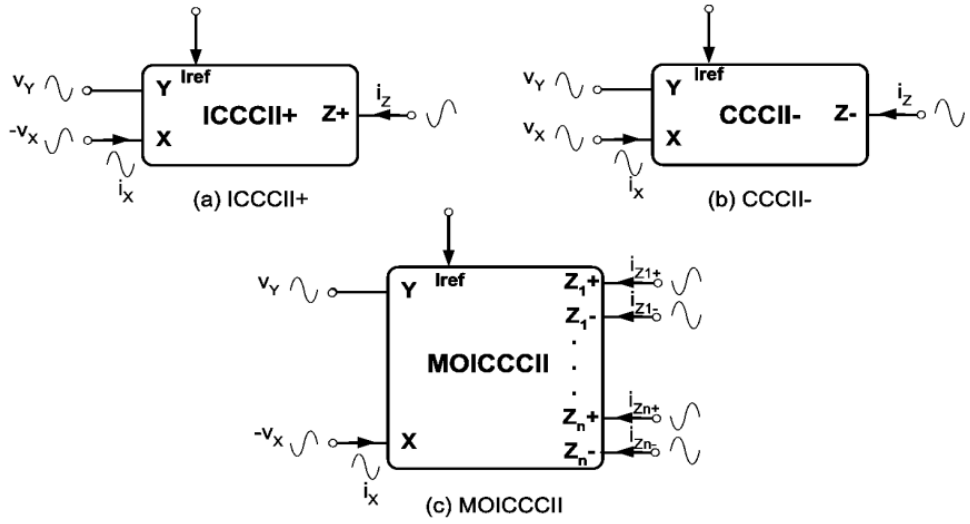


Fig.3.11 Block Diagram of (a) Inverse Current Controlled Second Generation CC (b) Negative type Current Controlled Second Generation CC (c) Multiple Output Inverse Current Controlled Second Generation CC [4]

3.4 Third generation of Current Conveyor

In 1995, A Fabre designed the third generation of current conveyor CCIII [9]. The third generation of CC works in similar fashion as of first generation of CC or CCI. In first generation of CC, the current flowing through the terminal Y is the same as that flowing through terminal named as X i.e. $i_y = i_x$, in this generation it has been modified that the current flows through terminal Y is in reverse direction as per that flowing through the terminal named as X i.e.

$i_y = -i_x$. Now let us look at the matrix equation of third generation of CC which is shown in equation 3.5.

$$\begin{bmatrix} iy \\ vx \\ iz \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} vy \\ ix \\ vz \end{bmatrix} \tag{3.5}$$

From matrix equation 3.5 it's clear that the, current going through the terminal Y i.e. iy = -ix, the second equation obtained from the matrix states that $v_x = v_y$, i.e. the voltage at terminal named as X is equivalent to voltage at terminal named as Y and the last column of matrix shows that $i_z = \pm i_x$ which means that the current i.e. flowing in terminal named as Z is same in magnitude that flows through terminal X and as previously discussed current conveyor are of two types i.e. positive and negative so depending upon the configuration Z terminal can take respective direction.

3.4.1 Positive and Negative Type Third Generation Current Conveyor

As discussed in section 3.2.1, similar concept is followed in third generation of current conveyor too with the exception of iy = -ix. So in order to follow these changes the current mirror block that is present in block diagram of CCI is replaced by current follower block and the direction of current that is flowing in terminal Y is also inverted as shown in Fig. 3.12 and other concepts remains the same.

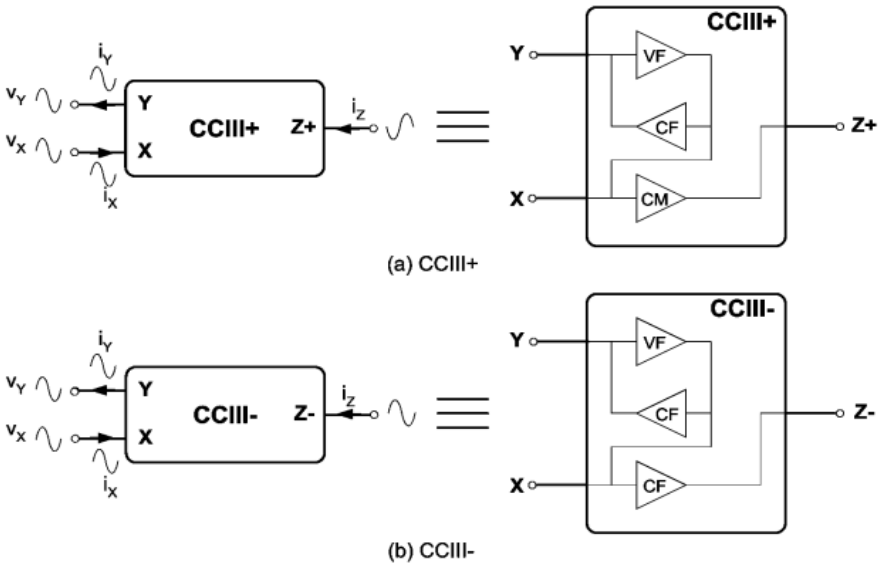


Fig.3.12 Block Diagram of (a) CCIII+ (positive type) (b) CCIII- (negative type) [4]

3.4.2 Direct and Inverse Third Generation Current Conveyor

Depending upon the polarity of the voltage at terminal named as Y the third generation of CCs can also be classified as Direct or Inverse. In (CCIII) Direct third generation of CC the polarity of voltage (vx = vy) of terminal names as X & Y are the same. On the contrary, if they have opposite polarity (vx = -vy) then they are called as Inverse third generation of current conveyor (ICCIII). Matrix eq.3.6 describes the relation between input/output current and voltages: -

$$\begin{bmatrix} iy \\ vx \\ iz \end{bmatrix} = \begin{bmatrix} 0 & -1 & 0 \\ \pm 1 & 0 & 0 \\ 0 & \pm 1 & 0 \end{bmatrix} \begin{bmatrix} vy \\ ix \\ vz \end{bmatrix} \quad (3.6)$$

Equation 1 of matrix is already described in section 3.4 and rest of the equations are already explained in section 3.2.2. Figure 3.13 shows the block diagram depiction of Direct and Inverse Third Generation Current Conveyor.

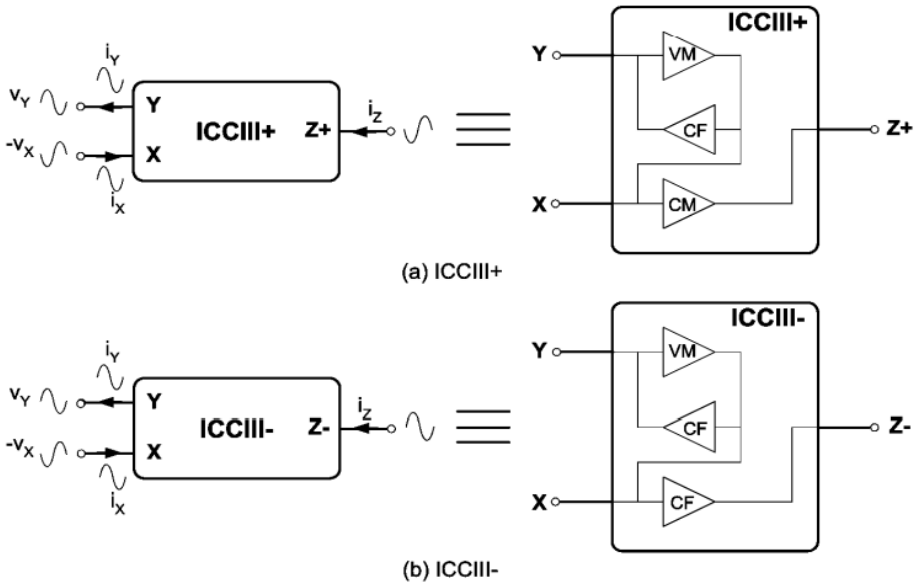


Fig.3.13 Block Diagram of (a) Direct CCIII+ (positive type) (b) Inverse CCIII- (negative type) [4]

3.4.3 Multiple Output Third Generation Current Conveyor

Similar concept, already explained in section 3.2.3. Block diagram for the same can be found in Figure 3.14

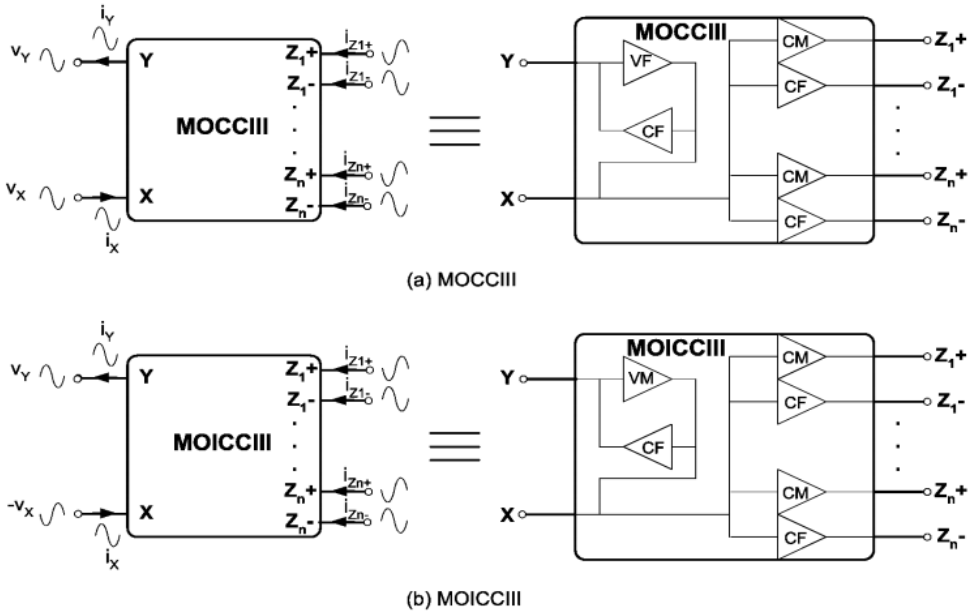


Fig 3.14 Block Diagram of CC (a) Multiple Output Third Generation CC (b) Multiple Output Third Generation CC [4]

3.4.4 Current Controlled Third Generation Current Conveyor

Similar concept, already explained in section 3.2.4. If an external current bias is applied to current conveyor, then its knows as Current Controlled Third Generation Current Conveyor. Figure 3.15 shows the block diagram for the CCC.

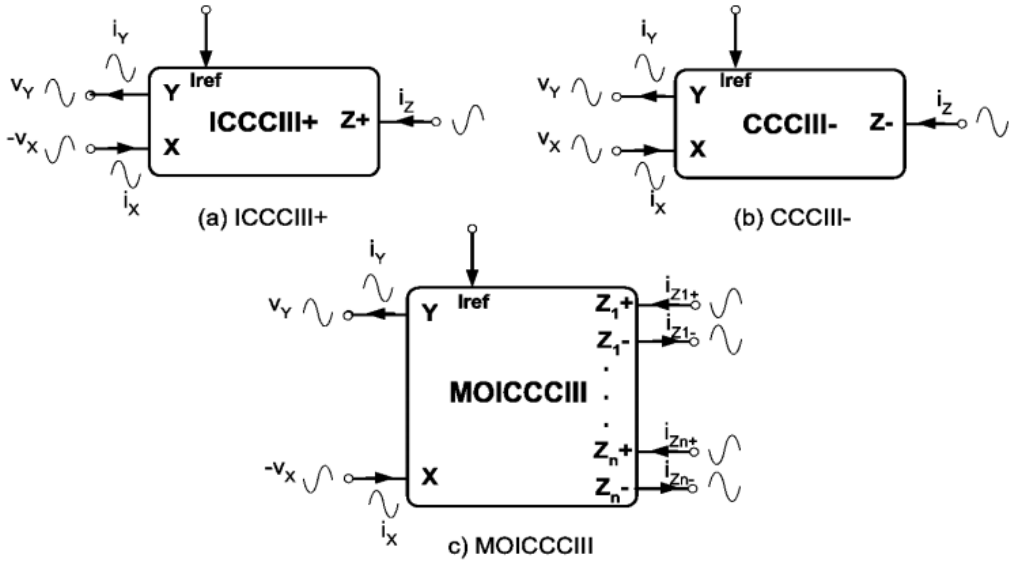


Fig.3.15 Block Diagram of (a) Positive type Inverse Current Controlled Third Generation CC (b) Negative type Current Controlled Third Generation CC (c) Multiple Output Inverse Current Controlled Third Generation Current Conveyor [4]

3.5 Summary

This chapter started with the introduction to current conveyors their advantages, then we have seen how first current conveyor was born with its functionality and authors observations regrading that. Later we have seen the bifurcation of current conveyors according to their generations and how they are further divided as shown in Fig.3.1. Detailed study of current convenors with their block diagram and conceptual study is present in this chapter.

CHAPTER 4: - OPERATIONAL FLOATING CURRENT CONVEYOR (OFCC)

Before directly jumping into the operation/functioning of OFCC block, let us look at what is current mode and voltage mode of operation of analog devices. The two regulating conditions that regulate the supply's output are current mode and voltage mode. A voltage source is often depicted as having a low supply output impedance. The reason for that is due to low impedance, the voltage drop across impedance is very low due to this it can supply maximum voltage to circuitry without any drop across low impedance, in this way we can say that supply is working is in voltage mode. While on the contrary, current mode is identical to voltage mode, except that it restricts and controls the supply's output current to the required level.

Moreover a current mode or a voltage mode device can be used for analog processing circuit. When the gain of a voltage mode device is raised, due to the fact that gain-bandwidth product remains constant, which leads to reduction in the bandwidth of the amplifier [10]. As a result, for circuits that run at high frequencies, at that high freq. current mode devices may be preferred. The following are some of the key benefits of the current model over voltage mode devices: -

(a) Larger dynamic range.

(b) Better linearity, higher slew rate.

(c) Wider bandwidth, constant bandwidth at different gain

In recent decades, current-mode design techniques have gotten a lot of attention because they have a broader gain independent bandwidth than their voltage equivalent. Current-mode circuits also have greater precision, linearity and dynamic range than traditional circuits [11, 12].

The OFCC (Operational Floating Current Conveyor) combines CCII± (second generation current conveyor) and CFOA (current feedback amplifier) [11] and which makes it flexible analog block. CCII functioning has been already explained in section 3.3 in greater depth. So, let us briefly study about CFOA (current feedback amplifier).

Comlinear Corporation [13] was the first to create the current feedback amplifier (CFA) based on the CCII+. The initial CFA circuit was a BJT, and after that, much work was put into developing a CFA circuit based upon CMOS technology for use in low power VLSI applications. [14] presented the operational floating conveyor (OFC) based on BJT transistors, which used the current feedback amplifier circuit as the main block. [Alison Payne et al]

Any closed-loop design in which the error signal utilised for feedback is in the form of a current is known as current feedback. Rather than an error voltage, a current feedback op amp creates a similar output voltage in response to an error current at one of its input terminals. Fig.4.1 shows the basic topology for the voltage feedback and current feedback amplifiers.

Despite the fact that the OFCC is a potential current mode device, research on it is quite restricted. [Anwar Khan] introduced the Operational Floating Current Conveyor circuit first, which used discrete BJTs and discrete components i.e. AD846 which is based on a commercial CFA. The same OFCC circuit was then used by [Ghallab et al.] in a variety of applications,

including instrumentation amplifier, a Wheatstone bridge, universal filter and Lab on chip systems etc. [15-17].

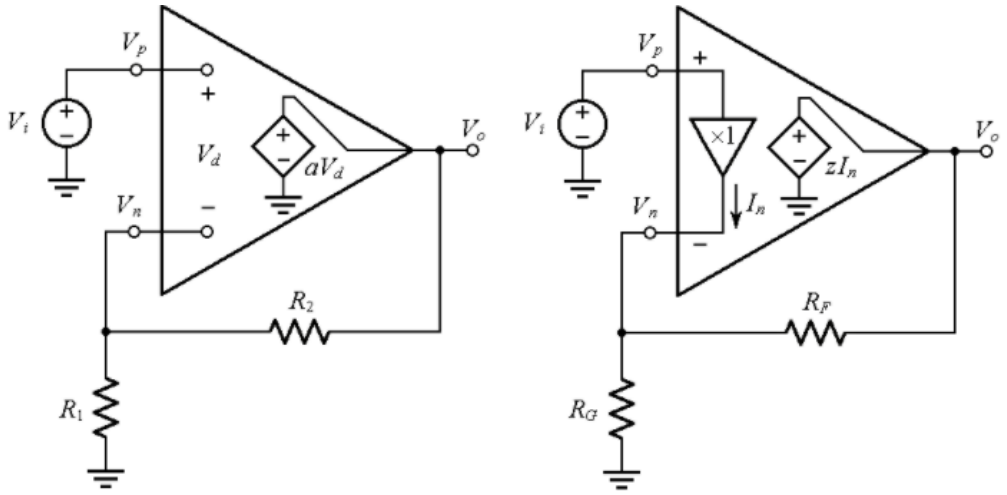


Fig.4.1 Basic topology of (a) Voltage Feedback Amplifier (b) Current Feedback Amplifier [31]

4.1 OFCC Block Diagram

As shown in figure 4.2, OFCC has five-port with three outputs and two inputs. In this figure, the low impedance current input is represented by port X, port Y represents the high impedance input voltage, the high impedance output current is represented by port Z+ and Z- with reversed polarities and the port labelled as W represents low impedance output voltage.

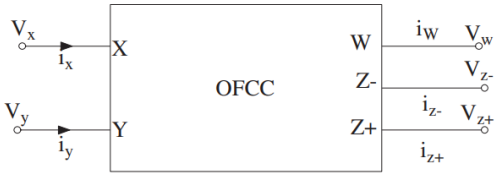


Fig.4.2 OFCC's block diagram [15]

Zt is open loop trans impedance gain which is multiplied by port X's input current due to which at port labelled as W, an output voltage generated. In OFCC input has voltage tracking property because port Y's voltage is seen on port X. There is current tracking behaviour too at the output port because the output current that flows at port labelled as W is in phase with that flowing into port Z+ and at port Z-same current flows but with reversed phase [15]. As a result, the ideal OFCC's transmission properties of the can be defined in matrix equation 4.1: -

$$\begin{bmatrix} iy \\ vx \\ vw \\ iz+ \\ iz- \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 \\ hv & 0 & 0 & 0 & 0 \\ 0 & Zt & 0 & 0 & 0 \\ 0 & 0 & hi1 & 0 & 0 \\ 0 & 0 & -hi2 & 0 & 0 \end{bmatrix} \begin{bmatrix} vy \\ ix \\ iw \\ vz+ \\ vz- \end{bmatrix} \quad (4.1)$$

where, port X has vx and ix as input voltage and current, vy and iy denote the inward voltage and current of the Y port, respectively, vz+ and iz+ denote the output voltage and current of

the port Z+. Similarly, the Z- port's output current and voltage are iz- and vz-, respectively and vw and iw denote the output voltage and current of the port W. Port X and W has impedance which is represented by Zt [15].

4.2 OFCC Circuit Design

After studying about the different blocks of OFCC, now it's high time to look into the transistor level implementation of OFCC. The implementation based on CMOS of OFCC is depicted in figure 4.3.

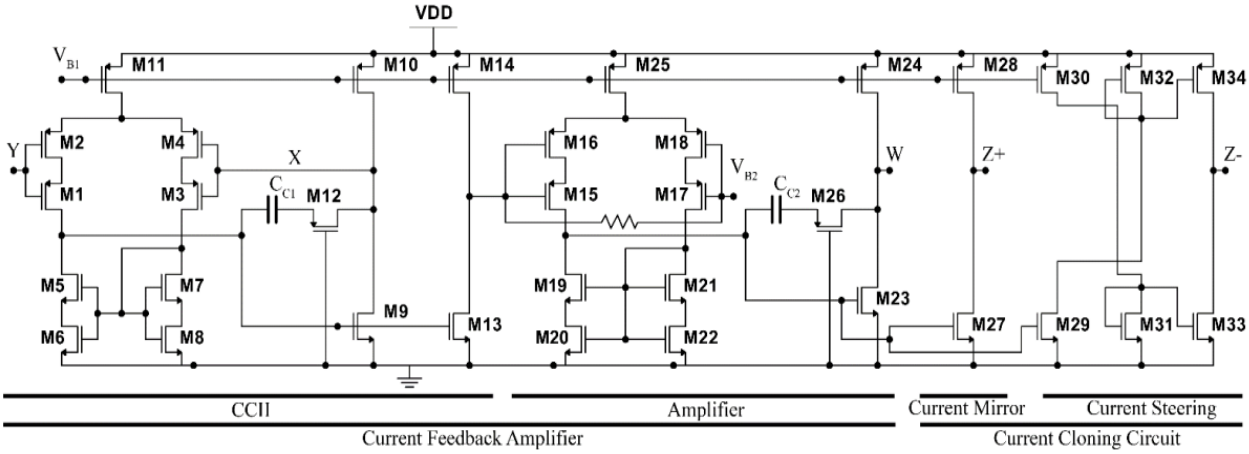


Fig.4.3 OFCC (Operational Floating Current Conveyor) Circuit [11]

As shown in Figure 4.3, CFOA and current cloning circuit (current mirror and current steering) are the two key components of OFCC. After CCII and then amplifier, can be used to design a low-power CFOA [18]. CCII is a two-stage op-amp having port X with unity gain feedback created by M [1-12] and for port Z a current mirror stage M [13-14] [16]. Since it uses the fewest MOSFETs, two stage topology was chosen. Because of the negative feedback, port X [16] impedance is typically zero, and if this impedance is divided by open loop gain and this will result in to output impedance of op-amp [19]. Tracking error of the CCII would be reduced if the Rx value is lower. Due to the presence of compensation capacitor Cc and the MOSFETs's operation in the subthreshold zone there is serious reduction in bandwidth of device, but a fair bandwidth can still be obtained due to the practicability of using large drain current in latest technology and the wide bandwidth of current mode devices [11].

Transistors M [1-24] make up the whole CFOA. Current Iw is copied by cloning circuit in phase to port Z+ via M [23] and M [27], and out of phase to port Z- via M [29-34] [11].

Table 4.1 and 4.2 shows the transistor sizing of OFCC at 90nm and 130nm respectively: -

Table 4.1 Transistor Sizing 90nm [11]

Transistor	W,L in um	Transistor	W,L in um	Transistor	W,L in um
M [17,18]	15, 2	M [26,28]	16, 0.5	M [22]	24, 0.5
M [2,4]	4, 1	M [1,3]	30, 2	M [23]	59.35, 0.5
M [5,7]	23, 2	M [6,8]	3.5, 2	M [24]	29, 0.5
M [25,27]	21, 0.5	M [19]	45, 0.2	M [11,12]	10, 0.5
M [9,13]	60, 0.5	M [20]	21.2, 0.5	M [10,14]	25, 0.5
M [15,16]	64, 2	M [21]	15, 0.5	M [29]	36, 0.5
Cc1	0.4 pF	Cc2	0.4 pF	M [30]	59.84, 0.5

Table 4.2 Transistor Sizing 130nm [11]

Transistor	W,L in um	Transistor	W,L in um	Transistor	W,L in um
M [12,26]	20, 0.12	M[6,8,20,22]	3, 2	M [29]	9.5, 0.39
M [2,4,16,18]	30, 1	M [10,14,24]	17.9, 0.39	M [30]	14, 0.39
M [19,13,23]	10.4, 0.39	M [13,15,17]	80, 1	M [31]	10, 0.39
M [11,25]	30, 2	M[5,7,19,21]	15, 2	M [32]	15, 0.39
Cc1	0.3 pF	M [27]	20.7, 0.39	M [33]	12.5, 0.39
Cc2	0.3 pF	M [28]	35.5, 0.39	M [34]	17.2, 0.39

4.3 Simulation

Now after studying the different theoretical concept of current conveyor and also about the OFCC block lets us now look into some simulation results. Simulation has been carried out using Symica DE software.

Fig4.4 shows the schematic of OFCC which is drawn of Symica DE.

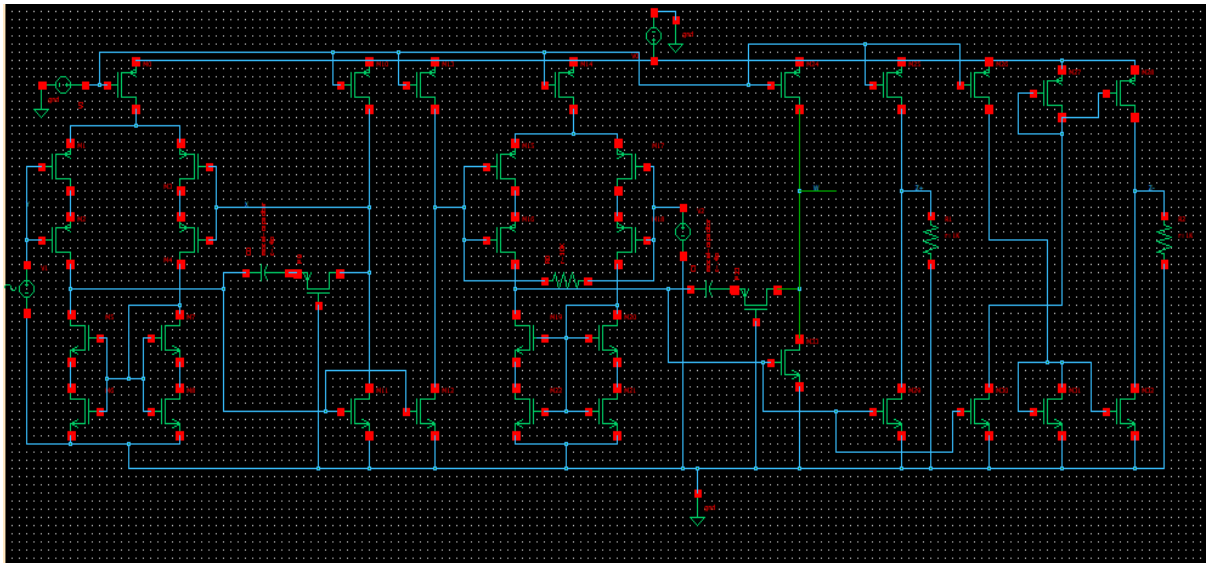


Fig 4.4 Schematic of OFCC

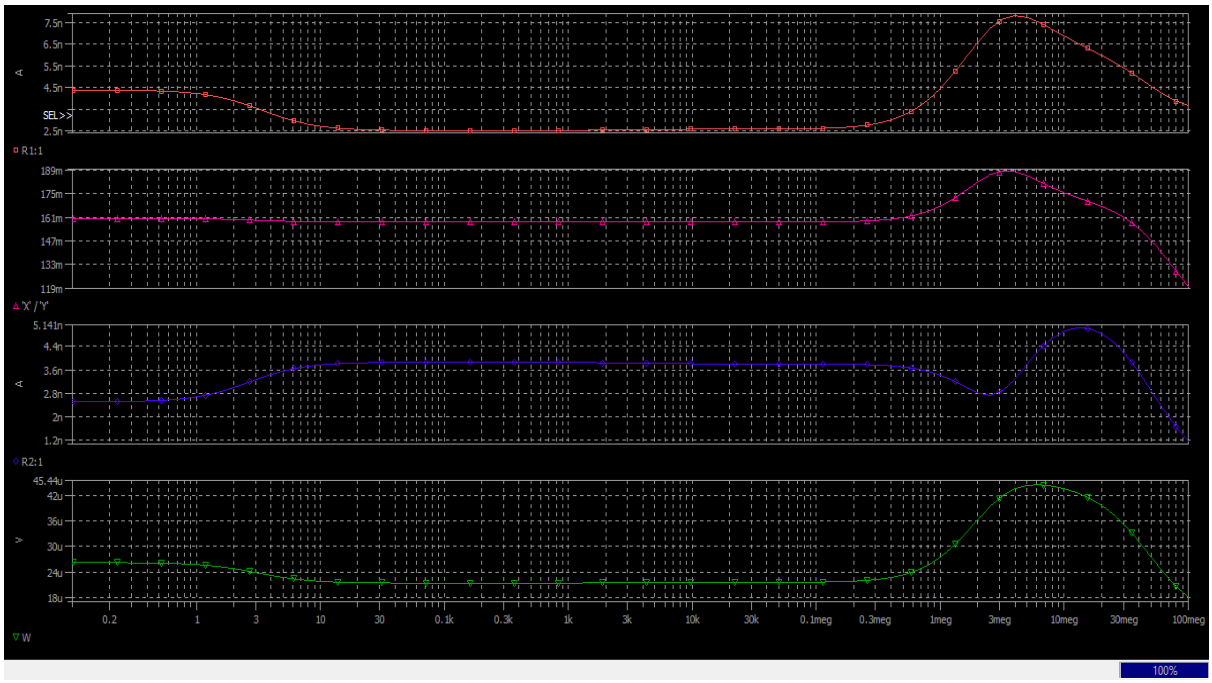
4.3.1 Plots for 90nm Technology Node

Supply Voltage = 0.4V

Input Voltage which is applied terminal Y is 1mv @1KHz

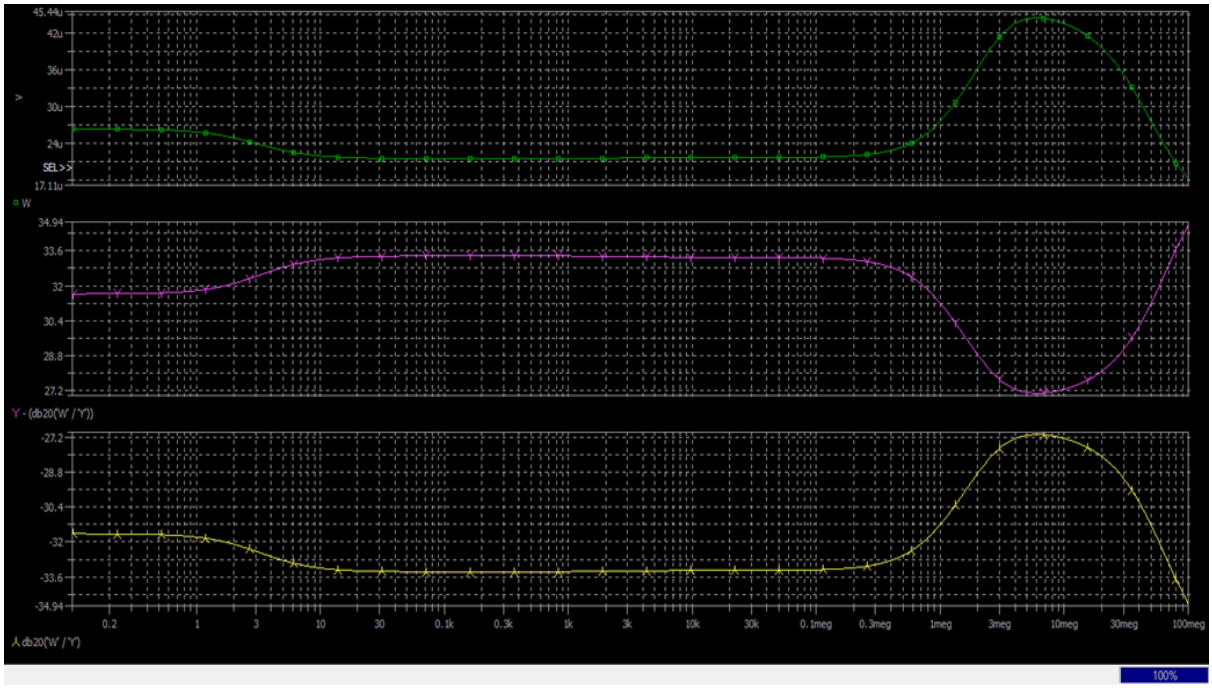
Analysis type is AC analysis with frequency sweep from 0.1Hz to 100MHz. (10dB per decade)

Plot 4.1 shows the plot of Vw, Iz+, Iz-.



Plot 4.1 Iz+, Iz-, Vw

Plot 4.2 shows the gain (dB20(Vw/Vy)) and bandwidth (can be seen from the plot)



Plot 4.2 Gain plot

Observations from above plots are: -

Gain (Vw/Vy) in dB is around 33.6dB

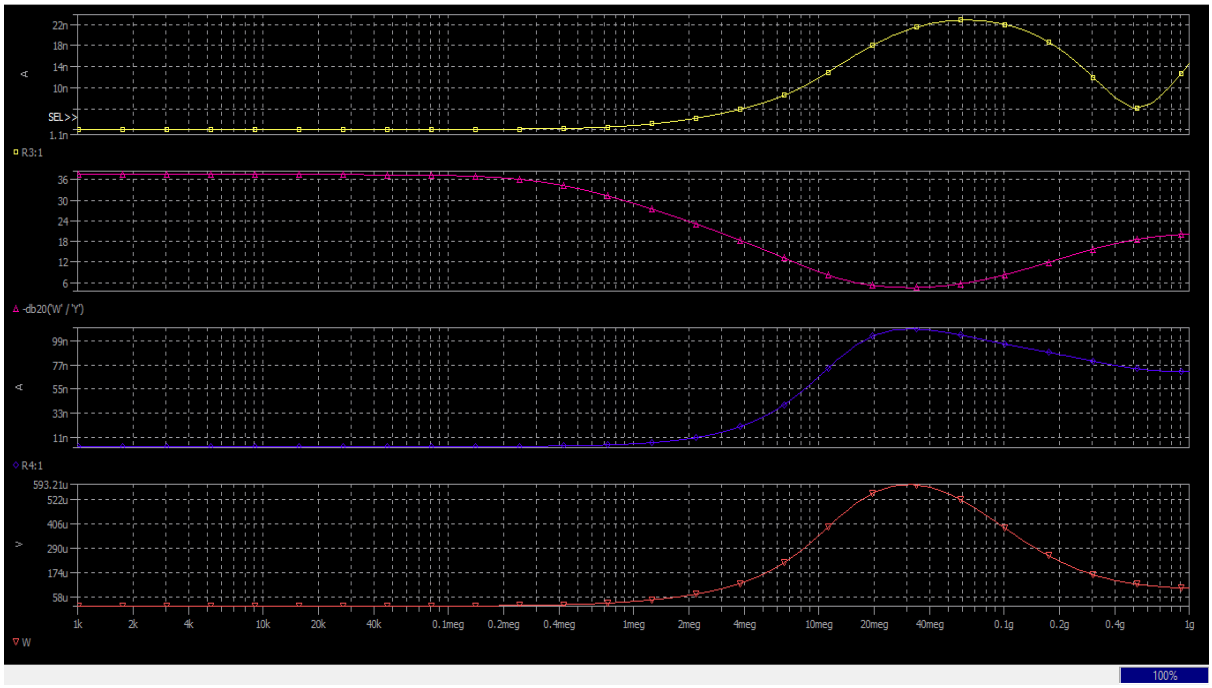
3dB Bandwidth observed = 1MHz (approx.)

4.3.2 Plots for 130nm Technology Node

Schematic is same for both the technology node only the W and L value are going to change which is already mentioned in Table 4.2.

Simulation environment is silmilar as disscussed in section 4.3.1

Plot 4.3 shows the Iz+, Iz-, gain (dB20(Vw/Vy)), Vw.



Plot 4.3 Iz+, Iz-, gain (dB20(Vw/Vy)), Vw

Observations from above plots are: -

Gain (Vw/Vy) in dB is around 36dB

4.4 Summary

In this chapter we have studied about voltage and current mode of operation of analog blocks, then we discussed what will happen if we use current mode devices in analog circuits and how they can be different form their voltage counter part. Later the differences between the voltage and current feedback amplifier is shown. Then we have studied about OFCC , its block diagram, matrix equation and also the CMOS implementaion of OFCC can be found in this chapter. This chapter also shows the simulation results of OFCC block in both 90nm and 130nm. Simulation has been performed using software Symica DE.

CHAPTER 5 : - AMPLIFIER IMPLEMENTATION

Amplifier as the name suggest, an amplifier is an electronics device which can be used to amplify the current or voltage at the output of any circuit and the amount of amplification can be measured by taking the ratio of output w.r.t input. In modern world amplifiers plays a very important role, almost all the electronic component uses amplifiers. Amplifiers have different types of topologies. They can be divided into feedback amplifiers without feedback amplifies. Back in 20th century voltage feedback amplifier plays a major role in electronics circuit, later advancements in technology also leads to development of current feedback amplifier. In chapter 4 we have basic introduction of voltage and current feedback amplifier and what are their differences. In this chapter, we'll look at the implementation of diverse amplifiers using new OFCC block.

Firstly, we will look into the block level representation of different amplifier configuration and after that we will see their simulations.

5.1 Voltage Amplifier

The electronic circuitry which can amplifies the voltage at output w.r.t input is called as voltage amplifier. Figure 4.1 shows the voltage amplifier using OFCC block.

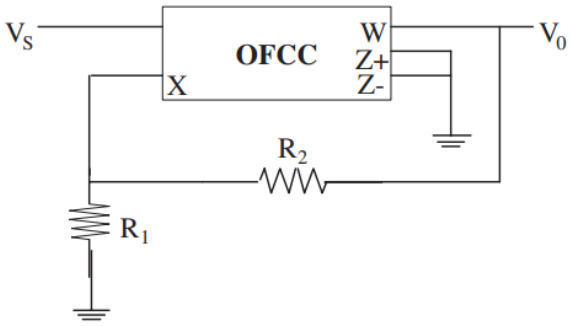


Fig.5.1 OFCC's Voltage Amplifier [15]

5.2 Trans Resistance Amplifier

The electronic circuitry which can amplifies the voltage at output w.r.t input current is called as trans resistance amplifier. The trans resistance amplifier using OFCC block is shown in Fig.5.2.

5.3 Trans Conductance Amplifier

The electronic circuitry which can amplifies the current at output w.r.t voltage at input is called as trans conductance amplifier. The trans conductance amplifier using OFCC block is shown in Fig.5.3.

5.4 Current Amplifier

The electronic circuitry which can amplifies the current at output w.r.t current at input is called as current amplifier. The current amplifier using OFCC block is shown in Fig.5.4.

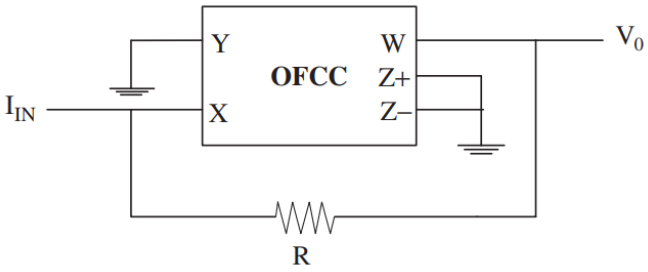


Fig.5.2 OFCC's Trans Resistance Amplifier [15]

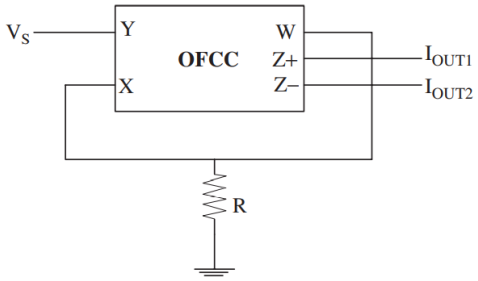


Fig.5.3 OFCC's Trans Conductance Amplifier [15]

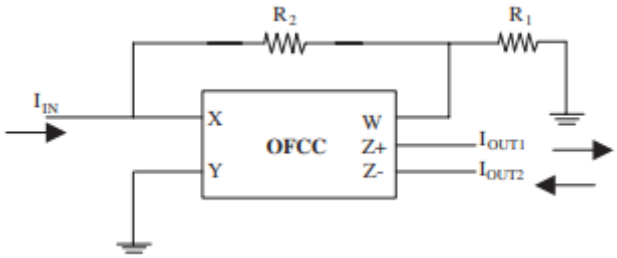


Fig.5.4 OFCC's Current Amplifier [15]

5.5 Simulation Results for 90nm Technology Node

5.5.1 Voltage Amplifier

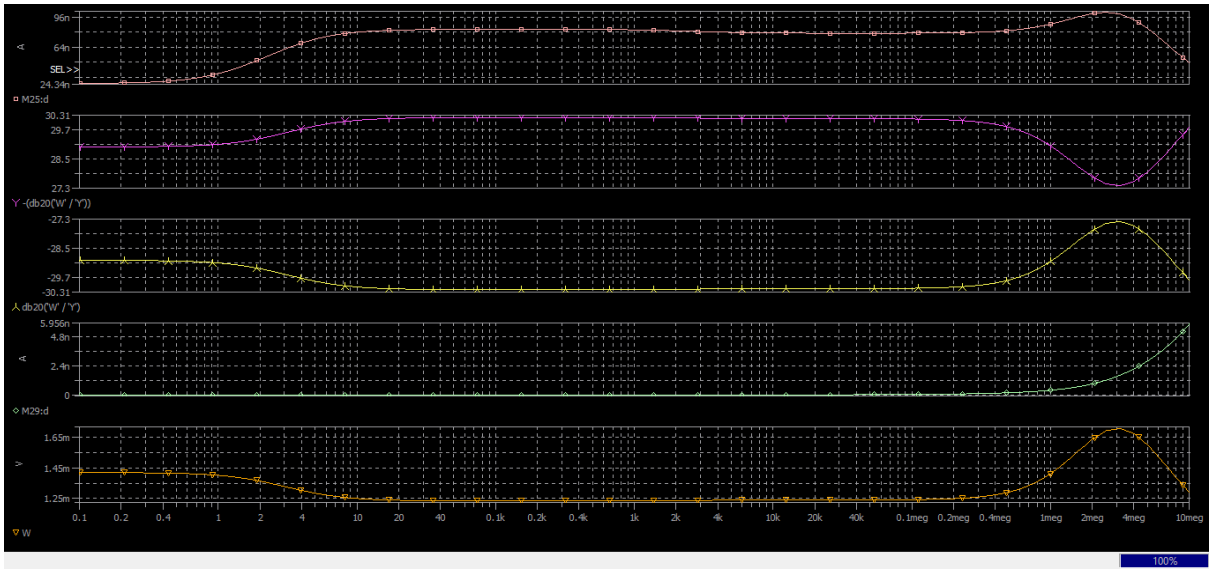
Simulation Environment: -

R2 = 10 kΩ, R1 = 1KΩ

Input voltage, Vs = 1mV @1KHz

Analysis type is AC analysis with frequency sweep from 0.1Hz to 10MHz. (10dB per decade)

Plot 5.1 shows the voltage amplifier based upon OFCC Block.



Plot 5.1 Voltage Amplifier

From Plot 5.1, observations are as follows: -

Voltage Gain = 30.31 dB

Bandwidth = 1MHz (approx.)

5.5.2 Trans Resistance Amplifier

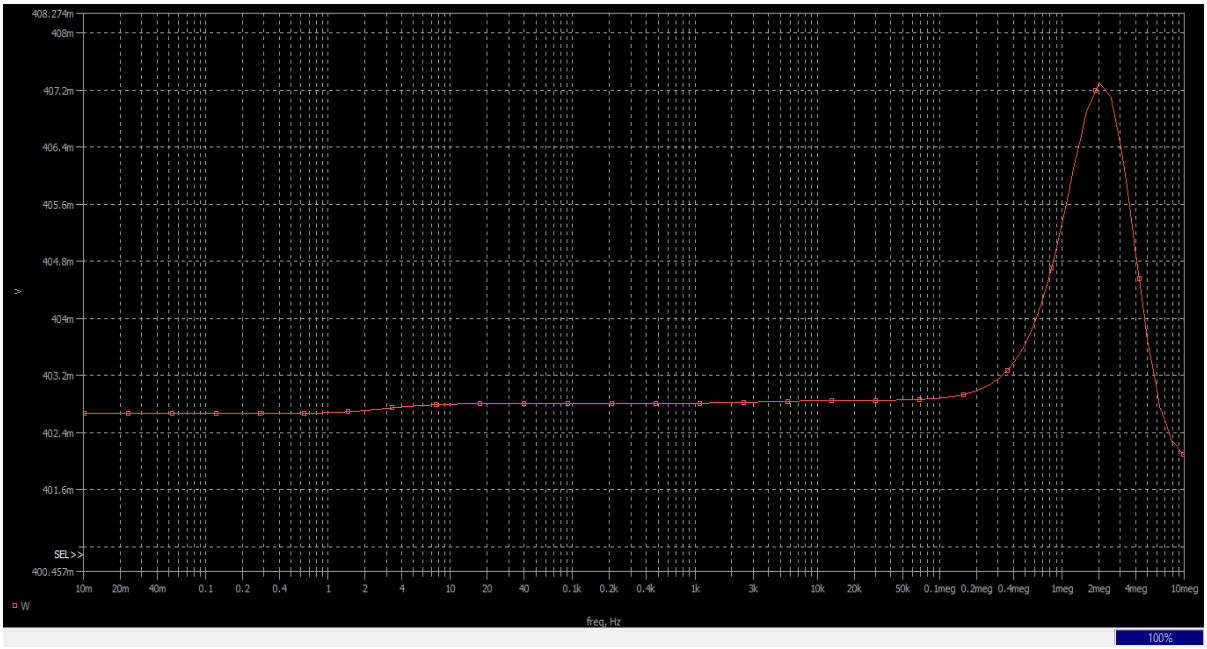
Simulation Environment: -

R1 = 1kΩ

Input Current, I_{IN} = 1mA @1KHz

Analysis type is AC analysis with frequency sweep from 0.01Hz to 10MHz. (10dB per decade)

Plot 5.2 shows the trans resistance amplifier based upon OFCC Block.



Plot 5.2 Trans Resistance Amplifier

From Plot 5.2, observations are as follows: -

Gain = 402.7Ω

5.5.3 Trans Conductance Amplifier

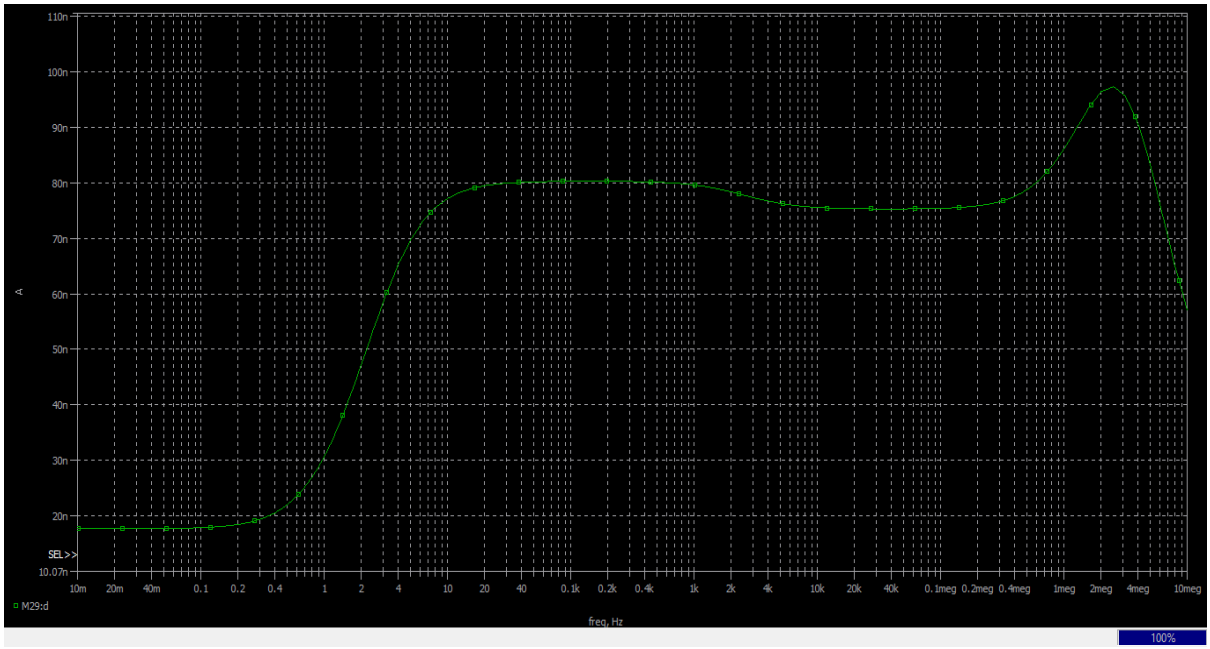
Simulation Environment: -

R1 = 1kΩ

Input voltage, Vs = 1mV @1KHz

Analysis type is AC analysis with frequency sweep from 0.01Hz to 10MHz. (10dB per decade)

Plot 5.3 shows the trans conductance amplifier based upon OFCC Block.



Plot 5.3 Trans Conductance Amplifier

From Plot 5.3, observations are as follows: -

Gain = 80µS

5.5.4 Current Amplifier

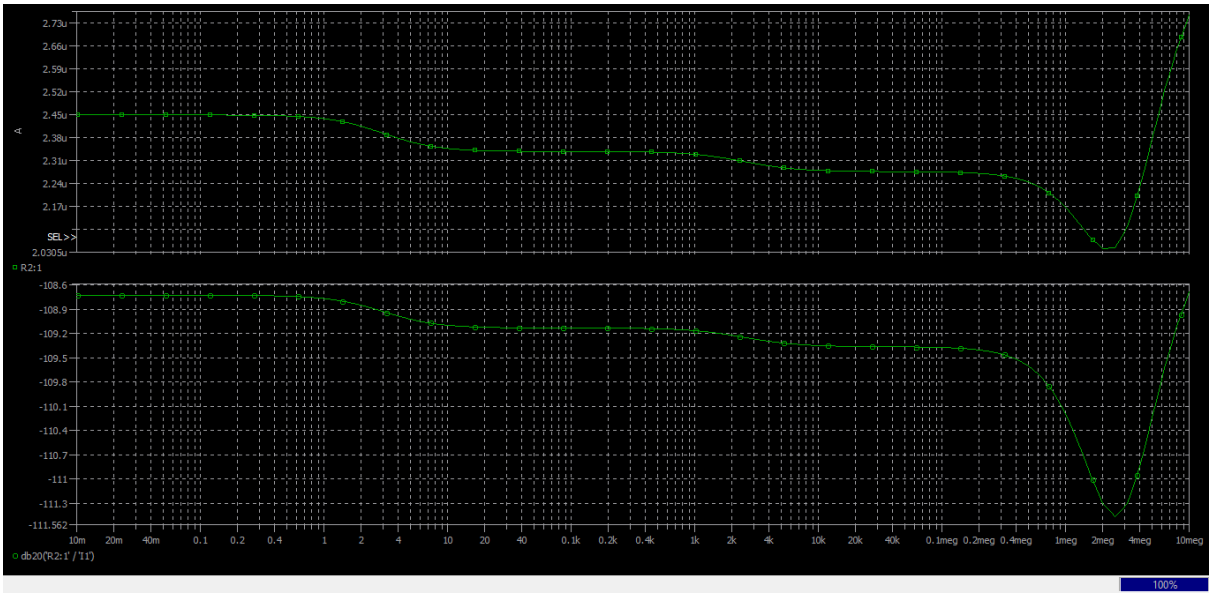
Simulation Environment: -

R1 = 10kΩ, R2 = 10KΩ

Input current, I_{IN} = 1mA @1KHz

Analysis type is AC analysis with frequency sweep from 0.01Hz to 10MHz. (10dB per decade)

Plot 5.4 shows the current amplifier based upon OFCC Block



Plot 5.4 Current Amplifier

From Plot 5.4, observations are as follows: -

Gain = 108.7 dB (approx.)

Bandwidth = 2.5MHz (approx.)

5.6 Simulation Results for 130nm Technology Node

5.6.1 Voltage Amplifier

Simulation Environment: -

R2 = 10 kΩ, R1 = 1KΩ

Input voltage, Vs = 1mV @1KHz

Analysis type is AC analysis with frequency sweep from 1Hz to 1GHz. (10dB per decade)

Plot 5.5 shows the voltage amplifier based upon OFCC Block.

From Plot 5.5, observations are as follows: -

Voltage Gain = 9dB

Bandwidth = 1MHz (approx.)

5.6.2 Trans Conductance Amplifier

Simulation Environment: -

R1 = 1kΩ

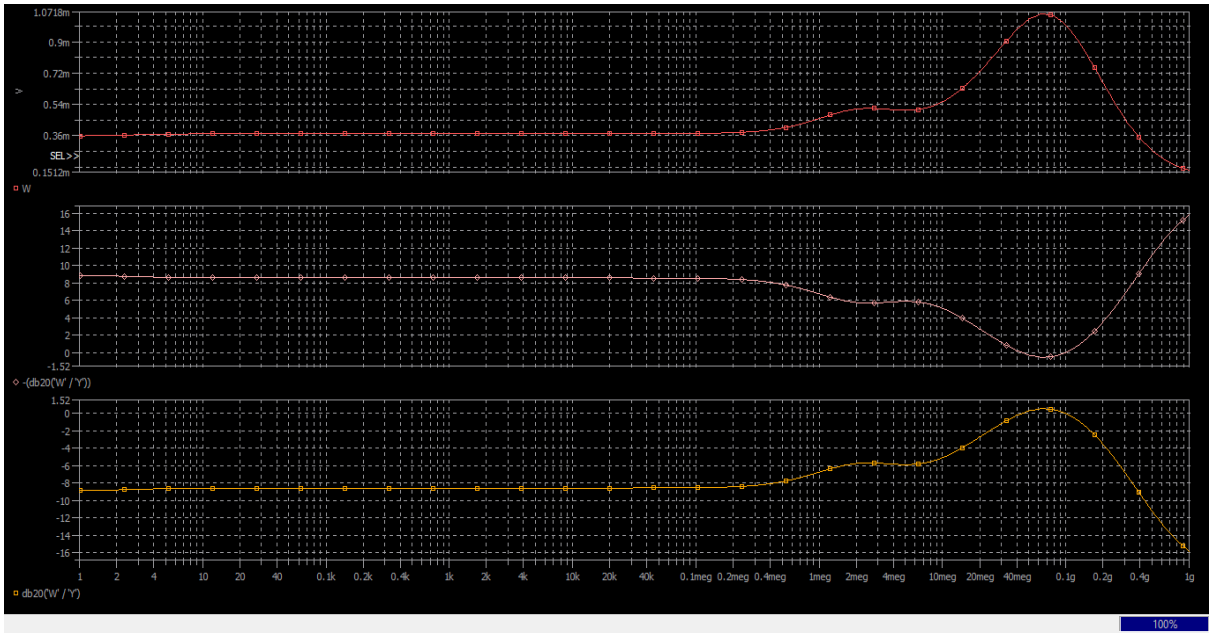
Input voltage, Vs = 1mV @1KHz

Analysis type is AC analysis with frequency sweep from 10Hz to 1MHz. (10dB per decade)

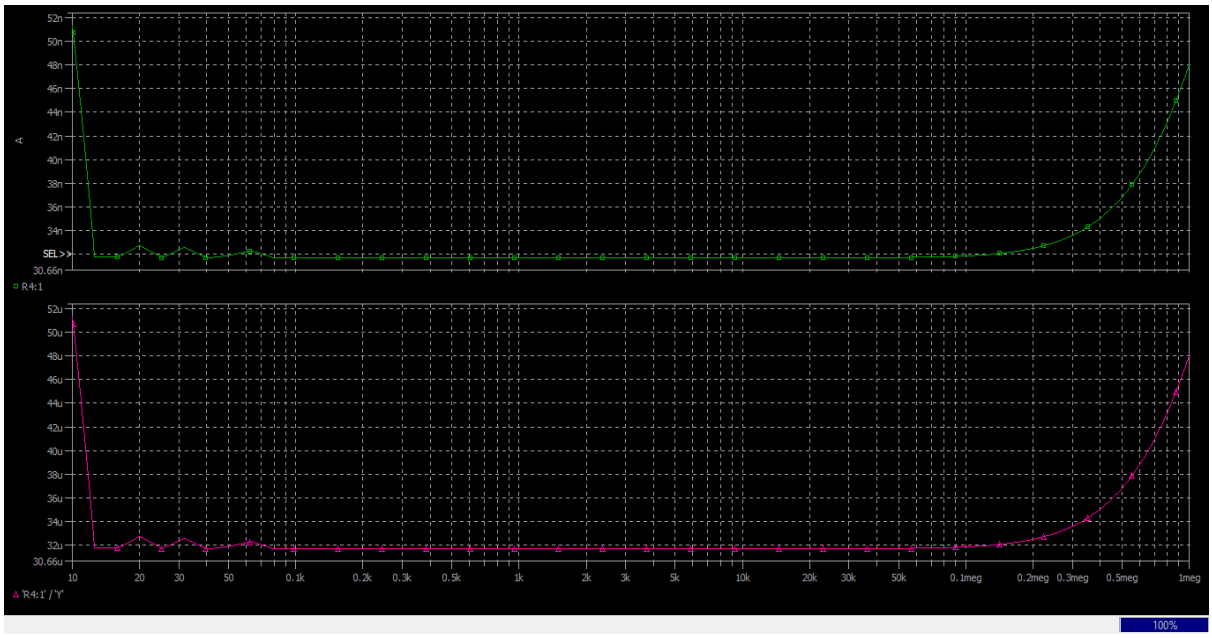
Plot 5.6 shows the trans conductance amplifier based upon OFCC Block

From Plot 5.6, observations are as follows: -

Trans conductance Gain = 31.7µS



Plot 5.5 Voltage Amplifier



Plot 5.6 Trans Conductance Amplifier

5.6.3 Current Amplifier

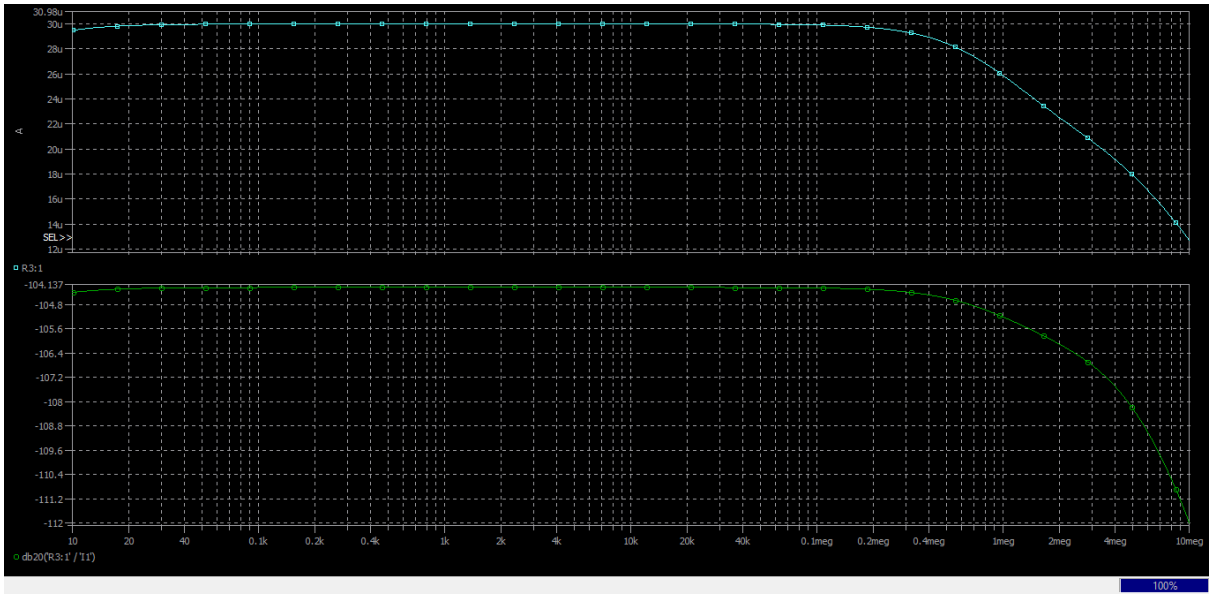
Simulation Environment: -

R1 = 10kΩ, R2 = 10KΩ

Input current, I_{IN} = 1mA @1KHz

Analysis type is AC analysis with frequency sweep from 10Hz to 10MHz. (10dB per decade)

Plot 5.7 shows the current amplifier based upon OFCC Block



Plot 5.7 Current Amplifier

From Plot 5.7, observations are as follows: -

Gain = 104.137 dB (approx.)

Bandwidth = 3MHz (approx.)

5.6.4 Trans Resistance Amplifier

Simulation Environment: -

R1 = 1kΩ

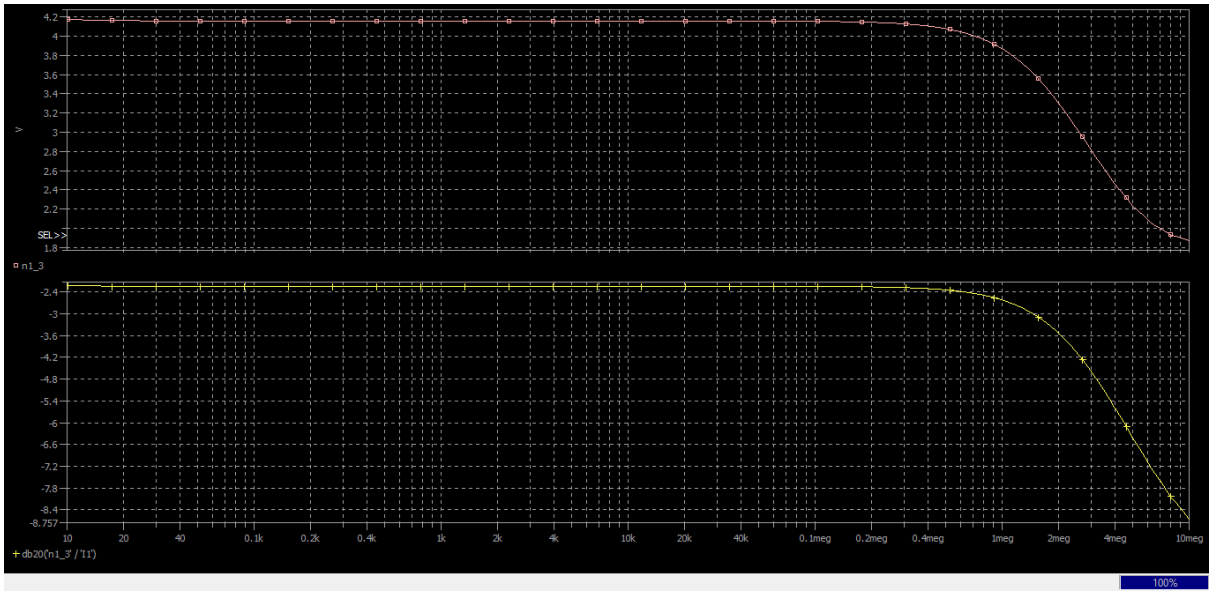
Input Current, I_{IN} = 1mA @1KHz

Analysis type is AC analysis with frequency sweep from 10Hz to 10MHz. (10dB per decade)

Plot 5.8 shows the trans resistance amplifier based upon OFCC Block.

From Plot 5.8, observations are as follows: -

Gain = 4.2kΩ



Plot 5.8 Trans Resistance Amplifier

5.7 Summary

This chapter introduces amplifier, their importance in electronic circuit. Then we have seen the different amplifier configuration using OFCC block. Later we have seen various plots associated with amplifiers.

CHAPTER 6: - FILTER IMPLEMENTATION

Filter is an electronic circuitry which can be used to separate the signals, depending upon there frequencies some signal is passed and unwanted signals are attenuated. In a cut short manner, it can be said that Filters are devices that filter signals based on their frequency. The impedance of capacitors as well as inductors depends upon the frequency that can be used to illustrate the basic notion of a filter. When we look at the impedance of inductors and capacitors it can be seen that their impedance depends upon the frequency, in case of inductor it is directly proportional and in case of capacitor its inversely proportional to frequency. Let's see an example for that, consider an example in which output is taken across the reactive element in a potential divider circuit. The value of the reactive impedance changes when the frequency is altered, and the voltage divider ratio varies as well. The frequency response is the result of this process, that is a frequency dependent change in the transfer function (output/input) . Figure 6.1 displays the ideal response of various filters.

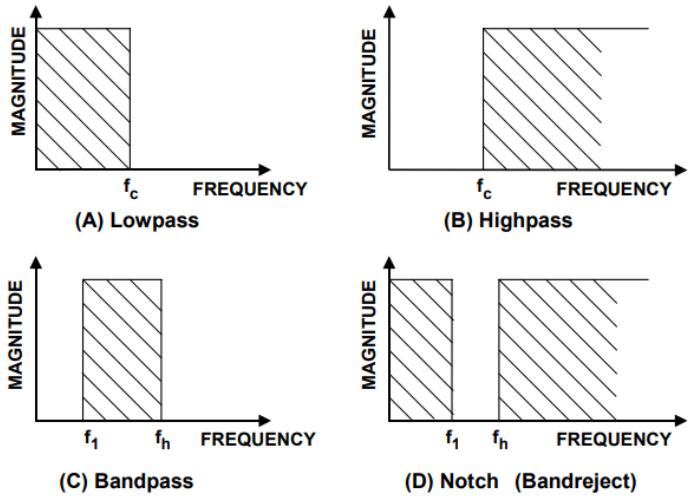


Fig.6.1 Ideal Filter Response (a) Low Pass (b) High Pass (c) Band Pass (d) Notch [30]

6.1 Filter Implementation using OFCC Block

[Nawwrocki and Klein] created the first operational trans conductance (OTAs) amplifiers-based active universal biquad filter. But due to low bandwidth and lower output driving capability OTA performance has been limited [15]. Despite of this fact, for integration purpose OTA was preferred because it has no resistors in the circuit. For these applications, alternative to OTA's are high performance current conveyors (CCs) due to their enhanced current driving capabilities and increased bandwidth. As previously said, the characteristics of OFC and CFB are combined in to OFCC [15, 20-22].

Figure 6.2 shows, the second-order active filter in its block level implementation having three inputs and an output.

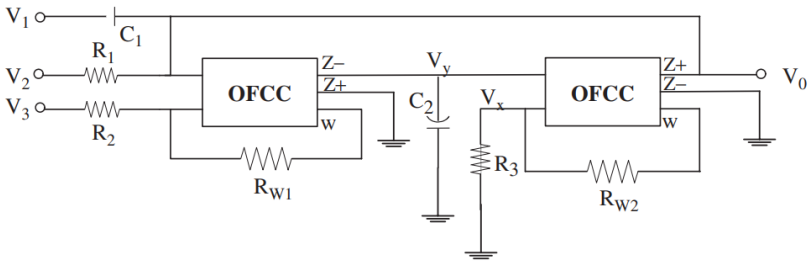


Fig.6.2 Active biquad filter [15]

The filter's transfer function is given by:

$$V_0 = \frac{V_1 S^2 C_1 C_2 + \frac{SC_2}{R_1} + V_3 \frac{1}{R_2 R_3}}{S^2 C_1 C_2 + \frac{SC_2}{R_1} + \frac{1}{R_2 R_3}} \tag{6.1}$$

expression 5.2 gives the Q (quality factor) and ω0 (natural frequency): -

$$\omega_0 = \left[\frac{1}{C_1 C_2 R_2 R_3}\right]^{1/2}$$
$$Q = R_1 \left[\frac{C_1}{C_2 R_2 R_3}\right]^{1/2} \tag{6.2}$$

The above filter configuration has been realised in a) TAM (Trnasadmittance Mode) b) VM (Voltage Mode) c) TIM (Transimpedence Mode) d) CM (Current Mode) and various filter response are present in their respective sections.

6.2 Schematic of OFCC Filter Implementation

Software Used = Symica DE

Technology Node = 130nm

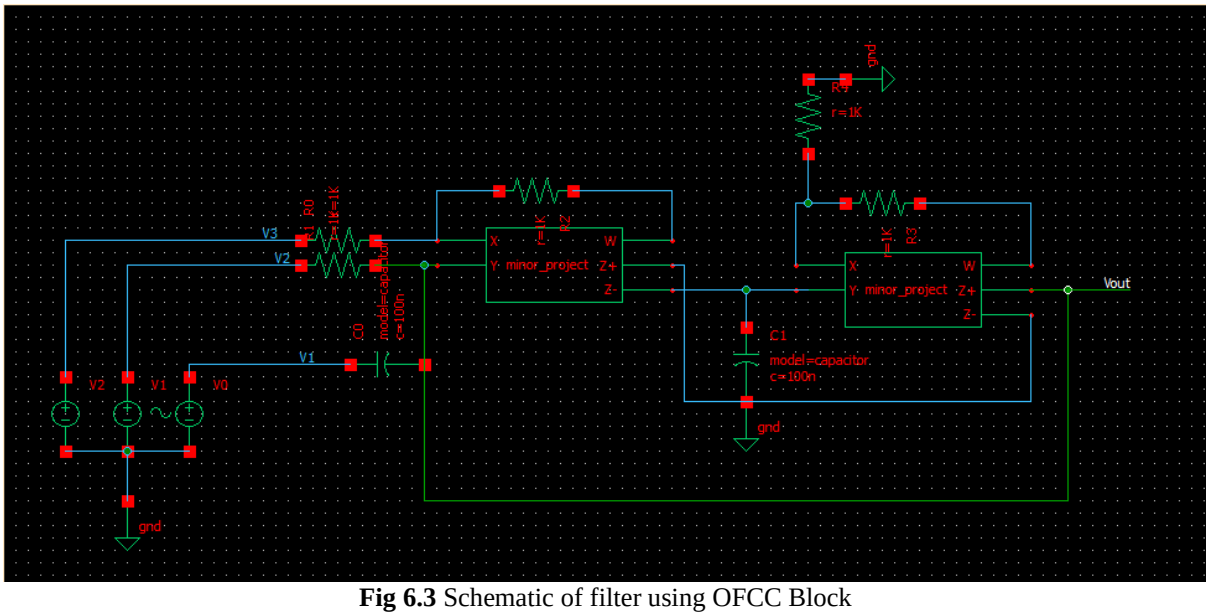


Fig 6.3 Schematic of filter using OFCC Block

6.3 Simulation results of Filter using OFCC Block in Voltage Mode

Schematic used for the simulation in voltage mode is depicted in Figure 6.3 and the different combination of voltage to apply and get the various filter response is shown in table 6.1.

Table 6.1 Sequence of input to obtain various filter configuration in voltage mode

Output Voltage and Filter response	Input Voltage		
Vout(Vo)	V1	V2	V3
High Pass	1	0	0
Low Pass	0	0	1
Notch filter	1	0	1

Simulation environment: -

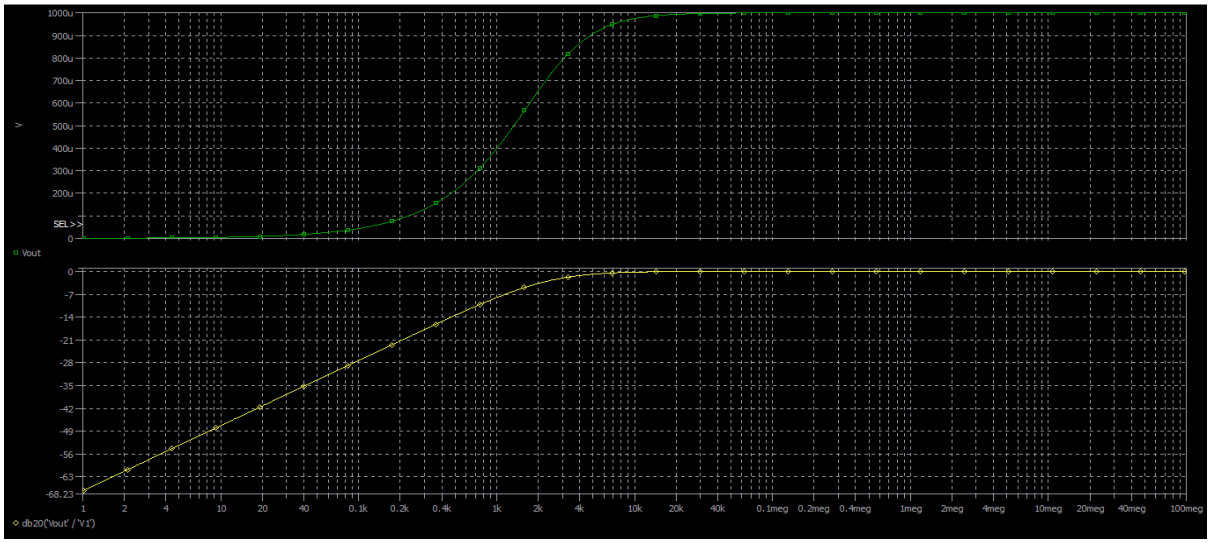
Different values of capacitors & resistors are as follows: -

R1 = R2 = R3 = 1KΩ, C1 = C2 = 100nF.

Input Voltage = 1mV @ 1KHz (depending upon response required, as mentioned in Table 6.1)

6.3.1 High pass filter

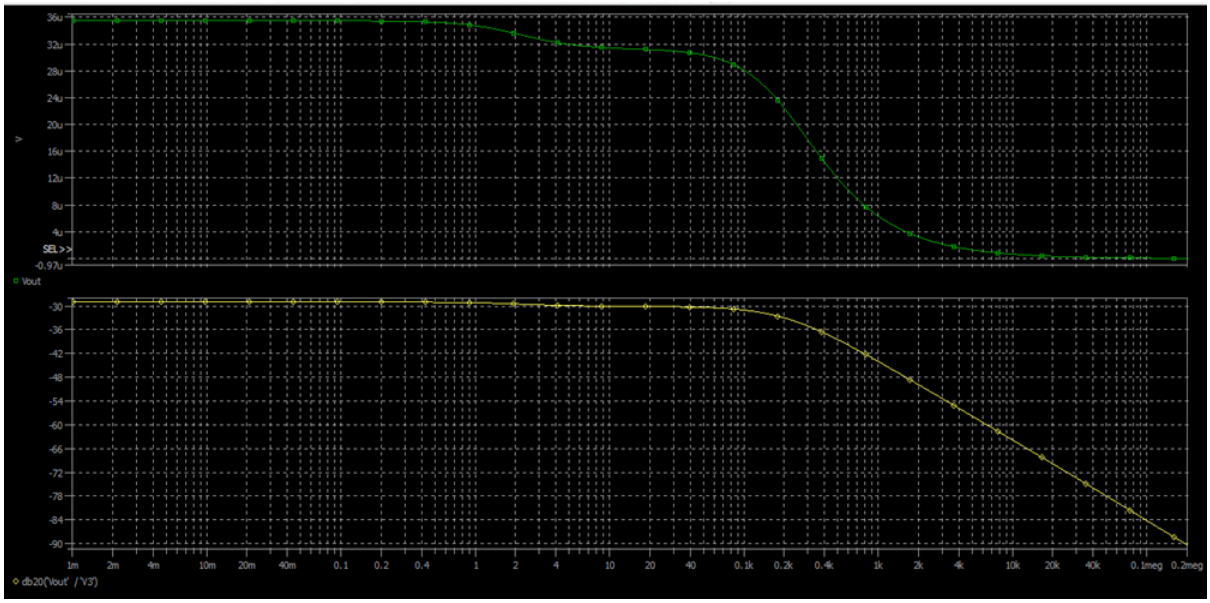
Plot 6.1 depicts the response of high pass filter using OFCC Block in voltage mode, as it can be observed from plot that it's attenuating the low frequencies but it is allowing high frequencies to pass through. In plot 5.1 the green colour plots shows output voltage and yellow one shown the gain plot (dB(Vout/Vin) w.r.t. frequency (varying from 1 Hz to 100 MHz) (Cutoff frequency = 3 KHz)



Plot 6.1 High Pass Filter

6.3.2 Low Pass Filter

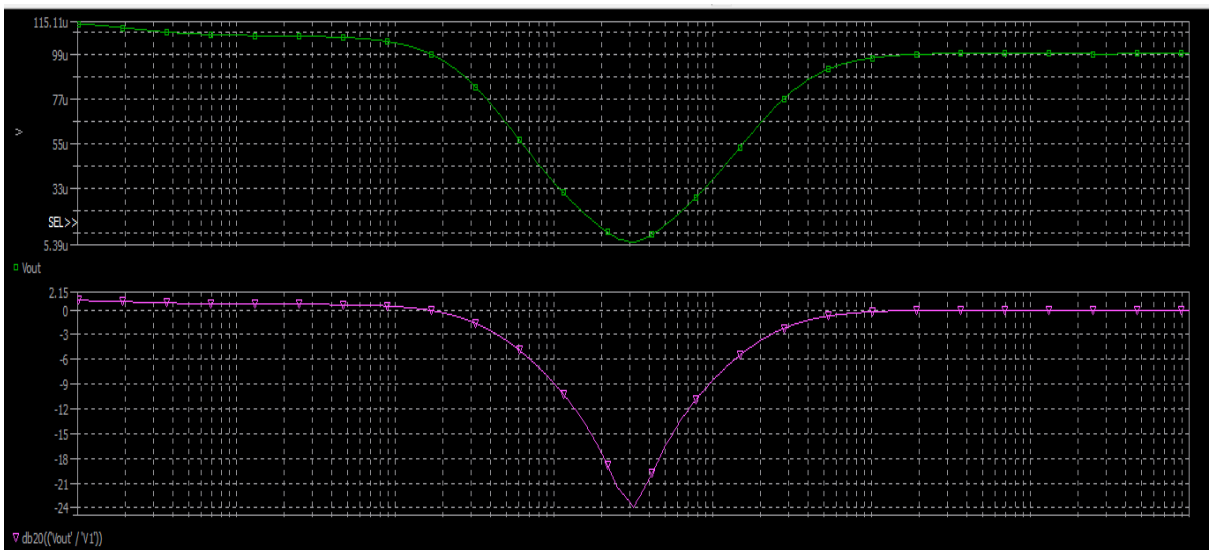
Plot 6.2 shows the response of low pass filter using OFCC Block in voltage mode, as it can be observed from plot that it's attenuating the high frequencies but it is allowing low frequencies to pass through. In plot 6.2, the green colour plots shows output voltage and yellow one shown the gain plot (dB(Vout/Vin)) w.r.t. frequency (varying from 0.001 Hz to 0.2 MHz). (for this filter R2's value is changed to 10KΩ and rest of the values remain same)



Plot 6.2 Low Pass Filter

6.3.3 Notch Filter

Plot 6.3 shows the response of notch filter using OFCC Block in voltage mode, as it can be observed from plot that it is attenuating a particular frequency, in frequency range which is around 3 KHz. In plot 6.3, the green plot shows the Vout v/s frequency and the pink one shows the gain plot (dB(Vout/Vin)) w.r.t. frequency (varying from 1 Hz to 10 MHz).



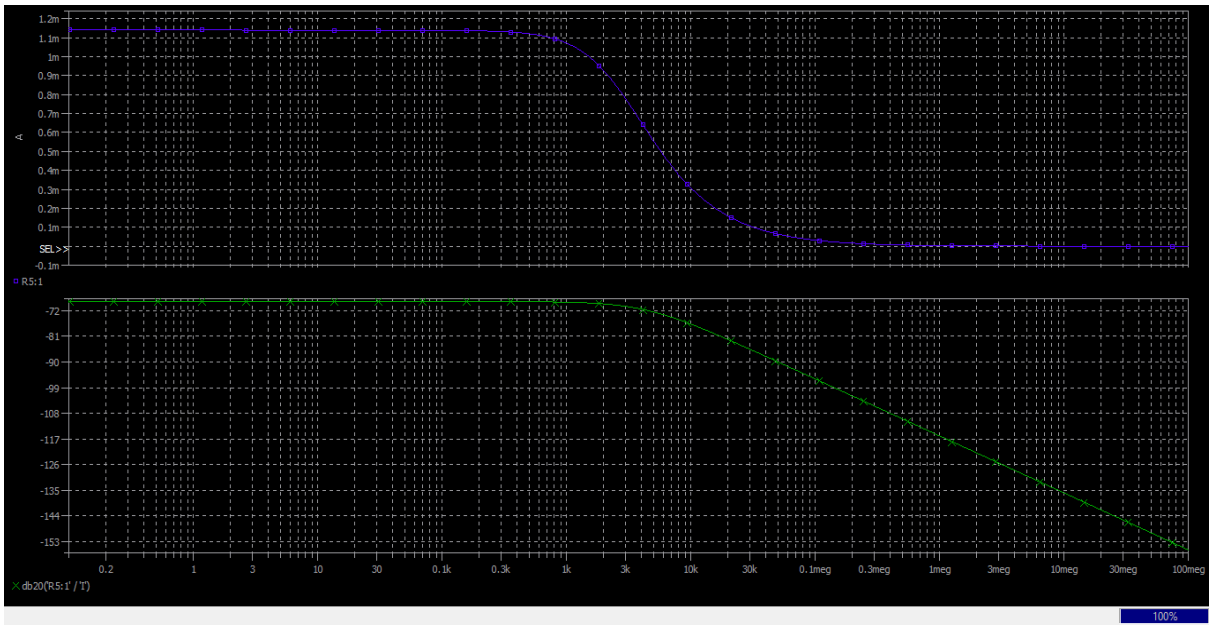
Plot 6.3 Notch Filter

6.4 Simulation results of Filter using OFCC Block in Current Mode

Plot 6.4 shows the low pass filter response of OFCC block in current mode and the input current is applied to Y terminal of first OFCC Block which is shown in Figure 6.3. To obtain the output current a resistor R of value 1KΩ is added at terminal Z+.

Input Current = 1mA @ 1 KHz

In plot 6.4, the blue colour plots shows output current and green one shown the gain plot (dB(Iout/Iin) w.r.t. frequency (varying from 0.1 Hz to 100 MHz). (Cutoff Freq. = 10 KHz)



Plot 6.4 Low Pass Filter

6.5 Simulation results of Filter using OFCC Block in Trans Admittance Mode

In this mode the output is taken in the form of current while input voltage is applied to OFCC. Schematic used for the simulation in trans admittance mode is depicts in Fig.6.3 and different combination of voltage to apply and get the various filter response is shown in table 6.2

Table 6.2 Sequence of input to obtain various filter configuration in trans admittance mode

Output Current and Filter Response	Input Voltage	
Iout	V1	V2
High Pass Filter	1	0
Low Pass Filter	0	1

Simulation environment: -

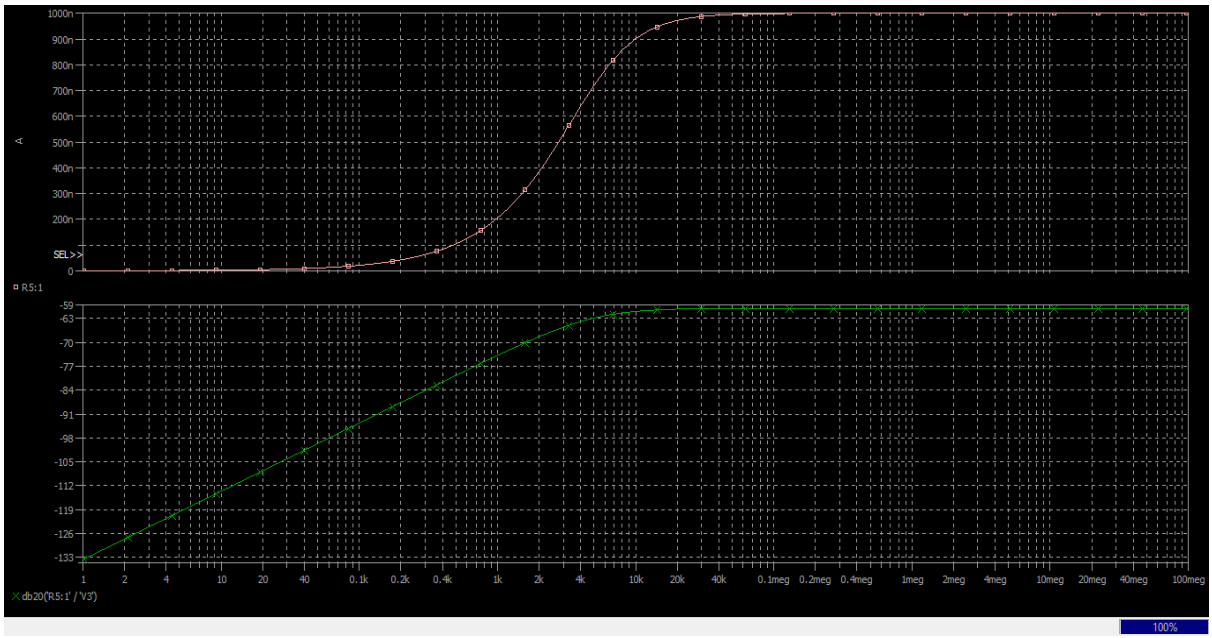
Different Values of resistors and capacitors are as follows: -

R1 = R2 = R3 = 1KΩ, C1 = C2 = 100nF.

Input Voltage = 1mV @ 1KHz (depending upon response required, as mentioned in Table 5.2)

6.5.1 High pass filter

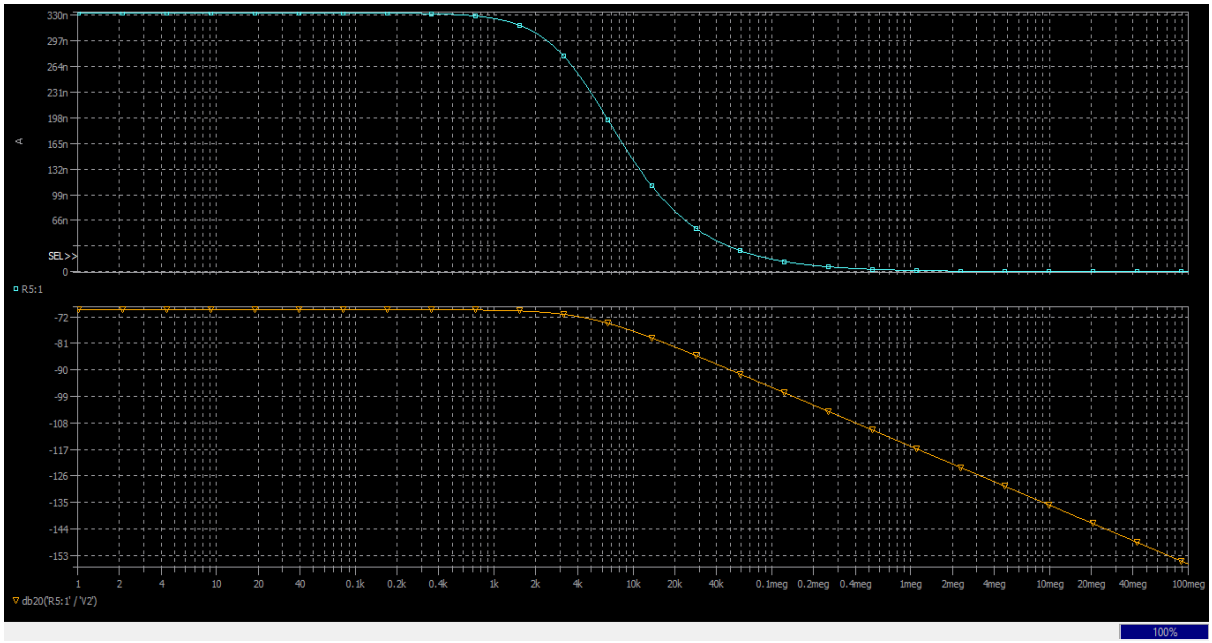
Plot 6.5 shows the response of high pass filter using OFCC Block in trans admittance mode, as it can be observed from plot that it's attenuating the low frequencies but it is allowing high frequencies to pass through. In plot 6.5 the orange colour plots shows output voltage and green one shown the gain plot (dB(Iout/Vin)) w.r.t. frequency (varying from 1 Hz to 100 MHz). (Cutoff Frequency = 6 KHz approx.)



Plot 6.5 High Pass Filter

6.5.2 Low Pass Filter

Plot 6.6 shows the response of low pass filter using OFCC Block in trans admittance mode, as it can be observed from plot that it's attenuating the high frequencies but it is allowing low frequencies to pass through. In plot 6.6, the blue colour plots shows output voltage and yellow one shown the gain plot (dB(Iout/Vin)) w.r.t. frequency (varying from 1 Hz to 100 MHz). (Cutoff Frequency of LPF = 10 KHz approx.)



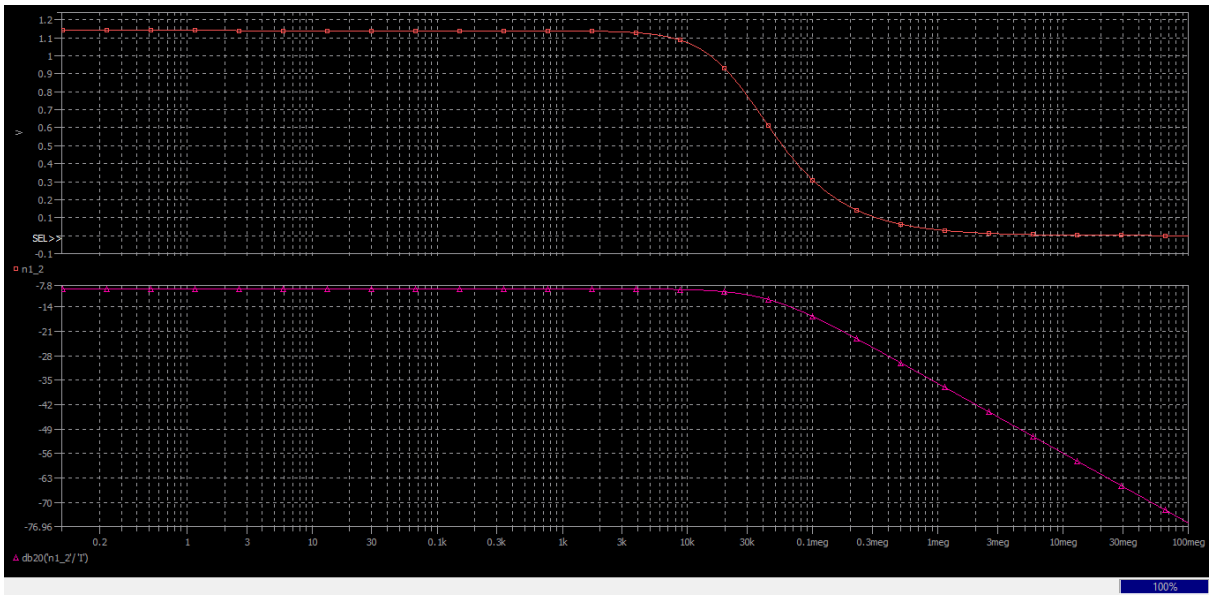
Plot 6.6 Low Pass Filter

6.6 Simulation results of Filter using OFCC Block in Trans Impedance Mode

Plot 6.7 shows the frequency response of low filter in trans impedance mode. In this mode of operation, the input current is applied to the terminal Y which is present in Fig.6.3 and the output is measured in terms of voltage which is mentioned as Vout in Fig.6.3.

Input Current = 1mA @ 1 KHz.

In plot 6.7, the orange colour plots shows output current and pink one shown the gain plot (dB(Vout/Iin) w.r.t. frequency (varying from 0.1 Hz to 100 MHz). (Cutoff Frequency = 20 KHz approx.)



Plot 6.7 Low Pass Filter

6.8 Summary

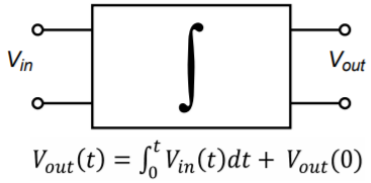
In this chapter we have the filter implementation using OFCC Block in different mode and their various responses are shown in their respective section. It's worth noting that in voltage mode high pass, low pass and notch filter are implemented, in case of current mode and in case of trans impedance mode low pass filter is implemented and in trans admittance mode low pass and high pass filter are presented. The observation is also present in their respective section. They are implemented in CMOS 130nm technology and AC analysis has been done using software Symica DE. Later we have seen that the comparison between filter implementation using other active block also it is presented in section 6.6.

CHAPTER 7: - INTEGRATOR & DIFFRENTIATOR

Integration and differentiation are the two fundamental operations of analog processing circuits; they have wide variety of applications in analog circuits. In earlier days these type of circuits is designed with opamp. But when the advancements came in analog electronics circuit design technique, CCs can now also be used to design these types of mathematical operation preforming circuits. In this chapter we will see the implementation of differentiator and integrator by using this new block of OFCC which is presented in [11].

7.1 Integrator

Many technical and engineering specific applications relies on the mathematical operation known as integration. Figure 6.1 depicts block diagram for the integrator block with its mathematical equation.



$$V_{out}(t) = \int_0^t V_{in}(t)dt + V_{out}(0)$$

Fig.7.1 Block diagram of Integrator [29]

From the equation shown in Fig.7.1 we can see that the output voltage (V_{out}) is equal to the integration of input voltage (V_{in}) over a time which is varied from t = 0 to some arbitrary time 't'. In simple words integrator defines the area under the V_{in} curve from time t = 0 to any arbitrary time 't' in a Vin(t) vs t plot. Now let's take a look at the implementation of integrator by using the OFCC Block which is described in chapter 4.

7.1.1 Schematic and Output Waveform of Integrator using OFCC Block

Fig.7.2 shows the schematic of integrator implemented using the OFCC Block which is described in chapter 4.

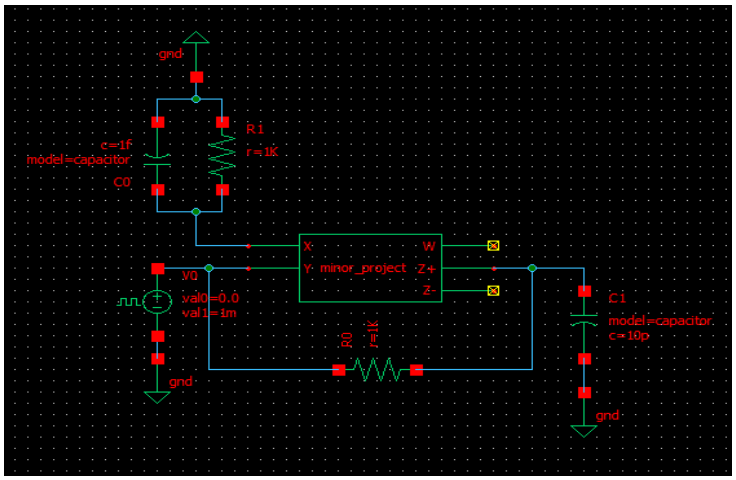


Fig.7.2 Schematic of Integrator

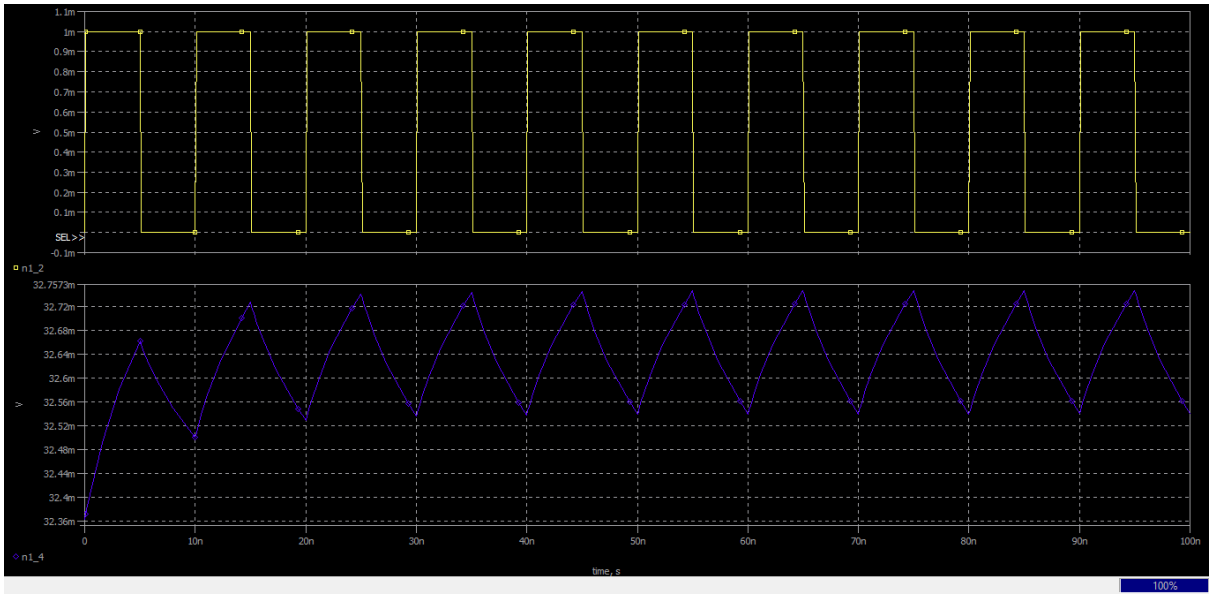
Simulation Environment: -

R0 = R1 = 1KΩ, C0 = 1fF, C1 = 10pF.

Input Voltage, V = (V0 = 0V, V1 = 1mV), with time period = 10ns.

Analysis type is Transient.

Plot 7.1 shows the variation of input voltage and output voltage with time over a period of 100ns.



Plot.7.1 Input and Output voltage waveform of integrator

From plot.7.1 the yellow colour plot shows the input voltage waveform which is of square type and the integration of square waveform is triangular waveform which is shown by blue colour plot and it the output of integrator.

7.2 Differentiator

Many technical and engineering specific applications relies on the mathematical operation known as differentiator. Fig.7.2 shows the block diagram for the differentiator block with its mathematical equation.

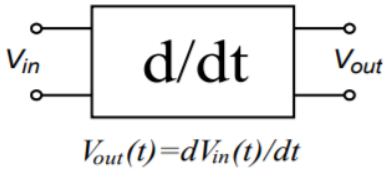


Fig.7.3 Block diagram of Differentiator [29]

From the equation shown in Fig.7.3 we can see, the output voltage (V_{out}) is equal to differentiation of the input voltage (V_{in}). In simple words differentiation can be defined as the rate of change of one quantity with respect to other, in this case the output voltage is defined

as rate of change of input voltage with respect to small change in time. Now let's take a look at the implementation of differentiator by using the OFCC Block which is described in chapter 4.

7.2.1 Schematic and Output Waveform of Differentiator using OFCC Block

Fig.6.4 shows the schematic of integrator implemented using the OFCC Block which is described in chapter 4.

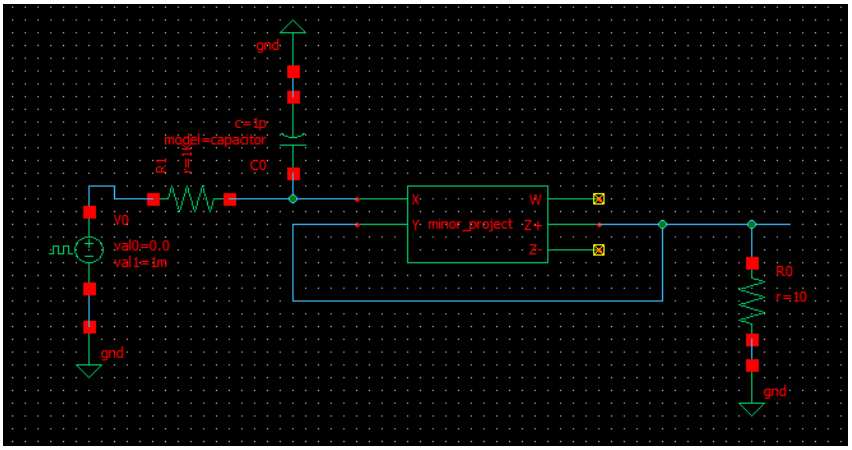


Fig.7.2 Schematic of Differentiator

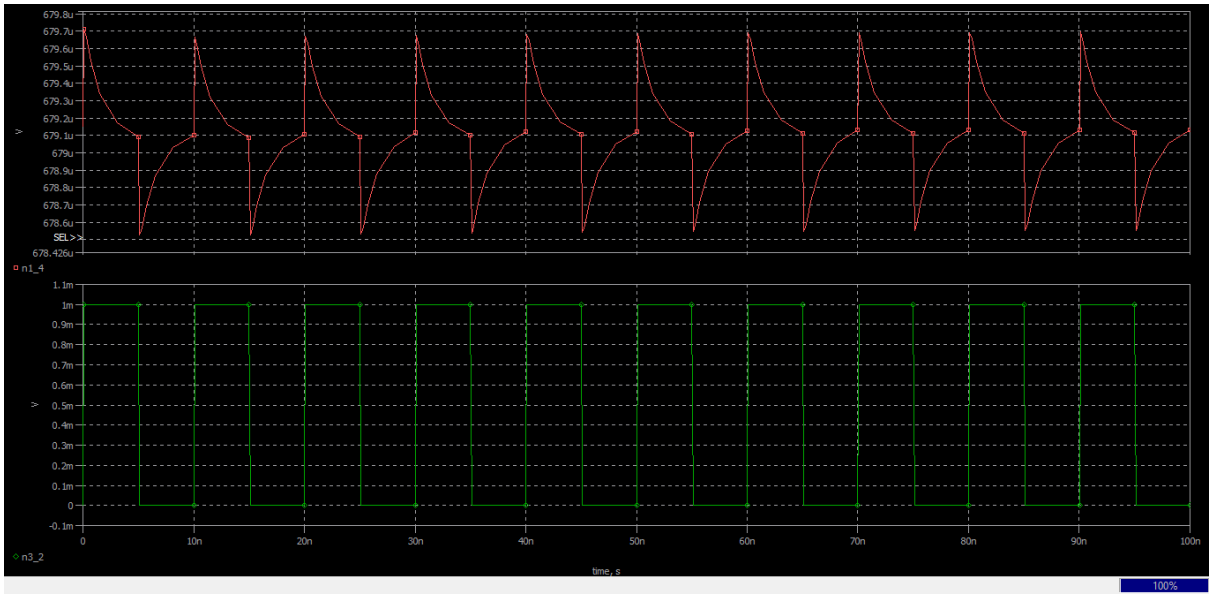
Simulation Environment: -

R0 = 10Ω, R1 = 1KΩ, C0 = 1pF.

Input Voltage, V = (V0 = 0V, V1 = 1mV), with time period = 10ns.

Analysis type is Transient.

Plot 7.2 shows the variation of input voltage and output voltage w.r.t time over 100ns period:-



Plot.7.2 Input and Output voltage waveform of differentiator

From plot.7.2 the green colour plot shows the input voltage waveform which is of square type and the differentiation of square waveform is impulse waveform which is shown by red colour plot and it the output of integrator.

7.3 Summary

In this chapter we have seen the implementation of integrator and differentiator using the new OFCC Block and that OFCC Block is proposed by [11]. The all the simulation results are also shown and the simulation is carried out at 130nm technology node by using the software Symica DE.

CHAPTER 8: - CONCLUSION & FUTURE SCOPE

The current conveyor (CC) concept was first introduced in 1968 and in 1970 second generation has been developed. A CC has various useful applications and it can be used as general building block for different applications. A CC is a minimum 3-terminals device, when paired with different electronic components like resistor, capacitor, transistor etc. in a circuit, it can perform a number of beneficial analog signal processing jobs. OFCC, is one of the famous and elementary building blocks which can be used to perform various analog processing function in terms of current. (second generation current conveyor) CCII± & CFOA (current feedback amplifier) are combined to form the OFCC (Operational Floating Current Conveyor) which makes it flexible analog block.

The primary goal of this thesis is to use this newly designed OFCC Block by [11] for low voltage application ant try to implement the different amplifier configuration and filter implementation and some mathematical operation like integrator or differentiator using this low power OFCC Block. The main chapter in which the OFCC Block, amplifier and filter implementation with their simulation results are present in Chapter 4,5 and 6. 0.4V DC supply voltage is used to give supply to this OFCC block and for amplifier and filter implementation too same supply voltage is used. The simulation for OFCC block has been done in CMOS 90nm and 130nm technology node and also the amplifier using this block is implemented for both the CMOS technology node using software Symica DE, their respective simulation graphs are present in chapter 4 and chapter 5.

Chapter 6 shows the filter implementation using this low power OFCC Block. Filters are implemented in different modes. In voltage mode this OFCC block can be used to realized only low pass, high pass and notch filter, in current mode and also in trans impedance mode only low pass filter is realized and in trans admittance mode only low pass and high pass filter are realized further research can be extended or circuit can be modified in such a way that this OFCC Block proposed by [11] can also be used to implement other remaining filter responses for different modes of operations and maybe in future this block can also be used in other anlog applications.

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