# STUDY OF GaN-BUFFERED TRENCH GATE MOSFET: A TCAD NUMERICAL STUDY

A DISSERTATION

SUBMITTED IN PARTIAL FULFILLMENT OF THE

REQUIREMENTS

FOR THE AWARD OF THE DEGREE

for

## MASTER OF TECHNOLOGY

in

**Control & Instrumentation**

Submitted by:


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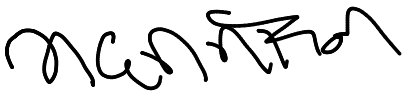
**2K19/C&I/09**


Under the Supervision of

**Prof. M.M. Tripathi**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I, SHREYA SAHU, Roll No. 2K19/C&I/09 student of M. Tech (Control and Instrumentation), hereby declare that the Project dissertation titled **"STUDY OF GaN-BUFFERED TRENCHED GATE MOSFET"** which is submitted by me to the Department of Electrical Engineering, Delhi Technological University in partial fulfillment for the award of the degree of Master of Technology is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship, or other similar title or recognition.

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## CERTIFICATE

I, SHREYA SAHU, Roll No. 2k19/C&I/09 student of M. Tech. (Control and Instrumentation), hereby declare that the dissertation/project titled "STUDY OF GaN-BUFFERED TRENCHED GATE MOSFET: A TCAD Numerical Study" under the supervision of Prof. M.M. Tripathi of Electrical Engineering Department Delhi Technological University in partial fulfillment of the requirement for the award of the degree of Master of Technology has not been submitted elsewhere for the award of any Degree.

(M.M. Tripathi)

Signature of Supervisor

Date: 08-Aug

Place: Delhi

Signature of Student

Date: 08-Aug

Place: Delhi

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## ACKNOWLEDGEMENT

I would like to express my gratitude towards Prof M.M Tripathi (Professor), Dr. Ajay Kumar who have contributed their precious time and effort to help me without whom it would not have been possible for me to understand and complete the project.

I would like to thank Prof. M.M. Tripathi (Professor), DTU Delhi, Department of Electrical Engineering, my Project guide, for supporting, motivating, and encouraging me throughout this work. His readiness for consultation always, his educative comments, his concern, and his assistance even with practical things have been invaluable.

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# ABSTRACT

This Project presents T-CAD simulation of GaN-buffered trench gate MOSFET (GaN-BTG MOSFET). We investigated the numerical simulations on GaN-BTG MOSFET for the suppression of SCEs and the effect of the high-k buffer on the linearity/analog performance and Low-power applications.

Different electrical characteristics and linearity/analog parameters; drain current (Id), transconductance ($g_m$), higher order transconductances ($gm_2$, $gm_3$) O/P conductance ($g_d$), transconductance generation factor (TGF), $2^{nd}$ and $3^{rd}$ order of Voltage Intercept point, $3^{rd}$ order of Current Intercept Point, 1-dB Compression Point, $3^{rd}$-order Intermodulation Point, $2^{nd}$ and $3^{rd}$ orders of Harmonic Distortion Point have been analyzed.

From the simulated results obtained, we have found that the use of elevated-k buffer remarkably improves the electrical as well as analog figure of merits (FOMs) of the device while linearity parameters for Low-power applications needs more investigation. Thus, the GaN-BUFFERED TRENCH GATE MOSFET can be considered as suitable candidate in digital and analog Ckt. applications.

Results recommend that the introduction of GaN instead of silicon in a trenched gate structure not just improves the device's performance at room temperature (300K) yet additionally enhances the thermal stability of the device. The simulations are observed and are supported by the data presented in the results section which are being performed using TCAD tool ATLAS and Deckbuild.

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# LIST OF SYMBOLS AND ABBREVIATIONS

| S.No. | PARTICULARS |
|---|---|
| 1. | TCAD: Technology computer-aided design |
| 2. | MOSFET: Metal oxide SC field effect Tx. |
| 3. | CTG MOSFET: Conventional trenched gate MOSFET |
| 4. | BTG MOSFET: Buffer trench gate MOSFET |
| 5. | GaN-BTG MOSFET: Gallium nitride buffer trenched gate MOSFET |
| 6. | $t_{ox}$: oxide thickness |
| 7. | $g_m$: transconductance |
| 8. | $I_d$ : Drain current |
| 9. | $V_{gs}$: Gate to Source Voltage |
| 10. | $V_{ds}$: Drain to Source Voltage |
| 11. | $L_g$: Gate Length |
| 12. | $HfO_2$: Hafnium Oxide |
| 13. | $SiO_2$: Silicon dioxide |
| 14. | $V_{th:}$ Threshold Voltage |
| 15. | $L_{ch}$: Channel length |
| 16. | SCEs: Short Channel Effects |
| 17. | EF: EF |
| 18. | DIBL: Drain induced barrier lowering |
| 19. | $I_s$: Saturation current |
| 20. | $R_{on}$: ON Resistance |
| 21. | $V_{BD}$: Breakdown Voltage |
| 22. | SC: Semiconductor |
| 23. | Tx.: Transistor |
| 24. | Ckt.: Circuit |

# CHAPTER- 1

## INTRODUCTION

### 1.1 BACKGROUND

A SC is a material whose electrical properties lie b/w the insulators and conductors. The elements used in the SC are the fourth group elements like Germanium and Silicon whose forbidden gap is very small of the order of 0.7eV and 1.1eV respectively. Example: GaAs, Ge, Si are the most used whereas Si is used in electronic Ckt. fabrication [1].

Depending upon the working, SC can be classified into two types:

- INTRINSIC SEMICONDUCTOR:
  A SC which is in its extremely pure form is known as Intrinsic SC where electrons and holes are solely created by thermal excitation. Electrical conductivity is low also it depends on temperature.
- EXTRINSIC SEMICONDUCTOR:
  A SC which is in a little quantity of pentavalent or trivalent impurity atoms are added is known as Extrinsic SC. Electrical conductivity is elevated also it depends on temperature and impurity.

Depending upon the impurity the SC is of two types:

- P-type:
  When in SC a least quantity of trivalent impurity.
  Eg: B, Ga or In is added to pure SC then the resultant is P-type SC where holes are the majority carriers and electrons are the minority carriers.
- N-type:
  When in a SC a least quantity of pentavalent impurity.
  Eg: Sb, P, Ar is added to pure SC then the resultant is N-type SC where electrons are the majority carriers and holes are the minority carriers.

## Use of Semiconductor:

- For electronic component several combinations of P-type and N-type SCs are utilized.
- For diodes which is also used as a rectifier a combination of p-type and n-type SCs are utilized.
- For Tx. one type of SC is placed b/w two layers of other type of SC.
- Tx. and MOSFET used as a switch.

## Properties of Semiconductor:

- At 0 K, SC acts as an insulator; as temperature escalates it acts as conductor. SC have elevated resistivity than conductor but less than insulation. Increment in temperature leads to decrement in resistance of SC and vice-versa.
- SC have less power losses.

## Applications of Semiconductor:

For various purposes; SC's low cost, reliability, controlled condition of electricity makes it ideal for wide-range of computations and devices like diodes, Tx., IC, microcontroller.
SC devices are the driving force in today's global economy and one of the most dynamic sectors. The structure of the SC industry can be discussed in a pyramid.

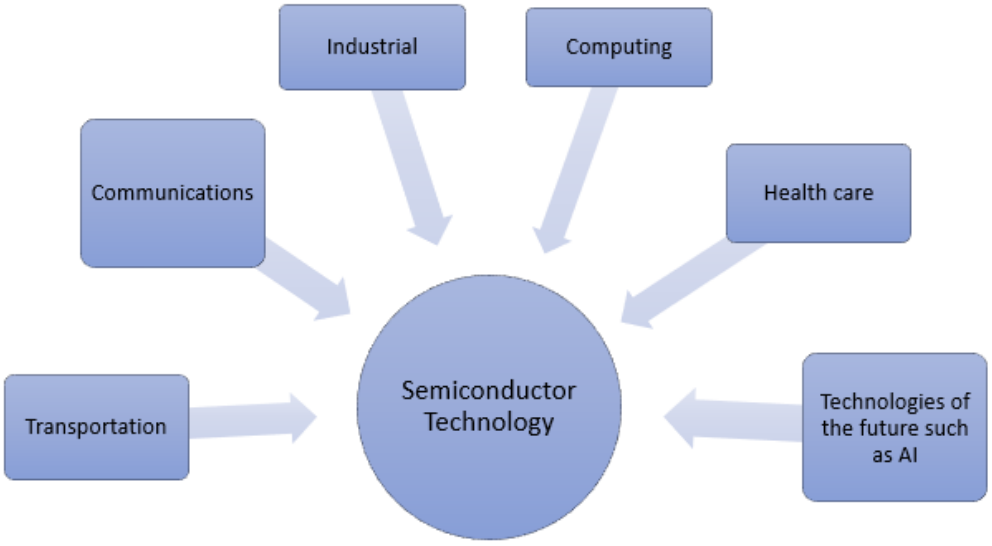


Fig 1: Applications of SC technology

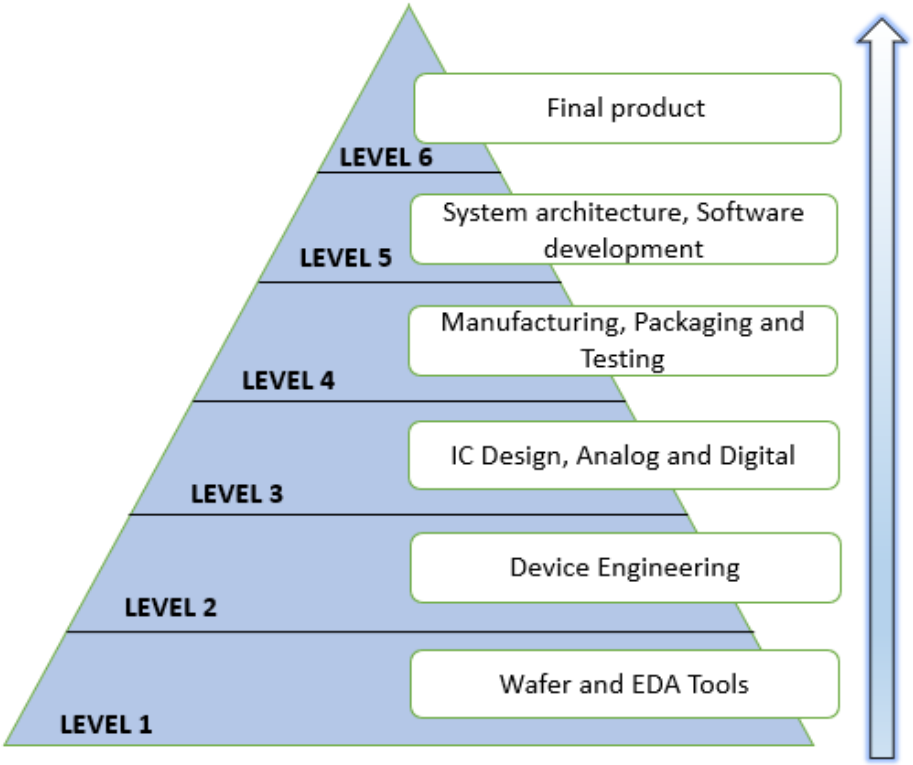


Fig 2: Different levels of SC devices manufacturing

## 1.2 TRANSISTOR ACTION

The word Tx. was invented by Shockley in 1947, Brattain. The Tx. is a device where the resistance b/w the 2-terminals is governed by voltage/current at the 3-terminal.

In the era of nanotechnology, the discovery of Bipolar Junction Tx. (BJT) in 1948 brought a drastic change in the field of electronics. BJTs can be still used in the elevated-frequency Ckt.s. For e.g., RF Ckt.s [1-3]. In the SCs industry, MOSFET is the base of most of the IC applications since 1959, where a new dimension of origination was discovered, and since then, various researchers have prospered this technology, and once such embellishment was scaling down device's dimension in accordance with the Moore's Law, also elevated-performance Tx.s with improved packaging density which can correlate with the size reduction.

Generally, MOSFETs take effect as switches in IC. However, not the ideal switches (believed to absorb NO power) in OFF state, delivers an elevated current in no time in ON state. A slight amount of $I_{OFF}$ is present also even when it is switched OFF as it consumes power from the supply. And this is the static power dissipation ($P_s$) [2].

$$P_S = V_{DD} \times I_{OFF}$$

where $V_{DD}$ ($V_s$) and $I_{OFF}$ (leakage current) percolates the Tx. even when the switch is OFF. Also, it consumes remarkable amount of power when it is switched ON from OFF or vice-versa. Here, the power consumption is the dynamic power dissipation ($P_d$), depends upon the frequency of switching.

$$P_D = V_{DD}^2 \times C_L \times f_\alpha$$

Where, $\alpha$ is switching probability, $C_L$ is load capacitance and $f$ is frequency of operation.

# CHAPTER -2
## MOS TRANISTOR STRUCTURE AND OPERATION

### 2.1 METALLIC- OXIDE-FIELD-EFFECT TRANSISTOR:

In MOSFET, MOS Capacitor-core of MOSFET grasps the notion of "field-effect". The field-effect described as governing the charge dynamics with the help of an EF [2].

The MOS Capacitor as the name suggest it consists of three layers: metal-oxide-SC. B/w the metal and SC there is an insulating layer. The MOS Capacitor doped with an N-type SC or with a P-type SC is called N-type MOS Capacitor & P-type MOS Capacitor respectively. Through gate voltage capacitance of the MOS structure might be governed. Occurrence of charge dynamics happens at the surface of MOS devices. As, Si-$SiO_2$ interface comprises the finest variety SC-insulator interface, Si- the most preferred material for MOS devices.

### 2.2 MOSFET STRUCTURE:

The MOS Tx. comprises of a SC substrate generally Si, "thin layer of insulating oxide" grown ($SiO_2$) [thickness:80-1000Å]. The gate electrode which is deposited above oxide layer is conducting layer used made of poly silicon. The source and drain which is densely doped (0.1-1µm) formed on the substrate on each side of the gate which slightly overlaps gate. Two p-n junctions are formed back-to-back equivalent to source-drain electrodes and the region b/w drain and source junctions called the channel region. MOS Tx. is a four-terminal device from Ckt. model which are designed as gate(G), source(S), drain(D) and substrate or bulk(B). The role of D and S is defined after applying the terminal voltage.

EF due to applied voltage at the G terminal, governs the flow of charge carriers in the channel region b/w other terminals; S and D. The device is designated as MOS Field-Effect-Tx. (MOSFET) [3-6] as the its current is controlled by the EF, so-called as an Insulated-Gate-Field-Effect-Tx. (IGFET) as the gate is electrically isolated from other two electrodes.

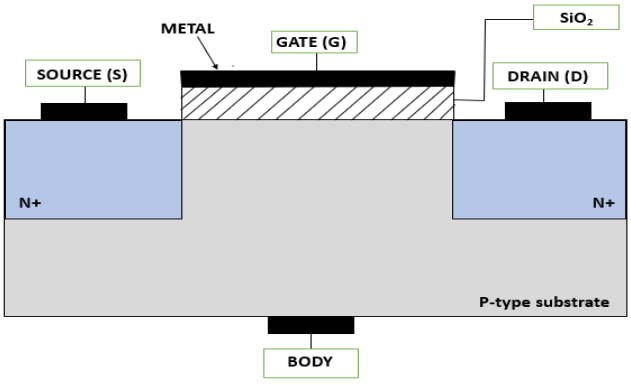


Fig 3: MOSFET Structure

## 2.3 OPERATING MODES:

MOSFET is mainly defined into two types in terms of fabrication:

### 1. N-Channel MOSFET (NMOS):

The NMOS is a 4-terminal device in which N-channel region is situated in b/w the S and D terminals. In this type of FET, S and D are densely doped $n^+$ region whereas body is P-type. When voltage greater than zero is applied with repulsive force at the G terminal, the holes which are existing underneath the oxide-layer forced towards the B. In NMOS current flow is due to electrons.

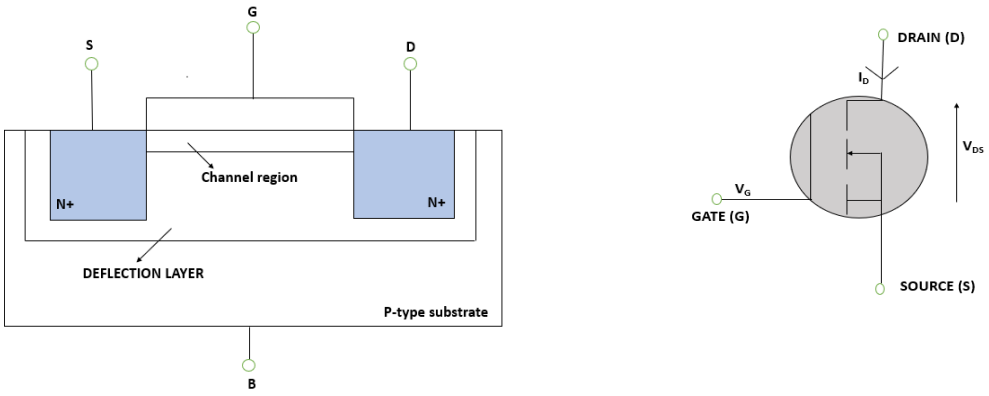


Fig 4: NMOS Structure and Symbol

### 2. P-Channel MOSFET (PMOS):

PMOS is a 4-terminal device which has a P-channel region positioned in b/w the S and D terminals. In this type of FET, S and D are densely doped $p^+$ region where body is n-type. [4-6] When negative voltage is applied with repulsive force at the G terminal, the electrons which are existing below the oxide-layer pushed towards substrate. In PMOS current flow is due to holes.

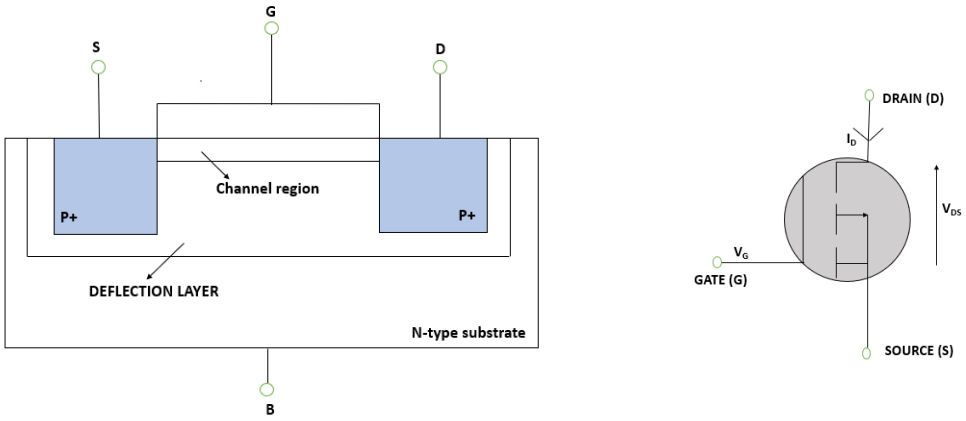


Fig 5: PMOS Structure and Symbol

MOSFETs can be further classified, defining the fundamental mode of operation of MOSFETs:

- **ENHANCEMENT MOSFET-**
  It is a type of MOSFET where there is no channel constructed during fabrication, but it can be induced in the substrate using the gate voltage. Enhancement MOSFET or E-MOSFET does not conduct at no zero-gate voltage ($V_{GS}$). Therefore, there is no path for the conduction b/w S and D and is described as normally OFF Tx.
- **DEPLETION MOSFET-**
  In this MOSFET the channel is constructed while fabrication. Depletion MOSFET or D-MOSFET can conduct b/w S and D when the $V_{GS}$=0V. Therefore, Depletion-MOSFET is called normally ON Tx.

The Depletion-MOSFET and Enhancement-MOSFET can be N-channel or P-channel on the basis of channel used. The type of channel also affects its speed, biasing as well as current capacities.

| | | GATE VOLTAGE | |
|---|---|---|---|
| **DEVICE TYPE** | **NORMAL STATE** | **N-channel** | **P-channel** |
| Enhancement mode | OFF | $+V_g$ turns ON | $-V_g$ turns ON |
| Depletion mode | ON | $-V_g$ turns OFF | $+V_g$ turns OFF |

Table 1: Four different types of MOSFETs

## 2.4 Transfer Characteristics and O/P Characteristics:

The Transfer Characteristics refers; the relationship b/w O/P current ([$I_d$]) and the I/P voltage [$V_{gs}$] for a specific $V_{ds}$(drain voltage). The $I_d$ is minimal below threshold voltage governed by the diffusion of carriers from D to S region. As soon as $V_g$ escalates above the $V_{th}$ an inversion layer is formed and the $I_d$ escalates notably.

The O/P characteristics refers to the relationship b/w the O/P current and the O/P voltage for a particular $V_{gs}$. The $I_d$ first escalates linearly with $V_{ds}$ & further gets saturated owing to the pinch-off of the channel region at D end. The inversion escalates with increment in $V_{gs}$ resulting in higher $I_d$. [6]

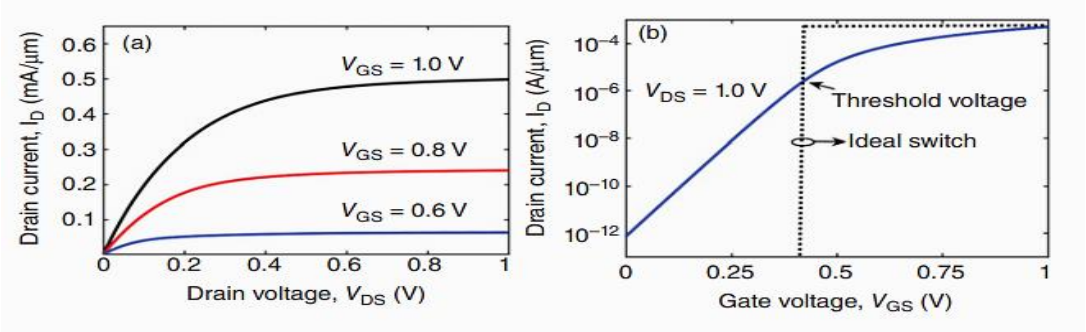


Fig 6: (a) O/P Characteristics and $I_d$-$V_g$ Characteristics (b) in Log scale.

# CHAPTER-3

## SCALING- *Good things come in small packages*

MOSFET miniaturization helped the microelectronics industry since last 3 decades. The continuous strive for scaling down the dimensions of MOSFET allows the industry to put millions of Tx. on a single chip. Due to escalated advantageousness and minimal cost of large variety of IC and systems lead to its advantages for the consumers and essentially the SC industry.[7] The reduced cost of manufacturing, increment in data transfer speed, enhanced computer processing power and multitasking concurrently are some of the benefits gained because of Tx. scaling.

### 3.1 THE NEED FOR CMOS SCALING:

In digital Ckt.s like microprocessors operates at elevated frequency (-GHz range), the dynamic power significantly contributes in net power consumption. The static power dissipation relies on the $_{Vs}$ ($V_{DD}$) and the $I_{OFF}$. Therefore, a decrement in $V_{DD}$ or $I_{OFF}$ can lead to reduction in static power dissipation. The dynamic power dissipation relies on $V_{DD}$, $f$, α, $C_L$., where α relies on the functioning of the digital Ckt. which cannot be modified also the frequency f requires to be elevated for the speedy consumption rate. Thus, the power dissipation can be reduced by lowering $C_L$ and drain voltage. For optimum switching operation the ratio [ $I_{ON}/I_{OFF}$] must be at the minimum $10^4$, as fall in the $V_s$ will further reduce $I_{ON}/I_{OFF}$ ratio because of limit on subthreshold swing.

$C_L$ is the load capacitance or the I/P capacitance of similar logic Ckt.s which might get reduced by scaling down the dimensions of MOSFETs.

### 3.2 MOSFET SCALING:

Throughout the last 2 decades, the dimensions of MOS Tx. have been scaled down systematically to achieve increased Ckt. density and performances (increased switching speed and reduced dissipation in power). Dennard proposed the rules of scaling for reduction in the size of the device while not disturbing the current-voltage behavior of the MOSFET. According to G. Moore's article, "Cramming more components onto Integrated Ckt.s." By 1975 it will become certain to accommodate $6.5\times10^4$ components onto a single chip, provided the number of active Tx. per chip doubled roughly every year. These days, there are approx. half a billion Tx. integrated on single microprocessor as shown in Fig 7.

According to scaling rule, all vertical as well as horizontal device dimensions (device's length-L, width-W, gate-oxide thickness-$t_{ox}$ and S/D junction depth-$X_j$) and voltages; also scaled down by a factor $\kappa > 1$, described as the scaling factor, while doping concentrations $N_b$ also improved by the same factor.

Thus, scaling of MOSFET's $L_g$ leads to reduction in capacitance and permits elevated-frequency operation while escalating the no. of Tx. and performance in each chip area [8,9]. CMOS scaling is the most appropriate method to achieve elevated efficiency in power and elevated-speed multifunctioning device.

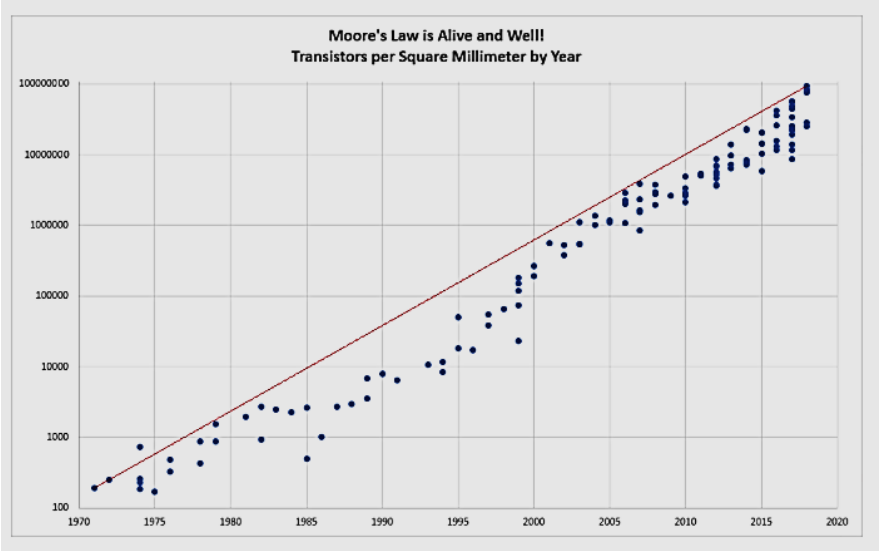

Fig 7: Moore's Law: The numeral of Tx's integrated in a commercially available processor.

There are two types of scaling. Theory and features of both type of scaling are given below:

- **Constant Field Scaling:**
  For reducing linearly, the dimension of the Tx. with the $V_s$ in an attempt to improve the functioning of a MOSFET also with increase in doping concentrations in such a way to keep the EF constant - henceforth "constant field scaling".
  The scaling is done by a linear transformation of 3 design parameters (voltage, doping concentrations, and physical dimensions) of a particular gen. of Tx. by the scaling factor κ. This constant field scaling results in decrement in the power-delay product of a single Tx. nevertheless, this needs a fall in power $V_s$ all together reduces the lowest feature size.
- **Constant Voltage Scaling:**
  Since, the aforementioned method delivers voltage compatibility with older Ckt. technologies do not have a problem of reduction in power supply. The disadvantage is, the EF escalates as the length is decreased which further saturates velocity, degrades mobility, escalates leakage currents and fall in breakdown voltages.
  In general, scaling of voltage (V) and gate oxide thickness scaling is done by a factor of β and other linear dimensions scaled by factor of α.

### 3.3 PROBLEMS WITH SCALING OF MOSFET:

1. If the power supply voltages are kept constant, the internal EFs in the device would increase.
2. The transverse EFs and the longitudinal EFs across the gate oxide escalates with MOSFET scaling.
3. With an escalation in temperature in the device, formation of hotspots occurs which can damage the MOSFET.
4. Problems known as hot carrier effects and SCEs.

The basic problem of scaling in MOSFETs is the scaling limits imposed by the gate-oxide thickness ($t_{ox}$). As the $L_{ch}$ decreases, $t_{ox}$ also decreases in order to maintain proportionality. However, decreasing the $t_{ox}$ possesses the problem of quantum mechanical tunneling which further leads to the G $I_{OFF}$ with the decrease in insulating capabilities of gate-oxide. However,

with this the gate capacitance decreases by decreasing the current driving capabilities of the device. Therefore, we need to increase the physical oxide thickness keeping in mind to maintain the electrical thickness at the same time. This problem is alleviated by using Elevated-K dielectric stack as gate insulator instead of using $SiO_2$ as the gate-oxide.

### 3.4 Challenges in scaling the MOSFET:

Scaling of the MOSFETs till the sub nanometer range, in long channel devices i.e., the devices in which $L_{ch}$ is largely compared to the depletion regions formed at the S and D junctions, the D has minimal effect on the channel characteristics and the device's ON or OFF is decided by the gate only.[7] In other words, the direct coupling b/w the D and S is negligible in long channel devices however, as the $L_{ch}$ approaches the nm dimensions, the D starts influencing the channel formation which is known as SCE. The depletion region width at the S-channel and channel-D interface, the doping concentrations of S/D region is $N_D=10^{20}$ $cm^{-3}$ and channel is $N_A=10^{16}$ $cm^{-3}$. As the $L_{ch}$'s are scaled down, various physical occurence emerge and reduces the functioning of MOSFETs.

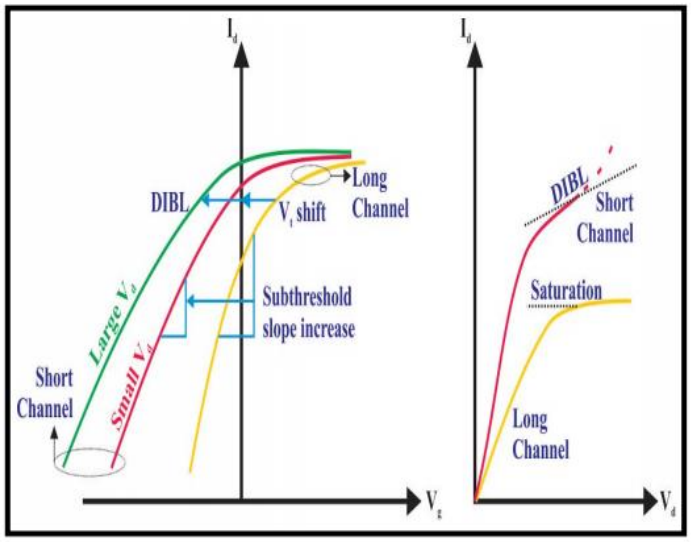


Fig 8: Impact of SCEs on $I_d$-$V_g$ characteristics of a MOSFET [13]

# CHAPTER-4
## SHORT-CHANNEL EFFECTS

If $L_{ch}$ is of the identical arrangement of vastness as well as depletion layer widths of S and D junction then device is short. As the $L_{ch}$ is decreased to enhance both the no. of components as well as operational speed, the SCEs arise [10].
The SCEs dominates the performance of MOSFETs and are allocated to two reasons:

- The electron-drift characteristics in the channel are imposed minimally.
- Due to shortening of $L_{ch}$ the modification of $V_{th}$.

Five different SCEs can be distinguished:

### 4.1 Threshold Voltage Roll-Off:

The S/D region extend into the P-channel and get exhausts at the channel-drain & source-channel interface, when depletion regions have elevated doping in a MOSFET. The D/S-induced depletion region widths are a notable portion of the overall $L_{ch}$ as the $L_G$ of MOSFET is scaled down to short-channel regime. Thus, charge dynamics is no more governed by the "field-effect" of the G electrode in the D/S induced depletion region. The amount of $V_g$ needed for inversion of the channel region decreases, this fall in channel charge and the $V_{th}$ needed for inversion of the channel with $L_g$ scaling described as $V_{th}$ roll-off.

### 4.2 Drain-Induced Barrier Lowering:

In an ideal "long channel MOSFET" the height of source to channel barrier iss governed by $V_g$. Nevertheless, interaction may happen as $L_{ch}$ is scaled to the short-channel regime b/w the channel-drain depletion region and the source-channel depletion region. In the short-channel MOSFETs, $V_d$ moreover decreases the electron energy level in the D region but the D EF also pairs through the depletion region and decreases the source to channel barrier height. Since, $V_{ds}$ is not marked in the long-channel MOSFETs attributable to the absence of interaction b/w the depletion regions and decrement in the height of the source-channel barrier. However, DIBL decreases the height of the source to channel barrier with improved $I_{OFF}$.

### 4.3 Hot Electron Effect:

With scaling of $L_{ch}$, the lateral EF escalates significantly, the magnitude of the EF is elevated in short-channel MOSFETs. Since, due to lateral EF, elevated momentum and K.E gained by the channel electrons results in collision and atoms exchanging their momentum and energy which further heads to formation of an electron-hole pair if the electrons transfer optimum amount of energy to the atoms.

$V_g$ in addition produces a longitudinal EF in the channel region and the collision-generated electrons move towards it and might invade the oxide and hit out the electrons. The hot electrons (~3.1eV) [11-18] enters the oxide-layer by degrading the insulation capability of oxide layer and these may gather under the oxide-layer as charges and effects the $V_{th}$.

### 4.4 Gate Leakage Currents:

Due to continuous reduction in thickness(~2nm) of $SiO_2$ layer utilized as the gate dielectric results in $I_{OFF}$ due to the tunneling of electrons through the $SiO_2$ layer [19-21] and the leakage current will be so elevated that the Ckt. power dissipation will get enhance with tremendous rate.

### 4.5 Surface Scattering:

The longitudinal EF escalates attributable to the decrease in $t_{ox}$, as $L_{ch}$ reduces which is attributable to the lateral extension of the depletion layer also the surface mobility becomes field dependent[20]. The surface scattering which is the collisions suffered by the electrons which are moved towards the interface and the carrier transport in MOSFET is confined within the narrow inversion layer causes the decrement in mobility. Thus, mobility of electrons is difficult in parallel to the interface thus, the average surface mobility is about half as much as that of bulk mobility.

All these SCEs degrades the performance and makes the process of scaling difficult. To overcome the problem of oxide scaling, the use of elevated-k dielectrics is used as a gate insulator.

# CHAPTER-5

## HIGH-K DIELECTRIC AS GATE INSULATOR

As mentioned, due to the quantum mechanics tunneling the scaling of an oxide leads to the leakage current and static power dissipation and the unwanted modification of an oxide.
A FET device is capacitance-operated, where the S-D current of the FET relies on $C_g$.

$$C = \varepsilon 0KA/t$$

Where A=area, t = thickness ($SiO_2$) and ε = relative permittivity.

The tunneling problem can be resolved by replacing $SiO_2$ with a physically thick layer of a new material of higher dielectric constant K [22]. Replacing $SiO_2$, maintains the identical capacitance however, will reduce the tunneling current. Thus, "elevated-K oxides" are the material with elevated dielectric constant.

For designing of all FET devices, the dimensions are scaled proportionally and to describe "electrical thickness". Electrical thickness of the new gate oxide in terms EOT so that the material doesn't affect electrical design, defined as below

$$t_{ox} = EOT = (3.9/K)t_{HiK}$$

Where 3.9 is dielectric constant of $SiO_2$. High-K dielectric oxide is required for scaling to lower values of EOT.

### 5.1 Properties of High-K Dielectric:

Microelectronics uses Si technology because of its advantages though has standard production however importantly, $SiO_2$ is elevated quality insulator as it can be produced soberly by thermal oxidation, considering other SC has a poor native oxide or poor interface with its oxide (Ge, GaAs, GaN, SiC). $SiO_2$ has minimal electronic defects and forms as an outstanding, abrupt interface with Si due to its amorphous nature. It can be carved and patterned to a nm scale, only issue is to tunnel down it's thickness and must lose the benefit of $SiO_2$ and start using a new High-K.
The needs of a new High-K oxides given as:

1. High-K value to use economically for feasible amount of scaling.
2. Thermodynamical stability with the oxide.
3. Band-offsets with Si of over 1 eV, utilized as an insulator.
4. Kinetically stable so that it can be processed at 10000 C for 5s.
5. Electrical interface with Si is good.
6. Limited electrical active defects.

Replacing $SiO_2$ as dielectric, advantages related to performance of Si are lost. So, SCs like Ge or III-Vs might get considered for utilizing as the channel. Si requirement is considered for the fabrication process with automatic-loading tools. As, industry is driving for larger Si wafers with diameters predicted to be no less than 450nm [23-25], will continue governing material for IC manufacturing in almost every aspect.

## 5.2 Requirements of High-K oxide:

### 5.2.1 *K Value*

The value of an oxide should be above 12, is a trade-off b/w K value and the band-offset condition reasonably a larger band-gap. In order to have a larger band-gap we requisite low K value. Various oxides with extremely high K value suitable for DRAM capacitor dielectrics however with very low band-gaps ($Ta_2O_5$, $SrTiO_3$). The conduction or valence band offsets must be greater than 1eV from Si, band gap with ~3.1ev is considered.

| | *K* | Gap (eV) | CB offset (eV) |
|---|---|---|---|
| Si | | 1.1 | |
| $SiO_2$ | 3.9 | 9 | 3.2 |
| $Si_3N_4$ | 7 | 5.3 | 2.4 |
| $Al_2O_3$ | 9 | 8.8 | 2.8 (not ALD) |
| $Ta_2O_5$ | 22 | 4.4 | 0.35 |
| $TiO_2$ | 80 | 3.5 | 0 |
| $SrTiO_3$ | 2000 | 3.2 | 0 |
| $ZrO_2$ | 25 | 5.8 | 1.5 |
| $HfO_2$ | 25 | 5.8 | 1.4 |
| $HfSiO_4$ | 11 | 6.5 | 1.8 |
| $La_2O_3$ | 30 | 6 | 2.3 |
| $Y_2O_3$ | 15 | 6 | 2.3 |
| a-$LaAlO_3$ | 30 | 5.6 | 1.8 |

Fig 9: Static dielectric constant (K), experimental band gap, (consensus) conduction band offset on Si and other various oxides

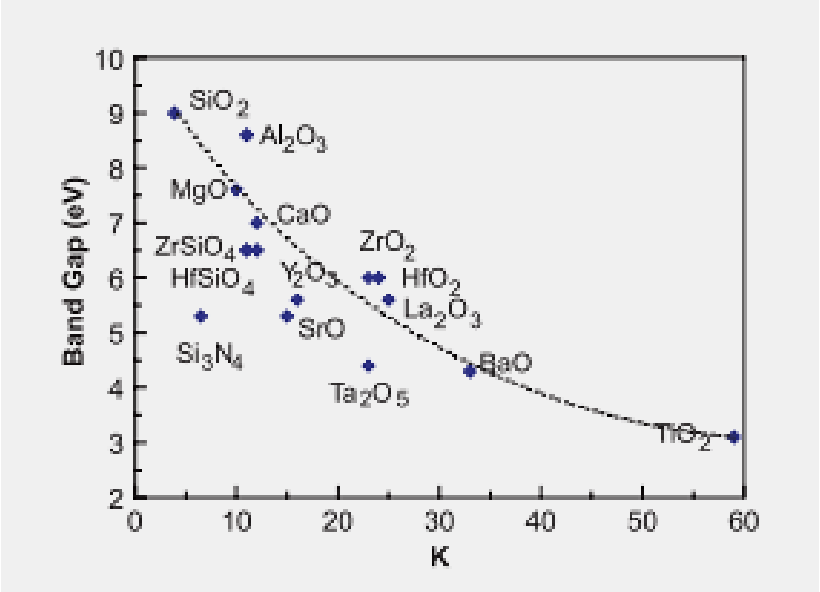


Fig 10: K vs. band gap for various gate oxides

### 5.2.2 *Thermodynamic Stability*

For thermodynamic stability oxide should not respond with Si to form $SiO_2$, for restricting $SiO_2$ heat of formation of the oxide must be higher than $SiO_2$.[26] Therefore, the possible oxides from II to IV in the periodic table are restricted. The oxides of group II are not favored because are

very reactive with water. So, the desirable group IV oxides are $HfO_2$, $ZrO_2$, $Al_2O_3$, $La_2O_3$, $Y_2O_3$ and numerous lanthanides. Zr being less stable than Hf in terms of their thermodynamic stability due to which it might get with Si to form Silicide, $ZrSi_2$. Therefore, $HfO_2$ is the most desired high-K oxide over $ZrO_2$.

### 5.2.3 *Band Offsets*

The band-offsets needs to be elevated for maintaining insulating properties of the gate dielectric stack, high-K oxide should utilize as an insulator. For inhibiting the conduction by Schottky emission of electrons or holes into the oxide bands, requires that the potential barrier at each bond should be above 1eV. $SiO_2$ has a wide band gap of 9eV. The group IV oxide satisfies the criteria and this group also passes the thermal stability criterion because of the elevated heat of formation which correlates with a wide band gap.

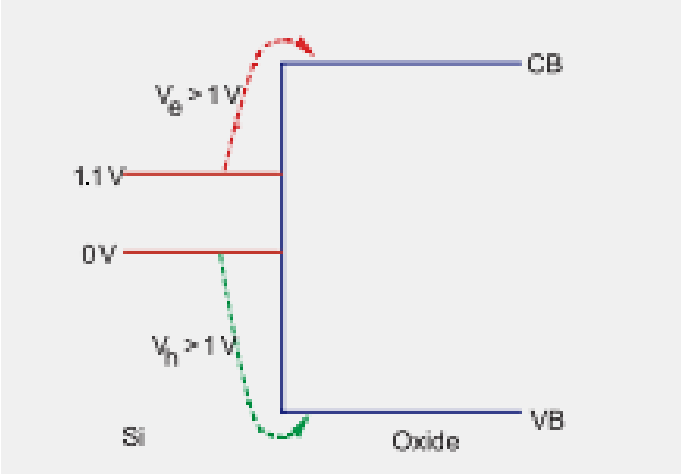


Fig 11: Schematic diagram of band offsets determining carrier injection in oxide band states

### 5.2.4 *Interface Quality and Defects*

With the aim to avoid scattering carriers, the electrical quality of the Si: high K interface should be of the supreme quality with reference to roughness & absence of defects. Electrically active defects can be described as atomic configurations, are responsible for electronic states in the oxide band gap to trap carriers [25]. Usually, the aforementioned are the sites of surplus or deficit of $O_2$ or impurities that might get formed either in oxide layer or at the interface.

Undesirability for defects:

- Charges trapped in defects, the voltage at which it turns ON, shifts the gate $V_{th}$ of the Tx.
- The trapped charge commutes with time so $V_{th}$ shifts with time, leads to the instability of operating characteristics.
- Trapped charges scatter carriers in the channel, moreover lowers the carrier mobility.
- The starting point for electrical failure, defects cause unreliability and oxide breakdown.

The elevated-K oxides vary from $SiO_2$ as $SiO_2$ has a minimum concentration of defects that gives hike to states in the gap which is basically, it's less coordination number. $HfO_2$ and $ZrO_2$ being the most suitable gate dielectrics, $HfO_2$ being the more preferred material over $ZrO_2$ as it can react with Si to form $ZrSi_2$.

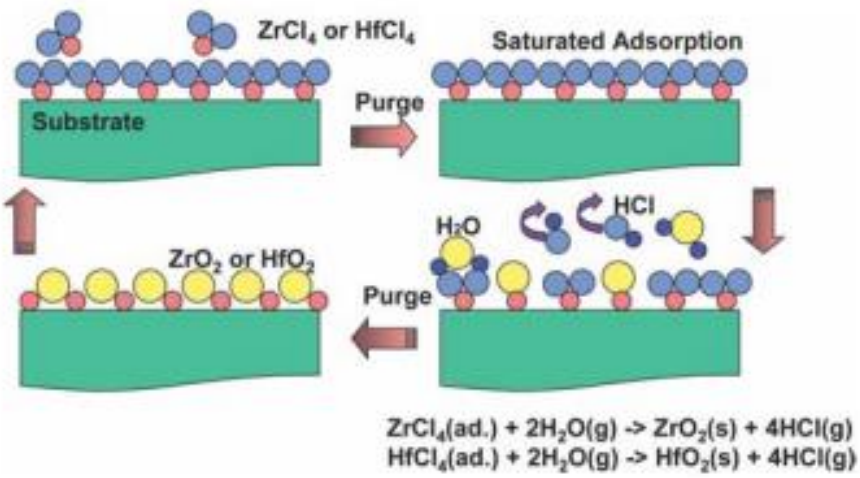


Fig 12: Schematic of the cyclic process of Atomic Layer Deposition.

### 5.3 Improvements in device performance:

The utilization of high-K dielectrics stack for recessed channel MOSFETs results in enhancement of device performance in terms of decreased off current, decreased subthreshold conduction, higher ON to OFF current ratio, improved mobility, decreased gate capacitance etc.

#### 5.3.1 *$I_{ON}$ and $I_{OFF}$ Ratio*

Utilizing high-K dielectrics jointly with $SiO_2$, the value of D $I_{OFF}$ is decreased as compared to $SiO_2$ alone for gate insulator. The physical thickness of a gate oxide with elevated dielectric constant is more, increase in physical oxide thickness elevates the barrier distance b/w S and D curbing short-channel leakage current effect.

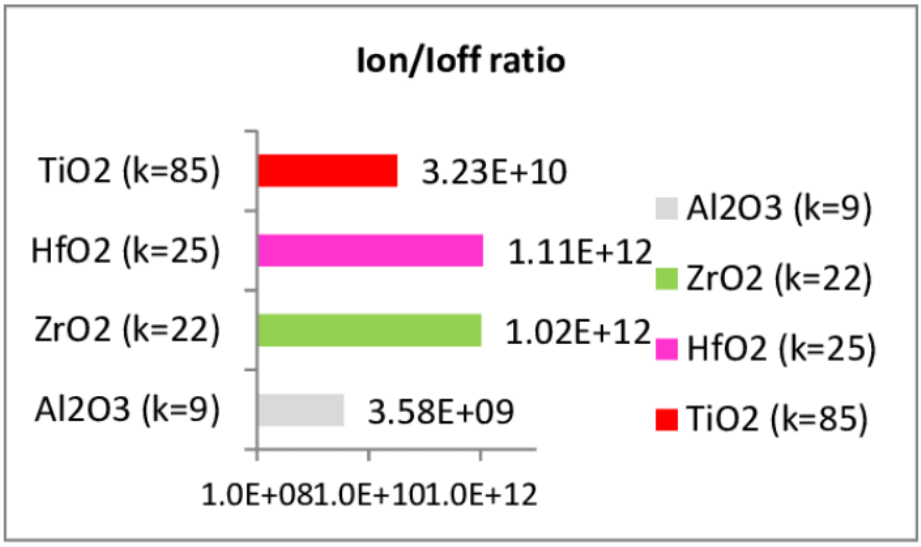


Fig 13: $I_{ON}/I_{OFF}$ ratio variation for various dielectrics

#### 5.3.2 *Sub-threshold Condition*

With dielectric constant of gate stack elevates the sub-threshold slop decreases. The increase in $V_{th}$ as sub-threshold conduction decreases exponentially with increase in $V_{th}$ for the same $V_g$. As

$V_{th}$ decreases, sub-threshold current escalates. This can be overcome with elevated-K gate stack as its use escalates $V_{th}$ reducing the sub-threshold conduction. The decrease in sub-threshold slope reduces losses in the weak inversion regime leading to static power dissipation.

### 5.3.3 *Electric Field*

Due to the increase in physical distance b/w the S and D terminal when a high-K gate stack is used, value of EF at the drain end elevates as the dielectric constant of gate stack escalates being minimum for $HfO_2$ (k=30) and maximum for $SiO_2$ (k=3.9). because EF is inversely proportional to distance for the same electric potential difference, EF decreases as physical thickness escalates due to the increment in dielectric constant maintaining the same Effective Oxide Thickness (EOT). This decrease in EF prevents the attainment of elevated K.E of the electrons near drain end and thereby preventing the device damage due to impact ionization.

### 5.3.4 *Transfer Characteristics*

Due to increment in dielectric constant of the gate stack, the drain current decreases for the same $V_g$. This is due to the rise of channel resistance with increase in the physical distance b/w the S and D.

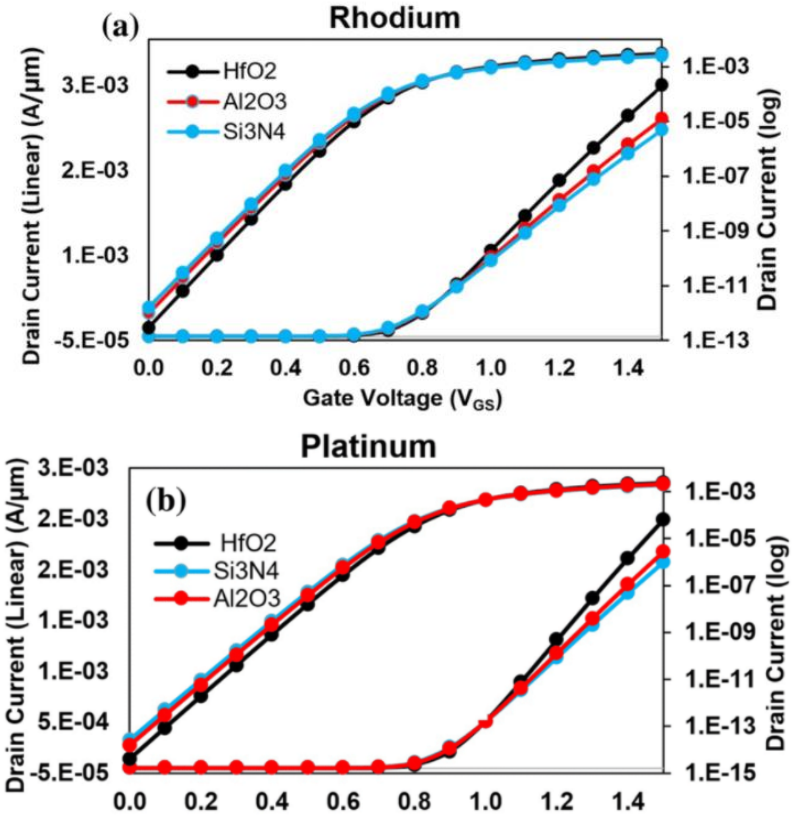


Fig 14 (a) and (b) Effect of different elevated-k dielectric on Transfer characteristics.

Thus, it can be concluded that there is a need of some extra device engineering if high-K dielectrics are to be used as a gate insulator. The use of elevated-K dielectric stack for gate insulator improves device's performance tremendously.

# CHAPTER-6
## TRENCH GATE STRUCTURE

The earlier section has emphasized on the need of using Elevated-K dielectrics to improve the device performance in OFF state or rather low performance of the device. However, today there is an increasing demand and need of elevated-power devices i.e., devices whose current driving capability is very elevated. Conventional methods of improving current driving capability include high oxide capacitance of the device by reducing oxide thickness [26]. This method ceases to feasible below the oxide thickness of ~3nm due to the rise in leakage current which is because of the quantum mechanical tunneling. Other option is to increase the $v_s$ to increase current, which is also not feasible due to ratings and decreased efficiency.

Efficient MOSFET's capable of elevated efficiency are in elevated demand. To counter the impacts of short channel, different models were presented and any of them, favorable is trenched gate structure [3]. Although, this structure decreases SCE, some reduction in Saturation current (Is) can be seen alongside a rise in the limit voltage (Vth). Trench Gate MOSFET enables the coherent performance as a discrete power device for moderately minimal voltage applications attributable to their least achievable $R_{ON}$ as compared to structure of otherwise alike specifications.
A trench gate MOSFET, an effort to make a complete chip conduct the current vertically from one surface to the other to achieve elevated drive capability. Millions of trenches packed on a chip, having adequate depth to penetrate oppositely doped 'body' region below the top surface. A gate dielectric and gate electrode are present in each trench to govern the current conduction in its vicinity by the virtue of field effect.

Similar to MOSFET, a trench MOSFET cell contains the D, G, S, B & the channel regions demonstrates a vertical direction of current flow. Cells are connected in parallel to bring down the value of $R_{ON}$. Along with, LDD region b/w the channel and the D to withstand large voltage in OFF-state condition. In the ON-state condition, under the effect of the potential difference, the charge carriers are simply drifted through the LDD region towards the D. Thus, LDD [27] region known as the 'drift region'. The crucial design considerations of a trench gate power MOSFET are reduction of $R_{ON}$, intensification of $V_{BD}$, decrement in switching delays, intensification in "gm" and in dV/dt capability, elevated damage immunity while switching large current in inductive loads and deprecation of energy losses.

Thus, the design of a trench gate MOSFET is a tradeoff b/w its performance parameters for a particular application. With the sweep of time, numerous advancements have been put forward, analyzed, and implemented to alter the device structure for enhancing above mentioned tradeoffs.

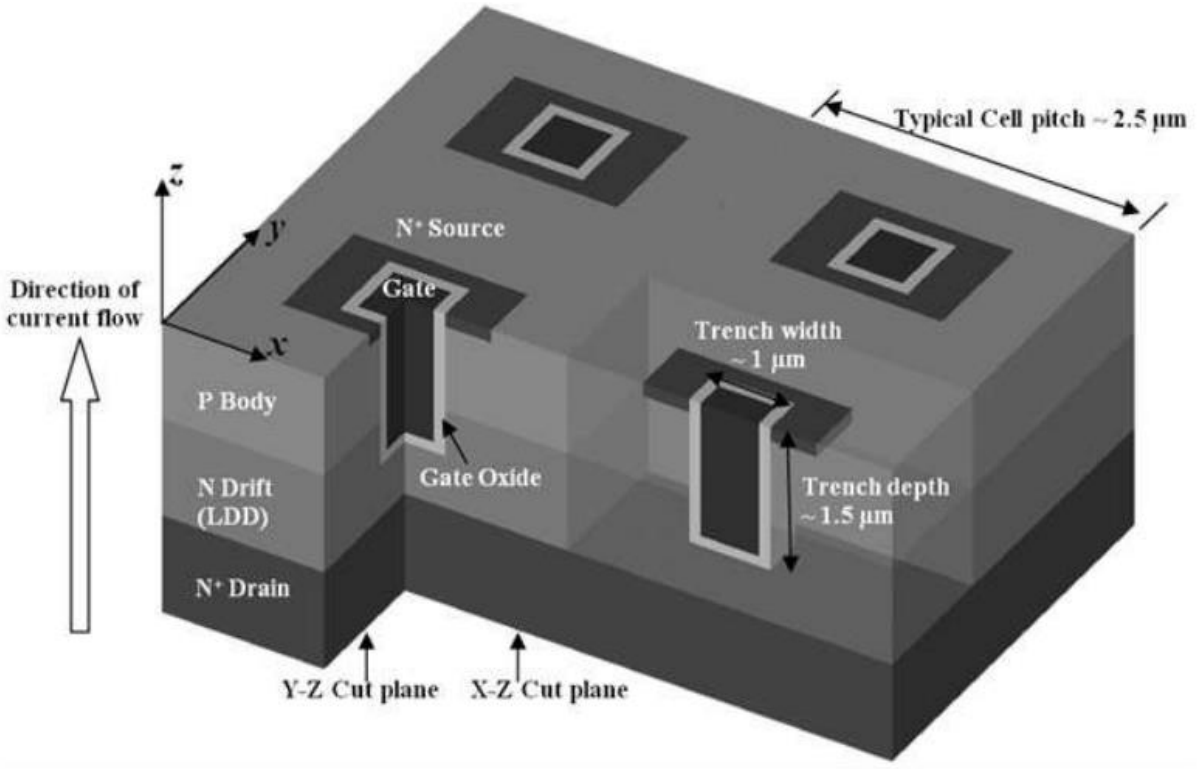


Fig 15: Trench gate power MOSFET's typical dimensions in a 3D view

This analysis describes the stacking of $HfO_2$ with $SiO_2$ at gate terminal in CTG, to make use of benefits of the structure and up-scale its functioning through enhancing the $I_s$ and $V_{th}$. $HfO_2$-insulator and functions as a buffer layer in b/w $SiO_2$ and gate electrode [28]. Its elevated dielectric constant aides in accomplishing larger oxide capacitance, which escalates the $I_s$ of MOSFET and diminishes the formation of hot electrons.

The presented GaN in lieu of Si-wafer, in the similar trenched gate structure. Notable preferences of GaN is conceivability to reduce the dimensions of the device with smaller $R_{ON}$ and elevated $V_{BD}$ than is conceivable with Si. GaN has elevated electron mobility thus, an improved $I_{ds}$. GaN shows a wide bandgap of 3.4 eV and has elevated warmth capacity. Thus, useful for elevated-temperature operation (400°C) applications and efficient operation at large voltages. [28-30] It has elevated electron mobility (1500 cm2 /V-sec) than Si, which implies it displays elevated critical EF strength than Si. Elevated mobility attributable to quicker switching rate respecting fewer switching losses.

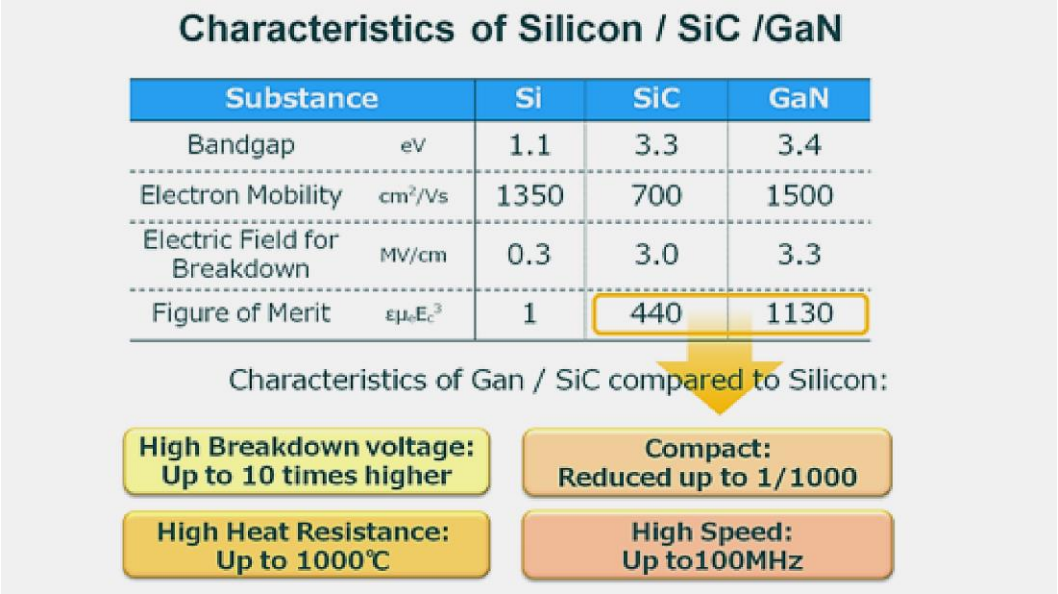


Fig 16: Characteristics of GaN

GaN is developing as a significant material for MOSFET attributable to its thermal stability superior to Si. Further presentation of GaN as a base device material instead of Si enhances the functioning of trenched gate MOSFET in contrast to conventional MOSFET at room temperature of 300K[29]. Nonstop utilization of gadgets may prompt the development of hotspots in ICs resulting in inappropriate working and failure of the SCs.

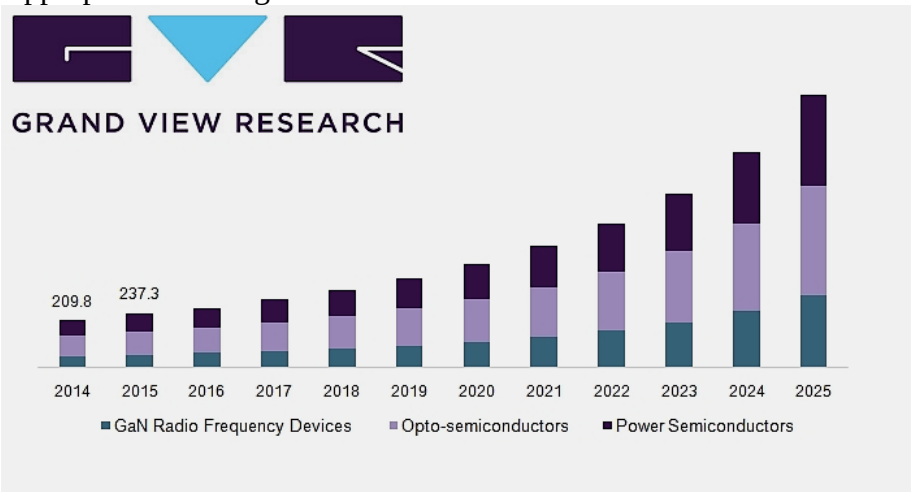


Fig 17: GaN SC Devices market to touch USD 4.3 million by 2025.

Henceforth, developing gadgets that can function successfully at elevated temperatures for considerable amount of time. The device's temperature behavior can be understood from its different boundaries like $I_d$-$V_g$ characteristics, gm, $V_{th}$, switching ratio, $I_{OFF}$, saturation resistance, and EF. These parameters should be free of variation in temperature or impact of temperature ought to be as least as could reasonably be expected. As temperature in thin gate oxide devices elevates, leakage current rises. To limit the leakage current and better gate control, EOT ought to be minimum [9]. For minimum EOT, gate stacking is utilized where a high-K dielectric material $HfO_2$ is utilized to supplement $SiO_2$ as a gate stacking material. Efficient control of gate is accomplished by elevating Cox. This project describes the functioning of GaN-

BTG-MOSFET (Device C) is investigated and correlated with CTG-MOSFET (Device A), BTG (Device B) MOSFET. Further parameters of GaN like electrical parameters, analog/linearity parameter of the devices are analyzed and compared.

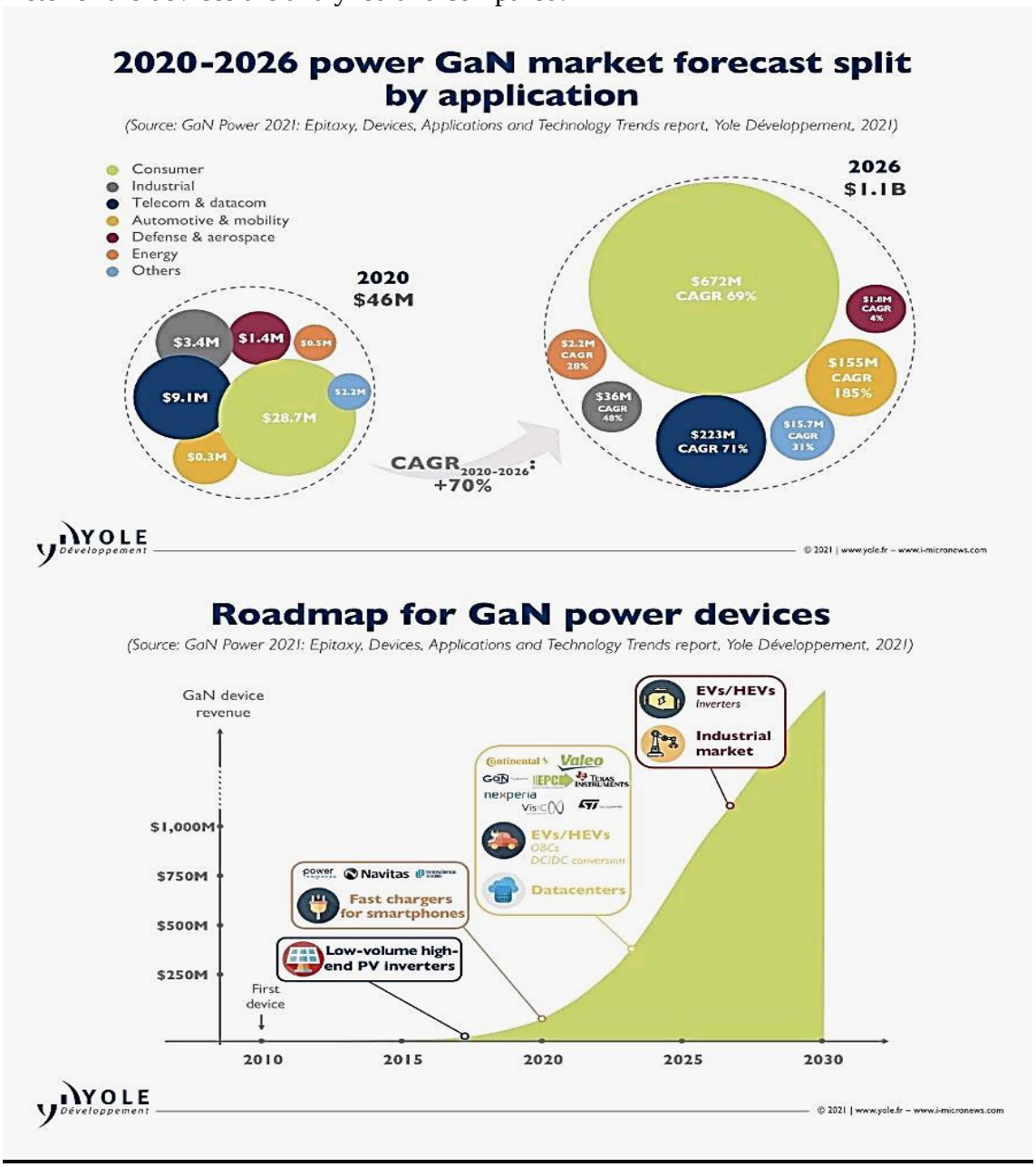


Fig 18: The next wave of GaN power market 2021.

Devices based on GaN proposed to be the best fit for expansion of renewable energy at the same time addressing the issues. With the world on course to move from 8 billion to 30 billion connected devices over the next few years.

# CHAPTER-7
## LITERATURE REVIEW

This chapter includes the Research papers and books that are referred to complete the *"Study of Nanoscale Trenched Gate MOSFET"*. The topics enrolled in selecting research papers are MOSFET, Trenched Gate MOSFET, Silvaco TCAD Atlas Simulations.
The review work is done for the areas mentioned below-

- Trenched Gate MOSFET
- Physics of materials
- Temperature analysis

While working on MOSFET and its nano-scaled structure on Silvaco TCAD ATLAS, the following literature are referred:


[1] B. Razavi, Design of analog CMOS integrated Ckt.s. Tata McGraw-Hill Education, 2002. [2] A. S. Sedra and K. C. Smith, Microelectronic Ckt.s: theory and applications. Oxford University Press, 2013.
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[8] T. Cheung, M. J. Butson, K. J. P. i. M. Peter, and Biology, "Effects of temperature variation on MOSFET dosimetry," vol. 49, no. 13, p. N191, 2004.
[9] A. Kumar, M. Tripathi, and R. J. I. T. o. E. D. Chaujar, "Reliability issues of In 2 O 5 Sn gate electrode recessed channel MOSFET: Impact of interface trap charges and temperature," vol. 65, no. 3, pp. 860-866, 2018.
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[16] S. Veeraraghavan and J. G. J. I. T. o. E. D. Fossum, "Short-channel effects in SOI MOSFETs," vol. 36, no. 3, pp. 522-528, 1989.
[17] N. D. Arora, MOSFET models for VLSI Ckt. simulation: theory and practice. Springer Science & Business Media, 2012.
[18] B. Doris et al., "Extreme scaling with ultra-thin Si channel MOSFETs," in Digest. International Electron Devices Meeting, 2002, pp. 267-270: IEEE.
[19] A. Kumar, P. M. Tripathi, H. Soni, R. J. I. C. Chaujar, Devices, and Systems, "Numerical Simulation and Parametric Assessment of GaN Buffered Trench Gate MOSFET for Low Power Applications," 2020.
[20] L. Li et al., "Wafer-scale fabrication of recessed-channel PtSe 2 MOSFETs with low contact resistance and improved gate control," vol. 65, no. 10, pp. 4102-4108, 2018.
[21] H. Soni, P. M. Tripathi, M. Tripathi, A. Kumar, and R. Chaujar, "Thermal Reliability of GaN-BTG-MOSFET for Elevated-Performance Applications in Integrated Ckt.s," in 2020 IEEE 40th International Conference on Electronics and Nanotechnology (ELNANO), 2020, pp. 220-223: IEEE.

# CHAPTER-8
## DEVICE STRUCTURE

Till now it has been that to successfully scale a device all its dimension must be scaled proportionally. Scaling leads to the onset of SCEs which have been handled in the following hierarchy:

1. *Problem:* Channel scaling leads to the depletion region under the S and D to become comparable to the channel length which can lead to punch through.

   *Solution:* The use of recessed channel device where the gate-oxide comes in b/w S and D terminals hence eliminating the possibility of punch through.

2. *Problem:* Oxide scaling leads to quantum mechanical tunneling which leads to gate leakage current that elevates the static power dissipation and can destroy the oxide properties.

   *Solution:* The use of high-K dielectrics for gate insulator.

3. *Problem:* The use of dielectric though improves the OFF-state performance of the device, these do not do so much to improve current driving capability.

   *Solution:* Using a Trenched gate structure.

With smaller scales, the problems related to leakage shows the importance of higher $V_t$. higher conductivity in the gate is predominant as the oxide dielectric layers can't be reduced any further to elevate the speed.
The major drawback of nanoscale MOSFET is that it can't generate power at elevated frequencies due to smaller area of Tx's. Thus, Tx's are prone to failure with even a small voltage or current.

### 8.1 Physical device structure and parameters

Based on the above observations, the physical device structures are shown below in the hierarchical manner of their development for this research work.

#### 8.1.1 Gallium-Nitride (GaN) BTG MOSFET:

The Device C in Fig 19 $L_g$ of MOS is 25nm, oxide thickness ($t_{ox}$) is 2nm. A GaN substrate is used in place of Si, S and D region are extensively doped (1×1019cm-3). The Device C is examined with the help of ATLAS simulator. For simulation, mobility and recombination models were utilized with a $V_g$ of 2.0V and a steady $V_d$ of 0.2V.

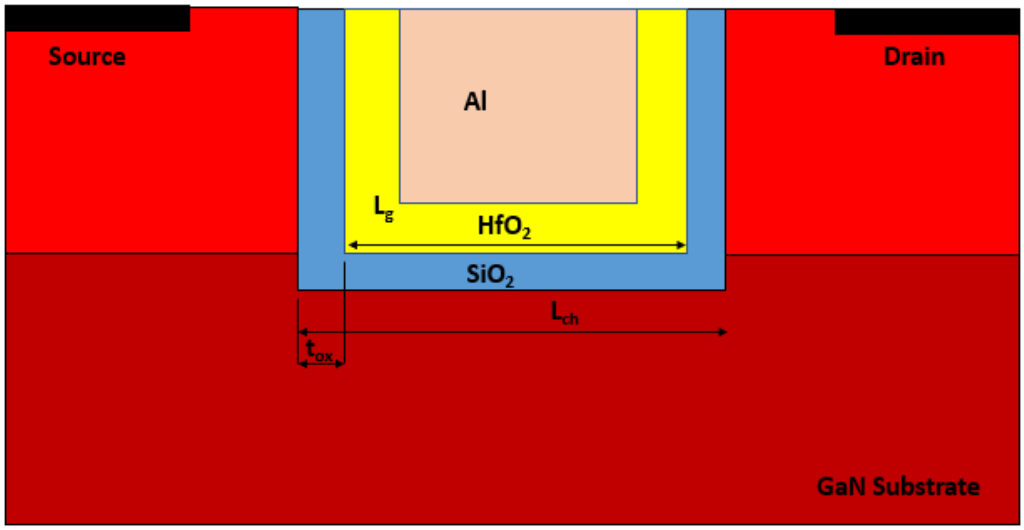
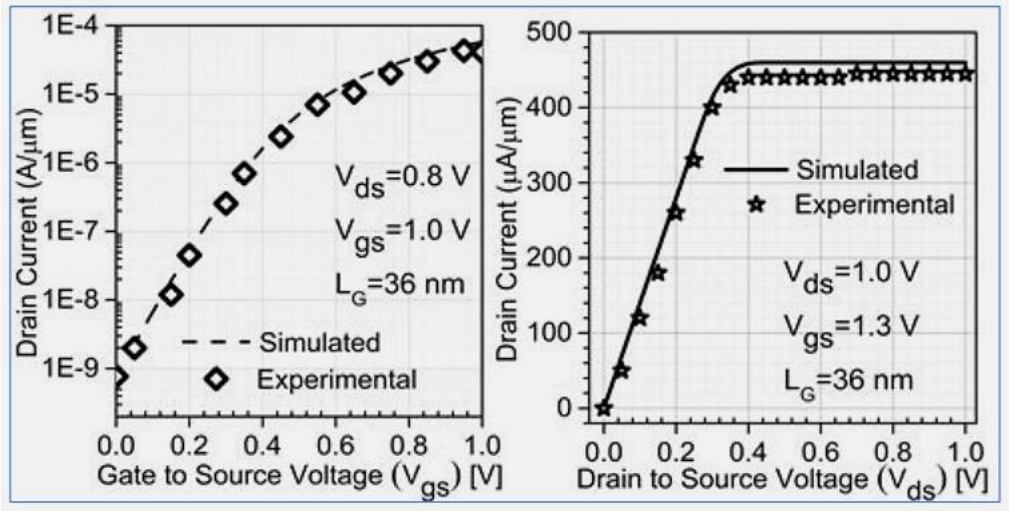



Fig 19: Structure of Device C

The models used are tabulated in Table 8.2

| S.No | Models | Description |
|---|---|---|
| 1. | Mobility models | Lombardi CVT and Constant Low Field Mobility Model. |
| 2. | Recombination model | Shockley Read Hall (SRH) Recombination that incorporate minority recombination effects with carrier lifetime=1×107 s. |
| 3. | Statistics | Boltzmann statistics is valid in SC device theory, Fermi-Dirac statistics are required to observe properties of extensively doped materials. |
| 4. | Impact ionization & Tunneling model | For evaluation of hot carrier performance. |
| 5. | Energy transport model | Hydrodynamic model is prominently accurate than drift-diffusion method and it includes nonlocal effects. Drift diffusion is prone to failure as $L_{ch}$ scaled down to 50nm. |




(a) (b)

Fig.20. (a) Transfer and (b) O/P characteristics calibration of simulated and experimental data for 36 nm recessed channel MOSFET.

For the approval of model's simulation, the trial information of a fabricated trenched gate MOSFET ($L_g$=36 nm) was used & analyzed for the correlation with simulation data in terms of $I_d$-$V_g$ characteristics and O/P characteristics in Fig. 20 (a) and (b) respectively.

### 8.1.2 CONVENTIONAL TRENCHED GATE (CTG) MOSFET:

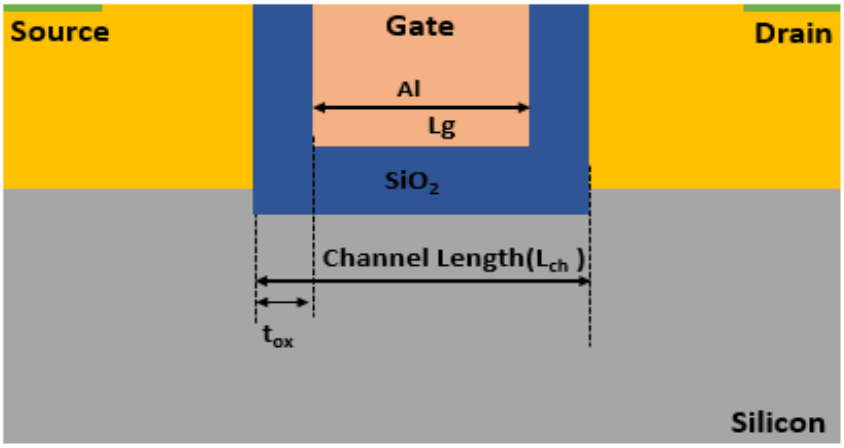



Fig 21: Device A

Scaling of Conventional MOSFETs at the nanoscale are not possible because of SCE's and HCE's, Trenched Gate MOSFET [29] is a favorable candidate for reducing the abundant SCEs and HCEs. Fig 21 represents Device A designed in Silvaco TCAD ATLAS. Due to elevated density of EF lines the potential barriers formed at the corners. Carriers in the channel now require sufficient energy to overcome the barriers, as barriers restricts its carrier transport efficiency and thus, lowering the driving current. In conventional MOSFET a trench is introduced in the electronic channel of the MOSFET, this trench is responsible for MOSFET's operation at nanoscale.

### 8.1.3 BUFFER TRENCHED GATE (BTG) MOSFET:

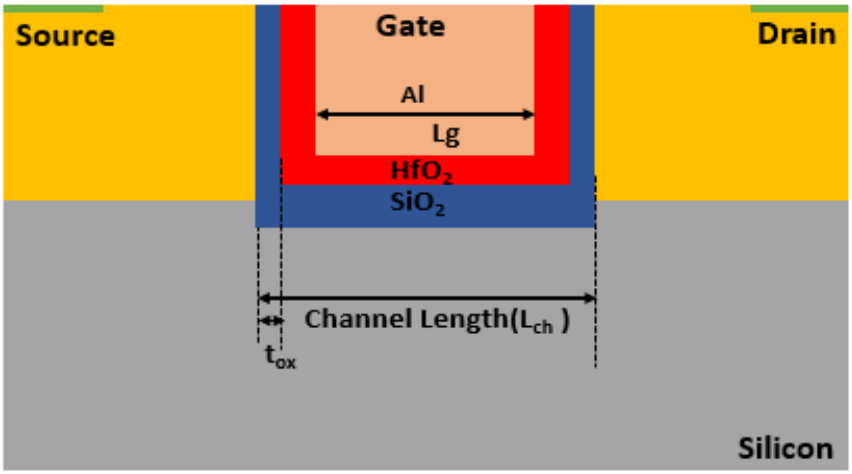



Fig 22: Device B

With the stacking of $HfO_2$ with $SiO_2$ at gate terminal in Device A structure, as spoken to in Fig 22. To use the benefits of the structure and furthermore up scaling its performance by enhancing the $I_s$ and $V_{th}$ simultaneously. Hafnium Oxide- an insulator & behaves like buffer layer in b/w $SiO_2$ and electrode. Elevated K [31] results in getting higher $C_{ox}$, brings about a gain in the $I_s$ of MOSFET & furthermore, diminishes the formation of hot electrons. Going above and beyond, presented GaN instead of Si-wafer, in the same trenched gate structure.

### 8.1.4 GALLIUM NITRIDE (GaN)BTG MOSFET:

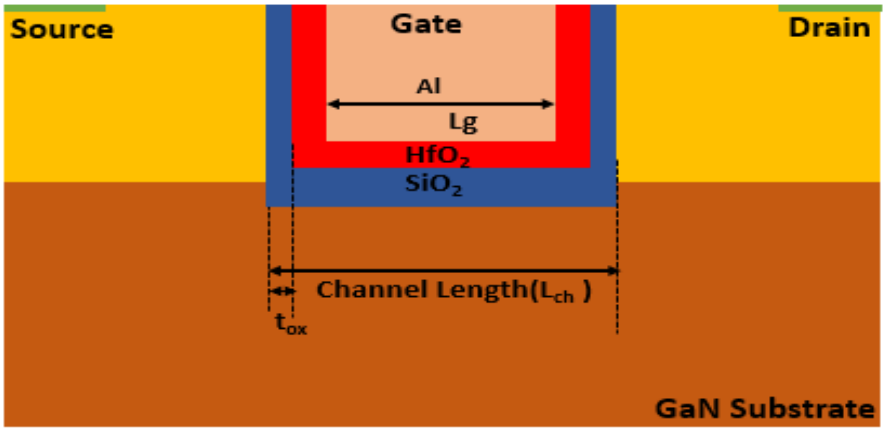



Fig 23: Device C

Major significant benefit of GaN is that it is feasible to additionally downsize the device with little $R_{ON}$ and higher $R_{BD}$ than is conceivable with Si [32-41]. GaN possess elevated electron mobility resulting in an improved D to S current. Fig 23 speaks to Device C, GaN displays a wide bandgap of 3.4 eV & possess elevated warmth limit, that is helpful for elevated-temperature activity (400°C) applications & can function productively at large voltages. It possesses elevated electron mobility [36] (1500 cm2 /V-sec) as compared to Si, due to this reason it shows higher critical EF strength than Si. Elevated mobility results for quicker switching speeds and less losses.

# CHAPTER-9
## SIMULATION RESULTS

The content and results of the following Research papers have been reported in this chapter:

### 9.1 PARAMETER ANALYSIS:

#### 9.1.1 Transfer Characteristics

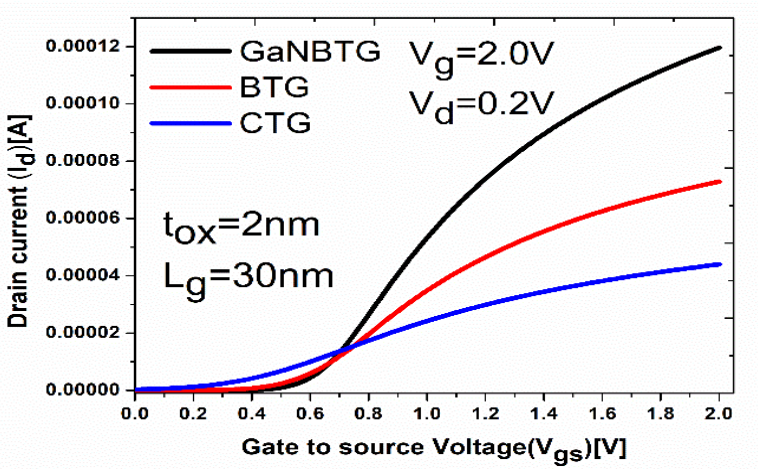



Fig 24: $I_d$-$V_g$ of Device A, B and C.

$I_d$-$V_g$ characteristics implying to the correlation with the $I_d$ and the $V_g$ for a specific $V_d$ seen in Fig. 24. The $I_d$ originates for least even beneath $V_{th}$ & from the S to D region, the diffusion of carriers is governed [31]. As $V_g$ keeps on escalating more than $V_{th}$, the $I_d$ escalates with a production of an inversion layer. The $I_d$-$V_g$ characteristics for Device C for the identical $V_g$, the increment in $I_d$ is identified owing to elevated dielectric of the buffer & the elemental electron mobility [31].

#### 9.1.2 O/P Characteristics:

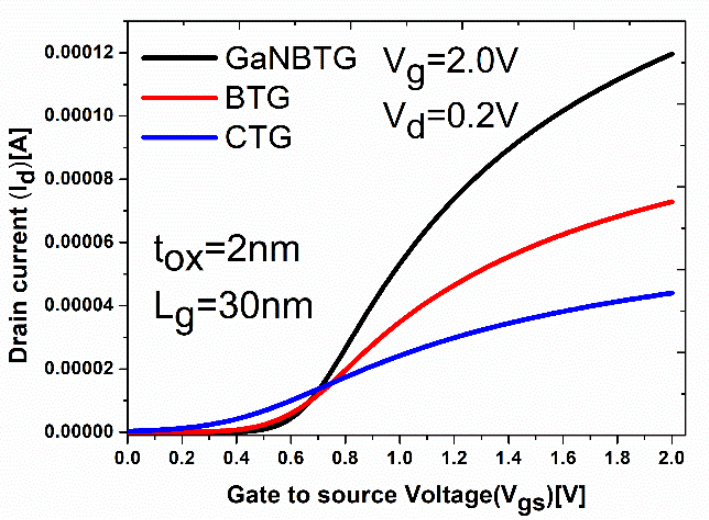



Fig 25: O/P characteristics of Device A, B and C.

O/P characteristics in Fig. 25, point towards the $I_d$ with the $V_g$ for a particular $V_g$. The O/P current starts with linear escalation along with O/P voltage & attain drenched state attributable to pinch-off voltage of the channel region at the drain end [31]. As $V_g$ rises, the channel layer charge rises accompanied by $I_d$ [31]. The $I_d$-$V_d$ curve of Device C is better than that of Device A as well as Device B at 300K [29]. Although, having identical biasing in all the 3 devices due to alofted mobility of electron gives an upraised $I_{ds}$ which illustrates elevated critical field strength than Si [31].

### 9.1.3. Transconductance:

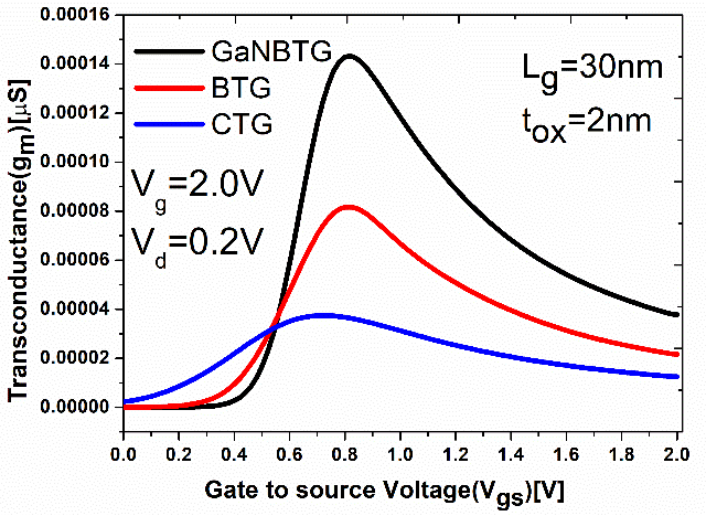
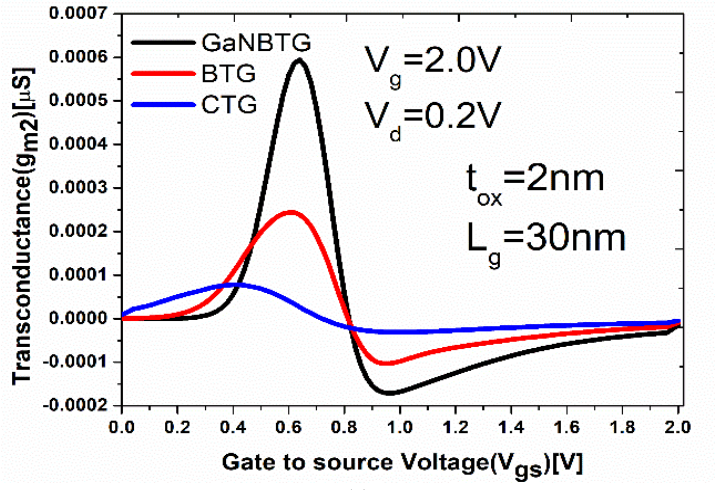


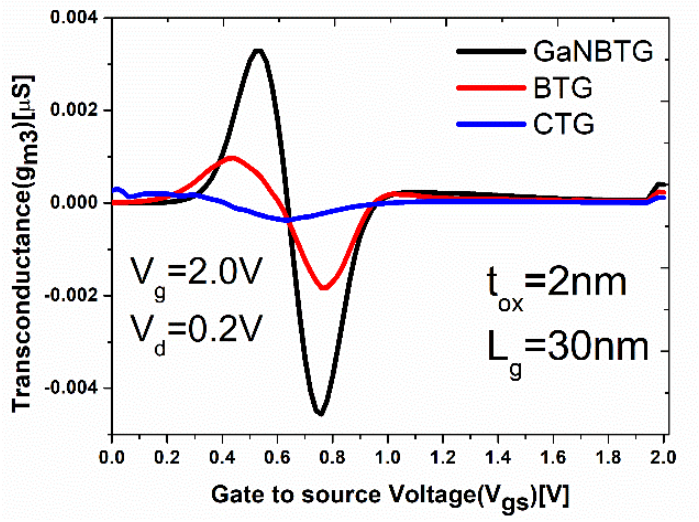

Fig 26: 1st order transconductance ($g_{m1}$) of Device A, B and C.

Through the application of $V_g$, substrate or drain results in variation in $I_d$ under normal conditions [31]. The fraction of increment in the $I_d$ to $V_g$ while maintaining the $V_{bs}$ and $V_{ds}$ constant is called transconductance or gate transconductance ($g_m$) in Fig 26. It provides the measure of device's gain.

### 9.1.4. Higher-order Transconductance:




(a)




(b)

Fig 27 (a) and (b): 2nd and 3rd order of Transconductances of Device A, B and C.

Hence, overall higher order transconductances ($g_{m3}$) escalates. The various higher-order derivatives of transconductance are described by Eq. 1:

$$g_{mn} = \frac{1}{n!}\frac{\delta^n I_{DS}}{\delta V_{GS}^n}, \text{ where n = 1, 2, 3} \qquad (1)$$

The variation of $V_{gs}$ and $V_{th}$, called $V_{gt}$ [$V_{gt}=V_{gs}-V_{th}$]. For comprehensive amplification, $g_m$ Device C should have supreme value, elevated current density & electron velocity and rise in electron mobility helps in escalating $g_m$ [31]. The reason of maxima for $g_{m2}$ and $g_{m3}$ for Device C, is that the denominator contains change in the voltage (gate) as this value keeps getting smaller as the order of the derivative increases [31]. Thus, overall higher order transconductances ($g_{m2}$, $g_{m3}$) shows greater values in Fig 27 (a) and (b).

### 9.1.5. Transconductance Generation Factor:

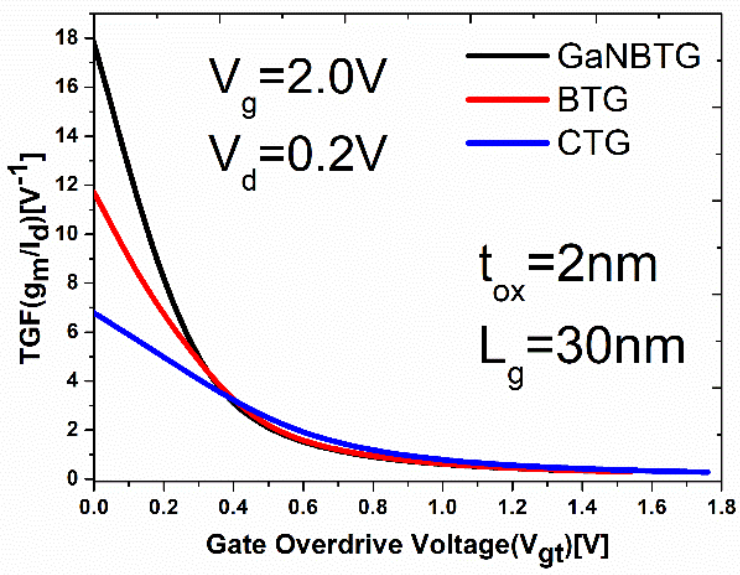



Fig 28: TGF variation as a function gate overdrive voltage($V_{gt}$) of Device A, B and C.

The TGF is described as an attainable gain per unit power loss. Higher TGF enhances the performance and efficiency of the device so that it can function at low $V_s$ in Fig. 28[31].

### 9.1.6. O/P Conductance:

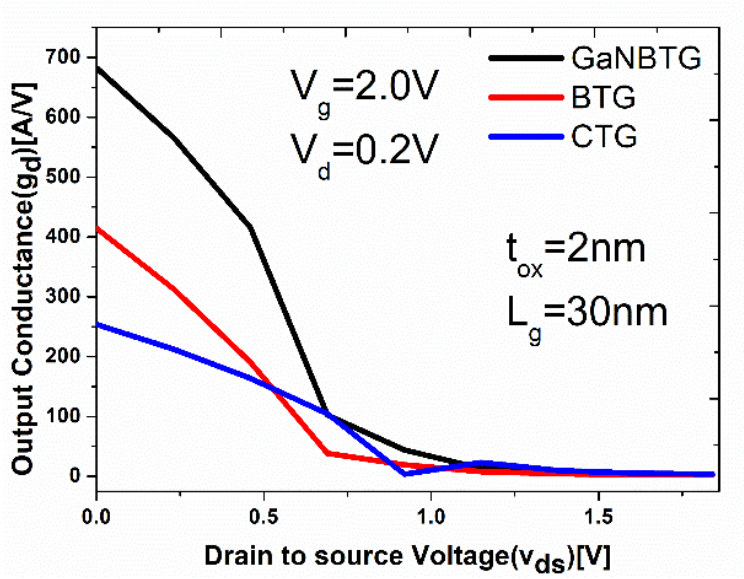



Fig 29: O/P conductance($g_d$ ) variation with drain voltage ($V_{ds}$) of Device A, B and C.

The O/P conductance in Fig. 29, is the proportion of variation in $I_d$ to variation in $V_{ds}$ with $V_{gs}$. The rise in $V_{ds}$ leads to fall in $g_d$ and it tends to zero as the device drift towards saturation region.

The parameters discussed above are being described by the Eq. 2 to Eq. 6 as listed below.

1. Transconductance:

$$g_{m1} = \frac{\delta I_d}{\delta V_{gs}} \qquad (2)$$

where $I_d$ indicates drain current and $V_{gs}$ indicates gate voltage.

2. Higher-order Transconductance:

$$g_{m2} = \frac{\delta^2 I_d}{\delta Vgs^2} \qquad (3)$$

$$g_{m3} = \frac{\delta^3 I_d}{\delta Vgs^3} \qquad (4)$$

3. Transconductance generation factor (TGF):

$$TGF = \frac{g_m}{I_d} \qquad (5)$$

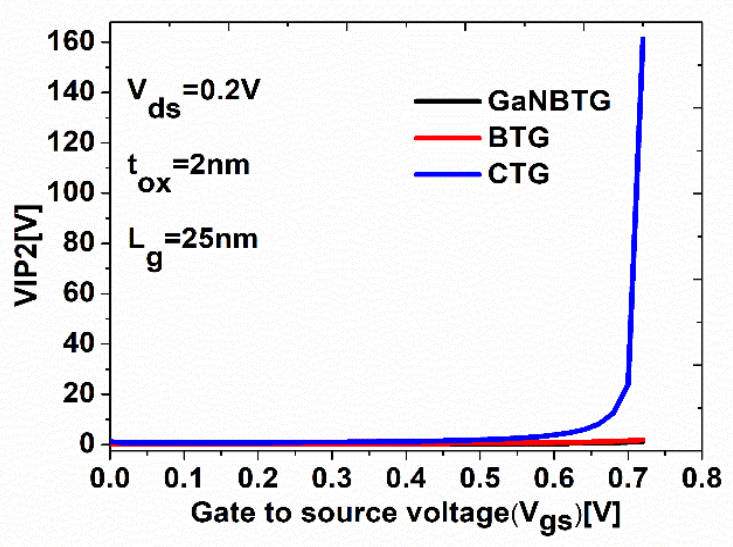
4. O/P Transconductance:

$$g_d = \frac{\partial I_d}{\delta V_{gs}} \qquad (6)$$

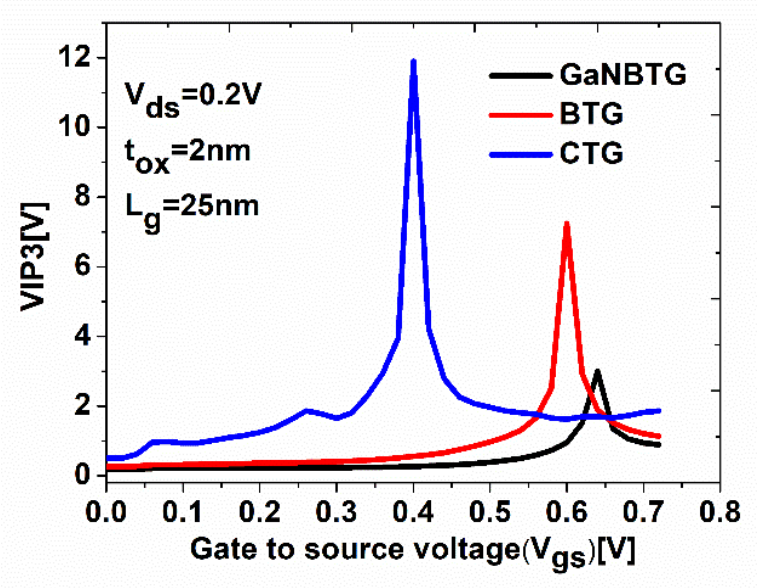
### 9.2. Analog/Linearity Parameters:

The analog parameters and electrical characteristics of Device A, B and C is examined & compared in the matter of linearity parameters, 2nd and 3rd order of VIP, IIP3, IMD3, HD2, HD3 & 1-dB compression point, in contrast to all the other two devices with 25nm $L_g$ at $V_{gs}$=1.3V and $V_{ds}$=0.2V.

### 9.2.1. Voltage Intercept Point (VIP):




(a)




(b)

Fig 30: 2nd and 3rd order of Voltage Intercept Point of Device A, B and C.

Less intermodulation distortion, also elevated linearity, is must for working in weak signals for a CMOS device. Hence, the performance metrics used in this analysis are a 2nd and 3rd order of VIP and IIP, 3rd-order IMD, 2nd and 3rd-order of HD [11]. Non-linearity commences IMD which further gives rise to undesirable deteriorated signals in the O/P of different frequency signals as

compared to an I/P signal. For dc parameters, VIP2, VIP3 are determined for the distortion characteristics.

The general I/P voltages ($2^{nd}$ and $3^{rd}$-order VIP) comprises the I/P voltages at which higher-order harmonics are similar as shown in Eq.2.

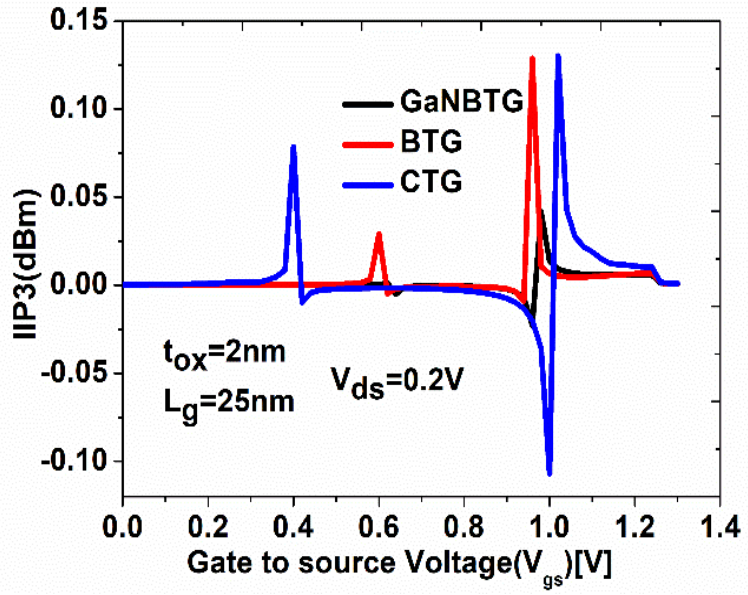
$$VIP2 = 4\frac{g_{m1}}{g_{m2}} \qquad (7)$$

$$VIP3 = \sqrt{24 \times g_{m1} / g_{m3}} \qquad (8)$$

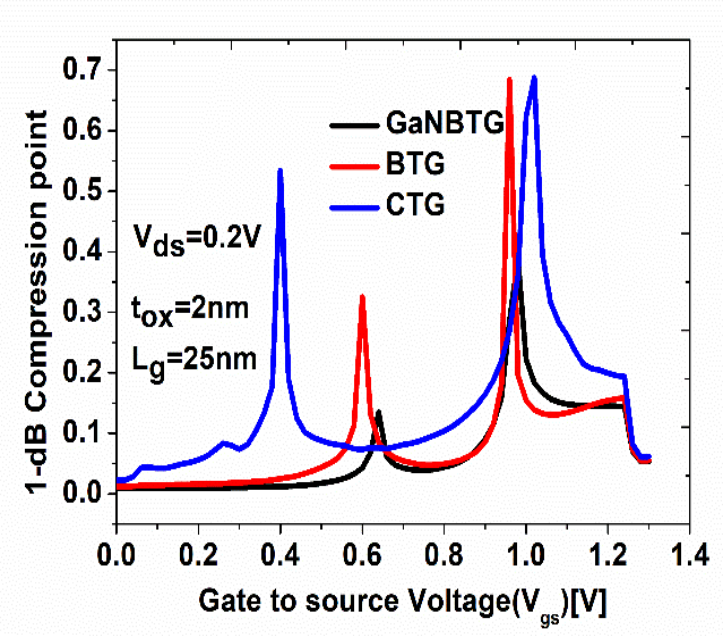
Fig. 30 (a) and (b) highlights the variation of $2^{nd}$ and $3^{rd}$ order of VIP with the $V_{gs}$ for Device A, B and C. To ensure higher linearity of the device, $3^{rd}$ – order $g_m$ must be very low, also for low distortions, the values of $2^{nd}$ and $3^{rd}$ -order VIP must be larger than the desired peaks but in Device C, due to high transconductance ($g_{m3}$) the device does not favor the larger values of VIP2 and VIP3 as compared to Device A and B characteristics of VIP2 and VIP3 are observed much better.

**9.2.2.(a) Current Intercept Point ($3^{rd}$ order):**

**(b) 1-dB depression point:**




(a)




(b)

Fig 31: (a) and (b) 3rd order intercept point (IIP3) and 1-dB compression point of Device a, B and C.

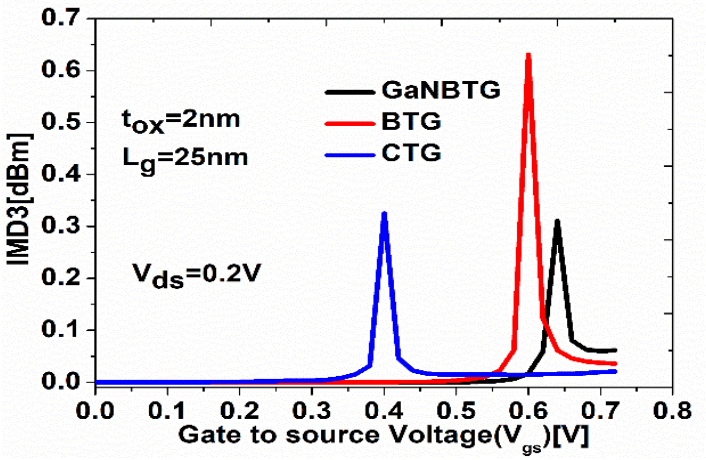
In Fig. 31 (a) and (b) shows the significant results, it describes the efficiency of an amplifier also its linearity i.e., 3rd -order IIP and 1-dB compression point respectively. For MOS amplifiers, the larger the O/P at the intercept results in improved linearity, and can be evaluated by Eq.9 and 10. The 1-dB compression point is required for the understanding the presence of compression so that to intercept distortion at the I/P levels [3]. The I/P power that results in gain to decrease by 1-dB crosses the compression point and for the amplifier with elevated linearity, it must be prolonged as high as possible. Fig.31 (a) and (b) shows much improved 1-dB compression point's characteristics for Device A and B but in Device C, having high current driving capability due to its elevated conductivity, the higher peaks are not observed in owing to higher $g_{m3}$

The above-mentioned parameters are described by the following equations:

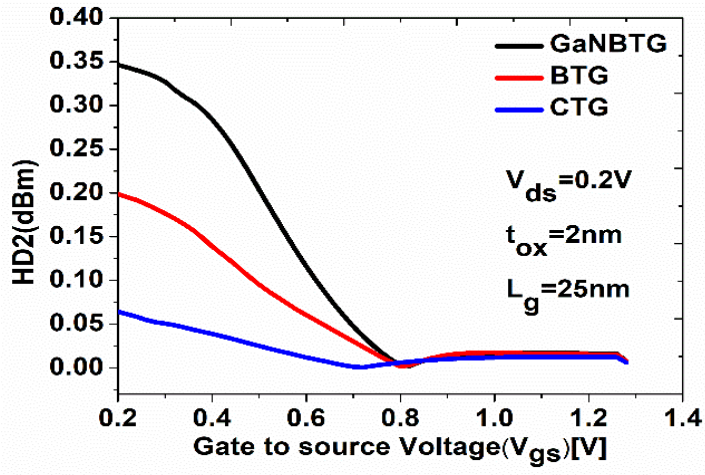
$$IIP3 = \frac{2}{3}\frac{g_{m1}}{g_{m3} \times Rs} \qquad (9)$$

$$1-dBCompressionPoint = 0.22\sqrt{\frac{g_{m1}}{g_{m3}}} \qquad (10)$$

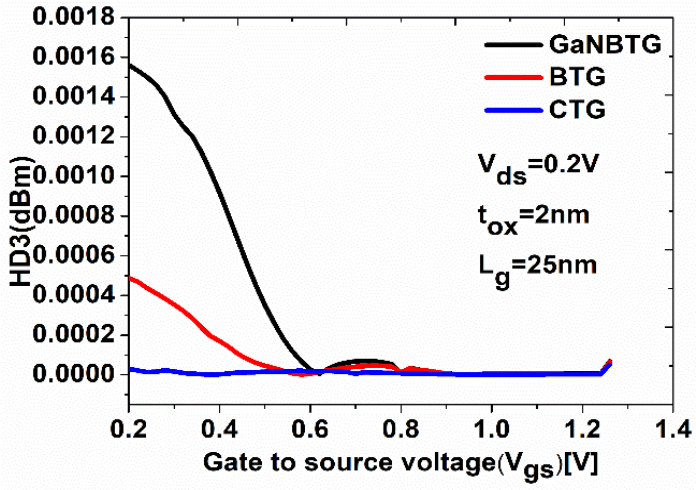
**9.2.3 (a) 3rd order Intermodulation Distortion:**
**(b) 2nd order of Harmonic Distortion:**
**(c) 3rd orders of Harmonic Distortion:**




(a)




(b)




(c)

Fig 32. (a) 3rd order Intermodulation Distortion, (b) 2nd order of Harmonic distortion and (c) 3rd order Harmonic Distortion

In addition, Fig. 32 (a), (b), and (c) shows the major issues that arises in the amplifier's linearity resulting in nonlinear behavior of device. IMD3 is the intermodulation current at which the intermodulation harmonic current is of higher order and it can be calculated with the help of Integral Function Method (IFM). In Device C, the IMD3 degrades because of decrement in VIP3 due to increased $g_{m3}$ values, and it is evident that Device A and B provide a better response in terms of IMD3 than Device C.

For minimum distortion in device operation, values of HD2 and HD3 must be minimum. In this comparative study from Eq.11, 12, 13, Device C shows elevated values of distortions for HD2 and HD3. Therefore, the Device C's results are not adequately satisfying for both analog and linearity parameters as compared to Device A and B.

The above-mentioned parameters are calculated by the following equations:

$$IMD3 = \left(\frac{9}{2}\times(VIP3)^3 \times g_{m3}\right)^2 \times R_S \qquad (11)$$

$$HD2 = 0.5V_a \frac{\left(\frac{dg_{m1}}{dV_{GT}}\right)}{2g_{m1}} \qquad (12)$$

$$HD3 = 0.25V_a^2 \frac{\left(\frac{d^2 g_{m1}}{dV^2{}_{GT}}\right)}{6g_{m1}} \qquad (13)$$

**9.3. Small signal behavior modeling:**

Non-quasi-static (NQS) small-signal equivalent Ckt. is presented, used in operation of strong inversion region for the extraction of RF small-signal parameters of Device A, B and C. Networks operating at μwave frequencies & RF, Y & S parameters are most widely taken, where admittances are obtained, if comparison done with currents and voltages as it is a challenge to estimate currents & voltages at elevated frequencies. The contribution of the extrinsic part of the Tx. dominates as the operating frequency escalates into terahertz range. MOSFET at RF, consists of parasitic components as well as the intrinsic part of the Tx. namely, the S/D resistances $R_s$ and $R_d$. Transconductance $g_m$ and intrinsic G-to-D conductance $g_{ds}$ also $R_{gs}$ and $R_{ds}$ are the distributed channel resistance, $C_{gd}$ as well as $C_{gs}$ are the intrinsic G-to-D capacitance and G-to-S capacitance respectively [4]. MOSFETs used in a two-port configuration with B and S connected to the ground ($V_S$=$V_B$=0V) for RF measurements.

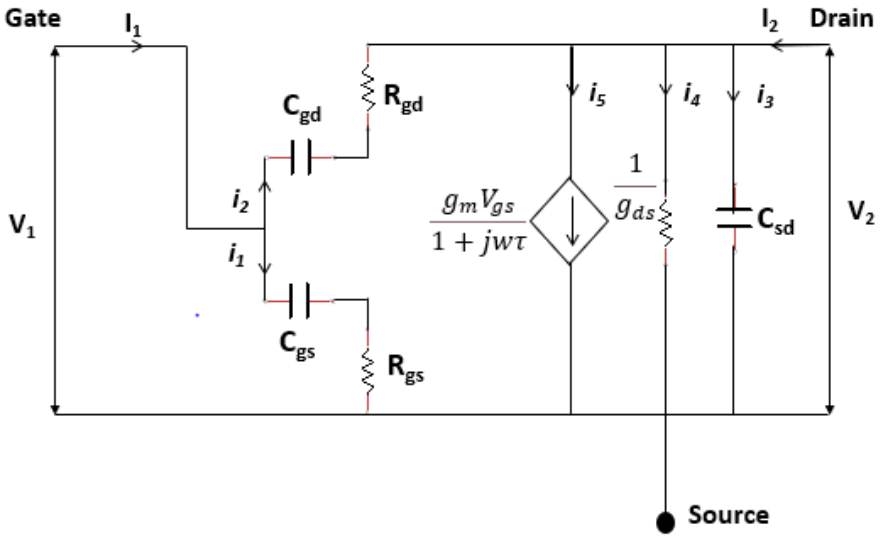



Fig.33. NQS small-signal equivalent Ckt. of an RF MOSFET

### 9.3.1. Admittance (Y) parameters:

The Tx. can be expressed as a small-signal equivalent Ckt. at elevated frequencies to generate its Y-parameter ($Y_{11}$, $Y_{12}$, $Y_{21}$, $Y_{22}$). Under ac short-Ckt. conditions the Y parameters are defined either at the O/P or at the I/P terminal and the values are dependent on the dc bias conditions as well as on the operating frequency. AC currents at low frequencies and voltages are measured however these parameters are measured at elevated frequencies which are difficult to measure. Frequencies of higher values, another set of parameters known as scattering(S) parameters are examined.

Y-parameters are estimated:

Net current at the i/p port,

$$I_1 = i_1 + i_2 \qquad (14)$$

Net current at the o/p port,

$$I_2 = i_3 + i_4 + i_5 - i_1 \qquad (15)$$

Through nodal analysis at i/p node,

$$\frac{V_1}{X_1}+\frac{V_2-V_1}{X_2}=0 \qquad (16)$$

$$\frac{V_2}{X_3}+\frac{V_2-V_1}{X_2}+\frac{g_m V_{gs}}{1+jw\tau}=0 \qquad (17)$$

where

$$X_1=\frac{1+jwR_{gs}C_{gs}}{jwC_{gs}},\ X_2=\frac{1+jwR_{ds}C_{ds}}{jwC_{ds}},\ X_3=\frac{1}{g_{ds}+jwC_{sd}}$$

By solving Equations (16) and (17), and using approximations

$$w^2R_{gs}^2C_{gs}^2<<1,\ w^2R_{gd}^2C_{gd}^2<<1,\ w^2\tau^2<<1$$

Short Ckt. i/p admittance

$$Y_{11}\cong w^2(R_{gs}C_{gs}^2+R_{gd}C_{gd}^2)+jw(C_{gs}+C_{gd}) \qquad (18)$$

$$Y_{11}\cong w^2(\alpha+\beta)+jw(C_{gs}+C_{gd}) \qquad (19)$$

Where $\alpha=R_{gs}C_{gs}^2,\ \beta=R_{gd}C_{gd}^2$

Thus, short-Ckt. o/p admittance is given by

$$Y_{22}\cong g_{ds}+w^2\beta+jw(C_{gd}+C_{sd}) \qquad (20)$$

Short-Ckt. forward transfer admittance:

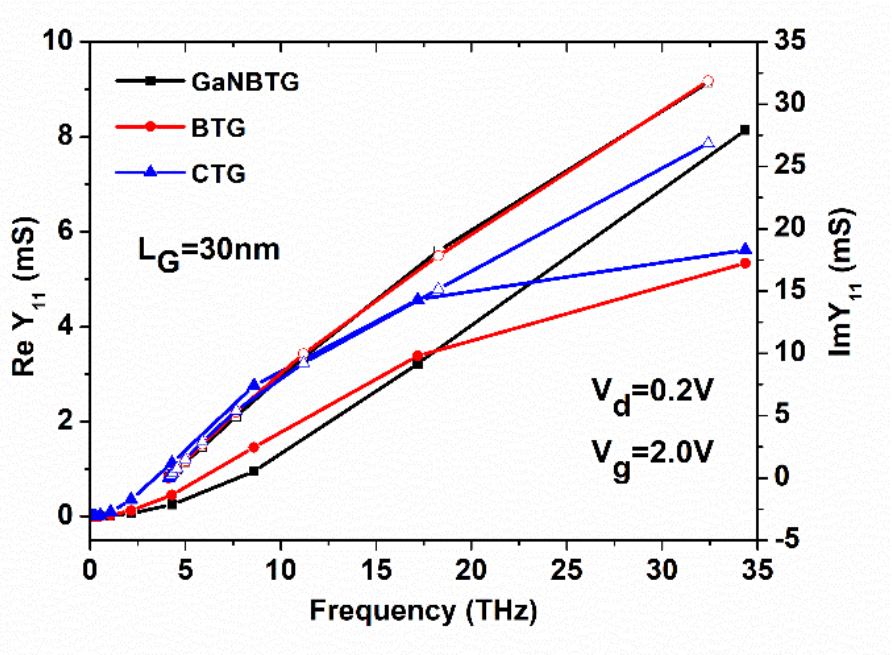
$$Y_{12}\cong -w\beta-jwC_{gd} \qquad (21)$$

Short-Ckt. reverse transfer admittance:

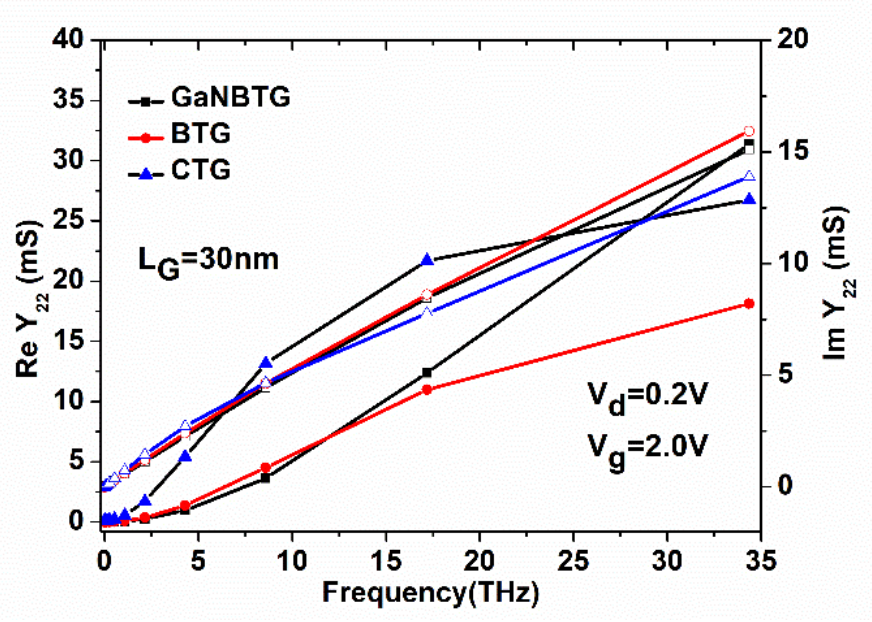
$$Y_{21}\cong -w^2\beta-jwC_{gd}+g_m(1+\tau) \qquad (22)$$

Short-Ckt.I/P admittance $Y_{11}$ and short-Ckt O/p admittance $Y_{22}$ have been evaluated for Device C and compared with Device A and B are shown in Fig. 34(a) and (b), $Y_{11}$ and $Y_{22}$ are elevated in Device C as comparison to Device A and B. $Y_{11}$ and $Y_{22}$ should be low in RF region for the better performance of the device[4]. Short-Ckt. forward transfer admittance $Y_{12}$ and Short-Ckt. reverse transfer admittance $Y_{21}$ are both lower in case of Device C [See in Fig. 35 (a) & (b)].

Enhancement in Y-parameters will indicate the decrement in parasitic capacitances and also better transconductance [5].

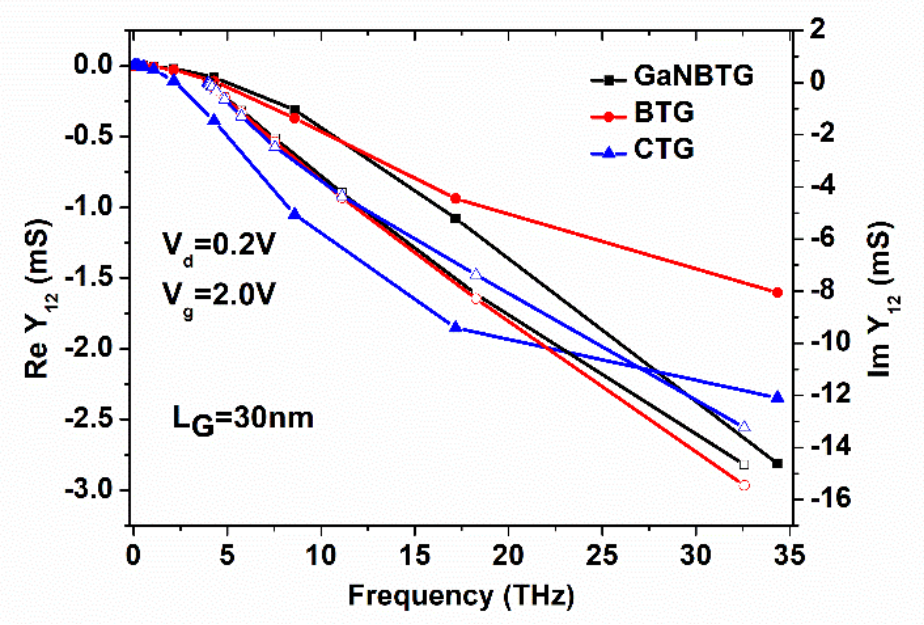



(a)

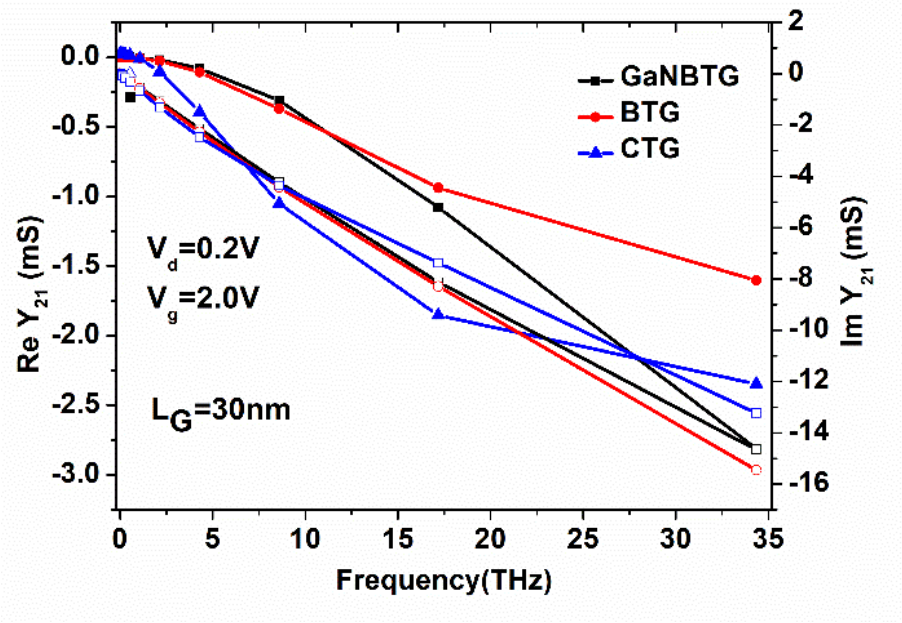



(b)

Fig.34. (a) and (b) Admittance parameters ($Y_{11}$ and $Y_{22}$), w.r.t. frequency.




(a)




(b)

Fig.35. (a) and (b) Admittance parameters ($Y_{12}$ and $Y_{21}$), w.r.t. frequency

### 9.3.2. Scattering parameters:

At elevated frequencies, extraction of S-parameters is the best optimal method to study the small signal behavior of MOSFET. Fig.36. and 37 shows the S-parameters which are simulated as well as modeled where the bias conditions are kept same for the Device A, B and C.

S-parameters, the i/p reflection coeff. at port-1 $S_{11}$ & the o/p reflection coeff. at port-2 $S_{22}$ which accounts for quality of the match. From Fig.36(a) and (b) (Eqs. 23,24) $S_{11}$ and $S_{22}$ reduces the frequency and reduction is more. Reverse isolation parameter $S_{12}$ and forward transmission

coefficient $S_{21}$ describes the value of feedback from the o/p of an amplifier [6] to i/p of an amplifier. $S_{12}$ decreases in the Device C as compared to other two devices[7]. The decrement in $S_{12}$ is observed due to the lower values of Z-parameters.

Similarly, $S_{12}$ and $S_{21}$ are calculated as follows:

$$S_{11} = \frac{(Z_{11} - Z_{01}^{*})(Z_{22} + Z_{02}) - Z_{12}Z_{21}}{(Z_{11} + Z_{01})(Z_{22} + Z_{02}) - Z_{12}Z_{21}} \tag{23}$$

$$S_{11} = \frac{\left(\frac{g_{ds} + w^2\beta + jw(C_{gd} + C_{sd})}{\chi} - Z_{01}^{*}\right)\left(\frac{w^2(\alpha+\beta) + jw(C_{gd} + C_{gs})}{\chi} + Z_{02}\right) - \left(\frac{-w\beta + jwC_{gd}}{\chi}\right)\left(\frac{w^2\beta + jwC_{gd} - g_m(1+\tau)}{\chi}\right)}{\left(\frac{g_{ds} + w^2\beta + jw(C_{gd} + C_{sd})}{\chi} + Z_{01}\right)\left(\frac{w^2(\alpha+\beta) + jw(C_{gd} + C_{gs})}{\chi} + Z_{02}\right) - \left(\frac{-w\beta + jwC_{gd}}{\chi}\right)\left(\frac{w^2\beta + jwC_{gd} - g_m(1+\tau)}{\chi}\right)} \tag{24}$$

$$S_{11} = \frac{\left(\frac{g_{ds} + w^2\beta + jw(C_{gd} + C_{sd})}{\chi} - Z_{01}^{*}\right)\left(\frac{w^2(\alpha+\beta) + jw(C_{gd} + C_{gs})}{\chi} + Z_{02}\right) - \left(\frac{w\beta + jwC_{gd}}{\chi}\right)\left(\frac{w^2\beta + jwC_{gd} - g_m(1+\tau)}{\chi}\right)}{\xi} \tag{25}$$

Similarly,

$$S_{22} = \frac{(Z_{11} + Z_{01})(Z_{22} - Z_{02}^{*}) - Z_{12}Z_{21}}{(Z_{11} + Z_{01})(Z_{22} + Z_{02}) - Z_{12}Z_{21}} \tag{26}$$

$$S_{22} = \frac{- \left(\frac{w\beta + jwC_{gd}}{\chi}\right)\left(\frac{w^2\beta + jwC_{gd} - g_m(1+\tau)}{\chi}\right)}{\left(\frac{g_{ds} + w^2\beta + jw(C_{gd} + C_{sd})}{\chi} + Z_{01}\right)\left(\frac{w^2(\alpha+\beta) + jw(C_{gd} + C_{gs})}{\chi} + Z_{02}\right) - \left(\frac{w\beta + jwC_{gd}}{\chi}\right)\left(\frac{w^2\beta + jwC_{gd} - g_m(1+\tau)}{\chi}\right)} \tag{27}$$

$$S_{22} = \frac{-\left(\frac{w\beta + jwC_{gd}}{\chi}\right)\left(\frac{w^2\beta + jwC_{gd} - g_m(1+\tau)}{\chi}\right)}{\xi} \qquad (28)$$

Thus, $S_{12}$ & $S_{21}$-

$$S_{12} = \frac{2Z_{12}(R_{01}R_{02})^{1/2}}{(Z_{11}+Z_{01})(Z_{22}+Z_{02}) - Z_{12}Z_{21}} \qquad (29)$$

$$S_{12} = \frac{2\left(\frac{w\beta + jwC_{gd}}{\chi}\right)(R_{01}R_{02})^{1/2}}{\left(\frac{g_{ds} + w^2\beta + jw(C_{gd}+C_{sd})}{\chi} + Z_{01}\right)\left(\frac{w^2(\alpha+\beta) + jw(C_{gd}+C_{gs})}{\chi} + Z_{02}\right) - \left(\frac{w\beta + jwC_{gd}}{\chi}\right)\left(\frac{w^2\beta + jwC_{gd} - g_m(1+\tau)}{\chi}\right)} \qquad (30)$$

$$S_{12} = \frac{2\left(\frac{w\beta + jwC_{gd}}{\chi}\right)(R_{01}R_{02})^{1/2}}{\xi} \qquad (31)$$

Similarly,

$$S_{21} = \frac{2Z_{21}(R_{01}R_{02})^{1/2}}{(Z_{11}+Z_{01})(Z_{22}+Z_{02}) - Z_{12}Z_{21}} \qquad (32)$$

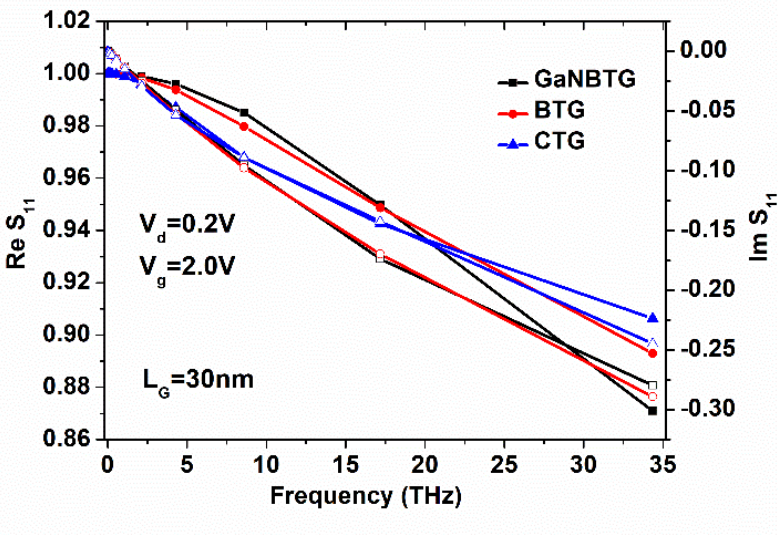
$$S_{21} = \frac{2\left(\frac{w^2\beta + jwC_{gd} - g_m(1+\tau)}{\chi}\right)(R_{01}R_{02})^{1/2}}{\left(\frac{g_{ds} + w^2\beta + jw(C_{gd}+C_{sd})}{\chi} + Z_{01}\right)\left(\frac{w^2(\alpha+\beta) + jw(C_{gd}+C_{gs})}{\chi} + Z_{02}\right) - \left(\frac{w\beta + jwC_{gd}}{\chi}\right)\left(\frac{w^2\beta + jwC_{gd} - g_m(1+\tau)}{\chi}\right)} \qquad (33)$$

Where,

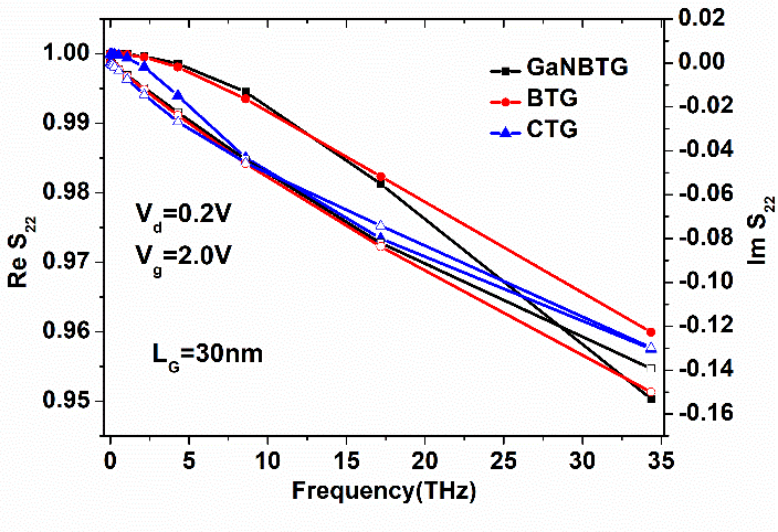
$$\xi = \left(\frac{g_{ds} + w^2\beta + jw(C_{gd}+C_{sd})}{\chi} + Z_{01}\right)\left(\frac{w^2(\alpha+\beta) + jw(C_{gd}+C_{gs})}{\chi} + Z_{02}\right) - \left(\frac{w\beta + jwC_{gd}}{\chi}\right)\left(\frac{w^2\beta + jwC_{gd} - g_m(1+\tau)}{\chi}\right)$$

and,

$$\chi = jw(C_{gs}g_{ds} + C_{gd}g_{ds} + C_{gd}g_m + \tau C_{gd}g_m)$$
$$+ jw^3(\alpha C_{gd} + \beta C_{gs} + C_{sd}(\alpha + \beta)) + \alpha\beta w^4$$
$$+ w^2(\alpha g_{ds} + \beta g_{ds} - C_{gs}C_{sd} + \beta g_m(1+\tau) + C_{gd}^2)$$

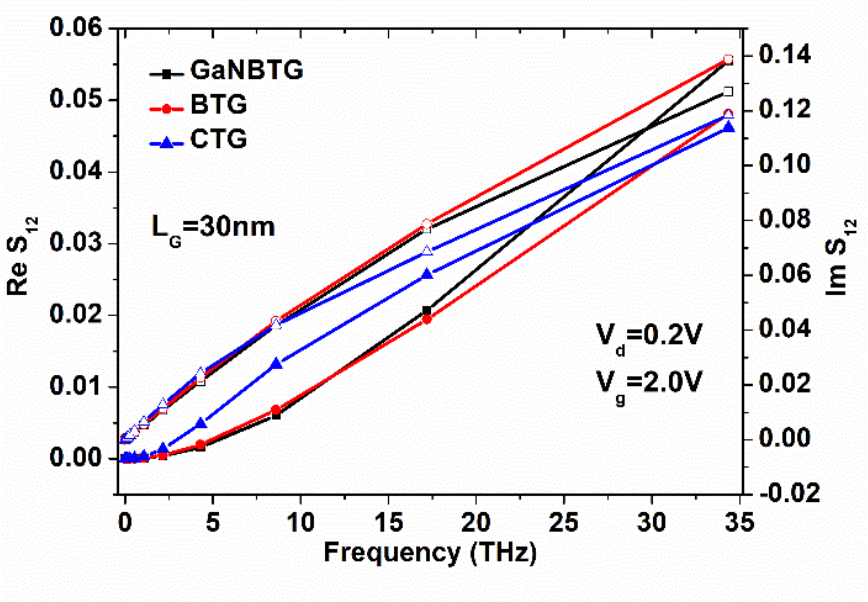



(a)

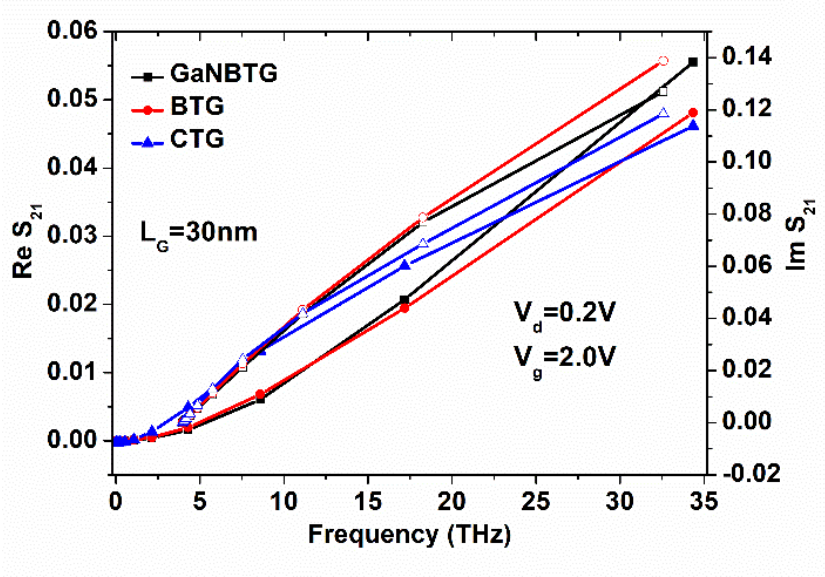



(b)

Fig.36. (a) and (b) Scattering parameters ($S_{11}$ and $S_{22}$), w.r.t. frequency




(a)




(b)

Fig 37. (a) and (b) Scattering parameters ($S_{12}$ and $S_{21}$), w.r.t. frequency

# CHAPTER-10
## CONCLUSION

This Report features three devices dissecting the chance of enhancing the performance of a Device A and B and downsizing simultaneously. The electrical characteristics and performance factors of the proposed devices are analyzed and contrasted with Device A and B, and observed outcomes are defended for each device. We see that SCEs are limited by the presence of the buffer layer and advancement in the outcomes was seen on supplanting Si with GaN. Moreover, in Device C lower OFF-current was perceived, leads to efficient energy consumption.

Device C exhibits higher O/P characteristics at 300K on account of increased electron mobility, and enhanced $I_{ds}$ also $I_d$-$V_g$ for the same $V_g$, increased $I_d$ is observed attributable to elevated- dielectric of the buffer. It is also perceived that FOMs for analog applications of Device C is enhanced on account of elevated mobility of electron, critical EF strength than Si considering for increased switching speed [31]. Device C with the stacking of $HfO_2$ not only enhances the analog parameters however, the performance parameters of the proposed device [31]. However, analog and low-power elevated-linearity parameters of Device C in comparison to Device A and B are not up to the mark and need more improvement.

This research also discusses the μwave parameters with the discussion of small signal modeling of Device C, i.e., admittance and scattering parameters. Reduction of SCEs and elevated ON current improves the gain. The results of presented model consisting small-signal parameters with simulated results are acquired at THz range and validates the small-signal model. Outcomes shows that the Device C needs more investigation for superiority of RF/μwave applications.

# CHAPTER-11
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