DESIGN OF ENERGY EFFICIENT TRANSCEIVER BLOCKS FOR WIRELESS SENSOR NODES

SAJI M ANTONY

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY, NEW DELHI

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SAJI M ANTONY

(2K14/PHDEC/01)

under the Guidance of

Prof. S. Indu
Department of Electronics and Communication Engineering,
Delhi Technological University, Delhi

and

Prof. Rajeshwari Pandey
Department of Electronics and Communication Engineering,
Delhi Technological University, Delhi

DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY, NEW DELHI

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CERTIFICATE

This is to certify that the thesis titled "**Design of Energy Efficient Transceiver Blocks for Wireless Sensor Nodes"** being submitted by Saji M Antony to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi, for fulfilment of requirements for award of degree of Doctor of Philosophy, is a record of bonafide research work carried out by her under our guidance and supervision. In our opinion, the thesis has reached the standards fulfilling the requirements of the regulations relating to the degree.

It is also certified that this thesis has not been submitted to any other university or institute for the award of any degree or diploma.

Prof. S. Indu
Professor
Department of Electronics and - Communication Engineering,
Delhi Technological University,
Delhi - 110042

Prof. Rajeshwari Pandey
Professor
Department of Electronics and - Communication Engineering,
Delhi Technological University,
Delhi - 110042

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Contents

Certificate ……. **i**

Acknowledgements **ii**

List of Figures …….. **vi**

List of Tables **viii**

Abstract …….. ……. **ix**

1. Introduction …… **1**

1.1. Importance of the design of energy efficient wireless sensor nodes 2

1.2. Problem definition …… 3

1.3. Overview of the research work 5

1.3.1. Design of high speed low power vedic multipliers for wireless sensor nodes. 5

1.3.2. Design of energy efficient ALU using Vedic multipliers 6

1.3.3. Design of improved power amplifiers for making energy efficient transceiver blocks 6

1.3.4. Design of an efficient solar energy harvesting system for wireless sensor nodes 7

1.4. Thesis layout …….. 7

2. Energy efficient wireless sensor nodes: a review …… **10**

2.1. Low power wireless sensor nodes 11

2.2. Multipliers for sensor nodes ……. 14

2.3. Design of ALU for sensor nodes 18

2.4. Power Amplifiers for energy efficient Transceiver Blocks 20

2.5. Energy harvesting systems for wireless sensor nodes 22

2.6. The thesis in perspective: Motivation and Contributions …….. 25

3. High speed low power Vedic multipliers for wireless sensor nodes 30
3.1. Introduction 30
3.2. State of the art 31
3.3. Problem formulation 34
3.4. Methodology …… 35
3.4.1. Vedic mathematics 35
3.4.1.1. Urdhva Triyakbhyam Sutra**.** 36
3.4.2. Multiplexer based adders 39
3.5. Simulation Results ……. 41
3.5.1. Simulation of proposed 8-bit Urdhva Multiplier 41
3.5.2. Simulation of 8-bit conventional Urdhva Multiplier 42
3.5.3. Simulation of 16-bit Multipliers 43
3.5.4. Synthesis …….. 44
3.5.5. Results 45
3.6. Conclusion 49
4. Energy efficient ALU using Vedic multipliers ……. **51**
4.1. Introduction 51
4.2. State of the Art 52
4.3. Problem formulation 56
4.4. Methodology …….. 56
4.4.1. Artificial Neural Networks (ANN) 57
4.4.2. Components of ANN 59
4.4.3. Advantages of ANN 61
4.4.4. Design of Vedic neuron 61
4.4.5. Design of ALU using Vedic neurons 62
4.5. Simulation results …… 65
4.5.1. Simulation of Vedic neuron 65
4.5.2. Simulation of proposed ALU 67
4.5.3. Results 73
4.6. Conclusion …….. …….. 75

5. Design of improved power-amplifiers for making energy efficient transceiver blocks …… 76

5.1. Introduction 76

5.2. State of the Art 77

5.3. Problem formulation ……. …… 80

5.4. Methodology 80

5.4.1. Power Amplifier 81

5.4.1.1. Amplification Methods 81

5.4.2. Class E Power Amplifier …….. 82

5.4.2.1. The Cascode Amplifier 84

5.4.2.2. Common drain common source (CD-CS) configuration 85

5.5. Simulation results …….. …… 85

5.6. Conclusion 92

6. An efficient solar energy harvesting system for wireless sensor nodes …….. **93**

6.1. Introduction 93

6.2. State of the Art 94

6.3. Problem formulation 96

6.4. Methodology 96

6.4.1. Solar Energy Harvesting (SEH) system 98

6.4.2. Modified Solar Energy harvesting System for WSN Nodes 100

6.5. Results 103

6.6. Conclusion 105

7. Conclusion **108**

7.1. Summary of Work Done 109

7.2. Future Work 111

Annexure ……. 113

References 113

Published works 138

List of Figures

2.1 Block diagram of a Sensor Node …… 12

3.1 Urdhva multiplication method for 2 bit binary numbers …… 37

3.2 Block diagram of 2x2 bit Urdhva multiplier 37

3.3 Line diagram for 4 bit Urdhva multiplication ……. 38

3.4 Hardware architecture for 4-bit Urdhva multiplier ……. 38

3.5 Block diagram for 4x4 Vedic multiplier using 2x2 multipliers .. 39

3.6 Full adder with XOR gates and MUX …….. 40

3.7 Simulation result of proposed 8-bit Urdhva multiplier …….. 42

3.8 Simulation Result of conventional 8-bit Urdhva multiplier…..... 42

3.9 Simulation result of proposed 16-bit Urdhva multiplier……. 43

3.10 Simulation result of 16-bit conventional Urdhva multiplier ….. 43

3.11 RTL view of full adder of (a) Proposed (b) Conventional Urdhva multipliers ……. ……. 44

4.1 Block diagram of nervous system ……. 58

4.2 Basic artificial Neuron model …… 59

4.3 Hardware implementation of single neuron …….. 60

4.4 Hardware implementation of Vedic neuron …… …….. 62

4.5 Block diagram of ALU circuit ……. …. …….. 64

4.6 Simulation results of 8-bit Vedic multiplier …….. 66

4.7 Simulation result of activation function ……. 66

4.8 Simulation result of Vedic Neuron ……. 67

4.9 Simulation results of 8-bit Adder ……... 69

4.10 Simulation results of 8-bit Subtractor …… … 69

4.11 Simulation results of 8-bit Incrementor ……. …… ….. 70

4.12 Simulation results of 8-bit decrementor ……. ……. …. 70

4.13 Simulation results of 8-bit AND gate ……. 71
4.14 Simulation results of 8-bit OR gate ……. 71
4.15 Simulation results of 8-bit NOT gate …….. …… 72
4.16 Simulation results of 8-bit XOR gate 72
4.17 Simulation results of Vedic ALU ……... 73
5.1 Block diagram of transceiver in a sensor node ……. 77
5.2 Circuit of class E power amplifier …….. 83
5.3 Class E amplifier with double cascading ……..... 86
5.4 Simulation results of class E amplifier with double cascoding .. 86
5.5 Frequency response of double cascode amplifier ……... 87
5.6 Class E amplifier with CD-CS cascading ……... 88
5.7 Simulation results of Class E amplifier with CD-CS cascading. 88
5.8 Frequency response of CD-CS cascading ……... 89
5.9 Simple class E amplifier circuit …….. 90
5.10 Simulation results of simple class E amplifier circuit……. 90
5.11 Frequency response of class E Amplifier ……... 91
6.1 Components of SEH system ……... 99
6.2 Block diagram of proposed SEH system …… 100
6.3 Circuit diagram of solar harvesting for wireless sensor node …. 102
6.4 Photo of design implementation in lab ……... 102
6.5 Circuit diagram of inverter ……. 103

List of Tables

3.1 Logical effort for different inputs of CMOS gates ……. 41

3.2 Synthesis results of logic utilization for 4-bit multipliers …….. 46

3.3 Synthesis results of logic utilization for 8-bit multipliers …….. 46

3.4 Synthesis results of logic utilization for 16-bit multipliers …… 47

3.5 Synthesis results on delay ……. …… 47

3.6 Summary of synthesis results …… …… …….. … 48

3.7 Delay comparisons reported by previous approaches ……. .. 48

3.8 Area comparisons reported by previous approaches ….. …….. 49

3.3 Performance analysis …….. 49

4.1 Delay comparison …….. 74

4.2 Device utilization summary for Vedic logic Vs. Conventional logic of eight bit ALU …… - 74

4.3 Performance analysis ……. 75

5.1 Performance comparison table …….. 91

6.1 Experimental results …….. 104

6.2 Performance comparison with existing system ……. ……... 104

ABSTRACT

Sensor networks have been recognised as one of the most advanced technologies of the 21st century with vast practical applications. The life of a sensor network is mainly determined by its energy consumption. Commercially available sensor nodes are battery driven devices. As most sensor nodes are deployed widely scattered and in isolated areas, replacing battery is not an option. This dissertation focuses on extending the lifespan of sensor networks by reducing energy consumption in design and operation of sensor nodes.

The study goes in depth to analyse the state of art technology to achieve energy efficiency in sensor nodes and identify scope for further research in this field. In the architecture of sensor nodes, multipliers are the main blocks for designing an energy efficient processor. Vedic Mathematics provides principles of high speed multiplication. The main reason for power dissipation in multiplier circuit is due to power dissipation of full adder circuit. Low power multipliers have been designed by using low power adders. Motivated by this, a high speed Vedic multiplier has been designed using multiplexer based adder. When compared with existing Vedic multipliers, proposed designs showed significant improvement in reduction of delay and energy consumption.

Sensor nodes consume maximum power during data communication. So processing data locally at each node in a sensor network is important for minimizing power consumption. High processing speed and low area designs are in ever growing demand. In order to predict outcomes, based on previous inputs, ALU can be designed with neurons. Processing speed of ALU can be improved by replacing conventional multipliers with Vedic multipliers. This research work suggests implementation of high speed ALU using Vedic neurons. The analysis of the results shows that the proposed design leads to

reduction in the delay and reduction in LUT count (an indicator of area) of the ALU.

Use of energy efficient power amplifiers is an essential requirement for sensor nodes, as power amplifiers are responsible for the main power consumption in the transceivers of sensor nodes. Again, wider band width is another important requirement for power amplifiers used in sensor transceivers especially in wireless visual sensor networks and wireless multimedia sensor networks. Reliability of a power amplifier can be increased by designing it at smaller supply voltage. This thesis suggests improvements in design of power amplifier in class E configuration, for transceivers in wireless sensor nodes. In order to achieve wider band width, cascade of common drain followed by common source in class E configuration has been designed; and for more reliable operation with higher efficiency, class E in double cascoded has been implemented. The proposed designs, when simulated in SPICE, higher efficiencies and band widths have been achieved.

This research also explored to design a robust solar energy harvesting system to enhance life time of sensor nodes. Proposed solar energy supply system mainly consists of a solar panel, rechargeable battery and a control circuit. To obtain sufficient voltage to charge battery, electrical energy generated through panel is boosted by boost converter. Different sensor nodes are supplied with energy from this system. An inverter is also designed for AC applications. Experimental results show that this compact, self-sufficient system enables outdoor based wireless sensor network nodes to operate successfully for longer periods.

CHAPTER 1.

INTRODUCTION

A wireless sensor network (WSN) comprises of spatially distributed autonomous devices employing sensors to cooperatively monitor environmental or physical conditions, like sound, temperature, vibration, light, humidity, motion, pollutants or nature of biological organisms at varying locations [1]-[4]. Wireless sensor networks were originally developed for defence applications like battle field surveillance. Now a days WSNs are used in many non-military applications such as precision agriculture, transportation, environment and habitat monitoring, structural health monitoring, medical monitoring, home automation, traffic control, etc [5]-[8]. Sensor networks are basically different from standard communication networks as the aim of sensor network is to monitor a phenomenon over space and time and not to just send data from one node to another. So, the underlying communication infrastructure is used to achieve a larger objective of geo-temporal sampling and the subsequent detection and classification of events of interest [9], [10].

Sensor networks have been recognised as one of the most advanced technologies of the 21st century. Current developments in micro-electro-

mechanical systems (MEMS), advances in the fabrication and integration of sensing and communication technologies have simplified the design of multifunctional sensor nodes and have enabled the development of smaller size sensor nodes that are low-cost and low power consuming. They can sense various information from the surroundings, and they have capabilities of data processing, communication, storage etc. The sensor nodes are therefore capable of collecting, processing, storing and communicating data to other nodes in the network and even to outside the network.

1.1 Importance of the Design of Energy Efficient Wireless Sensor Nodes

A wireless sensor network consists of large number of sensor nodes, densely deployed in region, either inside a phenomenon or very close to it. It gives significant improvement over the traditional sensors. When compared to the deployment of a few very accurate and high expensive sensors, using a large number of inexpensive sensors has many advantages, like achieving more spatial resolution, reduced total system cost, easy to deploy, robustness against failures from distributed operations, less obtrusiveness and uniform coverage [11], [12].

The life of a sensor network is mainly determined by its energy consumption. Commercially available sensor nodes are driven by batteries. As most sensor nodes are deployed widely scattered and in isolated and inaccessible areas, replacing battery is not an option. Hence, low energy consumption requirement is the most crucial constraint of sensor nodes, as life of a sensor network mainly depends on energy consumption of sensor nodes. In many applications large number of networked sensors require

unattended operations. Also, applications such as health monitoring of animals or humans, require the sensor nodes to be unobtrusive in the normal functioning of the individual. Another factor that highlights the importance of low energy consumption requirement is the fact that battery technology itself hasn't advanced as much as the computer technology in the last few decades. So, energy utilized by each part of individual nodes precisely affects the life of the complete network. This leads energy optimization more complicated, as it involves increasing life of sensor network by reducing energy consumption. This can be achieved with energy awareness in each and every step of design and operation [13]-[16].

1.2 Problem Definition

Like any other technology, sensor networks also have some key issues that need to be understood in order to completely appreciate the contributions of this work. This dissertation focuses on extending the lifespan of sensor networks by reducing energy consumption in design and operation of sensor nodes. The study goes in depth to analyse the state of art technology to achieve energy efficiency in sensor nodes and identifies scope for further research in this field.

Due to diverse application domains of sensor networks, a variety of data types are included from temperature, pressure, magnetic field, acceleration etc. The data collected by these sensors is rarely forwarded in raw form. It is subject to some form of signal processing mainly to reduce communication costs. The size of sensors and actuators have made down to the millimetre scale due to advancement in MEMS. Also advances in VLSI technology have made very small button sized computers a reality. However, such devices, are designed with low cost in mind and it results

limited computational resources, like CPU speed and memory. Based on these observations, we address the following problems in this thesis.

a) In the architecture of sensor nodes, multipliers are the main structure for designing an energy efficient processor. Many research works have been focused on design of low power multiplier algorithms, but it is not explored for real time applications, using efficient adder circuits with more power savings and speed.

b) Similarly, for application-oriented processors, not much has been explored in the design of ALU. A conventional ALU is less capable of intelligently predicting outcomes based on previous inputs. Its neural counterpart, on the other hand, aims at improving its prediction capabilities by employing an activation function and making it an intelligent ALU.

c) In a sensor node, most of the power is consumed in transceivers; and in transceivers the most significant power consumption is contributed by power amplifiers. Requirement of high efficiency power amplifiers without reducing bandwidth and sensitivity demands new design strategies. Adequate work has not been found in the design of power amplifiers for higher efficiency of the transceiver blocks.

d) Various harvesting techniques are available such as solar energy, wind energy, piezo electric energy, etc. Among these, currently most matured technology is based on solar cells and it gives high power density. But efficient solar energy harvesting technology for small systems have not been explored much.

1.3 Overview of the Research Work

This dissertation focuses on extending the lifespan of sensor networks by reducing energy consumption in design and operation of sensor nodes. The study goes in depth to analyse the state of art technology to achieve energy efficiency in sensor nodes and identified scope for further research in this field.

1.3.1 Design of high speed low power Vedic multipliers for wireless sensor nodes.

In the architecture of sensor nodes, design of multipliers plays a major role in making an energy efficient processor. The speed of multiplier is limited by the speed of adders used in partial product addition [17]. Fast multiplication can be achieved by using the principles of Vedic mathematics [18]-[21]. From the performance analysis on delay, power dissipation, transistor count etc, it is observed that full adder with XOR and multiplexer (MUX) gives best performance [22]. Motivated by this, a high speed Vedic multiplier based on Urdhva Triyakbhyam Sutra is proposed in this research. Summation of partial products is done with high speed MUX based full adders. The proposed design gives much less delay and power dissipation as compared to other conventional Vedic multipliers.

1.3.2. Design of energy efficient ALU using Vedic multipliers.

This thesis also focuses on designing a high speed ALU using Vedic neurons. A conventional ALU is incapable of intelligently predicting outcomes based on previous inputs [23]-[25]. Its neural counterpart, on the other hand, aims at improving its prediction capabilities by employing an activation function and making it an intelligent ALU. But ALU designed with neurons suffers from bulky and slow architecture. This can be solved by implementing the Vedic logic in all arithmetic and logical operations performed. The Vedic logic helps in performing faster calculations by utilizing simple techniques to solve complex problems. This provides a faster and a smarter ALU design. This work is intended for laying a foundation for the intelligent sensor nodes by implementing Vedic logic on neural platforms.

1.3.3 Design of improved power amplifiers for making energy efficient transceiver blocks.

The essential quality required for a power amplifier in wireless sensor nodes is its efficiency. Power amplifier with low power supply gives more reliable operation. But overall gain and efficiency are decreased due to reduced power supply [26], [27]. In class E power amplifiers, these combinations do not exist. So our study focuses on modifications for basic class E amplifier to achieve efficiency without reducing bandwidth and sensitivity at lower power supply. Two different configurations using basic class E amplifier are proposed in this work. The first configuration is class E amplifier with double cascoding and second design is class E amplifier designed using common drain followed by common source (CDCS) cascading. The proposed designs give better efficiency, and more reliable operation with higher bandwidth.

1.3.4 Design of an efficient solar energy harvesting system for wireless sensor nodes.

Nowadays various harvesting techniques from the renewable energy sources are available to design self-powered wireless sensor nodes. Solar energy, wind energy and piezo electric energy are some of the available ambient energy sources [28]. Among these, currently most matured technology is based on solar cells and it gives high power density [29]. Requirement of small sized sensor nodes demands small solar panels in the harvesting system which leads to design a compact and simple solar energy harvesting system (SEH) for sensor nodes. This research also designed a solar harvester for WSN nodes with compact models of solar panel and harvesting circuits to increase the life span of battery. Proposed design combines energy harvesting system with a compact energy storage device. It gives stable operation with high reliability, efficiency and less power loss.

1.4 Thesis Layout

1. Introduction

This chapter broadly covers the motivation and purpose of the outlined research topic. It contains the main idea for the development of the thesis along with different issues associated with energy efficiency of wireless sensor nodes.

2. Energy efficient wireless sensor nodes: A review

This chapter discusses the state of art techniques developed in existing research work in the field of “Design of Energy efficient Wireless

Sensor Nodes". It also highlights the inadequacies and deficiencies in the existing work that has stimulated the development of research objectives of the dissertation.

3. High speed low power Vedic multipliers for wireless sensor nodes

This chapter presents use of multiplexer based adder in designing a high-speed Vedic multiplier. It gives a brief introduction to Vedic mathematics and also cover multiplication techniques used in Vedic mathematics. This chapter concludes with results and comparative analysis with the related work.

4. Energy efficient ALU using Vedic multipliers.

This chapter introduces a high speed ALU, using Vedic neurons. It covers the problems encountered with implementation of ALU using neurons. Design of ALU using Vedic neurons is explained in this chapter, followed by results and comparisons with the existing methods in the literature.

5. Design of improved power amplifiers for making energy efficient transceiver blocks.

In this chapter, we propose improvements in the design of class E power amplifier for transceivers in wireless sensor nodes. Two different configurations using basic class E amplifier are discussed in this section. The first configuration is class E amplifier with double cascoding and second design is class E amplifier designed using common drain followed by common source (CDCS) cascading. Finally, analysis of results is done with various state of art techniques.

6. An efficient solar energy harvesting system for wireless sensor nodes

This chapter presents a solar energy harvester for wireless sensor nodes with compact models of solar panel and harvesting circuit. It introduces a suitable method for effective utilization of solar energy for small wireless sensor nodes and concludes with the analysis of obtained results.

7. Conclusion

This chapter contains the brief summary of the work done. We also outline the future scope of this work.

CHAPTER 2

ENERGY EFFICIENT WIRELESS SENSOR NODES: A REVIEW

Sensor networks are self-sustaining systems of nodes that co-ordinate amongst themselves autonomously but, their enhancement is restricted by the limitations of the devices used. First, they are restricted by power consumption, which leads to eventual device failure and in turn makes energy efficient communications an essential requirement. Their computing power is also limited, which prevents running of sophisticated network protocols. They also have limited bandwidth which constraints the amount of communication to be transmitted. Human intervention to keep the network up and running, in such conditions, is at the least a tedious job and mostly infeasible. It is for this reason that there is a continued effort to make sensor networks as autonomous as possible. Many research efforts are being focused towards overcoming the common issues that are peculiar to sensor networks.

Objective of the present study is to increase the life of sensor nodes by reducing the energy consumption of sensor nodes with suitable energy conserving designs. In this literature survey, the discussion is divided under the categories of multiplier and ALU design for sensor nodes, power amplifier configurations for transceivers of sensor nodes, and energy

harvesting systems for sensor nodes. Recently many research efforts have been directed towards overcoming the energy constrained nature of WSN nodes. Such efforts are mainly focused in improving energy efficient, intelligent software rather than in improving hardware. Due to the demand of low power sensor nodes in wide range of applications, recent research has been focused on every block of sensor nodes.

2.1 Low Power Wireless Sensor Nodes.

Wireless sensor networks consist of large number of sensor nodes deployed in target region or very close to it randomly. These nodes collect information from the surrounding and send through wireless transmission. Like any embedded system, sensor nodes also face the challenge of reducing energy consumption, as much as possible to maximize its operational life span without changing batteries. Therefore, one of the key objectives while designing sensor nodes is to minimize the power consumption. To reduce the power consumption of a sensor node, researchers preferred to employ both unique structural solutions and progressive power saving techniques. I F Akyildiz et al. focus on the importance of power management and power consumption in sensor networks [30]. A detailed analysis on wireless sensor networks has been discussed in this paper. The potential tasks and applications of WSN are explained and a survey has been conducted on the factors effecting the design of sensor network and on the communication architecture for sensor networks. Protocols and algorithms suitable for various layers are discussed in this paper. Reference [3] provides a detailed investigation of embedded sensor networks. Authors explore challenges in three major areas. Energy consumption, signal processing algorithms and self-configuration. Figure 2.1 shows block diagram of a sensor node [31].

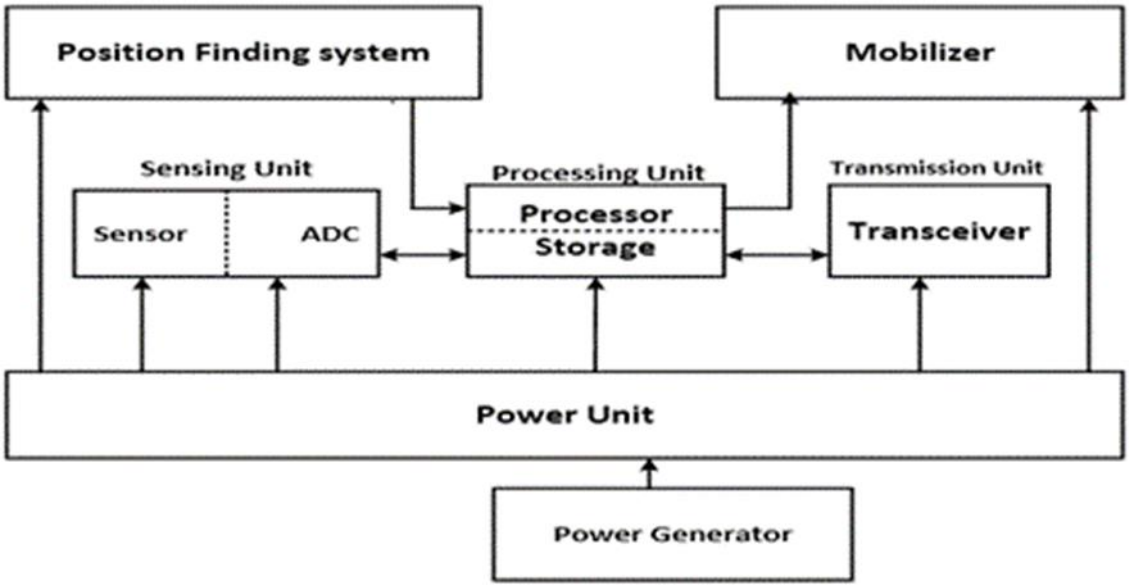


Figure 2.1. Block diagram of a Sensor Node [7].

As shown in Figure 2.1, sensor node consists of sensor unit, processor unit, power unit and transmission unit. Sensor unit consists of a sensor along with an analog-to-digital converter (ADC). Sensor unit converts physical inputs into electrical signals. These analog signals produced by sensors are converted to digital signals by ADC. Processor unit comprises of microcontrollers or microprocessors, which control sensors, execute communication protocol and signal processing algorithms on collected data. Transmission unit collects information from processor unit for transmitting to the outside world. Power unit monitors the battery power to sensor node. The main characteristics sensor nodes required to implement sensor networks are low cost, small size and low power [5]. Recent advances in micro-electro-mechanical systems (MEMS) have made it possible to bring the size of sensors and actuators down to the milli meter scale. Similarly, progresses in VLSI technology have made button sized

computers a reality. Such devices, however, are designed with low cost in mind and as a result the computational resources, such as CPU speed and memory are limited [32].

Characteristics of sensor networks are as under:

a) Self-organizing abilities,
b) Multi-hop routing and broadcast & short range communication,
c) Close deployment and collaborative efforts of sensor nodes,
d) Capability to change topology due to node failure and fading
e) Constraints on computing power, memory and transmission power.

These characteristics distinguish sensor networks from traditional ad hoc wireless networks [11]. Even though implementation of sensor networks and their applications uses ad hoc wireless networking techniques, most algorithms and protocols of wireless networks are not suited for sensor networks because of their unique features. Sensor nodes are based on broadcast communication standards, but many ad hoc networks use point to point communications. Due to the need for large quantity of sensors and high overhead (operating cost), sensors may not have global identification. Instead of traditional single hop communication, multi-hop communication gives less power consumption as neighbour nodes may be very close to each other due to dense deployment of large number of sensor nodes. Signal propagation effects in long distance wireless communication can be reduced in multi hop communication [30].

One of the most important constraints on sensor node is low power consumption requirements. Sensor nodes carry limited, irreplaceable power source. Therefore, traditional networks design to achieve high

quality while sensor network design focuses on power conservation. Many researchers are presently focused on developing designs to achieve these requirements [33]-[37].

2.2 Multipliers for Sensor Nodes.

The performance of a processor is mainly determined by its speed. In arithmetic operations, multiplication is an important fundamental function. Compared to other arithmetic operations like addition and subtraction, multiplication has large delay and complex algorithm. In many applications like digital signal processing (DSP) applications such as filtering, convolution, Fast Fourier Transform (FFT) etc. and arithmetic functions such as inner products, multiply and accumulate (MAC) unit, frequently use operations based on multiplication [38], [39].

In digital image processing systems multiplier is an important unit. In many signal processing applications such as weather forecasting, analysis of satellite data involve large amount of data and multiplier should be capable of handling this huge data quickly and efficiently so that entire operation is completed in minimum time. In addition to ALU, multipliers are used in other parts of processor design such as various data path units. For processing acquired signal in real time applications, high speed processing is an essential requirement [40], [41]. So demand for high speed multiplier circuit with reduced power consumption has been continuously increasing. Multiplication operations are complex and require more power consumption. Due to the demand of high speed processing and wide range of applications, many research efforts have been made on various multiplication algorithm to decrease the delay and power consumption [42]-[45].

A unique system of mathematics prevalent in ancient India is known as Vedic mathematics. Mathematics is known as mother of all other sciences. It is full of numbers and its mysteries. The ancient Indians understood these numbers and developed easy techniques to solve these mysteries. In ancient times, Indians employed these techniques in varying fields such as astrology, construction of temples, medical science etc., which may be the reason for India's rise as one of the richest countries in the world. This ancient Indian system of calculations were known as "Vedic Mathematics". The word 'Vedic' is derived from the word 'Veda' which means the store-house of all knowledge. Vedic mathematics is primarily consists of sixteen Sutras or techniques dealing with different branches of mathematics like algebra, arithmetics, geometry etc. Vedic Mathematics unveils the outstanding applications to algebraic equations, factorisations, complex multiplications, arithmetical calculations, quadratic and higher order equations, theory of numbers, partial fractions, squaring, cubing, square rooting, cube rooting, coordinate geometry and calculus etc [46].

In this ancient method, basic arithmetic problems were solved by simple, logical and powerful methods. Added advantage is its Consistency. Vedic Mathematics has emerged as a major topic for research due to these advantages. Among sixteen Sutras of Vedic approach, Urdhva Triyakbhyam and Nikhilam are used for multiplication. Vedic multipliers are the best compared to conventional ones and Urdhva Triyakbhyam Sutra architecture is more efficient compared to Nikhilam Sutra [47], [48]. It is well known from literature [49] that Nikhilam Sutra based multipliers expected to work for larger inputs, that is, inputs near to base (20% from the nearest base). Regularity and simplicity of Vedic Mathematics leads to

easy implementation in FPGA [50]. Another advantage of this approach is that all partial products required for multiplication are calculated much before actual multiplication begins. Based on the Vedic Mathematics algorithm, these partial products are added to obtain final product which leads to a very high speed approach [51], [52]. In addition, high speed multiplier designs based on Vedic mathematics consume low power too [53].

In reference [54], a high speed Vedic multiplier based on Urdhva Triyakhbyam Sutra is proposed. In this paper, multipliers with four, eight, sixteen and thirty two bits are implemented using Vedic technique and its performance has been compared with conventional method based multiplier which evidently shows that Vedic multipliers are much faster. For Vedic multipliers with large number of bits, design complexity reduces due to their hierarchical nature. Reference [55] presents a similar method for hierarchical multiplier design for Urdhva multiplier wherein 4x4 and 8x8 multipliers are designed using 2x2 multipliers. Comparison of Urdhva and Nikhilam multipliers is drawn in [56] for various bit multiplications starting from 8x8 bits to 64x64 bits.

For small inputs Urdhva multiplier performs better than Nikhilam multiplier and when size of multiplicand increases, Nikhilam multiplier performs much faster than Urdhva multiplier. So integrated Vedic multiplier architecture is proposed in [49], which is capable of selecting appropriate multiplier based on the given inputs. The work presented in [47] focuses on implementation and comparison of array, Urdhva and Nikhilam multiplier for 8bits, 16bits and 32 bits. It is observed that the Urdhva multiplier is best among the three. A high performance multiplier with low energy utilisation and small critical path is proposed in reference

[57] especially for DSP applications. This paper designs a high-performance low power consuming partial product accumulation tree for a multiplier using approximate adder. Approximate adder ignores the carry propagation by generating an approximate sum and an error signal. To overcome main limitations like power utilization, performance delay, and to achieve greater performance for real time applications various multiplier architectures have been explored and analysed in references [58] - [62].

The speed of multiplier is limited by the speed of adders used in partial product addition. Performance comparison of various adders is done in [63]. It is observed that carry save adder is having minimum delay, but among seven adder topologies carry increment adder has best balance between area and delay. Logic optimization of adders through technology independent mapping was proposed by R. Uma and P. Dhavachelvan in reference [22]. Concept of logical effort has been used to bring out the differences in performance of the various full adder configurations. The work presents 20 different logical constructions to implement one bit full adder circuit. From the performance analysis on delay, power dissipation, transistor count etc., it is observed that full adder with XOR and MUX gives best performance. Full adder with XNOR, NOT and MUX is the second optimized adder. The basic unit of the multiplier is an adder, so delay of multiplier can be reduced by reducing the delay of adder. So adders have a critical role, in the design of an efficient multiplier. To overcome crucial constraints like power utilization, speed, and to achieve greater performance, configurations of several adders have been discussed and reviewed in [64]-[69].

2.3 Design of ALU for Sensor Nodes.

Due to the wide range of applications, a lot of research has been focused on power dissipation, physical size and processor design of sensor nodes. The main difference of sensor networks from standard wireless communication networks is, sensor networks are used to detect some events, and not for just sending data from one node to another. Currently, sensor networks are mostly used to sense phenomena and act as information sources. On the occurrence of certain events they have to perform related actions; such as mobilizing robots in case a target is detected or activating water sprinklers in case of a fire. In such real time applications, quick responses should be automatically generated without any human intervention. To achieve fast acting and fault tolerant responses, it is desirable to design network as distributed as possible [70], [71].

The exact position of sensor nodes may not be predetermined or engineered. This permits random deployment in isolated regions or for disaster relief operations. These regions may include: in the atmosphere, inside buildings, in vehicles, under water and on bodies. So algorithms and protocols used in the sensor networks should have self-organizing abilities. Self-organization means that the network should acquire and retain the essential organizational structures for survival without depending upon human intervention [72]. So, sensor network should be able to execute functional operations through individual nodes. Another distinct characteristic of sensor networks is the coordinated attempt of sensor nodes in collecting the data. Instead of sending the raw data, sensor nodes use their computing abilities to locally carry out simple computations and transmit only partially processed, required data [73], [74]. Necessity of

prediction based monitoring in large sensor networks to increase energy efficiency and life time, is explained in [75].

In WSN, primary functions of sensor nodes are to detect events, process and transmit data. Therefore, major domains of power consumption are during Sensing, Communicating and data processing. Among these three domains, maximum energy consumption takes place during data communication. Energy consumption for processing data is very little compared to communicating data. So instead of transmitting raw data, sensor nodes carry out simple computations locally, then transmit partially processed required data. Hence, local data processing is very important for low power consumption in a WSN [76]. For many real time applications like monitoring battle field, controlling of environmental conditions, sensor nodes require fast processors for processing the detected signals. High speed processing and low area design are essential requirements for sensor nodes in an efficient WSN [77].

In reference [76], authors emphasized the necessity of local data processing at each sensor node. Data processing consumes much less energy compared to communication. So sensor nodes carry out data computation and transmit partially processed required data in place of entire raw data. A Munir et al. explain compromise between communication and data processing for many applications and permits transmission of event driven data to conserve energy [78]. So design of high speed low area processors, are essential for various applications in wireless sensor networks [79], [80].

Structure of biological neuron and its basic behaviour are explained in [81]. This behaviour is emulated in an artificial neuron in references

[82], [83]. Implementation of network model for neurons and synapses are demonstrated in these papers. In reference [84], complicated models of biological systems are accurately simulated. Neuron model VHDL library has been established which empowers a wide variety of complex neuron systems. Availability of standard library allows to implement complex neuron system on field programmable gate array (FPGA).

A conventional ALU is incapable of intelligently predicting outcomes based on previous inputs. Using artificial neural network (ANN), as basic building block, digital logic circuits are realized, and verified in [85]. Using ANN, a 5-bit ALU has been designed in this paper. Major disadvantages of designed ALU are slow and complex architecture. By using Vedic algorithm, computation speed of single neuron is increased in [86]. Using Vedic Mathematics, Anshika et al. implemented high performance neuronal logic gates in [87]. High speed neural network has wide range of applications like medical applications, image compression and many more.

2.4 Design of Power Amplifiers for Energy fficient Transceiver Blocks.

Due to plenty of sensor nodes installed in isolated area and long lifespan requirement, replacing battery is not an option. So, energy optimization in sensor network is more complicated as it involves reducing the energy utilization and increasing the lifespan of sensor network. In sensor nodes, power is consumed mainly in transceivers and in transceivers, the most significant power consumption is contributed by power amplifiers [88], [89]. In reference [90], N O Sokal has introduced

class−E amplifier with parallel capacitor which was a famous technological breakthrough obtaining ideal power efficiency value as 100%.

To achieve low power and long life time, circuit-level design procedures are focused in [91]-[93]. Importance of low power transceiver design is explained in [94]. This paper focuses on the design parameters which significantly influence energy consumption of transceiver unit. D G Rahn et al. have designed a transceiver for multiple input / multiple output wireless LAN applications in [95]. In RF transceivers, the major power consumption unit is power amplifier. Class AB operation is suitable for improved linearity and higher power added efficiency. Adaptive biasing schemes can be implemented for low power applications. Low power amplifier with adaptive biasing is designed in reference [96]. In reference [97], Daniela D Vento and Jan Rabaey designed a high resolution transceiver using class E power amplifier for smart and implantable microprobes that were capable of transmitting neural data to outside world through RFID.

High linearity, greater average output power, wider operating bandwidths and reduced energy consumption are the key design aspects for power amplifiers. In power amplifiers working in switch-mode configuration, the transistor operates in saturation, and either voltage or current, is switched on and off, depending on class of amplifier. A switch can be used in place of transistor. Only voltage is present across an open switch and current flows through the closed switch. So class E power amplifier has zero overlap of time between voltage and current. It gives 100% theoretical efficiency. Class-E power amplifier is a compromise between switched configuration and linear class AB configuration [98], [99]. M P Gopalrao et al. have done a comparative study of switch-mode

power amplifiers with different classes of operation and technologies for radio frequencies in [100]. Use of CMOS technology gives compactness and better results. Different techniques such as feedback, feed forward, and distortion to improve linearity of amplifier are discussed in [101]. Analysis of basic class E amplifier and design procedures are given in [102]-[106]. Reference [107] suggests improvements in design of basic class E power amplifier using self-biasing to improve efficiency. To minimise power loss and reduction in delay the active device is turned off by charging acceleration technique in reference [108].

To obtain higher output power and efficiency, mixed mode switching power amplifiers are discussed in reference [109]. The main mixed mode switching power amplifiers consist of class EF and class EM. Authors focused on the analytical study of duty ratio effects and nonlinearity effects of the gate to drain and drain to source parasitic capacitances on the performance of class EM power amplifiers. Authors also focused on the design procedures of class EM power amplifiers at any duty ratio. A single ended parallel circuit class E/F power amplifier is proposed by Chang Liu and Qian-Fu Cheng in [110]. Compared with other class E power amplifiers, proposed structure has same theoretical efficiency with improved performance in peak drain voltage, maximum operating frequency and power output capacity without much complexity in circuit. Reference [111] presents a two-stage class E linear power amplifier with greater power added efficiency.

2.5 Energy Harvesting Systems for Wireless Sensor Nodes.

Limited and irreplaceable battery energy is the most important constraint for wireless sensor nodes in sensor networks. Adapting more

advanced technologies, sensor nodes can be powered even without batteries by employing energy harvesting systems. The most suitable approach is to combine energy harvesting system with a compact energy storage device. In parallel with existing energy management approaches, which generally focused on power saving architecture and power saving network design at each communication layer, active research has also been taken place in the field of renewable energy harvesting techniques [112], [113]. Many research efforts are focused on energy harvesting from the renewable energy sources in order to design self-powered WSNs. Nowadays various harvesting techniques are available. Solar energy, wind energy, piezo electric energy are some of the ambient energy sources available for harvesting [114], [115]. Among these, currently most matured technology is based on solar cells and it gives high power density [116]-[119]. M Rahim et al. have carried out studies to extend life span of wireless sensor network by allowing a small percentage of network nodes to move in search of energy. These autonomously mobile nodes recharge and supply energy to immobile energy drained nodes [120].

Zheng et al. proposed a new piezo electric energy harvesting technology for WSN nodes in [121]. In order to achieve the impedance matching between energy supply system and vibration source, proposed circuit applies an optimum control voltage to piezo electric element and efficiency has been improved four times. In reference [122], energy is harvested from load power cables using a single split core toroidal coil current transformer (SCCT) to supply power to WSN node. Simultaneously, same SCCT estimates the main current in the power line. Thus, in this research work, a system which is capable of supplying power

to a WSN node and at the same time estimating current consumption has been discussed.

A solar harvester with self-powered WSN nodes with maximum power point tracking (MPPT) is proposed in [123]. Their design enhanced the efficiency of solar harvester working under varying light irradiance conditions. Instead of using microcontrollers and DSP processors for control action in MPPT algorithm, a comparator is used in the design. A high speed comparator is used in maximum light irradiance conditions and an ultra-low power comparator is suggested in poor light irradiance. The potential of solar cell to supply energy for one node is studied in detail in [124]. In this paper, characteristics of solar cell and design of control circuit to control the voltage for battery are described in detail. A detailed survey has been conducted on solar energy harvesting for WSN nodes by H Sharma et al. [125]. Authors conducted survey at four basic levels; solar energy harvesting level, sensing level, computation level and communication level. An in depth survey of solar cell efficiency, DC-DC converter, MPPT and energy prediction algorithms have been discussed. Design challenges and their practical solutions are explained in detail.

An efficient solar energy harvesting system has been proposed in [126] with pulse width modulation (PWM) and MPPT for WSN nodes. Modelling, simulation, optimization and hardware implementation are performed in this research work. PWM and MPPT control techniques for solar harvesting system have been analysed and compared. Efficiency of MPPT controlled systems were found to be better than PWM controlled systems. Design and development of efficient wind energy harvesting system is discussed in references [127]-[129]. An optimised wind energy harvesting system for WSN nodes using specially designed ultra-low power

management circuit is discussed in [130]. Instead of using conventional MPPT algorithm boost converter with MPPT techniques based on the impedance matching is implemented in this research paper. Another effective approach to harvest wind energy to keep self-powered low power WSN nodes running independently for years is proposed in [131]. This paper focuses on an optimized wind energy harvesting system with specially designed DC-DC Converter - aware Optimal Power Management (DCOPM) technique. Micro-scale wind energy harvesting system and power management units are discussed in detail in this paper.

2.6 The Thesis in Perspective: Motivation and Contributions.

In previous sections, we discussed different approaches to increase the life span of wireless sensor nodes. Few challenges are addressed in recent works. However, there are still many challenges unattended. A brief of issues to be addressed are given in succeeding paragraphs.

After conducting a detailed literature review, it is found that most of the research works have been directed towards software techniques for power savings in WSN applications. But very few efforts have been done for improving the hardware to reduce the power consumption. Many research works have focused on design of low power multiplier algorithms, but it is not explored for real time applications, using efficient adder circuits in order to achieve more power savings and speed.

Similarly, for application-oriented processors, not much has been explored in the design of ALU. Works have been concentrated in the modification of general transceiver architecture to save power. Adequate work has not been found in the design of power amplifiers for energy

efficient transceivers. Even though, lots of literature are available for solar energy harvesting, efficient energy harvesting technology for small systems have not been explored much.

Motivated by these observations we present in this thesis novel methods to reduce the energy consumption of sensor nodes and to increase the life time of sensor network. Our contributions are under:

(a) We have developed a high speed, low power Vedic multiplier for sensor nodes. To make multiplier suitable for all types of inputs, Urdhva Triyakbhyam Sutra is selected for multiplier architecture. Summation of partial products is done with high speed multiplexer based full adders. When compared with other conventional Vedic multipliers, proposed design gives much less delay and area utilisation.

The proposed design of Urdhva Vedic multiplier is coded in Verilog HDL and functionally verified through simulation using Modelsim SE 6.4. First a basic 2x2 Urdhva Vedic multiplier is designed, using half adders. This basic 2x2 multiplier is further used to implement 4x4 bits to 16x16 bits multipliers and are then simulated. The performance of proposed design is also compared with conventional Urdhva Multiplier.

(b) An energy efficient ALU using Vedic multipliers has been designed for energy efficient sensor nodes. A conventional ALU is incapable of intelligently predicting outcomes based on previous inputs. Its neural counterpart, on the other hand, aims at improving its prediction capabilities by employing an activation function and making it an intelligent ALU. But ALU designed with neurons suffers from bulky and slow architecture. This can be solved by implementing the Vedic logic in all arithmetic and logical operations performed. The Vedic logic helps in

performing faster calculations by utilizing simple techniques to solve complex problems. This provides a faster and a smarter ALU design. This work is intended for laying a foundation for the intelligent sensor nodes by implementing Vedic logic on neural platforms.

Proposed design of ALU has been coded in Active HDL and verified through simulation using ModelSim SE 6.4. The Active HDL codes of the ALU were synthesized using Xilinx ISE 14.7.

(c) Improved power amplifier configurations for making energy efficient transceiver blocks of sensor nodes have designed in this thesis work. The efficiency and bandwidth are the most important characteristics of power amplifier in sensor nodes. Low power sensor nodes must communicate with their neighbours at hundreds of kilobytes per second and have to operate at higher volumetric densities especially in wireless visual sensor networks and wireless multimedia sensor networks [132]-[135]. High data rate requires wider band width. But wider bandwidth limits the sensitivity and range. Requirement of wider bandwidth and higher efficiency without reducing sensitivity demands new design strategies.

Power amplifier with low power supply gives more reliable operation. But overall gain and efficiency are decreased due to reduced power supply. In class E power amplifiers, these combinations do not exist. So our study focuses on modifications for basic class E amplifier to achieve improved band width and efficiency at lower power supply.

Two different configurations using basic class E amplifier are proposed in this work. The first configuration is class E amplifier with double cascoding and second design is class E amplifier designed using common drain followed by common source (CDCS) cascading.

The transceivers should operate at high data rate for better efficiency which allows many nodes to share same channel through time division multiplexing. Thus, wider band width is another important requirement for power amplifiers used in sensor transceivers. In order to achieve wider band width, cascade of common drain followed by common source in class E configuration has been designed.

Power amplifier can be designed at smaller supply voltage for enhanced reliability. For more reliable operation with higher efficiency, class E in double cascoded has been implemented.

(d) We have designed an efficient and compact energy harvesting system to increase life of wireless sensor nodes. Using more advanced technologies, sensor nodes can be powered even without batteries by employing energy harvesting systems. The most suitable approach is to combine energy harvesting system with a compact energy storage device. More research efforts are focused on energy harvesting from the renewable energy sources to design self-powered WSNs.

Nowadays various harvesting techniques are available. Solar energy, wind energy, piezo electric energy are some of the available ambient energy sources. Among these, currently most matured technology is based on solar cells and it gives high power density. Requirement of small sized sensor nodes demands small solar panels in the harvesting system which leads to design a compact and simple solar energy harvesting system (SEH) for sensor nodes. We have designed a solar harvester for WSN nodes with compact models of solar panel and harvesting circuits. This design performed stable with high reliability and efficiency and without much

power loss. In order to achieve long lasting power for the system, proposed design focused energy saving principles by using low power consumption devices in each module.

CHAPTER 3

HIGH SPEED LOW POWER VEDIC MULTIPLIERS FOR WIRELESS SENSOR NODES

3.1 Introduction

In real time applications like measuring various environmental conditions, fast response of the processor is required to process the measured signals. In arithmetic operations, multiplication is a fundamental function. Operations based on multiplication are frequently used in critical applications of digital signal processing (DSP) like convolution, Fast Fourier Transform (FFT), filtering etc. These are also used in arithmetic functions like inner products, MAC (multiply and accumulate) units etc. Multiplier is an important unit in digital image processing systems. Multipliers are used not only in ALU but also in other components of processor implementations, like various data path units.

Currently, with large number of applications in consumer and industrial sectors, internet of things (IOT) is a widely accepted reality. For IOT to continue growing, many intelligent devices and WSN are required

[136] – [139]. Hence, in order to develop efficient and reliable sensor networks for real time and IOT applications, high speed processing is essential, to process acquired signals. So demand for low power consuming multiplier circuit with high speed for small sensor nodes has been continuously increasing.

3.2 State of the Art

Recently, many efforts have been directed towards increasing the speed of multiplier with reduction in power consumption. As the efficiency of basic building block determines the performance of the system, multiplier plays an essential role in the performance of wireless sensor nodes. As the demand for high performance multipliers is highly increasing, many research efforts have been focusing on multiplication algorithms and various types of adders.

Generally, multipliers with different algorithm require large area, more power consumption and long latency. Multiplier architecture based on Vedic mathematics achieve high speed, low area and low power consumption.

Using Vedic mathematics, complex calculations can be executed with simpler steps. Due to this, recent research has focused on implementation of Vedic multiplier. Vedic algorithms for multiplication are used with different approaches as existing multiplier architectures have their own limitations.

G Ganesh Kumar et al. [54] proposed the design of high-speed Vedic multiplier and established the efficiency of Urdhva Triyakbhyam Sutra in Vedic mathematics for multiplication and explained the difference from the

conventional method of multiplication. Vedic multiplier can be efficiently used for parallel generation of partial products and for eliminating steps for multiplication with zeroes. Proposed design used Karatsuba algorithm for higher bit levels. 32*32 bit multiplier using Urdhva Triyakbhyam Sutra and its FPGA has been implemented using Verilog HDL coding and Xilinx synthesis tool on Spartan 3E kit. They have implemented proposed multiplier and conventional multiplier with shift and add techniques for 4,8,16 and 32 bits. It is observed that Vedic architecture provides least delay.

C Sheshavali et al. [50] has designed a Vedic multiplier based on ROM approach on a cyclone IIIFPGA. Their proposed multiplier is compared with Array multiplier and conventional Urdhva multiplier for 8bit and 16 bit input data. Proposed 16*16 bit multiplier is 150% faster and consumes 42% area.

Harish Kumar [47] presented different architectures for multipliers. He focused generally on array multiplier and Vedic multipliers based on Urdhva Triyakbhyam Sutra and Nikhilam Sutra. To find out best architecture for multiplication, comparison of these architectures is carried out for 8, 16, 32 bits inputs, in terms of power and delay. The designs are done in Verilog and simulated using Xilinx10.1 ISE. From the results of power, delay and memory he proved that multiplier architecture using Urdhva Triyakbhyam Sutra gives best results compared with Array and Nikhilam architecture.

Poornima M et al. [55] have carried out an in depth study of Vedic mathematics and Urdhva Triyakbhyam Sutra for multiplication. Their paper presents study on 8*8 Vedic multiplier architecture using Urdhva

Triyakbhyam Sutra. Authors concluded that proposed Vedic multiplier is faster than Array Booth multipliers.

Surbhi Bhardwaj et al. [19] presents a Vedic multiplier using Urdhva Triyakbhyam Sutra. Authors have synthesized their proposed design in 4*4, 8*8 and 16*16 using Xilinx ISE tool and speed is compared with existing multiplier architectures. Comparison results show that proposed architecture has achieved more speed.

S R Panigrahi et al. [42] also developed a Vedic multiplier using Urdhva Triyakbhyam Sutra. Their proposed architecture is designed using VHDL and simulated using Xilinx ISE. The results has shown that their design required lesser amount of hardware with reduced delay. Their proposed design is, thus, suitable for many real time signal and image processing applications.

Ramachandran S et al. [49] focused on Vedic multiplier algorithms based on Urdhva Triyakbhyam Sutra and Nikhilam Sutra. Authors have designed 8x8 bits, 16x16 bits, 32x32 bits and 64x64 bits Urdhva and Nikhilam multipliers on Xilinx ISE 11 and concluded that Urdhva multipliers work faster and better for smaller inputs; and multipliers based on Nikhilam Sutra are suitable for larger inputs. So authors designed an integrated Vedic multiplier architecture that can select better multiplier Sutra on the basis of incoming inputs. In their model, for larger inputs, ie upto 20% from the nearest base, Nikhilam multiplier has been selected; otherwise Urdhva multiplier has been selected.

M Uma Maheswara Sainath et al. [56] developed a Vedic multiplier using Urdhva Triyakbhyam Sutra. But a high speed approach using 4 : 2 compressor for addition has been included in their architecture. On the

basis of comparing speed and area occupied with existing multiplier architectures, authors concluded that Vedic multiplier based on compressor is more efficient.

Premananda B S et al. [39] designed an eight bit Vedic multiplier with the help of Urdhva Triyakbhyam Sutra. Addition of partial products in Vedic multiplier has been implemented employing carry skip technique. Simulation of architecture is carried out using Xilinx and results have shown 13.65% increase in the speed of their proposed design compared with conventional multipliers.

From the literature, we can conclude that multiplier architecture using Vedic mathematics found to be a better option compared with other conventional multipliers. Among 16 Sutras of Vedic mathematics, Urdhva Triyakbhyam Sutra and Nikhilam Sutra are for multiplication. Among these two, Nikilam Sutra is suitable only for larger inputs. Hence, Urdhva Triyakbhyam Sutra is suitable for all other types of data. Further speed of multiplier speed is limited by speed of adders used for partial product addition. So the performance of Vedic multiplier can be improved if we select proper adder circuit in the multiplier architecture.

3.3 Problem Formulation

The main aim of the present work is to design a high speed low power Vedic multiplier. The proposed design integrates high speed multiplication features of Urdhva Triyakbhyam Sutra and MUX based adders for minimizing delay and power dissipation. Urdhva Triyakbhyam Sutra is used for generating partial products and MUX based adders for adding partial products.

3.4 Methodology

The research objective is to design high speed, low power Vedic multiplier. In order to make multiplier suitable for all types of inputs, Urdhva Sutra is selected for multiplier architecture. To enhance the speed of multiplier operation, instead of traditional adders, full adder with MUX is used. The proposed architecture reduces the propagation delay significantly. The proposed design integrates the high speed multiplication features of Urdhva Triyakbhyam Sutra and MUX based adders for minimizing delay. Urdhva Triyakbhyam Sutra is used for generating partial products and MUX based adders for adding partial products.

The proposed design of Urdhva Vedic multiplier is coded in Verilog HDL and is functionally verified through simulation using ModelSim SE 6.4. First a basic 2x2 Urdhva Vedic multiplier is designed, using half adders. This basic 2x2 multiplier is further used to implement 4x4 bits to 16x16 bits multipliers and are then simulated. The performance of proposed design is also compared with conventional Urdhva multiplier.

3.4.1 Vedic mathematics

Vedic mathematics is an ancient system of mathematics existed in India. In this eminent approach, methods of basic arithmetic are simple, powerful and logical. Another advantage is its regularity. Because of these advantages, Vedic mathematics has become an important topic for research. The techniques in Vedic mathematics are mainly based on sixteen Sutras. Among sixteen Sutras, Urdhva Triyakbhyam and Nikhilam are used for multiplication [46]. Vedic multipliers have proved to be more efficient when compared to conventional ones. Urdhva Triyakbhyam Sutra

architecture is more efficient compared to Nikhilam Sutra [47]. It is well known from literature [49] that Nikhilam Sutra based multipliers are expected to work better for larger inputs, that is, inputs near to base (20% from the nearest base).

Regularity and simplicity of Vedic mathematics leads to easy implementation in FPGA [50]. Another advantage of this approach is that all partial products required for multiplication are calculated much before actual multiplication begins. Based on the Vedic mathematics algorithm, these partial products are added to obtain final product which leads to a very high speed approach [56]. In addition, high speed multiplier designs based on Vedic mathematics consume low power too [54]. Therefore, in this research, a high speed multiplier using Vedic mathematics has been designed. The speed of multiplier is determined by the speed of adders used for partial product addition. Hence, in this part, we use multiplexer based full adders to increase the speed of multiplier.

3.4.1.1 Urdhva Triyakbhyam Sutra.

'Urdhva' literally conveys "vertical and cross-wise" and suggests that vertical and crosswise multiplication is done for obtaining the partial products and their concurrent addition. Because of the parallel processes of partial product calculation and their addition, Vedic multiplier does not depend on clock frequency. Implementation of a 2x2 Urdhva multiplier is shown in Figure 3.1 and Figure 3.2. Vedic multiplier architecture can be easily extended to higher inputs due to its regular structure. Figure 3.3 shows generation of partial products using "vertical and crosswise" logic for a 4x4 multiplier. Parallel addition of these partial products is done along with their generation [47]. Implementation of 4x4 Vedic multiplier

is shown in Figure 3.4 [136]. The 4x4 multiplier can also be constructed using four, 2x2 multiplier blocks which is shown in Figure 3.5 [47].

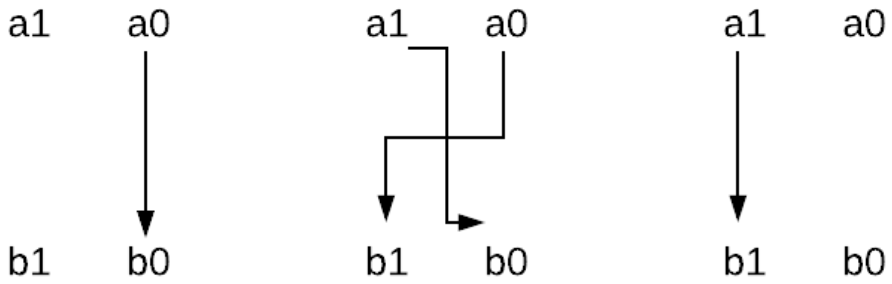


Figure 3.1. Urdhva multiplication method for 2 bit binary numbers [47]

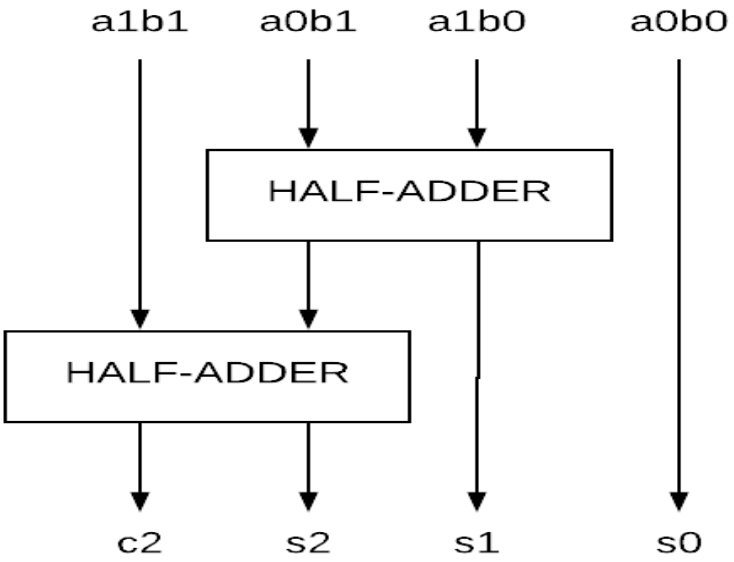


Figure 3.2. Block diagram of 2x2 bit Urdhva multiplier [47]

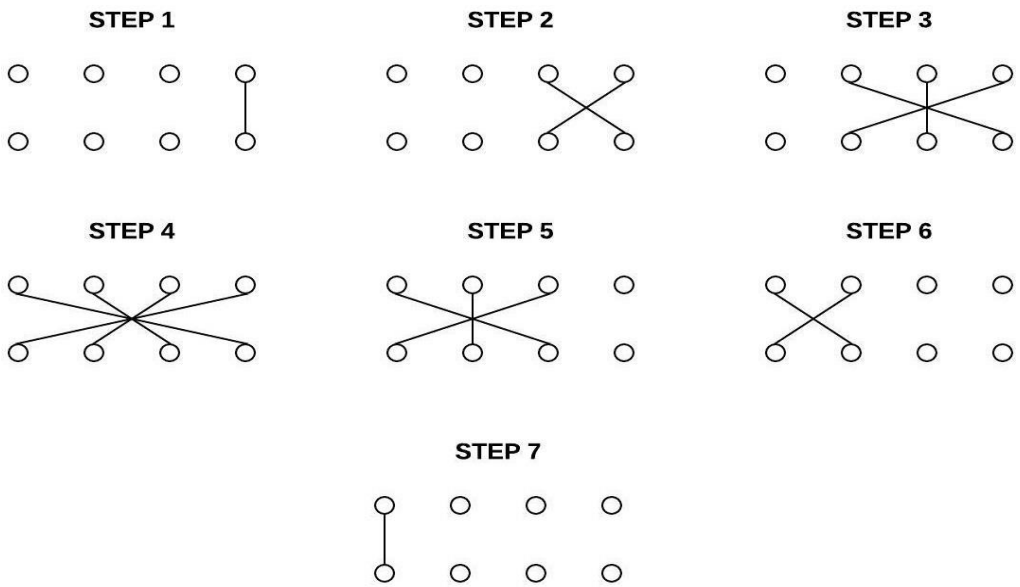


Figure 3.3. Line diagram for 4 bit Urdhva multiplication [49]

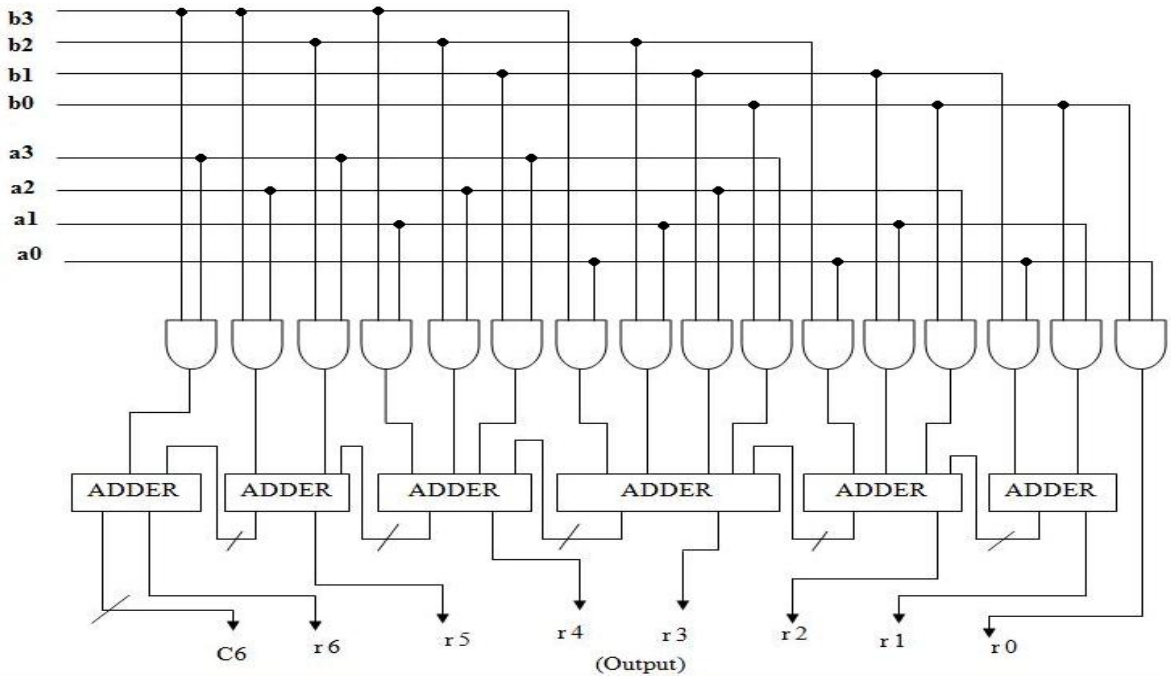


Figure 3.4. Hardware architecture for 4-bit Urdhva multiplier [140].

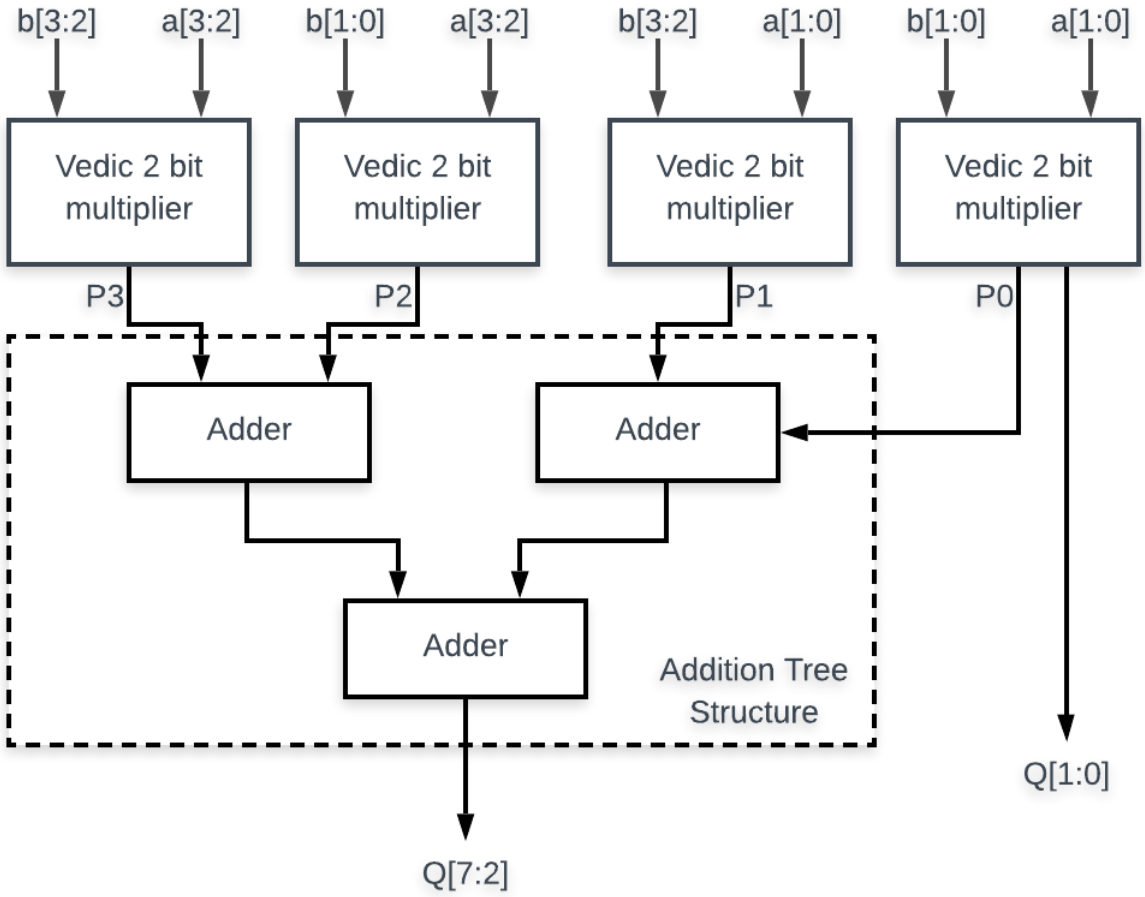


Figure 3.5 Block diagram for 4x4 Vedic multiplier using 2x2 multipliers [47].

3.4.2 Multiplexer Based Adders

Adders become a critical hardware unit for efficient implementation of multiplier unit. Reducing the delay of full adder ultimately increases the speed of multiplier. From the literature [22], [44] and [63], it is observed that full adder with multiplexer and XOR gate gives best performance, especially in terms of delay and power dissipation. It consists of two XOR gates and one 2x1 MUX as shown in Figure 3.6.

Instead of using simulation tools, we can calculate delay mathematically using logical effort method. It gives a simple method to select best logical construct (topology) [22]. Equation (3.1) gives delay (d)

for a single stage network in terms of logical effort (g), electrical effort (h) parasitic delay (p).

$$d = g*h + p; \qquad (3.1)$$

where ‘g’ represents logic gate’s ability to produce output current (compared to inverter, how much worse it is in producing output current), ‘h’ gives ratio of output capacitance to input capacitance and ‘p’ gives delay of gate due to internal capacitance. As ascertained from the Table 3.1, the logical effort of 2X1 multiplexer is constant for any number of inputs, where ‘n’ represents number of inputs. But the logical effort for XOR, NOR and NAND gate is higher, which were the components of conventional full adder circuits. Therefore, the above full adder circuit gives minimum delay compared to other full adder circuits.

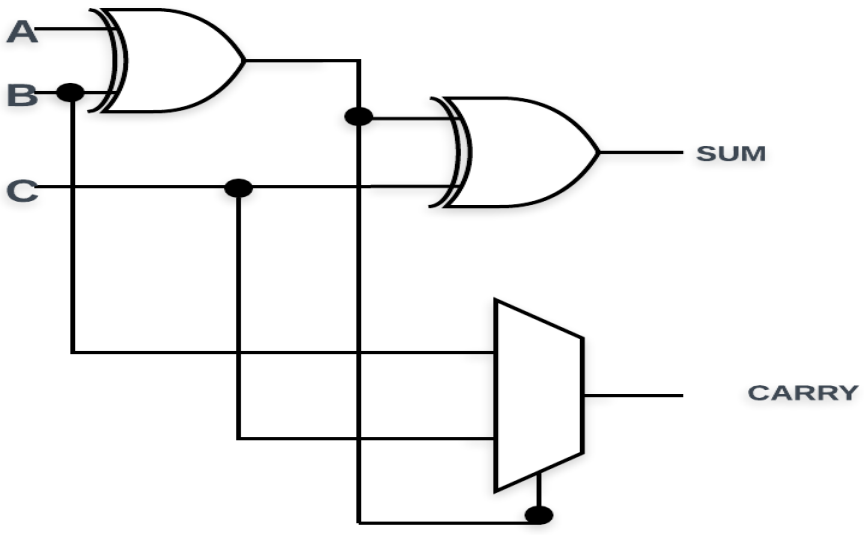


Figure 3.6 Full adder with XOR gates and MUX [22].

Table 3.1.

Logical Effort for Different Inputs of CMOS Gates

Gate Type	Number of Inputs (n)					
	1	2	3	4	5	6
Inverter	1					
NAND		4/3	5/3	6/3	7/3	(n+2)/3
NOR		5/3	7/3	9/3	11/3	(2n+1)/3
XOR(parity)		4	12	32		
Multiplexer		2	2	2	2	2

3.5 Simulation Results.

The proposed design of Urdhva Vedic multiplier is coded in Verilog HDL and is functionally verified through simulation using ModelSim SE 6.4. First, a basic 2x2 Urdhva Vedic multiplier is designed, using half adders. This basic 2x2 multiplier is further used to implement 4x4 bits to 16x16 bits multipliers and are then simulated. To establish superiority of the proposed design, the existing Urdhva multiplier circuits [19] & [47] are also simulated for same simulation settings. The performance of proposed design is also compared with conventional multiplier.

3.5.1 Simulation of proposed 8-bit Urdhva multiplier.

Considering ‘a’ and ‘b’ the binary inputs and ‘c’ as their product the proposed multiplier operation is functionally verified with different sets of

inputs. A typical simulation result for a = 00000110 and b = 00001010 is shown in Figure 3.7 and their product c = 0000000000111100**.**

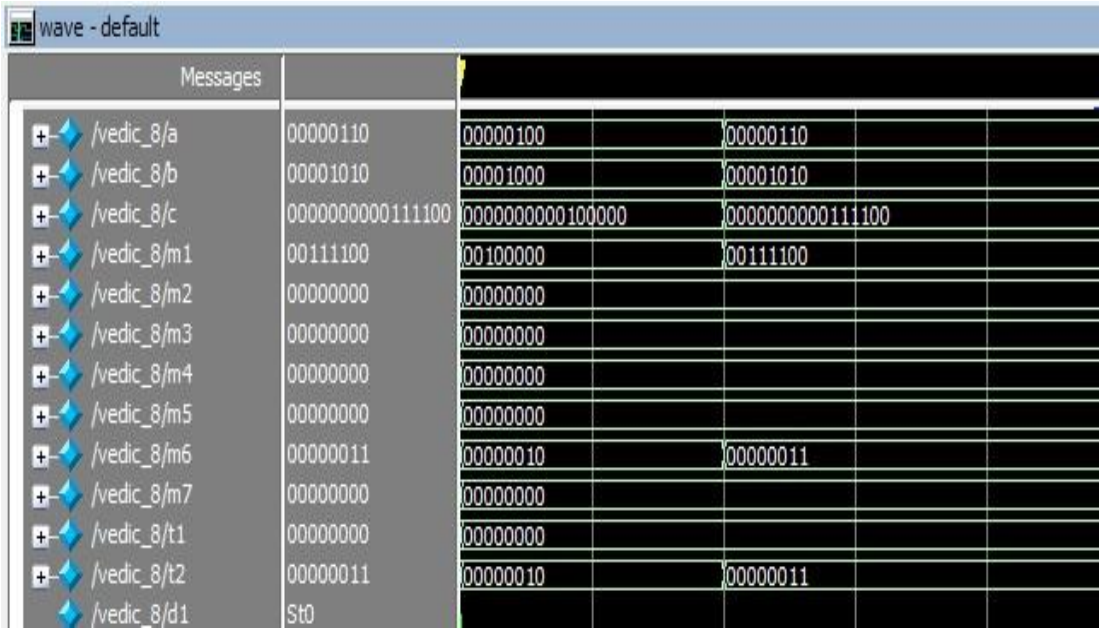


Figure 3.7. Simulation result of proposed 8-bit Urdhva multiplier

3.5.2 Simulation of 8-bit conventional Urdhva multiplier

The simulation result of 8-bit Urdhva multiplier for same set of inputs as used in Figure 3.7, is shown in Figure 3.8.

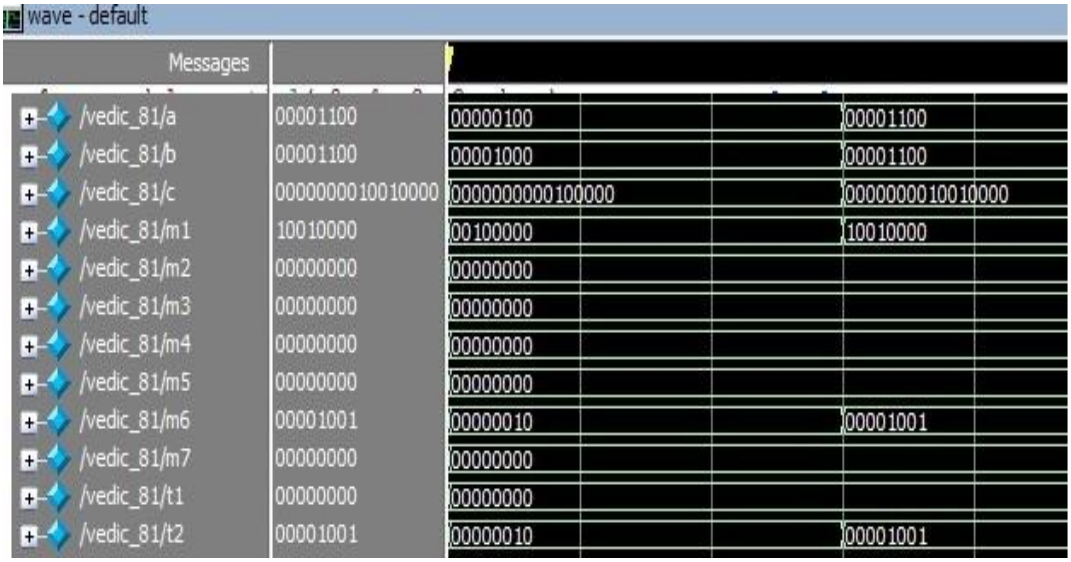


Figure 3.8. Simulation esult of conventional 8-bit Urdhva multiplier

3.5.3 Simulation of 16-bit multipliers:

16-bit multipliers are also designed in the same way as 8x8 multipliers were designed using 4x4. Simulation result of 16x16 proposed multiplier is shown in Figure 3.9 whereas that of conventional multiplier is shown in Figure 3.10. In each case 'a' and 'b' are the inputs and 'c' is their product. Result is verified using different set of inputs.

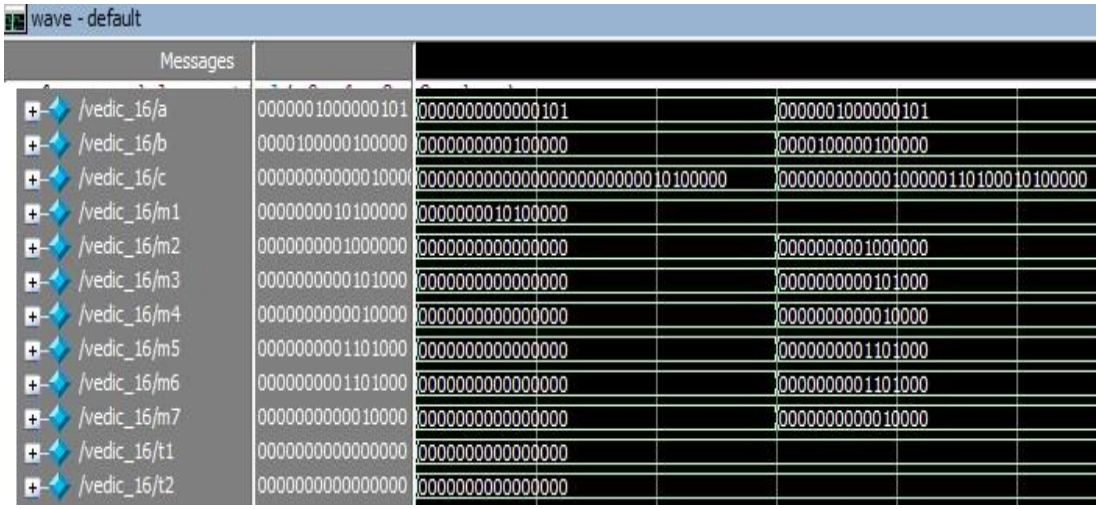


Figure 3.9. Simulation result of proposed 16-bit Urdhva multiplier.

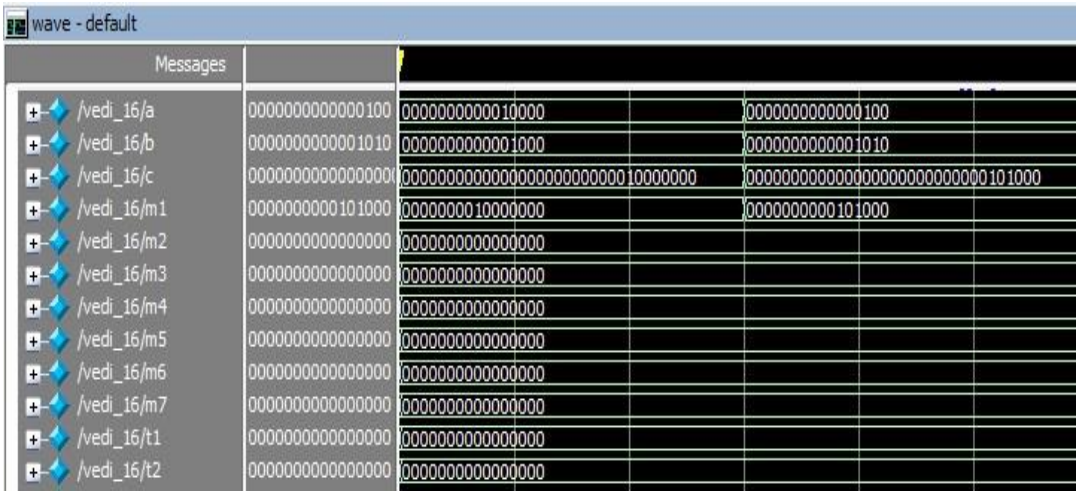
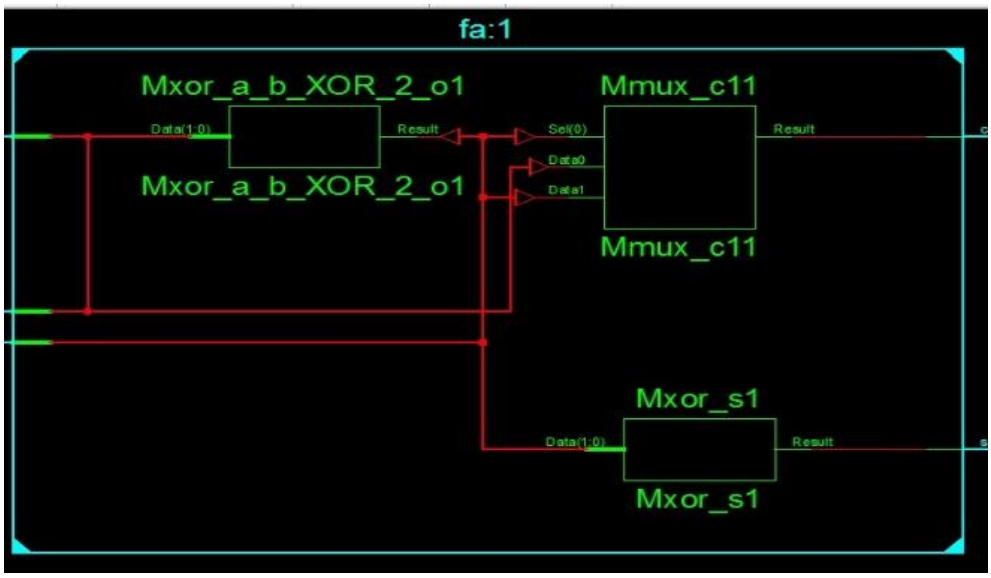


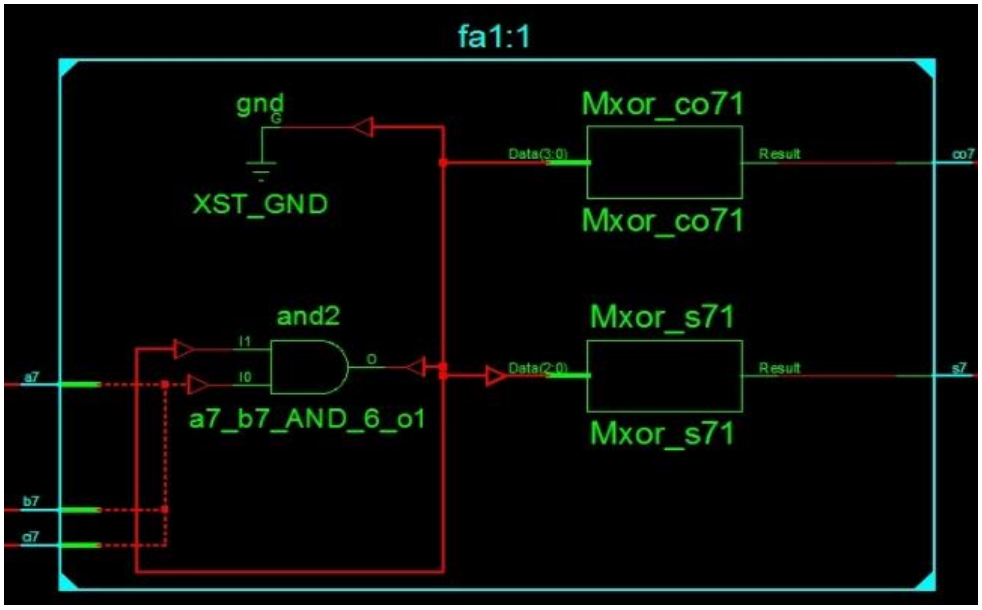
Figure 3.10. Simulation result of 16-bit conventional Urdhva multiplier

3.5.4 Synthesis

The Verilog codes of the multipliers were synthesized on Xilinx ISE 14.7 and the synthesis report was generated for Virtex-6 family of FPGA. RTL schematics for both the 16-bit multipliers were generated.



(a)



(b)

Figure 3.11. RTL view of full adder of (a) Proposed (b) Conventional Urdhva multipliers.

3.5.5 Results

The zoomed RTL view the adder circuits of the proposed and conventional 16-bit Urdhva multipliers are depicted in Figure 3.11 (a) and (b) respectively. The proposed design differs with conventional Urdhva multiplier in the adder circuit; therefore, zoomed RTL view of both the full adders only are depicted.

From the RTL views of both full adders, in the conventional full adder carry is generated using XOR and AND circuits whereas only MUX is used to generate carry in the second case. Our research work focused mainly on the parameters of delay and area. Main parameters focused in our work are delay and area. Implementation results of 4-bit, 8-bit and 16-bit conventional and proposed multipliers are shown in Table 3.2 to 3.4. Table 3.5 shows delay of proposed and conventional multipliers for 4-bit, 8-bit and 16-bit inputs. Table 3.6 shows that proposed multipliers have reduced delay and number of slice LUTs (hardware resources) compared to conventional multipliers. Delay and number of slice LUTs of various Urdhva multipliers in references are shown in Table 3.7 and Table 3.8. Results from these tables report that proposed multipliers performed better. Performance analysis of both multipliers are compared in Table 3.9. From the table it is observed that delay obtained for Urdhva multiplier with MUX based adder is much less than the delay obtained for conventional multipliers. Also, from the results of synthesis, it can be ascertained that the new model occupies much less area on chip (reduced no. of slices) which is an added advantage. Table 3.9 shows the values of quantitative improvement in performance characteristics.

Table 3.2.

Synthesis result of logic utilisation for 4-bit multipliers

No of slice LUTs	Conventional Multiplier	Proposed multiplier
Used	22	19
Available	46560	46560
Utilisation	0.047%	0.040%

Table 3.3.

Synthesis result of logic utilisation for 8-bit multipliers

No of slice LUTs	Conventional Multiplier	Proposed multiplier
Used	133	107
Available	46560	46560
Utilisation	0.285%	0.229%

Table 3.4.

Synthesis result of logic utilisation for 16-bit multipliers

No of slice LUTs	Conventional Multiplier	Proposed multiplier
Used	742	594
Available	46560	46560
Utilisation	1.59%	1.27%

Table 3.5.

Synthesis results on delay

Multipliers	Delay	
	Conventional Multiplier	Proposed Multiplier
4-bit	4.714ns	3.254ns
8-bit	12.588ns	9.130ns
16-bit	20.338ns	16.994ns

Table 3.6

Summary of Synthesis Results

Multipliers	Delay (in ns)		No. of *slice LUTs*	
	Conventional	Proposed	Conventional	Proposed
4-bit Urdhva	4.714	3.254	22 out of 46560	19 out of 46560
8-bit Urdhva	12.588	9.130	133 out of 46560	107 out of 46560
16-bit Urdhva	20.338	16.994	742 out of 46560	594 out of 46560

Table 3.7

Delay comparisons reported by previous approaches

Type of multiplier	Delay		
	4-bit	8-bit	16-bit
Urdhva multiplier proposed in [19]	11.695nS	18.532nS	30.659nS
Urdhva multiplier using carry skip adder proposed in [39]	NR	15.050nS	NR
Urdhva multiplier proposed in [42]	5.759nS	NR	NR
Urdhva multiplier proposed in [47]	NR	23.079nS	41.350nS
Urdhva multiplier proposed in [49]	NR	13.455nS	25.083nS
Urdhva multiplier based on ROM approch proposed in [50]	NR	NR	23.87nS
Urdhva multiplier with Karatsuba algorithm optimized in [54]	NR	15.418nS	22.604nS

NR = Not reported

Table 3.8

Area comparisons reported by previous approaches

Type of multiplier	4-bit	8-bit	16-bit
Urdhva multiplier proposed in [19]	29	149	661
Urdhva multiplier proposed in [42]	42	NR	NR

NR = Not reported

Table 3.9.

Performance Analysis

Multipliers	Percentage improvement in speed	Percentage improvement in area
4-bit	30.97%	13.6%
8-bit	27.47%	19%
16-bit	16.44%	20%

3.6 Conclusion

Contribution from this research is designing a high speed low power Vedic multiplier based on Urdhva Triyakbhyam Sutra. A combination of Vedic mathematics and MUX based adder circuit has been employed in this work. Summation of partial products has been implemented with high

speed MUX based full adders. Compared with other conventional Vedic multipliers, proposed design has achieved much lesser delay and LUT count - which is an indicator of area and power dissipation. Comparative results show that proposed multipliers have 30.97%, 27.47% and 16.44% less delay for 4bit, 8bit and 16bit multipliers respectively. Comparative results further show that utilisation of number of slice LUTS has reduced, i.e., 13.6%, 19% and 20% less number of slice LUTs for 4bit, 8 bit and 16 bit multipliers respectively. Proposed multiplier can be used to design MAC units [141], [142] and ALUs [143], [144]. Our proposed design provides method for hierarchical multiplier design. For inputs of large number of bits, design complexity has been reduced and modularity has been enhanced.

CHAPTER 4

ENERGY EFFICIENT ALU USING VEDIC NEURONS

4.1 Introduction

Achieving low power consumption is a major challenge in designing any wireless sensor node. In WSN, primary functions of sensor nodes are to detect events, process and transmit data. Therefore, major domains of power consumption are during sensing, communicating and data processing. Among these three domains, maximum energy consumption takes place in data communication. Energy consumption for processing data is very little compared to communicating data. So instead of transmitting raw data, sensor nodes perform simple computations locally, then transmit partially processed data. Hence, processing data locally at each node in a sensor network, is important for minimizing power consumption [30]. For many real time applications like monitoring battle field, controlling of environmental conditions, sensor nodes require fast processors for processing the detected signals. High speed processing and low area design are essential requirements for sensor nodes in an efficient WSN. Necessity of prediction based monitoring to increase efficiency and hence life time is explained in [145]. Presently, WSN system uses prediction based monitoring in large number of applications like environmental data prediction, moving object tracking system, etc. [146]-[149]. In many applications, sensor networks are required to adapt to the

changing environment, demonstrating intelligent behaviour. Internet of Things (IOT), Under Water Sensor Network (UWSN), and Mobile Wireless Sensor Network (MWSN) are some of such emerging areas. So computational intelligence capability is required for a sensor node to adapt its operations according to unpredicted changing environment [150]-[154].

4.2 State of the Art

I F Akyildiz et al. [30] have explored on the main factors effecting the design of sensor networks. Authors have conducted an in-depth review on the communication architecture for sensor networks. A detailed survey has also been conducted on the algorithms and protocols developed for each layer. In this paper, authors have also presented examples of important sensor network applications. According to their research, as most of the sensor nodes are closely deployed, multi hop communication consumes less power compared to traditional single hop communication. The important functions of a sensor node in sensor network include detecting events, processing data and transmitting data. So total power consumption in a sensor node can be mainly divided into three areas, viz., sensing, communicating and data processing. Among these three functions, maximum power is consumed in communicating data. Communication includes data transmission and data reception. Energy consumed in data communication is much more compared to energy consumed in data processing. So, an important factor to minimize overall power consumption is local data processing.

C Buratti et al. [76] have emphasized importance of signal/ data processing to achieve low device complexity with low energy consumption. In this research paper, authors have presented a case study

on environmental monitoring. This survey paper mainly focused on IEEE 802.15.4 standard that is widely used in various applications of sensor networks. Technical characteristics related to physical and MAC layers and higher layers are presented in this paper. Their work gives outline of WSN technologies, their application and standards, features and issues in WSN design and their evolution.

A Munir et al. [78] proposed a design for heterogeneous hierarchicalmulti-core embedded wireless sensor networks (MCEWSNs) and architecture for nodes used in MCEWSNs. Intensive computational tasks such as encryption, information fusion, etc. will benefit from the enhanced computational power of multi core embedded sensor nodes. Currently MCEWSNs have wide range of applications like wireless multimedia sensor networks and wireless video sensor networks, fault tolerant sensor networks, space shuttle sensor network, aerial terrestrial hybrid sensor networks, satellite based wireless sensor networks etc. In this paper, authors have investigated performance of two multicore architectures symmetric multiprocessors (SMPs) and tiled many core architecture (TMAs). From the recorded result, we can conclude that TMAs provide better performance as compared to SMPs.

S Pragati et al. [155] have designed an ALU unit with the help of FPGA processor for WSN nodes. Their simulation results are compared with MSP 430, which is commonly used in WSN nodes. Proposed model consumes less power, less area and has increased computational speed. M Sarath et al. [156] also designed an energy efficient ALU using clock gating for sensor node. Authors focused on reducing dynamic power consumption using clock gating method. Clock gating scheme is applied to 16-bit ALU with block enabled clock gating and functional unit enabled

clock gating. Verilog HDL is used to design 16bit ALU and simulations are performed using Xilinx Vivado simulator. Reduction in power consumption is achieved in both technologies, especially at high frequencies. Functional unit enabled clock gating technique has achieved significant power reduction compared to block enabled clock gating. In this method for frequencies 100-200MHz, power reduction varies from 50% to 60% and for 500MHz to 1 GHz power reduction is from 75% to 80%.

S Goel et al. [75] have proposed prediction-based monitoring for sensor networks in an energy efficient way. Using block matching algorithm authors have designed prediction models. Proposed algorithm has been implemented in test bed of Rene Motes. Experimental results have shown that the proposed model helped in decreasing the number of transmissions from sensors and thereby decreasing the power consumed by more than five times.

F Xia et al. [147] have introduced a prediction-based data transmission approach for wireless body sensors. Since body sensors are implanted into human body, they were designed light-weight and small in size. Another critical design issue is their energy conservation. Authors have a generic prediction algorithm for predicting data sampled by wireless body sensors. Their approach combines a dual prediction frame work and proportional integral derivative technique, which leads an effective approach to energy efficient data transmission.

Recently researchers have focused on introducing computational intelligence into WSNs in order to become adaptive to unpredictable changes and to exhibit intelligent behavior. Intelligent optimization of

WSN through bio-inspired computing has been implemented in reference [151] and [152]. An adaptive architecture based on natural algorithm for under water WSNs has been introduced by S A Sofi et al. [153]. In UWSNs signal attenuation under water is more compared to traditional WSNs. There are chances of frequent changes in the position and location of nodes due to water current and other factors. So adaptive and energy efficient routing is required for UWSNs. Based on natural algorithm, an adaptive architecture is implemented to keep the nodes connected. They employed an advanced node as a dedicated cluster head to overcome the additional power requirement due to signal attenuation. G Serpen et al. [157] focused on using artificial neural network for developing adaptation capability and introducing intelligence into wireless sensor nodes which resulted in improved functionality, utility and survival.

From the literature, it can be concluded that for reducing energy consumption and for increasing battery life of sensor, local data processing is required, before transmitting collected data. Employment of artificial neural network will help sensor nodes to transmit prediction based processed data, to adapt to the changing environment and thus exhibiting intelligent behavior. R Raeisi et al. [85] implemented digital logic circuits using artificial neural network (ANN). The most important characteristics of ANN is that it can be used in applications where input and output relation is unknown. Authors have explored the advantages of ANN and designed digital gates and logical circuits in hierarchical method. 1 bit and 5-bit ALUs have been designed and verified using Easy NN-plus tool. But major disadvantage of this design is its complex and slow architecture.

S Yamuna et al. have implemented Vedic neuron in reference [86]. Neural network computations are performed using Vedic multiplier instead

of conventional multiplier. Authors explored the possibility of increasing the computation speed of single neuron. Single neuron is implemented using conventional multiplier and Vedic multiplier in VHDL and synthesis has been done in Xilinx ISE using model Sim. Comparative results have shown that the delay of Vedic neuron has been less compared to the use of conventional neuron. Hence, Vedic neuron can be effectively used in the design of ALU using ANN.

4.3 Problem Formulation

A conventional ALU is incapable of intelligently predicting outcomes based on previous inputs. Its neural counterpart, on the other hand, aims at improving its prediction capabilities by employing an activation function and making it an intelligent ALU. But ALU designed with neurons suffers from bulky and slow architecture. This can be solved by implementing the Vedic logic in all arithmetic and logical operations performed. The Vedic logic helps in performing faster calculations by utilizing simple techniques to solve complex problems. This provides a faster and a smarter ALU design. This work is intended for laying a foundation for the intelligent sensor nodes by implementing Vedic logic on neural platforms.

4.4 Methodology

The objective is to implement high speed ALU using Vedic neurons realizing faster computational speed and lower area than that achieved with current standards. In the first stage, we have implemented 8 bit Vedic multiplier using Urdhva Triyakbhyam sutra, which is explained in chapter

three of this thesis. In next stage, all multipliers in the neuron structure are replaced with this designed Vedic multipliers and thus Vedic neuron has been designed. Using this Vedic neuron, all arithmetic and logical functions have been implemented in the third stage. In the final stage, proposed ALU has been implemented using above arithmetic and logical functions.

4.4.1 Artificial Neural Networks (ANN)

Research on ANN has been inspired from the complex structure of human brain. Using neurons, human brain can compute much faster than equivalent digital hardware circuit. The computation can be viewed as a system in which, external stimulus sends input to receptors. The function of receptors is to transform the received stimulus from outside into electrical impulses. These electrical impulses carry information to the neural net. According to received electrical impulses, the neural net sends information to effectors. These effectors issue an excellent response to stimulus as shown in figure 4.1. The brain is composed of an integral constituent known as neuron. By training these neurons, brain is skilled to differentiate contrasting patterns and gives appropriate output. Behaviour of a brain can be emulated with the concept of ANN.

ANN is a parallel distributed unit, consisting of many highly inter linked processing elements, known as artificial neurons. These processing elements store experiential knowledge and make it available for further use. Analogous to human brain, ANN also acquires knowledge through learning process from environment. The learned knowledge is stored in interneuron connection strengths as synaptic weights.

An ANN is a collection of interconnected nodes known as artificial neurons. Artificial neuron is a simplified model of biological neuron in a human brain. The connections between artificial neurons transmit signals from one neuron to another inter connected neuron. Received signals are processed by artificial neuron and it, in turn, signals other inter connected neurons.

In ANN implementation, the signal at the connection between neurons is always a real number. The output of a neuron is arrived at by a non-linear function of total of its inputs. The artificial neurons and connections have weights that adapt itself with on-going learning experience. These weights control the signal strength at the connections. Artificial neurons have a threshold value and signal will be transmitted by neurons only when the aggregate signal exceeds the value of threshold.

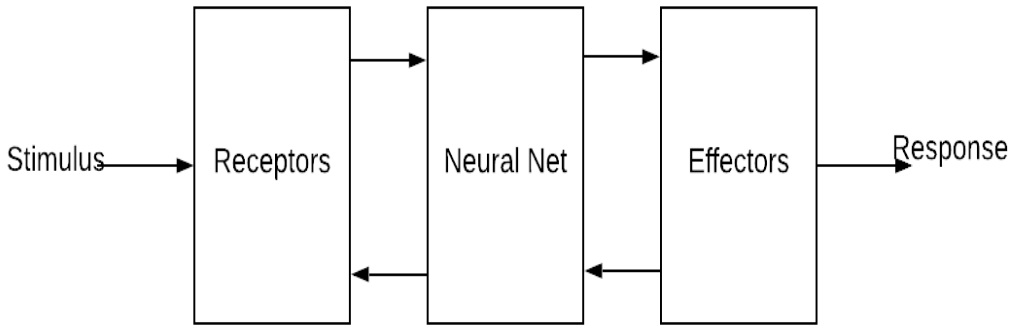


Figure 4.1 Block diagram of nervous system [86]

4.4.2 Components of ANN

The model of basic artificial neuron is shown in Figure 4.2. The basic components are weighting factors, summation function, activation function and transfer function.

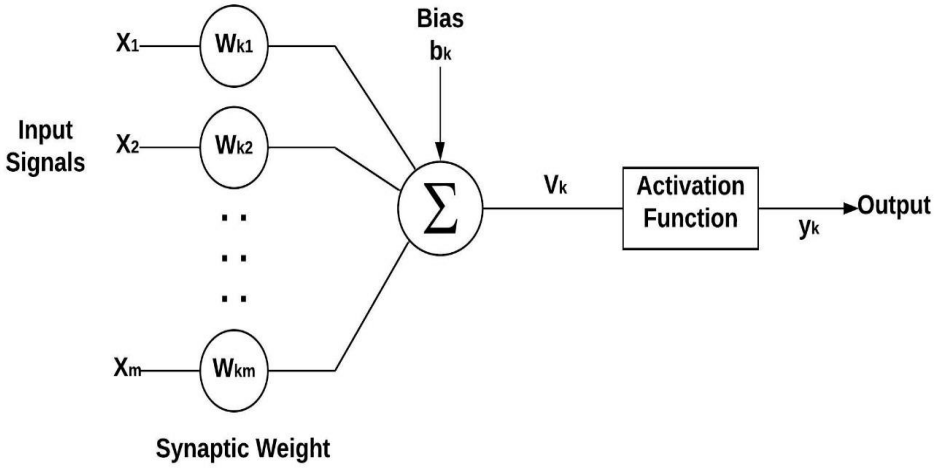


Figure 4.2. Basic artificial neuron model [86]

a) **Weighting Factors:** Weights are adaptive coefficients which determine strength of input signal. In other words, these weights are measures of an input's connection strength. They can be modified. Each input has its own corresponding weight.

b) **Summation Function:** Considering (x1, x2 . . . xn) as inputs and (w1, w2 . . . wn) as relative weights, Product of these two vectors gives total input signal. Total of all these products are derived in the summation function.

b) Activation Function*:* Summation functions are passed on to nonlinear filter called activation function. The activation function enables

the summation output to change with respect to time. The activation functions are basically divided into linear activation function and nonlinear activation function. In linear activation function output will not be limited between any ranges. But in nonlinear activation function output will be confined between limits.

c) **Transfer Function:** Neural output is calculated by comparing summation with threshold in the transfer function. If summation is greater than threshold, a signal is generated by the processing element. If total sum is less than threshold, no signal will be generated.

Hardware implementation of artificial neuron has been of prime focus for many scientists for many last few decades. Figure 4.3 shows hardware implementation of single neuron.

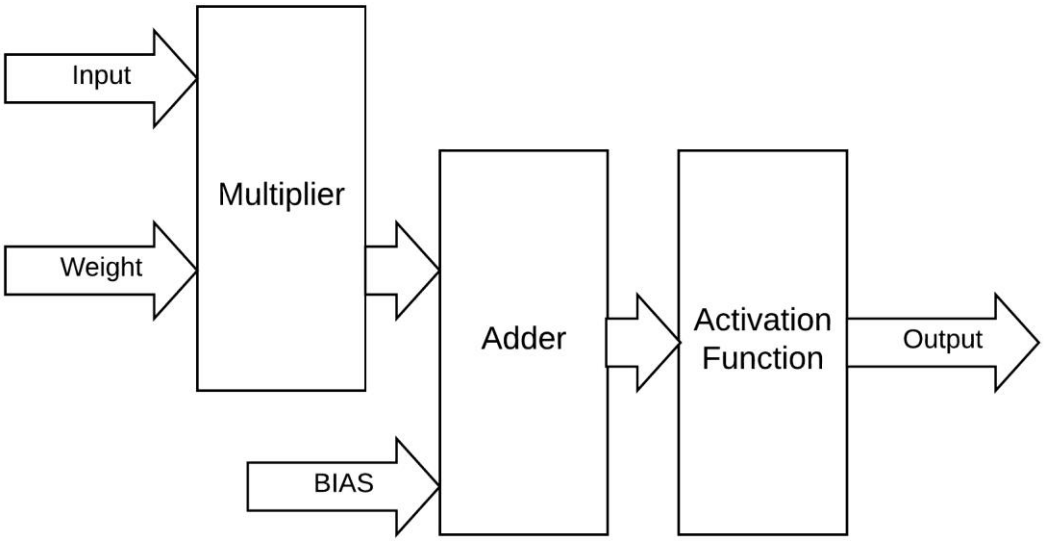


Figure 4.3 Hardware implementation of single neuron.

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4.4.3 Advantages of ANN

Key advantages of ANNs make them capable of solving certain specific problems and situations, as under:

a) ANNs can memorize and represent complex and non-linear relationships. So ANNs have great importance in real life situations due to complex and non-linear nature of relations of inputs and outputs in real life.

b) After analysing inputs and their relationships, ANNs can predict unobserved relationships on undetected data, and can generalize the model.

c) Unlike other prediction methods, ANNs do not impose any constraints on the input parameters. Also research has shown that ANNs have better ability to learn hidden relationships in the data without applying any established relationships in the data [86].

4.4.4 Design of Vedic neuron

Hardware of Vedic neuron can be implemented by replacing standard multiplier with Vedic multiplier in the hardware of single neuron. Figure 4.4 shows hardware implementation of Vedic neuron. In this proposed model, we have used Urdhva Triyakbhyam Sutra. Using these proposed Vedic neurons, various arithmetic and logic circuits for ALU have been designed.

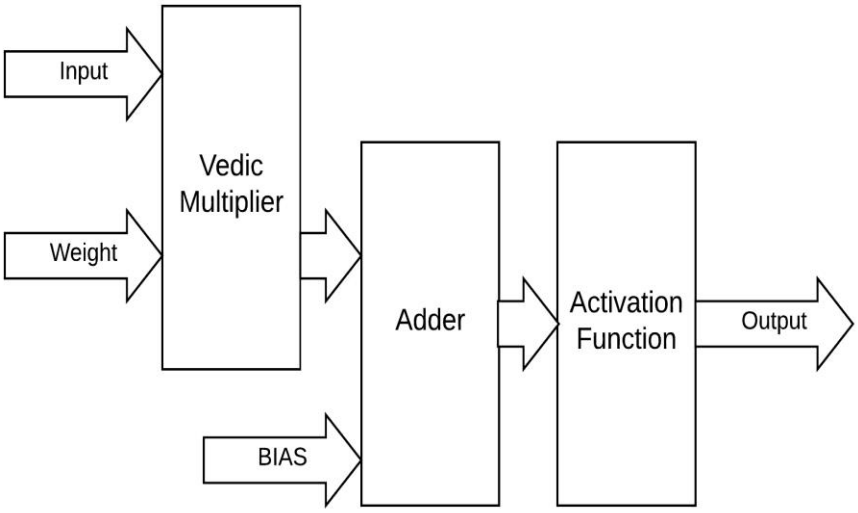

Figure 4.4 Hardware implementation of Vedic neuron

4.4.5 Design of ALU using Vedic neurons.

Block diagram of an ALU is shown in Figure 4.5. This block diagram has been adapted in proposed design, where each block is designed using Vedic neurons.

Use of neurons in the design, gives prediction capability by employing activation function and helps to design an intelligent ALU. To improve the processing speed and efficiency, conventional multipliers in the Neurons are replaced with Vedic multipliers using Urdhva Triyakbhyam Sutra.

Using these Vedic neurons, arithmetic and logical functions have been implemented. The logic gates are designed according to individual truth table conditions. Threshold values and weights are also selected as per the gates. For modeling the AND gate, threshold values and weights can be set as given below:

$w_1 x_1 + w_2 x_2 - \Theta < 0$ i.e. $\Theta > 0$ (when x1 = x2 = 0)

$w_1 x_1 + w_2 x_2 - \Theta < 0$ i.e. $w2 < \Theta$ (when x1 = 0, x2 = 1)

$w_1 x_1 + w_2 x_2 - \Theta < 0$ i.e. $w1 < \Theta$ (when x1 = 1, x2 = 0)

$w_1 x_1 + w_2 x_2 - \Theta \geq 0$ i.e. $w1 + w2 \geq \Theta$ (when x1 = 1, x2 = 1)

x, w and Θ are the input, weight and threshold respectively.

For modeling the OR gate, threshold values and weights can be set as given below:

$w_1 x_1 + w_2 x_2 - \Theta < 0$ i.e. $\Theta > 0$ (when $x_1 = x_2 = 0$)

$w_1 x_1 + w_2 x_2 - \Theta \geq 0$ i.e. $w_2 \geq \Theta$ (when $x_1 = 0, x_2 = 1$)

$w_1 x_1 + w_2 x_2 - \Theta \geq 0$ i.e. $w_1 \geq \Theta$ (when $x_1 = 1, x_2 = 0$)

$w_1 x_1 + w_2 x_2 - \Theta \geq 0$ i.e. $w_1 + w_2 \geq \Theta$ (when $x_1 = 1, x_2 = 1$)

For modeling the XOR gate, threshold values and weights can be set as given below:

$w_1 x_1 + w_2 x_2 - \Theta < 0$ i.e. $\Theta > 0$ (when $x_1 = x_2 = 0$)

$w_1 x_1 + w_2 x_2 - \Theta \geq 0$ i.e. $w_2 \geq \Theta$ (when $x_1 = 0, x_2 = 1$)

$w_1 x_1 + w_2 x_2 - \Theta \geq 0$ i.e. $w_1 \geq \Theta$ (when $x_1 = 1, x_2 = 0$)

$w_1 x_1 + w_2 x_2 - \Theta < 0$ i.e. $w_1 + w_2 < \Theta$ (when $x_1 = 1, x_2 = 1$)

For modeling the NOT gate, threshold values and weights can be set as given below:

$w_1 x_1 - \Theta \geq 0$ i.e. $\Theta \geq 0$ (when $x_1 = 0$)

$w_1 x_1 - \Theta < 0$ i.e. $w_1 < \Theta$ (when $x_1 = 1$)

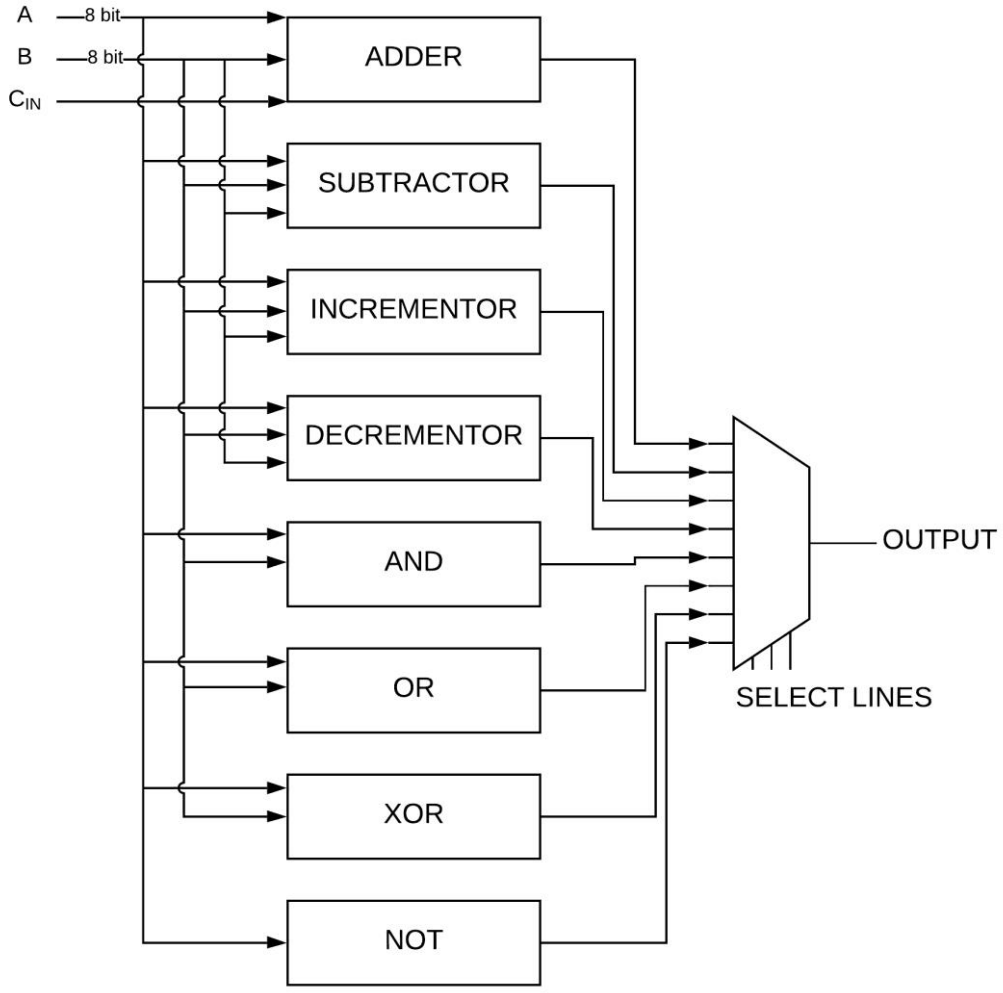

Figure 4.5. Block diagram of an ALU circuit.

4.5 Simulation Results.

Proposed design of ALU has been coded in Active HDL and verified through simulation using Modelsim SE 6.4. The Active HDL codes of the ALU were synthesized using Xilinx ISE 14.7.

4.5.1 Simulation of Vedic neuron.

Eight-bit Vedic multiplier using Urdhva Triyakbhyam has been implemented and its simulation results are shown in Figure 4.6. Considering 'a' and 'b' the binary inputs and 'm' as their product the proposed multiplier operation is functionally verified with different sets of inputs. A typical simulation result for a = 10101100 and b = 01010101 is shown in Figure 4.6 and their product m = 0011100001110000. Figure 4.7 shows simulation results of designed activation function. Considering 'x_1' and 'w_1' as the input and weight signals, and 'y_1' as output of the activation function, operation is functionally verified with different sets of inputs. A typical simulation result for x_1 = 01110000, w_1 = 1000 1110 with bias input = 0000000000010100, output obtained is y_1 = 00011101100100100. Using above Vedic multiplier and activation function, Vedic neuron has been designed. For inputs $x_1 = x_2 = x_3 = 1$, weights are given as w_1 = 000101000, w_2 = 00101000, w_3 = 00111100. For zero threshold, output obtained is y =1. Simulation results of designed Vedic neuron are given in Figure 4.8.

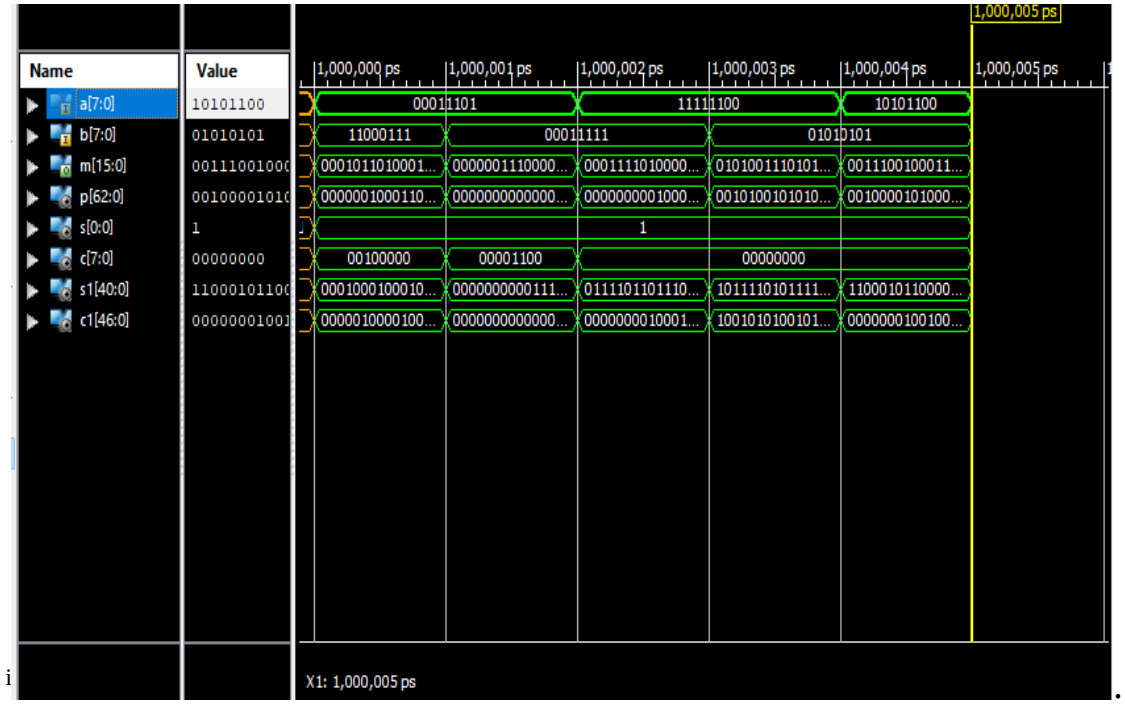

Figure 4.6. Simulation results of 8-bit Vedic multiplier

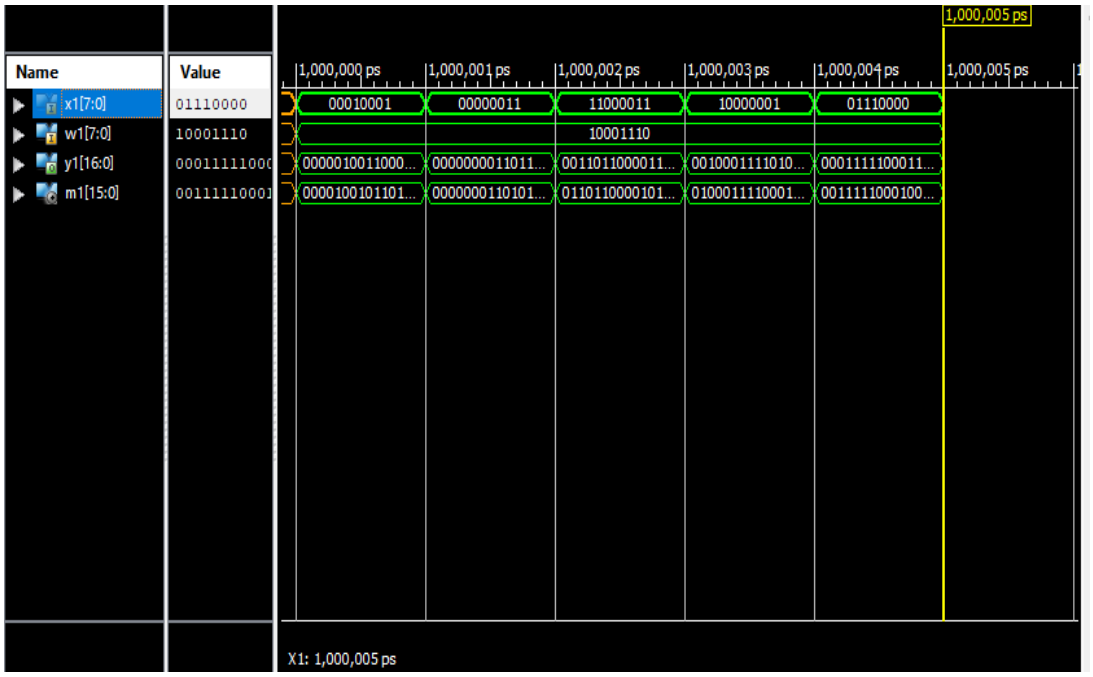

Figure 4.7. Simulation result of Activation Function

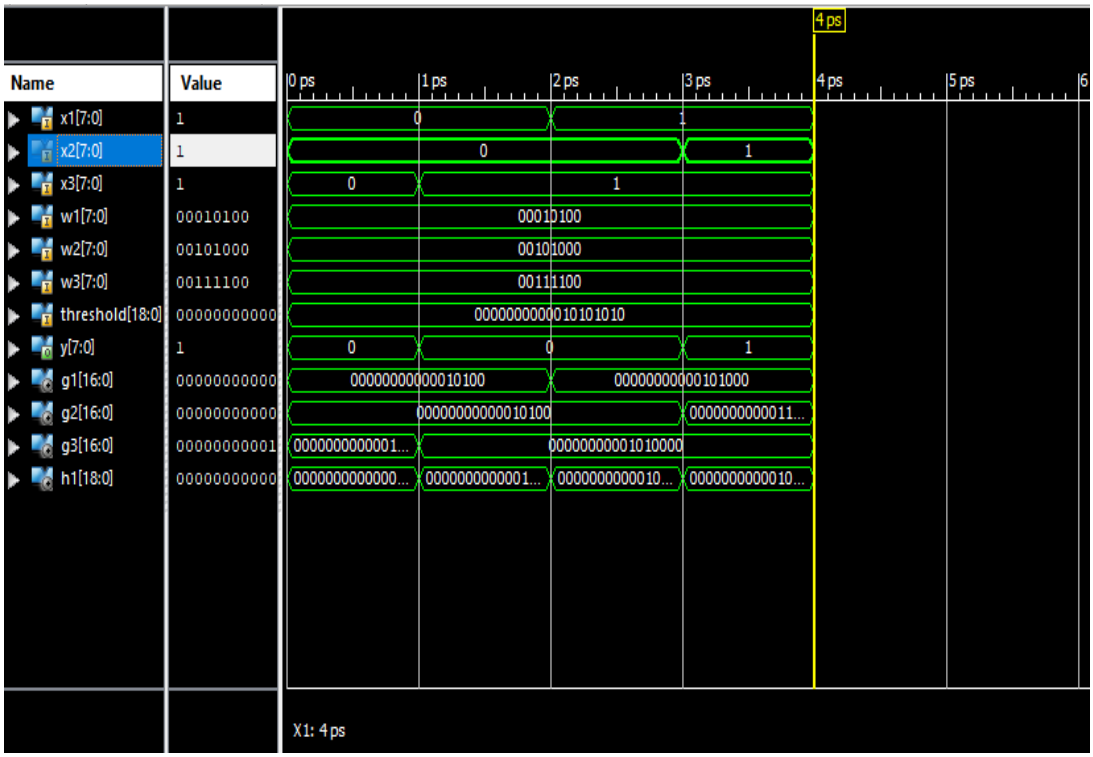

Figure 4.8. Simulation result of Vedic neuron

4.5.2 Simulation of proposed ALU

To design proposed ALU, all arithmetic functions and logical functions given in Table 4.1 have been implemented. Simulation result of eight bit adder is shown in Figure 4.9. Considering ‘a’ and ‘b’ as the binary inputs and ‘y’ as their sum, the proposed addition operation is functionally verified with different sets of inputs. A typical simulation result for a = 10101010 and b = 10101001 with carry c = 1, is shown in Figure 4.9 and their sum y = 01010100 with carry out cout = 1. Simulation result of eight bit subtractor is shown in and Figure 4.10. Considering ‘a’ and ‘b’ as the binary inputs and ‘y’ as their difference, the proposed subraction operation is functionally verified with different sets of inputs. A typical simulation result for a = 10111000 and b = 11111000 with borrow

cs =1, is shown in Figure 4.10 and their difference y= 10111111 with borrow out bout =1. Simulation result of incrementor is shown in Figure 4.11. For eight bit binary input a = 01010111, output obtained is y = 01011000. Simulation result of decrementor circuit is shown in Figure 4.12. For eight bit binary input a = 10101101, output obtained is y = 10101100.

Simulation result of AND gate is shown in Figure 4.13. Considering 'x_1' and 'x_2' as the binary inputs and 'y' as output the proposed AND operation is functionally verified with different sets of inputs. A typical simulation result for x_1 = 01010101 and x_2 = 01110011 is shown in Figure 4.13 and output y = 01010001. Simulation result of eight bit OR gate is shown in Figure 4.14. For input x_1 = 11110011 and x_2 = 01111110, output obtained for designed OR gate is y = 11111111. Simulation result of eight bit NOT gate is shown in Figure 4.15. For input x_1 = 11010101, output obtained for proposed NOT gate is y = 00101010. Simulation result of eight bit XOR gate is shown in figure 4.16. Considering 'x_1' and 'x_2' as the binary inputs and 'y' as output, the proposed XOR operation is functionally verified with different sets of inputs. A typical simulation result for x_1 = 11111110 and x_2 = 00110000 is shown in Figure 4.16 and output y = 11001110. Using all designed arithmetic and logical functions given in Table 4.1, ALU has been implemented. Figure 4.17 shows the simulation results of the proposed eight bit ALU. Using select signal, sel = 101, OR gate is selected. For input a = 00110110 and b = 01110110, output obtained for proposed ALU is out_ALU = 01110110. The existing ALU with all arithmetic functions and logical functions using ANN [85] is also simulated for same simulation settings to compare the performance of proposed designs.

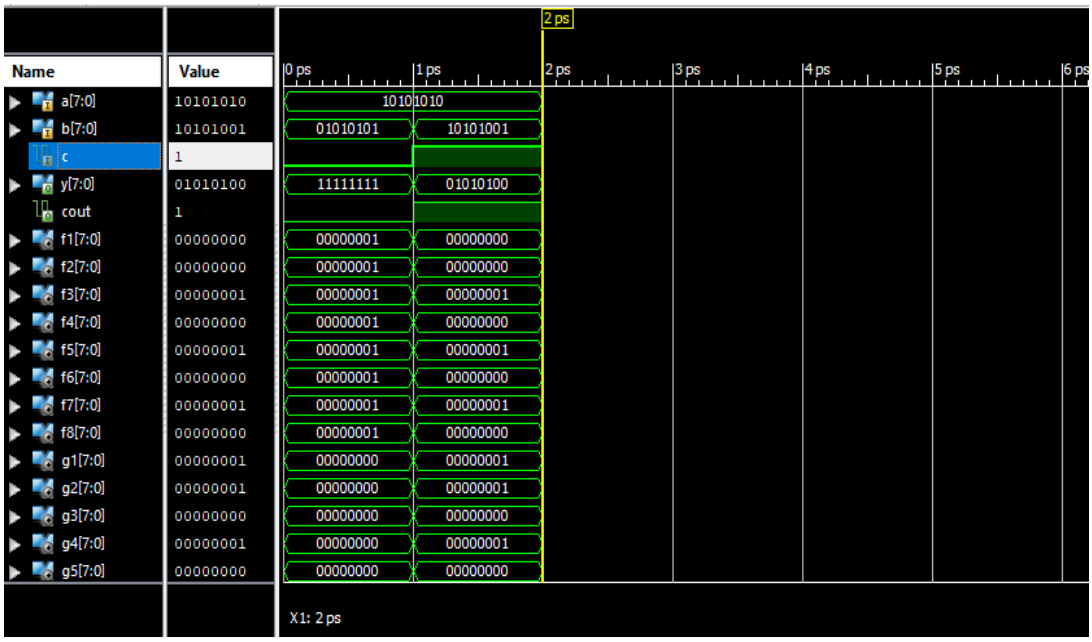

Figure 4.9. Simulation results of 8-bit Adder

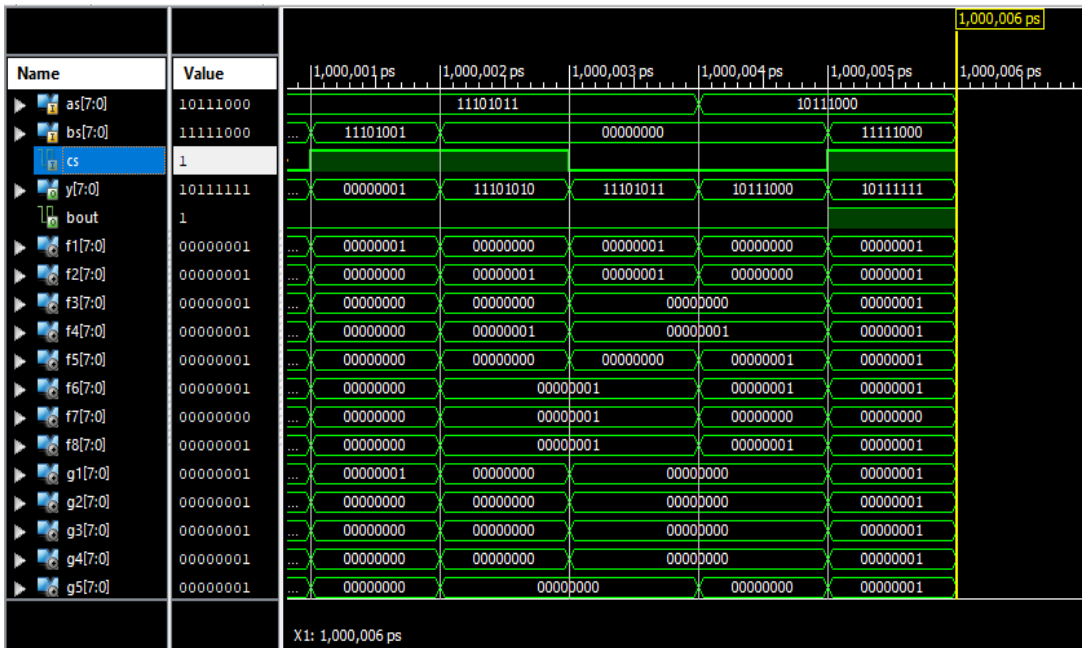

Figure 4.10. Simulation results of 8-bit Subtractor

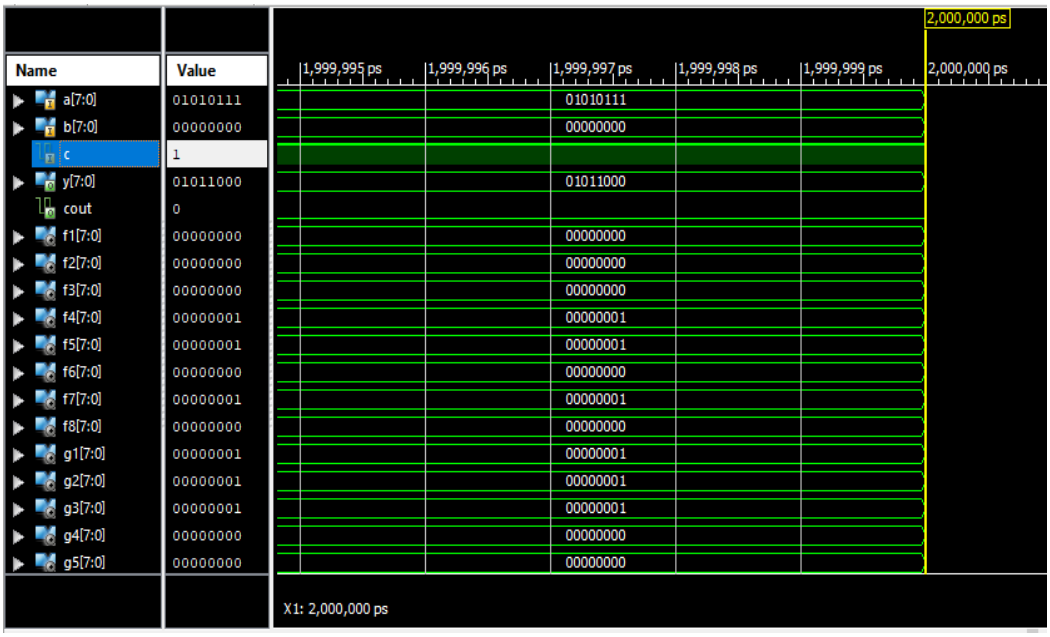

Figure 4.11 Simulation results of 8-bit Incrementor

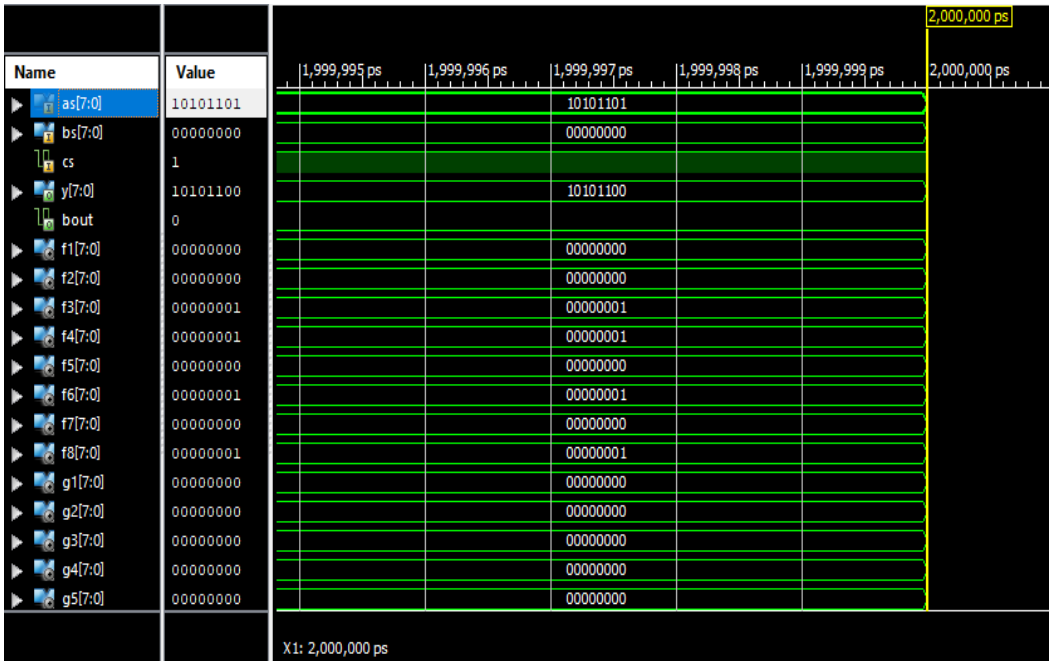

Figure 4.12 Simulation results of 8-bit decrementor

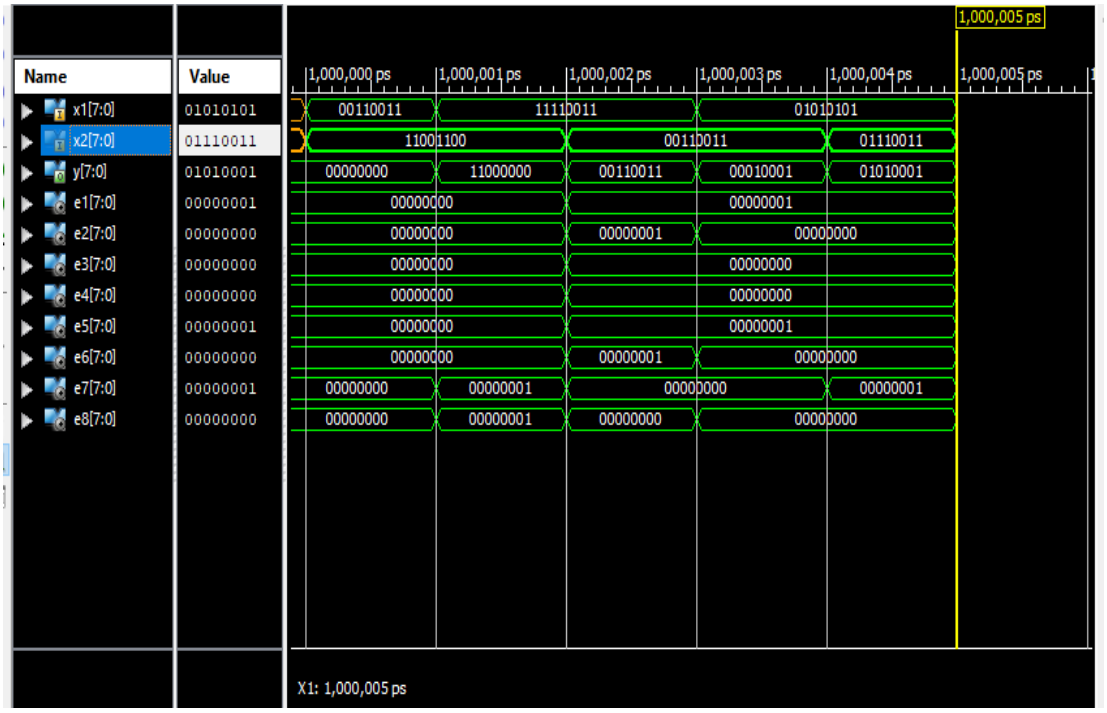

Figure 4.13. Simulation results of 8-bit AND Gate

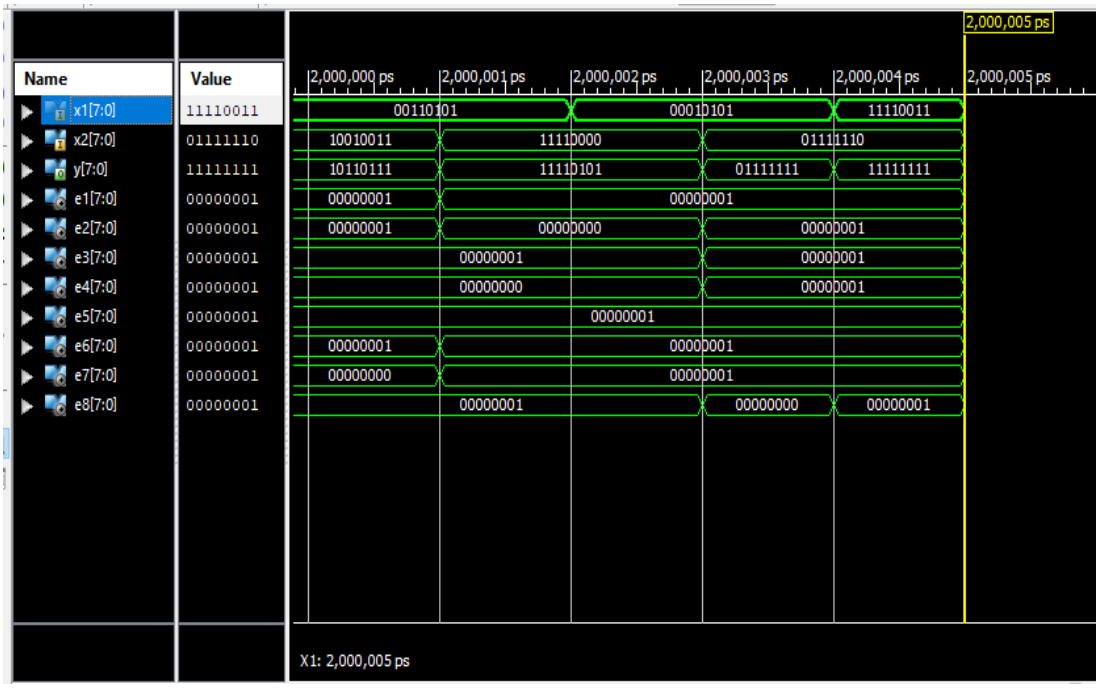

Figure 4.14. Simulation results of 8-bit OR Gate

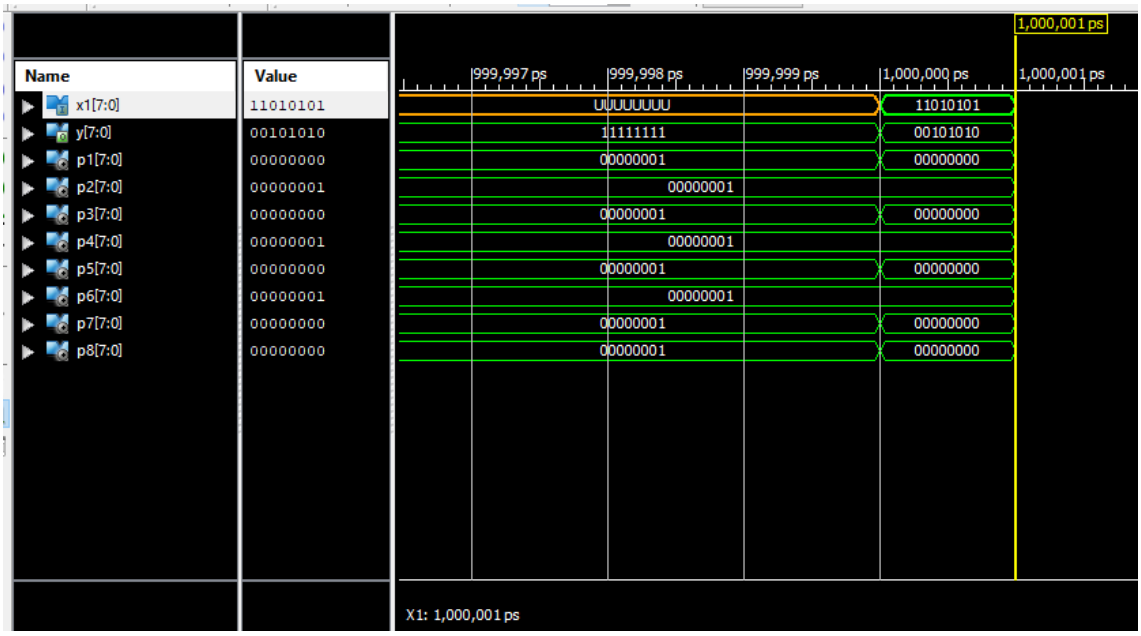

Figure 4.15. Simulation results of 8-bit NOT Gate

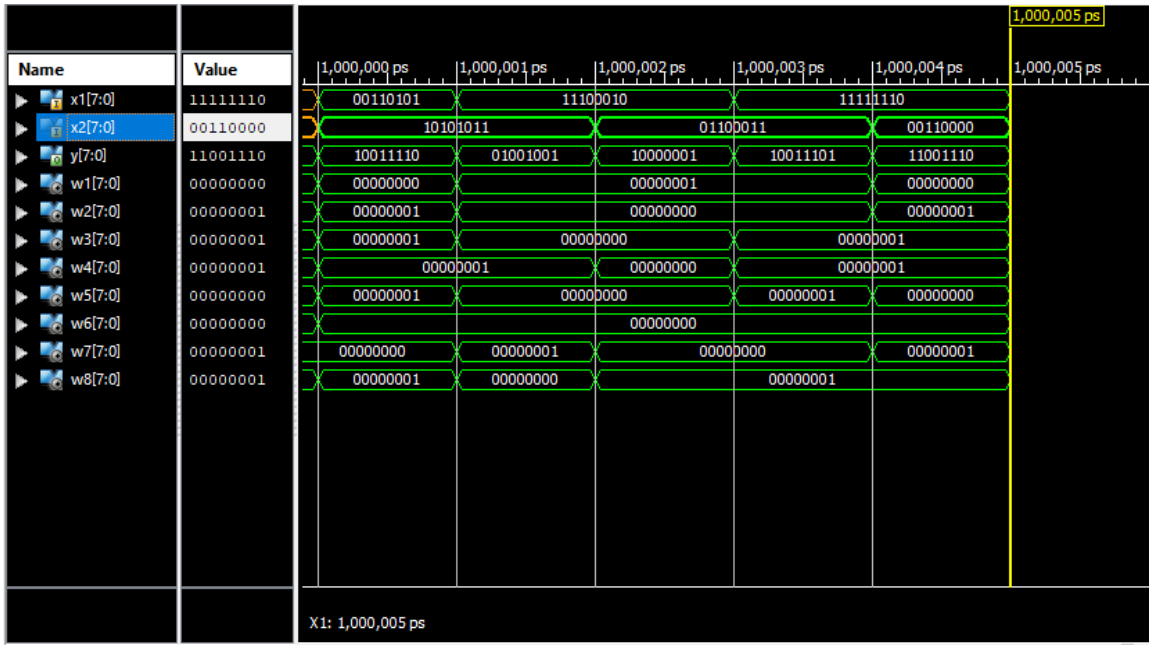

Figure 4.16. Simulation results of 8-bit XOR Gate

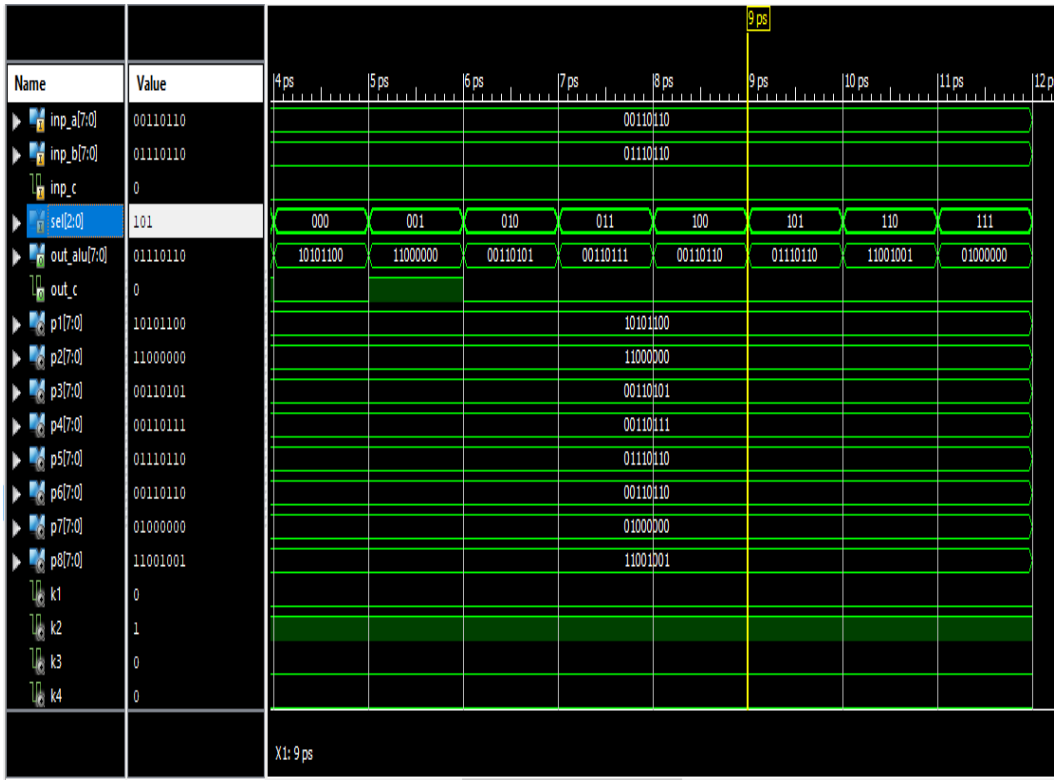

Figure 4.17 Simulation results of Vedic ALU

4.5.3 Results

The performance of proposed ALU is compared with existing conventional circuits. Proposed 8 bit ALU using Vedic neuron exhibits 140.29 ns delay, while conventional eight bit ALU gives 170.93 ns delay. It has been observed that proposed designs of all logical and arithmetic circuits exhibit better processing speed. Summarized results are shown in Table 4.1.

Device utilization summary for eight bit ALU using Vedic neurons and conventional ALU are shown in Table 4.2. Compared with conventional ALU, proposed design is more efficient as it is having less area utilisation**.** Performance analysis is shown in Table 4.3.

Table 4.1

Delay Comparison

S.No	Component	Vedic	Conventional
1.	ALU (8-BIT)	140.29ns	170.934ns
2.	ADDER (1-BIT)	22.8ns	23.1ns
3.	SUBTRACTOR (1-BIT)	45.3ns	48.5ns
4.	ADDER (8-BIT)	36.720ns	36.8ns
5.	SUBTRACTOR (8-BIT)	81ns	85ns
6.	INCREMENTER (8-BIT)	36.43ns	36.77ns
7.	DECREMENTER (8-BIT)	80.09ns	84.2ns
8.	AND (1-BIT)	11.909ns	14ns
9.	OR (1-BIT)	12.14ns	14.2ns
10.	NOT (1-BIT)	11.89ns	13.98ns
11.	XOR(1-BIT)	17.67ns	20.5ns
12.	AND (8-BIT)	34.5ns	37.8ns
13.	OR (8-BIT)	34.23ns	35.98ns
14.	NOT (8-BIT)	12.2ns	13.9ns
15.	XOR (8-BIT)	36.8ns	40.01ns

Table 4.2

Device utilization summary for Vedic logic Vs. Conventional - logic of eight bit ALU

Logic utilization	Vedic logic used	Conventional logic used
Number of Slice LUTs	10355	11625
Number of fully used LUT-FF pairs	0	0
Number of bonded IOBs	29	29
Number of BUFG/BUFGCTRLs	1	1

Table 4.3

Performance Analysis

Vedic ALU	Percentage improvement in speed	Percentage improvement in area
8-bit	17.925%	10.92%

4.6 Conclusion

Contribution from this research is designing an ALU using Vedic neuron, which has been implemented successfully. Compared with conventional ALU, proposed design is more efficient as it is having better processing speed and less area utilization. Overall performance of the designed ALU with Vedic neuron has improved significantly compared with conventional ALU. Processing speed has improved by 17.925% and area utilization has decreased by 10.92% as shown in Table 4.3. Moreover, added advantage of this design is that, artificial neuron can be further trained and used much more efficiently. This ALU design with Vedic neurons can be further refined and used in numerous applications where reduction in size and increase in computational speed are of primary concern.

CHAPTER 5

DESIGN OF IMPROVED POWER-AMPLIFIERS FOR MAKING ENERGY EFFICIENT TRANSCEIVER BLOCKS

5.1 Introduction

A wireless sensor network is a densely distributed group of sensor nodes with limited energy resources. In a sensor node, significant power consumption is contributed by transceivers. Within transceiver block, most of the power is consumed by power amplifiers. Figure 5.1 shows block diagram of transceiver in a sensor node [158]. Transceivers of sensor node consist of various circuits like filters, low noise amplifier, power amplifiers, mixer, oscillator, etc. Power amplifiers are an important part of transmitter section of transceiver. They are used to amplify input signal to be transmitted. An essential parameter for power amplifier is the measure of output power, which in turn, depends on targeted application, efficiency and linearity. Power amplifiers are required to transfer large output power to obtain required power at the destination. Power efficiency is a major issue for power amplifier.

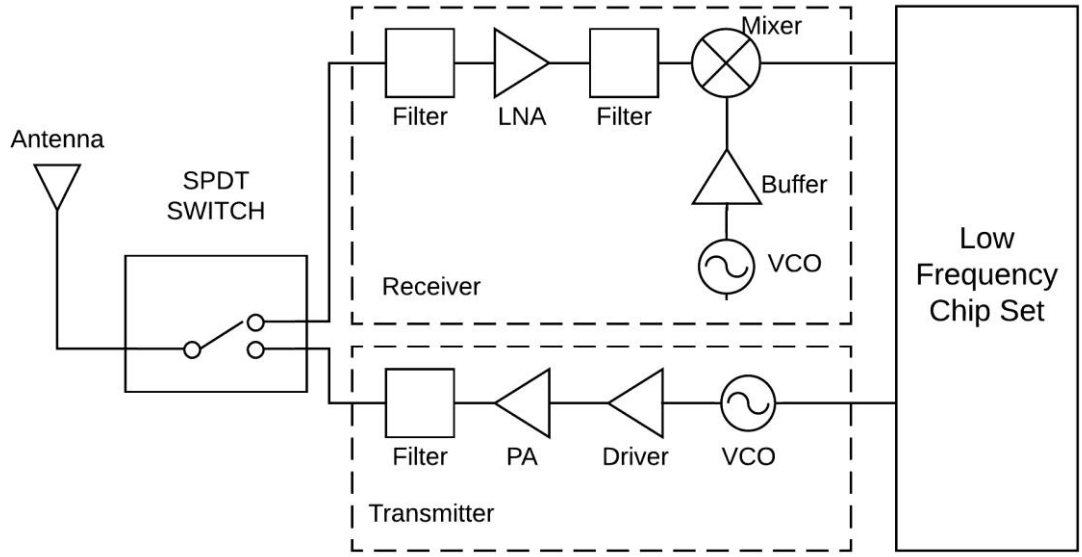

Figure 5.1. Block diagram of transceiver in a sensor node [158].

Since power amplifiers are major sources of energy consumption in the transceivers, energy efficiency of power amplifiers is an important criteria for sensor nodes. The efficiency and bandwidth are the most important characteristics of power amplifiers in sensor nodes. Low power sensor nodes must communicate with their neighbours at hundreds of kilobytes per second and have to operate at higher volumetric densities, as seen in wireless visual sensor networks and wireless multimedia sensor networks. High data rate requires wider band width. But wider bandwidth limits the sensitivity and range. Requirement of wider bandwidth and higher efficiency without reducing sensitivity demands new design strategies.

5.2 State of the Art

Many contemporary research works have focused their efforts towards reducing energy consumption in WSNs. Previous researches have not focused enough on power consumption in transceiver as compared to

energy consumption in other parts of sensor nodes. So, major part of energy is wasted through data transmission. To achieve low power and long lifetime, focus on circuit level design is required. A J Odey et al. have explained the importance of low power transceiver design in [94]. This research paper focuses on energy consumption map of transceiver in different states and within the state transitions of sensor node. Authors have proposed energy consumption model of transceiver and its design parameters which influences energy consumption in OPNET simulation environment.

D G Rahn et al. [95] have showcased a transceiver designed for multiple input/multiple output (MIMO) wireless LAN applications. Proposed transceiver consumed 195 mA in receiver mode and 240mA in transmitter mode with supply voltage of 2.75V. In this work, authors have also proved that power amplifier is a major power consumption unit in transceivers. Hence, class AB power amplifier with adaptive biasing has been designed in this work. Proposed amplifier automatically adjusts bias current according to varying input power and thereby, achieving high linearity.

Y H Chee et al. [98] also implemented a low power class AB power amplifier for WSNs. Proposed amplifier has achieved 35% drain efficiency and 26% power added efficiency while delivering 2.6mW from supply voltage of 1.2V. In reference [99] authors have described important aspects and limitations of power amplifier technology and focused on increasing efficiency and band width without reducing linearity. In switch-mode power amplifiers, the transistor operates in saturation, and either voltage or current, is switched on and off, depending on class of amplifier. A switch can be used in place of transistor. Only voltage is present when

the switch is open and current flows through it when the switch is closed. Hence, class E power amplifier has zero overlap of time between voltage and current. It gives 100% theoretical efficiency. Class-E power amplifier can be considered as a compromise between switched power amplifier and linear class AB power amplifier.

Nathan O Sokal has introduced the breakthrough innovation of the class E amplifier in reference [106]. General principle and operation of class E are described in detail in this paper. The paper presented the new procedure of designing high efficiency class E amplifier, with set of equations. For the designed circuit 96% transistor efficiency has been measured. Reference [111] presents two stage class E power amplifier with higher power added efficiency and linearity. Proposed circuit consists of two stages. A class E output stage and a driver stage. In every cycle, one transistor switches to on state and other transistor switches to off state. Switching operation and zero voltage switching conditions of class E operations lead to reduction in power losses and thereby increasing efficiency.

Our efforts are also focused on a similar direction. Since our aim is to reduce the power consumption of sensor nodes, we have focused on the power amplifiers of the transceivers, as they are responsible for major power consumption in a sensor node. High linearity, greater average output power, wider operating bandwidths and reduced energy consumption are the key design aspects for power amplifiers. This research work has focused on the design of switch mode power amplifiers in class E configuration with high power efficiency and wider bandwidth.

5.3 Problem Formulation.

The efficiency and bandwidth are the most important characteristics of power amplifier in sensor nodes. Low power sensor nodes must communicate with their neighbours at hundreds of kilobytes per second and have to operate at higher volumetric densities. High data rate requires wider band width. But wider bandwidth limits the sensitivity and range. Requirement of wider bandwidth and higher efficiency without reducing sensitivity demands new design strategies. Power amplifier with low power supply gives more reliable operation. But overall gain and efficiency are decreased due to reduced power supply. In class E power amplifiers, these combinations do not exist.

So our study focuses on modifications for basic class E amplifier to achieve improved band width and efficiency at lower power supply. In this study, we propose improvements in design of power amplifier in class E configuration, for the transceivers of wireless sensor nodes. In order to achieve wider band width, cascade of common drain followed by common source in class E configuration has been designed; and for more reliable operations with higher efficiency, class E amplifier has been implemented in double cascode configuration.

5.4 Methodology

To make class E amplifier suitable for sensor nodes, two different configurations using basic class E amplifier are proposed in this work. The first configuration is class E amplifier with double cascoding and second design is class E amplifier designed using common drain followed by common source (CDCS) cascading.

5.4.1 Power Amplifier

Power amplifiers are major source of energy consumption in transceivers. So recent research focused on power amplifiers in switch mode configuration. The RF power amplifiers are classified as classes A-F depending on method of operation. An RF power amplifier uses an active device (BJTS, JFETS, MOSFETS, GaAs MESFETS etc.), dc feed and output matching network.

5.4.1.1 Amplification methods

Class A: In this mode, the transistor in the amplifier always operates in the active region and gives sinusoidal voltage and current waveforms. It gives a maximum of 50% efficiency with linear amplification.

Class B: In class-B amplifier, half of the time the transistor is active and gives half-sinusoid current. Class B provides 78.5% efficiency with linear amplification.

Class C: In class-C power amplifier, less than half time the transistor is active. Efficiency can be enhanced around 100% by decreasing the conduction angle towards zero.

Class D: In Class-D power amplifiers transistors act as switches and generate square waves of voltage and current. Current flows only through on transistor and results ideally 100% efficiency. With faster switching action, efficiency cannot be degraded by load reactance.

Class E: Transistor is biased as a switch in the class E power amplifier. Class E power amplifier is a compromise between switched

power amplifier and class AB amplifier. There will be no overlap between voltage and current through transistor.

Class F: Class F power amplifier uses harmonic resonators in the output to shape voltage and current at drain. In Class-F amplifiers, the drain voltage waveform is square; current waveform is half-sinusoidal [94], [101].

5.4.2 Class-E Power Amplifier

The research in switch mode power amplifier aims to increase efficiency and band width without reducing linearity. Due to high power efficiency, class E configuration is commonly used. A class E amplifier circuit is shown in Figure 5.2 [102]. It consists of transistor Q as a switch, a shunt capacitor C_P, and a series LC circuit. The L_F is a radio frequency choke, which has high impedance at operating frequency. The values of C_P, L, C, L_F and R_L are selected such that power switching losses of transistor are minimised. The shunt capacitor absorbs the parasitic capacitance at the output of transistor. Presence of larger shunt capacitor for same power, load and supply, enables class E amplifier to operate at higher frequencies. During the off state of transistor the current bypasses through the shunt capacitor. The LC series resonator circuit allows current of fundamental frequency to flow from output to load. Class E power amplifier with finite DC inductance provides efficient output matching network. It also provides many other benefits like reduction in size, supply voltage and cost.

For Class E amplifier output waveforms are analog in shape compared with the ideal pulse shaped form of other modes of operation. So class E

amplifiers can be supported by slow switching transistors and are better suited to high frequency operation. Class E power amplifier with shunt capacitor gives 100% ideal power efficiency [95].

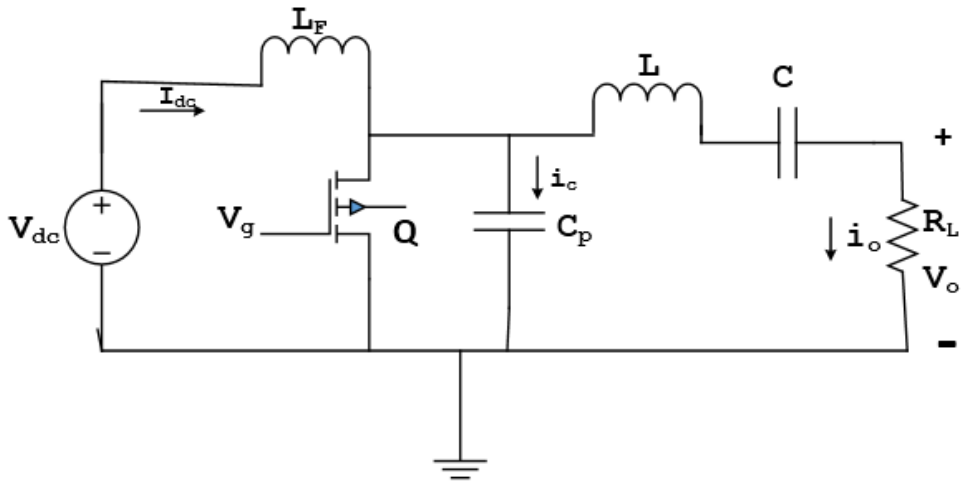

Figure 5.2 Circuit of class E power amplifier

The design equations [26], [102]-[106] for class E power amplifier are as below:

The load resistance R_L is given by

$$R_L = \frac{8{V_{cc}}^2}{(\pi^2+4)P} \qquad (5.1)$$

where V_{CC} and P represent the supply voltage and power respectively.

The current drawn from dc supply (I_o) can be expressed as

$$I_0 = \frac{P}{V_{CC}} \qquad (5.2)$$

The shunt capacitance may be computed as:

$$C_P = \frac{I_0}{\omega R_L V_{CC}} = \frac{1}{\omega\pi\left\{\frac{\pi^2}{4}+1\right\}\frac{\pi}{2}} \qquad (5.3)$$

The components L and C of series resonator are respectively given by (5.4) and (5.5).

$$L = \frac{QR_L}{\omega} \quad (5.4)$$

$$C = \frac{1}{\omega R_L\left\{Q - \frac{\pi(\pi^2-4)}{16}\right\}} \quad (5.5)$$

The radio frequency choke inductance may be computed as

$$L_{f(min)} = 2\left\{\frac{\pi^2}{4} + 1\right\}\frac{R_L}{f} \quad (5.6)$$

Input power $P_{idc} = V_{cc} * I_{dc}$ (5.7)

Output power: $P_{oac} = {I_{R_L(rms)}}^2 * R_L$ (5.8)

Efficiency: $\eta = \frac{Outputpower}{Inputpower}$ (5.9)

5.4.2.1 The Cascode Amplifier

A cascade of common source amplifier followed by common gate is termed as cascode amplifier. The basic idea behind cascode amplifier is to combine the high frequency response and current buffering properties of common gate configuration with large transconductance and high input resistance obtained in common source amplifier. Absence of Miller effect makes common gate high frequency response far superior to common source configuration [159].

The Cascode topology allows design of power amplifier at reduced V_G and V_{DS}, which leads to more reliable operation [97]. Higher output resistance and higher gain can be obtained by adding another level of cascoding. Here another transistor in common gate is added, and it results in increase of output resistance by a factor equal to voltage gain. Common gate configuration acts as current buffer. It takes input signal current at low input resistance and provides nearly equal current at very high output resistance. Presence of common gate configuration has resulted in

increased load current, and in turn, increased efficiency and bandwidth [159].

5.4.2.2 Common drain common source (CD-CS) configuration.

Common drain common source cascading gives wider band width, compared with common source configuration. Transistor in common source configuration, will exhibit a Miller effect that results in large input capacitance. Buffering action of common drain configuration causes a low resistance across input capacitance of common source configuration. Impedance match provided by the common drain configuration in CD-CS cascading results less loss across the load. It leads high load current and increases efficiency and bandwidth [159].

5.5 Simulation Results

First, Class E amplifier with double cascoding as shown in Figure 5.3 is simulated. Following design specifications are used for double cascode class E amplifier: Supply voltage = 12V, Output power = 10W, D = 0.5, Q= 10. For given specifications components values are computed as R_L = 8.31Ω, L_F = 57.6 µH, L_S= 13.22 µH, C_S = 2.17nF. The R_D for CS configuration is considered as 30 Ω and R_S for CG configuration is 100 Ω. Power MOSFET IRF 510 is used for simulation purpose. Transient output of double cascode class E amplifier is as shown in Figure 5.4. Load current measured is $I_{RL\ (RMS)}$ = 1.71 Amp , with DC current I_{DC} = 2.1Amp. The efficiency for the observed values is computed as 96.43%.

Frequency response of double cascode class E amplifier is as shown in Figure 5.5. Band width for this configuration is obtained as 284.4 KHz.

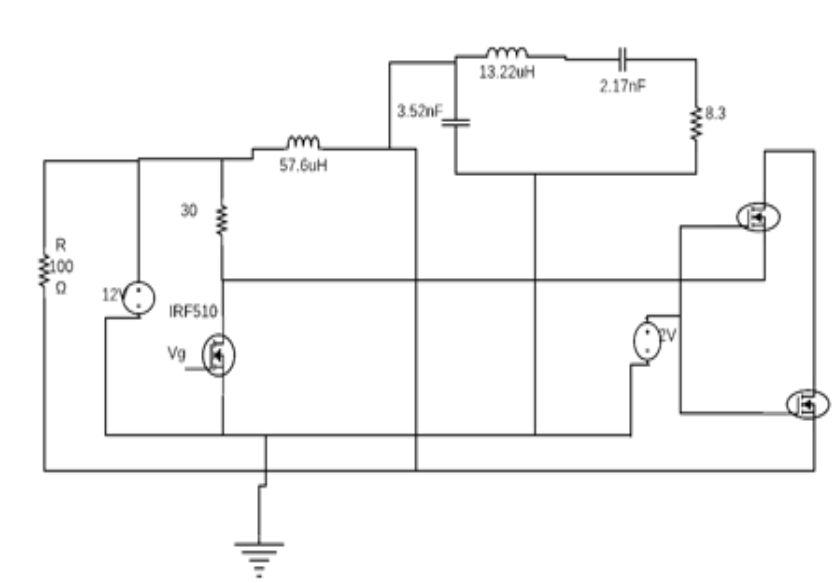

Figure 5.3: Class E amplifier with double cascoding

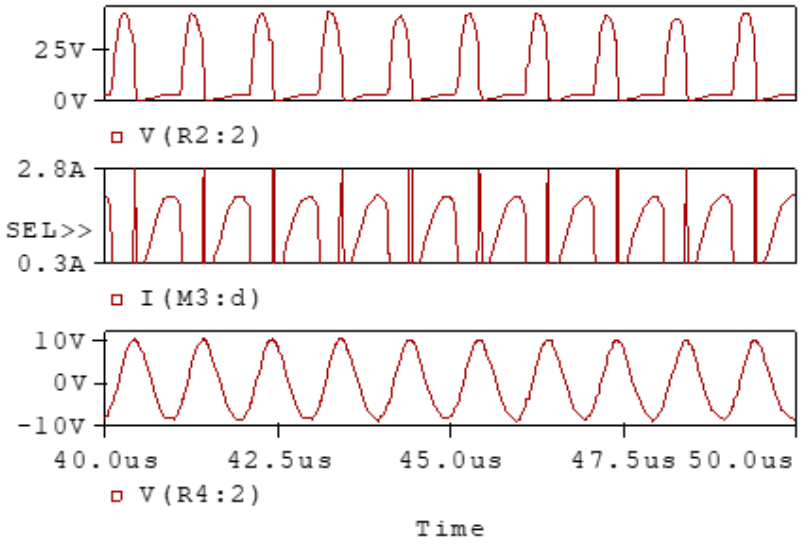

Figure 5.4. Simulation results of class E amplifier with double cascoding.

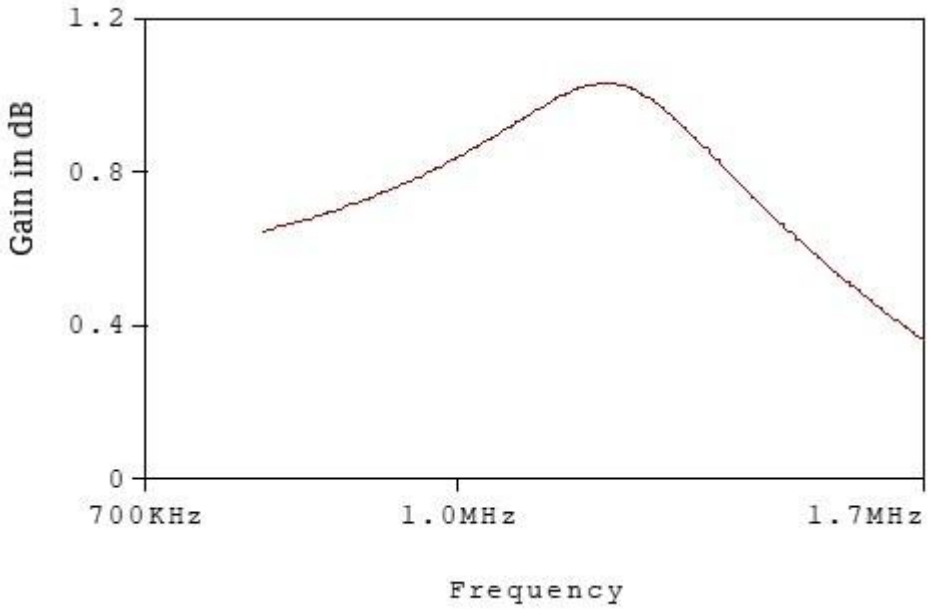

Figure 5.5. Frequency response of double cascode amplifier

The CD-CS configuration is implemented as shown in Figure 5.6. switching transistor IRF 510 is used for both CD and CS configuration. Supply voltage = 12V, 1MHz square pulse of amplitude 1V is applied as V_G. This configuration is also simulated for same design specifications as used for double cascoding amplifier. For given specifications components values are computed using design equations as R_L = 8.31Ω, L_F = 57.6 µH, L_S= 13.22 µH, C_S = 2.17nF. The value of R_D for CS configuration is chosen to be 30 Ω and the R_S for CD configuration is considered to be 100 Ω.

Transient output of class E CD-CS configuration is shown in Figure 5.7. The rms value of load current $I_{RL\ (RMS)}$ is obtained as 4.39 Amp and the dc current is observed to be I_{DC} 14.1 Amp. Hence, the efficiency is computed as 94.65%. Frequency response of CD-CS class E configuration is as shown in figure 5.8 and the band width obtained is 391 KHz.

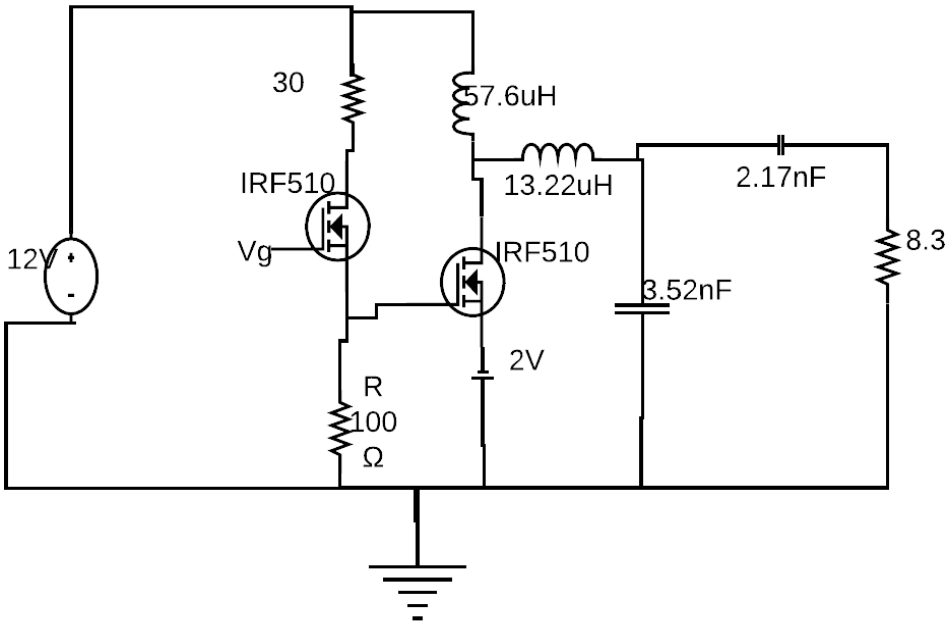

Figure 5.6. Class E amplifier with CD-CS cascading

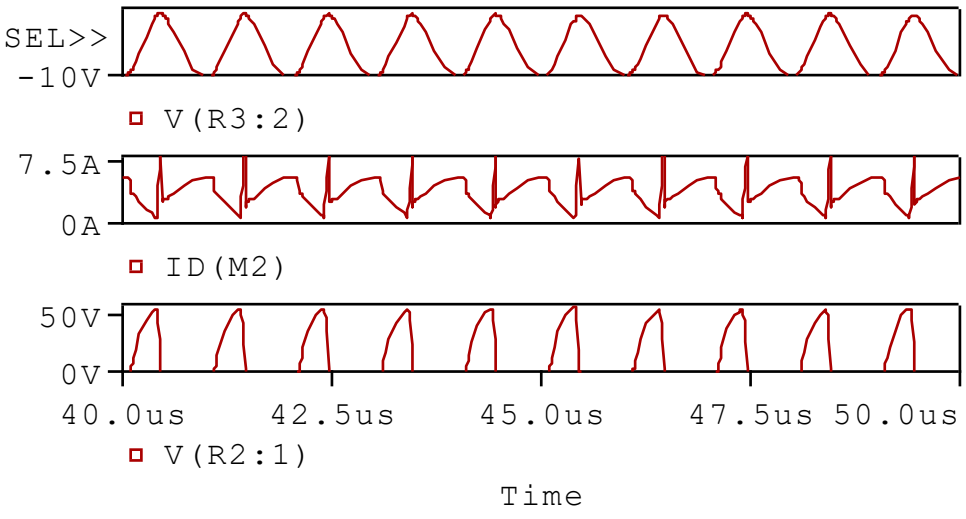

Figure 5.7. Simulation results of Class E amplifier with CD-CS cascading.

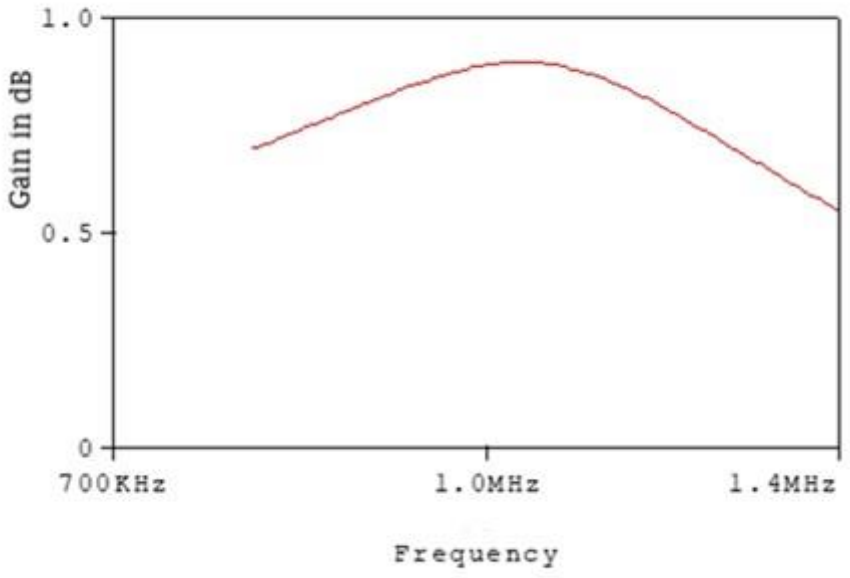

Figure 5.8. Frequency response of CD-CS cascading

The existing class E circuit shown in Figure 5.9 [102] is also simulated for same simulation settings to compare the performance of proposed designs. The transient output is showed in Figure 5.10, where the peak switch voltage is obtained as 43.8V and current is observed as 1.65 Amps. Frequency response of class E configuration is as shown in Figure 5.11 and the band width obtained is 97.3 KHz. From these simulated values the efficiency is computed as 91.67%.

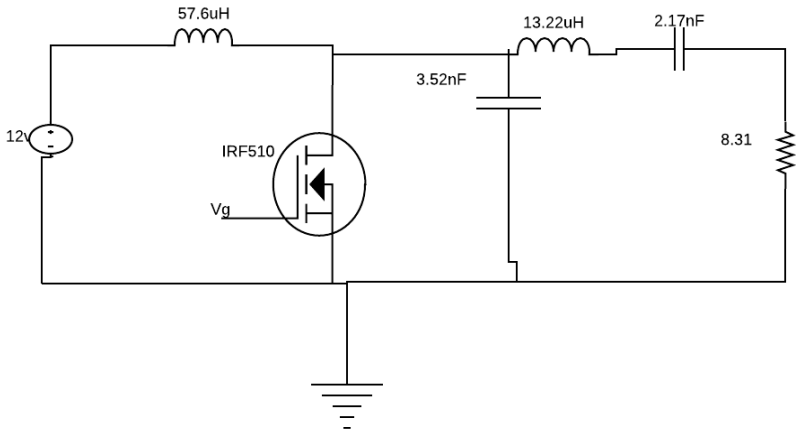

Figure 5.9. Simple class E amplifier circuit.

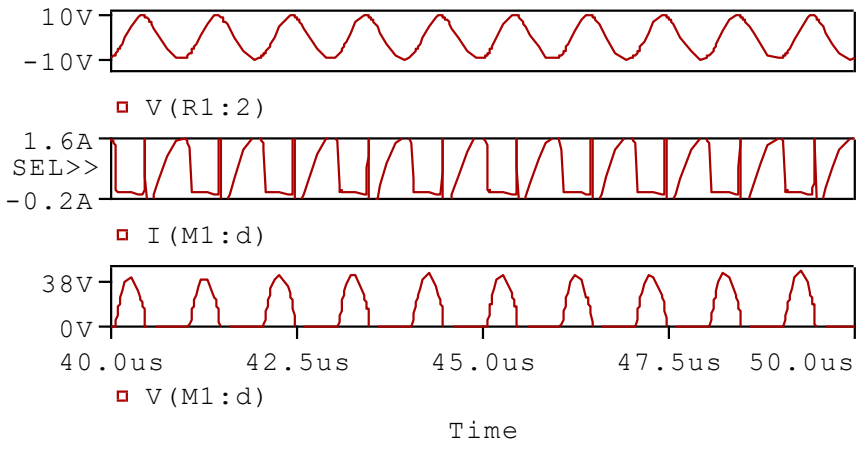

Figure 5.10. Simulation results of simple class E amplifier circuit.

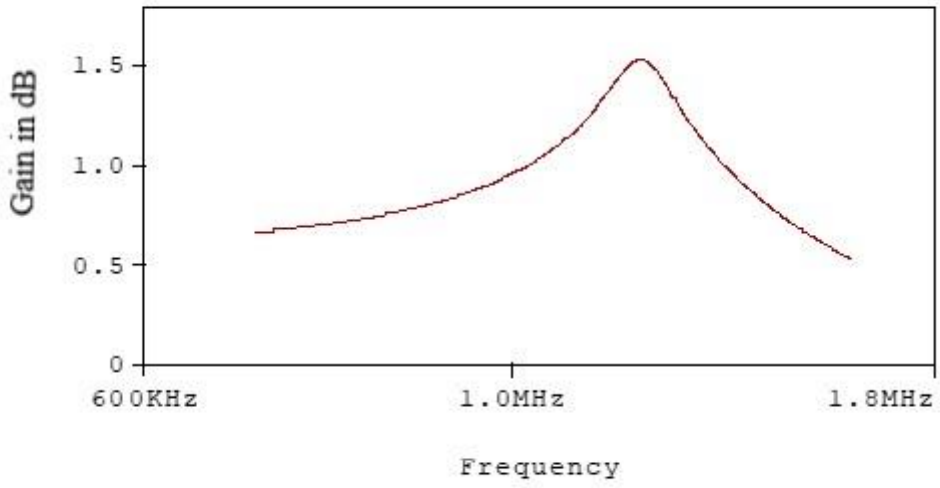

Figure 5.11. Frequency response of class E amplifier

It is thus observed that proposed designs outperform in terms of efficiency and bandwidth. The results are summarised in Table 5.1. It is found from the table that the proposed class E double cascoded configuration is suitable for wide band width and increased efficiency. The CD-CS Class E amplifier gives Maximum bandwidth.

Table 5.1
Performance Comparison Table

Circuit	DC Current (I_{DC})	RMS current (I_{RL})	Efficiency	Band Width
Simple Class E Amplifier[102]	0.52A	0.83A	91.67%	97.3KHz
Proposed double Cascode Class E amplifier	2.1A	1.71A	96.43%	284.4KHz
Proposed CD-CS Class E amplifier	14.1A	4.39A	94.65%	391KHz

5.5 Conclusion

Contribution from this research is designing a class E amplifier suitable for sensor nodes - two different configurations using basic class E amplifier are proposed in this work. The first configuration is class E amplifier with double cascoding and second design is class E amplifier designed using common drain followed by common source (CDCS) cascading.

The transceivers should operate at high data rate for better efficiency which allows many nodes to share same channel through time division multiplexing. Thus, wider band width is another important requirement for power amplifiers used in sensor transceivers. In order to achieve wider band width, cascade of common drain followed by common source in class E configuration has been designed.

Power amplifier can be designed at smaller supply voltage for enhanced reliability. For more reliable operation with higher efficiency, class E in double cascoded has been implemented. Simulated results show better efficiency and band width as compared to existing class E amplifier.

Further low power and high accuracy can be achieved using optimal pulse bias. To reduce supply voltage and DC power consumption, Darlington configuration can be employed. To improve the efficiency, self-bias can be implemented in double cascoding and CD-CS configurations.

CHAPTER 6

AN EFFICIENT SOLAR ENERGY HARVESTING SYSTEM FOR WIRELESS SENSOR NODES

6.1 Introduction

Limited and irreplaceable battery energy is the most important constraint for wireless sensor nodes in sensor networks. Applications like health monitoring of human beings and animals, need unobtrusive sensors. Also in many applications, sensor nodes in the network require unattended operations. Existing power management approaches for sensor networks, mainly focuses on low power architecture and network design. So current researches are focusing on environment energy harvesting techniques along with design of low power architecture.

In this chapter we describe design of a robust solar energy harvesting system to enhance life time of sensor nodes. Using more advanced technologies, sensor nodes can be powered even without batteries by employing energy harvesting systems. The most suitable approach is to combine energy harvesting system with a compact energy

storage device [121]. More research efforts are focused on energy harvesting from the renewable energy sources to design self-powered WSNs. Nowadays various harvesting techniques are available. Solar energy, wind energy, piezo electric energy are some of the available ambient energy sources. Among these, currently most matured technology is based on solar cells and it gives high power density. Requirement of small sized sensor nodes demands small solar panels in the harvesting system which leads to design a compact and simple solar energy harvesting system (SEH) for sensor nodes.

6.2 State of the art

Due to the demand of self-powered WSN nodes, considerable research works have been focusing on various energy harvesting techniques available for WSN nodes. H Sharma et al. [125] have proposed solar energy harvesting (SEH) system as a new design solution for energy constrained wireless sensor nodes. Authors have conducted an in depth survey on SEH that provides an alternative energy source for sensor nodes. Low power energy harvester circuits with small size solar panels and rechargeable batteries will help WSN nodes to become completely self-powered for almost infinite network time. A detailed survey of solar cell efficiency, maximum power point tracking (MPPT) algorithms, solar energy prediction algorithms, DC-DC power converters, processors used for the implementation of these algorithms, battery and super capacitors used for energy storage have been presented. Block diagram of proposed model with detailed description of each block is given the research paper. To implement proposed system, complex hardware systems are required which decreases the reliability and stability of the system.

D Dondi et al. [123] have designed a solar harvester for self-powered wireless sensor nodes with MPPT. This research work has concentrated to maximise efficiency in transferring energy from solar panel to storage device. An analytical model of solar panel based on parameter extraction procedure is used to predict instantaneous power collected by PV panel. Architecture of solar energy harvesting system mainly consists of DC-DC input stage, maximum power point tracker and output DC_DC converter. Instead of using microcontrollers and DSP processors for control action in MPPT algorithm, a comparator is used in the design. A high-speed comparator is used in high light conditions and an ultra-low power comparator is suggested in poor light conditions. Super capacitor is used to store the harvested energy. Efficiency of the implemented circuit is reported as 85%.

Y Li et al. [29] propose a novel intelligent SEH system for WSN nodes suitable for Internet of Things (IOT). Proposed system consists of solar panel, lithium battery and control circuit. To avail full advantage of solar energy, maximum power point tracking circuit is used in the system. Instead of software, charging of lithium battery is managed with hardware using comparator circuit, which resulted in great increase in the robustness of the system and ensures exceptionally long life. O N Samijayani et al. [124] have focused on the potential of solar cell to supply energy for one node. In this research paper, characteristics of solar cell and design of control circuit to control the voltage for battery are described in detail. Control circuit is designed to harvest energy from outdoor at high intensity of light to power battery and also supply directly to sensor node. When battery is fully charged, supply to battery will be stopped and continue supply to sensor node. Characteristics of

solar cell and power needed by WSN nodes are described in detail in this work. From experimental results, authors have proved that to fulfil power requirements of WSN nodes, single solar panel of 180*81*1.55 mm has sufficient capacity even during small light intensity in the mornings and afternoons. Efficiency of solar panel is around 76.59% in the morning and 56.22% in the afternoon. With smaller panels like 70*55*3 mm, enough energy will not be available in small light intensity. Solar panel of 70*55*3 mm has efficiency of 44.51% in morning and 49.94% in the afternoon. The solar energy harvesting models described in state of art is suitable for large systems. These models use complex processors to implement MPPT algorithm or complex hardware circuits to control charging of battery. Our efforts were focused to design a small and compact solar energy harvesting system suitable for sensor nodes.

6.3 Problem Formulation

Recent advances in the applications of WSNs, demands self-powered sensor nodes. Such nodes can be developed by harvesting energy from renewable sources like wind, solar, vibrations, thermal and tidal waves. Hence new design strategies are to be developed for effective utilisation of renewable energy for such self-powered sensor nodes. In this chapter we describe solar energy harvesting for powering small WSN nodes, as it is a mature technology. To minimize the maintenance and cost of operation, we are proposing an efficient, simple and compact solar energy harvesting system for WSN nodes.

6.4 Methodology

The research objective is to design a compact and stable solar

energy harvester circuit for wireless sensor nodes. In order to achieve higher efficiency and reliability, and to avoid usage of complex processors to control battery charging, a simple hardware circuit is proposed in this chapter.

Generally, wireless sensor nodes, operates at 5V DC. Maximum current required by transceiver module of sensor node for enable mode is 40mA and for operation mode is 38mA. Maximum current requirement for sensing unit is 30mA and processing unit is 50mA. Therefore, total maximum current requirement in a sensor node is approximately 120mA. Therefore, maximum power required for one wireless sensor node is 0.6W.

In order to make small portable energy harvesting system, we have used Liberty Solar 3 watt 6 volt solar panel Model No. TOS-03W 6VC. The solar panel of 15cm*15cm (without frame) has the following specifications.

Electrical: Power Max (Pm) - Watt 3 +/- 3% .
Maximum Voltage (Vmp) 9 V.
Maximum Power Current (Imp) 0.333 A .
Open Circuit Voltage (Voc) 10.8 V .
Weight 0.494 Kg with 18cm*18cm*1.5cm dimensions with frame.

To test the performance of proposed energy harvesting system, we have used two sensor nodes DHT 11 and HC05.

DHT 11 is a digital humidity and temperature sensor with the following specifications:

Temperature: 0°C to 50°C

Voltage : 3.5V to 5.5V

Humidity: 20% to 90%

Operating current: 0.3mA (measuring) 60uA (standby)

Output: Serial data

Accuracy: ±1°C and ±1%

Body size: 15.5mm*12mm*5.5mm

HC 05 module - a blue tooth serial port protocol (SPP) - has the following specifications:

Operating Voltage: 4V to 6V (Generally +5V)

Operating Current: 30mA

Range: Less than 100m

Follows IEEE 802.15.1 standardized protocol.

It uses Frequency-Hopping Spread spectrum (FHSS)

It can operate in Master, Slave or Master/Slave mode

6.4.1 Solar Energy Harvesting (SEH) system

Block diagram of a general solar energy harvesting system (SEH) is given in Figure 6.1. Major components in the SEH are solar panel, DC-DC converter, energy storage unit (battery or super capacitor), control unit for DC-DC converter and protection circuit for energy storage unit.

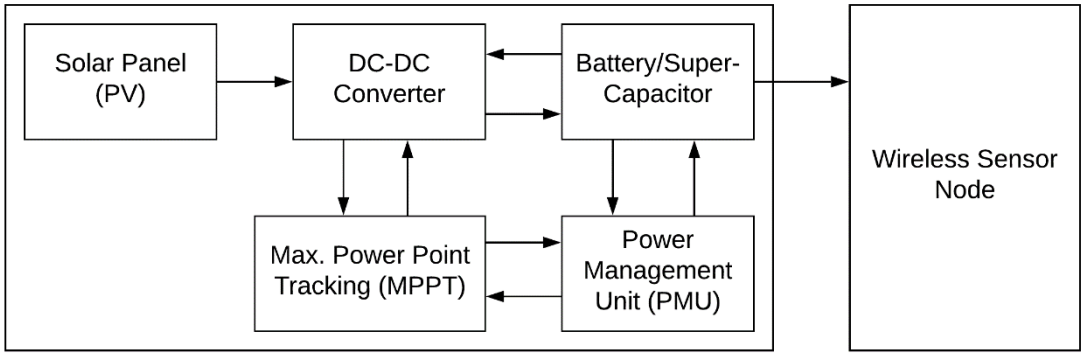

Figure 6.1. Components of SEH system.

Solar energy generation uses photovoltaic (PV) panels consisting of a series of cells made of photovoltaic material. In order to obtain required output voltage and current, these PV cells are arranged in parallel and series combinations in the PV generator. DC - DC converter is a circuit which converts an input DC voltage from one voltage level to another level. This converter is used to match the output voltage from solar cells with the input requirements of battery. MPPT method commonly used in photovoltaic applications for extracting maximum possible solar power under all solar conditions. MPPT controller continuously measures voltage and current from the solar panel and calculates the duty cycle to be applied to the switching device of DC-DC converter. Solar Energy Prediction Algorithms (SEPA) are also available to calculate amount of energy to be extracted during the day at a specific instant. It predicts the energy on the basis of available energy during past days at same times. But SEPA has very high prediction errors. Commonly used energy storage devices in SEH-WSN nodes to store generated electrical energy are batteries and super capacitors.

6.4.2 Modified solar energy harvesting system for WSN nodes

Solar energy harvester for WSN nodes with compact models of solar panel and harvesting circuits includes a photovoltaic (PV) panel, DC-DC converter and control circuit, battery and an inverter. The circuit architecture of modified SEH system is presented in Figure 6.2. Energy harvesting using small portable polycrystalline PV panel is used to enable WSN nodes in the proposed design. Requirement of small size sensor nodes demands smaller size solar cells that can generate only limited energy. Voltage generated from the compact PV panel is less than the required output voltage even at maximum sunlight. In order to increase the voltage, PV panel is directly connected to boost converter. Since super capacitors have lower power density and higher leakage, Lead acid rechargeable battery is used as energy storage device.

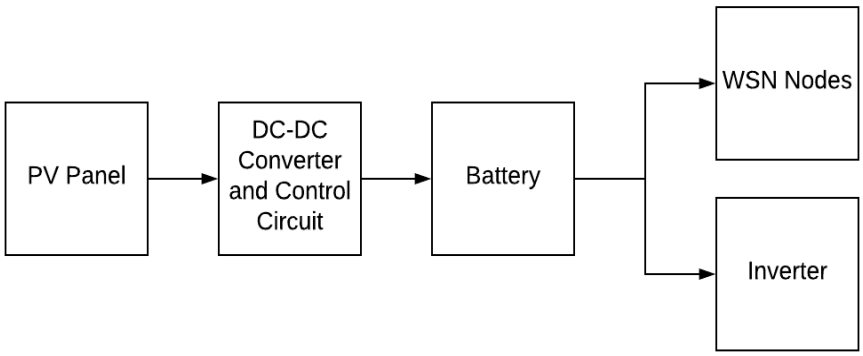

Figure 6.2. Block diagram of proposed SEH system

The complete circuit diagram of the proposed system is given in Figure 6.3 and its hardware implementation is shown in Figure 6.4. In

the proposed circuit diode D1 is used to reverse current protection of solar panel. The LED gives indication of current flow from solar panel. Voltage booster circuit for doubling the voltage from solar panel is designed using 555 IC and it again boosted at the next stage. Transistor BC547 act as a switching device. The 555IC is configured to operate in astable multivibrator mode. Representing ON and OFF times of astable multivibrator by t_1 and t_2 respectively the design equations to determine the time period $(t_1 + t_2)$ of the output can be expressed as

$$t_1 = 0.693(R_1+R_2) \quad (6.1)$$

$$t_2 = 0.693(R_2) \quad (6.2)$$

$$(t_1 + t_2) = 0.693 (R_1+2R_2). \quad (6.3)$$

This boosted voltage is used to charge the battery. In this design, charging of battery is controlled by a hardware circuit using voltage regulator and switching diode D. During sun light rechargeable battery is charged. If voltage of battery crosses the upper limit voltage that is determined by regulator output, switching diode turns off and battery charging discontinues. When battery voltage drops beneath the threshold voltage, switching diode becomes ON and battery continues to charge. MPPT algorithm is widely used in medium and high power solar systems. But it demands very complex control measures which are built into the design employing micro controllers and DSP processors. This increases the cost and complexity of the system. Proposed system is more stable compared with the existing microcontroller based system. Complex algorithms are avoided in the proposed system. Digital temperature and humidity sensor DHT 11, and blue tooth module HC05 are connected from 12V battery through 5V regulator ICs. An inverter

using two MOSFETs instead of four is also designed to convert DC input into AC output which is shown in Figure 6.5. If any sensor applications requires AC, such as remote sensors to energise loads, like water pump, alarm lights etc, this inverter output can be used.

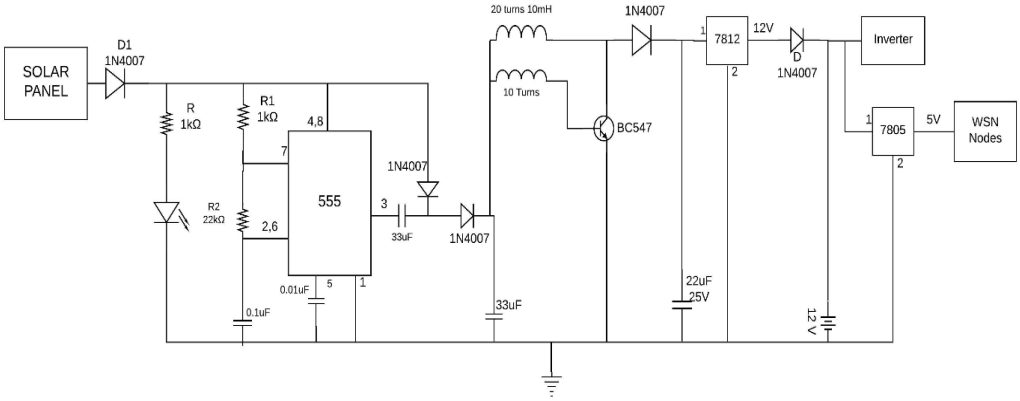

Figure 6.3. Circuit diagram of solar harvesting for wireless sensor node

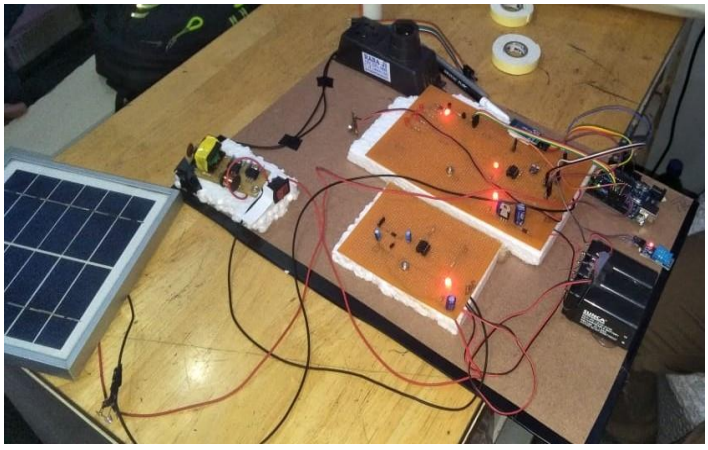

Figure 6.4. Photo of design implementation in lab

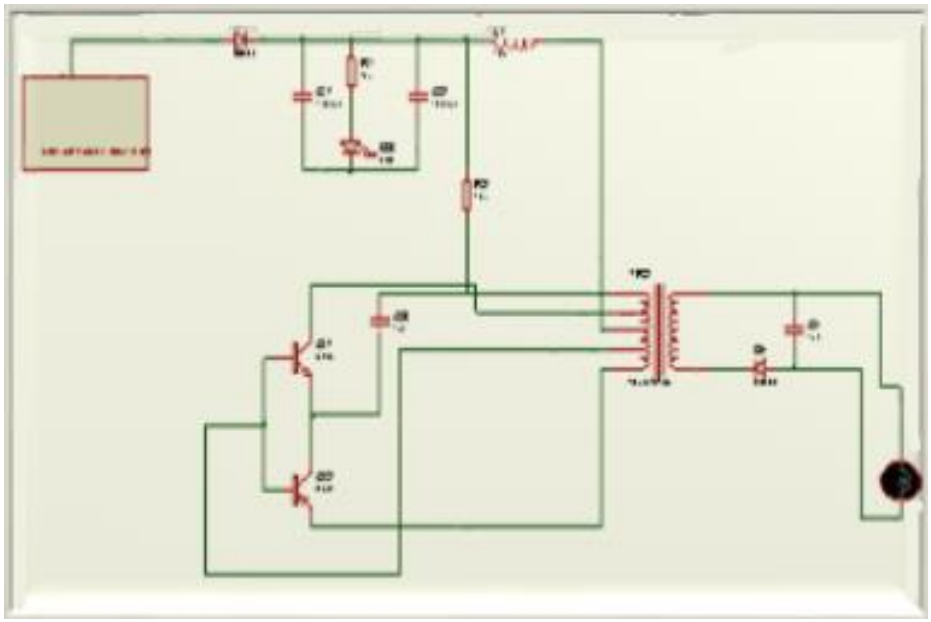

Figure 6.5. Circuit diagram of inverter.

6.5 Results

The experimental results are shown in Table 6.1. In normal indoor condition, panel output was measured as 2.8V. This panel output of 2.8 V is stepped up by booster DC- DC converter into 22V. Battery output achieved was 11.26V. The inverter circuit converts this input into 96.5V. Output from voltage regulator 7805 to sensors DHT-11 and Bluetooth module HC05 were measured as 4.91V and 4.9V respectively. Same set of readings were recorded at different indoor and outdoor conditions with varying intensity of light as shown in Table 6.1. At intense sunlight, maximum panel output was found to be 5.88V. This further proves that the proposed design requires only boost converter circuit. There is no requirement of buck converter or boost-buck converter in this system. Experimental results show that this solar

supply system can enable WSN nodes to operate normally and is suitable for low power applications. Table 6.2 shows values of quantitative improvements in performance characteristics compared with existing system [126].

Table 6.1
Experimental Results

S NO	CONDITION	PANEL OUTPUT	BOOSTER OUTPUT	BATTERY OUTPUT	AC OUTPUT	INPUT TO DHT-11	INPUT TO BLUE-TOOTH
1	NORMAL	2.8V	21.49V	11.26	96.5V	4.91V	4.9V
2	2FLASH LIGHT	3.5V	22V	11.26	95V	4.9V	4.9V
3	4FLASH LIGHT	3.7V	22V	11.26V	95V	4.9V	4.9V
4	AT SUNLIGHT	5.88V	22V	11.26V	96V	4.91V	4.9V

Table 6.2
Performance Comparison with Existing System

S No		EXISTING SYSTEM [126]	PROPOSED SYSTEM
1	No of sensors used	01	02
2	Maximum Voltage and Current Requirements for each Sensor	5V, 120 mA	5V, 120 mA
3	Solar Panel used	5W, 8V, 0.65 A	3W, 6V, 0.5 A
4	PV Module voltage (Minimum Value) To Battery Voltage	3.3 V to 5 V Battery	2.8 V to 12 V Battery
5	AC Output Voltage	-	96 V

6.6 Conclusion

Contribution from this research is designing a solar harvester for WSN nodes with compact models of solar panel and harvesting circuits. The proposed system is suitable for many outdoor applications such as precision agriculture monitoring systems, forest fire detection systems, bird detection and monitoring systems and weather monitoring stations etc.

Recent advances in sensor and wireless technologies provide boundless opportunities in development and application of wireless sensor systems for precision agriculture. Wireless sensors are used to understand changes in the crops to assess optimum point for crop harvesting, in estimating requirement of fertilizers and to accurate prediction of crop performance. WSN plays an important role in the handling and managing of water resources for irrigation. Our proposed energy harvesting system can be used for DC and AC requirements of WSNs used in such precision agriculture field.

At present wireless sensor networks are using commonly for forest fire detection in place of traditional watch towers, optical smoke detectors etc. Line of sight and early stage of fire process problems are solved with the introduction of WSNs, because it provides all required information that influences the environment at any moment. Real time monitoring can be obtained by using neural wireless sensor networks. Proposed system can be used to recharge batteries and to operate alarm lights motors and communication equipment in case of emergency.

Development of WSN technology have led to affordable and sustainable weather boards that can operate as mini weather stations. Since procuring and maintaining traditional weather stations is very expensive, these professional weather stations are replaced by mini weather stations. Proposed solar energy harvesting system can be used with these weather monitoring stations.

In bird monitoring system a force sensitive resistor is used to sense the amount of seed present in the feeder. To obtain physical weather data temperature and humidity sensors are attached along with webcams. Generally four AA batteries are used in the monitoring system. Proposed solar energy harvesting can be used to recharge these batteries and can enhance life span of monitoring system. Proposed system can also be used to operate motors to fill seed or water in the feeders.

This design performed stable with high reliability and efficiency and without much power loss. In order to achieve long lasting power for the system, proposed design focused energy saving principles by using low power consumption devices in each module. The designed system can afford stable power supply with 5V output voltage through voltage regulator. Output of voltage regulator IC supplying power to WSN nodes required to match operating voltage of sensors adopted. Selection of voltage regulator IC depends on the sensors employed in the system. To achieve more efficiency, polycrystalline solar panel used in proposed design, can be replaced mono crystalline panel, which is more compact and costly. Low cost Lead acid battery in this design can be replaced with lithium battery in order to minimise maintenance and to enhance the lifespan.

Exploiting available energy sources from the surroundings of the sensor nodes for recharging batteries and for powering sensor nodes is an attractive proposition to enhance the life time of power constrained WSNs. Instead of solar, RF energy harvesting can be used for low power wireless devices and is suitable for wide range of applications [160]-[164].

CHAPTER 7

CONCLUSION

In this thesis, for accomplishing our research objectives, we have focused on blocks of sensor node in which power consumption is comparatively large and tried to develop solutions for the same. Multipliers have an important role in the architecture of low power sensor nodes. Full adder is the major source of power consumption in multiplier. Hence, decreasing the power dissipation in full adder, in turn, will reduce the overall power dissipation of the multiplier.

Major domains of power consumption in a sensor node are during sensing, communicating, and data processing. Power consumption for processing data is much less compared to power consumption for data communication. So local data processing at each node is important in minimising power consumption of a sensor node.

In a sensor node, maximum power consumption is in transceivers. In transceivers most significant power consumption is contributed by power amplifiers. So design of power amplifier plays a significant role in minimising power consumption of a sensor node.

To design a self-powered wireless sensor node, various harvesting techniques from renewable energy sources are available. Using more advanced technologies and suitable energy harvesting system sensor nodes can be powered even without batteries. Among various ambient energy sources available most matured technology is based on solar cells and it gives high power density. Requirement of small sized sensor nodes demands small solar panels in the harvesting system which leads to design a compact and simple solar energy harvesting system for sensor nodes.

7.1 Summary of Work Done

Several important conclusions appear to emerge from this study. First, multipliers based on Vedic mathematics provides high speed and low power. Vedic multiplier architecture can be easily extended to higher number of bits due to its regular structure. In terms of delay and power dissipation full adder designed with multiplexer and XOR gate gives best performance. To improve the performance of multiplier instead of traditional full adders, full adder with multiplexer can be used. We have designed a high-speed Vedic multiplier based on Urdhva Triyakbhyam Sutra. Summation of partial products is done with high speed MUX based full adders. Compared with other conventional Vedic multipliers, proposed design gives much less delay and power dissipation.

Use of neurons in the design of ALU gives prediction capability by employing activation function and helps to design an intelligent ALU. But this design suffers from bulky and slow architecture. We have applied Vedic logic in all arithmetic and logic operations. Design of

ALU using Vedic neuron has been implemented successfully. Compared with conventional ALU, proposed design is more efficient as it achieves better processing speed and lower area utilization.

In class E power amplifier, compared with common source configuration, common drain common source cascading gives wider band width. Transistor in common source configuration, will exhibit a Miller effect that results in large input capacitance. Buffering action of common drain configuration causes a low resistance across input capacitance of common source configuration. Impedance match provided by the common drain configuration in CD-CS cascading results less loss across the load. It leads high load current and increases efficiency and bandwidth.

In cascode topology of class E power amplifier, high frequency response and current buffering properties of common gate configuration is combined with large trans conductance - high input resistance of common source amplifier. It allows the designer to design at reduced power supply, which leads to more reliable operation with higher efficiency and band width. We have designed these two configurations using basic Class E amplifier which are more suitable for sensor nodes.

We have designed a solar harvester for WSN nodes with compact models of solar panel and harvesting circuits to increase the life span of battery. This design has performed stable with high reliability and efficiency and without much power loss. In order to achieve long lasting power for the system, proposed design focused energy saving principles by using low power consumption devices in each module. AC output from inverter enables the designed solar system to use in applications

with remote sensors to energise loads, such as water pump, alarm lights, and telecommunication equipment. Experimental results have shown that this solar supply system could enable WSN nodes to operate normally for longer durations and is, thus, suitable for low power applications.

7.2 Future Work

The high-speed low-power Vedic multiplier designed in chapter 3 can be used in most frequently used computation intensive arithmetic functions (CIAF) like multiply and accumulate and inner product. It can be implemented in Digital Signal Processing (DSP) applications like convolution and Fast Fourier Transform and filtering. It can also be used in ALU of processors. Multiplication time is a dominant factor in determining instruction cycle of DSP chips, as execution time of DSP algorithms mostly determined by multiplication. Due to the regular and parallel structure of designed multiplier, for large number of inputs, design complexity decreases.

In chapter 4, ALU has been designed using Vedic Neurons. Compared with conventional ALU, proposed design is more efficient as it results in better processing speed and less area utilization. Added advantage of this design is that, artificial neuron can be further trained and used much more efficiently. This breakthrough ALU design with Vedic neurons can be further refined and used in numerous applications where reduction in size and increase in computational speed are of primary concern.

Class E power amplifiers are designed and simulated with double cascoding and CD-CS cascading in chapter 5. Simulated results have shown better efficiency and band width as compared to the existing Class E amplifier. These designed configurations can be used in wireless visual sensor networks and wireless multimedia sensor networks as high data rate requires wider band width. Further, low power and high accuracy can be achieved using optimal pulse bias. To reduce supply voltage and DC power consumption, Darlington configuration can be employed. To improve the efficiency, self-bias can be implemented in double cascoding and CD-CS configurations.

In chapter 6, we have designed a solar harvester for WSN nodes with compact models of solar panel and harvesting circuits. Further, a hybrid energy storage module can be used with super capacitors as primary storage and batteries as backup energy source for better performance. Low cost Lead Acid Battery in this design can be replaced with lithium battery in order to minimise maintenance and to enhance the lifespan. For very low power wireless sensor nodes, RF energy harvesting can be used instead of other renewable energy sources.

Annexure

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Annexure

Published Works

International Journal Papers

1. Saji M Antony, S. Indu and Rajeshwari Pandey, "Design of High Speed Low Power Multiplier for Sensor Nodes", *International Journal of Control Theory and Applications,* ISSN: 0974-5572, Volume 11, Number 1, 2018, pp. 29 -38.

2. Saji M Antony, S. Indu and Rajeshwari Pandey, "Design Improvements in Power Amplifier for Making Energy Efficient Transceiver Blocks of Sensor Nodes", *International Journal of Innovative Technology and Exploring Engineering*, ISSN: 2278-3075, Vol 08, Issue 07, May 2019, pp 65-70 (**Scopus indexed**)

3. Saji M Antony, S. Indu and Rajeshwari Pandey, "High Speed ALU Design using Vedic Neurons for Energy Efficient Sensor Nodes", *International Journal of Recent Technology and Engineering.* ISSN: 2277-3878, Vol 08, Issue 01, May 2019, pp. 1085-1090 (**Scopus indexed**)

4. Saji M Antony, S. Indu and Rajeshwari Pandey, "An Efficient Solar Energy Harvesting System for Wireless Sensor Network Nodes", *Journal of Information and Optimization Sciences*, ISSN 0252-2667 Vol 41, Issue 01, February 2020, pp 39-50 **(ESCI).**

Conference Paper

1. Saji. M. Antony, S. Sri Ranjani Prasanthi, S. Indu, and Rajeshwari Pandey, "Design of High Speed Vedic Multiplier Using Multiplexer Based Adder", a paper presented and published in the proceedings of IEEE International Conference on Control, Communication & Computing India (ICCC-2015) held at Collage of Engineering, Trivandrum, during 19-21 November 2015, pp. 448-453.