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VI SEMESTER **B.Tech**

MID SEMESTER EXAMINATION ***MARCH 2019***

EC310 Testing and diagnosis of digital system design

Time: 90 Minutes *Max. Marks : 25*

Note : All questions carry equal marks.
Assume suitable missing data, if any.
All symbols and abbreviations have their usual meanings.

Q.1 [i]A gate level fan-out free realization of a circuit has 20 inputs and 2 outputs. What is the minimum number of tests we will need to test this circuit? (1)

[ii]If a fault f1 dominates fault f2, and the fault f2 dominates a fault f3, which of these faults can be deleted to reduce the fault list for fault detection? Explain why. (2)

[iii] Count the total number of possible single stuck at fault sites in Figure 1. (2)

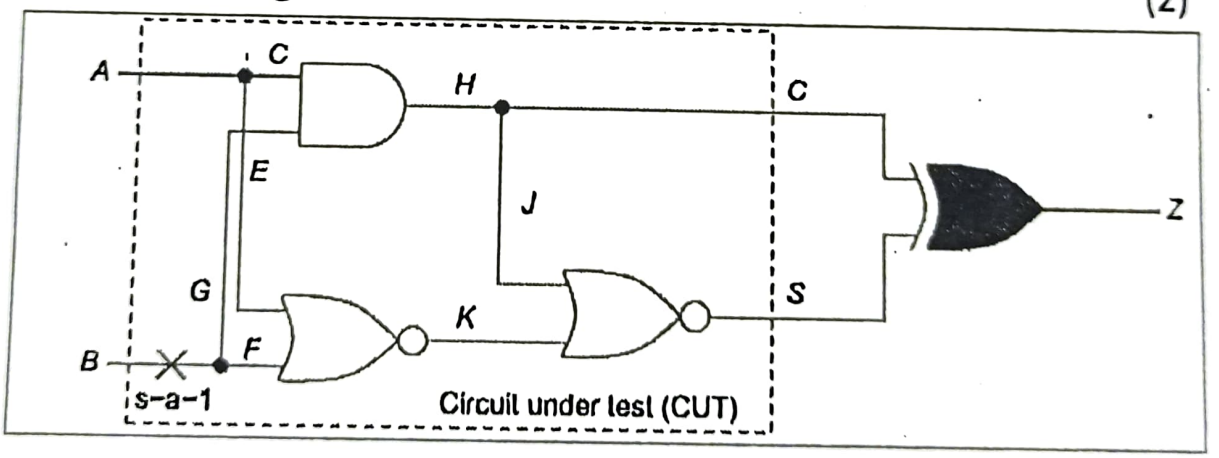

Figure 1

Q.2 **In Figure 2,** use the PODEM algorithm to test for a SA1 on the output of gate 6. Write on the figure and explain the sequence of decisions. (5)

P.T.O.

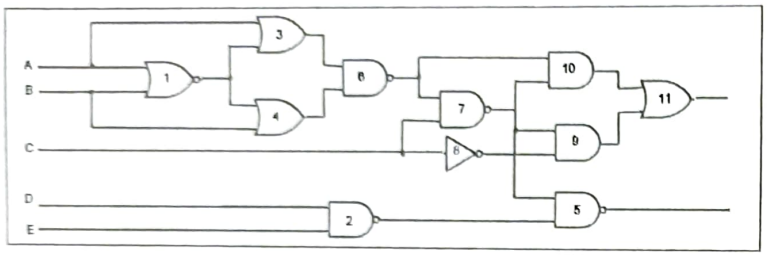

Figure 2

Q.3 [i] Let N be a nonredundant logic circuit that realizes the following Boolean function: $z = (x1 + x'2)(x1 + x'2x'3 + x4x5)' + x1(x2 + x4x5)$. Use the Boolean difference to find all test vectors that detect the SSL fault x1 stuck-at-1 in N. (3)

[ii] In **Figure 2**, determine the collapse ratio after applying equivalent fault collapsing. (2)

Q.4 [i] Write differences between distinguishing sequence and homing sequence. (1)

[ii] For the state table shown in Table 1, draw the distinguishing tree and find the distinguishing sequences. (2)

[iii] For the state table shown in Table 1, draw the homing tree and find all shortest homing sequences. (2)

Table 1

Present State (PS)	Next State (NS), Output(Z)	
	Input X=0	Input X=1
A	C,0	A,1
B	A,1	B,0
C	D,0	B,1
D	B,1	D,0

Q.5 In Figure 3,

[i] Enumerate the minimal set of single stuck-at faults that must be tested according to the Checkpoint Theorem. (3)

[ii] Show that the two faults d s-a-0 and g s-a-1 are equivalent. (2)

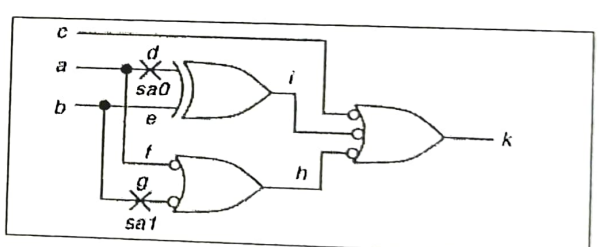

Figure 3

**********END**********

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