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6th SEMESTER B.Tech. [EC]

MID SEMESTER EXAMINATION (March-2019)

EC-302 VLSI DESIGN

Time: 1 1/2 Hours Max. Marks: 20

Note: Answer all questions.
Assume suitable missing data, if any.

1. a) Draw and Explain fabrication steps for twin-tub CMOS process. Aid your answer with suitable diagrams. (3)

   b) An NMOS transistor has threshold voltage on 1V. How would you change threshold voltage to 0.8V and 1.2 V without changing the substrate bias? (C_{ox} = 10 fF/cm^2). (2)

2. a) Explain the limitations imposed by small device geometries. How do scaling affect the doping concentrations and power density if constant voltage scaling is applied to MOS device. Why does V_T increase for a short channel device and show an increasing trend for narrow width device? (3)

   b) Consider an NMOS transistor with the following parameters: t_{ox} = 6 nm, L = 0.24 mm, W = 0.36 mm, drain (L_D) and source (L_S) lengths = 0.625 mm, C_{j0} = 2×10^{-3} F/m^2, C_{jsw0} = 2.75 ′ 10^{-10} F/m. Determine the zero-bias value of all relevant capacitances. (ε_o=8.85 x 10^{-14} F/cm, ε_{ox} = 3.9ε_o and neglect overlap capacitance). (2)

3. a) Design a depletion load inverter with specifications as: V_{DD} = 5V, V_{OL}= 0.2 V, $V_{To,driver}$ = 1V and V_{Tload} = -3V and power consumption of 1mW. Find the widths of driver and load transistor if both transistors have same channel length. (3)

   b) Write down the equations (and only those) which are needed to determine the voltage at node *X in* **Fig. 1**. Do NOT plug in any values yet. Neglect short channel effects and assume that $\lambda p = 0$. Determine the required width of the transistor (for L = 0.25 μm) such that X equals 1.5 V. $k'_p = 30\ \mu$A/V^2, $V_{T0,p} = -0.4$ V. (2)

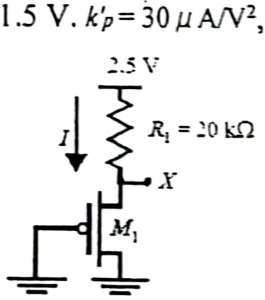

Fig. 1

4. Consider a CMOS inverter that is designed in a process with the following parameters: k_n' = 100μA/V^2, kp' = 40μA/V^2, V_{Ton} = +0.7v and V_{Top} = -0.8v. The transistors have aspect ratios of $(W/L)_n$ = 10 and $(W/L)_p$ = 15 and the power supply is chosen to be 5V. (i) Determine the value of switching threshold voltage. (ii) Compute the time it takes to rise from 1V to 4V when connected with C_{Load} = 0.5pF. (5)