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Mid Term Examination **March 2019**

B.Tech. IV sem (ECE)

Course Code: EC 208 **Subject Name: Computer Architecture**

Time : 1½ Hrs **Maximum Marks: 20**

Note: Answer all questions.

Q1 a A computer uses a memory unit with 256K words of 32 bits each. A binary instruction code is stored in one word of memory. The instruction has four parts: an indirect bit, an operation code, a register code part to specify one of 64 registers, and an address part. 3

a. How many bits are there in the operation code, the register code part, and the address part?

b. Draw the instruction word format and indicate the number of bits in each part.

c. How many bits are there in the data and address inputs of the memory?

b The content of the top of a memory stack is 5320. The content of the stack pointer SP is 3560. A two-word call subroutine instruction is located in memory at address 1120 followed by the address field of 6720 at location 1121. What are the content of PC, SP, and the top of the stack: 3

a. Before the call instruction is fetched from memory?

b. After the call instruction is executed?

c. After the return from subroutine?

Q2 a Write a program to evaluate the arithmetic statement: 6

$X= [A - B + C*(D*E - F)] / [G + H*K]$

a. Using a general register computer with three address instructions.

b. Using a general register computer with two address instructions.

c. Using an accumulator type computer with one address instructions.

b Convert the following arithmetic expressions from infix to reverse Polish notation. 2

a. A*B + C*D + E*F

b. A*B + A*(B*D + C*E)

c. A + B*[C*D + E*(F + G)]

d. A * [B + C * (D + E)] F*(G + H)

Q3 Show the contents in hexadecimal of registers PC, AR, DR, JR, and SC of the basic computer when an ISZ indirect instruction is fetched from memory and executed. The initial content of PC is 7FF. The content of memory at address 7FF is EA9F. The content of memory at address A9F is 0C35. The content of memory at address C35 is FFFF. Give the answer in a table with five columns, one for each register and a row for each timing signal. Show the contents of the registers after the positive transition of each clock pulse. 6

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