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FOURTH SEMESTER **B.Tech. (ECE)**

MID SEMESTER EXAMINATION ***(MARCH-2019)***

EC-204 DIGITAL DESIGN - II

Time: 1.30 Hours ***Max. Marks: 20***

Note: Answer all questions.
Assume suitable missing data, if any.

Q.1 Draw the circuit being represented by the code shown below. **(4)**

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.numeric_std.all;

entity counter is
port(clk : in std_logic;
reset : in std_logic;
count : out std_logic_vector(3 downto 0));
end entity counter;

architecture rtl of counter is
component FFD
port (CLK, D, reset : in STD_LOGIC;
                Q : out STD_LOGIC);
        end component;
signal q0,q1,q2: std_logic:='0';
signal q3: std_logic:='1';
begin
inst1: FFD port map (CLK=>clk, D=>q3, reset=>reset, Q=>q0);
inst2: FFD port map (CLK=>clk, D=>q0, reset=>reset, Q=>q1);
inst3: FFD port map (CLK=>clk, D=>q1, reset=>reset, Q=>q2);
inst4: FFD port map (CLK=>clk, D=>q2, reset=>reset, Q=>q3);
inst5: count<=q3&q2&q1&q0;
end architecture rtl;
```

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P.T.O

Q.2 [a] Find (i) and (ii) for given inputs A, B, C and D. **(3)**

A: in bit_vector (6 to17) := "101101101010";
B: in std_logic_vector (9 down to 0) := "0001011111";
C: in std_logic_vector (2 to 13) := "010001010011";
D: in bit_vector (12 down to 4) := "100010100";

(i) D(D'right-1 to D'left+2) & A(12) & NOT D(7) NOR not (A(A'left+3 to A'right-2)&A(15))

(ii) B & C(11) & B(6) XNOR NOT C(C'right to C'left) NAND C ror3

Q.2 [b] Differentiate between Signal and Variable in VHDL. **(1)**

Q.3 [a] Convert the given Mealy state table to Moore state table. **(2)**

PS	NS/Z	
	X=0	X=1
A	C,1	B,0
B	C,1	E,0
C	B,1	E,0
D	D,0	B,1
E	E,0	A,1

Q.3 [b] Make the state diagram for FSM (Moore) that has an input W and output Z. The machine has to generate Z=1, when the input is 0011 or 1010; otherwise, Z=0. Overlapping input patterns are allowed. **(2)**

P.T.O

Q.4 Reduce the given state table using merger and compatibility graph method. **(4)**

PS	NS/Output			
	Input w_1w_2			
	00	01	11	10
A	-,-	D,0	C,1	F,0
B	A,0	C,0	D,-	-,-
C	E,0	A,0	-,-	E,0
D	-,-	-,-	G,1	C,-
E	C,0	-,-	F,1	-,-
F	D,1	B,0	E,-	-,-
G	E,1	-,-	C,1	A,0

Q.5 Design the circuit for Mealy FSM to obtain 2's complement of a number. **(4)**

-End-