Total No. of Pages 2 FOURTH SEMESTER MIDSEM EXAMINATION Time 1:30 hours Q 1)Define the following terms: a. I/O Ports b. Types of instructions c. Timing and control d. Cache Memory e. Auto increment and decrement mode Q 2) b) a = 1b = 10c = 20

Roll No..... B.TECH (SE) MARCH 2019

SE204 (Computer Architecture and Organization)

Max. Marks:25

Note: Answer all the questions. All Questions carries equal marks Assume suitable missing data .if any

- a) A processor can support a maximum memory of 4GB where the memory is wor addressable (a word=2 bytes). The size of the address bus of the processor is atleast ho
- b) Explain register organization and types of interrupts and exceptions.

a) The value of float type variable is represented using the single precision 32-bit floating point format of IEEE-754 standard that uses 1 bit for sign, 8 bits for biased exponen and 23 bits for mantissa. A float type variable X is assigned the decimal value of -14.2 The representation of X in hexadecimal notation is?

c) The program below uses six temporary variables a, b, c, d, e, f.

d = a + b

e = c+d

f = c + e

b = c + e

e = b+f

d = 5 + e

return d+f

Assuming that all operations take their operands from registers, what is the minimur number of registers Needed to execute this program without spilling? (2.5)

P. T.O.

Q 4) What is direct mapping? What is disadvantage of direct mapping? Consider a machinish a byte addressable main memory of 2²⁰ bytes, block size of 16 bytes and a direct mapped cache having 2¹² cache lines. Let the addresses of two consecutive bytes in mamemory be (E201F)₁₆ and (E2020)₁₆. What are the tag and cache line address (in hex) for main memory address (E201F)₁₆?

Q 5)The frequency of different types of instruction executed by a machine is tabulated below

Addressing Modes	Frequency
Register	30
Immediate	20
Direct ·	22
Memory Indirect	17
Index .	11

Assuming 2 clock cycle are consumed for an operand to be read from the memory, 1 cloc cycle for index arithmetic computation and 0 clock cycle if operand available in register or within the instruction itself. The average operand fetch rate of the machine is? (5)