

**DESIGN AND ANALYSIS OF UNIVERSAL 4-BIT
BARREL SHIFTER USING LOW POWER
MULTIPLEXERS**

A DISSERTATION REPORT
SUBMITTED IN PARTIAL FULFILLMENT OF THE REQUIREMENTS
FOR THE AWARD OF THE DEGREE
OF

MASTER OF TECHNOLOGY
IN
VLSI DESIGN & EMBEDDED SYSTEMS

SUBMITTED BY
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CANDIDATE'S DECLARATION

I, (Nishant Kumar), Roll No. 2K18/VLS/08 student of MTech (VLSI design & Embedded systems), hereby declare that the project Dissertation titled “**Designing of Universal 4-bit Barrel Shifter**” which is submitted by me to the Department of Electronics and Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.



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CERTIFICATE

I hereby certify that the Project Dissertation titled “**Designing of Universal 4-bit Barrel Shifter**” which is submitted by Nishant Kumar 2K18/VLS/08, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfilment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.



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ACKNOWLEDGEMENT

Foremost, I would like to express my sincere gratitude to my mentor **Dr. Poornima Mittal** for helping me on each step of this research, due to her continuous help and support I completed this research. Her patience, motivation, enthusiasm and vast knowledge helped me in all the time of this research and in writing of this dissertation. Without her guidance, I could not have imagined of completing this research. Her suggestions and the way of managing the work were the most important key points, which made my path clear. She helped me use my full potential because of that I tried my best to get the maximum for this project. I am extremely thankful for guiding me throughout the project.

I am thankful to Electronics Department and faculties for helping me, and also thankful to my friends who helped me directly and indirectly in my research.



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M.Tech: VLSI Design and Embedded System

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ABSTRACT

This report highlights a comparative analysis of eight diverse techniques for 2×1 multiplexer. The functionality is similar but diversity achieved in terms of dynamic power consumption, delay and power delay product. Thereby enabling the designer to pick out the best fit technique for a specific application in keeping with their design requirement. The techniques that have been analysed are TG, GDI, PT, MSL, Static CMOS, CPL, CVSL and MTCMOS CVSL. For power application, GDI based multiplexer is the best suit as it reports minimum power consumption of 1.72 fW. While PT based technique has holistic power dissipation as the maximum and minimum power consumption is moderate at 198.53 nW and 0.2196 nW respectively. It also has least average power dissipation of 110.9 nW. If the timing plays a more crucial role for an application, then GDI is the fastest of all. It has the least input to output transmission time of 1.65 ps. While the power delay product is best for PT at 0.395 aJ. In terms of static power dissipation, the best performance is demonstrated by GDI based technique at 0.2199 nW. The multiplexers are designed at 90 nm technology node and simulated at supply voltage of 1 V.

FinFET device is one of the most advance devices by which any logic circuit can be designed and will give better performance compare to MOSFET. Comparison is completed between MOSFET and FinFET based multiplexers and analysis of delay and power. Switching and scaling is also an important factor by which analyses of devices can be done. Switching of the signals causes the changes in the overall power dissipation. If signal is switching at same time instance power dissipation will be more and if switching at different time instance power dissipation will be less. Devices are getting smaller in size, using of same power supply will lead to more power consumption. Scaling of power supply will improve the overall performance of the device. MOSFET is analysed at 1V, 0.8V, 0.6V and FinFET is analysed at 0.8V, 0.6V, 0.4V. The designing and simulation are done using MOSFET at 90nm technology node and by using FinFET at 10 nm technology on cadence virtuoso.

A comparison is made between FINFET based Gate Diffusion Input (GDI) and Pass Transistor (PT) based 2:1 Multiplexers in terms of delay, average power dissipation, and Power delay product (PDP). Both the multiplexers are designed using an 10nm technology node and functional at 0.8V supply voltage. GDI based mux consumes very less power dissipation of 839.3nW, which is 88.08% lesser than the PT based Mux. If the user requirement is of fast operation than GDI based Mux meets the criteria. It takes 0.0107ps to pass the signal at the

output, which is 165.42 times faster than PT based Mux. PDP of GDI and PT based Mux is 0.00029aJ and 0.1aJ. Additionally, GDI based Mux demonstrates better performance with 3.15nW power dissipation. The multiplexers can be used in many combinational circuits, therefore, if the performance of the multiplexer is improved, the complete circuit is bound to give better performance.

Finally, GDI and PT techniques are used to design barrel shifters for MOSFET as well as FinFET technology. Using FinFET based technology designing of barrel shifter is achieved, in both Barrel Shifter GDI based Barrel shifter shows the better performance, maximum power dissipation of GDI based barrel shifter is 468.5nW which is 13.85 times less than PT based barrel shifter. Whereas minimum power dissipation is 154.48nW. GDI based barrel shifter takes 47.27ps to pass the input to the output, it is 15.23ps less compare to PT based barrel shifter. Analysis states that GDI based Universal Barrel Shifter shows the better performance.

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LIST OF ABBREVIATIONS

TG- Transmission Gate

GDI- Gate Diffusion Input

PTL- Pass Transistor Logic

MSL- Multiplexer Single with Level Restoration

CPL- Complementary Pass Transistor Logic

CVSL- Cascode Voltage Switch Logic

MD- Multiplexer Double

MDL- Multiplexer Double with Level Restoration

DCVSL- Differential Cascode Voltage Switch Logic

CNTFET- Carbon Nano Tube Field Effect Transistor

SISO- Serial in Serial Out

SIPO- Serial in Parallel Out

PISO- Parallel in Serial Out

PIPO- Parallel in Parallel Out

PDP- Power Delay Product

CHAPTER-1

INTRODUCTION

1.1 INTRODUCTION

Combination logic is an integral part of digital circuit design. It is implemented using Boolean circuits where the output is exclusively dependent on the present state of input combination. Whereas in case of sequential circuits the output is dependent on the present inputs and the history of inputs. To store the pervious input combinations a sequential logic circuit needs a memory element while combinational logic circuit does not rely on the memory unit. Over the past decades, scaling of CMOS technology has been driving the electronics industries and providing a path for complex and faster integration. As the size of the transistor is decreasing, IC's getting more complex and denser. Power consumption for integrated-circuits (ICs) has always been an important factor. Voltage down-scaling technique has been quite helpful in bring down the power consumption of ICs. For some applications, such as medical devices, portable wireless devices, and sensor network nodes, if power supply is reduced just higher than the threshold voltage, results the reduction in power [1][2][3]. The necessity for low power devices has caused a significant effect on Daily life, whereas the power dissipation has become the important factor to improve the performance [2].

2×1 Mux is an elementary unit of the “switch logic”. The principle of switch logic is to implement the logic circuits as a combination of switches, rather than as a logic gate. Multiplexers are used as programmable logic machines, in telecommunications, in computer networks, and in digital video, in digital semiconductors also in CPUs and graphics controllers. Often named Multiplexer as data selector. A multiplexer is a hybrid circuit that selects and directs binary information from one to several input lines to a single output line [1]. 2×1 multiplexer circuit has one output, two inputs and one input selection. The selection of particular input line is controlled by a set of selection lines as illustrated in Fig. 1. The line of selection decides which bit of the input is transmitted to the output.

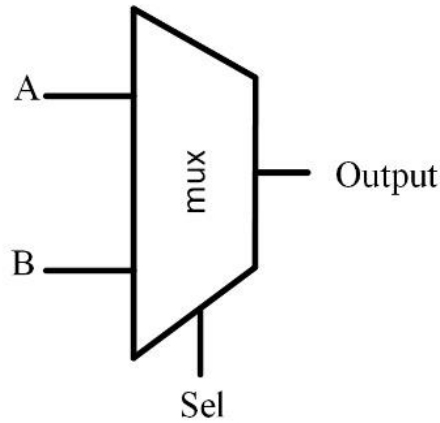


Fig. 1.1. Schematic of 2:1 Multiplexer.

Through advancements in large-scale automation, millions of transistors can be placed on a single chip for robust circuitry implementation. It depends on Moore's law however, According to the Moore's law the number of transistors on IC has doubled at every two years [2] As a consequence of having too many transistors in such a limited room, significant heat dissipation and power consumption issues have been introduced into the picture. Work to address these problems was done [3]. Solutions have been suggested to decrease transistor power supply voltage, switching frequency and capacitance reliant on the usage, the type of circuit to be applied, and the design methodology used, different performance considerations become relevant, disallowing the formulation of uniform rules for optimum logic types. In [4] author have analysed the different techniques of multiplexers circuits for low power applications, Analysis of GDI based Mux is performed by the author in [6]. CPL based Design is illustrated in [7] with their power analysis. In [11] author have designed and analysed the different pass transistor-based circuits.

In view of optimize the performance of 2×1 Mux, here different configurations including GDI (Gate Diffusion input), PT (Pass Transistor), MSL (Multiplexer single with level Restoration), TG (Transmission), Static CMOS, CPL (Complementary Pass Logic), CVSL (Cascode Voltage Switch Logic) and MTCMOS CVSL (Multi Threshold CMOS CVSL) are designed using MOSFET at 90 nm technology node. Further, their performance is analysed and compared by means of output response and dynamic power dissipation using Cadence virtuoso software. Additionally, power and delay are also analysed to find the best mux amongst all the configurations. After that designing of Universal 4-bit barrel shifter is done by using best performance 2×1 multiplexer.

1.2 MOTIVATION:

Due to the scaling of the device, dissipation of the energy has improved very significantly with new technology node, because there are billions of transistors are integrated on the chip. So, the power dissipation factor is important to consider the device efficient. One of the significant reasons behind the extensive usage of this barrel shifter is, it can perform multiple bit shifting operation in a single cycle. Further, area of this barrel shifter is small, so this barrel shifter demonstrates the optimum performance.

Barrel shifter is often used in many devices and designs like microprocessors, ARM processors, Digital signal processing, ALU, and many others. Fast Barrel shifter increases the performance of devices, so desired barrel shifter with optimum performance is required. Barrel shifter is a digital circuit to shift data by specific number of bits. It can shift n-bit data in a single cycle. N-bit Barrel Shifter can perform any shifting operation like right shift, left shift, rotate by N-1bits. The old version of shifter is shift register, these shift registers are SISO, SIPO, PISO and PIPO in which right, left and rotation operation is possible but requires more than one cycle to perform the operation. Further research is conducted to design the efficient barrel Shifter, which can perform shifting operation with a smaller number of cycles. Unidirectional shifter came out after shift register, which can shift the data bus using single cycle, but it is not able to perform shifting operation in both left and right direction. For bidirectional shifting operation new design is constructed, this can perform the shifting operation in both left and right direction. Designing of these shifters is done using MOSFET with different technology node after that FinFET is used to increase the performance and speed of the design and also requires less area compared to MOSFET. This motivates me to design barrel shifter, which gives better performance in terms of delay, area and power. In this thesis barrel shifter is designed using FinFET at 10nm technology node.

1.3 OBJECTIVE OF WORK:

Aim of this thesis is to design and simulate different 2x1 multiplexer using MOSFET at 90nm technology node, further analysis of delay and power is done, which gives the best performance multiplexer. After that best multiplexers are designed using FinFET to analyse the performance which further will be used for designing of Universal 4-bit barrel shifter using FinFET at 10nm technology node.

- Designing of different multiplexers is done using MOSFET at 90nm technology node, with their delay and power analysis. This analysis helps us to understand each aspect of the multiplexers design by which we can understand which multiplexer is showing better performance and why.
- When device is in stable condition it should not or dissipate less power compare to the condition when inputs are changing, this analysis is also done to find out which multiplexer dissipates minimal power. Switching is also another factor by which variation of power dissipation at different switching is analysed.
- After designing of different multiplexer using MOSFET at 90nm technology node, some of the multiplexer which demonstrates better performance in terms of delay and power are constructed using FinFET at 18nm technology node.
- Multiplexer which shows better performance designed using MOSFET and FinFET is used to construct the universal 4-bit barrel shifter. Further delay and power analysis is done.

1.4 ORGANIZATION OF REPORT:

This report has been organized into 7 chapters. Chapter 1 deals with the introduction of different multiplexers, it also includes the Motivation and aim of the report. Chapter 2 is about the previous work on designs and technical gap. Chapter 3 is related to the Schematic diversity and delay & power dissipation analysis of different multiplexers. Chapter 4 illustrates the static power dissipation and effect of switching on power dissipation. Designing and analysis of FinFET based multiplexers are done in Chapter 5, further delay and power analysis is also done in this section. Main aim of this report is to design the optimum universal barrel shifter using best performance multiplexer is illustrated in Chapter 6. Chapter 7 is about the conclusion and future scope.

- Chapter 1- Introduction of the design and operation of basic multiplexer is done with Motivation, Aim and organization of the report is illustrated in this chapter.
- Chapter 2- This chapter explains the previous work done on multiplexer and barrel shifter. SISO, SIPO, PISO and PIPO are the shift registers, which uses more than one cycle to shift and rotate the data, increases the power dissipation. After, Further research designing of unidirectional shifter is done, requires only one cycle to shift and rotate the data but its limited to the single direction either left or right. Unidirectional barrel

shifter can perform the shifting and rotating operation in both left or right direction using single clock

- Chapter 3- Designing of TG, GDI, PT, MSL, Static CMOS, CPL, CVSL and MTCMOS CVSL based multiplexer is done. Further, delay and power analysis are also done to find the finest multiplexer in terms of delay and power.
- Chapter 4- Static power dissipation is an important factor, which gives the information about the power dissipation when all the inputs are static. This chapter explains the static power dissipation of all the multiplexers. Variation in the switching of the input signals shows variation in power dissipation, if switching is occurring at the same time power dissipation will be more and if switching is at the different time then there will be less power dissipation. This chapter also illustrates the power dissipation of the multiplexer at different switching.
- Chapter 5- This chapter illustrates the design of PT and GDI based multiplexer, these both multiplexers shows finest performance when designing with MOSFET, so designing of these multiplexers with FinFET will increase the performance of multiplexer. Further, delay and power analysis are also accomplished.
- Chapter 6- Purpose of this report is to design the best performance universal 4-bit barrel shifter. This is done by improving the basic element of barrel shifter which is 2x1 multiplexer. In previous chapters different type of multiplexer have analysed in terms of delay and power, where two of them PT and GDI based multiplexers shows better performance. These two optimum multiplexers are further used in universal 4-bit barrel shifter. Designing and analysis of barrel shifter using MOSFET and FinFET is achieved in this chapter.
- Chapter 7- Conclusion of this report and future scope of this barrel shifter explained in this chapter

In the last of this report references are mentioned, which helped me a lot to complete my thesis and improved my knowledge in this domain.

CHAPTER II

LITERATURE REVIEW

2.1 PREVIOUS REPORTED WORK:

This section illustrates the work done on the multiplexers using MOSFET and FinFET. It also exemplifies the barrel shifter.

R. Avudaiammam, A. Rode V and D. Devi S [1], In this paper author designed and explained different 2x1 multiplexers using MOSFET at 180nm technology node. Various logic families are used to design multiplexers such as Pseudo NMOS logic, Static CMOS logic, Domino Logic and dual rail domino. Delay and power analysis of these multiplexers illustrates that Domino logic-based mux is the most efficient design because it shows 20.06% average power dissipation and 20.1% power delay product less than other techniques.

Z. Yan, W. Zhigong and L. Wei [5], have proposed the design of 80Gb/p 2x1 multiplexer using BICMOS at 130nm technology node. In this paper analysis and design multiplexer is done, this analysis shows that performance speed of this multiplexer is fast and can drive a high load of 50 Ω load. Working frequency of this design is 106GHz, Analysis demonstrates that it provides the highest data rate.

Z. Changchun, W. Zhigong, S. Shi and M. Peng [6], In this paper author presents the 5 Gb/s half rate multiplexer using MOSFET at 180nm technology node. Supply voltage used to analyse the design is 1.8V. In this design total power consumption is 70mW, where mux can work appropriately without any external clock because of CE (Clock Extraction).

M. Vyas, S. K. Manna, S. Akashe [7], this paper presents the design and simulation of different 2x1 multiplexers and comparison with the conventional multiplexer. Designing is done using FinFET at 45nm technology node and some designing is done using 120nm technology node to attain the operational speed of 34Gb/s with 0.7V power supply. Using of FinFET for multiplexer reduced some parameters like, dynamic power dissipation and leakage while increasing the performance of the design. Noise of the circuit is reduced about 60% whereas power dissipation and leakage are 40% and 50% respectively. So, designing of mux using FinFET provide the efficient and better performance compare to CMOS.

V. K. Agrawal, M. Guduri, A. Islam [8], have proposed the design and comparison of Static CMOS, CVSL, CPL, EEPL, SRPL and TG based multiplexers using FinFET at 16nm

technology node. Author has done the delay and power analysis of different multiplexers, this analysis states that CMOSTG multiplexer shows the better performance. Therefore, designing of this CMOSTG mux is done using CNFET. Designing of multiplexer using CNFET further reduced the power and leakage of the circuit. For CMOSTG average power dissipation is 17.97pW and for CNFET it is 7.67pW, which is 57.31% less than CMOSTG based mux.

A. Morgenshtein, V. Yuzhaninov, A. Kovshilovsky, A. Fish [9], in this paper analysis of low power CLA adder is done using GDI (Gate Diffusion Logic) at 40nm technology node. Simulation results shows the twice in area reduction and 5 times improvement in the dynamic power dissipation and 4 times decrement in the leakage with only 24% degradation in the performance. GDI cell consumes very less area because of less number of transistor used, less transistor leads to less switching which causes less power dissipation compare the other logic.

A. Morgenshtein, A. Fish, I. A. Wagner [10], this paper completely based on the basic of GDI cell and its performance and how many operations this cell can performance. Author analysed the various logic functions of GDI cell for different input. GDI cell only uses two transistors and which can perform AND, OR, NOT, Mux and other functions also. Comparing with TG logic, 45% reduction is achieved in GDI cell. So, any complex CMOS design can be implemented using GDI cell with less delay, area and power dissipation.

K. Yano, T. Yamanaka, T. Nishida, M. Saito, K. Shimohigashi, A. Shimizu [11], In this paper author proposed the CMOS based 16x16-b multiplier using CPL (Complementary Pass-Transistor Logic) at 4v power supply. CPL is twice as fast as compared to conventional CMOS and this can be improved further to 2.6ns using 60mW. Total power consumption in CPL very less compare to CMOS due to less input capacitances.

J.H. Pasternak, A. S. Shubat, C. A. T. Salama [12], This paper illustrates the design and analysis of CMOS differential pass-transistor logic (DPTL). By using this logic technique designing of any circuit offers better area efficiency, higher operating speed, less power dissipation and designing of circuits is simple compare to conventional PT logic. Sequential circuits can also take benefits from this DPTL logic. Possibility of programming of these pass arrays is less in proposed layout technique.

M. Suzuki, N. Ohkubo, T. Yamanaka, A. Shimizu, K. Sasaki [13], Author has proposed the circuit techniques for a high-speed adder using Pass- Transistor logic. DPL (Double Pass-Transistor) logic is used to improve the performance of the design with less usage of power supply voltage. It improves the gate speed without increasing of the input capacitance. By using

this technique time taken by the addition in 32-b ALU can be reduced by 30% compare to the conventional CMOS based ALU. Designing of this ALU is done at 250nm technology node at 2.5V supply voltage and it is capable of adding data in 1.5ns.

K. Yano, Y. Sasaki, K. Rikino, K. Seki [14], In this paper author proposed the design and analysis of Pass-Transistor logic. To clarify the potential of PT logic, construction of PT based cell library and synthesis tool are done. This method is called LEAP (Lean Integration with Pass-Transistor). Comparison is done between the, very simple cell library which have only 7 cells combined with synthesis tool named as “Circuit inventor” with the conventional CMOS library which includes more than 60 cells, combined with state-of-the-art logic synthesis. Result of this analysis states that area, power and delay all are improved by using this LEAP method and value cost ratio is also improved. Autor also have found that at low voltage supply nMOS based Pass transistor logic shows the better performance in comparison conventional CMOS circuits at 1V.

B.P. Singh, N. Arora, I. Gupta [15], This paper based in the, design, simulation and analysis of 2x1 multiplexer at 90nm technology node using Tanner EDA Tool. There comparative analysis with other multiplexer is done in terms of power, operating frequency, supply voltage, area and load capacitances. Different 2x1 multiplexers are NMOS based, CMOS, MSL (Multiplexer single with level restoration), MD (Multiplexer Double), MDL (Multiplexer double with level restoration), DCVSL (Differential Cascode Voltage Switch Logic), MDCVSL based multiplexers. Result of the complete analysis of multiplexers is that MDCVSL based multiplexer demonstrations the less power dissipation, output load capacitance and delay is also less. NMOS circuit reveals the better operating frequency, whereas MDCVSL shows the smallest amount of PDP (Power Delay Product).

A. Pahadia, U. R. Bhatt, V. Bhat [16], This paper illustrates the review on high performance multiplexers. Analysis of different 2x1 multiplexer is done using Tanner EDA tool and designing and analysis of the improved multiplexer is also done at microwind 3.5 version tool. Analysed multiplexers are NMOS CPL logic, CMOS, MSL, MD, MDL, DCVSL and MDCVSL based multiplexers. After analysing of all these multiplexers, it is concluded that MDCVSL shows the better performance in terms of dynamic and static power dissipation.

I. Hussain, A. Sing, S. Chaudhary [17], Aim of this paper is to design and analyse the CPL (Complementary Pass Transistor Logic) using both CMOS and CNTFET model at 90nm and 32nm technology for CMOS and 32nm technology node for CNTFET. In this analysis shows

that CMOS logic style performs better operation compare to Bulk-Si MOS technology. In CNTFET technology some basic gates such as NOR, NAND and Mux, for this CMOS logic style performs the better operation than CPL logic style. Another observation is that while scaling down the Bulk-Si MOS technology, overall performance of the design starts degrading and leakage is also increased which leads to more power consumption. This analysis states that CNTFET is better than other technology because static power dissipation and leakage is very less and area consideration is also very minimum.

K. Mishra, S. Akashe [18], Focus of this paper is to improve the performance and reduce area and power consumption of the 2x1 multiplexers. Different configurations are used are designed using diverse technology methods such as CMOS, TG (Transmission Gate), PT (Pass Transistor) using FinFET based. Several analyses are done such as leakage power, leakage current, operating power, operating current, optimum power, optimum current and delay atnm technology node with 0.7 supply voltage. All the analysis is done at different temp 10, 27 and 50 degree Celsius. After taking consideration of CMOS based mux and PT based Mux, in both of them pass transistor-based mux provides the better performance in terms of area, power and performance. It also shows the high-performance speed with less static power dissipation.

P. Mandal, S. Malani, Y. Gudepkar, S. Singhi, P. M. Palsodkar [23], have proposed the design of barrel shifter using 2x1 multiplexer and its VLSI implimentstion. In this paper four module have been designed which are, CMOS inverter, CMOS AND Gate, CMOS 2x1 mux and CMOS 4x1 mux. These all modules are used to design the barrel shifter, by which 4bit and 8bit barrel shifter can be designed.

S. Kotiyal, H. Thapliyal, N. Ranganathan [24], have designed the barrel shifter using Fredkin gate which can perform both shift and rotating operation. Barrel shifter which can perform both shifting and rotation is very for computational purpose. In this paper proposed design consist of both reversible Fredkin and Feynman gates to design barrel shifter, where Fredkin gate is used to design the reversible logical and arithmetic barrel shifter, while Feynman gate is used to evade the fanout because fanout is not acceptable in reversible logic.

J. H. Saho, N. K. Rout [25], This paper illustrates the comparative study of low power barrel shifter and rotator at 45nm technology node. In this paper initially barrel shifter and rotator is designed using CMOS logic and then different low power circuit is also used using cadence virtuoso tool. Used low power techniques to improve the design of barrel shifter are PTL (Pass Transistor Logic), LECTOR technique and DFAL Logic, where proposed design is Double

gate DFAL logic. Analysis shows that proposed design shows the better and efficient performance in terms of delay and power in comparison to other techniques at 0.8, 0.7 and 0.6V.

S. Devamane, A. Hanchate, U. Vagare, S. Ujagare, P. Teggelli [26], have designed and analysed the FPGA based barrel shifter. In this paper the author has proposed the 8-bit and 16-bit barrel shifter and designing and analysis is done using Verilog code. Designing of barrel shifter is done using multiplexer which can perform the right shift and right rotate operation at single clock.

R. Pappachan, V. Vijayakumar, T. Ravi, V. Kannan [27], have proposed the design of 4-bit low power barrel shifter at 20nm FinFET technology node. This barrel shifter can perform the both shifting and rotating operation such as, SRL (Shift Right Logical), SRA (Shift Right Arithmetic), RR (Rotate Right), SLL (Shift Left Logical), SLA (Shift Left Arithmetic) and RL (Rotate Left). Analysis of this FinFET based universal barrel shifter states that, FinFET based barrel shifter outperform the MOSFET based barrel shifter in terms of all three factors area, power and delay. So, designing of FinFET based barrel shifter performs the better performance.

2.2 TECHNICAL GAP

After analysing each points and factors in the previous researches and papers, there was a technical gap in the work. All the research was done on universal barrel shifter using MOSFET based technology which can be further improved by using the FinFET model at 10nm based technology node. Using MOSFET it increases the use of power and also requires more area to fabricate, whereas FinFET consumes very less power and requires minimal area in comparison to MOSFET. In terms of dynamic and static power dissipation FinFET dissipates many times lesser than MOSFET and the performance speed is also much faster than MOSFET.

Choosing FinFET over MOSFET improves the overall performance of the universal barrel shifter, which also overcomes all the short channel effects which occurs in the MOSFET while scaling down.

CHAPTER III

SCHEMATIC DIVERSITY OF MULTIPLEXERS

3.1 DIFFERENT MULTIPLEXERS

Multiplexers are defined as the data selectors in which large numbers of inputs are produced at the single output terminal on the basis of their respective turn, which is decided through selection line. In this section, different types of 2×1 multiplexer are designed and analysed. These multiplexers are different by means of structural configuration, delay, power dissipation and area. Some designs depict lesser area that too with low power dissipation but a degradation in output is observed. On the contrary, some designs are liable for non-degraded output but consumes more power and larger delay, as well. The schematic designs of different multiplexers are discussed in subsequent subsections.

3.1.1 TG Based Multiplexer

Transmission gate logic is designed using two pairs of NMOS and PMOS transistors (TG1 and TG2) wherein, the source and drain terminals of transistors are connected in parallel, as illustrated in Fig. 2. Additionally, the gate terminals of PMOS and NMOS are connected at input and output terminals of an inverter in TG1 and the connections are reversed in TG2 [7]. Both NMOS and PMOS permit the same input simultaneously and thus it is transferred at the output node through this transmission gate without any deterioration.

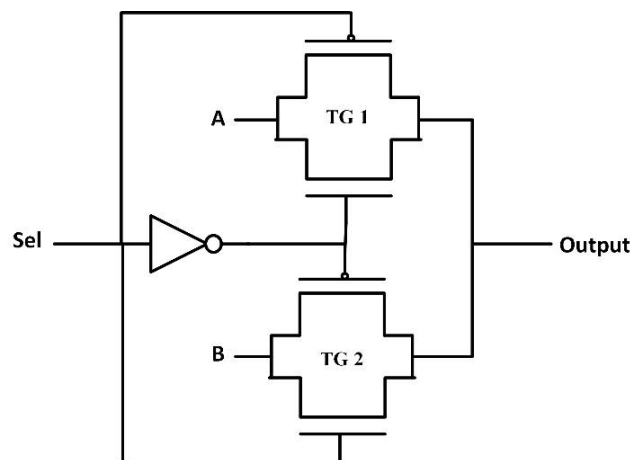


Fig. 3.1. Schematic of TG based Multiplexer

At high input signal, the NMOS gives a weak 1 at the output, however, PMOS provides a strong 1 at the same time. Similarly, at low input, the PMOS produces a weak 0 but NMOS a strong 0 at the output. This is a conventional 2×1 Mux, where total 6 transistors are used; 4 for two transmission gates and 2 for inverter. The gates; TG1 and TG2 are used to pass the input signal A and B, respectively. While Select signal; Sel is kept high, both PMOS and NMOS of TG1 remain OFF. On the contrary, the TG2 section is ON and thus the input signal B reaches at the output. The case is reversed at Sel = 0 and signal A is passed at the output terminal. Use of TG is not limited to multiplexer only; this is used as the basic building block for designing of logic circuits as it can isolate the components and signals/data from being transmitted to the other nodes without using any other hardware.

3.1.2 GDI Based Multiplexer

Gate Diffusion Input logic allows the user to design complex logic circuits using a smaller number of transistors. This is an appropriate technique for designing of fast and low power circuits using lesser number of transistors, as compared to CMOS and PTL techniques. The basic GDI cell is shown in Fig. 3, which resembles a CMOS inverter at first glance. Nevertheless, it is different in terms of accessing the inputs, which are applied at the coupled gate terminal (Sel signal) and source terminals of two transistors (inputs A and B) [8-9]. If Sel is 1, the NMOS transistor operates in ON mode and input signal B will pass to the output. On the other side, output receives the input signal A, when Sel is maintained at 0.

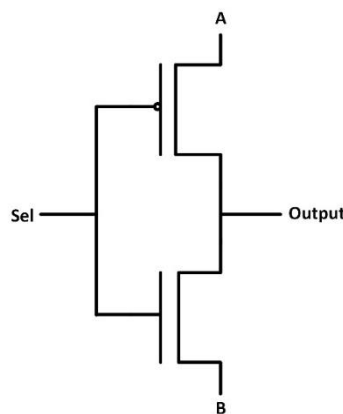


Fig. 3.2. Schematic of GDI based Multiplexer

Logic functions corresponding to various input combinations for GDI cell are summarised in Table 1. Several advantages associated with GDI technique are minimal transistors requirement, low power dissipation and fast operation. However, some limitations are also exhibited - (1) If A is equal to 0, then PMOS being a weak 0 will not pass a perfect 0 at the output, (2) The complementary is applicable for $B = 1$, as NMOS is weak 1. The major advantage that GDI has over other techniques is its low area requirement for implementation.

Table 3.1. Various Logic Functions of GDI Cell for Different Input Combinations.

Inputs		Selection input	Output	Function
A	B	Sel		
0	Q	P	$P'Q$	F1
Q	1	P	$P'+Q$	F2
1	Q	P	$P+Q$	OR
Q	0	P	PQ	AND
R	Q	P	$P'Q+PR$	MUX
0	1	P	P'	NOT

3.1.3 PT Based Multiplexer

Pass Transistor Logic (PTL) uses two NMOS transistors in pass transistor configuration. The inputs are connected at the sources of the NMOS. The drain ends are shorted and the output is sensed at the drain end. The gates of the two NMOS are controlled using select signal, Sel and complement of Sel [10-11]. This logic is different from CMOS design as the source side of logic network is connected to the input signal instead of power supply [12-13]. The schematic for the same is depicted in Fig. 4.

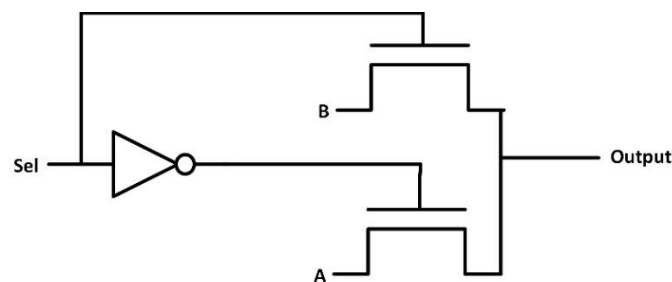


Fig. 3.3. Schematic of PT Based Multiplexer

When the Sel signal is low; then the lower NMOS is in ON state that leads the value at A to be appears at the output terminal. Whereas, when Sel signal is high the value at B gets passed to the output. The upsides to PTL are high speed, low power consumption and low interconnect effect. But the factors that limit the use of PTL technique are slow operation and reduced voltage swing owing to the inability of NMOS to pass a strong 1. Therefore, at conditions such as, Sel=1 and B=1 or Sel=0 and A=1, the output is obtained as a weak 1. Transmission Gate logic can be used to implement a wide range of functions using lesser transistors.

3.1.4 MSL Based Multiplexer

MSL based multiplexer is an improved version of PT based multiplexer. In this design, additional to the PT based multiplexer configuration a PMOS transistor is used to restore the output level. The gate of the PMOS is driven by an inverter controlled by the output of the PT based mux [14]. The gate and drain of PMOS are connected to the output and input of the second inverter, respectively as indicated in the Fig. 5. Similarly, gate terminals of both NMOS transistors are connected to the input and the output of the first inverter.

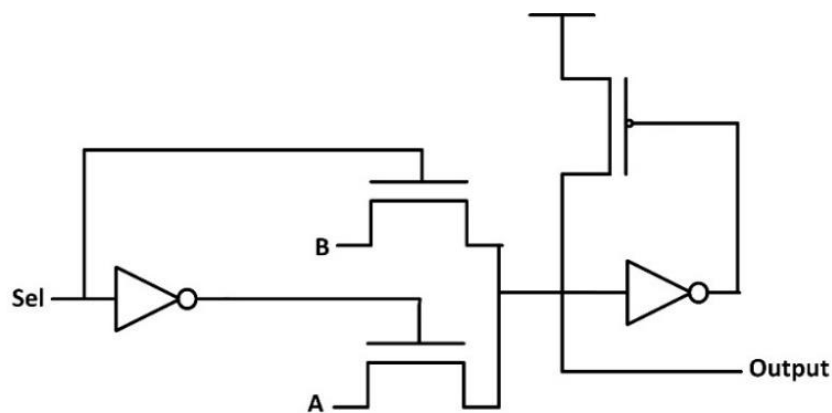


Fig. 3.4. Schematic of MSL Based Multiplexer

The purpose of designing MSL based mux is that it overcomes the major drawback of output deterioration in PT based multiplexer by using an inverter and a PMOS. When Sel is high and B = 1, the NMOS produces a weak 1 as has been explained in the previous subsection. To rectify the same MSL based mux converts the 1 to 0 through the inverter. This inverter then drives the PMOS to ON state, thereby making the output signal a strong 1. It also shows other advantages such as, fast operation and maximum output swing (nearly V_{DD} and 0). Also,

complemented input is not needed in this design. However, as it consists of more transistors in comparison to PT based design, it shows greater power dissipation and lower speed.

3.1.5 Static CMOS Based Multiplexer

Static CMOS based mux uses eight transistors, wherein four PMOS transistors forms the pull up network and the other four NMOS transistors form the pull-down network. An inverter is used to get the actual output, as illustrated in Fig. 6 [15]. When S is low and B = 0 or SB = 1 and A=1/0, the MP2, MP4, MN2 are ON and MN1, MN3, MP1 are OFF thus output becomes 0. There is some leakage due to MN2 and MN4 of pull-down network. Similar observations are achieved for SB=B=1 or S=0 and A=0/1 wherein, MP2, MN2, MN3 remain ON and MN1, MP1, MP4 are OFF thus input of the inverter gets connected to the ground through pull down network and 1 is produced at the output. This operation also shows some leakage because of MP1 and MP4 transistors in pull up network.

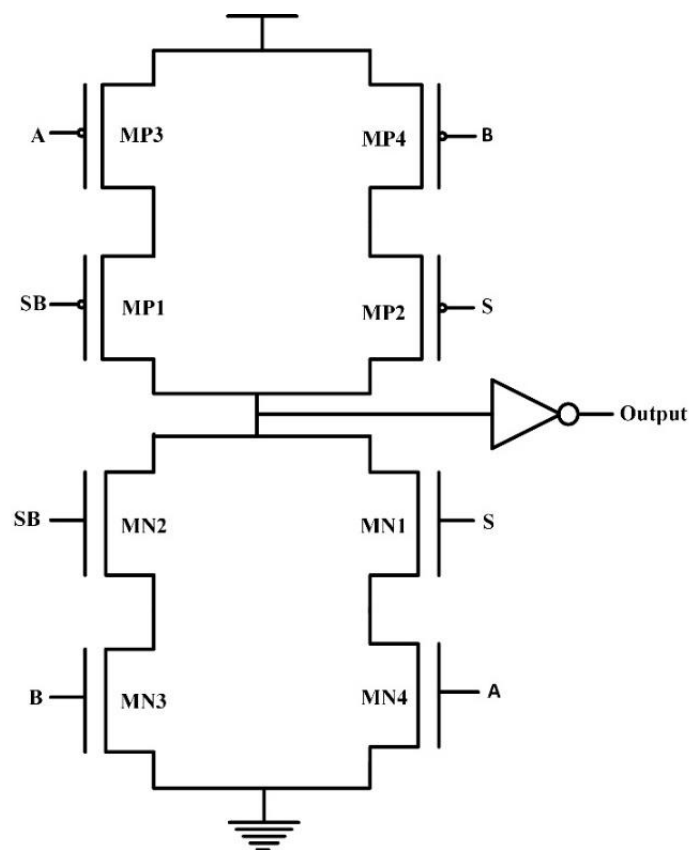


Fig. 3.5. Schematic of static CMOS based Multiplexer

Further, when S is high and A = 1 or SB = 0 and B=0/1, the transistors MN1, MN4, MP1 remain in ON condition and MN2, MP2, MP3 are in OFF. Consequently, the input of inverter

and passes input signal A, AB (complement of input A) respectively. With similar condition When $A=0$ ($AB=1$), then MP2 is ON and V_{DC} gets connected to the output of MN4 and restores the logic level 1 thus makes the 0 at the output, however if $A=1$ ($AB=0$) then MP1 switches ON and output of MN1 gets connected to V_{DC} as a result restores the logic level 1 thus gets the 0 at the outputB. This technique exhibits advantages like presence of both inverting and non-inverting logics at the output, fast operation and restoration of output level. But its high-power dissipation and larger circuit size serve as limiting elements.

3.1.7 CVSL Based Multiplexer

Cascode Voltage Switch Logic (CVSL) refers to a CMOS-type logic family. The logic function and its inverse are simultaneously implemented in this technique. The NMOS logic forms the pull-down network and generates the complementary logic. CVSL can be divided into two parts: a differential latching circuit and a cascaded complementary logic array. Therefore, this logic family is also acknowledged as Differential Cascode Voltage Switch Logic (DCVS or DCVSL) [14-15]. The schematic for 2×1 mux using this technique is illustrated in Fig. 8. As can be seen from the schematic a total of ten transistors are used, wherein, 4-4 NMOS transistors are used for input-select signals and one pair of PMOS is kept to restore the output logic level.

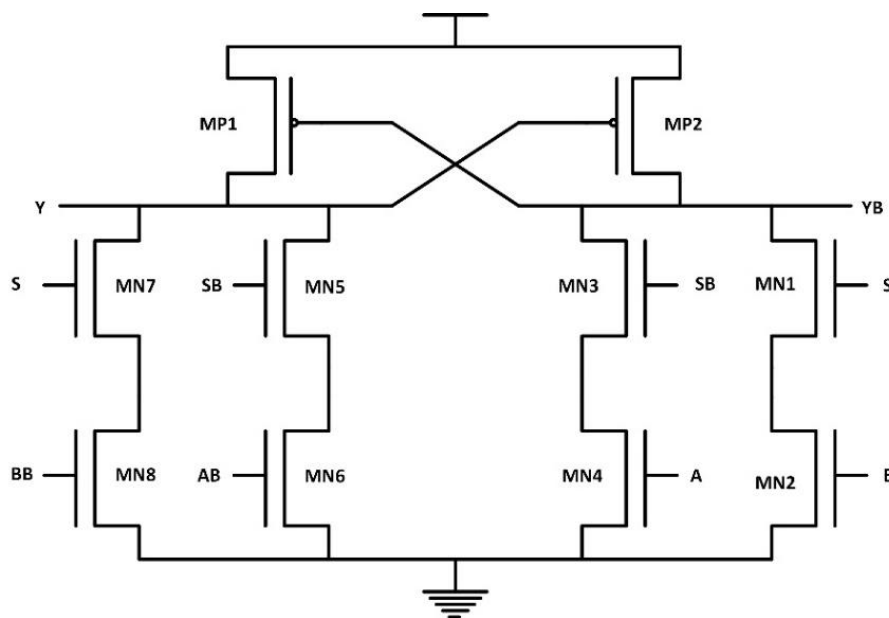


Fig. 3.7. Schematic of CVSL based Multiplexer

When S is low and A= 0, transistor MN3, MN5 and MN6 are ON, henceforth, the output Y and gate of MP2 gets connected to the ground terminal through transistor MN5 and MN6. Thus, the output obtained at Y is 0 (YB = 1). While, for S = 0 and A= 1, transistor MN3, MN4 and MN5 are ON and the ground gets connected to the output; YB through MN3 and MN4. Thereby making the output YB = 0 and Y = 1 as it gets connected to V_{DC} owing to the ON state of MP1. Similarly, while S is high and B = 0 transistor MN1, MN7 and MN8 turn ON and output Y and YB are obtained as 0 and 1 respectively. This configuration exhibits an advantage of elimination of large PMOS from each logic function leading to a significant area reduction.

3.1.8 MTCMOS CVSL Based Multiplexer

The functionality of multi threshold CMOS cascode voltage switch logic (MTCMOS CVSL) based mux is similar to the CVSL based mux. This technique is used to reduce the leakage in the circuit in static condition. In this configuration, one pair of PMOS-NMOS is used, wherein, PMOS isolates the logic circuit from V_{DC} and NMOS isolates the ground, as shown in Fig. 9. MTCMOS technique separates the circuit from the power supply and ground to prevent power dissipation in static state.

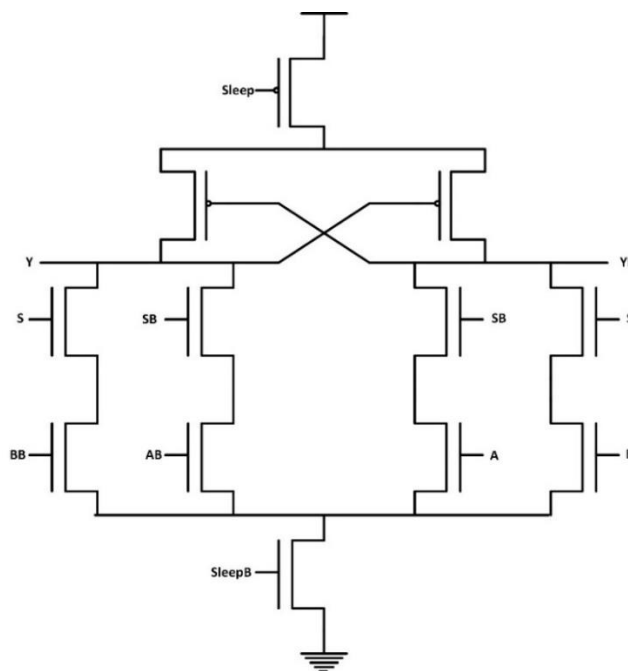


Fig. 3.8. Schematic of MTCMOS CVSL based Multiplexer

Here, two complemented sleep signals; sleep and sleepB are used to control the gates of PMOS and NMOS respectively. When sleep is low and sleepB is high, the circuit works as a standard CVSL based mux however, for the complementary case i.e. sleep = 1 and sleepB = 0, the circuit

gets disconnected from the supply and ground terminals which results in quite lesser static power dissipation than that of CVSL based multiplexer.

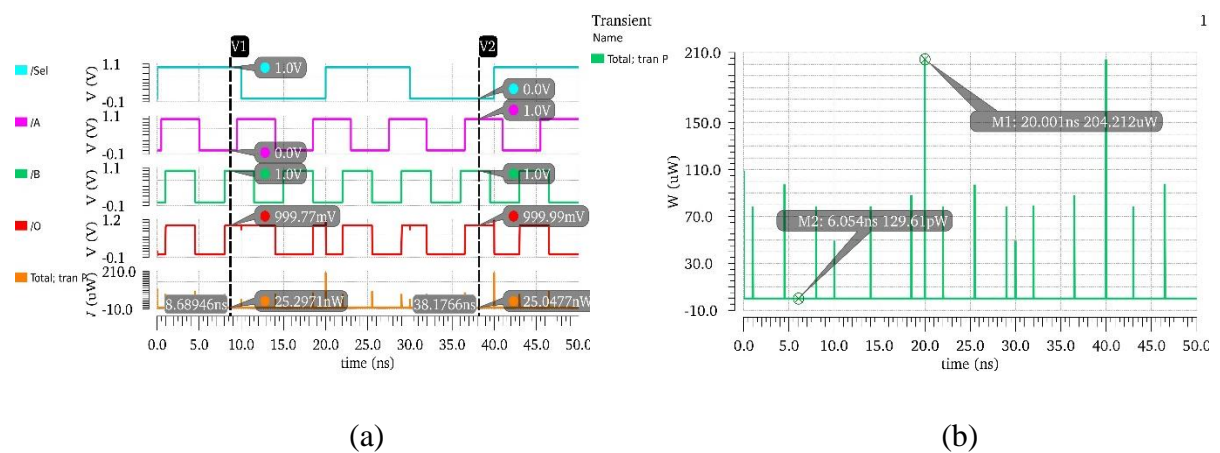
3.2 CHARACTERISTIC RESPONSE OF DIFFERENT MULTIPLEXERS

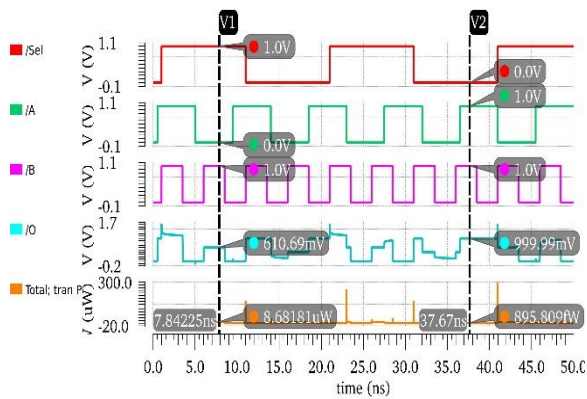
In this section, the output responses corresponding to different multiplexer techniques that have been discussed in the previous section are discussed and showcased. The common timing values used to generate output for the multiplexer techniques are given in Table 2. All the multiplexers are simulated for 50 ns to achieve the output waveform.

Table 3.2: Timing details of Sel, A, B

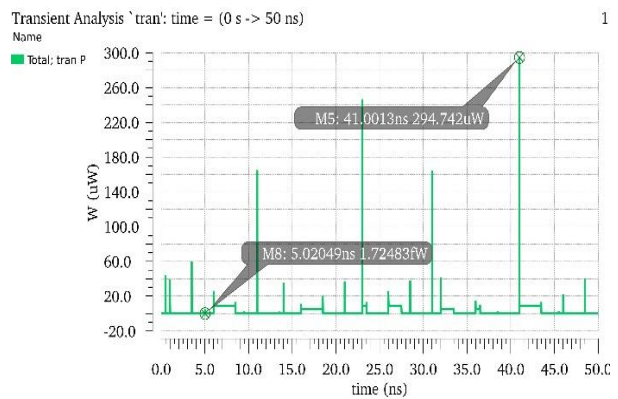
	Sel	A	B
Time period (ns)	20	9	7
Duty cycle (ns)	10	4.5	3.5
Delay (ns)	0	0.5	1

In an ideal scenario, the generated output waveform will attain 0 V and 1V level as per the input combination and select line configuration. If the output waveform is unable to attain a perfect 0 V or 1 V level, it is a non-ideal waveform. The output waveforms generated for all mux techniques is discussed here.





(c)

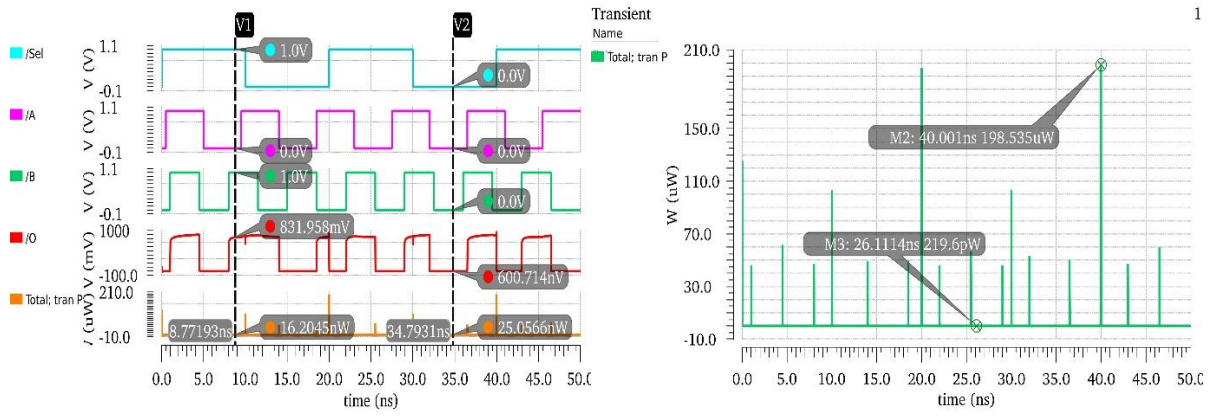


(d)

Fig. 3.9. Characteristic plot of TG based Mux (a) Output Response with Total Power Dissipation, (b) Total Power Dissipation, and GDI based Mux (c) Output Response with Total Power Dissipation, (d) Total Power Dissipation.

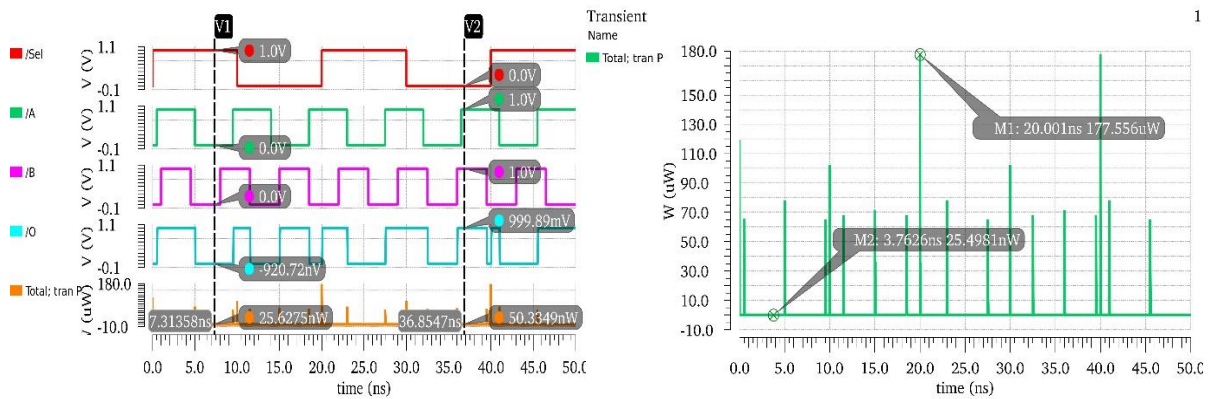
In TG based Mux all the signals transmitted through the Transmission Gate where both PMOS and NMOS is used. If input is 1 then PMOS will provide the strong 1 at the output and if input is 0 then NMOS will provide the strong 0 to the output. So, output in any case will not degrade as we can see in Fig. 10 (a). if Sel is 1, A is 1 and B is 0 then output is nearly 0 and if Sel is 0, A is 1, B is 0 then output is almost 1. This figure also shows the information about total power dissipation, at the time of switching power dissipation is more. Fig. 10 (b) shows the Total power dissipation, here the maximum power dissipation is 204.21uW and minimum power dissipation is 129.61pW.

In GDI based Mux only two MOSFET are used one PMOS and one NMOS. There is a drawback of degraded output in this type of Mux, when Sel is then PMOS will ON and if input is then PMOS will not be able to provide 0 at the output completely because PMOS gives weak 0, as we can see in Fig. 10 (c). whenever there will be switching in signals power dissipation will be more as we can see in Fig. 1 (c). Fig. 10 (d) shows the Total Power Dissipation where maximum power dissipation is 294.74uW and minimum power dissipation is 1.724fW.



(a)

(b)



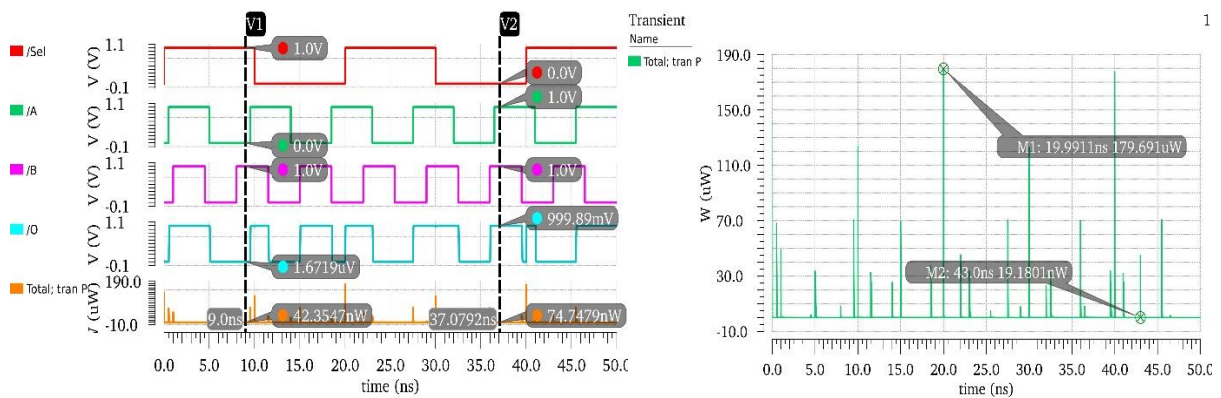
(c)

(d)

Fig. 3.10. Characteristic plot of PT based Mux (a) Output Response with Total power Dissipation, (b) Total Power Dissipation, and MSL based Mux (c) Output Response with Total Power Dissipation, (d) Total Power Dissipation.

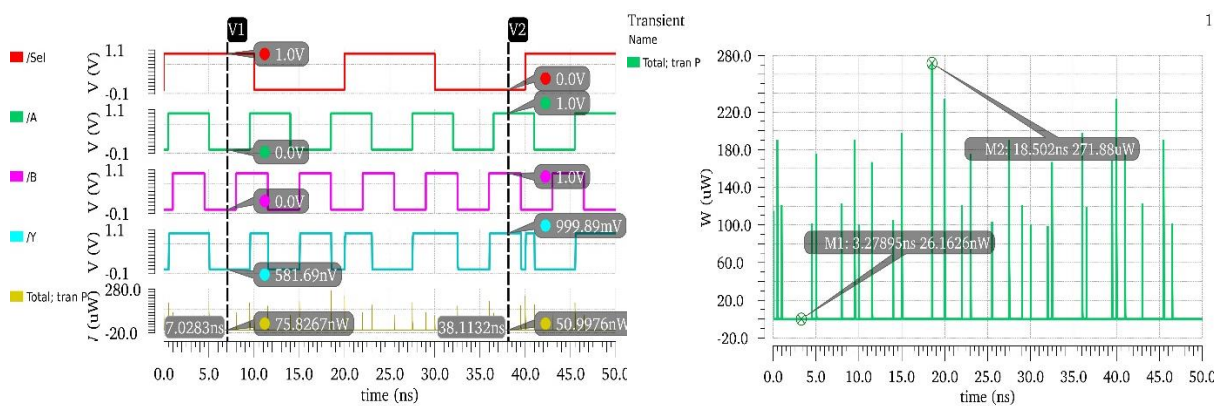
In PT based Mux only two NMOS is used to pass the input signals to the output and one inverter decides which input will pass to the output. Using NMOS as a switch to pass the input signal will increase the speed and area will be less in comparison to PMOS but there is a drawback of using NMOS, it gives weak 1 at the output. If Select signal is 1 and then Input B will pass to the output and if B is 0 then output will be 0 and if input B is 1 then output will not be completely 1 as shown in Fig. 11 (a), when Sel, B is 1 then output is nearly is 831.95mV. If Sel is 0 then input A will pass to the output and if A is 0 then output is 600.71nV which is nearly 0V. Total power dissipation in PT based Mux is shown in Fig. 11 (b) where maximum power dissipation is 198.535uW and minimum power dissipation is 219.6pW.

IN MSL based mux there is no level degradation problem because here one PMOS and one inverter is used in PT based Mux to restore the output level as shown in Fig. 11 (c). When Select signal is 1 then input A will pass to the output and if input A is 1 then output is nearly 1 and if input A is 0 then output is almost, so there is no drop of the signal level at the output. Same for input signal B, output will not degrade whatever the input signal. In MSL based Mux total power dissipation is shown in Fig. 11 (d), maximum power dissipation in MSL based Mux is less than PT based Mux which is 177.55uW and minimum power dissipation is more than PT based Mux which is 25.49nW.



(a)

(b)



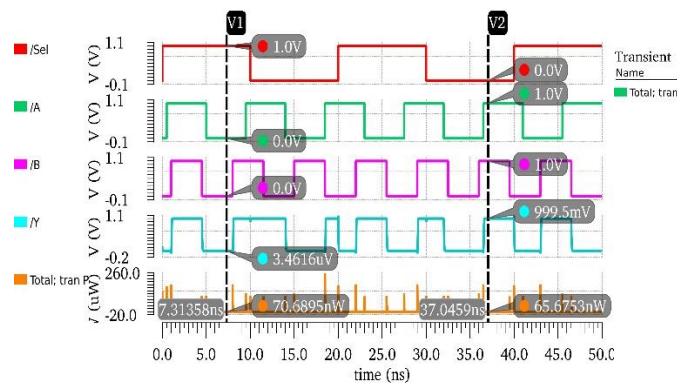
(c)

(d)

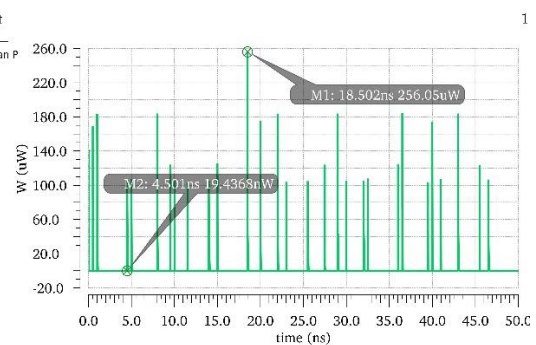
Fig. 3.11. Characteristic plot Static CMOS based Mux (a) Output Response with Total power Dissipation, (b) Total Power Dissipation, and CPL based Mux (c) Output Response with Total Power Dissipation, (d) Total Power Dissipation.

In Static CMOS based Mux both pull-up and pull-down network is used to perform the multiplexer operation. Total 8 MOS is used in which 4 for pull-down and 4 for pull-up network. It gives the complemented output, so one inverter is used to get the original output. Static CMOS based Mux requires both inverting and non-inverting input signals and one inverter to invert the select signal. If select signal is 1 then only A signal will pass to the output and if A is 1 then output is nearly 999.82 mV and if input signal A is 0 then output is 1.67uV which is nearly 0V as shown in Fig. 12 (a). Same case when select signal is 0 then input signal B will pass to the output. Output is not degraded in this type of Mux but it requires more numbers of MOS in compare to others. Power dissipation in Static CMOS based Mux is more compare to others because of a greater number of transistors used, maximum power dissipation is 179.69uW and minimum power dissipation is 19.18nW which is shown in Fig. 12 (b).

CPL based Mux provides both non-inverting and inverting output, when select signal is 1 then input signal A will pass to the output, if A is 1 then output Y will be 999.8mV approximately and YB will be nearly 0 as shown in Fig. 12 (c) and same case for when select signal is 0 then input signal B will pass to the output. Total power dissipation of CPL based Mux is shown in Fig. 12 (d), where maximum power dissipation is 271.88uW and minimum power dissipation is 26.16nW.



(a)



(b)

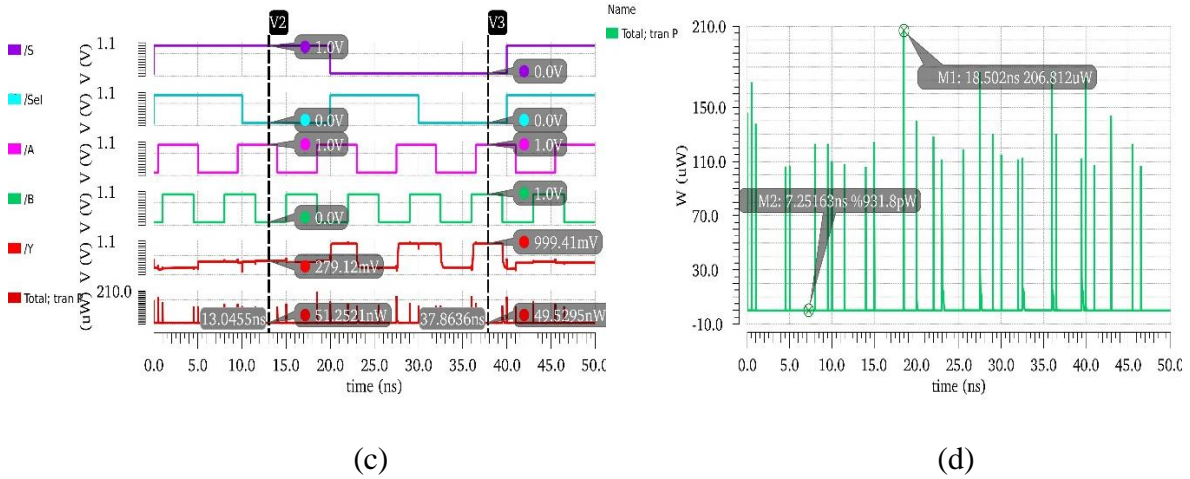


Fig. 3.12. Characteristic plot CVSL based Mux (a) Output Response with Total power Dissipation, (b) Total Power Dissipation, and MTCMOS CVSL based Mux (c) Output Response with Total Power Dissipation, (d) Total Power Dissipation.

CVSL based Mux stands for Cascode voltage switch logic. In this method both pull-up and pull-down network is used, in pull-down network 8 NMOS is used to pass the inverting and non-inverting signal of A, B and Sel but in pull-up network only two PMOS is used. By this CVSL based Mux both inverting and non-inverting output can be generated. When select signal is 0 then input signal A will pass to the output as shown in Fig. 13 (a), if A is 0 then output signal Y is almost 1.32uV and YB is 999.89mV and if input signal A is 1 then output Y is 999.89mV and YB is almost 1.30uV. Same condition for case when Select signal is 1 then input signal B will pass to the output, if B is 0 then output Y is 1.39uV And YB is 999.89mV, if B is 1 then output Y is 999.9mV and YB is nearly 43.75nV. Total power dissipation is consumed by CVSL based Mux is shown in Fig. 13 (b), here maximum power dissipation is 256.05uW and minimum power dissipation is 19.43nW.

MTCMOS CVSL based Mux is better than CVSL based Mux in terms of power dissipation. MTCMOS technique is used to reduce the static power dissipation when circuit is in idle condition. In MTCMOS technique two extra MOS is used one PMOS to isolate the power supply and one NMOS to isolate the ground to the main circuit because if there will be no connection of the circuit to the power supply then there will be no or very less power dissipation. Sleep signal is applied to those two extra MOS to reduce the consumption of power when there is no need of circuit. When sleep signal is 0 then circuit will work normal and if sleep signal is 1 then circuit will isolate form supply and also from the ground so, power dissipation will be less. When sleep signal is ON then output should be stable, there should not

be any change in the output by changing the input of the circuit because entire circuit is disconnected from the supply and ground as shown in Fig. 13 (c). Fig. 13 (d) shows the power dissipation analysis of the MTCMOS CVSL based Mux. Maximum power dissipation is 206.81uW, which is approximately 50uW less than CVSL based Mux and minimum power dissipation is 931.8pW, which is nearly 18nW less than CVSL based Mux.

3.3 DELAY AND POWER ANALYSIS

Use of multiplexer depends on some basic requirements like how much time it will take to pass the input signal to the output, how much power it will consume when inputs are switching, what is its average power dissipation and how much power it will dissipate when input are not switching means all are in static condition. If requirement is that multiplexer should be very fast in operation than we will use different multiplexer and if requirement is that it should dissipate very less power than multiplexer will be different. Below Table 3 shows the analysis of Delay, Average Power, PDP and Leakage. Expressions for power calculation is

$$P = V_{dd} \times I_{avg} \quad (1)$$

This is the total power consumption of the circuit. Where V_{dd} represents supply voltage and I_{avg} is the average current. Total power dissipation is the summation of Static and Dynamic power dissipation

$$P_{total} = \text{Static Power} \times \text{Dynamic Power} \quad (2)$$

This equation is represented by,

$$P(t) = V_{dd} \times I(t) \quad (3)$$

Static Power Dissipation (Leakage) is,

$$P = I \times V_{dd} \quad (4)$$

Dynamic Power Dissipation is,

$$P = C \times \alpha \times V_{dd} \times 2f \quad (5)$$

Where c is the capacitance, α is the switching activity, V_{dd} is the supply voltage, f is the frequency and I is the static current.

Table 3.3: - Delay, Average power, PDP and Static power dissipation analysis.

Mux	Delay (s)	Average Power	PDP (J)	Static Power Dissipation
Conventional TG MUX	3.844p (A to O) 4.832p (B to O)	158.9nW	0.61a	25.25nW
GDI Based Mux	1.65p (A to O) 2.42p (B to O)	1.64uW	2.7a	219.99pW
PT Based Mux	3.57p (A to O) 4.60p (B to O)	110.9nW	0.395a	25.22nW
MSL Based Mux	17.65p (A to O) 16.22p (B to O)	792.4nW	13.98a	25.49nW
Static CMOS based Mux	34.87p (A to O) 35.55p (B to O)	605.29nW	21.1a	25.48nW
CPL based Mux	47.57p (A to O) 47.47p (B to O)	1.42uW	67.54a	101.07nW
CVSL Based MUX	64.40p (A to O) 65.42p (B to O)	1.16uW	74.7a	65.85nW
MTCMOS CVSL based Mux	172.0p (A to O) 171.7p (B to O)	736.4nW	126.6a	63.83nW(S=0) 25.51nW(S=1)

By analysing the delay and power of different multiplexer it is clear that performance of each mux is different and two of them showing better performance compare to others in terms of delay, power and leakage. In Table 3 it is clear that delay of GDI based Mux is 1.65ps which is fast compare to all other Mux, if there is a requirement of fast operation then GDI based Mux should be used. In some scenario when circuit is in idle condition that's mean input signals are not changing at that time leakage will occur. For static condition GDI based Mux shows the best performance, it dissipates 219.99pW in idle condition. PT based Mux is little bit slower than the GDI based Mux and has the lowest Average power dissipation 110.9nW, if we want mux which should have less average power dissipation than PT based Mux is the best option. In some of the condition we check that PDP of the circuit should be minimum for better operation, for that PT based Mux shows the optimum performance. PDP of PT based Mux is 0.395aJ.

The Delay of the circuit represents the time taken by the signal to reach from the input to output. Higher the delay more time required by the circuit to reach the output.

$$\tau_{delay} = \frac{\tau_{PLH} + \tau_{PHL}}{2} \quad (6)$$

τ_{PLH} = time for the fall to rise of the signal.

τ_{PHL} = time for the rise to fall of the signal.

After the power and delay calculation power delay product are calculated, which is the multiplication of both delay and power, represented by PDP.

$$\text{PDP} = \text{Delay} \times \text{Power} \quad (7)$$

These calculations of the circuits help the designer and user to understand the performance of the circuit.

IMPORTANT OUTCOMES:

- Designing and analysis of different type of multiplexers is accomplished.
- All the designing is done using MOSFET at 90nm technology node at 1V.
- Analysis shows that in all different multiplexers GDI and PT based multiplexers provides the best and efficient performance.
- In both GDI and PT based mux delay of GDI is less and consumes less static power dissipation

CHAPTER IV

POWER ANALYSIS

4.1 STATIC POWER DISSIPATION ANALYSIS

In this section static power dissipation is analysed of different type of mux. Static power analysis is done when all the input signals are stable to either one or zero. Timing values used for analysis of static power dissipation is, Sel, input signal A is 1 and B is 0.

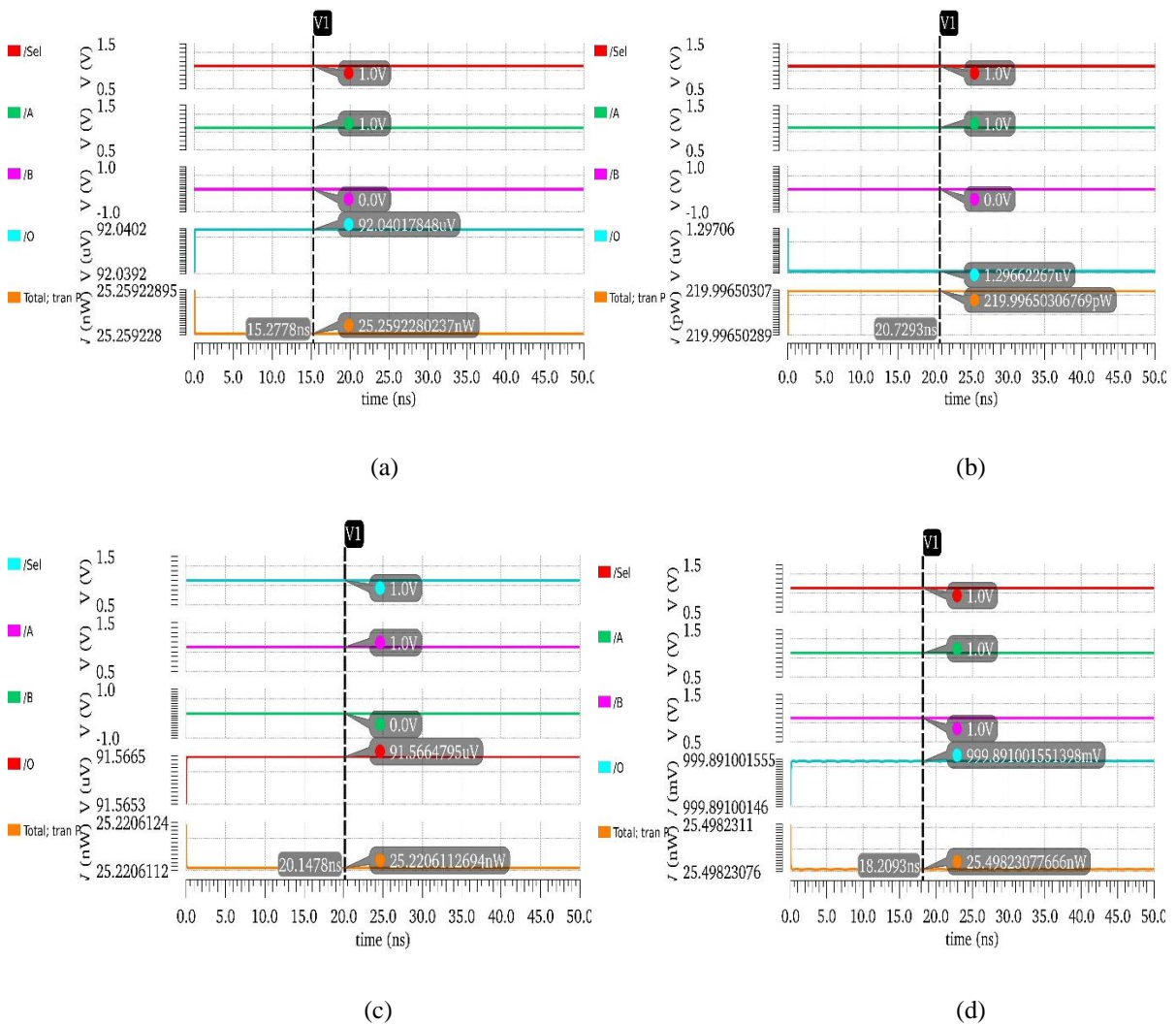
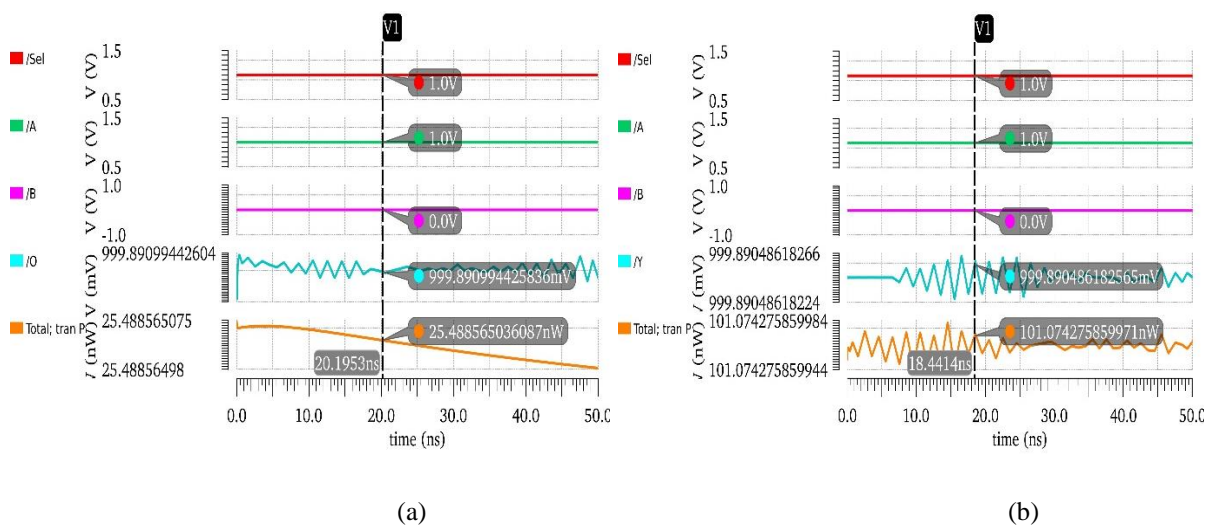


Fig. 4.1. Static power dissipation plot for (a) TG based Mux (b) GDI based Mux (c) PT based Mux (d) MSL based Mux.

TG based mux is a conventional type mux, where two transmission gates is used to pass the input signal and select signal is used to decide which input will pass to the output. Main power supply is only connected to the inverter which will invert the select signal. So, the static power dissipation which is also call leakage is 25.25nW as shown in Fig. 14 (a). GDI based mux looks like CMOS inverter but in GDI based mux both source of PMOS source of NMOS is connected to the input signals rather than connected to the power supply and the ground. In GDOI based cell only two MOS is used so static power dissipation in this mux is 219.99pW as shown in Fig. 14 (b) which is very less compare to others multiplexers. In PT based Mux two NMOS is used to pass the input signals to the output but contrary to GDI in PT based mux both MOS are NMOS and one inverter is also used to decide which input will pass to the output. In PT based Mux static power dissipation shown in Fig. 14 (c) is 25.22nW. Working and design of MSL based Mux is same as PT based mux with some extra hardware but. The advantage of MSL based mux over PT based Mux is that it overcome the drawback of low voltage swing. In PT based mux NMOS b pass the input signal to the output, if input is 1 then output will be less than 1 because NMOS gives weak 1 at the output. This problem can be solved by the MSL based Mux. Because of the use of extra circuit to overcome the drawback of PT based Mux static power dissipation is increased, as shown in the Fig. 14 (d) static power power dissipation is 50.54nW



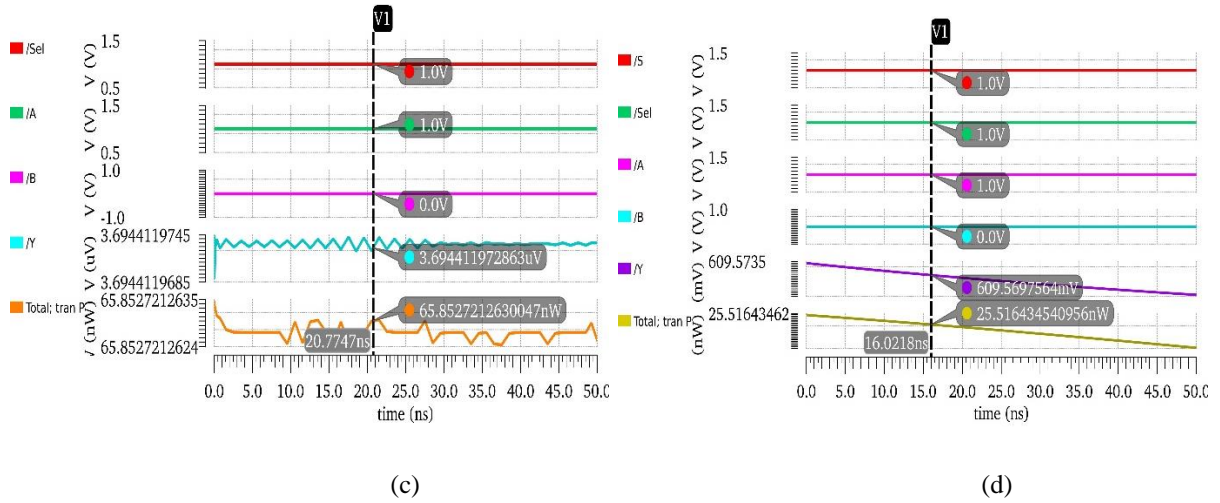


Fig. 4.2. Static power dissipation plot for (a) Static CMOS based Mux (b) CPL based Mux (c) CVSL based Mux (d) MTCMOS CVSL based Mux.

In static CMOS based Mux both pull-up and pull-down network is used, because of more than one transistor in series leakage path resistance is high which will reduce the leakage in this circuit, Fig. 15 (a) shows the static power dissipation 25.48nW. CPL stands for complementary pass transistor logic, in which NMOS pass transistor is used to pass the input signals with PMOS and inverter to restore logic level at the output of the pass transistors. When select, A is 1 and B is 0, then static power dissipation is 101.07nW depicted in Fig. 15 (b). In Cascode voltage switch logic only two PMOS is used rather than using dual of NMOS. Both PMOS are connected back to back, because to this method output will not degrade and in static input condition leakage will be less as shown in Fig. 15 (c). Static power dissipation is 65.85nW. MTCMOS CVSL based Mux is modified version of CVSL based Mux. MTCMOS technique is used to reduce the leakage in the circuit for this one NMOS is used to isolate the ground and one PMOS is used to isolate the supply. As we can see clearly that in MTCMOS CVSL based Mux static power dissipation is 25.51nW as shown in Fig. 15 (d). which is 40.34nW less than CVSL based Mux.

4.2 SWITCHING AND SCALING

This section illustrates the importance and details of scaling of the power supply and switching. Scaling of the power supply affects the dissipation of power in both dynamic and static condition. Less power supply causes less power dissipation, contrary is also true. Whereas,

switching of the signal also have an effect on power dissipation. If switching of the signals occurs at same time, then it increases the power dissipation.

4.2.1 Scaling of Power Supply:

Voltage Scaling is an essential part of VLSI (Very Large-Scale Integration) to increase the performance of the devices, demand and success of the industries. Voltage Scaling directly affects power dissipation. Scaling down the power supply leads to less power dissipation with the condition of not affecting the output. If by scaling down the voltage causing the wrong output, then it's the limit at which further scaling down is not possible. In this section, voltage scaling is done on multiplexers to get an analysis of power dissipation at the different power supply. MOS is a basic building block for any logic circuits and scaling of voltage in MOS improves its performance. After a complete analysis of delay, power dissipation, and leakage of the multiplexers it is found that two of them show better performance compared to others. Voltage Scaling of both multiplexers is shown in Table 4.

Table 4.1. Scaling on GDI based Mux and PT based Mux

Multiplexer	Scaling of supply	Maximum Power Dissipation	Minimum Power Dissipation	Average Power Dissipation	Leakage
GDI based Mux	1V	294.7uW	1.725fW	1.73uW	219.9pW
	0.8V	230.1uW	1.58fW	166.6nW	87.88pW
	0.6V	157.5uW	9.51fW	22.13nW	32.74pW
PT based Mux	1V	198.5uW	219.6pW	110.9nW	25.22nW
	0.8V	119.7uW	25.04nW	223.2nW	10.637nW
	0.6V	74.2uW	25.05nW	4.05uW	4.13nW

Above Table 4 clearly states that when we reduce the value of supply voltage there are some considerable amount of reduction in both dynamic and static power dissipation. Here up to at 3 level voltage power is analysed.

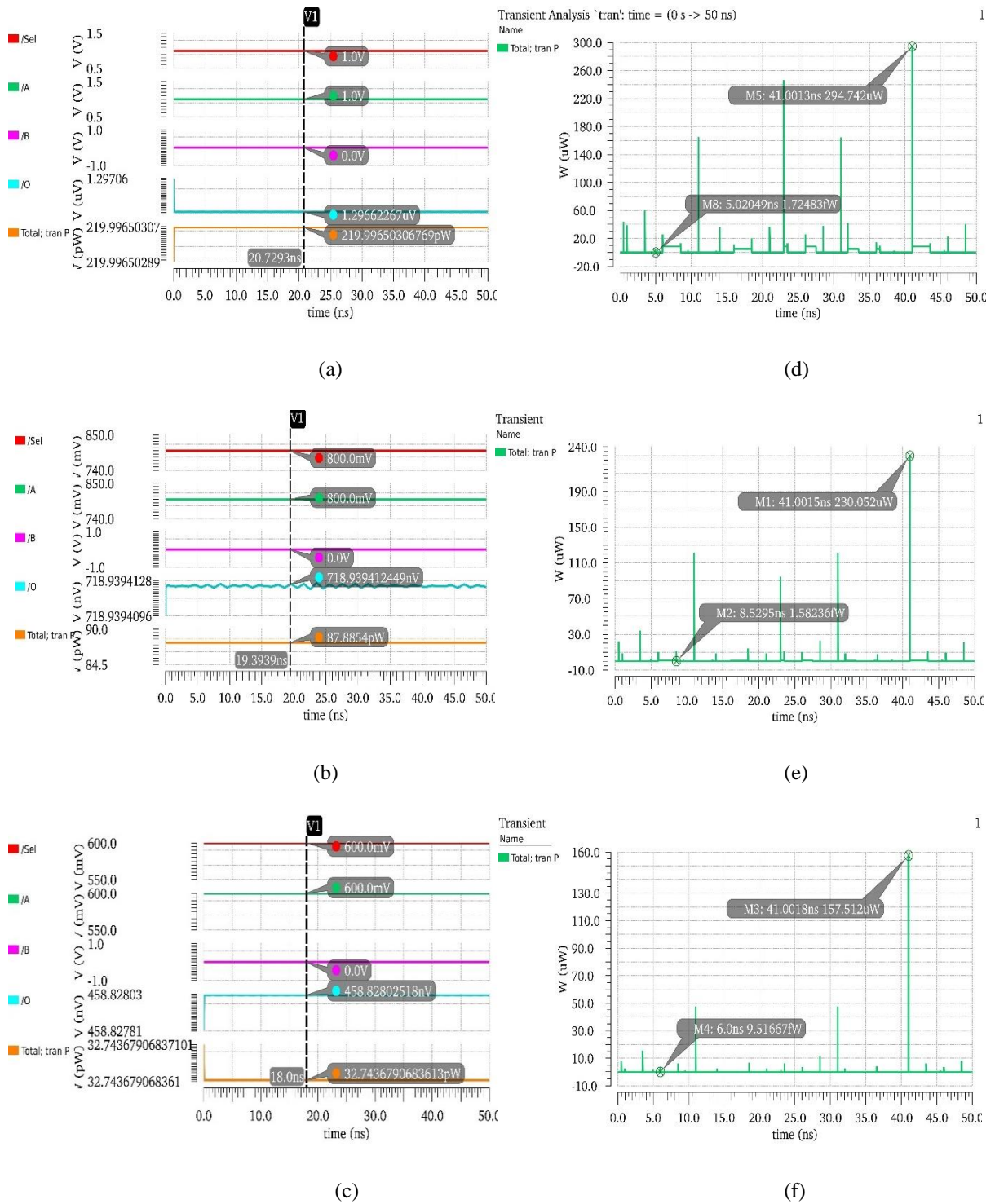
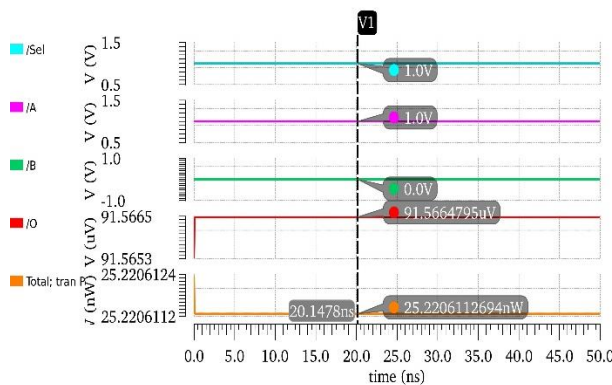


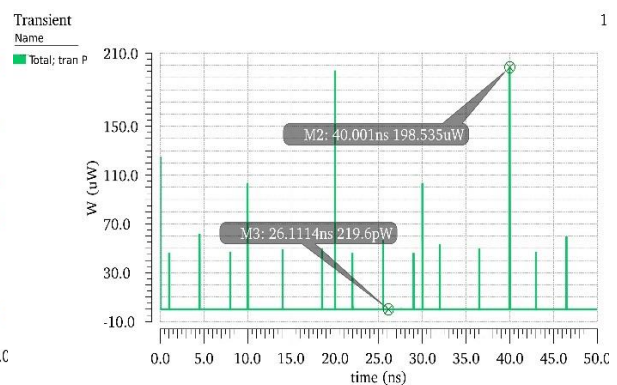
Fig. 4.3. Static Power Dissipation of GDI based Multiplexer at (a) $V_{dc}=1V$, (b) $V_{dc}=0.8V$ and (c) $V_{dc}=0.6V$. Total Power Dissipation of GDI based Mux (d) $V_{dc}=1V$, (e) $V_{dc}=0.8V$ and (f) $V_{dc}=0.6V$.

In GDI based Mux at $V_{dc}=1V$ maximum power dissipation is 294.7uW and average power dissipation is 1.73uW but when we reduce the power supply from 1V to 0.6V maximum power dissipation is also reduced to 157.5uW which is 46.55% less than of maximum power

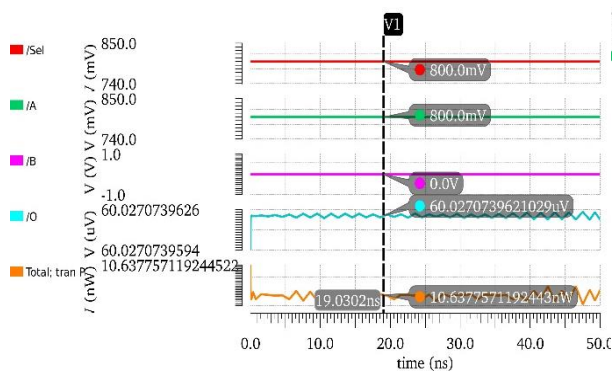
dissipation at 1V and average power dissipation reduced to 22.13nW at 0.6V which is 98% less than of average power dissipation at 1V as shown in Table 4. leakage is also 85.11% reduced from 219.9pW at 1V to 32.74pW at 0.6V as shown in Fig. 16 (a), (b), (c). While reducing the supply voltage output is not degrading but power dissipation is reduced which will improve the performance. Fig. 16 (d), (e), (f) shows the analysis of total power dissipation at different voltage node.



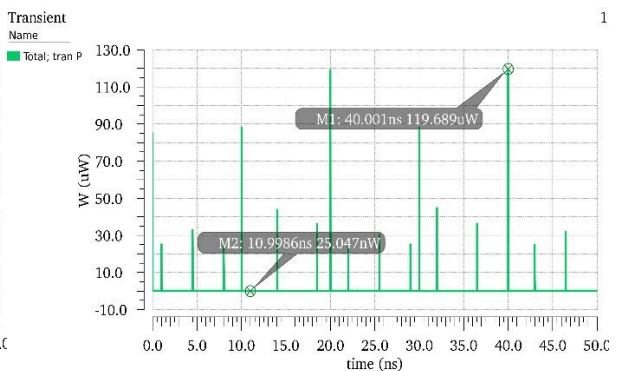
(a)



(d)



(b)



(e)

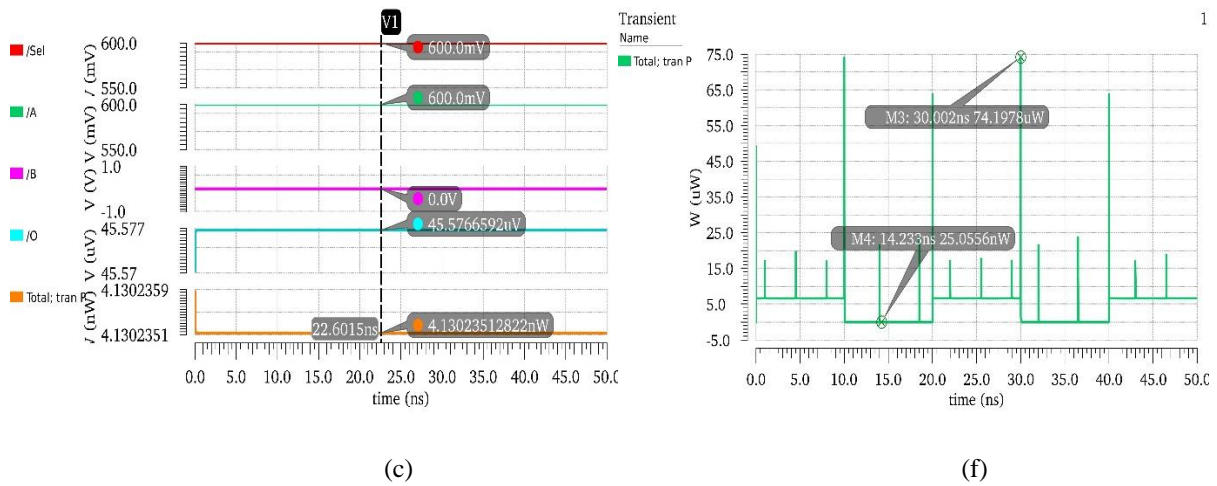


Fig. 4.4. Static Power Dissipation of PT based Multiplexer at (a) $V_{dc}=1V$, (b) $V_{dc}=0.8V$ and (c) $V_{dc}=0.6V$. Total Power Dissipation of PT based Mux (d) $V_{dc}=1V$, (e) $V_{dc}=0.8V$ and (f) $V_{dc}=0.6V$.

In PT based Multiplexers maximum power dissipation is reduces from 198.5uW at 1V to 74.2uW at 0.6V which is 62.61% less than maximum power dissipation at 1V shown in Table 4. 15. When circuit is static condition, leakage (static power dissipation) is also 83.62% reduced from 25.22nW at 1V to 4.13nW at 0.6V as shown in Fig. 17 (a), (b), (c). Analysis and variation of total power dissipation at different voltage level is shown in Fig. 17 (d), (e), (f).

4.2.2 Switching of the signals:

Switching at different time instances shows different power dissipation. If signals are switching at the same time than power dissipation will be more and if switching of the signals is happening at different time instances then power dissipation will be less. Two different Timing values which is being used in this analysis one for same time switching and one for different switching time. (1) Different Time Switching- for select signal Time period= 20ns, Duty cycle= 10ns and Delay= 0ns, for input signal A Time period=9ns, Duty cycle=4.5ns and Delay=0.5ns and for input signal B Time period= 7ns, Duty cycle= 3.5ns and Delay= 1ns. (2) Same time switching- for select signal Time period=50ns, Duty cycle=25ns and Delay= 0ns, for input signal A Time period= 9ns, Duty cycle= 4.5ns and Delay= 0.5ns and for input signal B Time period= 9ns, Duty cycle=4.5ns and Delay= 1ns.

Table: Timing Values

Timing	Signals	Time Period (ns)	Duty Cycle (ns)	Delay (ns)
Different Timing	Select	20	10	0
	A	9	4.5	0.5
	B	7	3.5	1
Same Time	Select	50	25	0
	A	9	4.5	0.5
	B	9	4.5	1

4.2.2.1 GDI based Multiplexer

In this multiplexer only two MOS is used to pass the input signals. Switching at different time and same time will change the power dissipation. Same switching more power dissipation and different switching less power dissipation.

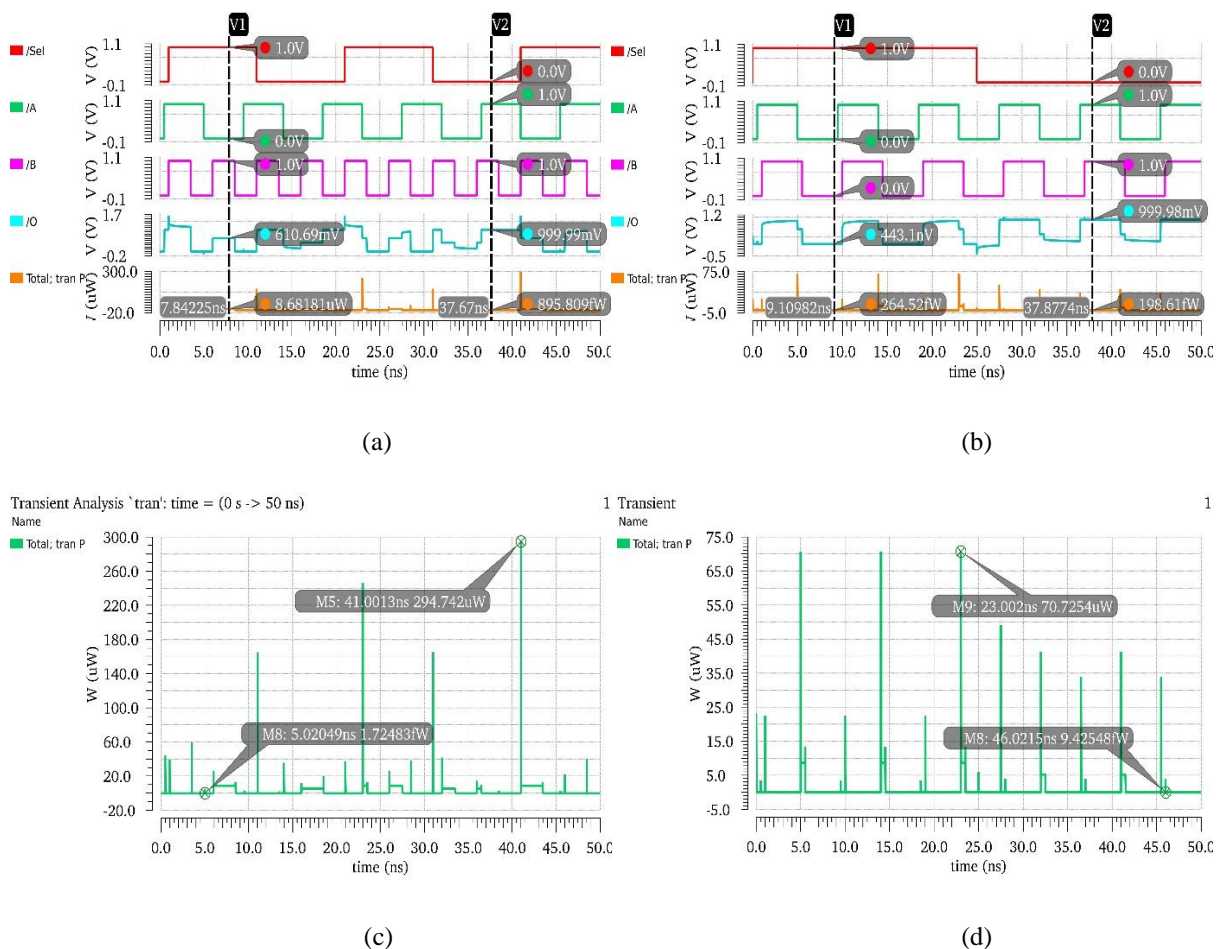


Fig. 4.5. GDI based Multiplexer (a) Output plot at Same Time Switching, (b) Output Plot at Different Time Switching, (c) Total Power Dissipation at Same Switching, (d) Total Power Dissipation at Different Time Switching.

Effect of the same time switching on power dissipation is shown in Fig. 18 (a), when select signal and input signal switch at the same time, power dissipation is more. Maximum power dissipation at same time switching is 294.74uW at V power supply as shown in Fig. 18 (c). When select signal and input signal switches at different time then power dissipation very less as shown in Fig. 18 (b). Switching at different time then power dissipation is reduced to 70.725uW shown in Fig. 18 (d), which is 76% less than of maximum power dissipation at same time switching. By just changing the switching time, we can save the large amount of power, so signal should not switch at the same time.

4.2.2.2 PT based Multiplexer

In PT based Multiplexer two NMOS is used to pass the input signal to the output. If both select signal and input signal will switch at same time then power dissipation will be more.

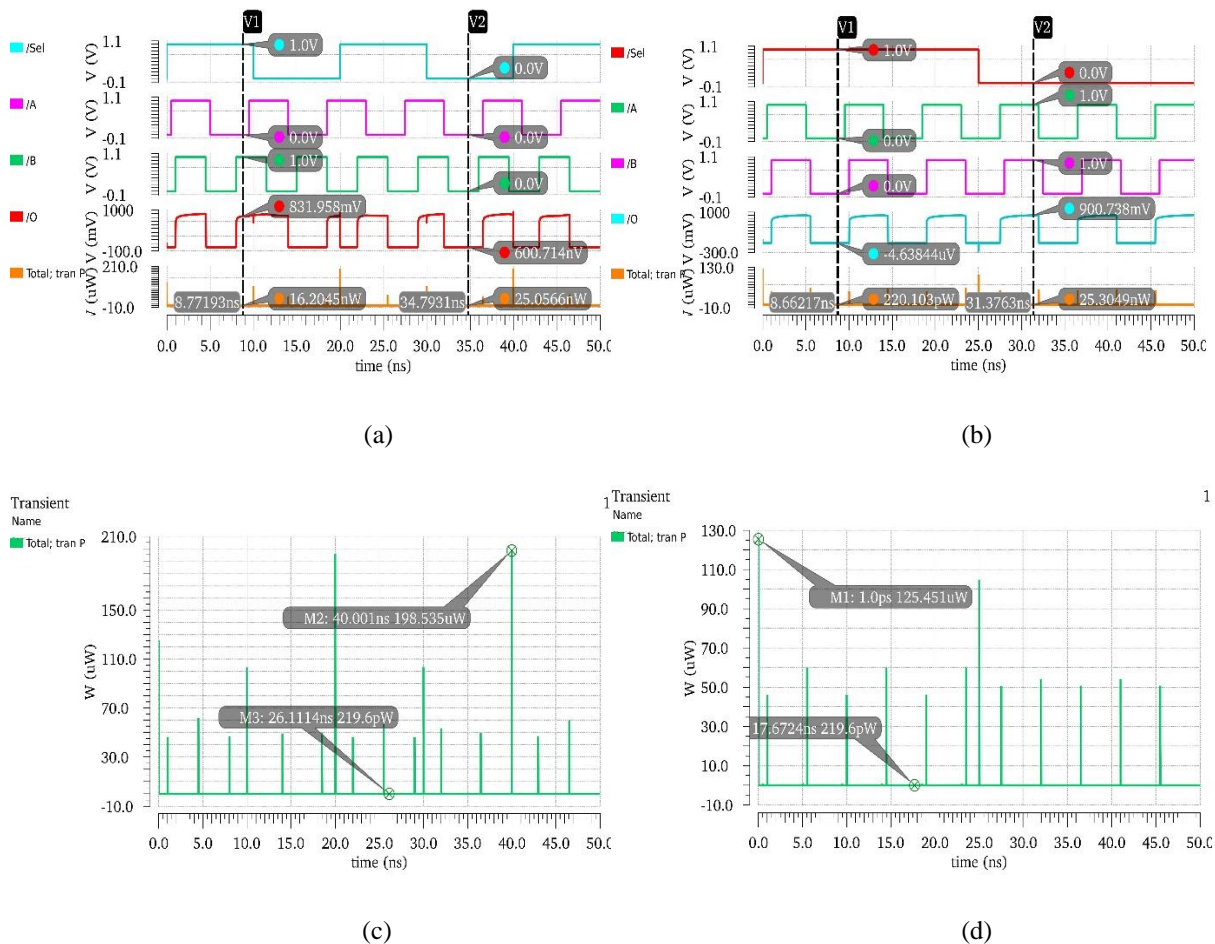


Fig. 4.6. PT based Multiplexer (a) Output plot at Same Time Switching, (b) Output Plot at Different Time Switching, (c) Total Power Dissipation at Same Switching, (b) Total Power Dissipation at Different Time Switching.

In PT based Multiplexer switching of the signal at same time is shown in Fig. 19 (a). when both signals will switch at the same time power dissipation will be more, So Maximum power dissipation when switching of the signal is at the same time is 198.53uW is shown in Fig. 19 (c). Fig. 19 (b) shows the output plot when switching is at different time causes less power dissipation. Maximum power dissipation is 125uW as shown in Fig. 19 (d), which is 36.8% less than maximum power dissipation when switching is same. This analysis of switching shows that we can reduce the dissipation of power by just switching in appropriate way.

IMPORTANT OUTCOMES:

- In this section static power dissipation analysis is done.
- Analysis of the effect on power dissipation caused by the scaling of voltage supply and switching of the signals is achieved.
- Scaling of voltage supply is done at 1V, 0.8V and 0.6V. whereas for switching two timing signals were used.
- All the analysis is done on GDI and PT based mux.
- Scaling of the supply states that, further reduction in power supply is possible to reduce the power consumption without degrading the output of the multiplexer.
- If signals switch at same time causes more power dissipation compares to switching at different time.

CHAPTER V

FINFET BASED MULTIPLEXERS

5.1 MULTIPLEXERS

To understand the FinFET based multiplexers, the knowledge of basic FinFET is important. FinFET stands for Fin Field-effect transistor which is multi-gate device. It is same as MOSFET where gate covers the channel from two, three or four sides, which forms a double gate structure. These devices given a name Finfet because the source and drain region forms a fin on the silicon substrate. FinFET have faster switching, high current density, less power consumption and reduced leakage. As technology node decreasing, many problems were arising in MOSFET due to short channel like DIBL, impact ionization, Hot electron effect, voltage saturation. FinFET technology overcomes this short channel effects and provides optimum performance in terms of delay and power with low power supply. Area consumed by FinFET is less than MOSFET leads to less power dissipation, fast operation and requires less supply voltage to operate. These are all the reasons to prefer FinFET over MOSFET.

In this section GDI based multiplexer and PT based multiplexer is designed using FinFET 18nm technology node. Switching at different time instance is also done to analyse the changes in power dissipation and leakage. Scaling of voltage from 0.8V to 0.4V will show the variation in power dissipation, leakage and its speed of operation.

5.1.1 PT based Multiplexer

PT based Mux is designed using two NMOS and one inverter to invert the select signal. Fig. 20 (a) displays the circuit diagram of PT (Pass Transistor) based mux. Designing of many circuits can be done using a smaller amount of transistors [10]-[12]. The Source of the NMOS is connected to the input signal and gates are connected to the select signal and invert of the select signal. By using this device number of transistors has reduced but it also has some drawback that, when 1 is provided to the input then output is not near to the input level because NMOS provides weak 1 at the output.

Merits and Demerits: For PT based Mux merits are, effects of interconnections is low, less power consumption and fast operation. It has also some disadvantages like Sluggish operation and Reduced voltage swing.

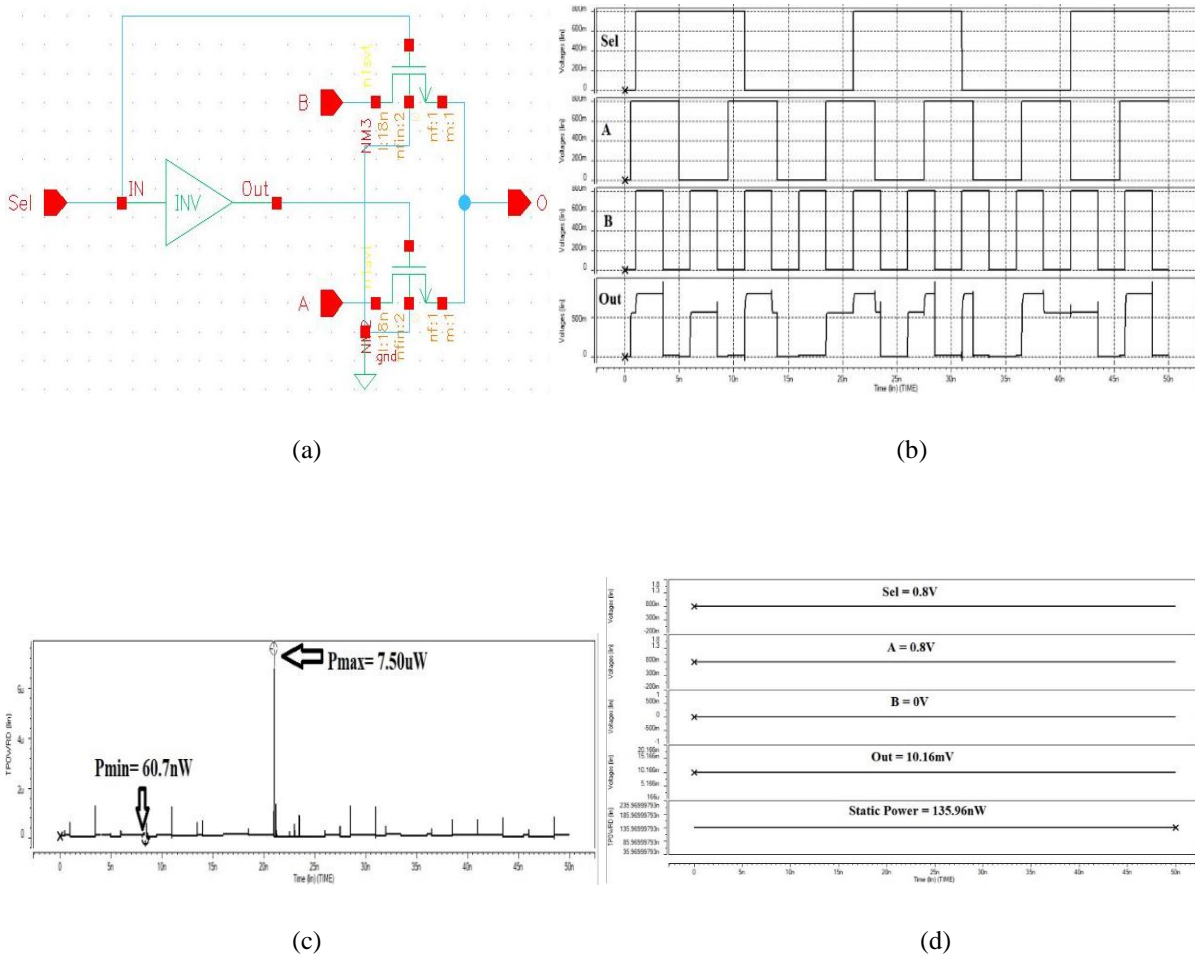


Fig. 5.1. PT based Multiplexer using FinFET (a) Schematic, (b) Output with Total power dissipation, (c) Total Power Dissipation and (d) Output with Static Power Dissipation.

Fig. 20 (a) displays the Schematic of PT (Pass Transistor) Based Multiplexer. The source is connected to input signals A and B. Gate of one NMOS is connected to a select signal and the gate of the second NMOS is connected to the invert of the select signal. Fig. 20 (b) demonstrates the output waveform. When Sel=1, then input B reaches the output, and if B=1 then output is 659.62mV which is approx. 140mV less than 800mV because NMOS provides weak 1 at the output. When Sel=0, then output is equal to input signal A and if input A is 0V then output is 72.9uV which is near to 0V because NMOS gives strong 0 at the output.

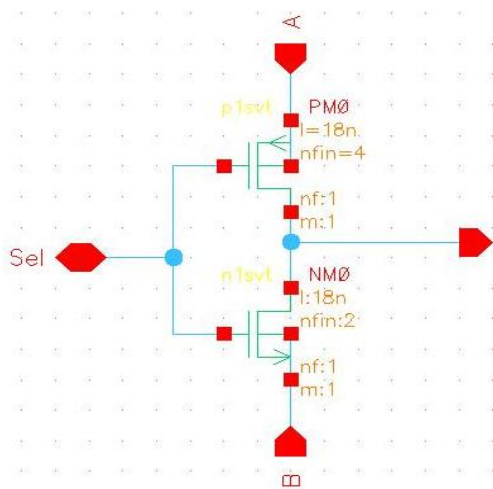
Static power dissipation in the PT based Mux is analysed by fixing the input signals Sel=A=0.8V and B at 0V. This case causes the 135.96nW static power dissipation which is more than GDI based Mux as shown in Fig. 20 (d). Although both GDI and PT use only two MOS to pass the input signal in PT based MUX both are NMOS. Now, when Sel=0, then input A passes to output and causes leakage at the NMOS where input B is connected. If Sel is 0.8V

then output is directly connected to the input B and leakage occurs at the NMOS where input A is connected. Total power dissipation plot is illustrated in the Fig. 20 (c), where maximum power dissipation is 7.50uW and minimum power dissipation is 60.7nW.

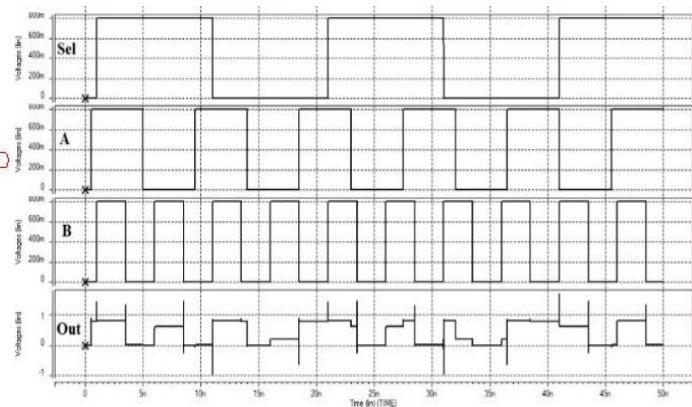
5.1.2 GDI based Multiplexer

GDI (Gate Diffusion input) cell is a novel type of circuit for a low power combinational circuit. Using this GDI cell complex circuit can be designed with a smaller number of transistors. GDI cell overcomes the drawback of CMOS, in terms of transistor count, delay, and consumption of the power. In CMOS, the dual method is used to design any circuit because of this transistor count in the circuit gets doubled, due to this area is increased and signal takes too much time to pass from input to output. All these problems can be resolved by using the GDI cell, by which area, delay, and power are reduced. GDI cell is constructed using two-transistor NMOS and PMOS, it resembles the CMOS inverter circuit [7]-[9]. In CMOS inverter source of PMOS and NMOS are connected to the supply and the ground respectively but in GDI cell source of PMOS and NMOS are connected to the input signal. Some advantages and disadvantages of GDI (Gate Diffusion input) are.

Merits and Demerits: Every system has several positive and negative points, therefore, qualities are number of transistors are very less, fast in operation and Power dissipation (Both static and Dynamic), However, drawbacks is that in certain state output is not near to the V_{dc} supply voltage. When Sel=B=1, NMOS will pass the input signal B to output O, if the input is 0, then the output will be 0 nonetheless if the input is 1 then output is not complete 1, because NMOS provides weak 1 at the output node.



(a)



(b)

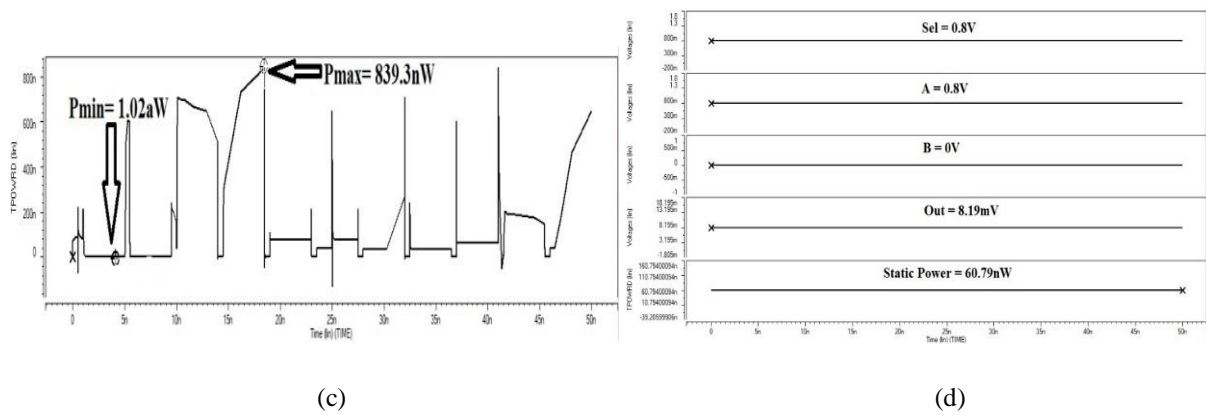


Fig. 5.2. GDI based Multiplexer using FinFET (a) Schematic, (b) Output with Total power dissipation, (c) Total Power Dissipation and (d) Output with Static Power Dissipation.

The source terminal of PMOS and NMOS are connected to input signals A and B respectively. Both MOS gates are connected to Select signal (Which will decide the input to output). The schematic of the GDI based Mux using FinFET is shown in Fig. 21 (a). If $Sel=0$, then input signal A passes to the output, if A is 0.8V then output is approx. 0.7V and if A is 0V then output is in 140.8mV. When, $Sel=1$, then output is directly connected to the input signal B. Output of GDI (Gate Diffusion input) based Mux is illustrated in Fig. 21(b). This Fig also illustrates the total power dissipation, where maximum power dissipation is 839.3nW and Minimum power dissipation is 1.02aW as depicted in the Fig. 21 (c). Dynamic power dissipation occurs at the time of switching of the signals. If switching of more than one signal is happening at the same time, then power dissipation will also be high.

Static power dissipation is analysed by keeping all the inputs stable at some supply voltage. In case, when select and input signal A at 0.8V and input signal B at 0V supply, Static power dissipation (leakage) in the circuit is 60.79nW as illustrated in Fig. 21 (d). When, $Sel=A=0.8V$ and $B=0V$, then input B passes to the output, at that moment leakage occurs in then PMOS. If $Sel=B=0$ and $A=0.8V$, subsequently NMOS causes the leakage in the circuit.

5.2 DELAY AND POWER ANALYSIS:

This section investigates the important factors of the multiplexer which are Delay and power dissipation. A circuit should be fast and must consume less power for better performance. Table 5 displays the maximum, minimum, and Average Power.

Table 5.1: Summary of Power and Average Power

Mux	Power		Average Power
	Max	Min	
GDI Based Mux	839.3nW	1.02aW	27.15nW
PT Based Mux	7.50uW	60.7nW	100.8nW

In this section analysis of delay and power, dissipation is done at 0.8V power supply. In GDI based Mux when a select signal is 0 input A will pass to the output and it will take 0.0107ps. The average power dissipation is 27.15nW, so the PDP (Power Delay Product) is 0.00029aJ. This PDP is very less compared to all other multiplexers and static power dissipation is 60.79nW. Table 6 displays the Delay, Average Power, PDP (Power Delay Product), and Static Power Dissipation [13-14].

Table 5.2: Delay, Average Power, PDP (Power Delay Product) and Static Power Dissipation.

Mux	Delay (s)	Average Power	PDP (J)	Static Power Dissipation
GDI Based	0.0107p	27.15nW	0.00029a	60.79nW
PT Based	1.77p	100.8nW	0.178a	135.97nW

In PT based Multiplexer, when Sel=0, at that time input signal A reaches to output with the delay of 1.77ps. The average power dissipation is 100.8nW, so power delay product (PDP) will be 0.178aJ, and static power dissipation is 135.97nW.

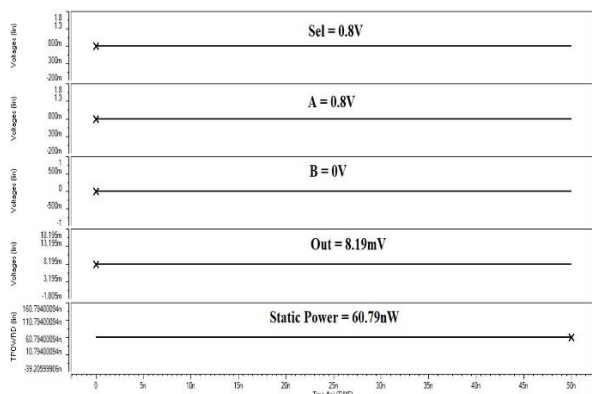
5.3 SCALING OF POWER SUPPLY

Scaling of power supply is done at 0.8V, 0.6V and 0.4V. At each voltage level maximum power dissipation, minimum power dissipation, average power dissipation, static power dissipation and delay is analysed. When we move toward the lower level of supply voltage, total power dissipation gets reduced and speed is increased. Table 7 shows the details of scaling of GDI and PT based Mux.

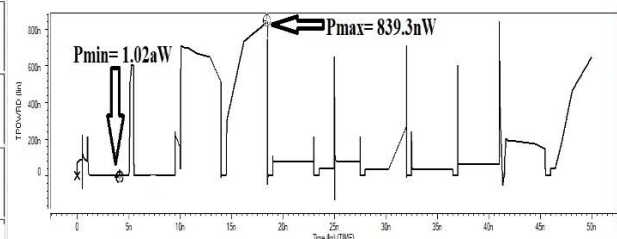
Table 5.3: Scaling of GDI and PT based Multiplexer.

Multiplexer	Scaling of supply	Maximum Power Dissipation	Minimum Power Dissipation	Average Power Dissipation	Static Power Dissipation
PT based Mux	0.8V	7.50uW	60.7nW	100.8nW	135.97nW
	0.6V	1.71uW	35.19nW	57.3nW	78.62nW
	0.4V	796.06nW	15.07nW	24.53uW	33.64nW
GDI based Mux	0.8V	839.3nW	1.02aW	27.15nW	60.79nW
	0.6V	548.4nW	2.02aW	15.36nW	35.19nW
	0.4V	146.49nW	1.26aW	6.85nW	15.08nW

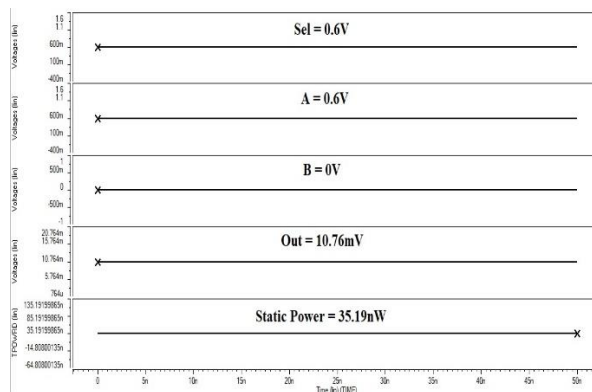
Maximum, minimum power dissipation, Average power and leakage all are reduced form 0.8V to 0.4V power supply.



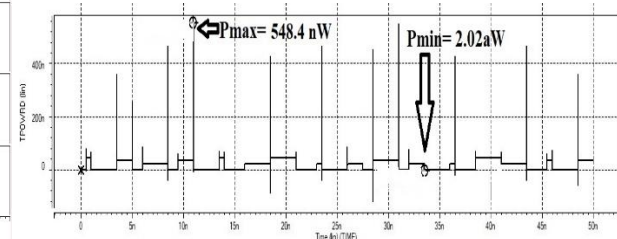
(a)



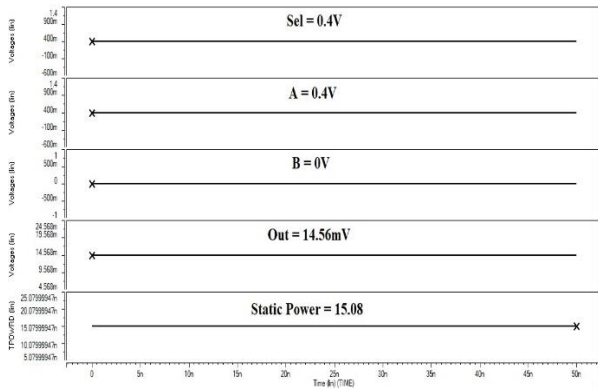
(d)



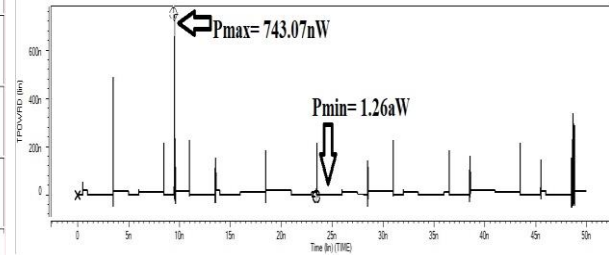
(b)



(e)



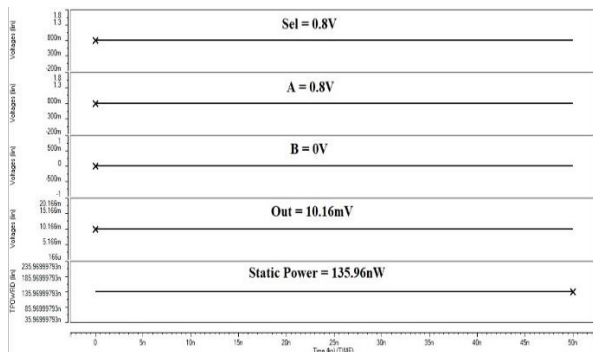
(c)



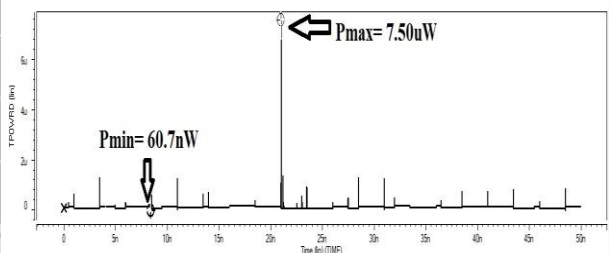
(f)

Fig. 5.3. Static Power Dissipation of GDI based Multiplexer using FinFET at (a) $V_{dc}=0.8V$, (b) $V_{dc}=0.6V$ and (c) $V_{dc}=0.4V$. Total Power Dissipation of GDI based Mux using FinFET at (d) $V_{dc}=0.8V$, (e) $V_{dc}=0.6V$ and (f) $V_{dc}=0.4V$.

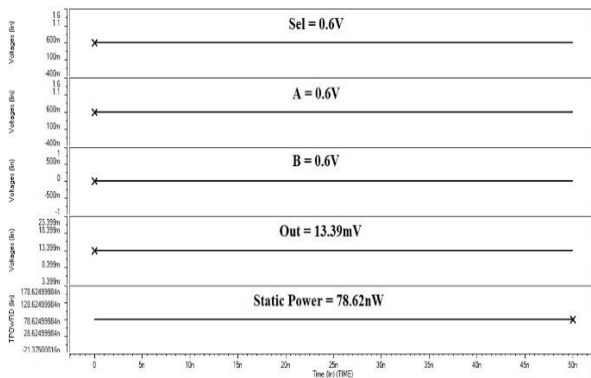
In GDI based Multiplexer static power dissipation at 0.8V is 60.79nW, if we reduce the supply to 0.6V and 0.4V then static power dissipation is 35.19nW and 15.08W respectively shown in Fig. 22 (a), (b), (c). Static power dissipation at 0.4V is 79.15% less than at 0.8V. Maximum power dissipation at 0.8V is 839.3nW, when we reduce the power supply to 0.6V then maximum power dissipation becomes 548.4nW, if we further reduce the power supply to 0.4V then power dissipation is 146.49nW. This analysis shows that power dissipation reduces when we reduce the supply voltage, here maximum power dissipation at 0.4V is 82.55% less than maximum power dissipation at 0.8V as shown in Fig. 22 (d), (e), (f). At 0.8V maximum power dissipation of MOSFET GDI based Multiplexer is 230.1uW, which is 274.15 times more than maximum power dissipation of FinFET GDI based Multiplexer at 0.8V. This analysis shows that parameters at 0.4V is far better than in compare to 0.8V.



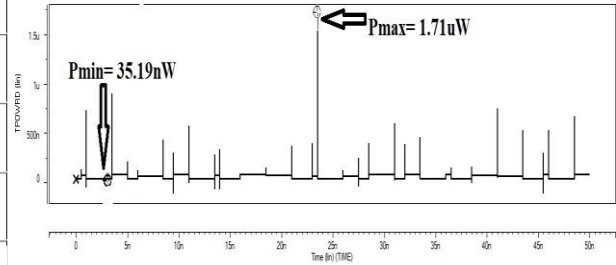
(a)



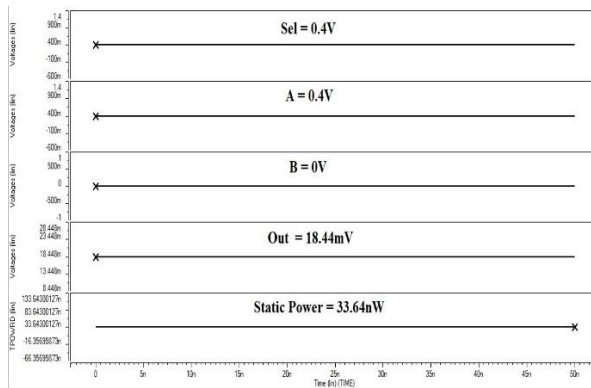
(d)



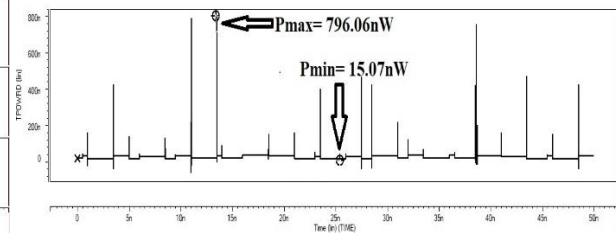
(b)



(e)



(c)



(f)

Fig. 5.4. Static Power Dissipation of PT based Multiplexer using FinFET at (a) $V_{dc}=0.8V$, (b) $V_{dc}=0.6V$ and (c) $V_{dc}=0.4V$. Total Power Dissipation of PT based Mux using FinFET at (d) $V_{dc}=0.8V$, (e) $V_{dc}=0.6V$ and (f) $V_{dc}=0.4V$.

Scaling in PT based Multiplexer will give the information about the variation in the static power dissipation also called leakage and change in total power dissipation. When supply voltage is high then power dissipation will be more as usual and when we reduce the supply voltage, it will reduce the power dissipation. At supply voltage 0.8V static power dissipation is 135.97nW shown in Fig. 23 (a) but when we reduce the supply to 0.6V it is 78.62nW Fig. 23 (b) and at 0.4V leakage is 33.64nW shown in Fig. 23 (c), which is 75.25% less than the static power dissipation at 0.8V supply voltage. Now the maximum power dissipation at 0.8V is 7.50uW shown in Fig. 23 (d), at 0.6V maximum power dissipation is 1.71uW shown in Fig. 23 (e) and at 0.4V it is 796.06nW shown in Fig. 23 (f), which is 83.38% less than maximum power

dissipation at 0.8V. Reduction in power supply reduces the dissipation power which will improve the performance of the device. This analysis states that device at 0.4V performs operation same as the device at 0.8V but it consumes less power.

5.4 SWITCHING OF THE SIGNALS

In devices there are any number of inputs and outputs which switches at different frequencies. If by any chance more than one input signals are switching at the same time then power dissipation will be more at that time. So, for better performance we should try to avoid that condition where more than one signal switches. Switching of the signal can lead to more power dissipation. This excess power dissipation can be eliminated by switching of the signal at different time instances.

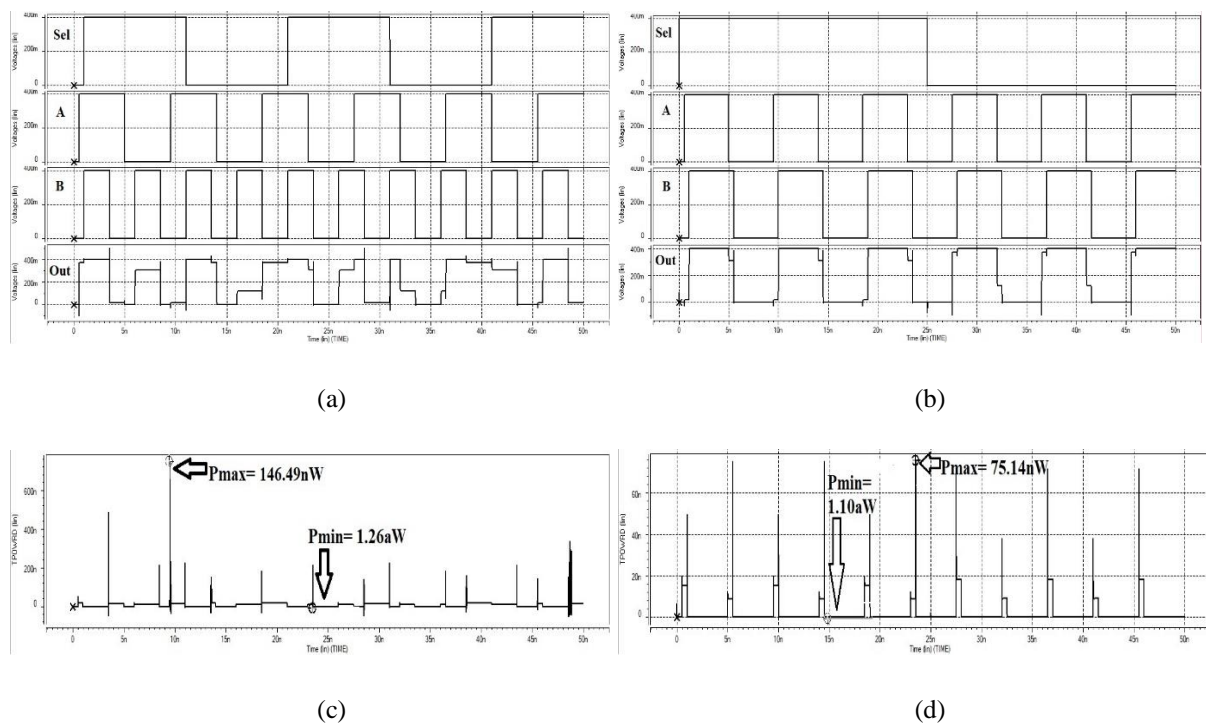


Fig. 5.5. FinFET GDI based Multiplexer (a) Output plot at Same Time Switching, (b) Output Plot at Different Time Switching, (c) Total Power Dissipation at Same Switching, (b) Total Power Dissipation at Different Time Switching.

Select signal and input signal are switching at the same time as shown in Fig. 24 (a) this causes a more power dissipation, maximum power dissipation at same time switching is 146.49nW as shown in Fig. 24 (c). when all the signals are switching at different time as shown in Fig. 24 (b), maximum power dissipation is 75.14uW as presented in Fig. 24 (d). Maximum power

dissipation at different time switching is 48.70% less than maximum power dissipation at same time switching.

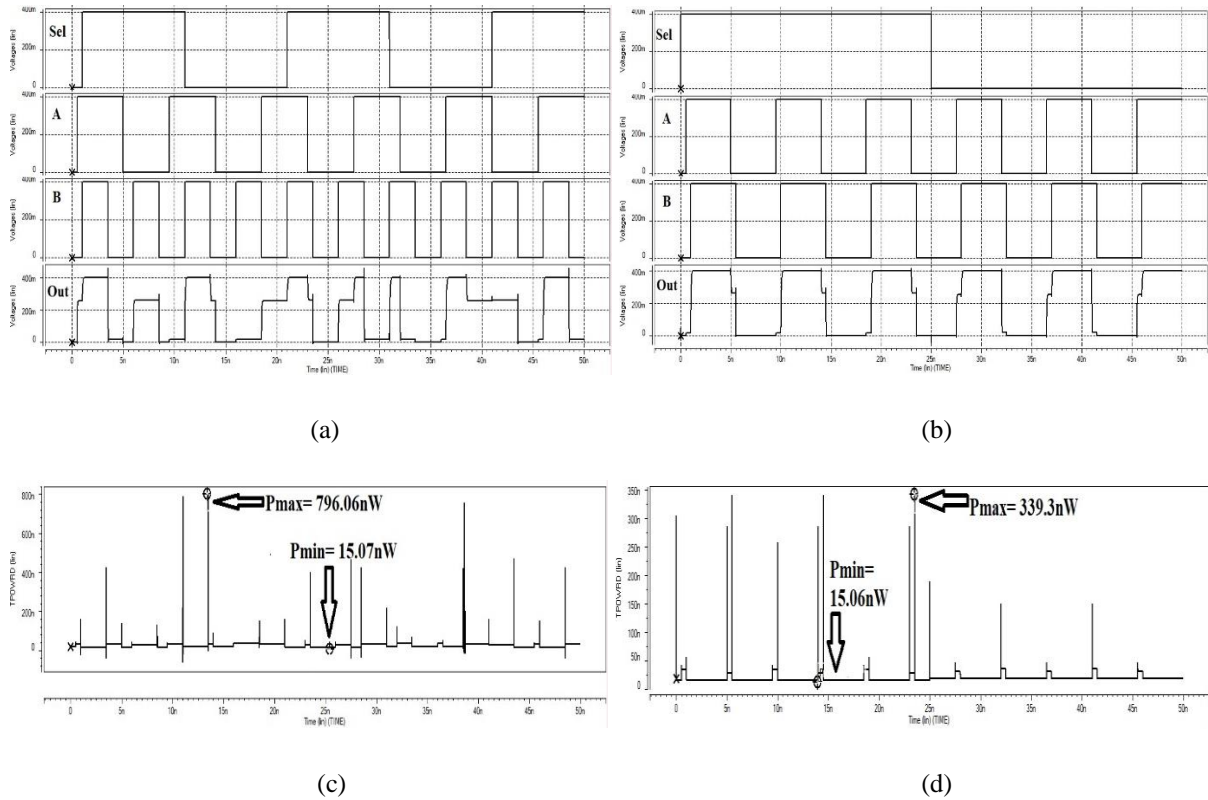


Fig. 5.6. FinFET PT based Multiplexer (a) Output plot at Same Time Switching, (b) Output Plot at Different Time Switching, (c) Total Power Dissipation at Same Switching, (d) Total Power Dissipation at Different Time Switching.

Switching of input signals at 0.4V power supply is shown in Fig. 25. In Fig. 25 (a) shows that select signal and input signal B both are switching at the same time, then power dissipation at that time is more. In Fig. 25 (b) all the signals are switching at different time leads to less power dissipation. When switching at same time, maximum power dissipation is 796.06nW as shown in Fig. 25 (c) but when signals are switching at different time then maximum power dissipation reduced to 339.3nW as shown in Fig. 25 (d). Maximum power dissipation at different switching is 57.37% less than the switching at same time.

IMPORTANT OUTCOMES:

- This section based on the analysis of multiplexers using FinFET at 10nm technology node. Analysis is done using HSPICE tool.
- In MOSFET based mux, GDI and PT were the best mux's, this mux is now designed with FinFET to improve the performance.
- Further scaling and switching analysis is also done to find at which supply and switching FinFET based mux will provide optimum performance.
- Analysis states that designing mux with FinFET, power dissipation is reduced significantly.
- It also improved the operating speed of the mux, delay of GDI based mux is 165.42 times less than PT based mux.

CHAPTER VI

UNIVERSAL 4-BIT BARREL SHIFTER

6.1 INTRODUCTION

Barrel shifter is a digital circuit which can perform shifting of data by specific number of bits. It can perform N-bit shifting of data in a single cycle. Barrel shifter is a logic device to perform many shift and rotate operations. Barrel shifters can be used in DSP. Some microprocessors use barrel shifter as a part of ALU in their design to provide fast and efficient shifting operation and many other devices. Some common use of universal barrel shifter is in hardware implementation of floating-point arithmetic. To add or subtract the floating-point number, the significands of the two numbers must be aligned for this shifting operation is required, changing the size of exponent until its matches to the larger number. This is accomplished by the subtracting the exponent number and shifting the smaller number by the difference, which is done by the barrel shifter in single cycle, on a contradictory simple shifter would take a greater number of cycles to shift the data.

Generally, two classification exist of the shifter first sequential shifter, which is called “The Shift Register” with usage of clock, such as SISO, SIPO, PIPO and PISO and another one is combinational shifter, which is called “Barrel Shifter” based entirely on combinational circuits such as multiplexers. Type of multiplexer is decided by the requirement, at how much bit’s operation is going to be performed. The normal size of the component design is (4,8,16... etc.) depends on the usage and requirements. Operations which can be performed by the barrel shifter are, Logical Right and Left Shift, Arithmetic Right and Left Shift, and Rotate Right and Left. In this section 4bit barrel shifter is designed using GDI and PT based multiplexer, which is already discussed in the earlier section.

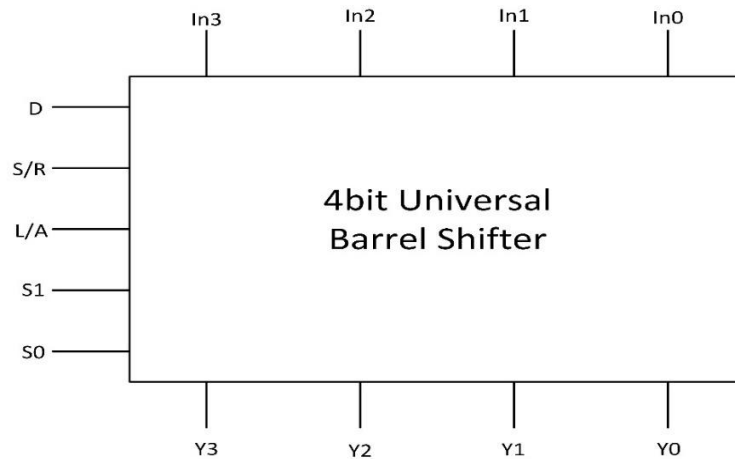


Fig. 6.1. Schematic of Barrel Shifter

Their Control signals:

1. Direction (D)
2. Shift or Rotate (SR)
3. Logical or Arithmetic (LA)
4. Select Signals (S1, S0) for 4-bit Barrel

Shifting operation depends on several control signals such as, D (Direction), where D=0 indicates all right shift and rotate operation and opposite when D=1. S/R (Shift or Rotate), when S/R=0, shift operation is going to be executed, on contrary rotate operation will perform when it is 1. L/A (Logical or Arithmetic), if L/A=0, point to Logical operation and if L/A=1 means Arithmetic operation will occur. S1 and So (Number of bits to be operate) are select signals, as depicted in the Fig. 26.

Barrel shifter performs 6 operations:

1. Shift Right Logical (SRL)
2. Shift Right Arithmetic (SRA)
3. Rotate Right (RR)
4. Shift Left Logical (SLL)
5. Shift Left Arithmetic (SLA)
6. Rotate Left (RL)

6.1.1 Shift Right Logical:

In this operation all the bits shift to the right. This operation is used to divide positive number by two. When control signal $D=S/R=L/A=0$, it indicates that only logical right shift operation will perform as illustrated in Table 8. Further if $S1=0$ and $S0=1$ then only one bit shifts to the right and zero is appended to the MSB. Similarly, for $S1, S0 =10$ and $S1, S0 =11$, two and three bits get shifted to the right, respectively as shown in Fig. 27.

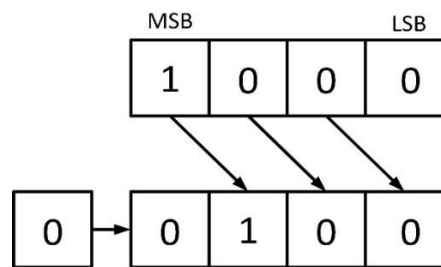


Fig. 6.2. Shift Right Logical 1-bit shift

For example, if input bit sequence is 1000 and $S1, S0 =01$, then output is 0100, similarly for other sequences. Shifting right by one bit indicates division by 2 as illustrated in the example, if input is 8 in decimal, then after one-bit right shift output is 4.

6.1.2 Shift Right Arithmetic:

Operation of this method is same as logical right operation but higher order region of the input is not filled with the zero. These bits are depending on the sign bits, the MSB of the data. As the last bit represents the sign of the data, so the last bit is filled by the sign bit, therefore sign of the data doesn't change. Arithmetic right shift is used to divide the signed data, which is not possible in the Shift Right Logical operation. When $D=S/R=0$ and $L/A=1$, then only Shift Right Arithmetic operation is going to perform. Further, if data selection bit is $S1=0$ and $S0=1$, then only one bit shifting will occur as demonstrated in the Fig. 28. MSB shows the sign of the data will remain same during shifting operation. Similarly, for $S1, S0 =10$ and $S1, S0 =11$, two and three bits get shifted to the right, respectively.

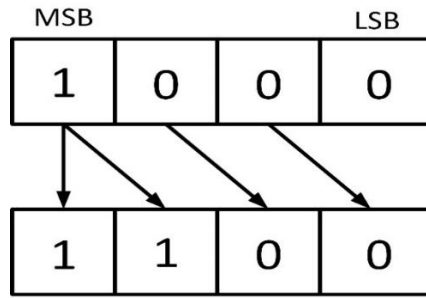


Fig. 6.3. Shift Right Arithmetic 1-bit shift

6.1.3 Rotate Right:

In this operation all the bit rotates in the right direction, with no loss of the data as demonstrated in Fig. 29. All the bits shift to the right and LSB of the data filled the MSB. This method is useful if it is essential to retain all the prevailing bits, which is frequently used in digital cryptography. When control signal $D=0$, $S/R=1$ and L/A can either be 0 or 1, this accomplishes the rotate right operation only. Further, if select signal is $S1, S0 = 00$, $S1, S0 = 01$, $S1, S0 = 10$ and $S1, S0 = 11$, then no operation, 1-bit, 2-bit and 3-bit rotate right operation will perform, respectively.

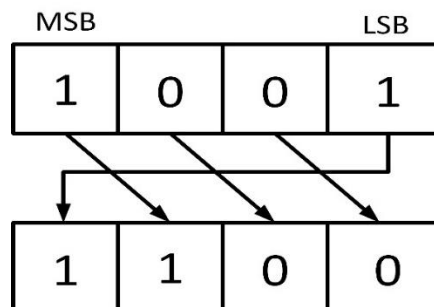


Fig. 6.4. Rotate Right by 1-bit

There is no blank space available because no shifting operation is performed here, then there is no need to place 0 at the MSB.

6.1.4 Shift Left Logical:

This operation is similar to the right shift operation, rather than shifting right, bits gets shifted to the left. While shifting bits to the left, 0 is padded to the LSB of the data as depicted in the Fig. 30. This operation performs the multiplication by 2, while shifting data by 1-bit. To perform Shift Left Logical operation set the control signal to, $D=1$, $S/R=L/A=0$. Now, if $S1$, $S0$ are 00, 01, 10 and 11, then no shift, 1-bit, 2-bit and 3-bit shifts respectively. For example, if input is 1001, then after 2-bit shifting operation output is 0100, here two 0 is padded to the side of lower bits.

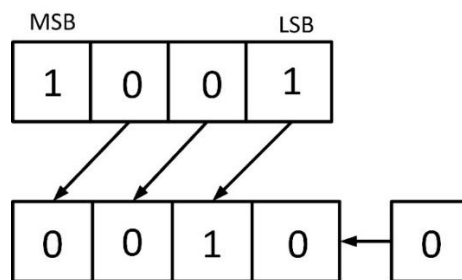


Fig. 6.5. Shift Left Logical 1-bit shift

6.1.5 Shift Left Arithmetic:

This operation also shifts the data to the left and 0 is padded to the lower bit side but MSB of the data retain its place to maintain the sign of the data. As MSB of the data represent then sign, then last bit of higher bits remains unchanged, while performing shifting operation as illustrated in the Fig. 31. Shift Right Arithmetic performs multiplication operation on the signed data. For this operation control signal should be $D=L/A=1$ and $S/R=0$, however if select signal $S1$, $S0$ is 00 then there is no shifting operation, while for 01 ,10 and 11 then 1-bit, 2-bit and 3-bit shifts to left respectively.

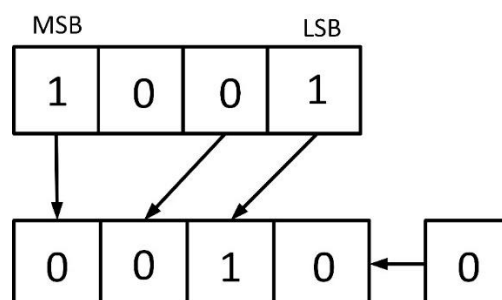


Fig. 6.6. Shift Left Arithmetic 1-bit shift

6.1.6 Rotate Left:

This is also a rotating operation, which performs the rotation in left direction. There is no requirement of 0 padding because blank space of LSB is filled by the MSB and no bit lost in this operation as demonstrated in the Fig. 32. For rotating of the data control signal is $D=S/R=1$ and L/A can either be 0 or 1. There is no shifting for $S1=S0=0$, but for $S1, S0= 01, 10$ and 11 , 1-bit, 2-bit and 3-bit rotate to the left.

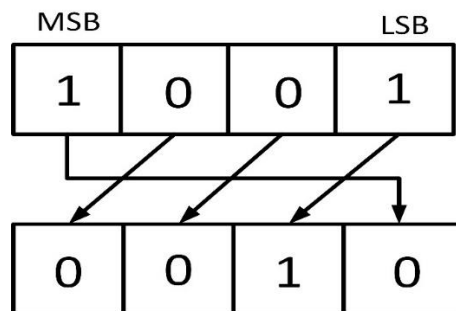


Fig. 6.7. Rotate Left by 1-bit

There are total 6 operations which can be performed using universal barrel shifter. Table 8 shows all the operation with their control signals. Control signals are $D, S/R$ and L/A and select signals are $S1$ and $S0$, these control signals decide which operation should perform and select signal decides the number of bits two be performed. Whereas Table 9 illustrate the list of all the operations and Table 10 shows the example of all shifting and rotating operation.

Table 6.1: Truth Table of Barrel Shifter

OPERATION	D	S/R	L/A	S1	S0	Y3	Y2	Y1	Y0
SHIFT RIGHT LOGICAL	0	0	0	0	0	I3	I2	I1	I0
	0	0	0	0	1	0	I3	I2	I1
	0	0	0	1	0	0	0	I3	I2
	0	0	0	1	1	0	0	0	I3
SHIFT RIGHT ARITHMETIC	0	0	1	0	0	I3	I2	I1	I0
	0	0	1	0	1	I3	I3	I2	I1
	0	0	1	1	0	I3	I3	I3	I2
	0	0	1	1	1	I3	I3	I3	I3
ROTATE RIGHT	0	1	X	0	0	I3	I2	I1	I0
	0	1	X	0	1	I0	I3	I2	I1
	0	1	X	1	0	I1	I0	I3	I2
	0	1	X	1	1	I2	I1	I0	I3
SHIFT LEFT LOGICAL	1	0	0	0	0	I3	I2	I1	I0
	1	0	0	0	1	I2	I1	I0	0
	1	0	0	1	0	I1	I0	0	0
	1	0	0	1	1	I0	0	0	0

SHIFT LEFT ARITHMETIC	1	0	1	0	0	I3	I2	I1	I0
	1	0	1	0	1	I3	I1	I0	0
	1	0	1	1	0	I3	I0	0	0
	1	0	1	1	1	I3	0	0	0
ROTATE LEFT	1	1	X	0	0	I3	I2	I1	I0
	1	1	X	0	1	I2	I1	I0	I3
	1	1	X	1	0	I1	I0	I3	I2
	1	1	X	1	1	I0	I3	I2	I1

Table 6.2: List of all the Operations

OPERATION	D	S/R	L/A
Shift Right Logical	0	0	0
Shift Right Arithmetic	0	0	1
Rotate Right	0	1	X
Shift Left Logical	1	0	0
Shift Left Arithmetic	1	0	1
Rotate Left	1	1	X

Table 6.3. Example of all Operations

	D	SR	LA	S1	S0	I3	I2	I1	I0
	0	0	0	0	0	1	0	1	1
SRL	0	0	0	0	1	0	1	0	1
SRA	0	0	1	0	1	1	1	0	1
RR	0	1	X	0	1	1	1	0	1
SLL	1	0	0	0	1	0	1	1	0
SLA	1	0	1	0	1	1	1	1	0
RL	1	1	X	0	1	0	1	1	1

In above Table 9 initial input is input is 1011 and control signals D, SR and L, and select signal S1 and S0 is 0,0,0,0 and 0 respectively. For one-bit shifting operation select signal is set to S1=0 and S0=1. Further if, control signal D, SR, LA= 000 and 001, then SRL and SRA operation will occur which will give the output 0101 and 1101 respectively. When D, SR, LA= 01X (where X indicates either 0 or 1), then RR operation is done gives the output 1101. Now if, D, SR, LA= 100, 101 and 11X, then SLL, SLA and RL operation provides the output 0110, 1110 and 0111 respectively.

6.2 DESIGNING OF UNIVERSAL 4-BIT BARREL SHIFTER

Multiplexer which is a basic entity for designing the barrel shifter, uses single cycle to perform any shifting operation. In this section two type of Mux is used, PT based Mux and GDI based Mux, these two multiplexers demonstrate the better performance compared to other multiplexers as discussed in earlier section. Universal Barrel Shifter is designed using 32x1 Multiplexer shown in Fig. 33 and schematic is illustrated in Fig. 34. There are 3 control signal and 2 select signal, therefore 32 combination is possible as illustrated in the Table 8. All the designing is done at 90nm technology node using cadence virtuoso software at 0.6V supply voltage. Further Delay and power are analysed for both the barrel shifter to discover which gives the better performance. Basic circuit design of barrel shifter is similar for both, which requires four 32x1 Multiplexers as there are 4 outputs demonstrated in Fig. 35. Each mux will provide single output according to the control signal and select signals.

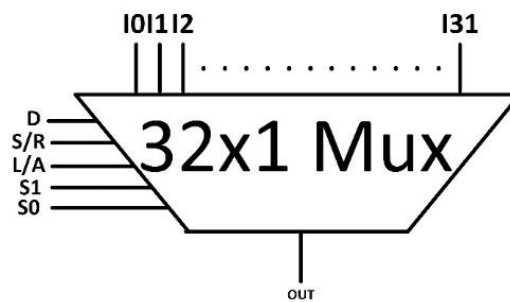


Fig. 6.8. 32x1 Multiplexer

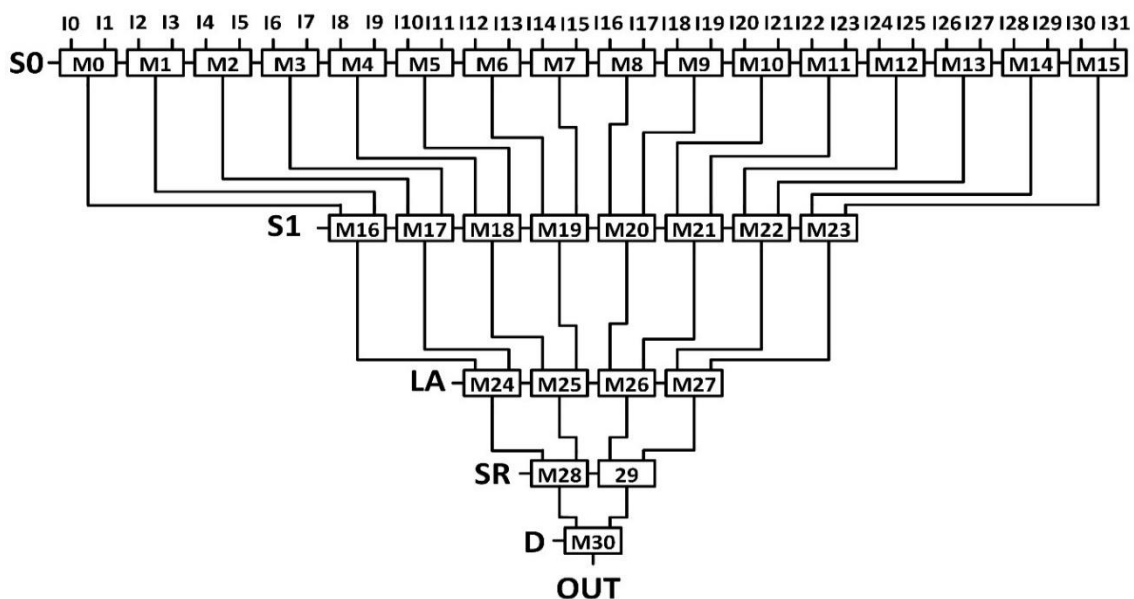


Fig. 6.9. Schematic 32x1 Multiplexer

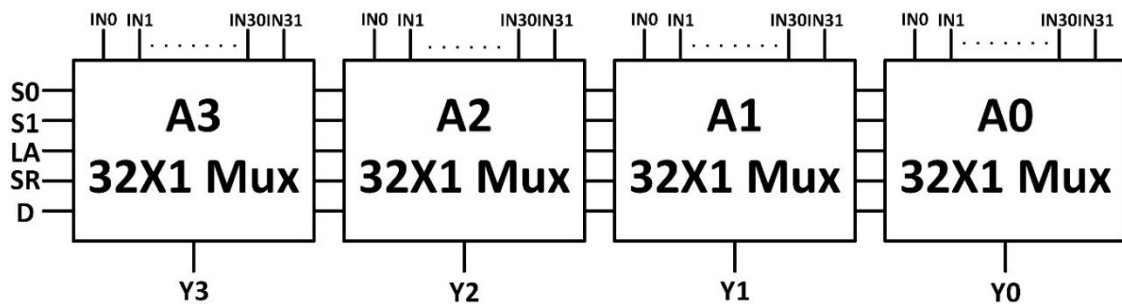


Fig. 6.10. Schematic of Universal 4-bit Barrel Shifter

In 32x1 Mux, inputs IN0, IN1, IN2 and IN3 are connected to 32 inputs of for multiplexers are illustrated in Table 11.

Table 6.4: Connections of inputs in barrel shifter

32x1 Mux	Barrel Shifter inputs	32x1 Mux input pins
A0	IN0	0, 4, 8, 12, 16, 20, 24, 28
	IN1	1, 5, 9, 13, 27, 31
	IN2	2, 6, 10, 14, 26, 30
	IN3	3, 7, 11, 15, 25, 29
	Gnd	17, 18, 19, 21, 22, 23
A1	IN0	3, 11, 15, 17, 21, 25, 29
	IN1	0, 4, 8, 12, 16, 20, 24, 28
	IN2	1, 5, 9, 13, 27, 31
	IN3	2, 6, 7, 10, 14, 26, 30
	Gnd	18, 19, 22, 23
A2	IN0	10, 14, 18, 22, 26, 30
	IN1	11, 15, 17, 21, 25, 29
	IN2	0, 4, 8, 12, 16, 20, 24, 28
	IN3	1, 5, 6, 7, 9, 13, 27, 31
	Gnd	2, 3, 19, 23
A3	IN0	9, 13, 19, 27, 31
	IN1	10, 14, 18, 26, 30
	IN2	11, 15, 17, 25, 29
	IN3	0, 4, 5, 6, 7, 8, 12, 16, 20, 21, 22, 23, 24, 28
	Gnd	1, 2, 3

There are 32 inputs from I0 to I31 and 5 select signals, where D, S/R and L/A are the control signal to decide which operation should perform and S1 and S0 are the select signal to decide how many bits is required to shift. All the simulation is done at input I3, I2, I1, I0= 1011 and on fixed timing values as illustrated in Table 12.

Table 6.5: Timing Values

	D	SR	LA
Period	30ns	15ns	15ns
Delay	0	10ns	5ns
Duty Cycle	15ns	5ns	5ns

6.2.1 Universal 4-bit Barrel Shifter using PT based Mux:

Construction of barrel shifter is done using four 32x1 multiplexers as shown in Fig. 36, and these multiplexers are designed using Pass Transistor Logic (PTL), which is already covered in the previous section II. Thirty-one 2x1 PT based Mux is required to design 32x1 multiplexer and four 32x1 multiplexer is used to design universal 4-bit Barrel shifter. Connection on inputs in 32x1 multiplexers is done using Barrel Shifter Truth Table shown in Table 8. Schematic design of Universal 4-bit PT based Barrel shifter is illustrate in Fig. 36. There are four inputs I3, I2, I1 and I0 with four outputs Y3, Y2, Y1 and Y0.

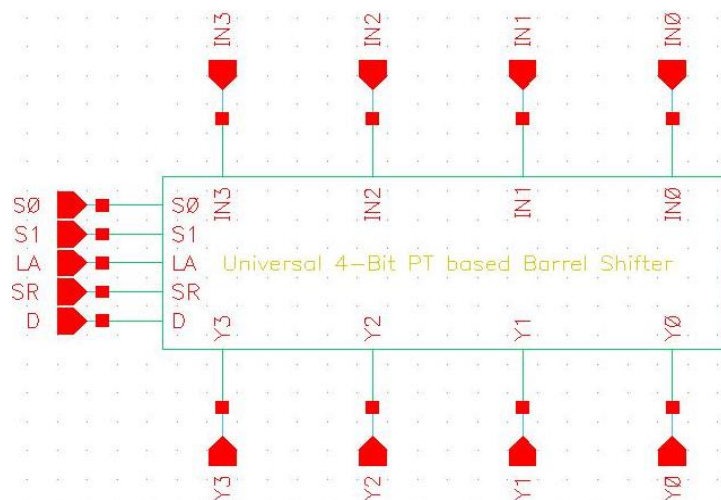


Fig. 6.11. Schematic of Universal 4-bit PT based Barrel Shifter

There are three control signals D, S/R and L/A, which will decide the type of operation like (SRL) Shift Right Logical, SRA (Shift Right Arithmetic), RR (Rotate Right), SLL (Shift Left Logical), SLA (Shift Left Arithmetic) and RL (Rotate Left) and two select signals S0 and S1, by which we will decide how much bits to be shift from 1 bit to 3 bit. If S1, S0= 01, then one-bit shifting operation will occur.

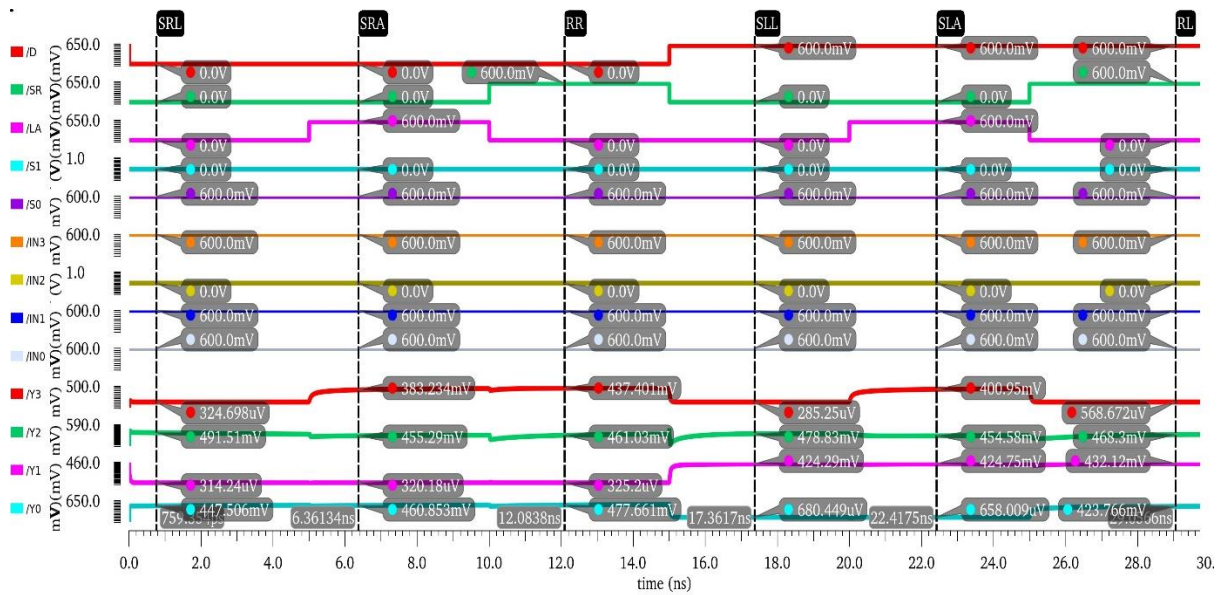


Fig. 6.12. Outputs of Universal 4-bit PT based Barrel Shifter

After simulation of Barrel Shifter, output of all the operation is demonstrated in Fig 37, which clearly shows the SRL, SRA, RR, SLL, SLA and RL operations, where input is fixed to 1011. However, when all the control signal with select signal is D, SR, LA, S1, S0= 00001, the output $Y_3= 324.69\mu\text{V}$, $Y_2=491.5\text{mV}$, $Y_1=314.24\mu\text{V}$ and $Y_0=447.506\text{mV}$, which is clearly 0101 performing the Logical Right Shift operation (SRL). When D, SR, LA, S1, S0= 00101, then output is $Y_3= 383.23\text{mV}$, $Y_2=455.29\text{mV}$, $Y_1=320.18\mu\text{V}$ and $Y_0=460.85\text{mV}$, indicates 1101, which is Arithmetic Right Shift operation (SRA). For Right Rotate (RR) Operation signals are D, SR, LA, S1, S0= 01001, this will rotate the input to the right with 1101 and provides the output $Y_3= 437.4\text{mV}$, $Y_2=461.03\text{mV}$, $Y_1=325.2\mu\text{V}$ and $Y_0=477.66\text{mV}$. Signal D, SR, LA, S1, S0= 00101, performs the Logical Left Shift Operation (SLL) delivers the output $Y_3= 285.25\mu\text{V}$, $Y_2=478.83\text{mV}$, $Y_1=424.29\text{mV}$ and $Y_0=680.449\mu\text{V}$, which is 0110. Shift Left Arithmetic (SLA) operation is done by signal D, SR, LA, S1, S0= 10101, provides 1110. So, the output of this operation is $Y_3= 400.95\text{mV}$, $Y_2=454.58\text{mV}$, $Y_1=424.75\text{mV}$ and $Y_0=658.009\mu\text{V}$. To perform the Rotate Left operation signals ought to be D, SR, LA, S1, S0=11001 passes the output 0111, which is $Y_3= 568.67\mu\text{V}$, $Y_2=468.3\text{mV}$, $Y_1=432.12\text{mV}$ and $Y_0=423.76\text{mV}$. This analysis shows that all the operations are working correctly and providing right output.

6.2.2 Universal 4-Bit Barrel Shifter using GDI based Mux:

The behaviour of this shifter is same as previous one. It also performs all the operations. GDI logic based 2x1 multiplexer is used to design this barrel shifter and 32x1 multiplexer is constructed by this GDI based multiplexer, which is covered in section II. Number of transistors used in GDI based multiplexer is less than PT based multiplexer, therefore less area will be covered in this multiplexer. Fig. 38 present the schematic of universal 4-bit GDI based Barrel Shifter.

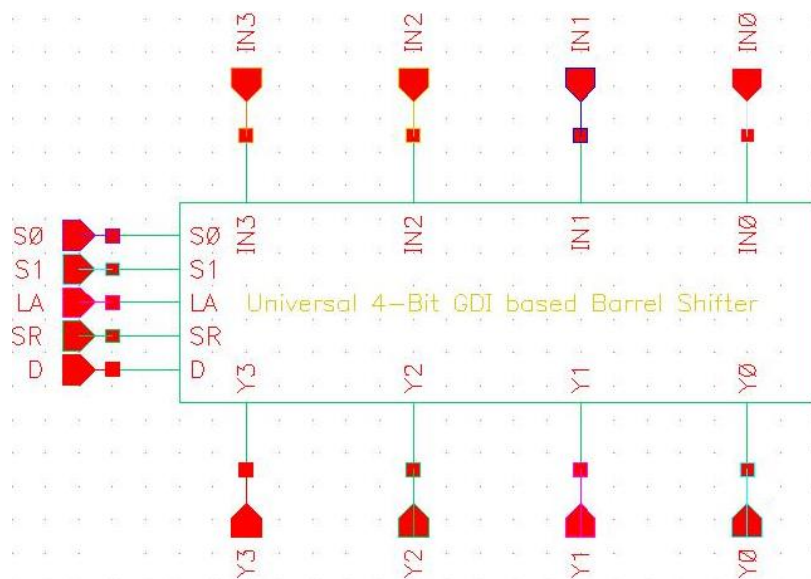


Fig. 6.13. Universal 4-bit GDI based Barrel Shifter

Difference in both GDI and PT based multiplexer causes variation in the output. In this GDI based universal 4-bit Barrel shifter output of all the operations with their control and select signal are depicted in Fig. 39.

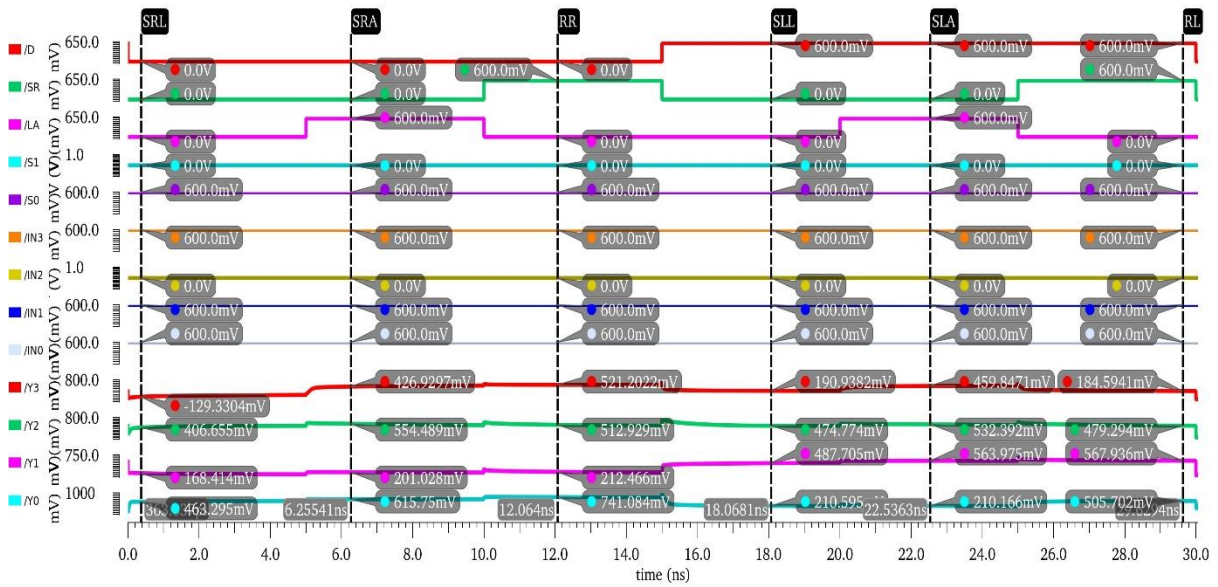
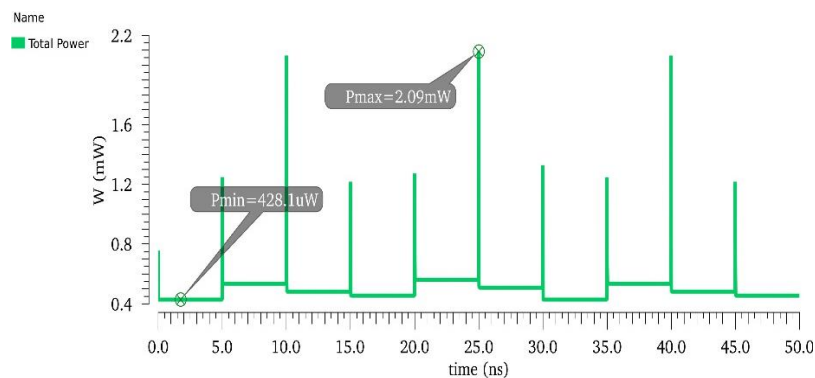


Fig. 6.14. Output of Universal 4-bit GDI based Barrel Shifter

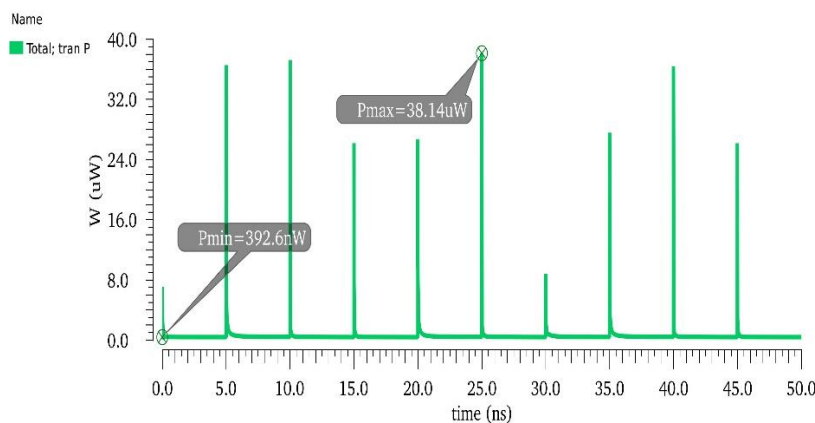
Simulation successfully depicted the output of all operations, where input is fixed to 1011. First all the right shift and rotate operation 0 is given to the D, which specifies right direction. When control signals are D, SR, LA, S1, S0= 00001, leads to shift right logical operation gives 0101 with output Y3= -129.33mV, Y2=406.65mV, Y1=168.414mV and Y0=463.29mV. Shift Right Arithmetic operation is done when, control signals are D, SR, LA, S1, S0= 00101, provides output Y3= 426.92mV, Y2=554.48mV, Y1=201.02mV and Y0=615.75mV, which is 1101 in logic form. Control signal D, SR, LA, S1, S0= 00011, performs the Rotate Right operation offers 1101 with output Y3= 521.20mV, Y2=512.92mV, Y1=212.46mV and Y0=741.08mV. Now, for the left shift and rotate operation control signal D is set to 1, which indicates left direction. Further if control signals D, SR, LA, S1, S0= 10001, shows the logical shifting in left direction, gives the output 0110 with values Y3=190.93mV, Y2=474.77mV, Y1=487.7mV and Y0=210.59mV. Arithmetic left shifting operation is done with control signals D, SR, LA, S1, S0=10101, where output is Y3=459.84mV, Y2=532.39mV, Y1=563.97mV and Y0=210.16mV. Further if control signal is D, SR, LA, S1, S0= 11001, Rotate left operation will perform, which provides the output 0111 and output values are Y3=184.59mV, Y2=479.29mV, Y1=567.93mV and Y0=505.7mV.

6.2.3 Delay and Power Analysis

This section illustrates the delay and power of the universal 4-bit Barrel Shifter. Delay depends on the time taken by the input signal to reach the output. Maximum, minimum and average power dissipation, PDP power delay product is also examined. For better performance power dissipation should be less as much as possible without degradation of output. In some design's user prioritize PDP to analyse the performance of the design. Fig. 40 displays the Total power dissipation of Universal 4-bit barrel shifter using PT and GDI based



(a)



(b)

Fig. 6.15. Total Power Dissipation of Universal 4-bit Barrel Shifter using (a) PT based multiplexer, (b) GDI based Multiplexer

After analysing the power dissipation of the circuit, it is clear the both barrel shifter has different value of power dissipation as illustrated in Table 13. In both of them GDI based Barrel

Shifter possess less power dissipation. Maximum power dissipation of GDI based Barrel shifter is 38.14uW, which is 98.71% less then PT based Barrel Shifter. Whereas minimum power dissipation is 392.6mW, 917 times more than PT based Barrel Shifter. Further average power dissipation is 509.3nW, 957.5 lesser than PT based Barrel Shifter.

Table 6.6: Total Power Dissipation of Universal 4-bit PT and GDI based Barrel Shifter

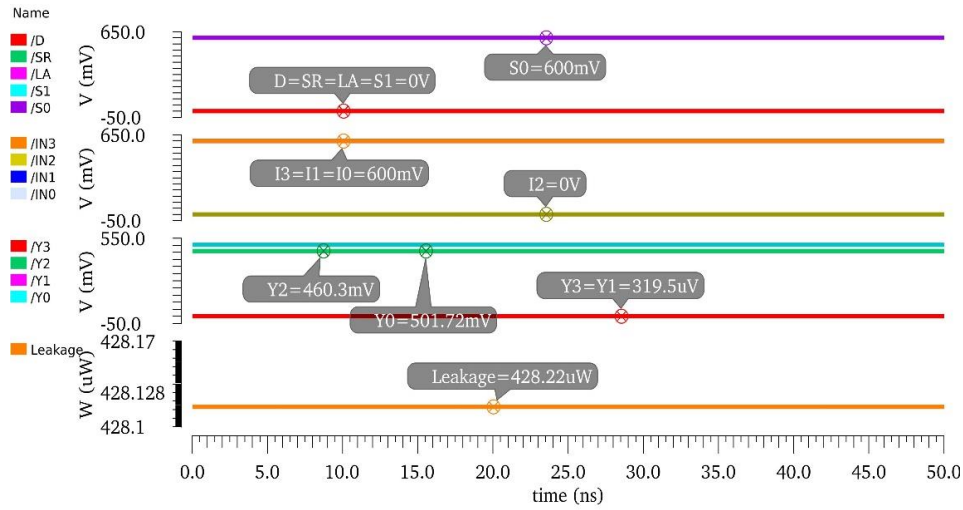
Universal 4-bit Barrel Shifter using	Power		Average Power
	Max	Min	
PT Based Mux	2.09mW	428.1uW	487.7uW
GDI Based Mux	38.14uW	392.6nW	509.3nW

Delay is a very important factor to analyse the performance of the design. In today's scenario research is growing to increase the speed of the device with less power dissipation. In many devices like DSP, microprocessors, ALU Barrel shifter is used to shift and rotate the data. Fast barrel shifter increases the performance of the design. Input signal in the PT based Universal 4-bit Barrel shifter takes 186ps to reach to the output which is 60.9ps higher than GDI based Barrel Shifter as demonstrated in the Table 14.

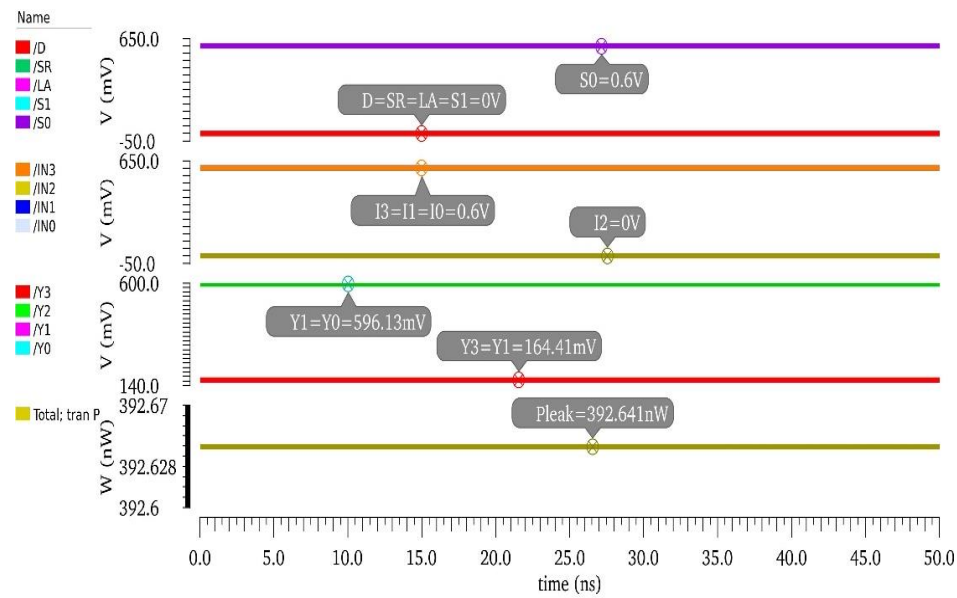
Table 6.7: Delay, Average, PDP and Static Power Dissipation

Universal 4-bit Barrel Shifter using	Delay (s)	Average Power	PDP (J)	Static Power Dissipation
PT Based Mux	186p	487.7uW	90712.2a	428.22uW
GDI Based Mux	125.1p	509.3nW	63.7a	392.64nW

There is another essential analysis called Power Delay Product (PDP), which is the multiplication of delay of the signal and power dissipation. Here GDI based Universal 4-bit Barrel Shifter shows the better power delay product 63.7aJ, which is 1424.0 times less than PT based Universal 4-bit Barrel Shifter.



(a)



(b)

Fig. 6.16. Static Power Dissipation of Universal 4-bit (a) PT, (b) GDI based Barrel Shifter

Static Power dissipation of any circuit is a very significant to analyse, it should be minimum to avoid the unnecessary power dissipation when device is not working. In the GDI based Barrel shifter static power dissipation is 392.64nW, which is 1090.5 times lower than the PT based Barrel Shifter as illustrated in the Fig. 41.

6.3 UNIVERSAL 4-BIT BARREL SHIFTER USING FINFET

This section illustrates the designing and simulation universal 4-bit barrel shifter using FinFET model at 10nm technology node with 0.4V power supply. Basic cell of this barrel shifter is 2x1 multiplexer, therefore GDI and PT based multiplexer is used to design barrel shifter. These GDI and PT based multiplexer shows the optimum performance compare to all other multiplexers which has already analysed in previous sections. The basic schematic of the barrel shifter is same as the MOSFET based barrel shifter.

6.3.1 Universal 4-bit GDI based Barrel Shifter:

Designing of this barrel shifter is done using GDI based multiplexer, which is the finest in compare to all other multiplexer. As illustrated in earlier sections, GDI Mux consist only two transistors n-type and p-type therefore less area will be required to design this universal barrel shifter. Schematic of this Barrel shifter is shown in Fig. 42.

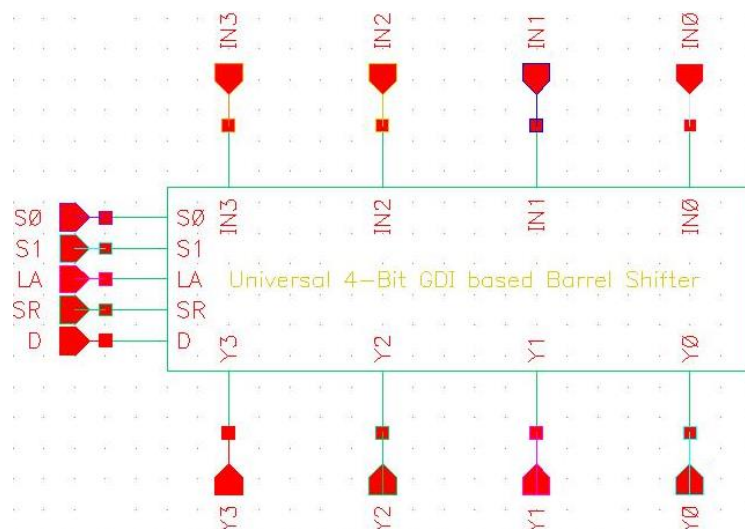
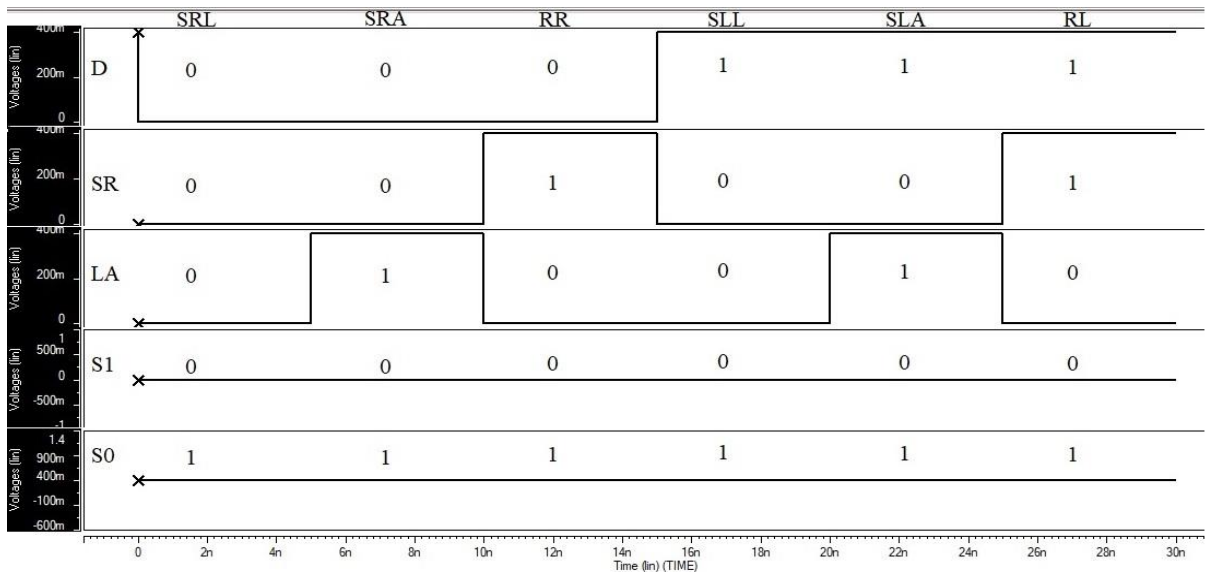
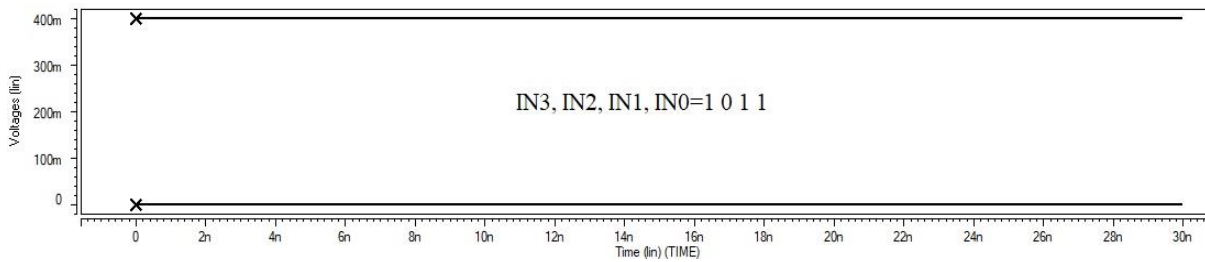


Fig. 6.17. FinFET based Universal 4-bit Barrel Shifter

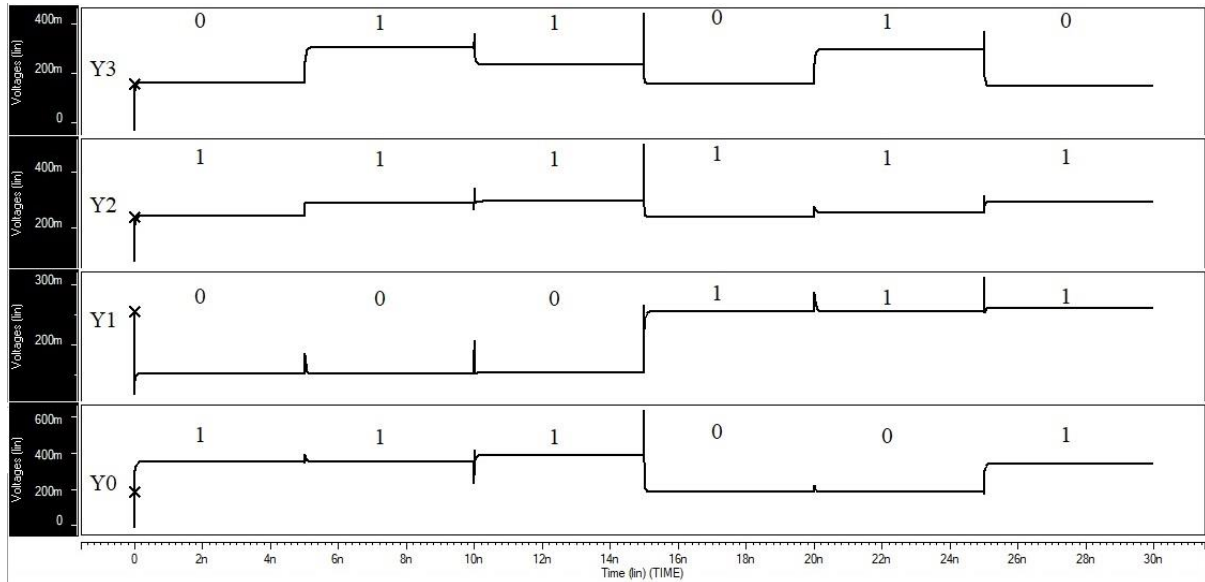
Output of this shifter is analysed while all the control signals are changing as shown in Table 8 and select signals are S1, S0= 01 indicates 1-bit operation. Fig. 43 demonstrate the output plot with all the operations SRL, SRA, RR, SLR, SLA and RL.



(a)



(b)



(c)

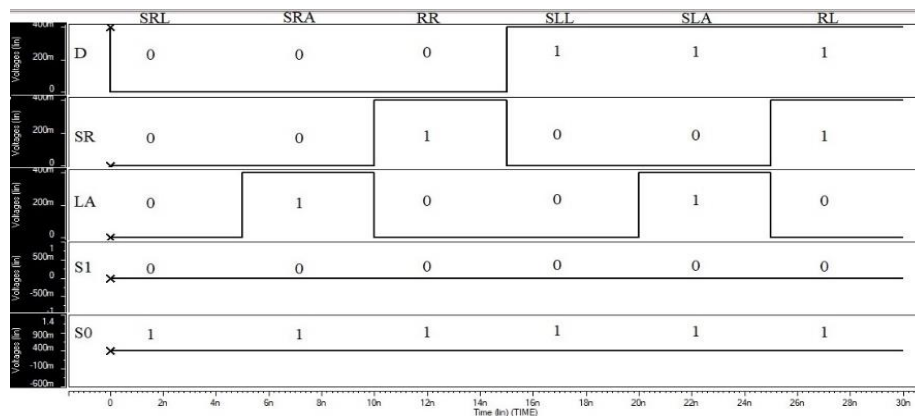
Fig. 6.18. Output plot of GDI based Universal 4-bit Barrel Shifter

Fig. 43 (a), is the plot of all the control signal with select signal and Fig. 43 (b) shows the input used in the barrel shifter which is IN3, IN2, IN1, IN0= 1011. Whereas Fig. 43 (c) illustrates the output. When control signals are D, SR, LA, S1, S0= 00001, indicate the SRL (Shift Right Logical) operation, provides the output 0101. If D, SR, LA, S1, S0 is 00101, then SRA (Shift Right Arithmetic) operation is going to perform giving output Y3, Y2, Y1, Y0= 1101, Shifting right by one bit and appending 1 at the MSB of the data. At control signal D, SR, LA, S1, S0= 01001, which is the RR (Rotate Right) operation therefore, output Y3, Y2, Y1, Y0 is 1101. D, SR, LA, S1, S0= 10001, performs the Shift Left Logical operation by one bit and the output is Y3, Y2, Y1, Y0= 0110, removing the MSB and shifting the data left by one bit. To perform the SLA (Shift Left Arithmetic) operation control signals are D, SR, LA, S1, S0= 10101, where data is shifted by one bit to left and placing the one at the MSB, delivers the output Y3, Y2, Y1, Y0= 1110. In the RL (Rotate Left) operation 4-bit data is shifted to the left and LSB is replaced by the bit of MSB. Control signal used for this operation is D, SR, LA, S1, S0= 11001, presents the output Y3, Y2, Y1, Y0= 0111.

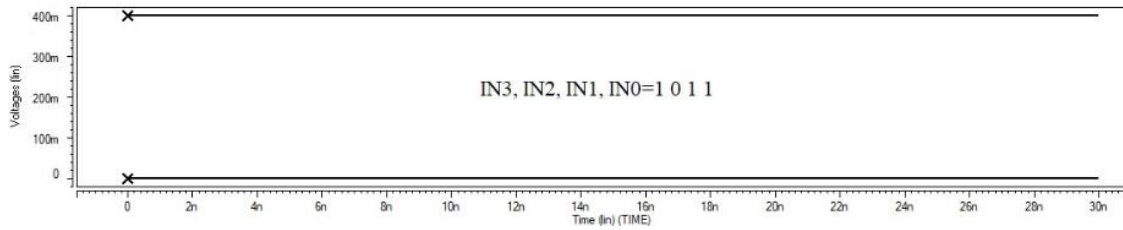
6.3.2 Universal 4-bit PT based Barrel Shifter:

Operation and designing of Universal Barrel Shifter using PT based multiplexer is same as GDI based universal barrel shifter. However, GDI based Multiplexer shows better performance in term of delay and power compare to PT based multiplexer and also it requires more transistors to perform the operation.

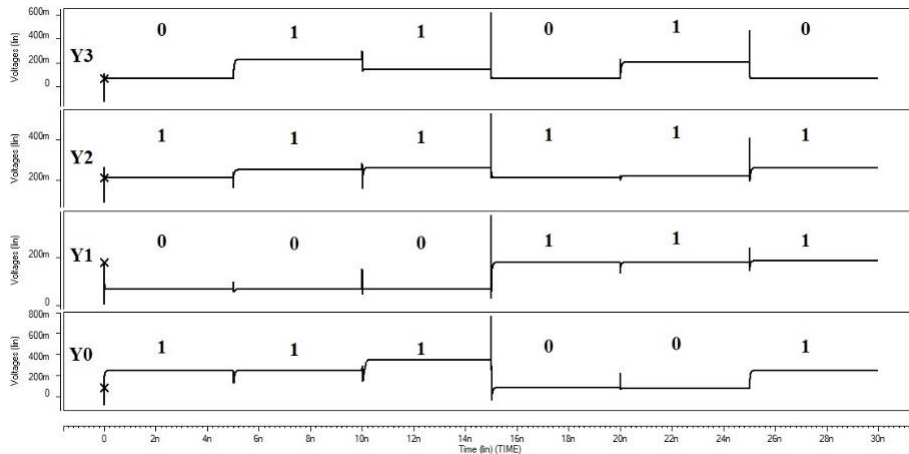
Output of this PT based universal barrel is shown in Fig. 44, where all the control signal changing according to the Table 8. Select signals are S1, S0 = 0, 1 and inputs are I3, I2, I1, I0 = 1, 0, 1, 1, this perform all the SRL, SRA, RR, SLL, SLA and RL operations as illustrated in Fig 44.



(a)



(b)



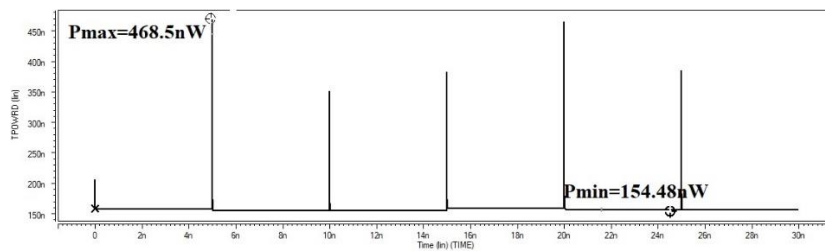
(c)

Fig. 6.19. Output plot of PT based Universal 4-bit Barrel Shifter

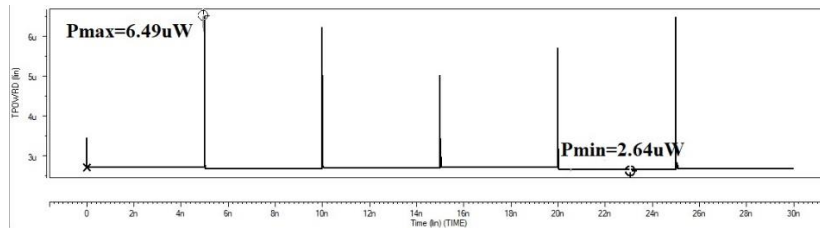
Output plot is depicted in the Fig. 44, whereas all the control and select signals D, SR, LA, S1, S0= 00001, are shown in Fig. 44 (a). In Fig. 44 (b) the inputs IN3, IN2, IN1, IN0= 1011 of the barrel shifter are illustrated. Fig. 44 (c) illustrates the output. SRL operation is performed when control signals are D, SR, LA, S1, S0= 00001 which provides the output 0101. If D, SR, LA, S1, S0 is 00101, indicates the SRA (Shift Right Arithmetic) operation and output Y3, Y2, Y1, Y0= 1101. At D, SR, LA, S1, S0= 01001, RR (Rotate Right) operation will perform therefore, output Y3, Y2, Y1, Y0 is 1101. D, SR, LA, S1, S0= 10001, performs the Shift Left Logical operation by one bit and the output is Y3, Y2, Y1, Y0= 0110, removing the MSB and shifting the data left by one bit. To perform the SLA (Shift Left Arithmetic) operation control signals are D, SR, LA, S1, S0= 10101, where data is shifted by one bit to left and placing the one at the MSB, delivers the output Y3, Y2, Y1, Y0= 1110. In the RL (Rotate Left) operation 4-bit data is shifted to the left and LSB is replaced by the bit of MSB. Control signal used for this operation is D, SR, LA, S1, S0= 11001, presents the output Y3, Y2, Y1, Y0= 0111.

6.3.3 Delay and Power Analyses

This section illustrates the delay and power analyses with both static and dynamic power dissipation of this GDI based universal 4-bit barrel shifter. Designer aims for the better performance in terms of all three factors, Area, Power and Delay. Multiplexer used in this barrel shifter consumes very less area therefor will consume minimal area for designing barrel shifter compare to others. Less number of transistors means less switching operation will perform which leads to less power dissipation. Further it provides the fast operation. Fig. 45 shows the Total power dissipation plot with maximum and minimum power dissipation.



(a)



(b)

Fig. 6.20. Total Power Dissipation of (a) GDI based and (b) PT based Universal 4-bit Barrel Shifter

FinFET based Universal 4-bit barrel shifter using GDI Mux dissipates 468.5nW maximum power dissipation which is 98.77% less than MOSFET based Barrel shifter using GDI Mux, whereas minimum power dissipation is 2.64uW, which is also less than 2.54 times less than minimum power dissipation of MOSFET based barrel shifter using GDI mux as demonstrated in Fig. 45 (a). Average power dissipation of this FinFET based barrel shifter is 156.55nW, 69.26% a lesser amount than MOSFET based Barrel shifter.

In PT based universal barrel shifter a greater number of transistors is used to perform the same operation. Due to larger number of transistor dynamic power dissipation when inputs are changing and static power dissipation when inputs are stable will be more compare to GDI based universal barrel shifter. Maximum power dissipation of PT based barrel shifter is 6.45uW

as depicted in Fig. 45 (b) which is 13.85 times more than maximum power dissipation of GDI based barrel shifter and Minimum power dissipation is 2.64uW, 17.08 times more than minimum power dissipation of GDI based barrel shifter. Whereas average power dissipation is 2.68uW, 17.11 times more than GDI based barrel shifter as illustrated in Table 15.

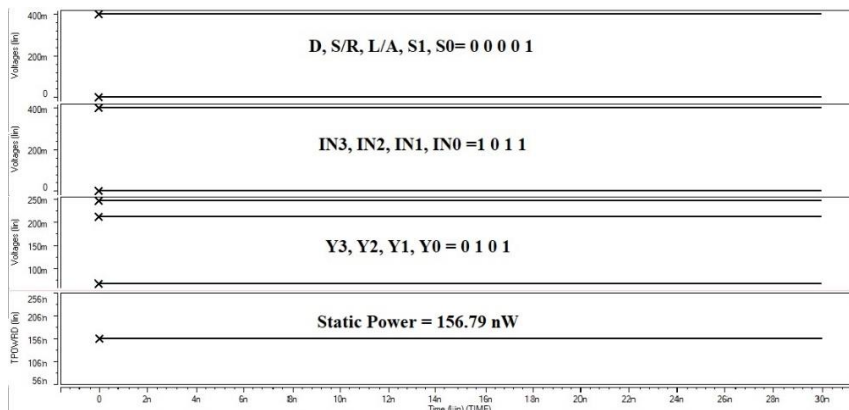
Table 6.8: Total Power Dissipation of Universal 4-bit PT and GDI based Barrel Shifter

Universal 4-bit Barrel Shifter	Power		Average Power
	Max	Min	
PT Mux	6.49uW	2.64uW	2.68uW
GDI Mux	468.5nW	154.48nW	156.55nW

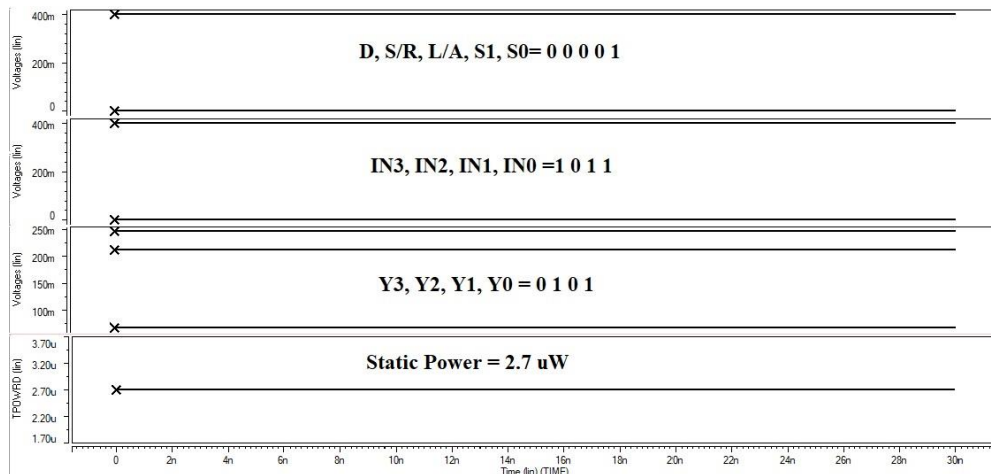
Delay of any design will provide the information that how much time the circuit will take to perform the complete operation, time to pass the input to the output. Less number of transistors will take less time to pass the input to the output, so as in GDI based barrel shifter a smaller number of transistors used to operate, therefore the delay of GDI based barrel shifter is 47.27ps which is 15.23ps less than PT based barrel shifter. Delay and Power values are demonstrated in Table 16.

Table 6.9: Delay, Average, PDP and Static Power Dissipation

Universal 4-bit Barrel Shifter	Delay (s)	Average Power	PDP (J)	Static Power Dissipation
PT Mux	62.5p	2.68uW	167.5a	2.7uW
GDI Mux	47.27p	156.55nW	7.4a	156.79uW



(a)



(b)

Fig. 6.21. Static Power Dissipation of (a) GDI and (b) PT based Universal 4-bit Barrel Shifter

The static power dissipation of FinFET based Barrel shifter using GDI mux is 156.79nW shown in Fig. 46 (a), which is 17.22 times less than FinFET based barrel shifter using PT Mux which is 2.7uW as shown in Fig. 46 (b). Therefore, FinFET based Universal Barrel Shifter using GDI Mux shows better performance in terms of both delay and power.

IMPORTANT OUTCOMES:

- Analysis of MOSFET and FinFET based universal barrel shifter is done at 90 and 10nm respectively.
- Six operations can be performed using universal 4-bit barrel shifter, which includes both shifting and rotation of the bits.
- Universal barrel shifter is designed using GDI and PT based multiplexers for both MOSFET and FinFET model. Aim is to analyse and find the best performance barrel shifter.
- After analysis it is observed that MOSFET based shifter dissipate more power and take more time to pass the input signal to the output. Whereas FinFET based shifter dissipates 98.77% less power dissipation compares to MOSFET.

CHAPTER VII

CONCLUSION AND FUTURE SCOPE

7.1 CONCLUSION

Eight diverse techniques for multiplexer implementation have been analysed for dynamic power consumption, delay, static power and power delay product. The maximum power dissipation of TG, GDI, PT, MSL, Static CMOS, CPL, CVSL and MTCMOS CVSL based Mux are 204.21, 294.74, 198.53, 177.55, 179.69, 271.88, 256.1 and 206.8 μW , respectively. While the minimum power dissipation is obtained as 0.1291, 0.00000172, 0.2196, 25.49, 19.18, 26.16, 19.44 and 0.931.8 nW respectively. If average power dissipation is considered then PT based Mux has achieved the best performance at 110.9nW. This is lower by 30.2%, 93.58%, 85.41%, 81.67%, 92.19%, 90.43% and 84.94% in comparison to TG, GDI, MSL, Static CMOS, CPL, CVSL and MTCMOS CVSL based mux, respectively. The delay analysis recommends GDI based Mux as the fastest mux as it has the least delay recorded at 1.65ps. Additionally, it also registers the minimum static power dissipation of 219.99 pW. While in terms of average power dissipation PT based mux out performs GDI based mux but it is slower by a factor of half than the GDI Mux.

The maximum power dissipation of PT and GDI based Mux using MOSFET are 198.53 and 294.74 μW , and by using FinFET at 10nm technology node, values are 7.50uW and 839.3nW. While the minimum power dissipation is obtained as 0.2196 and 0.00000172 nW using MOSFET and 60.7nW and 1.02aW nW using FinFET respectively. If average power dissipation is considered then GDI based Mux using FinFET has achieved the best performance at 27.15nW. This is lower by 75.51% and 60.72 times in comparison to PT and GDI based mux using MOSFET, respectively and 73.06% less than FinFET based PT Mux.. The delay analysis recommends GDI based Mux using FinFET as the fastest mux as it has the least delay recorded at 0.0107ps. While in terms of average power dissipation GDI based mux out performs the other MOSFET based multiplexers. The results obtained above strongly suggest that each mux techniques have its own merits. Some techniques demonstrate excellent power performance, while the other have faster operations, or are better at static performance. So the selections for integration into a digital circuit would depends on the application specifications.

Two different technique has been analysed successfully with FinFET 10nm technology node. The maximum power dissipation of GDI and PT based Mux. In both of them, GDI based

Mux shows better performance in terms of delay and power. The maximum power dissipation of GDI based Mux is 839.3nW, which is 88.80% less than PT based Mux. GDI mux shows a better performance in terms of Average power dissipation, GDI, and PT based Mux dissipates 27.15nW and 100.8nW. In terms of speed of operation, GDI performs fast operation with a 0.0107ps delay, which is 165.42 times faster than PT based Mux. The power delay product of GDI and PT based Mux is 0.00029aJ and 0.1aJ. There is a significant reduction in static power dissipation in GDI based Mux in comparison to PT based Mux. In GDI leakage is 60.79nW, 2.23 times less than PT based Mux. This analysis demonstrates that the performance of both Mux is different and according to the requirement of the designer appropriate mux can be selected to improve the performance of the entire circuit design.

In PT based Mux total of 4 transistors is used to operate (Two to pass the input to output and two to invert the select signal), whereas in GDI only two transistors are used to perform the same operation. So, in GDI based Mux by using a smaller number of transistors the same operation can be performed. These two multiplexers using MOSFET were used to design the universal barrel shifter and analysed the delay and power dissipation. The maximum power dissipation of GDI based barrel shifter is 38.14uW, in comparison to PT based barrel shifter, it is 83.29% less which is 2.09mW. The minimum power dissipation of GDI barrel shifter is 392.6nW and PT based barrel shifter is 428.1uW, which is 1090.4 times more than GDI based barrel shifter. The average power dissipation of PT based barrel shifter is 487.7uW, which is 957.5 times more than GDI based barrel shifter. Delay is another important factor which decides the performance of the design, GDI based barrel shifter takes 125.1ps delay to pass the signal and PT takes 186.6ps which is 60.9ps more than GDI based barrel shifter. Whereas power delay product of GDI based barrel shifter is 63.7aJ and PT based barrel shifter is 90712.2aJ, which is 1424 times more than GDI. When circuit is in static condition then static power dissipation of GDI based shifter is 392.64 and for PT based shifter is 428.22uW, 1090.6 times more than GDI based shifter. After analysing the delay and power, GDI based universal barrel shifter showing the better performance.

Designing of universal 4-bit barrel shifter is also done using FinFET 10nm technology node GDI and PT based multiplexers. For GDI based shifter maximum power dissipation is 468.5nW and minimum power dissipation is 154.48nW and for PT based shifter maximum and minimum power dissipation is 6.49uW and 2.64uW respectively, which is 13.85 and 17.08 times more than maximum and minimum power dissipation of GDI based universal barrel shifter. Average power dissipation of PT based shifter is 2.68uW, 17.11 times higher compare

to average power dissipation of GDI based shifter which is 156.55nW. In term of delay GDI based shifter perform the fast operation, takes only 47.27ps delay which is 15.23ps less than PT based shifter. Static power dissipation of GDI and PT based barrel Shifter is 156.79nW and 2.7uW respectively.

Finally, the MOSFET based and FinFET based GDI and PT techniques for mux implementation are used to design barrel shifters. And the performance of the barrel shifter for four different configurations are demonstrated.

7.2 FUTURE SCOPE

Analysis of universal barrel shifter using MOSFET concludes that it can't be scale down in technology node after some limit and in terms of power dissipation, delay and performance further improvement wasn't possible. So, to improve the barrel shifter FinFET is the one of the best options in today's scenario to improve the performance with less power dissipation and area consideration is also very less. Barrel shifter is very crucial part of ALU, microprocessors and others computational devices, where shifting and rotating of data is required. Improving of barrel shifter will directly improves the source design. In this report barrel shifter is designed and analysed using FinFET at 10nm technology node, which shows the promising improvements in the performance with less area requirement and less power dissipation. In future further improvement is possible to enhance the performance.

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2. N. Kumar and P. Mittal, "Performance Investigation of 2:1 Multiplexer using 90nm Technology Node for Low Power Application", *International Conference on Electrical and Electronics Engineering (ICE3-2020)*, MMMUT, Gorakhpur, UP, India, 14-15 Feb, 2020 (Published by IEEE, **Scopus Indexed**).
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1. N. Kumar and P. Mittal, "Tetra-variate scrutiny of diverse multiplexer techniques for designing a Barrel Shifter for Low Power Digital Circuits", *Journal of Computational Electronics* (ISSN: 1572-8137), **SCIE Indexed, Springer**, Submitted on Aug 24, 2020.
2. N. Kumar, P. Mittal and M. Mittal, "Dynamic Power Consumption and Delay Analysis for Ultra Low Power 2:1 Multiplexer Designs", *International Journal of Advances in Electrical and Electronic Engineering* (ISSN: 1804-3119), **Scopus Indexed**, Submitted on May 24, 2020 (Current status: Under Review).
3. N. Kumar and P. Mittal, "Design and Analysis of Universal Barrel Shifter with low power multiplexers using FinFET at 18nm technology", *International Journal of Information Technology* (ISSN: 2511-2112), UGC-CARE, **Springer**, Submitted on Aug 17, 2020.