OPTIMIZATION OF SINGLE ENDED SRAM WITH DYNAMIC FEEDBACK CONTROL USING GNRFET

A DISSERTATION

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Submitted by:
RAHUL RANJAN
2K18/VLS/13

Under the supervision of
Dr. ALOK KUMAR SINGH
Associate Professor

ELECTRONICS & COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042
JULY, 2020

ELECTRONICS & COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CANDIDATE'S DECLARATION

I, Rahul Ranjan, Roll No. 2K18/VLS/13, student of MTech (VLSI Design & Embedded System), hereby declare that the Project Dissertation titled "Optimization of Single Ended SRAM with Dynamic Feedback Control using GNRFET" which is submitted by me to the Department of Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not derived from any source without appropriate citation. This work has not previously formed the basis for the award of any Degree, Diploma Associate-ship, Fellowship or other similar title or recognition.

Place: Delhi **RAHUL RANJAN**

Date:11th July, 2020

ELECTRONICS & COMMUNICATION ENGINEERING
DELHI TECHNOLOGICAL UNIVERSITY
(Formerly Delhi College of Engineering)
Bawana Road, Delhi-110042

CERTIFICATE

I hereby certify that the Project Dissertation titled "Optimization of Single Ended SRAM with Dynamic Feedback Control using GNRFET" which is submitted by Rahul Ranjan, Roll No. 2K18/VLS/13, Electronics & Communication Engineering, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi

Date:11th July, 2020

Dr. ALOK KUMAR SINGH

SUPERVISOR

ASSOCIATE PROFESSOR

ABSTRACT

Random-access memory (RAM) is information storage commonly used for storing run time variables and instructions in microcontroller and processing units. A random-access memory gadget permits information to be perused or written in nearly a comparable measure of time regardless of the physical area of data inside the memory. There are two types in this category- Static and Dynamic type of RAM. Mainly, all memory cells have a requirement of being low power, high speed and should give higher efficiency.

In this paper, special type of SRAM which consists of a Dynamic Feedback Control technique is implemented on Simulation platform of HSPICE tool. The SRAM is analysed and improved using GNRFET technology in 22nm channel length. Also a new kind of power gating is introduced with adding of a GNRFET transistor in power path so as to increase the performance of the SRAM design in Dynamic Feedback Control. The proposed circuit improves the power by 71%. Delay, Power Delay Product and Leakage Current is improved by 99%. Also the power dissipation of the circuit is improved by 28%.

ACKNOWLEDGEMENT

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With profound sense of gratefulness, I thank Dr Alok Kumar Singh my Research Supervisor, for his encouragement, support, forbearance and his guidance in this project work. Furthermore, I would also like to thank Prof. N.S Raghava and Prof Rajeshwari Pandey, who gave me the permission to use all required equipment and the necessary format to complete the report. I heartily appreciate the guidance given by Prof Neeta Pandey in the project presentation that has improved my presentation skills with her comments and advices.

I take enormous delight in extending my acknowledgement to my family and friends who have helped me throughout this project work.

RahulRanjan

RAHUL RANJAN

2K18/VLS/13

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LIST OF ABBREVIATIONS

GNRFET – Graphene Nano-Ribbon Field-Effect Transistor

SRAM – Static-Random-Access Memory

DFC – Dynamic Feedback Control

SoC – System on Chip

PDYN – Dynamic Power

SNM – Static Noise Margin

AVLG – Adoptive Voltage Level Ground

CNFET – Carbon Nanotube Field Effect Transistor

SBFET – Schottky prevention field-sway transistors

NEGF – Non-balance Green's ability

FinFET – Fin Field Effect Transistor

ZGNR – Zig-Zag Graphene Nano Ribbon

AGNR – Arm Chair Graphene Nano Ribbon

CNP – Charge Fairness Factor

FCS – Feedback Control System

WWL – Write Word Line

RWL – Read Word Line

INTRODUCTION

1.1 INTRODUCTION

As nanometer process developments have moved, chip thickness and working repeat have extended, making power usage in battery-worked helpful contraptions a vital concern. Despite for no reduced devices, power usage is basic because of the extended packaging and cooling costs similarly as potential unflinching quality issues. Thusly, the rule structure objective for VLSI (huge scope coordination) fashioners is to meet execution essentials inside a force spending plan. As such, power adequacy has anticipated extended criticalness. This assignment investigates how circuits reliant on GNRFET (cutting edge type field-impact transistors), a creating transistor innovation that is likely going to improve or dislodge mass CMOS (equal metal-oxide-semiconductor) at 22-nm and past, offer captivating deferral power tradeoffs.

The aching to improve the structure estimations of execution, power, area, cost, and time to promote (opportunity cost) has not changed since the starting point of the IC business. Honestly, Moore's Law is connected to propelling those parameters. Regardless, as scaling of amassing centers progressed towards 20-nm, a bit of the device parameters couldn't be scaled any further, especially the force supply voltage, the common variable in choosing one of a kind force. Moreover, updating for one factor, for instance, execution therefore changed over into tremendous tradeoffs in various regions, like force. Another limitation as methods advanced toward 20-nm was how lithography was stuck at ArF lighting up source with a frequency of 193nm while the strategy essential component was pushing sub-20nm. Optical headways, for instance, dousing lithography and twofold altering made that possible, anyway to the detriment of extended variance. There were similarly various improvements on the way, for instance, High-K metal gate that helped – to a compelled degree – gate spillage issues. However, the truth remained that the structure window for upgrading among the recently referenced arrangement factors was contracting. Arranging in GNRFET broadens the structure window eventually. Working voltage continues scaling back, in a general sense getting a good deal on one of a kind and static force. Short channel impacts are decreased out and out, reducing the gatekeeper banding expected to oversee variability.

Likewise, execution continues improving appeared differently in relation to planar at an undefined center point. Believe it or not, at amazingly low force supply voltages, the execution good situation of the GNRFET appeared differently in relation to its planar indistinguishable broadens as a result of the unmatched gate control of the redirect in the GNRFET.

It is indicated that by virtue of overlooking short out current, past strategies proposed to propel the region of a fan-out tree may result in over the top force use. Unquestionably the dynamic mode power use, the clock power, and the typical spillage intensity of the combinational circuits are reduced by up to 55%, 29%, and 53%, independently, while keeping up relative speed and data security when appeared differently in relation to the circuits executed in CMOS and GNRFET innovation.

A stable cell for SRAM is produced by a Dynamic Feedback Control to mainly reduce the switching power in the circuit pf SRAM with DFC (Dynamic Feedback Control). [1] In VLSI world the memory and memory cells are the fundamental imperatives, while planning any gadget. The memory is utilized to store the information and these are accessible according to our applications. The Embedded memory, which is considered as an unavoidable entity of microchip controlled gadgets speaks to an enormous part of the framework on-chip(SoC). These versatile frameworks need ultra-low power expending circuits to use battery for an any longer span to increase the portability. [2]

Forcefully scaling the main supply voltage of SRAMs extraordinarily limits their dynamic and leakage power, a commanding segment in research for the power in present day ICs. [3] The power dissipation or consumption use can be limited using non-conventional device structures, new circuit topologies, and propelling the designing. Regardless of the way that, voltage scaling has provoked circuit activity in sub limit organization with least power use, anyway there is a downside of exponential diminishing in execution. [4] The standard activity in sub threshold limit is very troublesome in conventional SRAMs therefor the Dynamic Feedback Control based SRAM cells are gaining most importance in current research trends due to its high stability. [5] Thickness, power and execution are the basic parts required for these applications. Prior, those control to cutting edge rationale, which will be overpowered by unique power, has been lessened by cutting down those main voltages. [6] These advantageous structures need ultralow power consuming circuits to utilize battery for more term. The power use can be limited using nonconventional IC structures, new circuit topologies, and propelling the

building. Notwithstanding the way that, voltage scaling has incited circuit activity in sub limit organization with least power usage, anyway there is a disadvantage of exponential reducing in execution power. [7]

The power utilization by bit lines during composing is relative to the bit line capacitance, square of the bit line voltage and the recurrence of composing. There is a powerful approach in which the vitality put away in the bit line capacitance that is regularly lost to ground is gathered and siphoned once again into the source. This is known as vitality recuperation approach. Vitality put away in the bit lines is reused by the assistance of changes to neighboring piece lines so as to spare vitality in bit line charge-reuse strategy. This technique diminishes the swing voltages to a low swing voltage. In light of whether vitality reusing is done distinctly during composing cycle or during both composition and understanding cycles, there are variations. [8]

This thesis on GNRFET based SRAM in 9T power gated mode is an attempt to reduce issues such as short channel effects in MOSFET under 22nm technology. The thesis is gives as: the first part is introduction which gives brief about research scenario of SRAM, need and objectives. The second part is SRAM with Dynamic Feedback Control and GNRFET technology which are the main material and methods used in this work. The next part is proposed work which shows the GNRFET based Power Gated Circuit in 22nm and gives its working waveform information with simulation. The next part is the simulation results which are the main parametric comparisons which shows the improvements and hence in the last section this paper is concluded with future scope of it.

1.2 MOTIVATION

GNRFETs are a vital advance in the development of semiconductors since mass CMOS experiences issues in scaling past 32 nm. Utilization of the back gate prompts very intriguing plan openings. Rich decent variety of formation styles, made conceivable by free control of GNRFET gates, can be utilized magnificently to decrease absolute dynamic power utilization IG/LP mode circuits give an vesting tradeoff among power and zone. In these theories, 2:4 decoder is talked about with 14 transistor and 15 transistor LP, LPI, HP and HPI in present situation, power decrease is a noteworthy issue in the technology world. The low power configuration is serious issue in superior

computerized framework, for example, chip, advanced flag processors (DSPs) and different applications. The chip thickness and higher working pace prompts the arrangement of astoundingly complex chips with high clock frequencies. In this way, arranging of low power VLSI circuits is a mechanical need in these in light of the prominence for minimized buyer contraptions thing. In a microchip/microcontroller-based system, the most customarily used square is the bearing set decoder. In this way; it will be not wrong in case state the bearing set decoder uses more power. Along these lines overhauling the vitality of this square will be valuable to diminish the general power use of the system. Along these lines, proposed plan for this theory is the utilization of GNRFET system to diminish power utilization of guidance decoder. In this proposition, have proposed the structure of single ended dynamic feedback control based SRAM with the utilization of GNRFET logic to lessen the power of the decoder and subsequently will help in power decrease of generally framework.

1.2.1 Problem formulation

To Design a Low Power and High Speed GNRFET based SRAM with Dynamic Feedback Control. The MOSFET has been used extensively in current innovation. Be that as it may, underneath 22nm innovation, controlling the channel of the MOSFET winds up inconvenient. So there is need to make new innovation which will empower us to structure devices underneath 45nm innovation. Uproar in significant submicron innovation got together with the move towards dynamic circuit procedures has raised stresses over trustworthiness and imperativeness efficiency of VLSI structures in the significant submicron time.

1.3 OBJECTIVE

- To accomplish broad exploration, and research on low power consumption and High SRAM utilizing GNRFET innovation.
- To Design a low power consumption based GNRFET based SRAM with Dynamic Feedback Control.
- To do Comparative Analysis of GNRFET and MOSFET based SRAM with Dynamic Feedback Control proposed procedure as far as AVG POWER CONSUMPTION.
- To investigate the proposed strategy as far as following measurements- AVG POWER CONSUMPTION

- DELAY
- PDP &
- Power Dissipation
-Leakage Current

1.4 ORGANIZATION OF THE REPORT

This report of Low Power and High Speed GNRFET based SRAM with Dynamic Feedback Control circuit configuration venture is sorted out in five sections. 1 section gives you the outline of the work which is beginning from the writing of the past work done and the proposed work. In section 2 the definite writing is followed and hypothesis of GNRFET is spread in this part so have some firm information about GNRFET before continuing to applying procedures in circuit. In part 3 continue to certain assortments of SRAM with Dynamic Feedback Control and apply the low force method and compute execution measurements to present the proposed structure. In part 4 recreation results and section 5 has end made on premise of result.

CHAPTER 2

LITERATURE REVIEW

C. B. Kushwah et. al., [1], proposed A story 8-transistor (8T) static sporadic access memory cell with improved data quality in subthreshold movement is organized. The maker proposed single-got done with dynamic information control 8T static RAM (SRAM) cell updates the static upheaval edge (SNM) for ultralow power gracefully. Moreover, practiced improved SNM in subthreshold framework using SE-DFC and read decoupling plans. The maker proposed cell's zone is twice as that of 6T. Regardless, it's better natural system strength and dynamic voltage real nature engages it to be used like cells (8T, 9T, and 10T) nearby 1.8 ×−2× locale overhead.

Athira M R et. al., [2], The Embedded memory, which is considered as an unavoidable bit of microchip controlled devices addresses an immense piece of the structure on-chip(SoC). These helpful systems need ultra-low power consuming circuits to utilize battery for an any more extended range. A 8-transistor(8T) static self-assertive access memory cell with improved data security in subthreshold action is realized in Cadence virtuoso 45 nm Technology. The single-completed structure is used to decrease the differential trading power during scrutinize and create action.

Sonal Verma et. al, [3], Aggressively scaling the reserve voltage of SRAMs colossally confines their dynamic and spillage power, a staggering section of the whole power in present day ICs. Subsequently, essentialness constrained applications, wherever execution needs are helper, advantage widely from a SRAM that gives examine and create helpfulness at any rate possible voltage. In any case, bit-cells and plans achieving very high thickness conventionally disregard to work at low voltages. This paper delineates a high thickness SRAM in sixty-five nm CMOS that usages accomplice degree 8T bit-cell to accomplish a base operational voltage of 350 mV. Padded yield is used to guarantee read security, and periphery the leading group of each the bit-cell offer voltage and moreover the read-support's foot voltage change sub-create and read while not adulterating the bitcell's thickness.

Motla Sushma et. al., [4], This paper executes the arrangement of Single completed one of a kind analysis control 10T sub edge cell. The 10T can work at very low power levels,

for instance, ultra low power ranges. The trading pace of 10T is high when appeared differently in relation to the proposed methodology 8T cell. The proposed single-got done with dynamic analysis control 8T static RAM (SRAM) cell updates the static clatter edge (SNM) for ultralow power gracefully.

Devarapalli Mounika et. al., [5], A 8T-SRAM cell using Adoptive Voltage Level Ground (AVLG) strategy with better execution, low power use and less spillage power has been completed. The proposed 8T improves the circuit execution at ultra-low power supplies. It achieves less power usage than single completed 8T SRAM cell. By using AVLG system the circuit exhausts less power, in spite of the way that the no.of transistors and the region are high.

S Renukarani et. al., [6], An original thought of 8-Transistor (8T) static irregular access memory cell with upgraded data security, sub edge activity might be laid out. Those recommended novel assembled single-finished for dynamic control 8 transistors static RAM (SRAM) cell upgrades the static commotion edge (SNM) to grater low vitality supply. The recommended 8T takes less peruse and compose power supply contrasted with 6T. Those proposed 8T need higher static commotion edge than that from 6T. The convenient microchip chips need ultralow vitality devouring circuits on use battery to progressively drawn out range. The force use may be limited using non-regular contraption structures, new circuit to-pologies, and redesigning the design. Despite the fact that, voltage scaling expect of the activity finished over sub edge for low force utilization, and there will be a bother from exponential diminishing in execution. Nonetheless, to sub edge system, that information dependability of SRAM cell may an opportunity to be an astounding issue and declines for those scaling from claming MOSFET should sub-nanometer building innovation.

Aisha Mobeen Mohammad, et. al., [7], A tale 8-transistor (8T) static self-assertive access memory cell with improved data unfaltering quality in sub limit activity is illustrated. The proposed single got done with component input control 8T static RAM (SRAM) cell improves the static commotion edge (SNM) for ultra-low force supply. It achieves form SNM of1.4x and1.28x as that of its range 6T and read decoupled 8T (RD-8T), independently, at 300 mV. The standard deviation of make SNM for 8T cell is diminished to 0.4x and 0.56xas that for 6Tand RD-8T, independently. It in like manner

has another striking segment of high read SNM~2.33x, 1.23x, and 0.89x as that of 5T, 6T, and RD-ST, independently.

K.M.Santhoshi Priya, et. al., [8], In request to accomplish a more drawn out battery life concealment of vitality utilization is crucial. An interest for structure techniques for less vitality utilization is expanding. The subthreshold scaling can lessen vitality per cycle essentially by the scaling of supply voltage (VDD) underneath limit voltage (Vth). Limit voltage of CMOS innovation speaks to the estimation of the entryway source voltage when the current in a MOS transistor begins to increment essentially since the conduction layer just starts to show up. MOS transistor can likewise work effectively with an inventory voltage underneath its edge voltage (Vth), which is alluded to as sub-edge activity or powerless reversal of a transistor. The circuits that work under a stock voltage in the sub-limit extend are named sub-edge circuits. In ultra-low force structure, the activity of circuit in subthreshold system is generally significant and the SRAM circuit has the constraint of read upset. So as to wipe out this impediment, The Single-finished plan is utilized. In this paper we propose the single-finished with dynamic criticism control (SE-DFC) cell.

M.N. Naga Vyshnavi et. al., [9], An epic 8-transistor (8T) static arbitrary access memory cell with improved information dependability in subthreshold activity is planned. The proposed single-finished with dynamic input control 8T static RAM (SRAM) cell upgrades the static clamor edge (SNM) for ultralow power supply. It accomplishes compose SNM of 1.4× and 1.28× as that of iso-region 6T and read-decoupled 8T (RD-8T), individually, at 300 mV. The standard deviation of compose SNM for 8T cell is decreased as that for 6T and RD-8T, separately. It additionally has another striking component of high read SNM as that of 5T, 6T, and RD-8T, separately. The proposed 8T devours less compose power as that of 5T, 6T, and iso-zone RD-8T, separately. The force/vitality utilization of 1-kb 8T SRAM cluster during read and composes tasks limited. These highlights empower ultralow power utilizations of 8T.

Chandramauleshwar Roy, et. al., [10], We present a circuit-level strategy of planning a lower compose power alongside changeability safe 9-MOFTET static arbitrary access memory cell. Our proposed bitcell shows lower compose power utilization attributable to decrease of movement factor and separation of input way between the cross-coupled inverters during compose activity. It shows higher read static clamor edge (by 3.09 9)

contrasted and standard 6T SRAM cell @ least zone. LP9T shows higher static edge for compose activity (by 41%) contrasted and 8T (S6T) @ iso-region (least territory). These upgrades are accomplished because of separation of criticism way during the way toward composing a piece on to the capacity hub. The paper researches in detail the impact of variety in process related parameters, ecological parameters, for example, supply voltage and temperature on the vast majority of the significant plan parameters of the bitcell and contrasts the acquired reproduction results and ordinary 6-MOSFET (6T) and 8-MOSFET (8T) bitcells. It exhibits its perpetual quality by indicating 1.5 9 more tightly scatter in read time fluctuation with an expense of 1.41 9 higher read time contrasted and S6T @ least region. It additionally shows 39% smaller scatter in read time changeability in contrast with 8T @ iso-territory. It draws lower power (2.06 9) from supply voltage while flipping of put away information during compose mode contrasted and standard 8T SRAM cell @ iso-zone. It additionally contrasts key structure measurements of LP9T and those of not many other 9T SRAM cells found in the writing. This work additionally understands the proposed structure utilizing CNFET. The CNFET-based plan beats its CMOS partner in all regard.

Hader E., et. al., [11], Robust GNRFET/MOSFET Combination is utilized to construct different force gating structures utilizing 16nm innovation. The advanced Power Gating (PG) structure is made out of GNRFET as a footer rest transistor and Silicon CMOS rationale power gated module. The proposed structure settle the principle disadvantages of the customary PG plan from the perspective expanding the spread postponement and wake-up time in low–voltage areas. Spillage power, surge current, wake-up time and force postpone item are utilized as the presentation circuit parameters for the assessment. The presentation aftereffects of the anticipated power gating structure with single footer uncovers a decrease in spillage power, defer time, and wake-up time, on normal up to 88%, 44%, and 24%, separately, for various rationale circuit modules contrasted with the MOSPG construct.

H. V. Violate Aradhya, et. al., [12], The headway in IC innovation is basically credited to the MOSFET scaling hypothesis. As the transistor size decreased, power utilization additionally diminished. As the procedure innovation came to nano-meter system, silicon CMOS began growing Short-Channel Effects which prompted expanded force dissemination. An exchange off emerged between power-dispersal and region. Options to CMOS were found to stay away from the exchange off. Graphene based transistor end

up being a potential substitution to CMOS. The Arithmetic and Logic Unit is the essential processing unit everything being equal or microcontrollers. The equal viper frames the basic way in the ALU. The offered work structures and thinks about CMOS and GNRFET based 8-piece ALU models.

Yijian Ouyang: et.al [14] Scaling Comportments of Graphene Nanoribbon FETs: A Three Dimensional Quantum Simulation Study. The scaling of graphene nanoribbon (GNR) Schottky prevention field-sway transistors (SBFETs) are mulled over by understanding and separating the non-balance Green's ability (NEGF) transport condition in an atomistic reason set through a three-dimensional Poisson condition. The rocker edge GNR channel circuit gives likenesses to a bungle CNT, anyway it has an other fundamental geometry and quantum restriction limit condition the transverse way. The results shows that the I-V qualities are ambipolar and for the most part depend upon the GNR width as the bandgap of the GNR is oppositely comparative with its width, which according to progressing preliminaries. A various entryway helper geometry improves and overhauls protection from short channel impacts, anyway it offers less improvement when appeared differently in relation to Si MOSFETs viewing the on-current similarly as transconductance. Diminishing the oxide thickness by and large is more significant for improving transistor execution than using a high-κ door defender. Basic augmentation of the insignificant spillage current is seen when the channel length is scaled underneath 10 nm as the little suitable mass empowers strong source-channel tunneling. The GNRFET, thusly, doesn't really add to growing an authoritative scaling cutoff of Si MOSFETs. The trading pace of a GNRSBFET, is a couple of times snappier than that of Si MOSFETs, which could add to promising quick equipment applications, where the tremendous spillage of GNRSBFETs is of less concern."

"Abhijith A Bharadwaj: et.al[15] Design and Performance Comparison of finFET, CNFET and GNRFET based 6T SRAM Static Random Access Memory (SRAM) has from long the best way to deal with store data electronically on-chip, in quick circuits. The specifics of low zone, quick ICs are the responsibility of MOSFET scaling frameworks. Purposes of repression on MOSFET scaling results a necessity for new transistor development. Here it gives three SRAM (6T) cell models (Graphene Nanoribbon FET, Multi-walled CNT FET and MOSFET) which gives the course for advancement. The parameters as Read delay, Write deferral and Power-delay thing are contemplated. All the three advancements, 10nm entryway length is taken. Plan and

propagation of an all out SRAM cell is then thought of (6T SRAM cell, Sense intensifier ,Precharge circuit, Read and Write circuits) to give control assessment between 32X8, 32X16, 64x8 and 64x16 SRAM bunches. Circuit is organized and reenactment was done using HSpice and CosmosScope."

"PRAVEENA KUMARI: et.al [16] Design and Analysis of 16bit Ripple Carry Adder and Carry Skip Adder Using Graphene Nano Ribbon Field Effect Transistor (GNRFET) Moore's Law Cannot Be thought about extra Since MOSFET's Cannot Be Scaled Below 10nm Due To Its Physical and helper Properties .This Trade-Off results in a Way For New Material Used In Fetes To be according to Moore's Law. Distinctive Other Technologies Include Carbon Nano-Tube FET (CNTFET), Fin-Shaped FET (Finfet), Reconfigurable Logic ,Reversible Logic, And Grapheme Nano-Ribbon FET (GNRFET), Among The Available progressions GNRFET's Has Proven To Be An out and out Promising Potential Replacement In Terms Of Design Area, Faster Operation, Lower Power Consumption. Carbon Is can be used in wide scale applications Because Even If Some Material Is Made Up Of Carbon Atoms, It Can Have Various Characteristics and Morphologies Depending On How Carbon Atoms Bind Together. Organizing Of RCA And Cska Adders Using GNRFET."

Preetika Sharma: et.al[17]" Effect of temperature on conductivity of GNRFET Graphene nano strips are the layers and sections of graphene sheet which has open band gap in graphene. This opening of band gap overhauls the on off extent of GNR contraptions and add to its use in basis circuit applications. GNR in transistors give long range applications in these zones. A GNRFET demonstrates tremendous conductance with door voltages. The effect of temperature on this conductance in GNRFET is found in this paper by mirroring and arranging a GNRFET model in VNL. A GNRFET with jumble anodes and armchair channel is totally analyzed. The conductance in regards to temperature is watched and recorded. A temperature extent of 0 to 2000 K is taken for the assessment."

“HueiChaengChin: et.al[18] Enhanced Device and Circuit-Level Performance Benchmarking of Graphene Nanoribbon Field-Effect Transistor against a Nano-MOSFET with Interconnects Graphene nanoribbon field-sway transistor (GNRFET) and a nanoscale metal-oxide semiconductor field-sway transistor (nano-MOSFET) for applications in ultra enormous scope integration(ULSI) is shown. GNRFET is seen to

be unquestionably unmatched in the circuit-level execution and structure. The extraordinary vehicle properties of GNR direct it into an elective development to elimitations imposed by the silicon-based devices. Growing GNRFET, using the circuit level showing programming SPICE, shows improved execution for cutting edge method of reasoning doors in16nmprocesstechnology.The assessment of these introduction estimationsjoinsimperativenessdelayproduct(EDP)andpowerdelayproduct(PDP)ofinverterandNORandNANDgates,formingthebuildingblocksforULSI.TheevaluationofEDPanddPDPiscarriedoutforaninterconnectlengththatrangesupto100μm.Anexamination,considering the channel and entryway current-voltage(Id-Vd and Id-Vg),for sub edge swing(SS),drain-started block cutting down (DIBL), and current on/off extent for circuit use is given. GNRFET can overcome the short-channel impacts that are normal in sub-100nm Si MOSFET. GNRFET gives reduced EDP and PDP one solicitation of significance that is lower than that of a MOSFET. In spite of the way that the GNRFET is essentialness capable, the circuit execution of the contraption is obliged by the interconnect capacitances."

Amit Sangal: et.al [19]"GNRFET as future low force devices — The graphene nano-strip field sway transistor (GNRFET) is a creating development that gotten a lot of thought starting late. Late work on GNRFET circuit re-enactments has exhibited that GNRFETs may have potential in low force applications. In this paper, were see the present work on GNRFET circuit showing, consider the two arrangements of GNRFETs, Metal-Oxide-Semiconducting-(MOS-)type and Schottky Barrier-(SB-)type GNRFETs, and inside and out discussion about and examine their specific characteristics to the extent deferral, force, and commotion edge. Beginning here of view, we talk about their potential applications, especially the usage towards low-control figuring. Our re-enactments exhibit that ideal (nonideal)MOS-GNRFETconsumes18%(35%)and54%(102%)total power when appeared differently in relation to world class (HP) Si-CMOS and low-control (LP) SiCMOS, exclusively.

SB-GNRFET doesn't balance emphatically with MOSGNRFET to the extent power use. Regardless, great (non-great) SB-GNRFET has 3% (5.4X) and 0.45% (83.5%) essentialness concede thing (EDP) appeared differently in relation to Si-CMOS (HP) and Si-CMOS (LP), independently, whileideal(non-ideal)MOS-

GNRFEThas8%(93%)and1.25%(14.3%) EDP diverged from Si-CMOS (HP) and Si-CMOS (LP), separately."

"Wan Sik Hwang [20] Graphene Nanoribbon Field Effect Transistors on Wafer Scale Epitaxial Graphene on SiCsubstrates .We account the affirmation of top-gated graphene nanoribbon field sway transistors (GNRFETs) of ~10 nm width on colossal zone epitaxial graphene showing the opening of a band gap of ~0.14 eV. Differing to prior view of jumbled vehicle and extraordinary edge-cruelty effects of GNRs, the exploratory results presented here unquestionably exhibit that the vehicle instrument in meticulously made GNRFETs is common band-transport at room temperature and interband tunnelling at low temperature. The complete space of temperature, size, and geometry ward transport properties and electrostatics of the GNRFETs are elucidated by a standard thermionic transmission and tunnelling current model. Our joined test and showing work exhibits that carefully made tight GNRs go about as normal semiconductors, and remain potential contender for electronic trading contraptions Implementation of 2-dimensional (2D) graphene for mechanized method of reasoning devices has shown testing considering the material's zero band opening [1]. Distinctive trade propelled method of reasoning device structures have been proposed that abuse interlayer tunneling, graphene-3D semiconductor heterostructure, and properties that attempt the light-like imperativeness dispersing of transporters in 2D graphene [2-6]. From the viewpoint of recognizing standard field-sway transistors, all around controlled graphene nanoribbons (GNRs) mimic the sensational electrostatic properties of carbon nanotubes (CNTs) and offer trust in graphene-based propelled method of reasoning contraptions. The ultrathin body can engage scaling back to 10 nm or underneath while so far monitoring short channel degradation impacts. GNRs experience the evil impacts of edge-disagreeableness scattering impacts appeared differently in relation to CNTs, yet GNRs give a better gigantic area flexibility, planar production opportunity, and warmth spread breaking point than CNTs [9]. The availability of broken protections at the edges gives a fortunate opening to substance doping [10], which remains inconvenient in CNTs as a result of submerged sp2 manufactured bonds. Different "past CMOS" contraptions, for instance, the GNR tunnelling field-sway transistor (TFET) [11] can be recognized whether controlled GNRs can be fabricated on gigantic zone substrates. Along these lines, advance in the assembling and depiction of wafer-scale GNRs stands to possibly enable an enormous gathering of employments later on."

Hader E. El-hmaily: et.al [21] " High Performance GNR Power Gating for LowVoltage CMOS Circuits A solid imperativeness gating structure the use of Graphene NanoRibbon discipline-sway Transistors (GNRFET) is proposed the utilization of 16nm development. The force Gating (PG) shape is made out of GNRFET as an essentialness switch and MOS power gated module. The proposed shape settle the rule impediments of the traditional PG design from the point of view growing the inciting deferment and wake-up time in low–voltage regions. GNRFET/MOSFET Conjunction (GMC) is contracted to develop various systems of PG; GMCPG-SS and GMCPG-NS. in this manner to manhandling it to create multi-mode PG structures. Circuit assessment for CMOS quality gated dynamic capacity modules (ISCAS85 benchmark) of 16nm advancement is used to study the display of the proposed GNR essentialness move is diverged from the regular MOS one.Spillage quality, wake-up time and imperativeness concede thing are used as a rule execution circuit parameters for the evaluation. GMCPG-SS as a rule execution results screen a diminishing in spillage quality, concede time, and wake-up time, on customary as much as 88%, forty four%, and 24%, independently, and GMCPGNS structure reduces the spillage quality in 69% and ninety two%, and wake-up time through 27-forty six% for extraordinary ISCAS85 essentialness gated modules interestingly with the MOSPG shape. each multimode PG systems can diminish the spillage power appeared differently in relation to the alternative PG structures with headway inside the wake-up time by using ninety nine%."

"M. Akbari Eshkalak: et.al [22] Graphene Nano-Ribbon Field Effect Transistor under Different Ambient Temperatures This paper is the essential assessment on the impact of including temperature on the electrical qualities and high repeat displays of twofold entryway armchair graphene nanoribbon field sway transistor (GNRFET). The results diagram that the GNRFET under high temperature (HT-GNRFET) has the most raised cut-off repeat, least sub-edge swing, least trademark deferral and force delay thing differentiated and low-temperature GNRFET (LT-GNRFET) and medium-temperature GNRFET (MTGNRFET). Furthermore, the LT-GNRFET shows the most negligible off-state current and the most essential extents of Ion/Ioff, ordinary speed and adaptable charge. Additionally, the LT-GNRFET has the most essential door and quantum capacitances among three recently referenced GNRFETs."

"Youngki Yoon: et.al [23] Performance Comparison of Graphene Nanoribbon FETs with Schottky Contacts and Doped Reservoirs We present an atomistic 3D reenactment

look at of the general execution of graphene nanoribbon (GNR) Schottky impediment (SB) FETs and transistors with doped vaults (MOSFETs) by using oneself consistent answer of the Poisson and Schrödinger conditions inside the non-amicability green's trademark (NEGF) formalism. flawless MOSFETs show barely higher electrical execution, for each virtual and THz applications. The impact of non-idealities on device when all is said in done execution has been explored, contemplating the closeness of single void, an area cruelty and ionized contaminations near to the channel. Overall, MOSFETs show extra solid qualities than SBFETs. locale obnoxiousness and unmarried void issue, all things considered, influence as a rule execution of both mechanical assembly types."

CHAPTER 3

GNRFET TECHNOLOGY AND SRAM WITH DFC

3.1 INTRODUCTION TO GNRFET

Single layered Graphene, a shed composite of carbon, rose as a promising a seer in 2004, considering the way that the primary dimensional surface with hanging advanced, magneto-electronic and optoelectronic properties. Due to extravagant transportability ballistic vehicle, speedy state trading by virtue of especially high administration adaptability and electrostatic decrease in perspective on the 2d structure, Graphene basically based gadget shave a promising future in supplanting standard CMOS nano hardware.

The convenience of shed Graphene becomes recommended to be 100,000 cm 2V-1s-1 (On protected substrates) and 230,000 cm 2V-1s-1 for suspended structures. Graphene surely understood a warm conductivity of 5300Wm okay at room temperature. The primary area of Graphene into FET moved toward turning out to be gin 2007. The paper uses Graphene Nano-Ribbon (GNR) FETs. The chance of band opening building in GNR pushes the material for good measured future use in nanoelectronic circuits on account of its recognized qualities which fuse tremendous administration compactness and planar shape. Graphene a two dimensional material is engineered in a honeycomb pearl grid. It has various specific homes. These particular home shave made this material a potential chance for different bundles, for instance electronic gadgets, nanogadgets and dispatch. In any case not withstanding giving superb achievements in fantastic fields, a fundamental disadvantage of zero band holes limits its general execution. Graphene transistors ordinarily called as Graphene FETs display better by and large execution parameters in RF devices and correspondence structures due to its astoundingly high provider mobilities, am bipolarity, high warm conductivity and subsequently outperform the standard Si-based FETs. These transistor devices the use of graphene in like manner are totally used to as the arrangement silicon transistors. In any case, regardless of getting the incredibly extraordinary homes, it encounters its 0band opening.

This zero band gap makes the trading way hard and in like way the on−off extents of those gadgets are nearly nothing. The low on off extent in such gadgets does never again permit turn off and fittingly power wastage happens and results in all things considered execution defilement. The decrease all in all execution defilement can be finished with the guide of building up appropriate band gap in graphene. The outlet of band opening in graphene is finished by methods for different methodologies. Course of action of graphene nano ribbons is one among such method. This is practiced with the guide of encircling parts of graphene by method for decreasing the width of graphene sheet. Decrease in the width of graphene sheet presents band hole right now opening surface as GNRs along the side limits the development of venders and instigate equity hole that is alternately comparative with the width of the ribbon. As width of the ribbon diminishes, the band hole of graphene will increase with the lower. Graphene Nano ribbons are of two sorts. These can be either Zigzag (ZGNRs) or Arm chair(AGNRs).The advanced homes of these graphene nano ribbons can be considered by using the width and the geometry of the GNR along their edges. These additionally have an element desert that is a basic parameter to mull over as the edge flaws prompts for the most part execution shakiness. ZGNRs are steel even as the AGNR are made semiconducting in nature. Graphene nano ribbons have fundamental bundles in electronic devices containing subject effect transistors.

GNR basically based subject effect transistors is one of the normal transistor dependent on graphene/graphene nano ribbons. Correspondingly a FET, it additionally has the 3 terminals alongside channel, source and the gate. Single layered Graphene, a peeled amalgam of carbon, developed as a promising answer in 2004, as a result of the truth of the key dimensional material with hanging advanced, magneto electronic and optoelectronic properties. By virtue of over the top flexibility ballistic transport, speedy nation changing in view of unfathomably in ordinate administration compactness and electrostatic discount due to the 2d structure,Graphene based completely gadgets have a promising future in supplanting ordinary CMOS nano hardware. The convey ability of peeled Graphene ascend as recommended to be a 100, 000cm 2V-1s-1(On protected substrates) and 230,000cm 2V-1s-1 for suspended structures. Graphene understood a warm conductivity of 5300Wm-1 adequate at room temperature. The basic area of Graphene in to FET progressed toward turning out to be in 2007.

The paper uses Graphene Nano-Ribbon (GNR) FETs. The chance of band void designing in GNR moves the material for sizeable future use in nano-electronic circuits as a result of its undeniable qualities which join colossal provider versatility and planar shape. Graphene a dimensional texture is masterminded in a honeycomb valuable stone grid. Its has various explicit homes. These epic house shave made this material a capacity plausibility for different bundles which fuse electronic gadgets, nano contraptions and discussion.

Any way not withstanding giving wonderful achievements in marvellous fields a straightforward drawback of zero band opening limits its typical execution. Graphene transistors all things considered called as Graphene FETs superstar better quality execution parameters in RF contraptions and correspondence structures due to its strikingly high provider mobilities, ambipolarity, super warm conductivity and in this manner outperform the standard Si-based FETs. These transistor gadgets the usage of graphene moreover are called inlight of the way that the situated up silicon transistors. Regardless, not withstanding getting the first rate living courses of action, it encounters its zero band opening. This zero band gap makes the trading way hard and thus the on−off extents of these devices are by and pretty much nothing.

The low on off extent in such devices does never again allow get off and in this manner power wastage happens and impacts in all things considered execution defilement. The decrease all things considered display debasement may be finished with the advantage of setting up sensible band opening in graphene. The opening of band hole in graphene is finished by methods for different methodologies. Course of action of graphene nano ribbons is completely one of such methodology. That is accomplished with the benefit of confining parts of graphene through method for diminishing the width of graphene sheet. Refund in the width of graphene sheet presents band hole on this zero band void texture as GNRs along the side limits the development of dealer sand start a force opening it is then again corresponding to the width of the ribbon. As width of the ribbon diminishes, the band hole of graphene will increase with the reduction. Graphene Nano ribbons are of sorts. Those may be both Zigzag(ZGNRs) or Armchair(AGNRs).

The computerized homes of these graphene nano-ribbons may be considered with the guide of the use of the width and the geometry of the GNR close by their edges. Those

similarly have included abandons; this is a fundamental parameter to take agandert as the edge deformities prompts ordinary for the most part execution unsteadiness. ZGNRs are metal meanwhile as the AGNR are made semiconducting in nature. Graphene nano-ribbons have noteworthy applications in electronic gadgets including issue sway transistors. GNR based completely issue sway transistors is one of the not odd transistors dependent on graphene/graphene nano-ribbons. In like manner FET, it besides has the three terminals related to deplete.

3.2 INTRINSIC AND EXTRINSIC GRAPHENE

It has one of kind limits, so it's basic to perceive among inward and outward Graphene. Gapless graphene (both mono layer MLG orbilayer BLG) has a charge fairness factor (CNP) i.e., the Dirac factor, where its character modifications from being electron need to being unfilled individually. see: Density of conditions of graphene is close to the Diracpoint. Any such differentiation isn't important for a2D EG (or BLG with a colossal hole) considering the way that the regular gadget is actually an undoped gadget without an association (and accordingly is dull from the computerized dispatching living courses of action perspective).

In monolayer and bilayer graphene, the ability to gate (or dope) the machine through placing associations in to the conduction or valence band with the guide of tuning an outside gate voltage enables one to pass by methods for the CNP in which the invention limit (EF) is living precisely at the Dirac point. This structure with no loosened venders atT"0", and EF definitely at the Dirac point is all used to as trademark graphene with a completely packed (empty) valence (conduction) band.

3.3 MATERIAL PROPERTIES OF GRAPHENE

Graphene is a semi metal (zero opening semiconductors) with charge transporters carrying on as massless Dirac fermions. Underneath charge absence of predisposition conditions, the Fermi degree is at the square endeavour to the valance and conduction gatherings, yet may be moved with the utilization of a vertical electric controlled order to make a larger piece of openings or electrons. An advancement of the entryway coefficient from practical to horrendous characteristics is resolved. Graphene notable

shows incredibly in ordinate provider motility at room temperature because of a vulnerable electron telephone on affiliation.

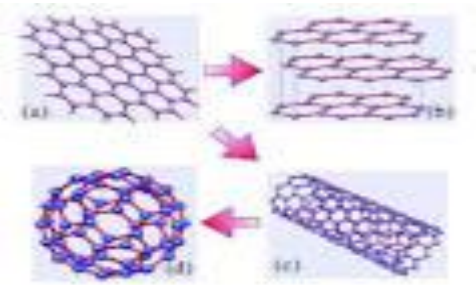

Figure 3.3 Structure of Graphene

3.4 SRAM with DFC

In this section, a brief description of methods used in improvement such as SRAM with dynamic feedback control and GNRFET is explained. This is an important part of the proposed methodology. Figure 3. 4 shows the circuit diagram of the existing Dynamic Feedback Control based SRAM.

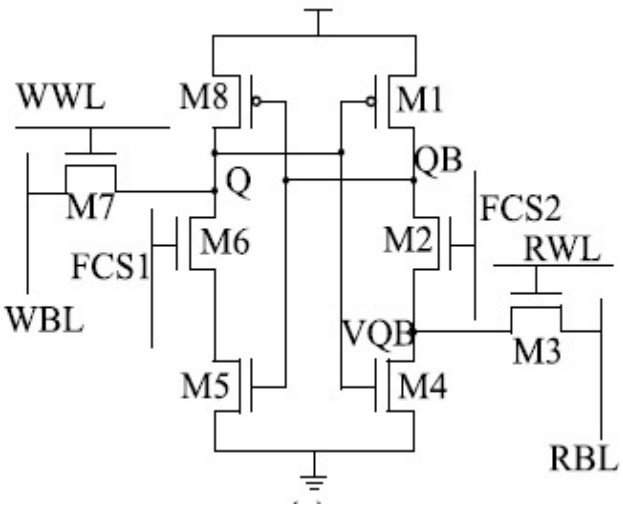

Figure 3.4 SRAM 8T with Dynamic Feedback Control using MOSFET [1]

The circuit in Figure 3.4 consists of 8 transistors namely, as M1 to M8. There are several signals as inputs which are WWL, RWL, that is Write Word Line and Read Word Line.

RBL and WBL which are Read Bit Line and Write Bit Line. FCS1 and FCS2 as the control signals. Q and QB are the SRAMs complementary nature outputs. The transistors are put up in such a way to perform as an SRAM as per the truth table given in Table 3.1.

	Hold	Read	Write 1	Write 0
WWL	0	0	1	1
RWL	0	1	0	0
FCS1	1	0	0	1
FCS2	1	0	1	0
WBL	1	1	1	0
RBL	1	Dis-charge	1	1

Table 3.1 Truth Table for SRAM with Dynamic Feedback Control

The configuration of 8T SRAM with Dynamic Feedback Control as shown in Figure 3.4 is implemented on Synopsys HSPICE tool under 22nm MOSFET technology. The width of PMOS is taken as 60nm and the width of NMOS is taken as 44nm. Next GNRFET is studied, which similar to MOSFET but consists of a GNR lattice as shown in Figure 3.5 b) part of the image. In the channel of the GNRFET the GNR lattice is fixed. The number of GNRs per GNRFET can be varied with the value of N, which the number of GNRs in lattice. The SPICE model is taken from Silicon industry models taken from the link- https://nanohub.org/resources/17074. [13] More parameters associated with the GNRFET are explained in the next session of proposed work.

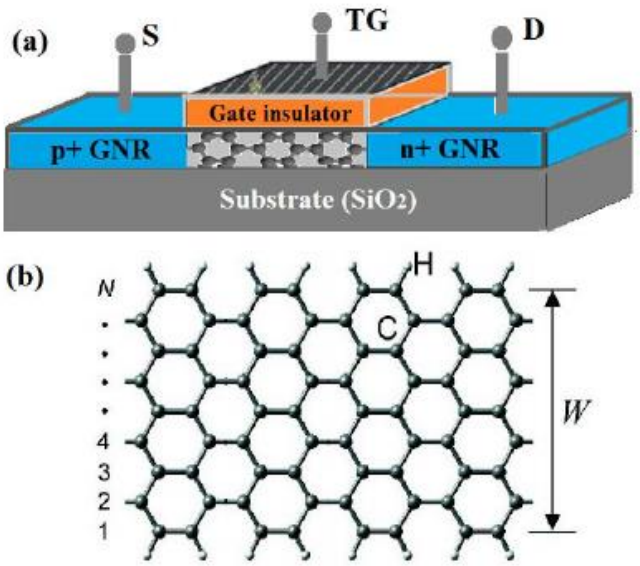

Figure 3.5: GNRFET a) Transistor Structure b) GNR lattice

The GNRFET gadget structure is fundamentally the same as MOSFET and is appeared in Figure 3.5. Regular Source design is portrayed in the Figure. The positive voltage at the back gate prompts the electron direct development in the GNR. The drain current is constrained by voltage at the top gate. The essential electron thickness is actuated by the back gate voltage. Numerous channels of GNR are designed on the substrate framing a multi-channel gadget. [12] The main material and methods for this research were briefly explained in this section, now these are combined in the next section of the proposed work of SRAM with GNRFET.

CHAPTER 4

DESIGN AND IMPLEMENTATION

4.1 PROPOSED WORK

This section proposes the circuit for 9T SRAM with dynamic feedback control in GNRFET 22nm with a Power Gating mode. The circuit consists of all GNRFETs and one more added transistor M9 in the main power supply path of the circuit. The circuit is shown in Figure 4.3 The signals for which are same as the previous one and the working is also as per the 8T SRAM. This circuit using the SPICE model of GNRFET is implemented on HSPICE by the use of node coding for each transistor. After which a transient analysis is performed on the circuit for proper analysis. There are basically three modes for the SRAM working which are Read, Write and Hold Mode as depicted from the truth Table 4. in Table 4. 1 also. The circuit is tested in all modes for proper analysis.

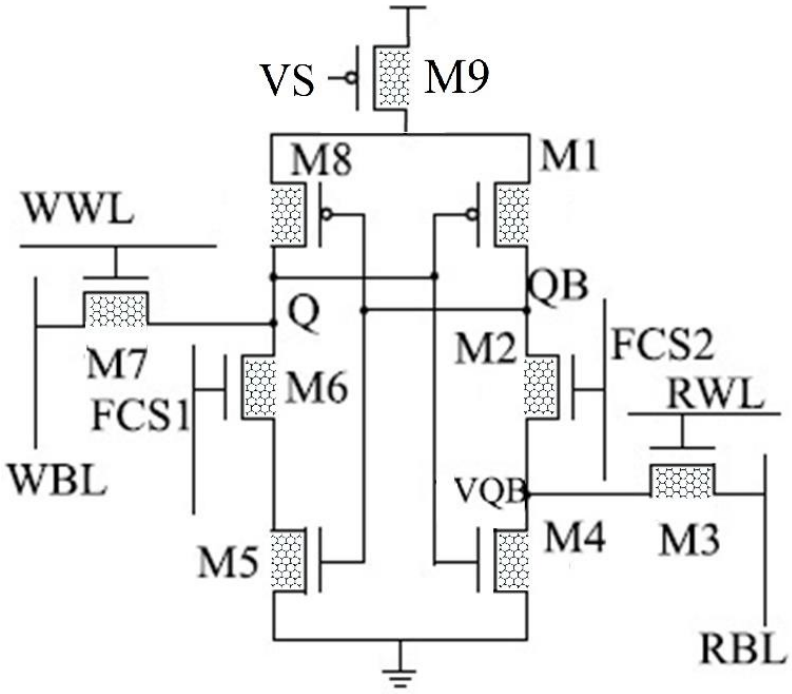

Figure 4.3 Proposed SRAM 9T using GNRFET and Power Gating with Dynamic Feedback Control

In Table 4. 2, the parameters for the GNRFET implementation and shown with meaning and values taken which gives the better improved circuit for SRAM based on Dynamic Feedback Control. The transient analysis performed in the circuit is from 1ns to 40ns. The calculated performance metrics are Average Power Consumption, Delay, Power Dissipation, PDP (Power Delay Product) and Leakage Current. The power dissipation is also analyzed in each of the modes for Read, Write and Hold modes. Also in Figure 4. 4 and Figure 4. 5 the write Mode waveforms of the implementation are shown.

GNRFET Parameters	Description	Value Taken
NRib	No. of GNR in Device	6
N	No. of Dimer Lines in the Lattice of GNR	12
Tox	Top Dielectric Material Thickness	0.95nm
sp	In one device spacing between two GNRs	2nm
dop	Source and drain doping fractions	0.001
p	Edge roughness fraction percentage	0
L	Length	22nm

Table 4. 2: Parameters Taken for GNRFET Implementation

The parameters shown in the Table 4. 2 are considered for improvement in the GNRFET based SRAM with DFC. These parameters basically improve the width effective of the GNRFETs which reduces the short channel effects in the transistor thereby giving a better performance.

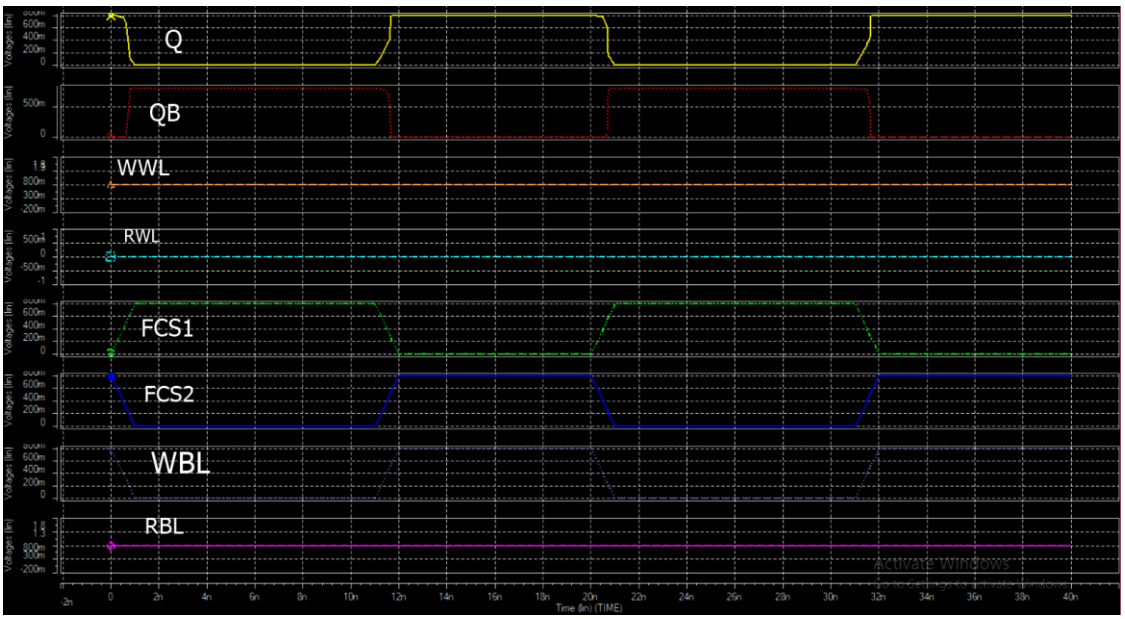

Figure 4.4 Waveform for SRAM8T MOS

In Figure 4.4 and Figure 4.5, the signals Q and QB are coming complementary which are in write mode of the SRAM in Dynamic Feedback Control. Both images in the waveforms shows that the working is same but the performance parameters are improved which are seen in the results section. The waveforms are taken using Avanwaves software which is a part of Synopsys HSPICE tool.

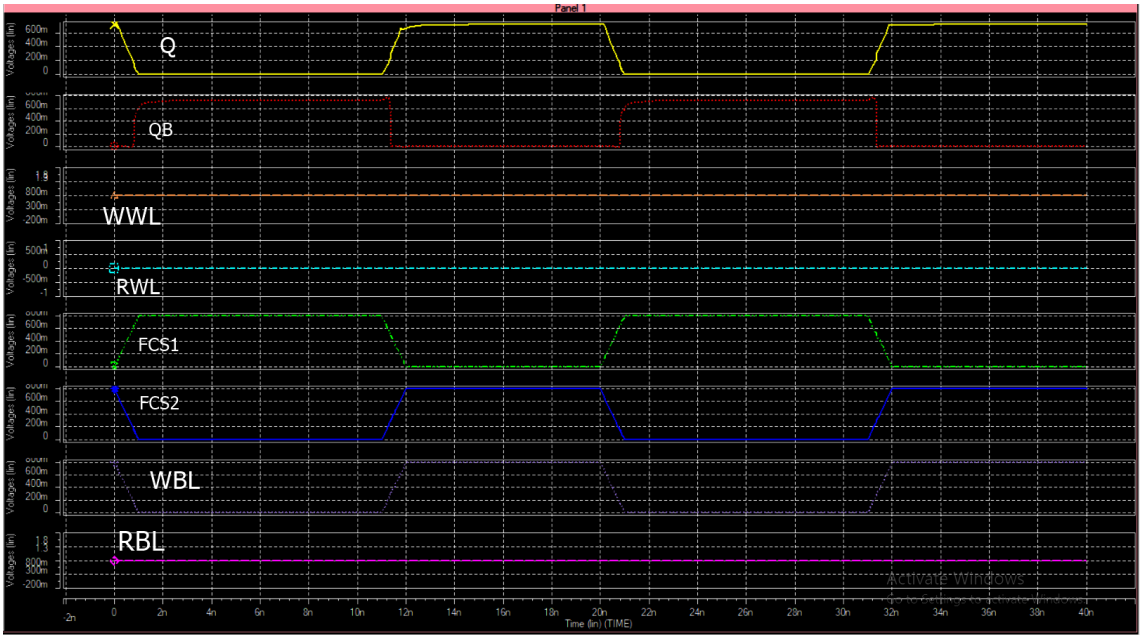

Figure 4.5 Waveform for SRAM 9T Proposed using GNRFET and Power Gating technique

4.2 RESULTS

In this segment the simulation results are presented. The implemented circuits for SRAM 8T based on MOSFET and SRAM 9T power gated based on MOSFET are made on 22nm technology in HSPICE. They are compared with the proposed 9T GNRFET based SRAM with Power Gating and Dynamic Feedback Control.

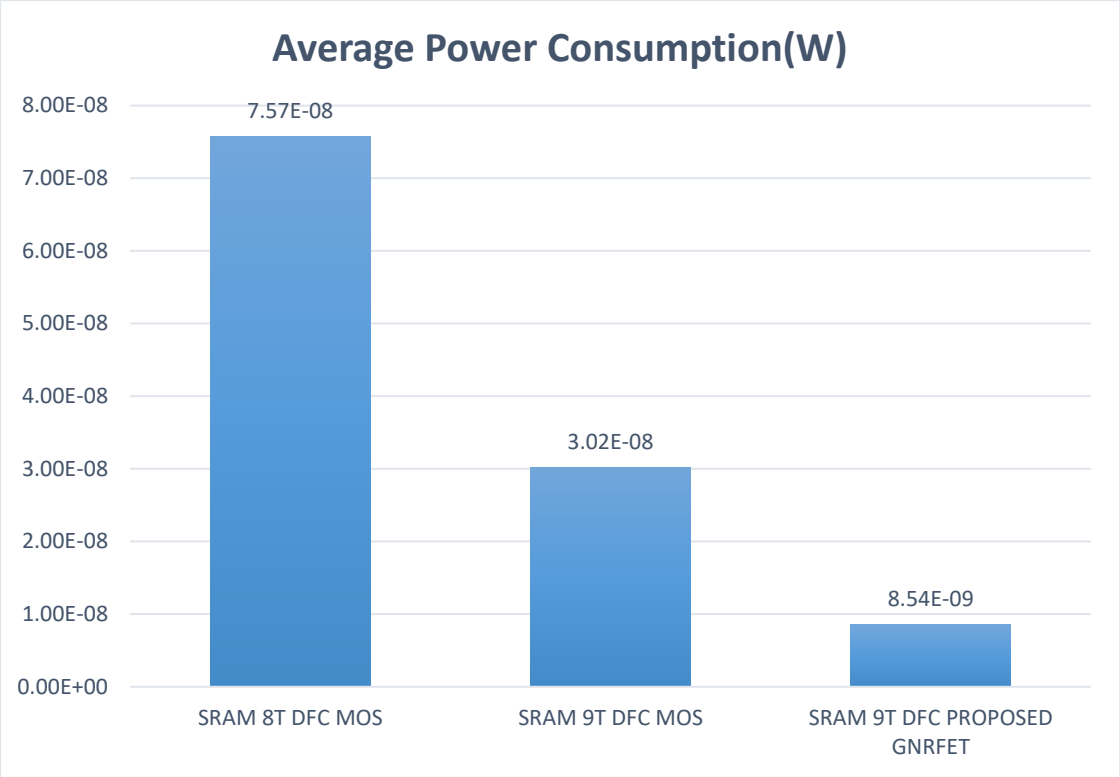

Figure 4.6 Average Power Consumption for SRAM8T MOS, SRAM9T Power Gated MOS and SRAM 9T Proposed using GNRFET and Power Gating

In Figure 4. 6, Average Power Consumption in full Write Mode is shown which shows that the SRAM 9T Proposed GNRFET performs the best. In Figure 4. 7, the lowest delay is in SRAM 9T proposed GNRFET based circuits which makes it high speed also.

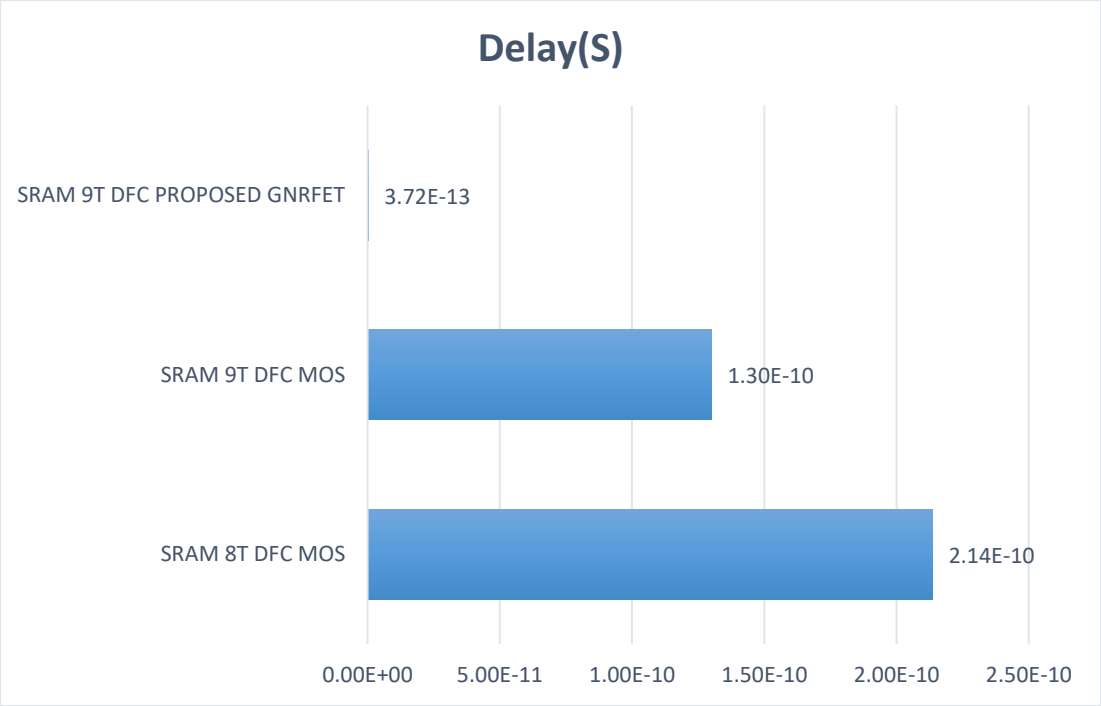

Figure 4.7 Delay for SRAM8T MOS, SRAM9T Power Gated MOS and SRAM 9T Proposed using GNRFET and Power Gating

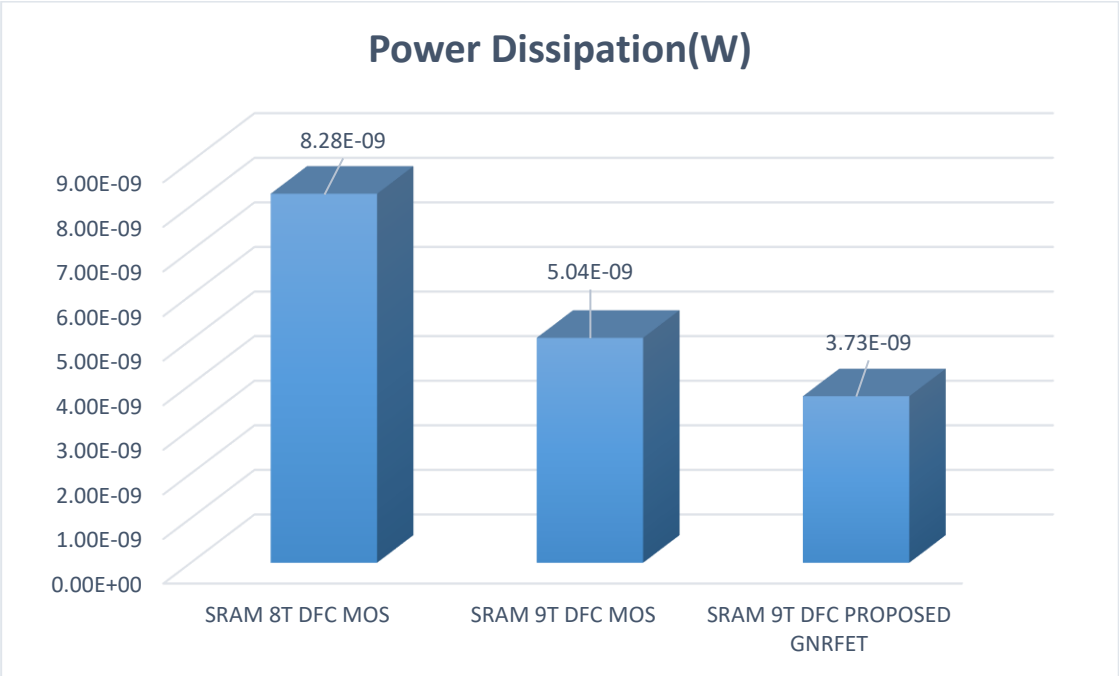

Figure 4.8 Power Dissipation for SRAM8T MOS, SRAM9T Power Gated MOS and SRAM 9T Proposed using GNRFET and Power Gating

In Figure 4.8 and Figure 4.9 the Power Dissipation and PDP results are shown which when compared with the SRAM MOSFET based GNRFET 9T SRAM is performing best in PDP efficiency and Power Dissipation also. All of these are taken into consideration in full write mode, which means incudes both write 1 and write 0 logics for the SRAM with Dynamic Feedback Control.

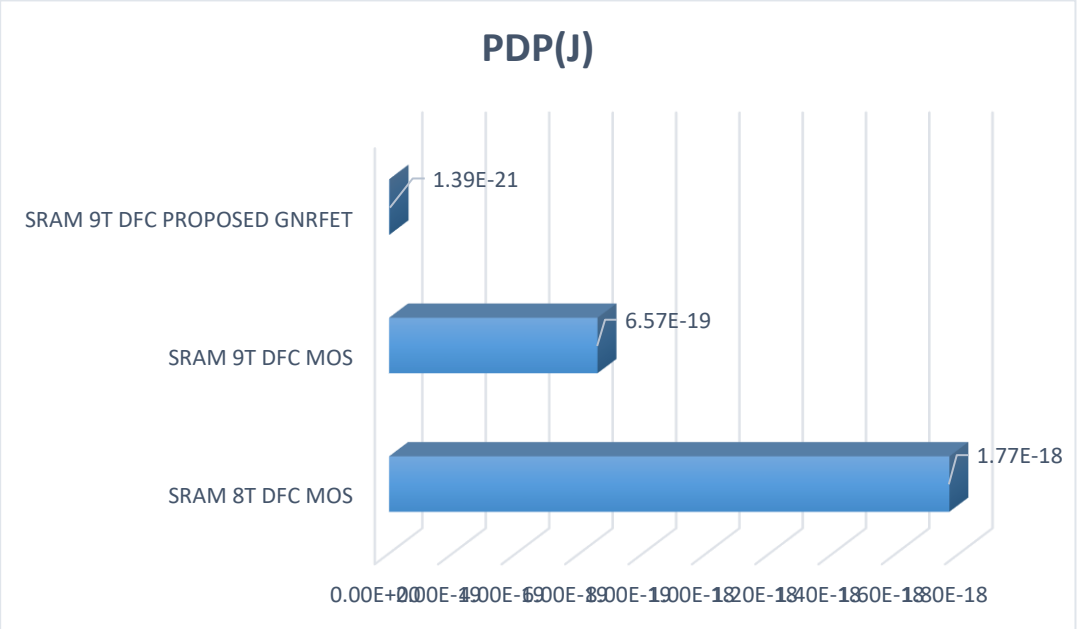

Figure 4.9 PDP for SRAM8T MOS, SRAM9T Power Gated MOS and SRAM 9T Proposed using GNRFET and Power Gating

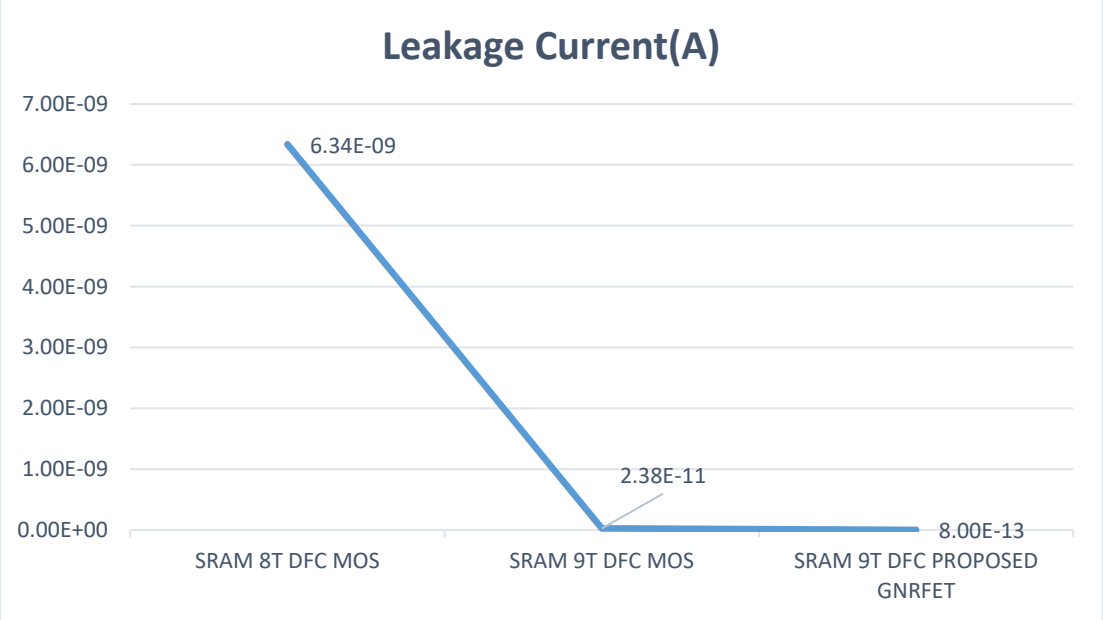

Figure 4.10 Leakage Current for SRAM8T MOS, SRAM9T Power Gated MOS and SRAM 9T Proposed using GNRFET and Power Gating

In Figure 4.10 leakage current in the write mode chart comparison is shown, which is best for the proposed GNRFET based 9T SRAM.

	SRAM 8T DFC MOS	SRAM 9T DFC MOS	SRAM 9T DFC PROPOSED GNRFET
Average Power Consumption(W)	7.57E-08	3.02E-08	8.54E-09
Delay(S)	2.14E-10	1.30E-10	3.72E-13
Power Dissipation(W)	8.28E-09	5.04E-09	3.73E-09
PDP(J)	1.77E-18	6.57E-19	1.39E-21
Leakage Current(A)	6.34E-09	2.38E-11	8.00E-13

Table 4.3 Simulation Results for Various Performance Metrics in SRAMs with Dynamic Feedback Control

In Table 4.3, all the simulation results are shown in tabular form for easier understanding and shows that in all of the performance metrics proposed circuit of SRAM with DFC and GNRFET has the best performance.

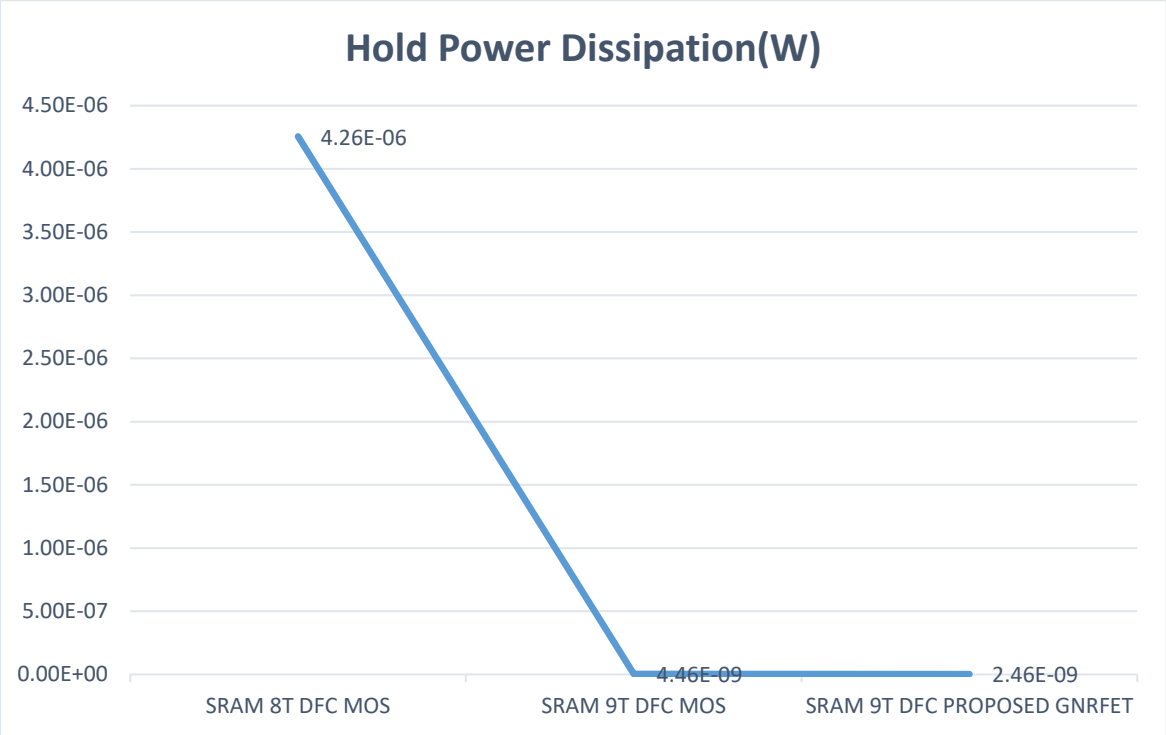

Figure 4.11 Hold Mode Power Dissipation for SRAM8T MOS, SRAM9T Power Gated MOS and SRAM 9T Proposed using GNRFET and Power Gating

In Figure 4.11, hold mode power dissipation chart is shown. In hold mode, highest power dissipation is for the MOSFET based SRAM due to short channel effects and lowest in the proposed GNRFET based SRAM with DFC.

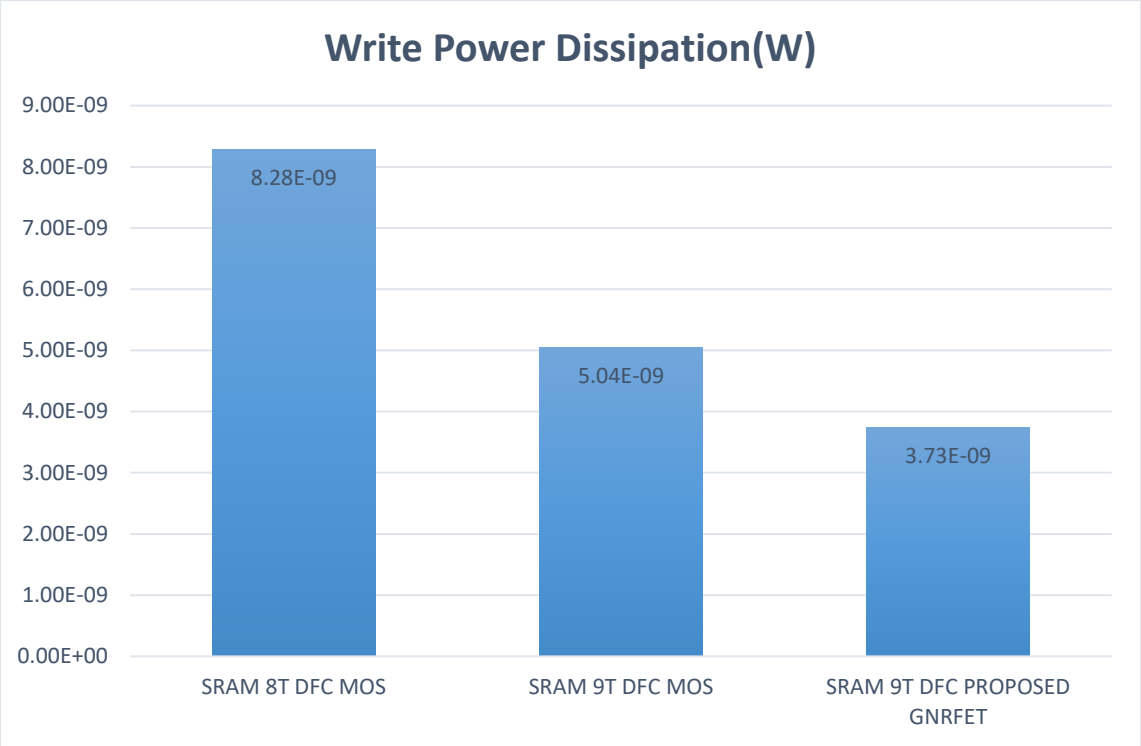

Figure 4.12. Write Mode Power Dissipation for SRAM8T MOS, SRAM9T Power Gated MOS and SRAM 9T Proposed using GNRFET and Power Gating

In Figure 4.12, write mode power dissipation chart is shown. In write mode also, highest power dissipation is for the MOSFET based SRAM and lowest in the proposed GNRFET based SRAM with DFC. Similarly, in Figure 4. 13 also the lowest read mode power dissipation is seen the case of SRAM 9T DFC Proposed GNRFET based circuit.

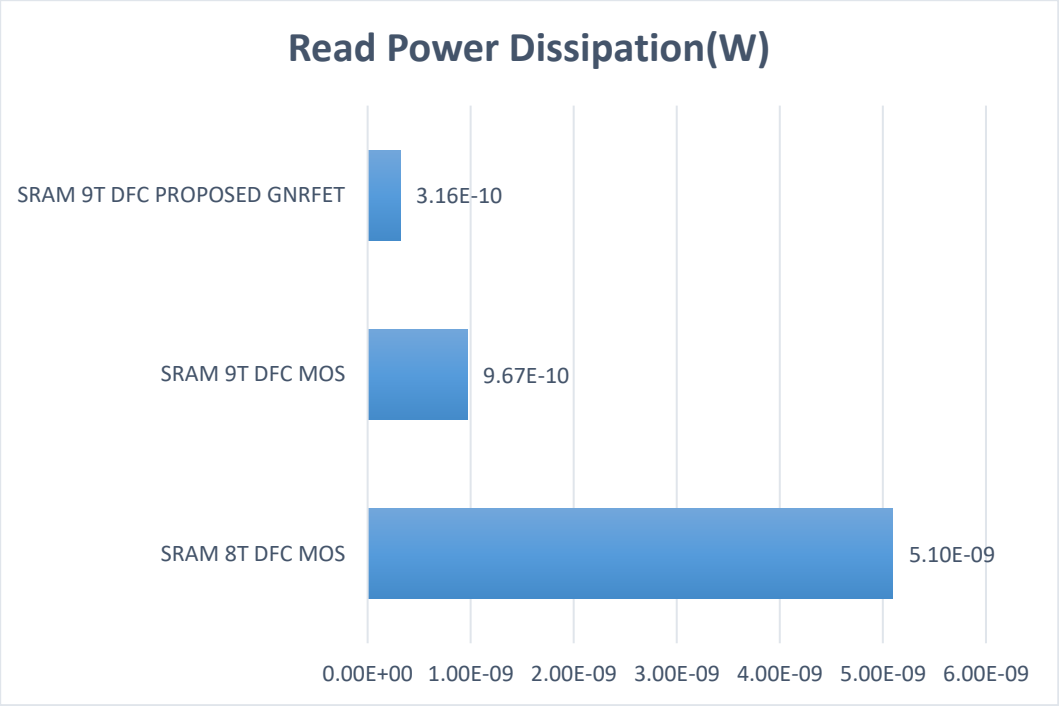

Figure 4.13 Read Mode Power Dissipation for SRAM8T MOS, SRAM9T Power Gated MOS and SRAM 9T Proposed using GNRFET and Power Gating

In Table 4.4, all three mode based power dissipation are shown in tabular form which shows that the proposed circuit is best in performance for power dissipation with use of GNRFET and power gating. Further these results are taken from HSPICE software from the output file known as. lis file.

	SRAM 8T DFC MOS	SRAM 9T DFC MOS	SRAM 9T DFC PROPOSED GNRFET
Hold Power Dissipation(W)	4.26E-06	4.46E-09	2.46E-09
Write Power Dissipation(W)	8.28E-09	5.04E-09	3.73E-09
Read Power Dissipation(W)	5.10E-09	9.67E-10	3.16E-10

Table 4. 4: Simulation Results for Write, Read and Hold Mode Power Dissipation in SRAMs with Dynamic Feedback Control

CHAPTER 5

CONCLUSION AND FUTURE ENHANCEMENTS

5.1 CONCLUSION

In this paper, the simulation results are taken from HSPICE software. The utilization of GNRFET SRAM over MOSFET SRAM in the proposed strategy diminishes Average Power utilization; it showed that GNRFET is a promising substitute for MOSFET SRAM past 22nm innovation. The decreased short channel direct impacts in GNRFET SRAM and better command over the gate of the GNRFET SRAM improves the Average Power in planned strategies. As of now appeared in recreation results, the proposed strategy has the most reduced voltage source power dissemination, this is accomplished at the lower delay in the proposed procedure by GNRFET SRAM. The Delay, PDP and Leakage Current are improved in the circuit by about 99% with Average Power being improved by 71%. Power Dissipation is improved by nearly 28%. The future scope of this work includes the implementation in 16nm or below, other transistor technologies like DGFET (Double Gate Field Effect Transistors), MGFET (Multi-gate Field effect transistors), SOIFET (Silicon on Insulator FET) can also be used in Dynamic Feedback Control for further research. Application of the proposed work finds use in all the memory based ICs such as microcontrollers and heavy end processors where portability, power and speed of the device is a major concern.

5.2 APPLICATIONS

GNRFETs have been appeared to have unrivaled on-current and off-current when contrasted with a customary transistor at a similar innovation hub. Their double door structure can be abused for inventive circuit plan. E.g., if a converse predisposition is applied to the back entryway of IG-mode GNRFETs, the limit voltage Vth of the front door can be regulated. Since Vth impacts both the subthreshold current and postponement of a transistor, it very well may be utilized as a handle to make delay-spillage exchange offs. Low force plan in computerized circuit, for example, RAM, as a result of its low off-state current. Force speaker or other application in simple zone which requires great linearity.

5.3 SCOPE OF FUTURE ENHANCEMENT

Innovation scaling has given us expanded circuit execution in the course of recent decades. The business has scaled the customary transistors for as far back as six years utilizing a few creative strategies, for example, high-k dielectrics and stressed silicon. In any case, scaling of ordinary transistors past the 22nm hub is extremely troublesome because of short-channel effects, for example, drain-prompted boundary bringing down (DIBL), sub edge incline and sub limit spillage current. DGFETs have risen as a potential answer for proceed with innovation scaling. Such FETs have two doors to control the convergence of the electrons in the channel and accordingly have unrivaled electrostatic uprightness. The two doors relieve the effect of the drain-source electric field in the channel and in this manner give unrivaled channel control. Among DGFETs, GNRFET have risen as the most practical arrangement because of their simplicity of creation. The manufacture procedure of GNRFETs is very like the creation procedure of traditional transistors. The tri-door adaptation of GNRFETs was as of late reported by Intel as its decision of transistor for manufacturing processors at the 22nm innovation hub.

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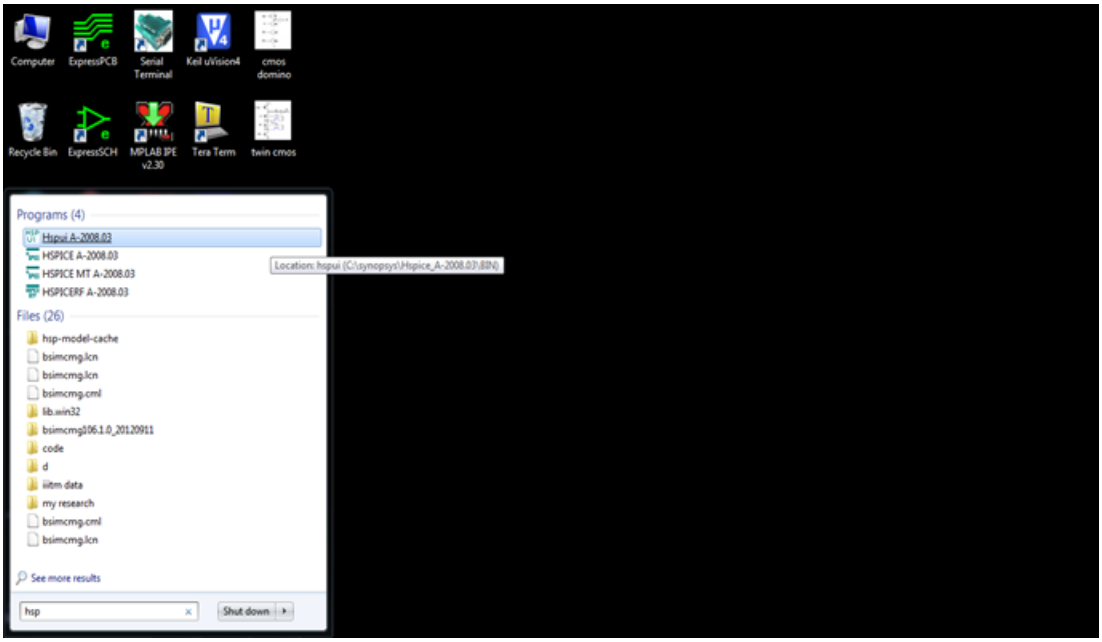
APPENDIX A

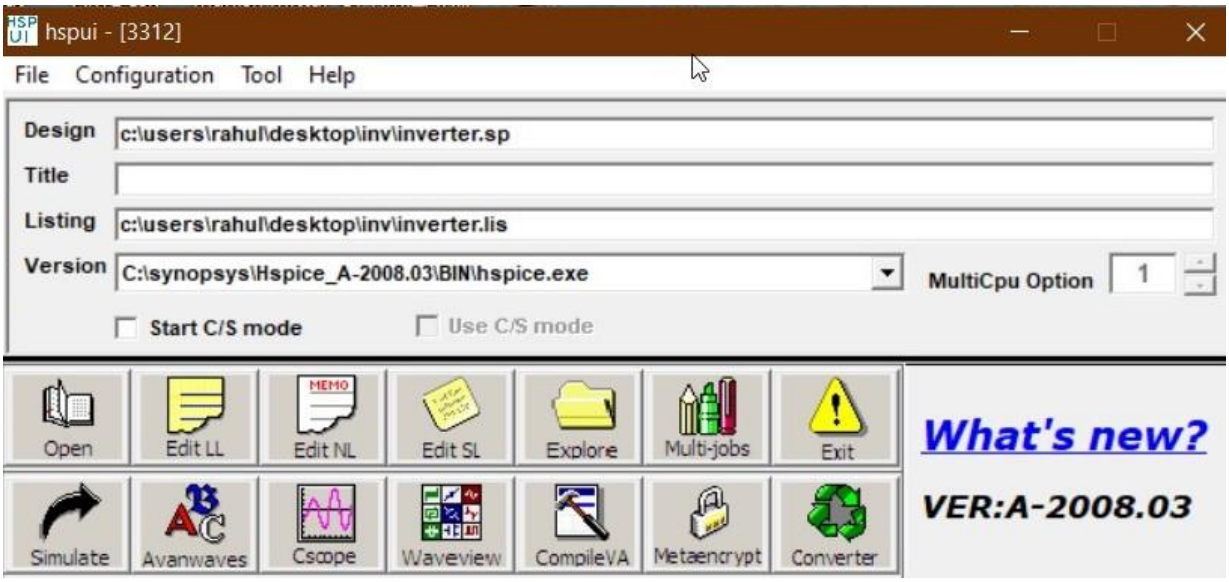
HSPICE

Synopsys HSPICE is an optimizing analog circuit simulator. You can use it to simulate electrical circuits in steadystate, transient, and frequency domains. HSPICE is unequalled for fast, accurate circuit and behavioral simulation. It facilitates circuit-level analysis of performance and yield, by using Monte Carlo,
worst-case, parametric sweep, and data-table sweep analyses, and employs the most reliable automatic-convergence capability (see Figure 1).

Here are the steps to use the HSPICElets start to simulate your design with HSPICE.

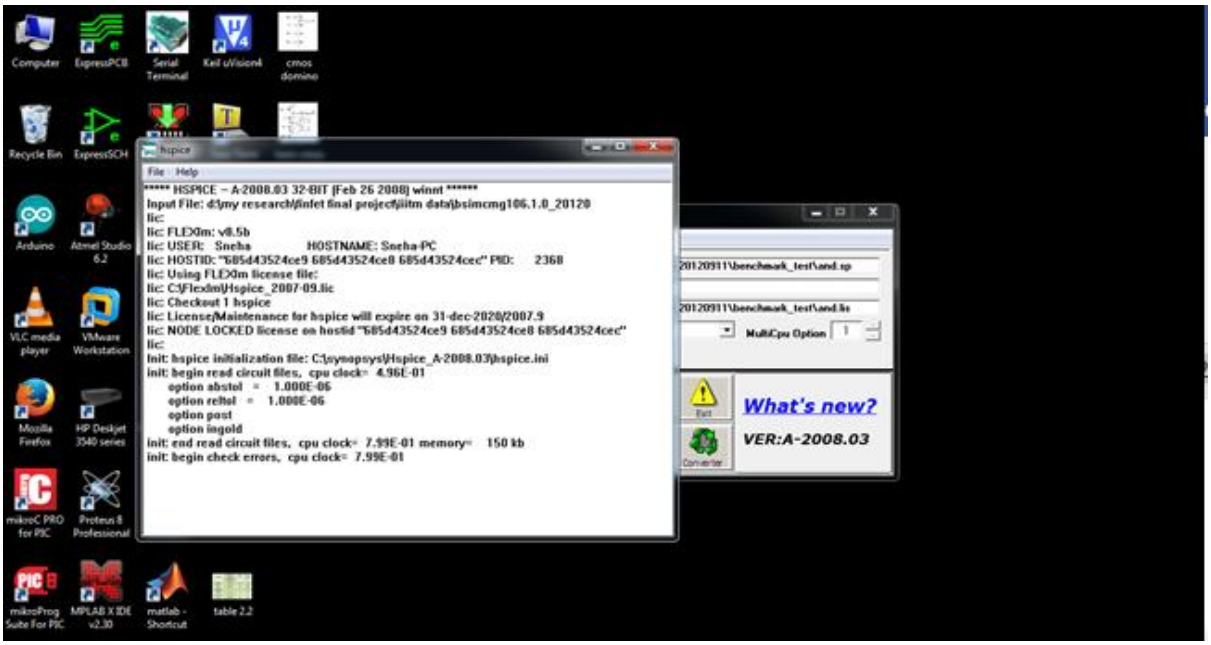
Step 1) Open the HSPICEpui





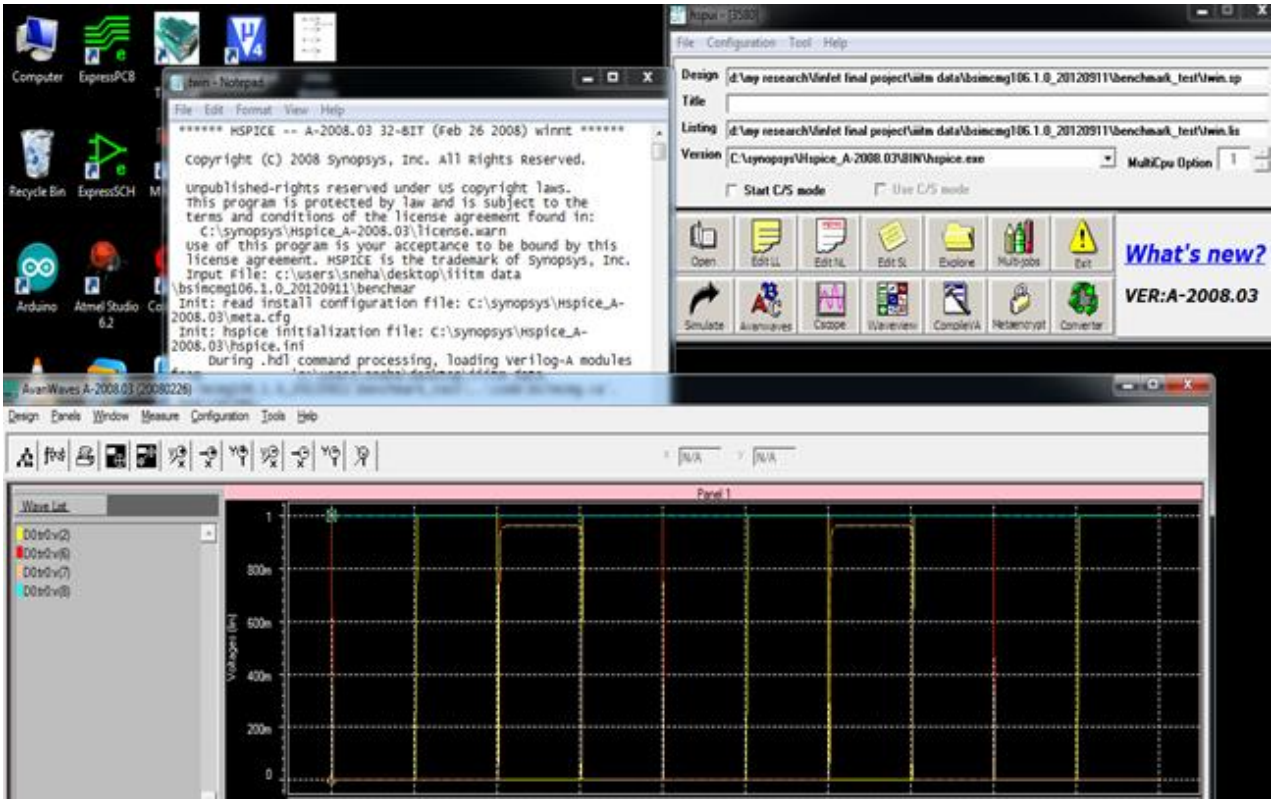
2) Click the OPEN Button to open the design file or the code file you wrote. Browse your design file in the design section and left rest of the thing.

3) Now click the Simulate button .

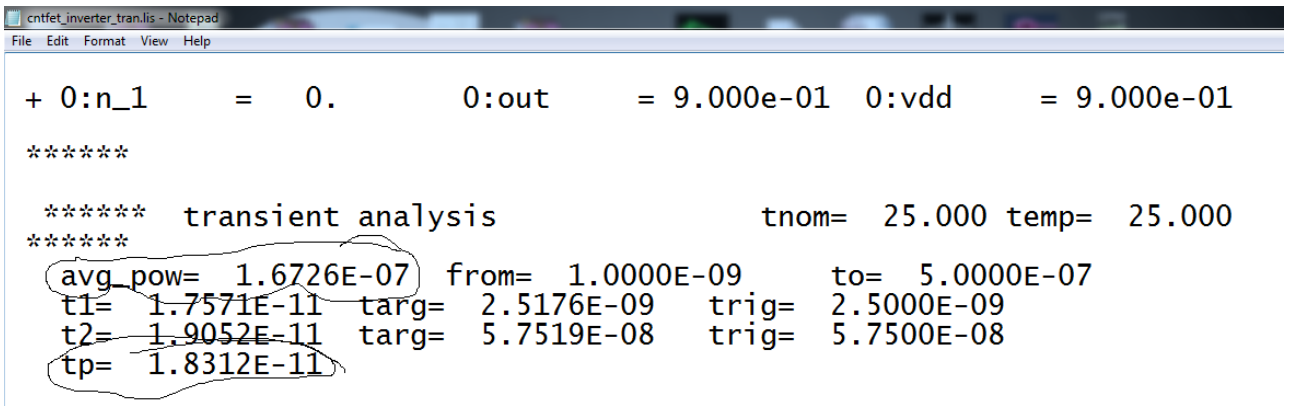


4) Now open the 'Avanwaves' to view your pulses or the output.

5) Now click the operating points you want to view like in my case i double click on vin and vout and see the wave form.



6) Now click on the Editll to view your result like Power , Propagation Delay.



APPENDIX B

BASIC SPICE COMMANDS

Voltage source: The command will start with v to defining the voltage source and are using two types of voltage source DC and PULSE

DC SOURCE

SYNTAX: Vname N+ N- <DC > Value

Where: Vname is the name of voltage source

DC for defining the source as dc source

N+ is the positive terminal

N– is the negative terminal

Example: VVoltageSource_1 VddGnd DC 1.0

PULSE SOURCE

SYNTAX: Vname N+ N- PULSE(Vo V1 Td TrTf Tw To)

Where: Vname is the name of voltage source

N+ is positive terminal

N- is ground terminal

PULSE is the type of voltage source

Vo is initial voltage

V1 is final voltage

Td is initial delay time

Tr is rise time

Tf is fall time

Tw is pulse width

To is period of wave

Example: VVoltageSource_2 clkGnd PULSE(0 1.0 0n 5n 05n 30n 100n)

.include

This statement is use to include the file or subciruits in the current circuit.

SYNTAX: .include 'filename'

Where: ‘filename’ is the path of the file

.lib

To create and read from libraries of commonly-used commands, device models, subcircuit analysis, and stat ements in library files, use the.LIB call statement. As HSPICE or HSPICE RF encounters each .LIB call name in the main data file, it reads the corresponding entry from the designated library file, until it finds an .ENDL statement.

SYNTAX: .lib 'filename'

Where: ‘filename’ is the path of the file

.TRAN Statement

This statement specifies the time interval over which the transient analysis takes place, and the time increments. The format is as follows:

SYNTAX: .TRAN TSTEP TSTOP <TSTART <TMAX>><UIC>

Where: TSTEP is the printing increment.

TSTOP is the final time

TSTART is the starting time (if omitted, TSTART is assumed to be zero)

TMAX is the maximum step size

UIC stands for Use Initial Condition and instructs HSPICE not to do the quiescent operating point before beginning the transient analysis. If UIC is specified, HSPICE will use the initial conditions specified in the element statements.

.PRINT and .PLOT

These statements will instruct HSPICE what output to generate. If you do not specify an output statement, HSpice will always calculate the DC operating points. The two types of outputs are the .PRINTs and .PLOTs . A print is a table of data points and a plot is a low-resolution graphical representation.

SYNTAX: .PRINT TYPE OV1 OV2 OV3

.PLOT TYPE OV1 OV2 OV3

in which TYPE specifies the type of analysis to be printed or plotted and can be DC, TRAN or AC.

The output variables are OV1, OV2 and can be voltage between nodes, the voltage between a node and ground. With currents, you can also specify the currents between nodes and more importantly, the currents running through a particular voltage source, which is useful for power consumption. In addition, you can define the type of output by simply putting a suffix after V or I. The suffixes are:

· M: Magnitude
· DB: Magnitude in dB (deciBels)
· P: Phase
· R: Real part
· I: Imaginary part

.MEASURE

.MEASURE is often used in circuit optimization. With it, you can find when a certain event occurs as you sweep various parameters. You can use .MEASURE for finding:

- Rise ,Fall and Time Delay

- Average, RMS, min, max, peak-to-peak and integral
    - Find X when Y occurs
    - Derivative and Integral Evaluation
    - Equation Evaluations

.END

the end statement of the circuit is always be .END. This statement must be a line by itself, followed by a carriage return!