DESIGN AND STUDY OF NANOSCALE TRENCHED GATE MOSFET: A TCAD NUMERICAL STUDY

A DISSERTATION

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I, HARSHIT SONI, Roll No. 2K18/C&I/09 student of M. Tech (Control and Instrumentation), hereby declare that the Project dissertation titled "**DESIGN AND STUDY OF NANOSCALE TRENCHED GATE MOSFET**" which is submitted by me to the Department of Electrical Engineering, Delhi Technological University in partial fulfillment for the award of the degree of Master of Technology is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship, or other similar title or recognition.

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ABSTRACT

This Project presents T-CAD simulation of buffered trench gate MOSFET (BTG-MOSFET), and GaN buffered trench gate MOSFET (GaN-BTG MOSFET). The electrical attributes of the devices are contrasted with conventional trench gate MOSFET (CTG-MOSFET). A comparative study between various performance factors, for example, electric field, electron velocity, electron mobility, the threshold voltage (V_{th}), and sub-threshold swing (SS) of the devices has been performed. Results uncover a 43.85% improvement in SS and 9.83% decrement in V_{th} for GaN-BTG-MOSFET. Further in this report, GaN-BTG-MOSFET's parameters are concentrated with variation in channel length, Effective Oxide thickness (t_{ox}), and Doping concentration. Thermal reliability of GaN- BTG-MOSFET for application in Integrated Circuits (ICs) at high temperatures (300K to 600 K) is examined. An intensive near examination of electrical characteristics GaN-BTG-MOSFET has been carried out. GaN-BTG MOSFET acts as a promising structure for further downsizing of the trenched gate MOSFET and guarantees better performance for sub-micrometer MOSFET.

Thermal reliability of GaN-BTG-MOSFET for application in Integrated Circuits (ICs) at high temperatures (300K to 600K). An intensive relative investigation of electrical characteristics, for example, transconductance, transfer characteristics, leakage current, and the electric field of the designed devices have been performed using the TCAD Atlas tool. A detailed discussion is introduced on the thermal stability of the device at high temperatures (300-600K). Report additionally presents the performance factors, for example, On-Resistance (R_{on}), leakage current, and threshold voltage (V_{th}). Results recommend that the introduction of GaN instead of silicon in a trenched gate structure not just improves the device's performance at room temperature (300K) yet additionally enhances the thermal stability of the device. The performance of GaN-BTG-MOSFET at high temperatures when contrasted with CTG MOSFET suggests that it tends to be utilized in ICs and shows preferred thermal stability than silicon-based devices.

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LIST OF SYMBOLS AND ABBREVIATIONS

S. No:	PARTICULARS
1.	TCAD: Technology Computer-Aided Design
2.	MOSFET: Metal Oxide Semiconductor Field Effect Transistor
3.	CTG MOSFET: Conventional Trenched Gate MOSFET
4.	BTG MOSFET: Buffer Trenched Gate MOSFET
5.	GaN-BTG MOSFET: Gallium Nitride Buffer Trenched Gate MOSFET
6.	V_{th}: Threshold Voltage
7.	SS: Sub-Threshold Swing
8.	t_{ox}: Oxide Thickness
9.	ICs: Integrated Circuits
10.	R_{on}: On- Resistance
11.	IGFET: Insulated Gate Field Effect transistor
12.	BJT: Bipolar Junction Transistor
13.	g_m: Transconductance
14.	I_d: Drain Current
15.	I_s: Saturation Current
16.	V_{gs}: Gate to Source Voltage
17.	V_{ds}: Drain to Source Voltage
18.	L_g: Gate Length
19.	I_{on}: On current
20.	I_{off}: Off current
21.	HfO_2: Hafnium Oxide
22.	SiO_2: Silicon dioxide
23.	eV: electron-Volt
24.	EOT: Equivalent Oxide Thickness
25.	C_{ox}: Gate oxide capacitance
26.	nm: nano-meter

CHAPTER - 1

INTRODUCTION

1.1 BACKGROUND

TODAY, most of the IC applications are based on MOSFET technology[1], MOSFET is a voltage-controlled electronic device having three terminals drain, gate, and source. The potential at the gate terminal controls the conductivity in the channel. MOSFET is a unipolar electronic device as conduction of current is carried by either electrons or holes. The conducting path among source and drain is regularly termed as channel. The potential at the gate is varied to control the width of the channel. In MOSFET gate terminal is not physically connected with the substrate.

The conductivity among source and channel is exceptionally subject to the applied potential at the gate terminal, this is the principle used for amplification and switching. MOSFET is likewise named as IGFET (Insulated Gate Field Effect Transistor). MOSFET has a preferred position over ordinary BJT as it requires no input current to control a large current.

MOSFET is mainly defined into two types in terms of fabrication:

- **N-Channel MOSFET (NMOS)**
- **P-Channel MOSFET (PMOS)**

N-Channel MOSFET:

- In NMOS, source and drain are comprised of n+ type Silicon while the substrate is comprised of p-type Silicon.
- In NMOS, the gate is biased by applying the positive potential and attracts the electrons of p-type substrate.

- In NMOS the drain and source are fabricated of n+ silicon while the substrate is fabricated of P silicon.
- The gate of NMOS is made of a layer of polysilicon.
- SiO_2 is a dielectric material NMOS behaves as a capacitor, Gate terminal and inversion layer behaves as its electrodes.
- When positive voltage is applied at the NMOS gate, it alters the charge distribution in device. increasing potential, the holes present under the oxide layer will experience a force of repulsion and holes move downward[2]. The depletion region will be aggregated by the bound negative charges which are connected with acceptors ions.

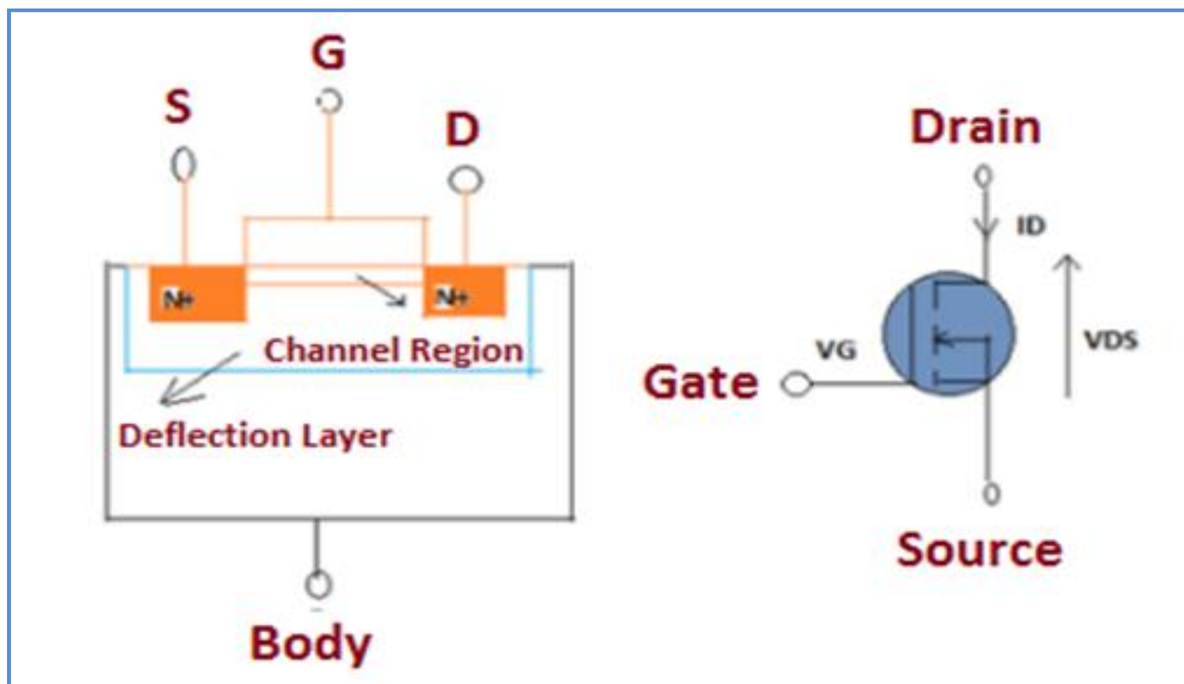


Fig.1: N CHANNEL MOSFET

The development of the electron channel is controlled by the positive potential applied to the gate terminal. On increasing the positive potential at the gate terminal, it will attract more electrons In this way, expanding the channel path between source and drain terminals.

Thus, increasing the positive potential at the gate terminal increases the conductivity of the NMOS. For a fixed value of V_{ds}, the value of transconductance can be found as $g_m = \Delta I_d / \Delta V_{ds}$ This ratio is transconductance abbreviation of "transfer conductance". The SI unit of transconductance (g_m) is Siemens or mho. The voltage gain of MOS increases with the increment in transconductance.

At V_{gs}=0, enhancement type NMOS behaves as an open switch (normally off), because of no channel in NMOS channel around the gate. This region is defined as cutoff region. The OFF condition of the NMOS is represented by dotted line, and the depletion region is shown by a continuous line, depicting the conduction region of the NMOS.

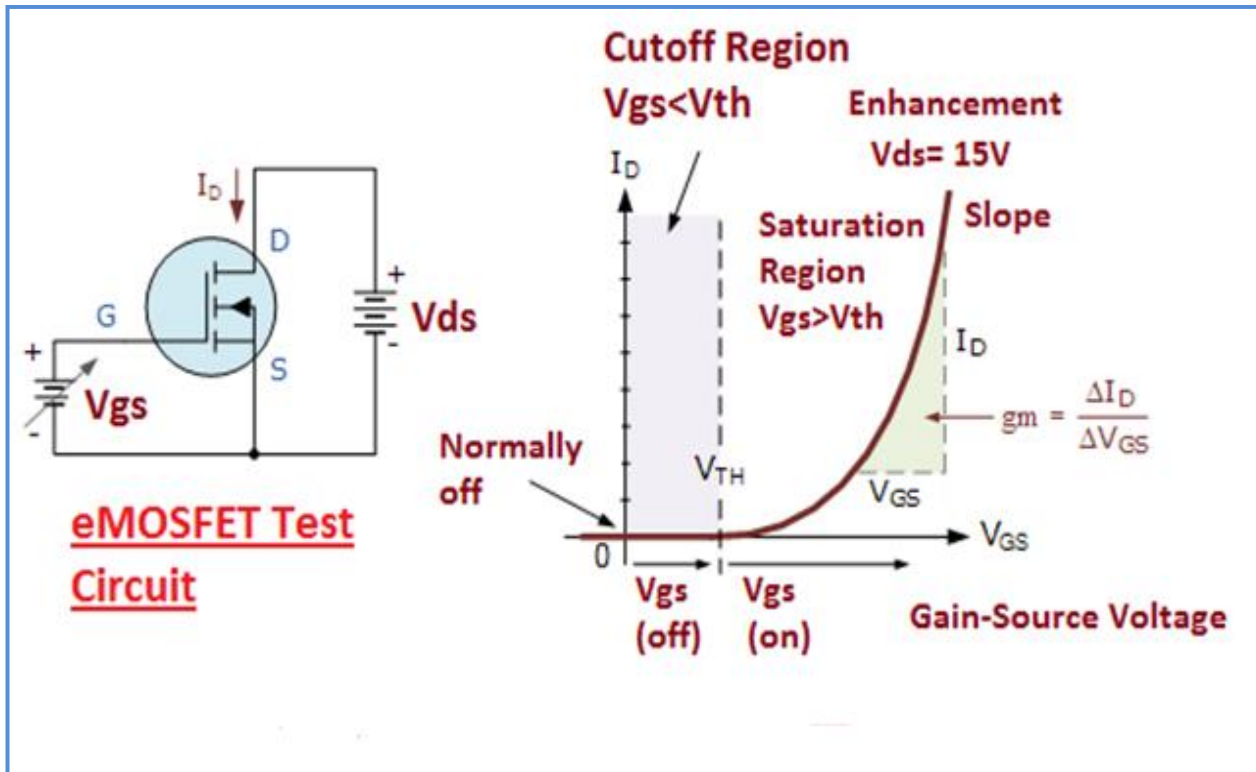


Fig 3:V-I Characteristics of MOSFET

Applying gate-source voltage V_{gs} at the gate terminal, it starts to conduct between the region of source and drain. The potential at which NMOS starts conducting is known as threshold voltage and is represented by V_{th}. Increasing the gate-source voltage allows the conducting channels to go wider and increase the drain current (I_d).

The gate terminal is never in contact with the inverting channel and is practically isolated from the conducting channel. MOSFET encompasses high input impedance which is useful for amplifying circuits. In the conduction or saturation region drain current can be calculated as:

$I_d = K(V_{gs} - V_{th}^2)$	;	$V_{gs} >= V_{th}$

The threshold voltage V_{th} and K(conduction parameter), From the VI characteristics, the slope of the characteristic curve increases with increase in drain current for a fixed drain-source voltage (V_{ds}). To operate the MOS in triode or saturation region, the gate terminal of the transistor must be biased more than its given threshold potential.

1.2 TRENCHED GATE MOSFET:

The invention of Bipolar Junction Transistor (BJT) in 1948 brought a revolution in the field of electronics, and since then, innovation is only moving forward and is still evolving to enhance current day technology.

With the introduction of MOSFET in 1959, a new dimension of innovation was discovered, and since then, various researchers have invested their time in further developing this technology, and one such enhancement was scaling down the size of the device. To counter the impacts of short channel, different structures were proposed and one of the promising types is trenched gate structure[3]. Although this structure helps in decreasing short channel effects, some decrement in Saturation current (I_s) can be seen alongside an increase in the limit voltage (V_{th}).

This analysis introduces the stacking of Hafnium Oxide (HfO_2) with Silicon dioxide (SiO_2) at gate terminal in conventional trenched gate (CTG) structure, to use the advantages of the structure and up-scale its performance by improving the saturation current and threshold voltage. Hafnium Oxide(HfO_2) is an insulator and acts as a buffer layer[4] in between SiO_2 and gate electrode. Its high dielectric constant aides in accomplishing higher oxide capacitance,

which brings out a further gain in the saturation current of MOSFET and diminishes the formation of hot electrons.

Going above and beyond, we have presented GaN in place of Silicon wafer, in the same trenched gate structure. One of significant preferences of GaN is that it is conceivable to further scale down the size of the device with smaller on-resistance and higher breakdown voltage than is conceivable with Silicon. GaN has high electron mobility[5] which reasons an improved drain to source current. GaN shows a wide bandgap of 3.4 eV and has high warmth capacity[6], which makes it useful for high-temperature operation (400°C) applications and can be operated efficiently at high voltages. It has high electron mobility (1500 cm^2/volt-sec) than silicon[6], which implies it displays higher critical electric field strength than silicon. High mobility also accounts for quicker switching speeds respecting less switching losses[7].

GaN is developing as a significant material for MOSFET as its thermal stability superior to the silicon. Further presentation of GaN as the base device material instead of silicon improves the performance of trenched gate MOSFET when compared with a conventional MOSFET at room temperature of 300K. Nonstop utilization of gadgets may prompt the development of hotspots[8] in integrated circuits (ICs) which results in inappropriate working and breakdown of the semiconductors.

Henceforth it is critical to develop gadgets that can perform successfully at high temperatures for a long term. The performance of a device with increasing temperature can be interpreted from its different boundaries like transfer characteristics, transconductance, the threshold voltage (V_{th}), switching ratio, leakage current, saturation resistance, and Electric field. These parameters should be free of temperature variations or impact of temperature ought to be as least as could reasonably be expected. With the increase of temperature in thin gate oxide devices, leakage current increases[2].

To limit the leakage current and improve gate control, the equivalent oxide thickness (EOT) ought to be as low as possible[9]. For EOT to be a minimum, gate stacking is utilized where a high-K dielectric material Hafnium Oxide (HfO_2) is utilized to supplement Silicon Di Oxide (SiO_2) as a gate stacking material. Improved gate control is accomplished by increasing gate oxide capacitance (Cox). In this project, the performance of GaN-BTG-MOSFET is

analyzed and compared with CTG-MOSFET. Further parameters of GaN like doping concentration, oxide thickness, and channel length are varied and electrical parameters of the devices are analyzed and compared.

1.3 PROBLEM WITH SCALING OF MOSFET

- ✓ The internal electric fields in the device would increase if the power supply voltages are kept the same.
- ✓ The longitudinal electric fields and the transverse electric fields across the gate oxide, increase with MOSFET scaling.
- ✓ With an increase in temperature of device formation of hotspots can damage the MOSFET.
- ✓ Problems known as hot carrier effects and short channel effects.

The problems associated with SCEs:

- Threshold Voltage (V_{th}) roll-off
- Punch-through
- Gate tunneling/leakage current

This is an era of fast-developing technology. This advancement in the semiconductor industry is supported by innovation where the focus is on high-performance transistors with improved packaging density. Improved packaging efficiency can be associated with a reduction in the size of the transistor which is following Moore’s Law. Trenched gate MOSFET[10] is one recent design for effective reduction of device size without compromising with its performance.

Nowadays GaN is emerging as an important material for MOSFET as its thermal stability is better than the silicon. Further introduction of GaN as the base device material in place of silicon improves the performance of trenched gate MOSFET when compared with a conventional MOSFET at room temperature of 300K. Continuous usage of devices may lead to the formation of hotspots[8] in integrated circuits (ICs) which results in improper functioning and breakdown of the transistors. Hence it is important to develop devices that can perform effectively at high temperatures for a long duration.

The performance of a device with increasing temperature can be interpreted from its various parameters like transfer characteristics, transconductance, the threshold voltage (V_{th}), switching ratio, leakage current, saturation resistance, and Electric field. These parameters should be independent of temperature variations or the effect of temperature should be least. With the increase of temperature in thin gate oxide devices, leakage current increases[11].

To minimize leakage current and improve gate control, the equivalent oxide thickness (EOT) should be as low as possible. For EOT to be a minimum, gate stacking is used where a high-K dielectric material Hafnium Oxide (HfO_2) is used to complement Silicon Di Oxide (SiO_2) as a gate stacking material. Improved gate control is achieved by increasing gate oxide capacitance (Cox)[12]. In this paper, the performance of GaN-BTG-MOSFET is analyzed and compared with CTG-MOSFET and at 300K, 400K, 500K, and 600K. The simulation results obtained from Silvaco TCAD ATLAS show that the performance of the GaN- BTG-MOSFET does not shift much with the adjustment in temperature 300K to 600K and it tends to be utilized in high-temperature gadgets.

CHAPTER 2

LITERATURE REVIEW

This chapter includes the Research papers and books that are referred to complete the study and DESIGN OF NANOSCALE TRENCHED GATE MOSFET. The topics enrolled in selecting research papers are MOSFET, Trenched Gate MOSFET, Silvaco TCAD Atlas Simulations. The review work is done for the areas mentioned below-

- Trenched Gate MOSFET
- Physics of materials
- Temperature analysis

While working on MOSFET and its nano-scaled structure on Silvaco TCAD ATLAS, the following literature are referred:

[1] [1] B. Razavi, *Design of analog CMOS integrated circuits*. Tata McGraw-Hill Education, 2002.

[2] A. S. Sedra and K. C. Smith, *Microelectronic circuits: theory and applications*. Oxford University Press, 2013.

[3] J. Appenzeller *et al.*, "Sub-40 nm SOI V-groove n-MOSFETs," vol. 23, no. 2, pp. 100-102, 2002.

[4] B.-Y. Tsui, C.-F. Huang, and C.-H. J. J. o. t. E. S. Lu, "Investigation of molybdenum nitride gate on SiO2 and HfO2 for MOSFET application," vol. 153, no. 3, p. G197, 2006.

[5] K.-S. Im *et al.*, "Normally off GaN MOSFET based on AlGaN/GaN heterostructure with extremely high 2DEG density grown on silicon substrate," vol. 31, no. 3, pp. 192-194, 2010.

[6] J. Leitner, A. Strejc, D. Sedmidubský, and K. J. T. a. Růžička, "High temperature enthalpy and heat capacity of GaN," vol. 401, no. 2, pp. 169-173, 2003.

[7] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, W. L. J. I. T. o. M. T. Pribble, and Techniques, "A review of GaN on SiC high electron-mobility power transistors and MMICs," vol. 60, no. 6, pp. 1764-1783, 2012.

[8] T. Cheung, M. J. Butson, K. J. P. i. M. Peter, and Biology, "Effects of temperature variation on MOSFET dosimetry," vol. 49, no. 13, p. N191, 2004.

[9] A. Kumar, M. Tripathi, and R. J. I. T. o. E. D. Chaujar, "Reliability issues of In 2 O 5 Sn gate electrode recessed channel MOSFET: Impact of interface trap charges and temperature," vol. 65, no. 3, pp. 860-866, 2018.

[10] A. Kumar, N. Gupta, and R. J. M. J. Chaujar, "TCAD RF performance investigation of transparent gate recessed channel MOSFET," vol. 49, pp. 36-42, 2016.

[11] C.-W. Lee *et al.*, "High-temperature performance of silicon junctionless MOSFETs," vol. 57, no. 3, pp. 620-625, 2010.

[12] A. Asenov, S. Kaya, and J. H. J. I. T. o. e. d. Davies, "Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations," vol. 49, no. 1, pp. 112-119, 2002.

[13] I. J. S. C. Silvaco, CA, Ver, "ATLAS user’s manual," vol. 5, 2011.

[14] B. J. Baliga, "Trench gate lateral MOSFET," ed: Google Patents, 1995.

[15] C.-Y. Tsai, T. Wu, and A. J. I. e. d. l. Chin, "High-Performance GaN MOSFET With High-$\kappa $$\hbox {LaAlO} _ {3}/\hbox {SiO} _ {2} $ Gate Dielectric," vol. 33, no. 1, pp. 35-37, 2011.

[16] S. Veeraraghavan and J. G. J. I. T. o. E. D. Fossum, "Short-channel effects in SOI MOSFETs," vol. 36, no. 3, pp. 522-528, 1989.

[17] N. D. Arora, *MOSFET models for VLSI circuit simulation: theory and practice*. Springer Science & Business Media, 2012.

[18] B. Doris *et al.*, "Extreme scaling with ultra-thin Si channel MOSFETs," in *Digest. International Electron Devices Meeting*, 2002, pp. 267-270: IEEE.

[19] A. Kumar, P. M. Tripathi, H. Soni, R. J. I. C. Chaujar, Devices, and Systems, "Numerical Simulation and Parametric Assessment of GaN Buffered Trench Gate MOSFET for Low Power Applications," 2020.

[20] L. Li *et al.*, "Wafer-scale fabrication of recessed-channel PtSe 2 MOSFETs with low contact resistance and improved gate control," vol. 65, no. 10, pp. 4102-4108, 2018.

[21] H. Soni, P. M. Tripathi, M. Tripathi, A. Kumar, and R. Chaujar, "Thermal Reliability of GaN-BTG-MOSFET for High-Performance Applications in Integrated Circuits," in *2020 IEEE 40th International Conference on Electronics and Nanotechnology (ELNANO)*, 2020, pp. 220-223: IEEE.

CHAPTER 3

TRENCHED GATE MOSFET

3.1 DEVICE DESIGN, MODELS, AND CALIBRATIONS:

The proposed GaN-BTG-MOSFET is depicted in Fig- 3. Gate length (L_g) of the MOS is 20 nm, negative junction depth is 10 nm, and oxide thickness (t_{ox}) is 2 nm. A GaN substrate is taken instead of silicon and source and drain region are intensely doped (1×10^{19} cm-3). For the performance analysis of the GaN-BTG device, the ATLAS simulator[13] has been utilized. In this simulation mobility and recombination, models have been utilized with a gate voltage of 2.0V and a steady drain voltage of 0.2V.

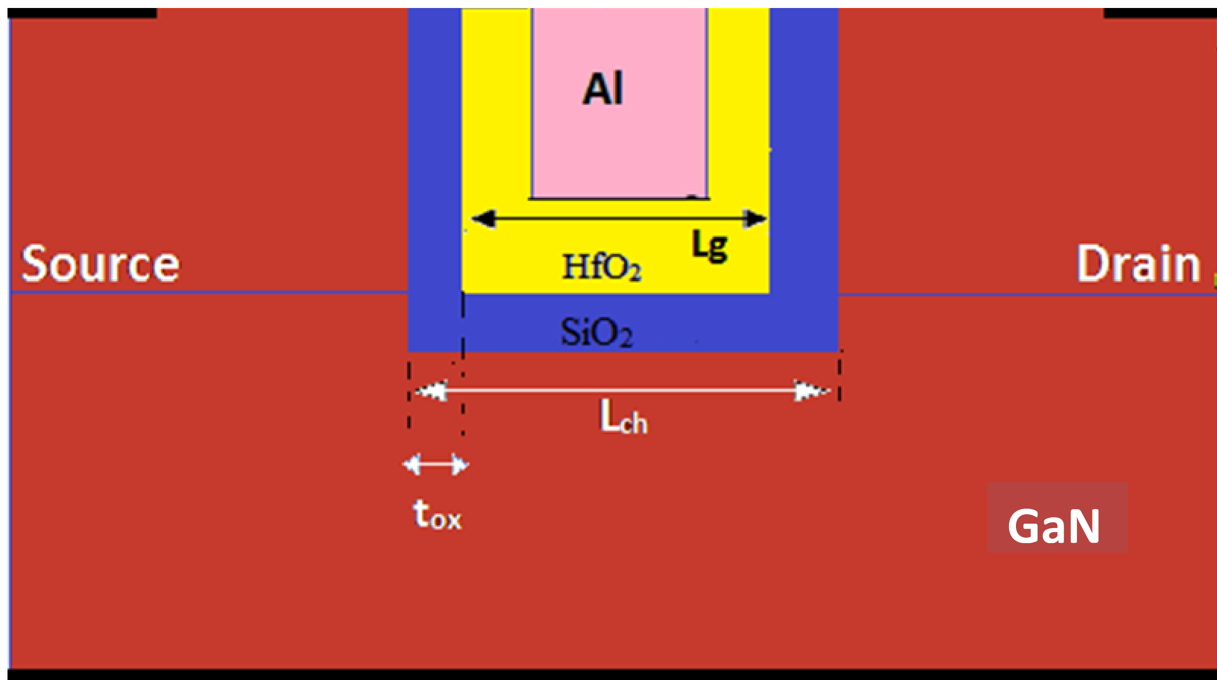


Fig 3: Structure of GaN BTG MOSFET

The simulation models utilized can be expressed by following equations -

1. POISSON'S EQUATION:

$$div(\varepsilon \nabla \varphi) = -\rho \quad \text{(1)}$$

Where ε is permittivity, ρ is space charge density, and φ is potential difference.

2. CURRENT CONTINUITY EQUATION:

For Holes and electrons-

$$\frac{\partial p}{\partial t} = \frac{1}{q} div \vec{J}_p + G_p - R_p \quad \text{(2)}$$

$$\frac{\partial n}{\partial t} = \frac{1}{q} div \vec{J}_n + G_n - R_n \quad \text{(3)}$$

Here, holes and electrons current densities are represented by j_p and j_n

G_p and G_n indicate generation rate for holes and electrons;

recombination rate for holes and electrons are R_p and R_n.

3. RECOMBINATION:

3.1 SRH (Shockley Read Hall)

$$R_{SRH} = \frac{pn - n_{ie}^2}{\tau_p[n + n_{ie}e^{(-(E_{TRAP}/kT_L))}] + \tau_n[p + n_{ie}e^{(-(E_{TRAP}/kT_L))}]}$$

__________(4)

Here, change in the intrinsic Fermi level and the trap energy level is represented by ETRAP; τ_n and τ_p, are the electron and hole lifetime.

Phonon transitions happen in the presence of a trap (or imperfection) within the forbidden gap of the semiconductor. This is a two-step process, the hypothesis of which was first derived by Shockley and Read and afterward by Hall.

$$R_{SRH} = \frac{pn - nie2}{TAUP0\left[n + nie\,exp\left(\frac{ETRAP}{kTl}\right)\right] + TAUN0[p + nie\,exp(-ETRAP/kTl)]}$$

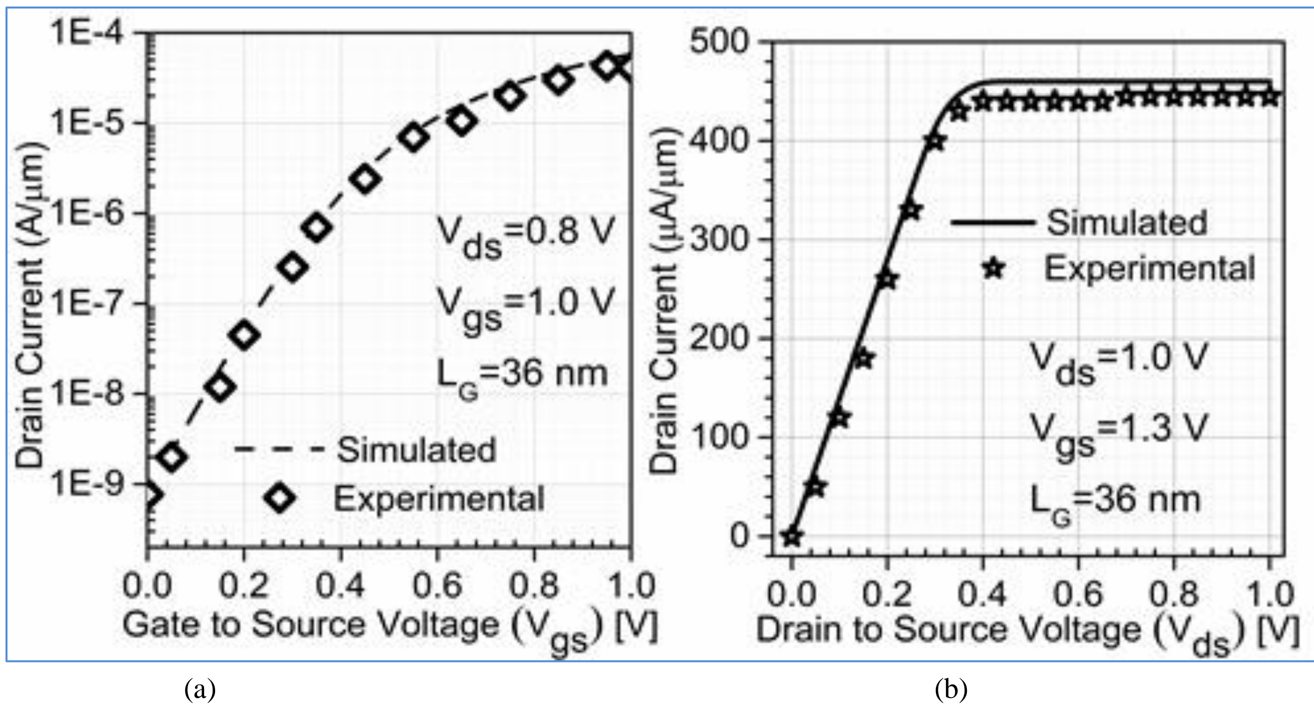
Here ETRAP is the difference between the trap energy level and the intrinsic Fermi level, Tł is the lattice temperature in degrees Kelvin and TAUN0 and TAUP0 are the electron and hole lifetimes. This model is initiated by using the SRH boundary of the MODELS statement. The electron and hole lifetime parameters, TAUN0 and TAUP0, are user-definable in the MATERIAL statement.

3.2 Auger recombination

$$R_{Auger} = AUGN\left(pn^2 - nn_{ie}^2\right) + AUGP\left(np^2 - pn_{ie}^2\right)$$ ____________(5)

AUGN and AUGP are user-defined where AUGN=8.3×10-32 cm^6/sec and AUGP=1.8×10-31 cm^6 /sec. Parallel electric-field-dependent mobility.

$$\mu(E) = \mu_0 \left[\frac{1}{1 + (\mu_0 E / \upsilon_{sat})^{\beta}} \right]^{1/\beta}$$ ____________(6)



(a) (b)

Fig.4. (a) Transfer and (b) Output characteristics calibration of simulated and experimental data for 36 nm recessed channel MOSFET.

For the approval of simulation models, the trial information of a fabricated trenched gate MOSFET (36 nm gate length) was taken and plotted for the correlation with simulation data in terms of transfer characteristics and output characteristics as shown in Fig. 4 (a) and (b) respectively. Fig. 4 shows that the experimental results and simulated results are well-calibrated, thus showing the legitimacy of simulation models.

Table 1: MATHEMATICAL MODELS ENROLLED in Simulations

S. No.	Physical Models	Description
1	**Mobility Models**	Lombardi CVT and Constant Low Field Mobility Model.
2	**Recombination Model**	Shockley Read Hall (SRH) Recombination is included to incorporate minority recombination effects with carrier lifetime=1×10^{7}s.
3	**Statistics**	Boltzmann Transport model, The use of Boltzmann statistics is normally justified in semiconductor device theory, but Fermi-Dirac statistics are necessary to account for certain properties of very highly doped (degenerate) materials.
4.	**Impact Ionization and Tunneling Model**	Such a model is used for evaluating hot-carrier performance.
5.	**Energy Transport Model**	Hydrodynamic Model is used as it includes all nonlocal effects and is more accurate than the drift-diffusion method. Drift diffusion Model show shortcomings as channel length scale down to 50nm.

3.2 CONVENTIONAL TRENCHED GATE (CTG) MOSFET

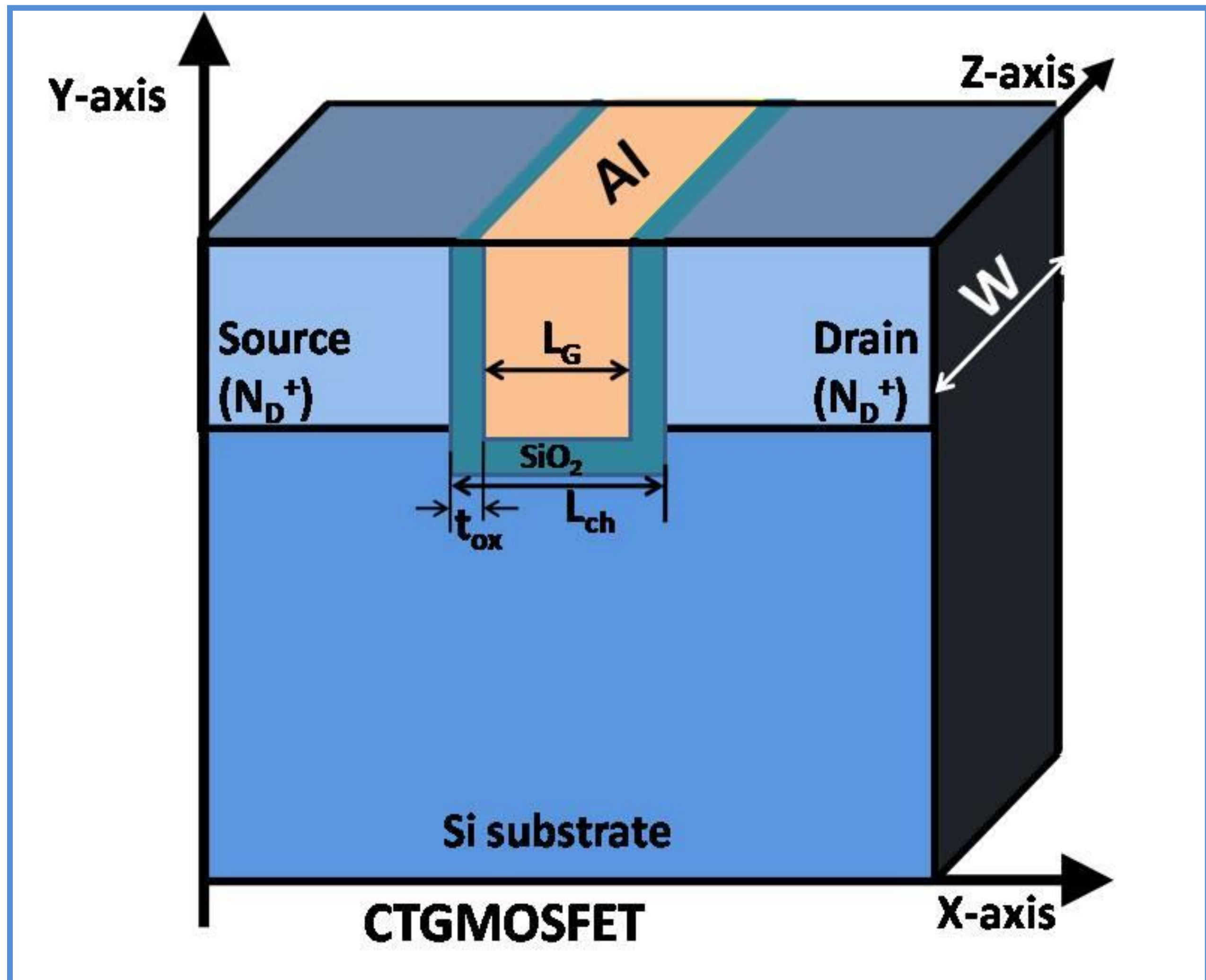


Fig 5: CTG MOSFET

Scaling of Conventional MOSFETs at the nanoscale are not possible because of Short channel effects and Hot carrier effects, Trenched Gate MOSFET[14] is a promising candidate for suppressing the various SCEs and HCEs. Fig 5 represents Conventional Trenched Gate (CTG) MOSFET designed in Silvaco TCAD ATLAS. Two potential barriers are formed at the two corners due to the high density of electric field lines. Carriers in the channel now require more energy to surmount these barriers, which limits its carrier transport efficiency and hence, lowering the current driving. In conventional MOSFET a trench is introduced in the electronic channel of the MOSFET, this trench is responsible for MOSFET's operation at nanoscale.

3.3 BUFFER TRENCHED GATE (BTG) MOSFET

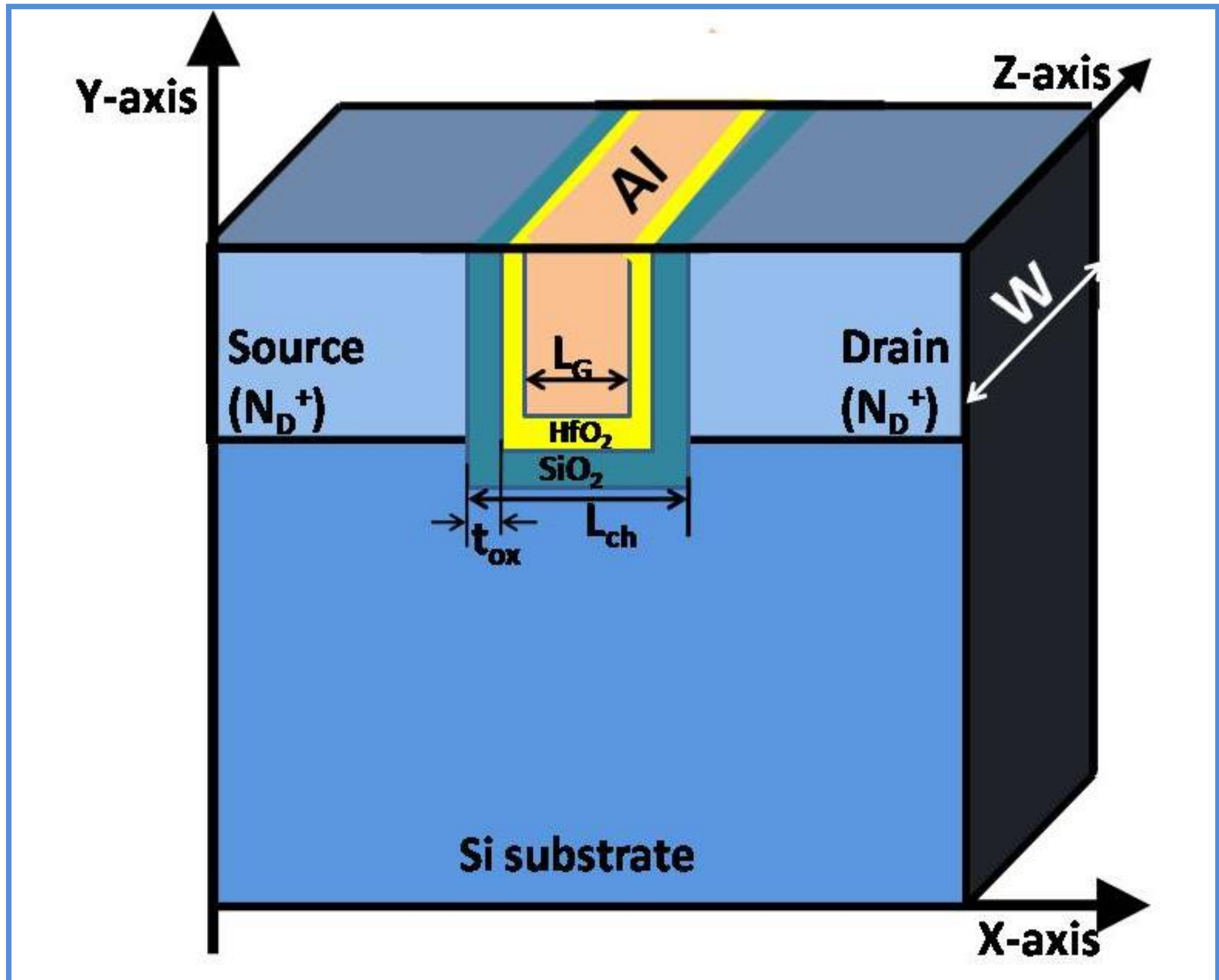


Fig 6: BTG MOSFET

With the stacking of Hafnium Oxide (HfO_2) with Silicon dioxide (SiO_2) at gate terminal in conventional trenched gate structure, as spoken to in Fig 6. To use the benefits of the structure and furthermore up-scaling its performance by improving the saturation current and threshold voltage simultaneously. Hafnium Oxide is an insulator and acts as a buffer layer in between SiO_2 and electrode. Its high dielectric constant[4] helps in accomplishing higher oxide capacitance, which brings about a further gain in the saturation current of MOSFET and furthermore diminishes the formation of hot electrons. Going above and beyond, we have presented GaN instead of Silicon wafer, in the same trenched gate structure.

3.4 GAN BUFFER TRENCHED GATE (GAN-BTG) MOSFET

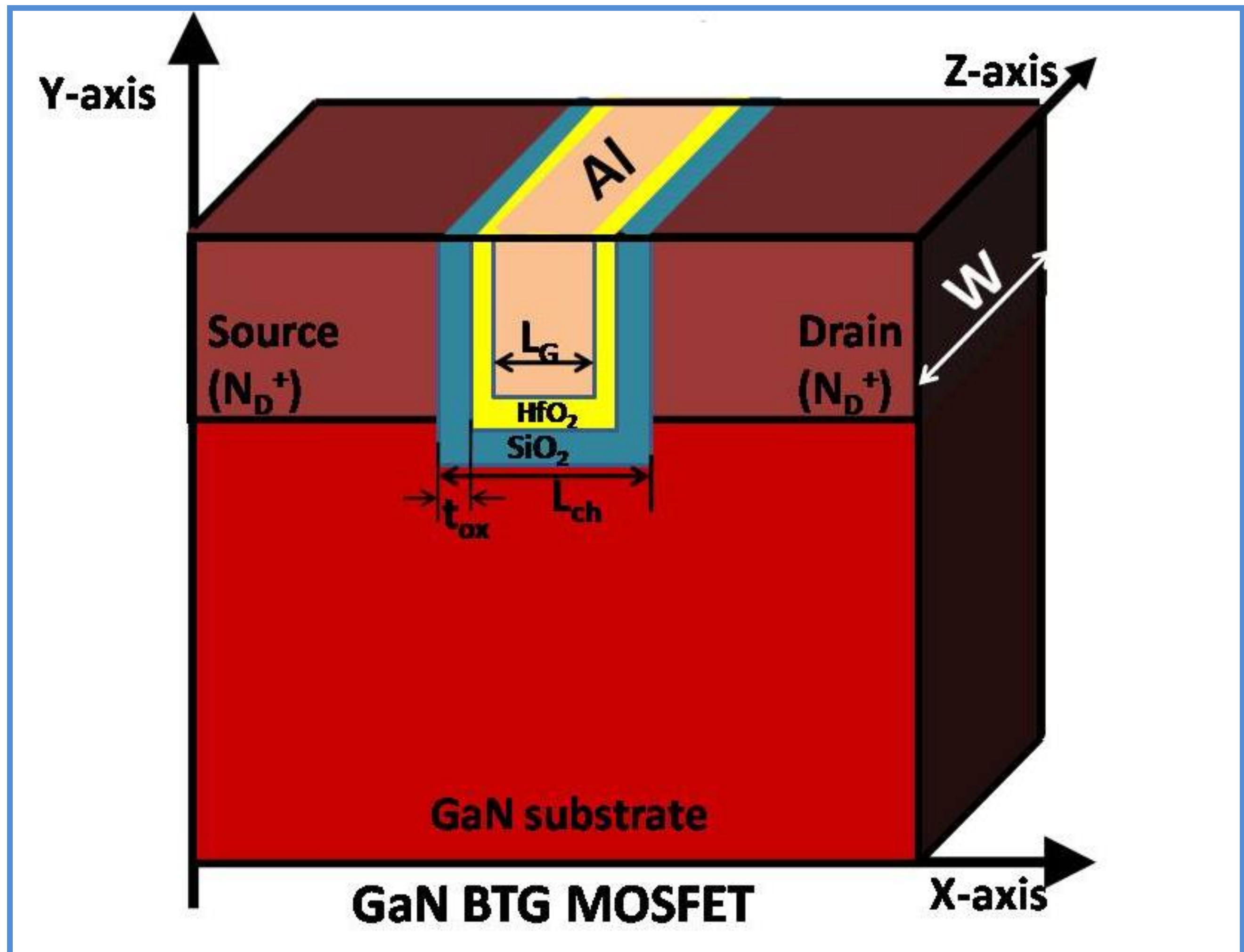


Fig 7: GaN-BTG MOSFET

One of the significant advantages of GaN is that it is possible to additionally downsize the size of the device with little on-resistance and higher breakdown voltage than is conceivable with Silicon[15]. GaN has high electron mobility which reasons with an improved drain to source current. Fig 7 speaks to GaN-BTG-MOSFET, GaN displays a wide bandgap of 3.4 eV and has high warmth limit, which makes it helpful for high-temperature activity (400°C) applications and can be operated productively at high voltages. It has high electron mobility (1500 cm^2/volt-sec) than silicon, which implies it shows higher critical electric field strength than silicon. High mobility also accounts for quicker switching speeds respecting less switching losses.

CHAPTER 4

SIMULATION RESULTS

The content and results of the following Research papers have been reported in this chapter:

- **H. Soni**, P. M. Tripathi, M. Tripathi, A. Kumar, and R. Chaujar, "Thermal Reliability of GaN-BTG-MOSFET for High-Performance Applications in Integrated Circuits," in *2020 IEEE 40th International Conference on Electronics and Nanotechnology (ELNANO)*, 2020, pp. 220-223: IEEE

- Kumar A, Tripathi PM, **Soni H**, Chaujar R. Numerical Simulation and Parametric Assessment of GaN Buffered Trench Gate MOSFET for Low Power Applications. IET Circuits, Devices & Systems. 2020 Apr 20.

- **H. Soni**, P.M. Tripathi, A. Kumar, and R. Chaujar "Novel GaN Buffered Trench Gate (GaN-BTG) MOSFET: A TCAD Numerical Study" in 8th International Conference on Computing, Communication and Sensor Networks, 2019.

4.1 PARAMETER ANALYSIS :

It is desired to have a high drain current at low gate voltages for a MOSFET[1, 16]. From Fig. 8, a derivation can be drawn that high drain current is accomplished for GaN-BTG-MOSFET at low voltages when contrasted to a conventional device.

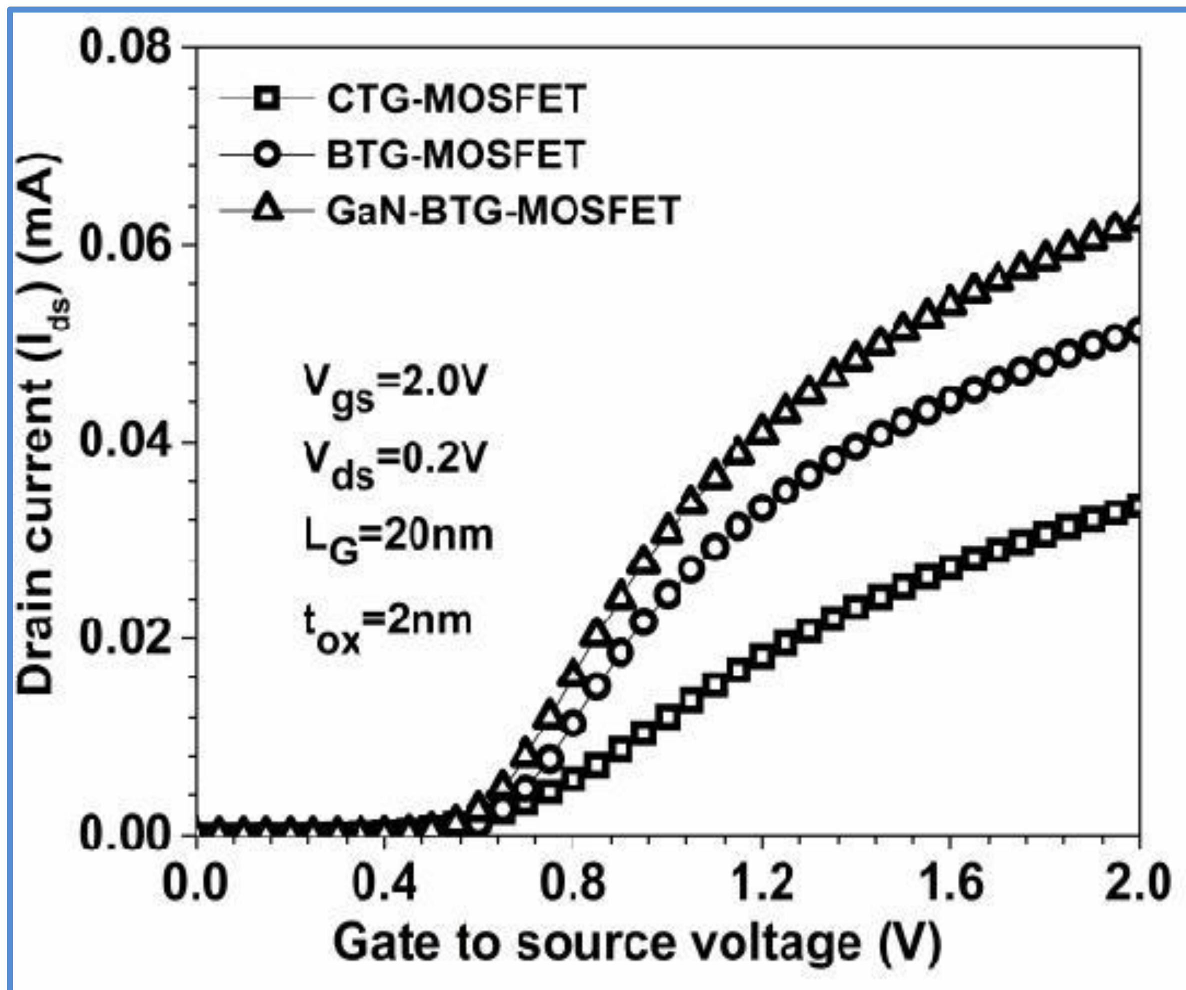


Fig. 8 Transfer characteristics of CTG, BTG, and GaN-BTG- MOSFET

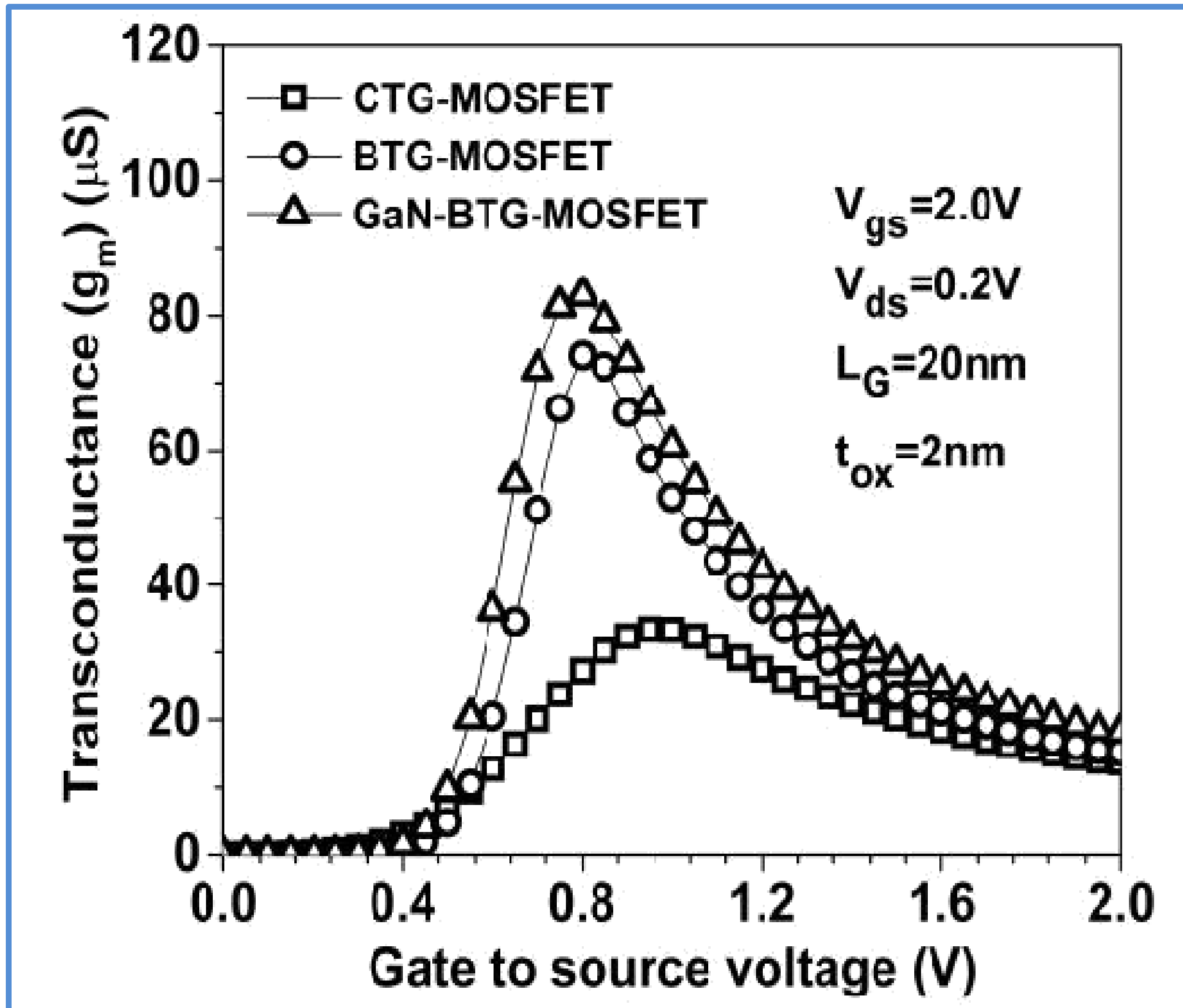


Fig. 9 Transconductance versus Gate voltage of CTG, BTG, and GaN-BTG-MOSFETs

Utilization of high-k HfO_2 in BTG-MOSFET builds the oxide capacitance, which improves the channel current. Further presentation of GaN instead of silicon, extra improvement is observed in the MOS, which is ascribed to high basic electron mobility of GaN. Transconductance (g_m)(shown in Fig. 9) shows quite a significant improvement on account of BTG-MOSFET which is ascribed to the high-k of the buffer as it results in higher gate oxide capacitance (C_{ox}) and thus increments in the gain of the device to the gate voltage V_g. Further spike is observed in GaN-BTG-MOSFET, which is because of higher elemental electron mobility of GaN. The transfer characteristics depict that for a similar gate voltage (V_g) higher channel current (I_d) is observed in the case of BTG-MOSFET as compared to that of CTG-MOSFET.

It is a direct result of high-k of a buffer that Cox is increasing and thus gain (g_m) is increasing consequently, increasing I_d[12], while GaN-BTG-MOSFET far better channel current curve due to its higher elemental electron mobility than that of Silicon.

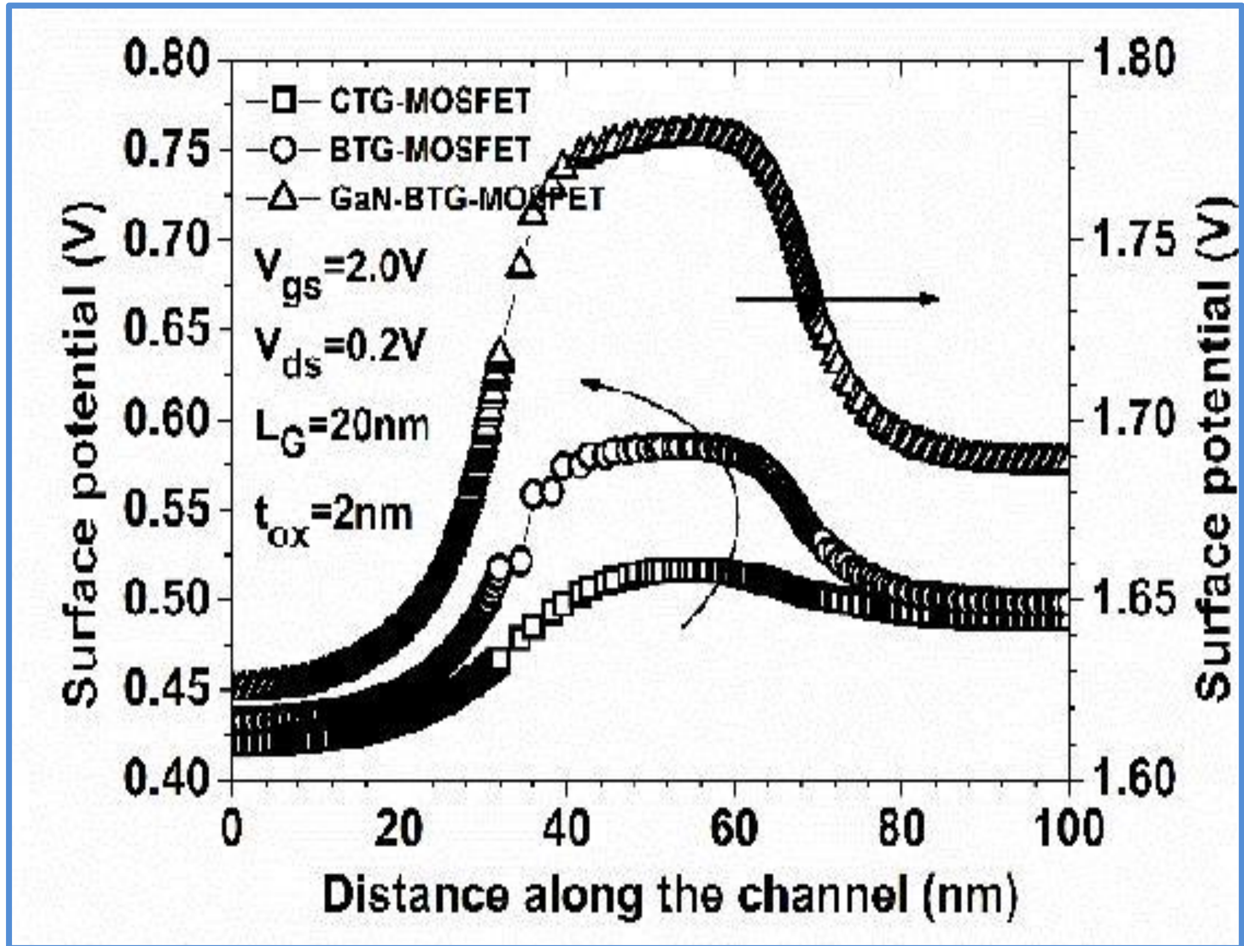


Fig. 10 Surface potential along the channel for CTG, BTG, and GaN-BTG-MOSFET.

Further, an enhancement in the potential boundary builds the surface potential of the GaN-BTG MOSFET, which can be observed seen the surface potential plot shown in Fig. 10. This enhancement is because of an increase in level band voltage of GaN (3.4eV) concerning silicon (1.1eV) which results in better gate control over the channel and consequently a higher surface potential[9] is observed.

Fig. 11 gives the record of the V_{th} and Sub-threshold slope (SS) of the devices. The threshold voltage curve reveals that V_{th} of BTG-MOSFET observed a decrement of 1.8% and that of GaN-BTG-MOSFET diminished by 9.83% when contrasted to that of a conventional MOSFET. The sub-threshold slope curve demonstrated an improvement of 40.33% in BTG-MOSFET and an overall improvement of 43.85% in SS of GaN-BTG-MOSFET.

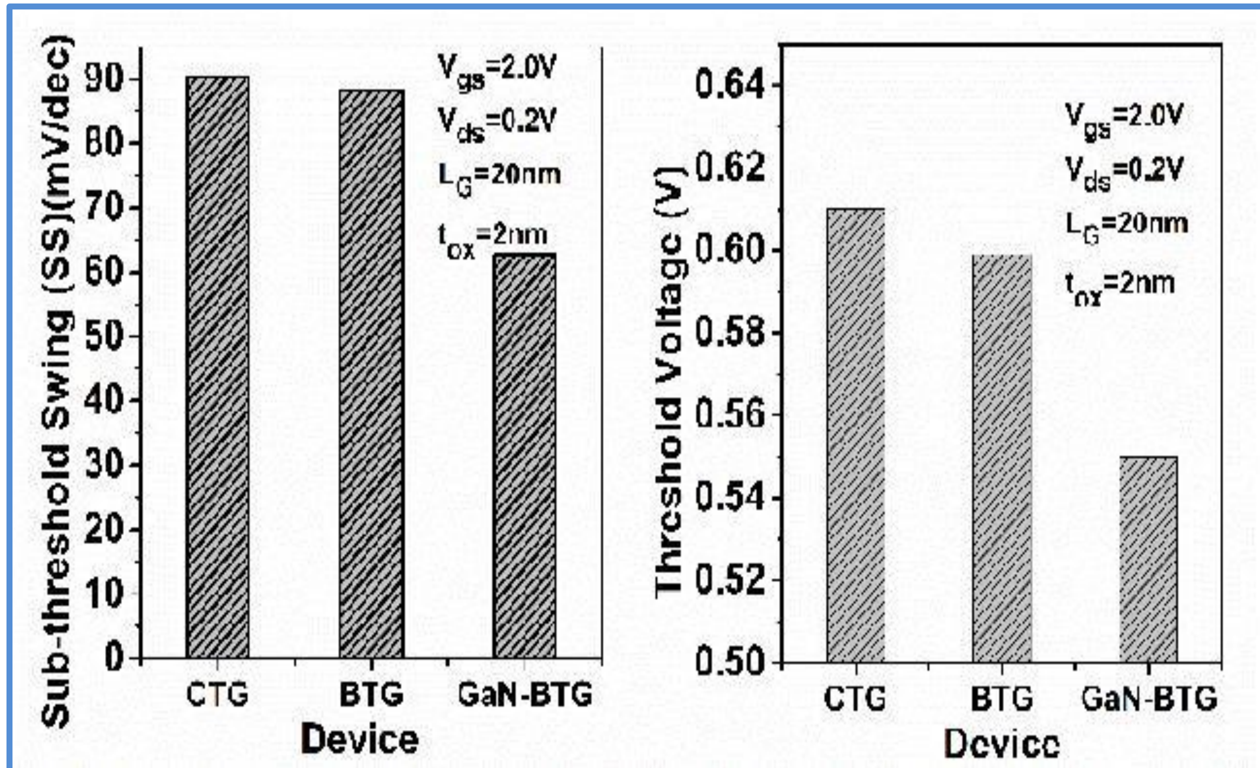


Fig. 11: (a) Sub-threshold Swing, and (b) Threshold Voltage of the CTG-MOSFET, BTG-MOSFET, and GaN-BTG-MOSFET.

This improvement in SS is because of 1.8% and 9.83% lower V_{th} of BTG-MOSFET and GaN-BTG-MOSFET respectively and improved turn-on characteristics because of which BTG-MOSFET and GaN-BTG-MOSFET cross the sub-threshold region quicker than the conventional MOSFET and henceforth improving the switching characteristics of the device.

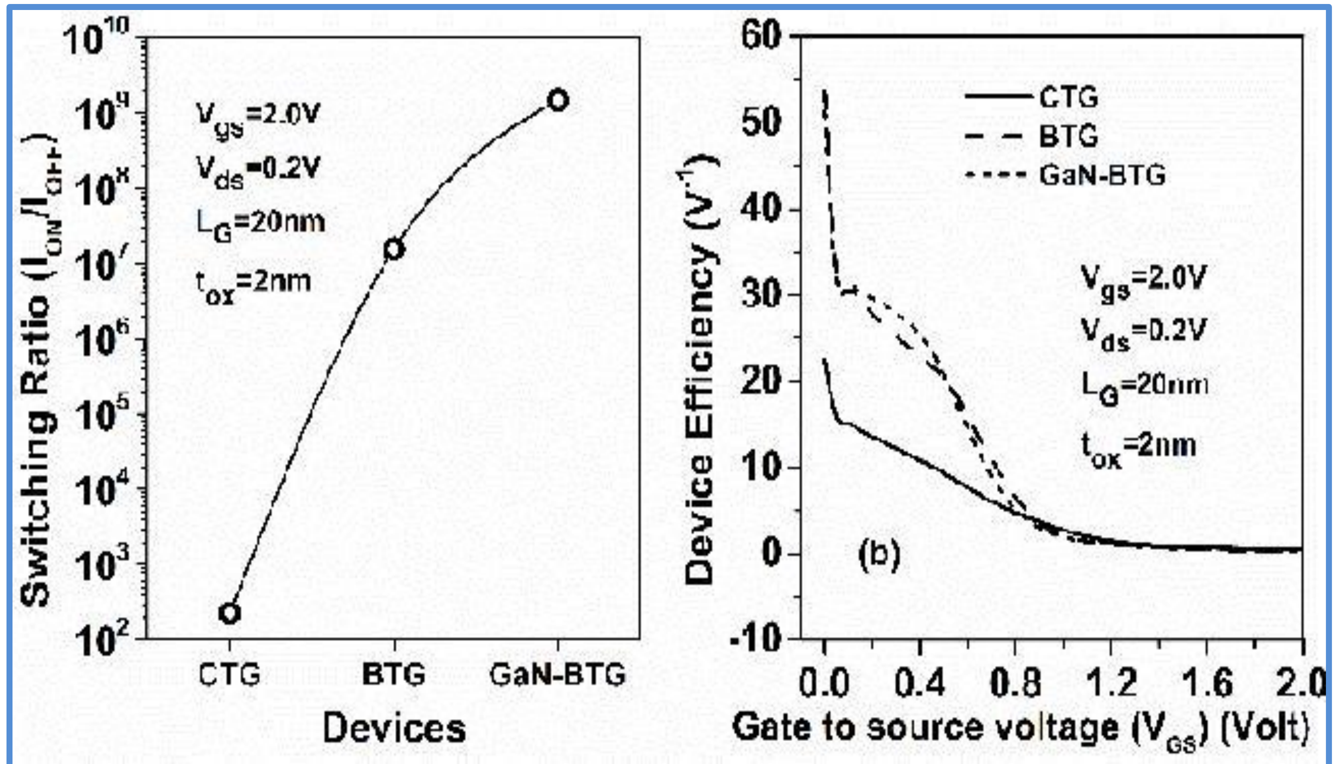


Fig. 12: (a) Switching ratio (I_{ON}/I_{OFF}) (b) Device efficiency of the CTG, BTG, and GaN-BTG MOSFETs.

From Fig 12(a), an improvement in switching ratio (I_{on}/I_{off}) can be observed. GaN-BTG-MOSFET shows a quicker-switching rate concerning CTG MOSFET and results in a lower leakage current which lessens power dissipation and results in a power-efficient device. Device efficiency (Fig 12 b) is the measure of the effectiveness to convert power into speed[1]. The Device Efficiency Curve shows that GaN-BTG-MOSFET performs adequately at low gate voltages and decreases power dissipation and results in a power-efficient MOS.

From on current (I_{on}) and off current (I_{off}) information of the devices, certain positive improvements can be deciphered. I_{on} of BTG-MOSFET is 6.23×10^{-5} A, and that of GaN-BTG-MOSFET is 7.54×10^{-5}A which is a serious improvement from 1.1×10^{-5} A of that of CTG-MOSFET. Leakage current I_{off} is observed to be decreased from 4.9×10^{-8} A to 3.99×10^{-12} A for BTG-MOSFET and 4.9×10^{-12} A to 5.02×10^{-12} A in GaN-BTG-MOSFET.

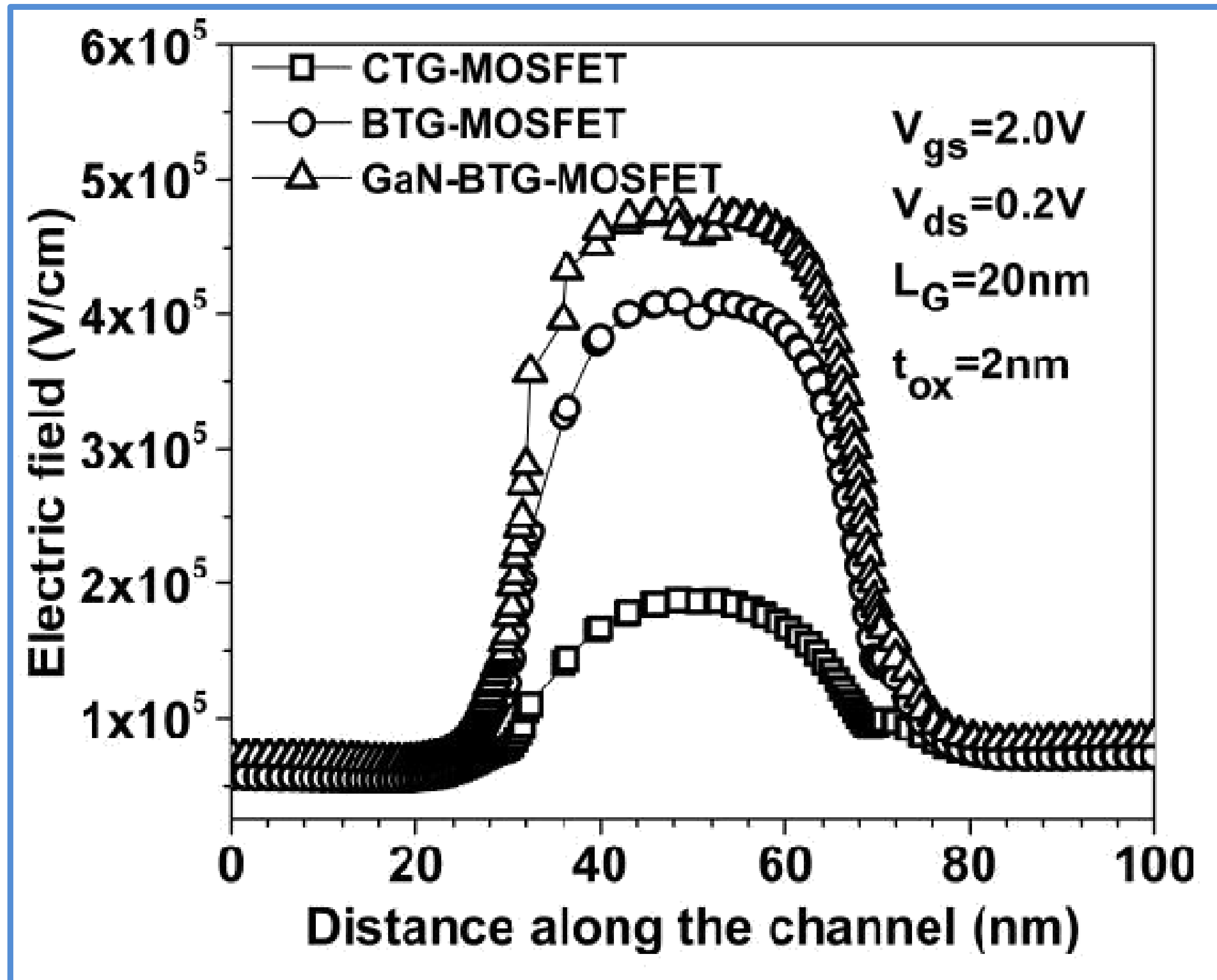
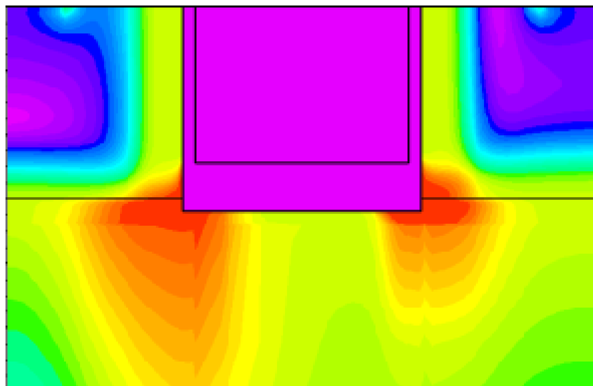


Fig 13 Electric field distribution along the channel for CTG, BTG, and GaN-BTG-MOSFET.

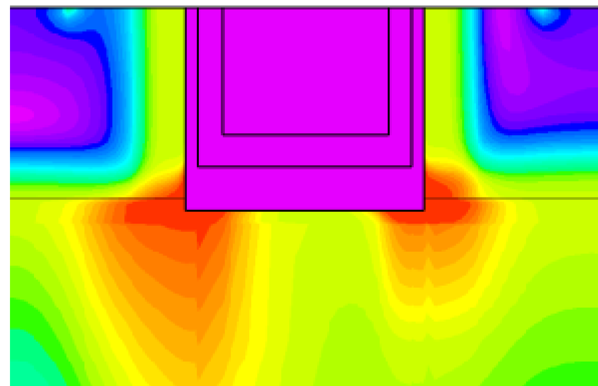
Fig. 13 shows the variation of the electric field in X- heading, and from the given graph, it can be derived that the electric field curve obtained in CTG-MOSFET improves significantly when a buffer is presented between the layers of channel and oxide. It is so because of high-k buffer due to which gate oxide capacitance (Cox) increases, which leads to the gathering of more charges in the channel and result in a higher electric field.

(a)

Fig 14 (a) Electron velocity along the channel for CTG, BTG, and GaN-BTG-MOSFET.



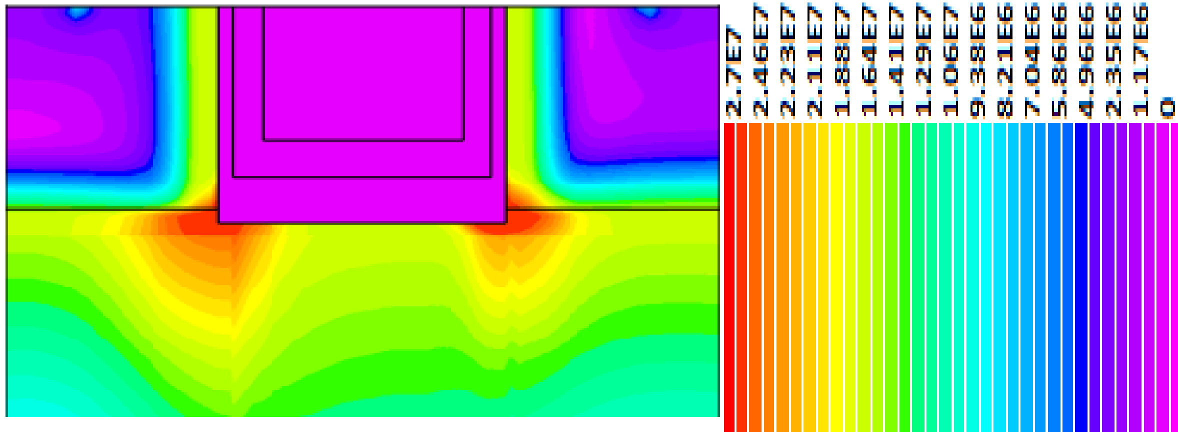
(b)



(c)

Fig. 14 (b): Contour plot of electron velocity for CTG-MOSFET.

Fig. 14 (c): Contour plot of electron velocity for BTG-MOSFET.



(d)

Fig 14 (a) Electron velocity along the channel for CTG, BTG, and GaN-BTG-MOSFET. (b) Contour plot of electron velocity for CTG-MOSFET Contour plot of electron velocity for BTG-MOSFET. (d) Contour plot of electron velocity for GaN-BTG-MOSFET.

Moreover, a further improvement is observed when the Silicon is supplanted by GaN, which is obvious from the curve, because of high natural mobility of the GaN, the electric field gets enhanced in the channel[15].

We additionally record an unexpected plunge in the electric field at X=0.05µm in both BTG-MOSFET and GaN-BTG-MOSFET. As examined over, the high-K buffer is having a significant impact on the electric field however it isn't so compelling in case of electron velocity and the curves of both CTG-MOSFET and BTG-MOSFET nearly concur in the principal half of the curve however some minute improvement is noticed in the subsequent half (as shown in Fig.14).

Notwithstanding, GaN BTG MOSFET shows noteworthy improvement in electron velocity because of which improvement in channel current is noticed. The electron mobility is assessed and contrasted with its counterpart devices as reflected in Fig. 15. The channel region showcases a precarious plunge in electron mobility. BTG-MOSFET and GaN-BTG-MOSFET show even lower electron mobility, which can be accounted for high scattering impacts due to the presence of an enormous number of electrons in the channel[7]. In non-channel regions, GaN-BTG-MOSFET shows better electron mobility when contrasted with BTG-MOSFET, which is credited to greater elemental electron mobility of GaN contrasted with that of Silicon.

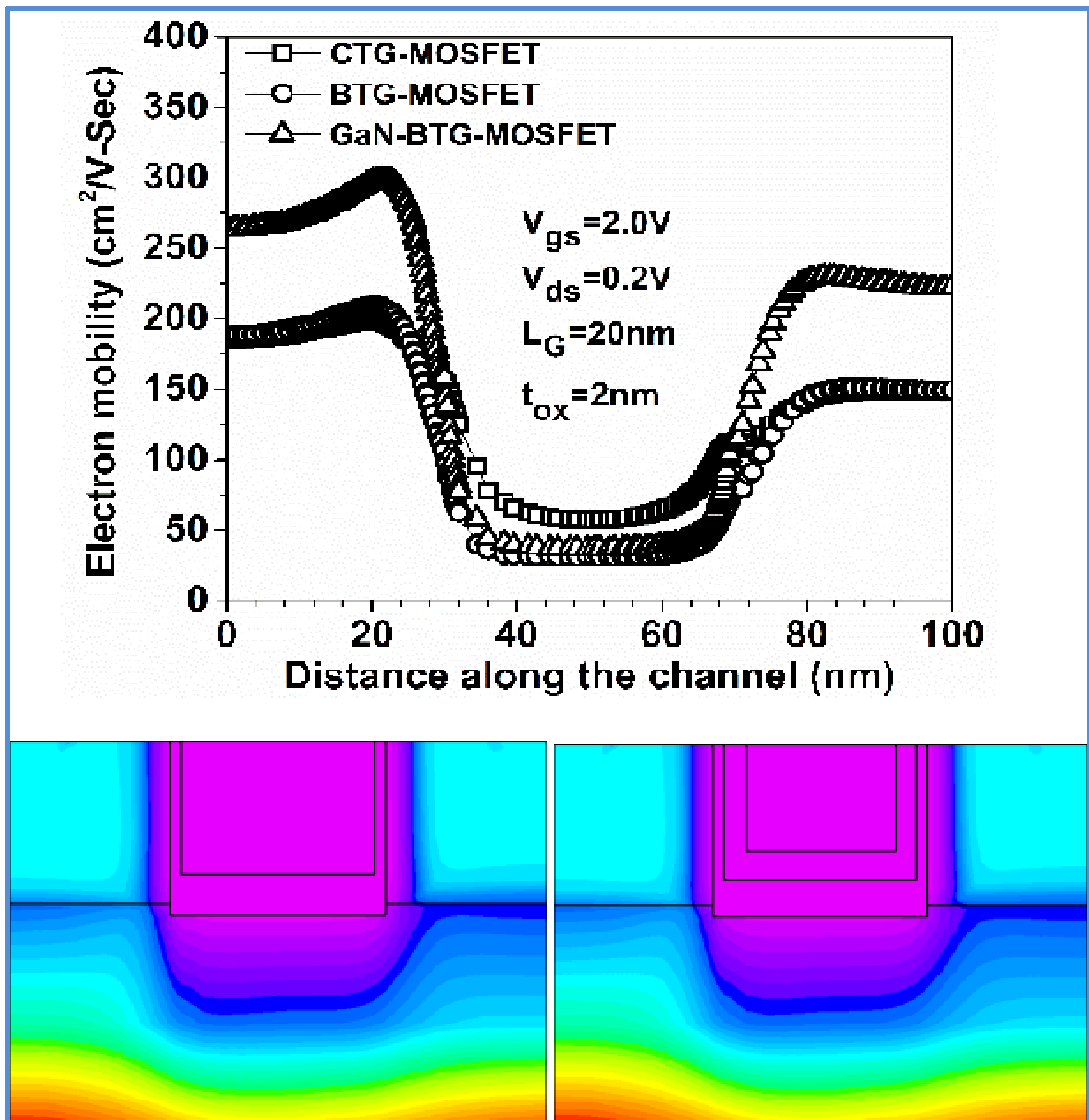


Fig 15 (a) Electron mobility along the channel for CTG, BTG, GaN-BTG-MOSFET. (b) Contour plot of electron mobility for CTG-MOSFET and GaN BTG MOSFET.

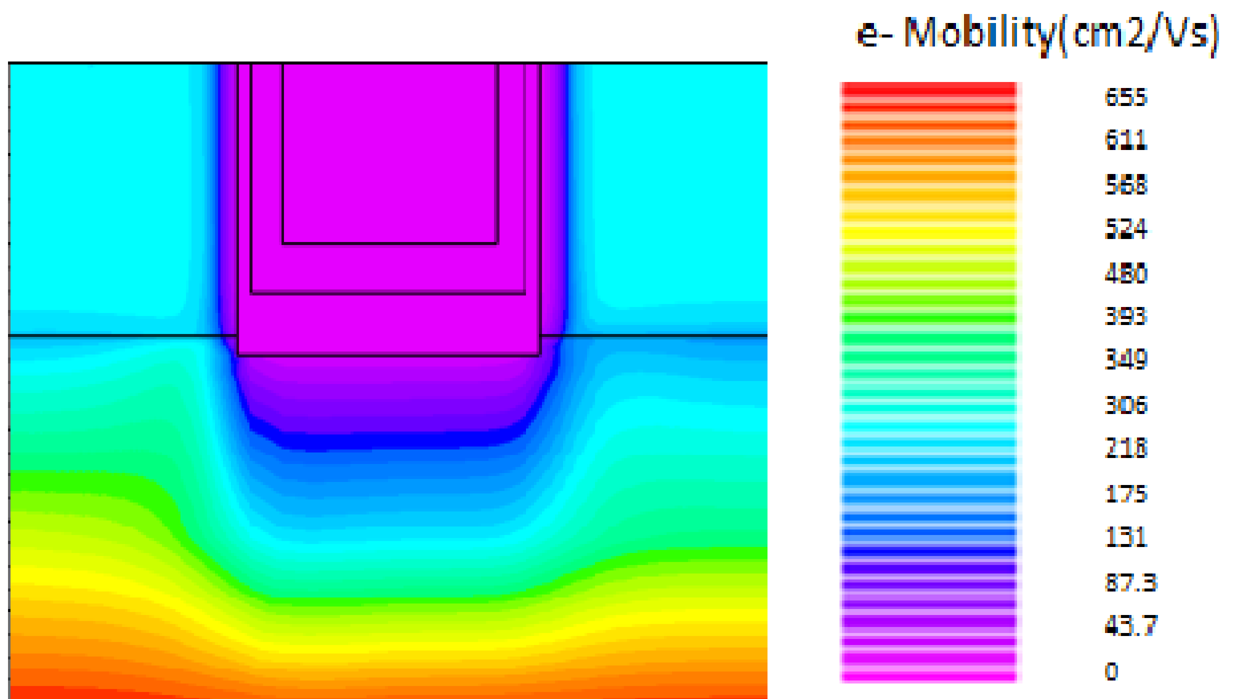


Fig 15 (a) Electron mobility down the channel for CTG, BTG, GaN-BTG-MOSFET. (b) Contour plot of electron mobility in CTG-MOSFET.(c) Contour plot of electron mobility in BTG-MOSFET. (d) Contour plot of electron mobility in GaN-BTG-MOSFET

To change the boundaries of GaN BTG MOSFET, initially, Length of the channel (L_g) fluctuates and different parameters are analyzed and compared for various channel lengths (15nm, 20nm, 30nm, and 40nm). Transconductance is the change in channel current I_d with fluctuating gate voltage V_g at a fixed drain voltage[17].

Fig. 16 compares the transconductance of GaN-BTG MOSFET at different channels. It is realized that with diminishing channel length, short channel effects (SCEs) and hot carrier effects (HCEs) increase in MOS because of which decrease in transconductance is observed for shorter channel lengths[18].

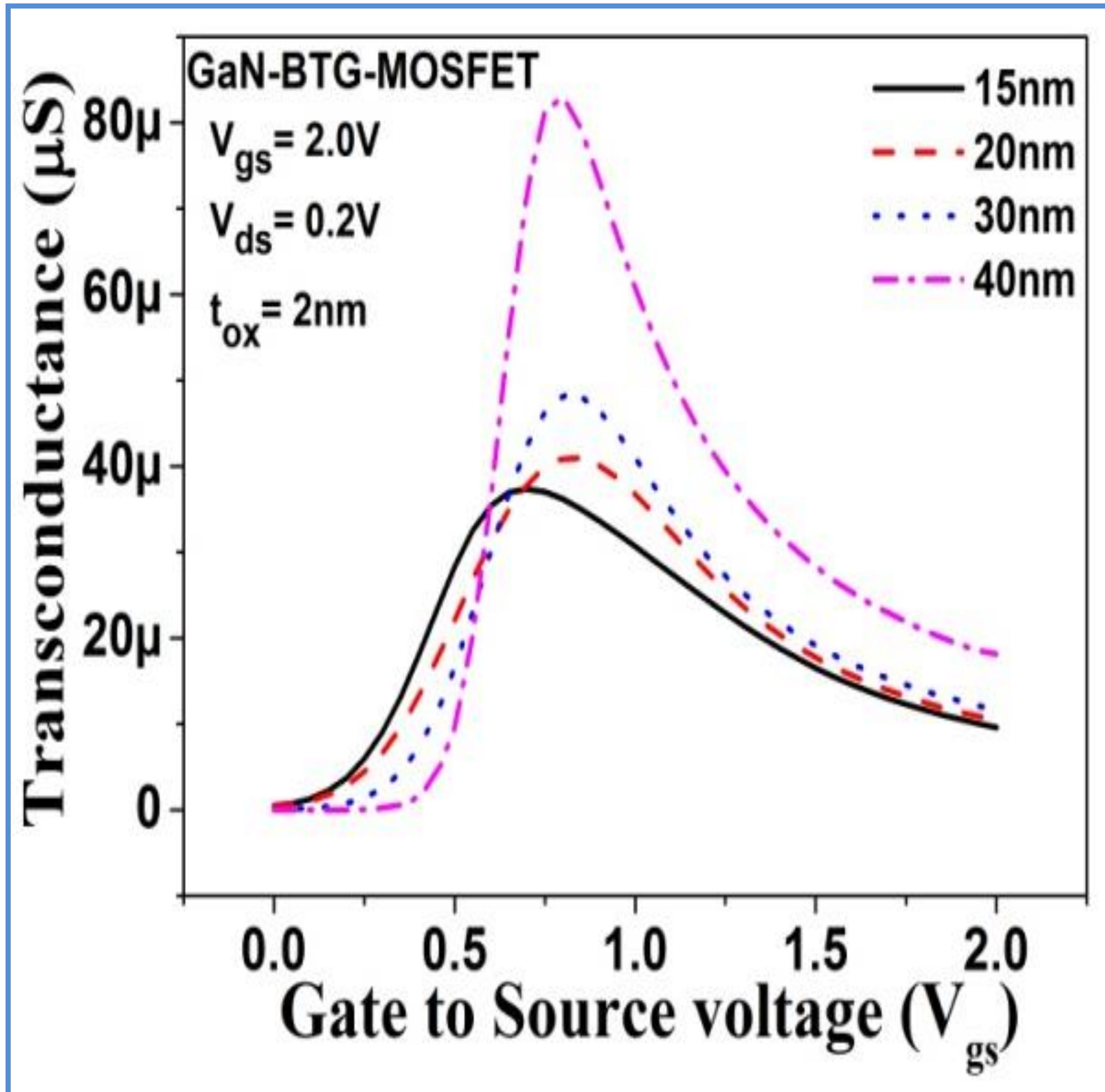


Fig. 16 Transconductance versus Gate voltage of GaN-BTG-MOSFETs with variation in channel lengths.

With reduced transconductance, it can be inferred that for the same MOS device design, On-resistance (R_{on}) of GaN-BTG-MOSFET increases which consequently brings about decreased transfer characteristics as shown in the figure below.

It is desired to have a high channel current at lower gate voltages, which is incidental from the above plot with decreasing channel length, similarly higher channel current is observed which affirms that channel length of GaN-BTG-MOSFET can be downsized.

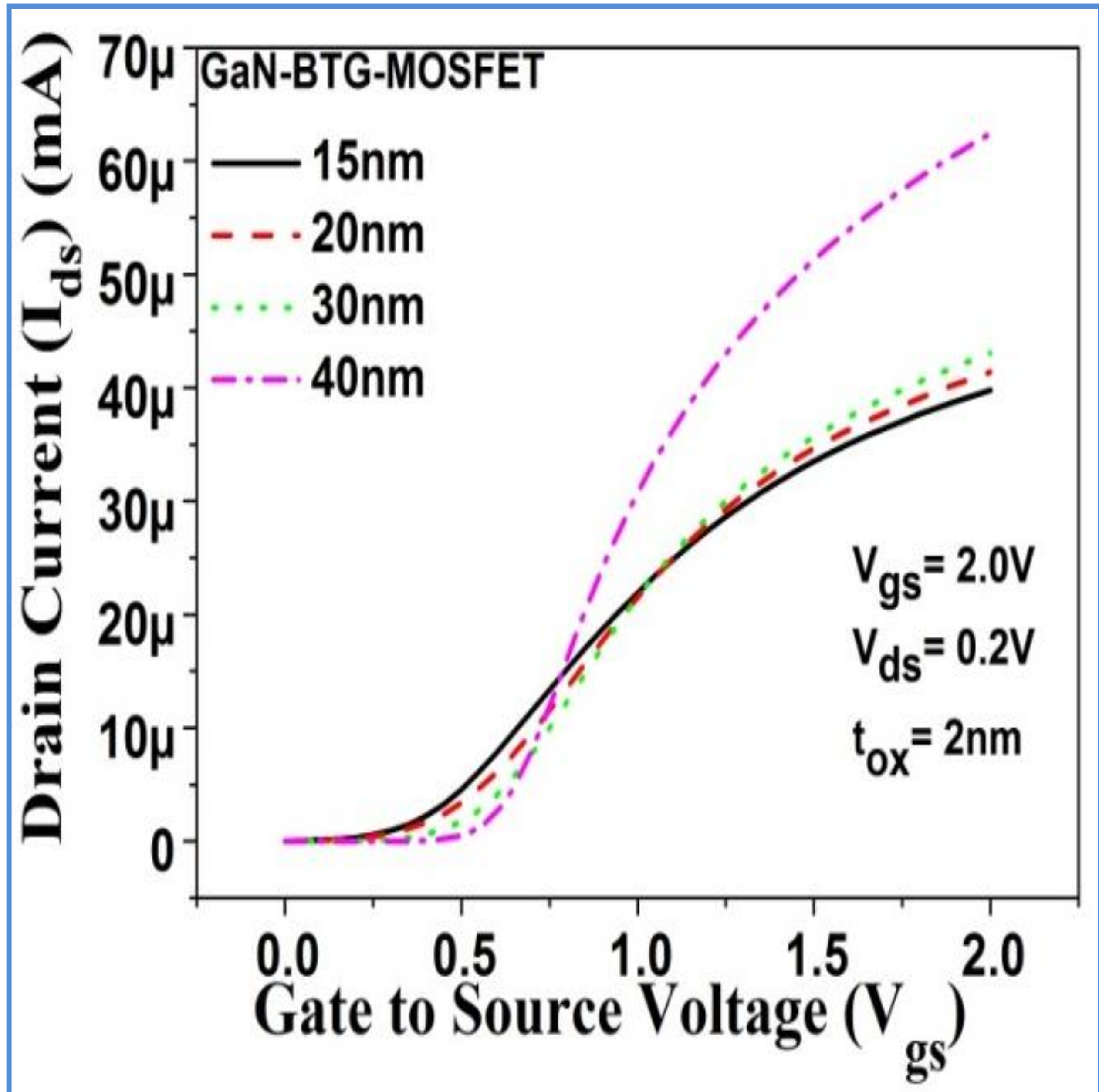


Fig. 17 Transfer characteristics of GaN-BTG- MOSFET with variation in channel length of the device

Transfer characteristics from the given plot (Fig.17) clear that with a decrease in channel length, the maximum drain current of GaN-BTG-MOSFET is diminished by 25% with a 62.5% decrease in channel length. The transfer characteristics depict that in the triode region, the proposed device has higher channel current at diminished channel lengths (15nm, 20nm, and 30 nm appear in the plot).

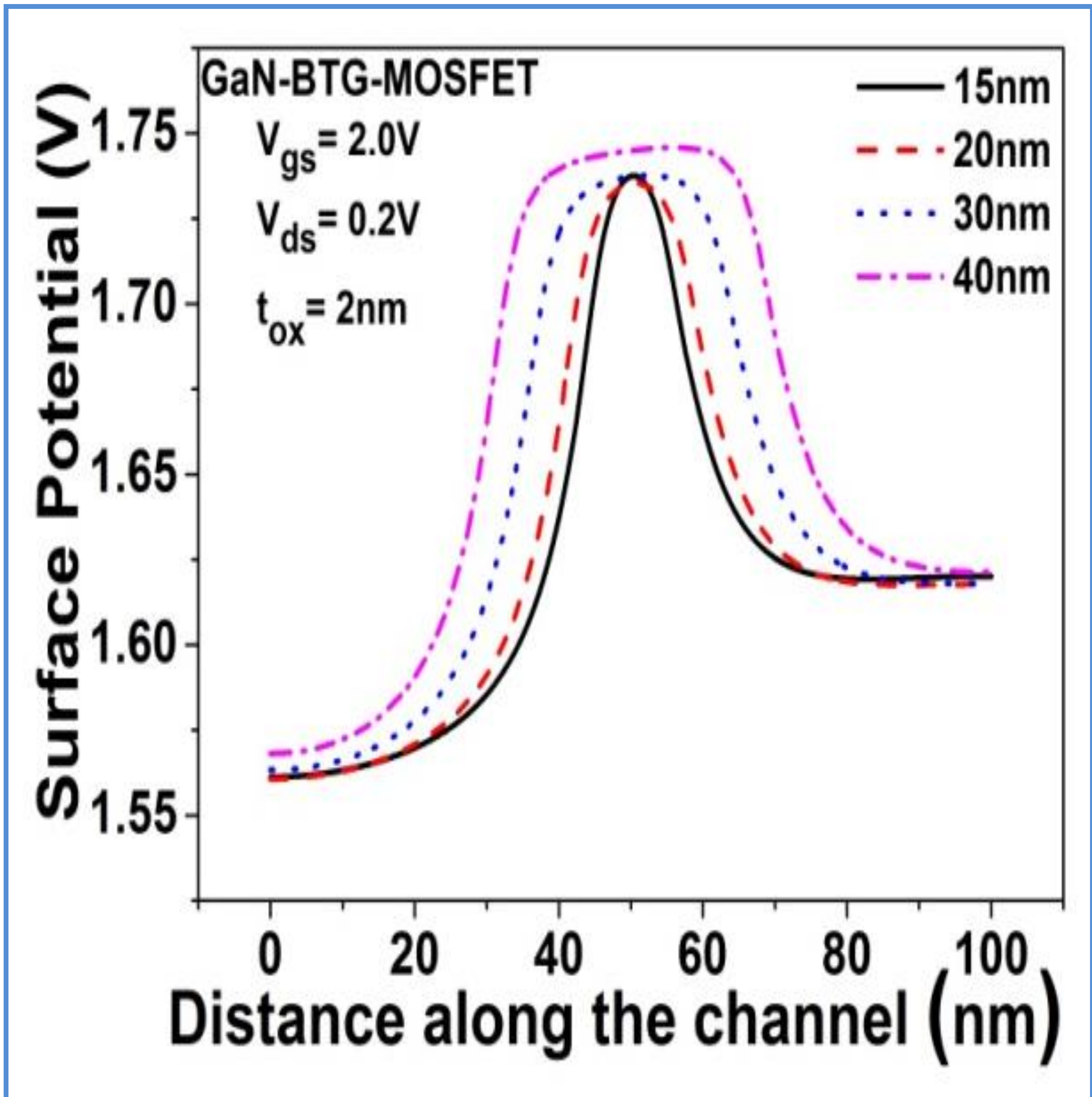


Fig. 18 Surface potential along the channel for GaN-BTG-MOSFET with variation in the channel length

Fig. 18 examines the surface potential at each point on the channel axis and shows that potential barrier with the change in channel length doesn't shift linearly. The potential barrier of the GaN-BTG-MOSFET has a variation of only 1.14% with a normal surface potential of 1.74 volts, while channel length has been reduced to 37.5% of 40 nm. The subthreshold swing for an ideal MOS is 60 mV/ decade.

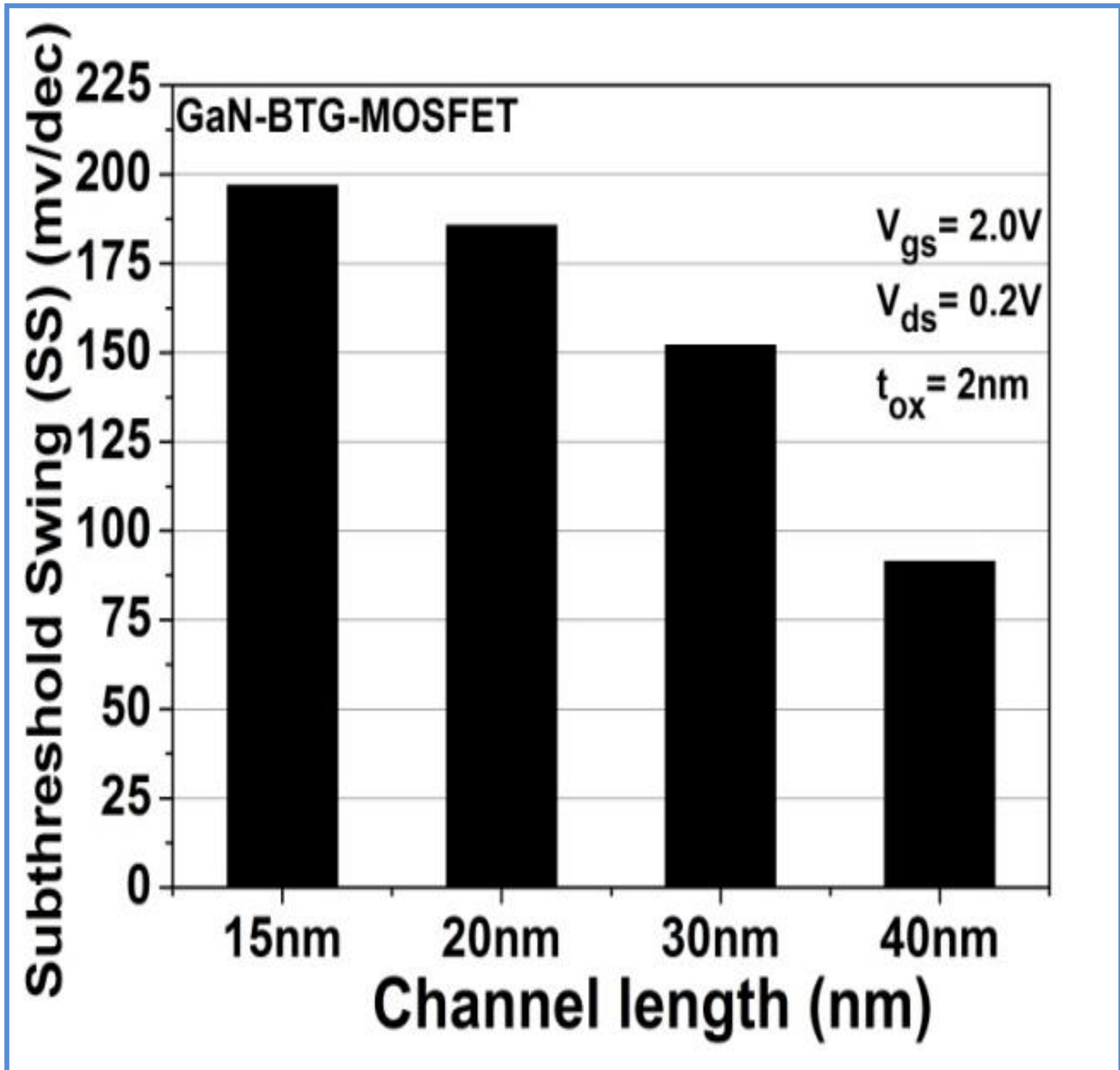


Fig. 19: Sub-threshold Swing of GaN BTG MOSFET with variation in the channel length

From Fig. 19, it can be noticed that the subthreshold swing (SS) of GaN-BTG-MOSFET is expanding with decrementing channel length of the MOSFET. An upsurge of 104% is seen in the Subthreshold swing with a decrease in channel length from 40nm to 15nm. Switching Ratio is portrayed in Fig. 20. The higher the switching ratio of a device better is the turn-on characteristics of the device. Here we observe the maximum switching ratio for 40nm channel length for GaN-BTG-MOSFET, which corrupts with decreasing channel length.

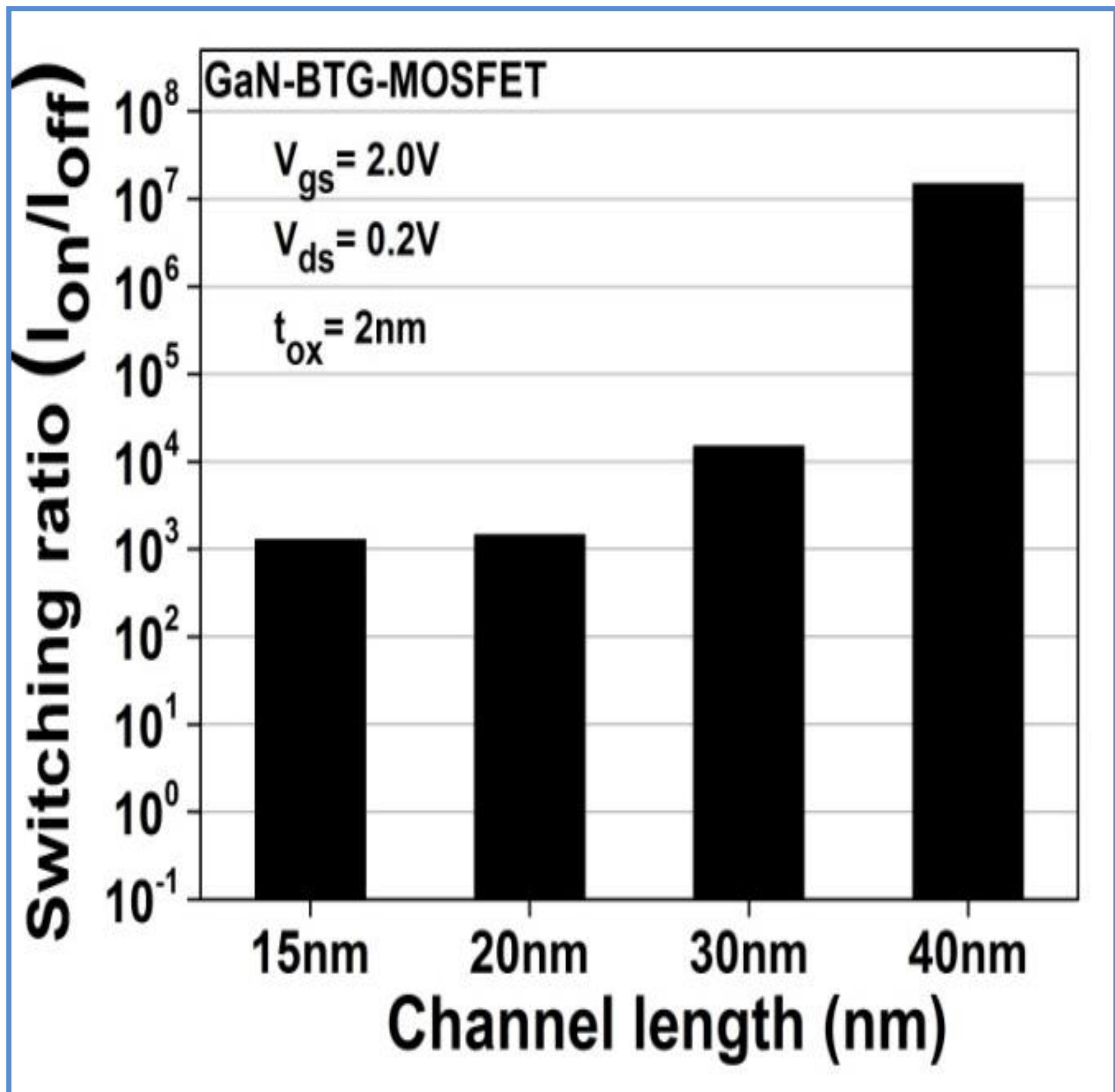


Fig. 20: Switching ratio (I_{ON}/I_{OFF}) for GaN-BTG-MOSFET with variation in the channel length

Fig. 21 shows that with a decrease in channel length, a littler threshold voltage for GaN-BTG-MOSFET is observed. With a reduction in channel length, GaN BTG MOSFET works at a lower threshold voltage and is power efficient[19]. At 15nm channel length, it can be observed threshold voltage value is 0.34V which is 57% of the threshold voltage at 40 nm channel length.

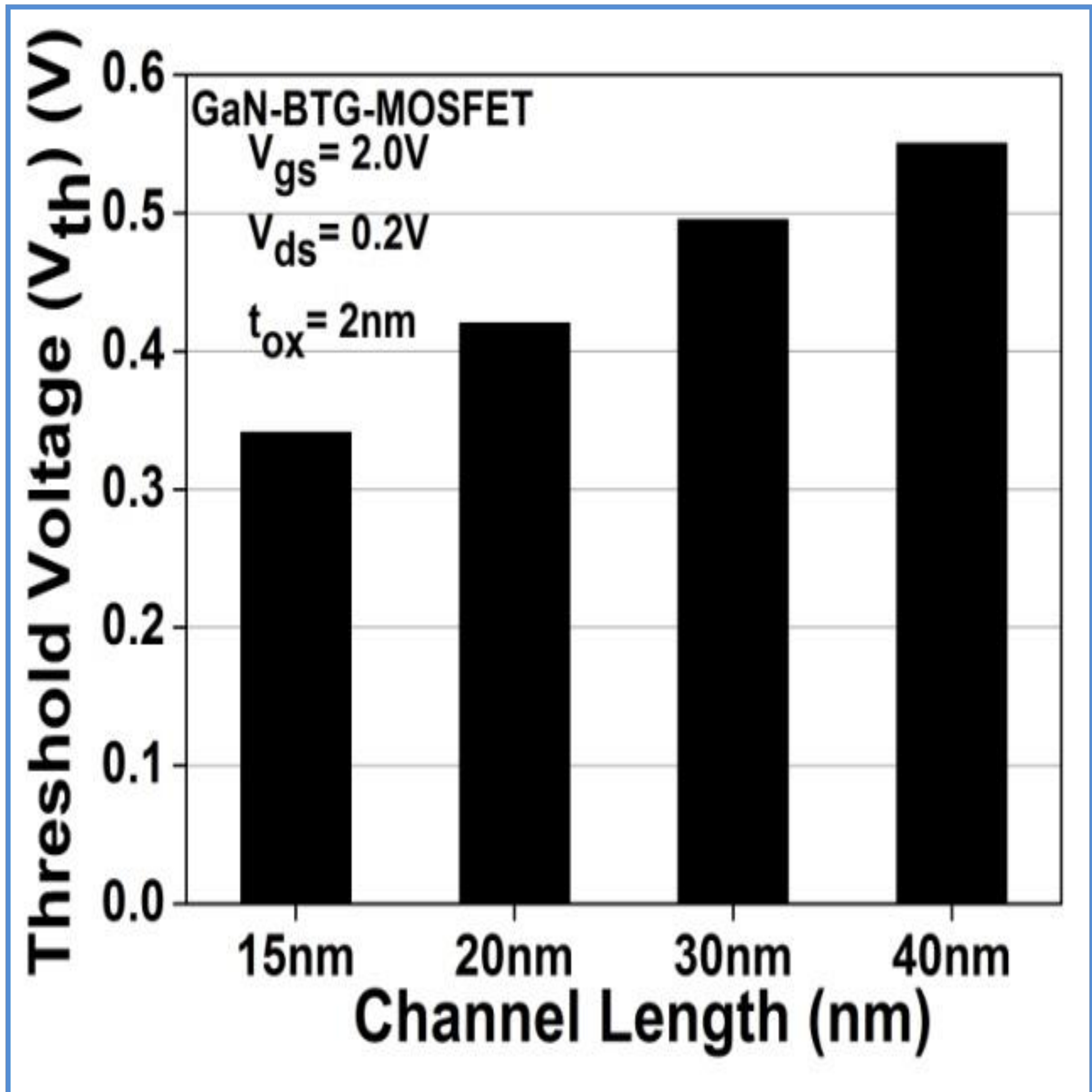


Fig. 21: Threshold voltage for GaN-BTG MOSFET with variation in the channel length.

Further examining GaN BTG MOSFET's boundary, doping concentration of n-type and p-type material is varied, and Different characteristic plots are observed, following table (Table 2) depicts the doping concentration of both n-type and p-type region.

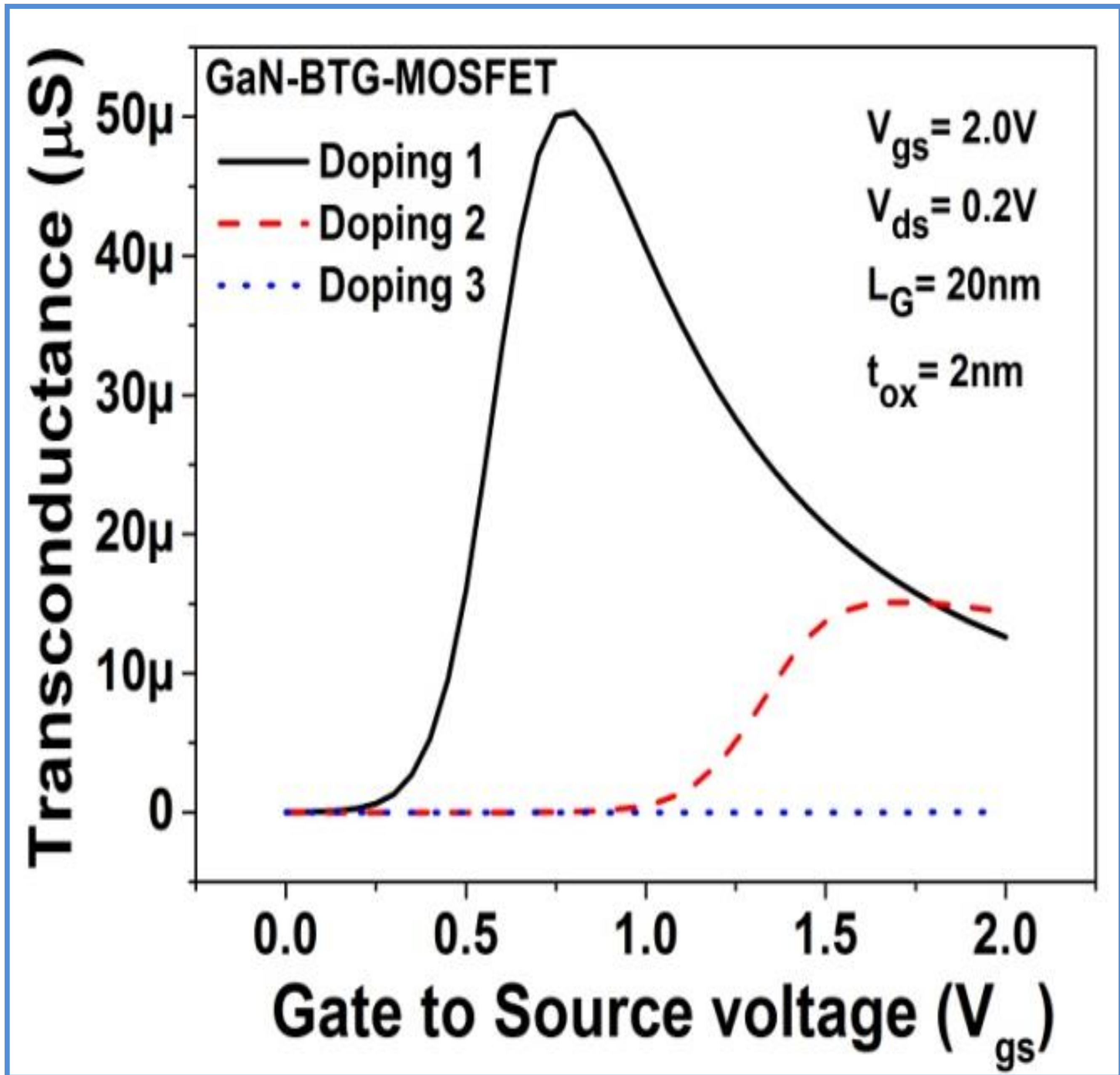


Fig 22 Transconductance versus Gate voltage of GaN-BTG-MOSFET with variation in doping concentration.

Transconductance is the change in drain current with changing gate voltage at constant drain voltage. Fig. 22, shows a basic transconductance for doping level 2. The transconductance of GaN-BTG-MOSFET stays zero if doping concentration is expanded past level 2 doping.

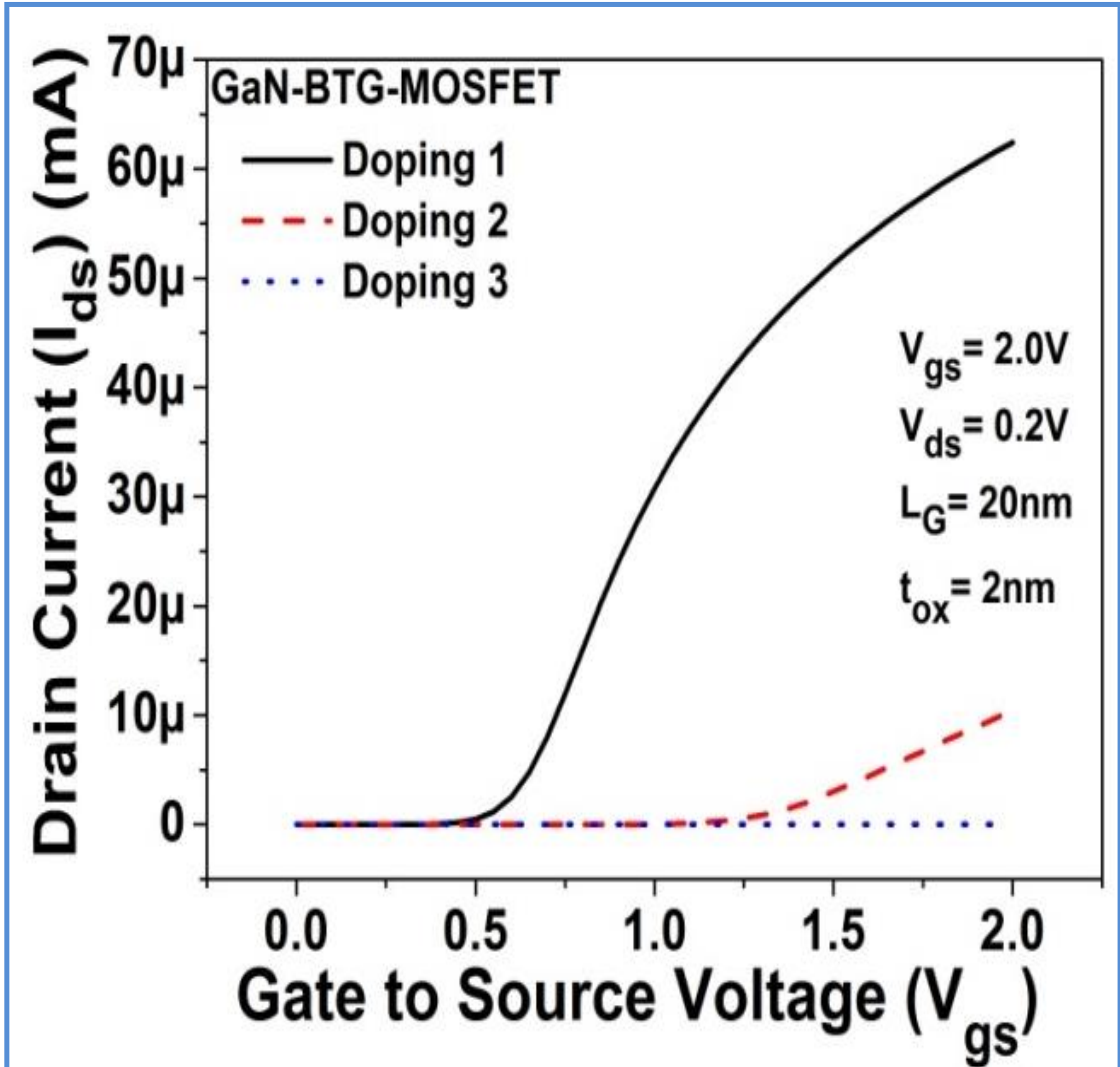


Fig. 23 Transfer characteristics of GaN-BTG MOSFET with variation in Doping concentration.

Table 2: Doping level

Doping Level	P-Type	N-Type
Doping 1	$1*10^{17}$	$1*10^{18}$
Doping 2	$5*10^{17}$	$7*10^{18}$
Doping 3	$1*10^{18}$	$1*10^{19}$

Both Fig 22 and Fig. 23 shows that GaN-BTG-MOSFET will behave as an open circuit if doping concentration is expanded past level 2, indicating infinite on resistance[1]. A similar property can be observed for the transfer characteristics of GaN-BTG-MOSFET with variation in the doping level as indicated previously.

GaN-BTG-MOSFET works in the cut-off region only with increased doping concentration past level 2 doping. With an expansion in the doping concentration level in GaN-BTG-MOSFET, we observe high barrier potential (allude Fig. 24). Here, the device behaves as an open-circuit for applied gate voltages.

This is the principal explanation for level 3 doping disappointment in GaN-BTG-MOSFET. It can be observed that with an expansion in doping concentration, the subthreshold swing of the GaN-BTG-MOSFET (Fig 25) has been decreased and it approaches the MOSFET's ideal subthreshold swing value at doping concentration level 3.

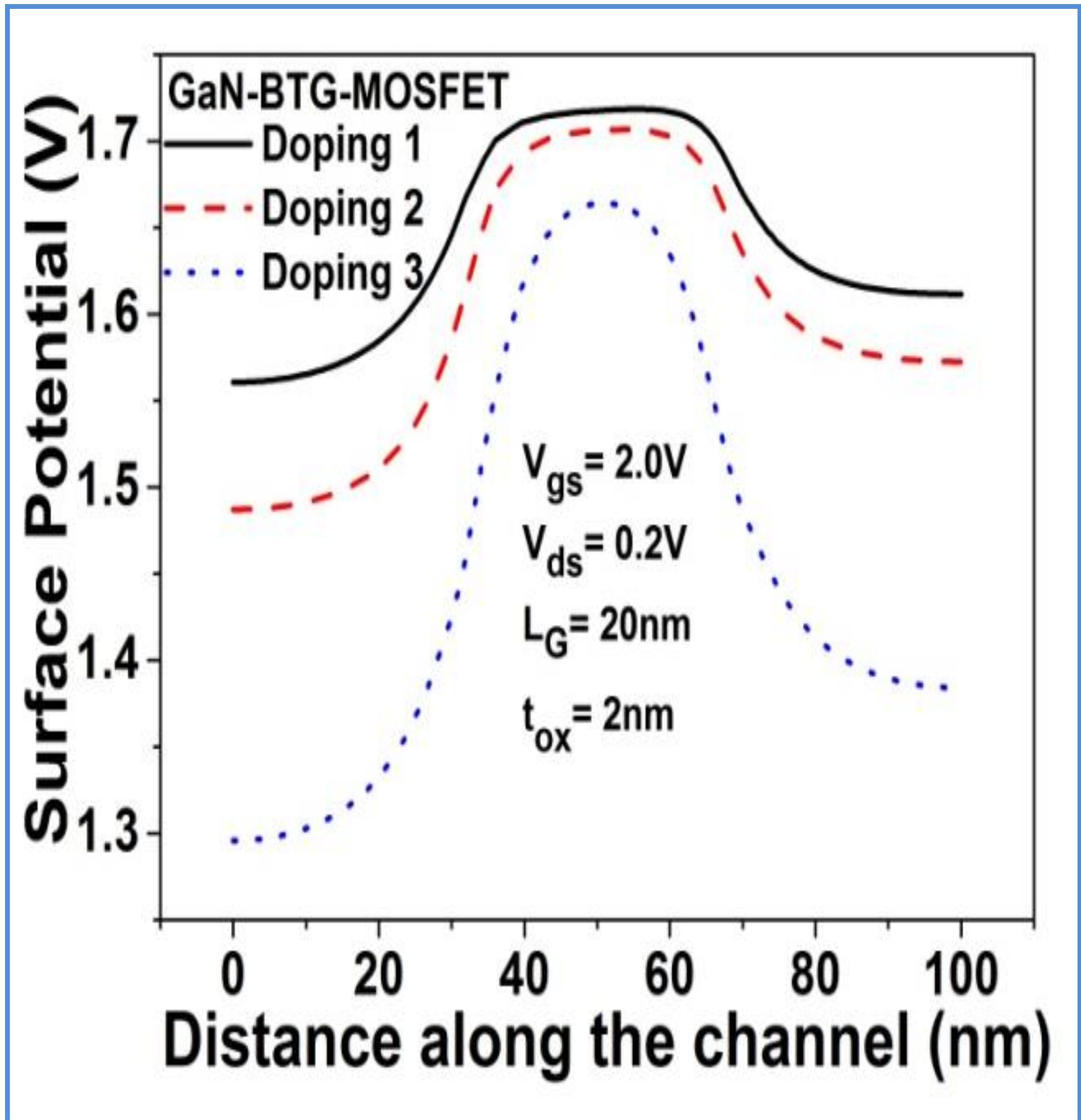


Fig. 24 Surface potential along the channel GaN-BTG-MOSFET with variation in doping concentration.

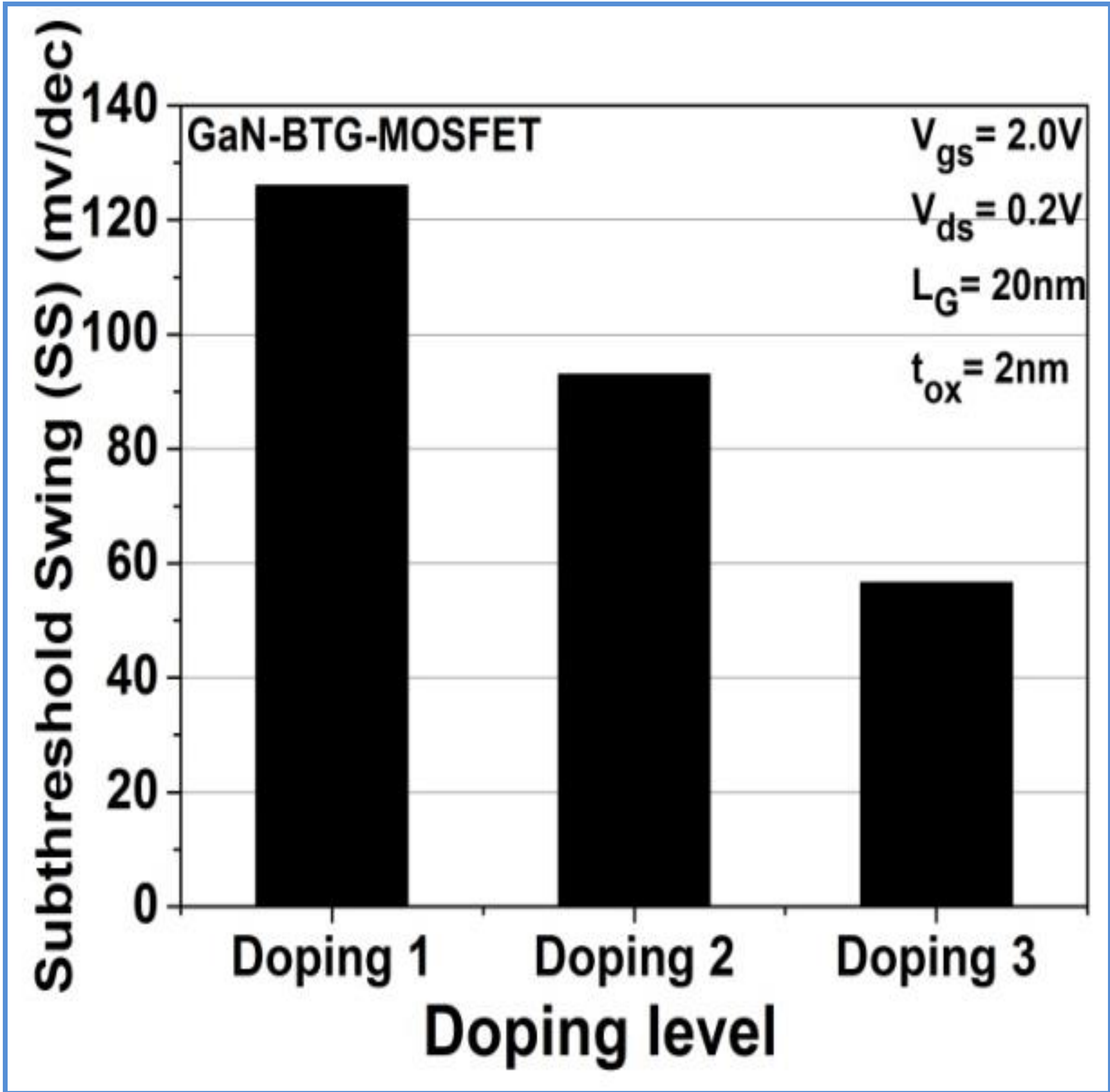


Fig. 25 Subthreshold Swing for GaN-BTG-MOSFET with variation in Doping concentration

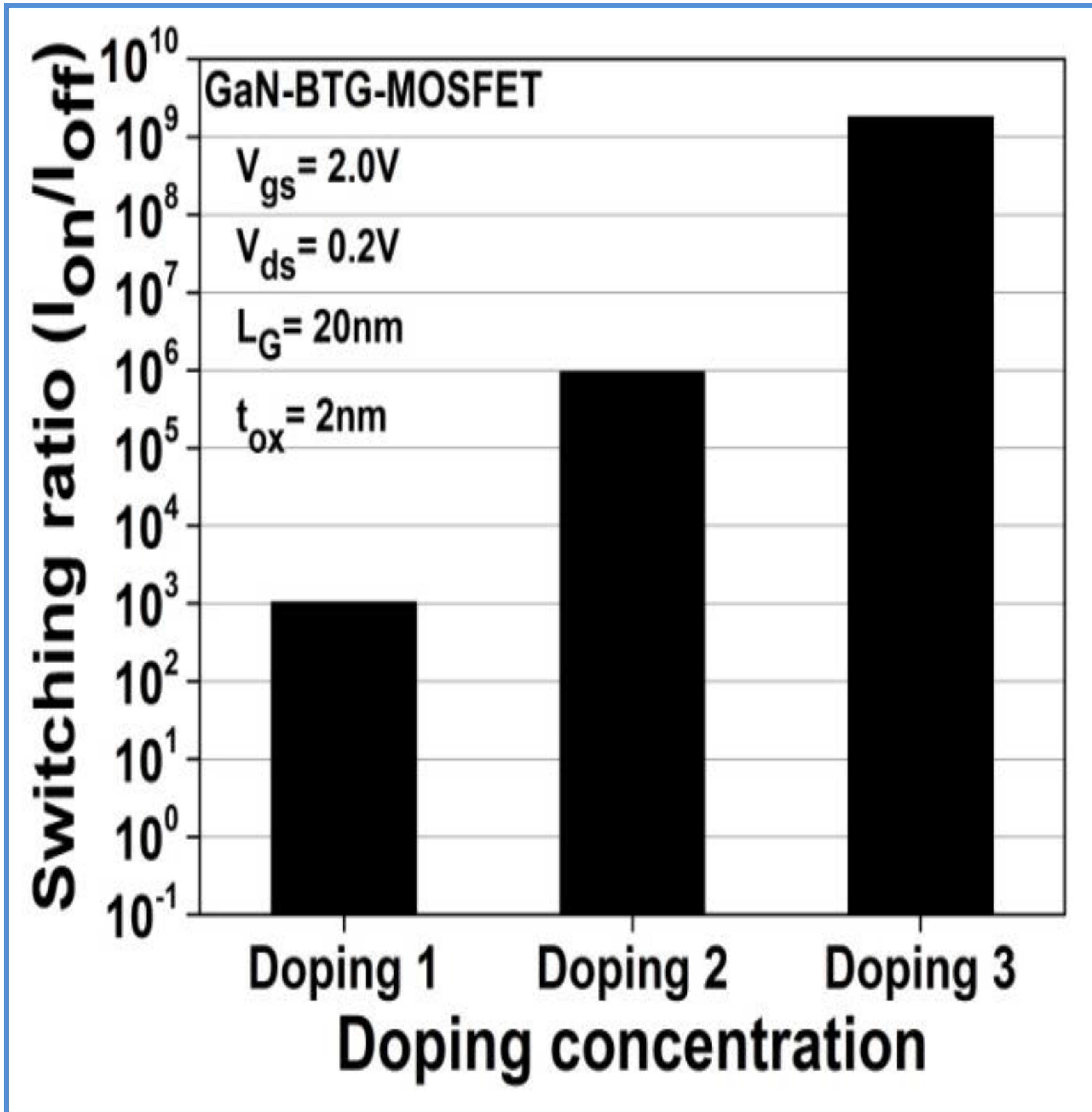


Fig. 26 Switching ratio for GaN-BTG-MOSFET with variation in Doping concentration

Fig. 26 shows the switching ratio of GaN-BTG-MOSFET with variety in doping concentration. With an expansion in doping concentration, switching ratio value for GaN-BTG-MOSFET diminishes to 10^3 at doping level 3 from 10^9 at doping level 1. An expansion in doping concentration past level 2 outcomes in the activity of GaN-BTG MOSFET in the cut-off region.

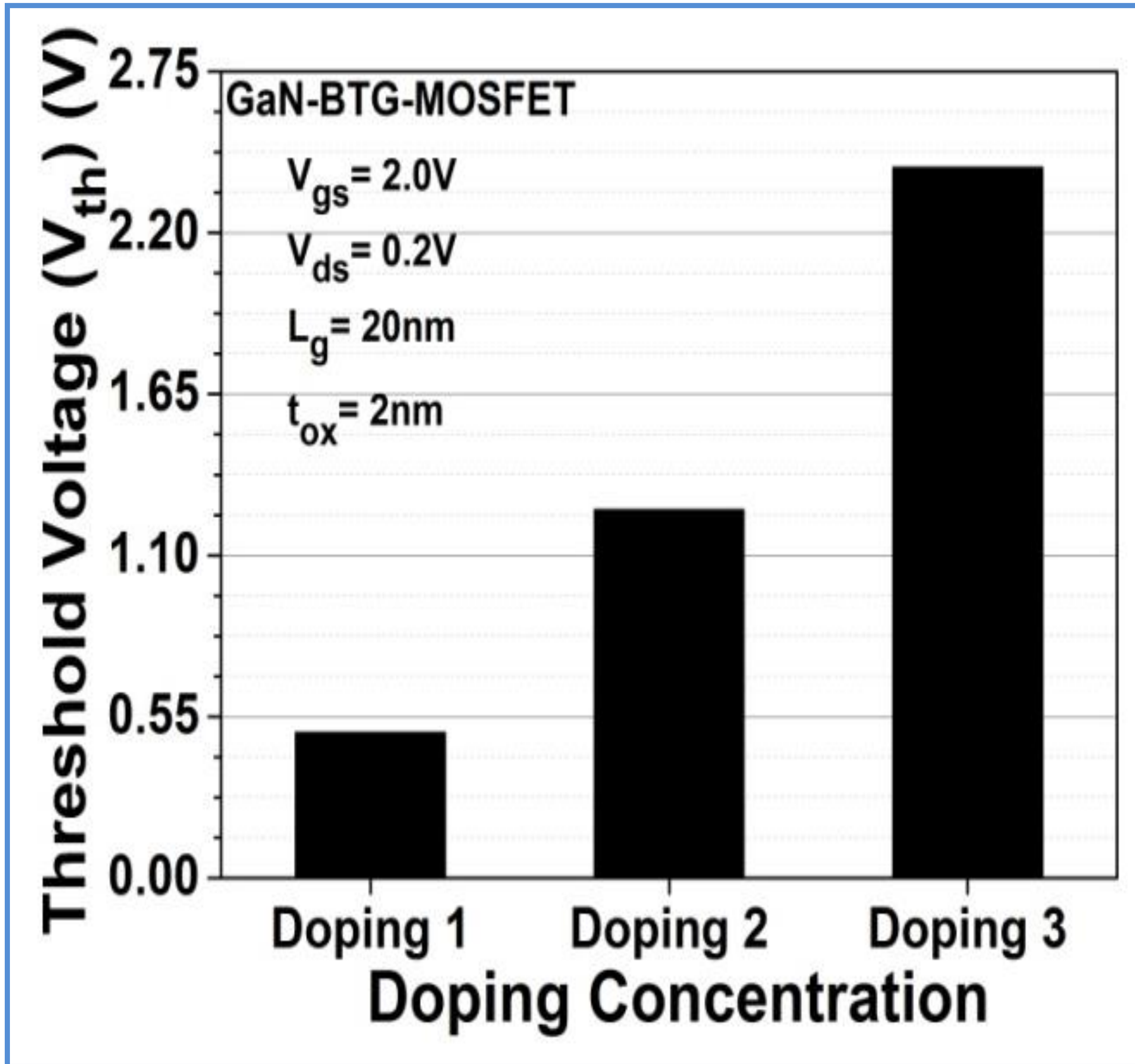


Fig. 27 Threshold Voltage for GaN-BTG MOSFET with variation in Doping concentration

Fig. 27 portrays that with an expansion in doping concentration, the threshold voltage of the device has been increased by 392.85% and is noted to be 2.415V.

During the simulation, a gate voltage is increased up to 2 volts only hence MOSFET at Level 3 doping will be in the cut-off region behaving as an open circuit. Proceeding with the further examination, thickness oxide (t_{ox}) of GaN BTG MOSFET is varied and change in parametric qualities has been discussed. At first, t_{ox} is taken as 2nm, which is changed to 1nm and 3 nm, and perceptions are recorded and investigated as follows.

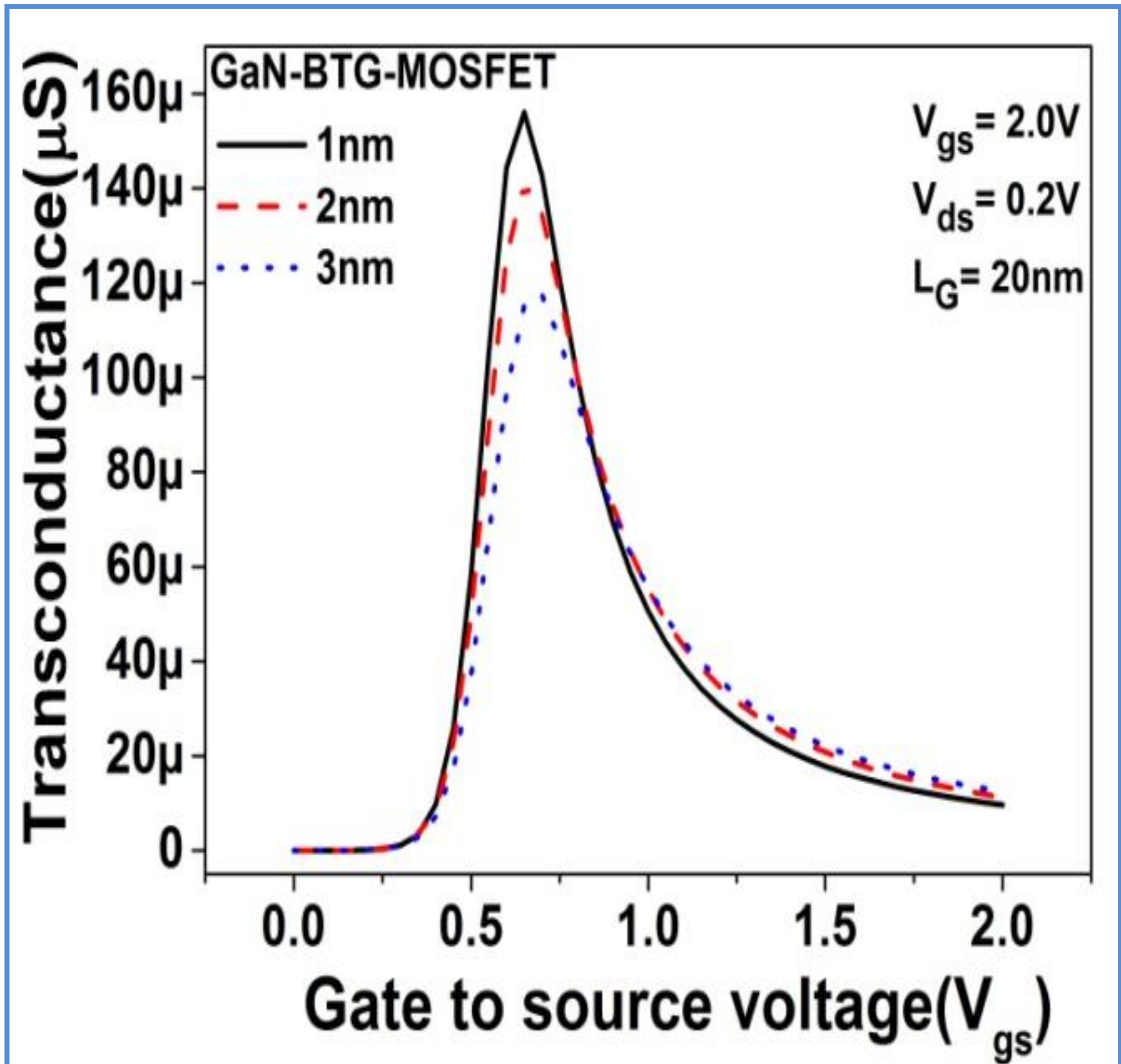


Fig. 28 Transconductance versus Gate voltage of GaN-BTG-MOSFET with variation in oxide thickness

Fig. 28 infers that the decrement in the thickness of the oxide increases the transconductance of the device. Here 33.3% improvement is seen in transconductance while diminishing effective thickness of the oxide (t_{ox}). Transfer characteristics of GaN-BTG MOSFET are observed in Fig. 29 with variation in thickness of the oxide in the device.

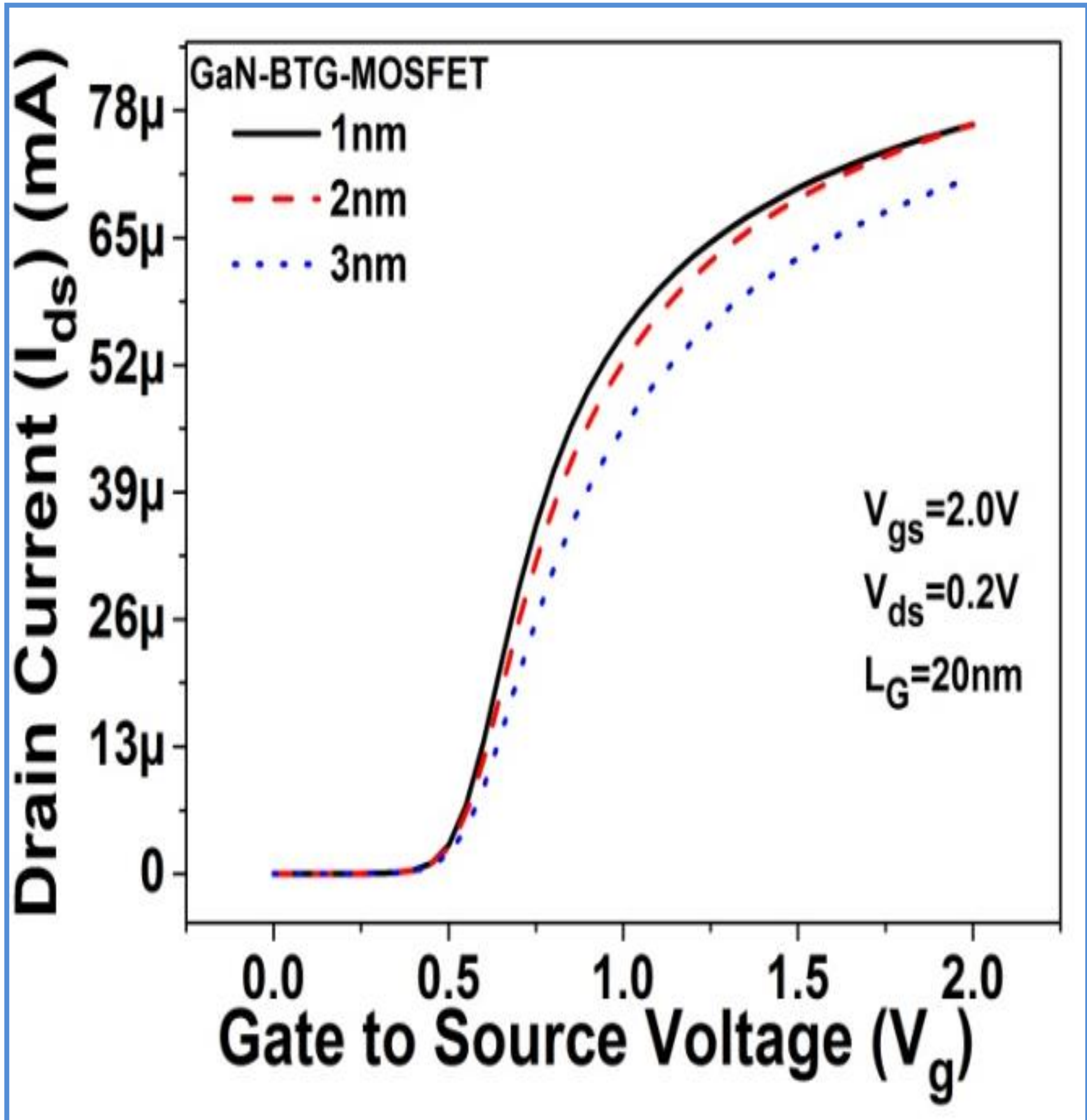


Fig. 29 Transfer characteristics GaN-BTG MOSFET with variation in oxide thickness

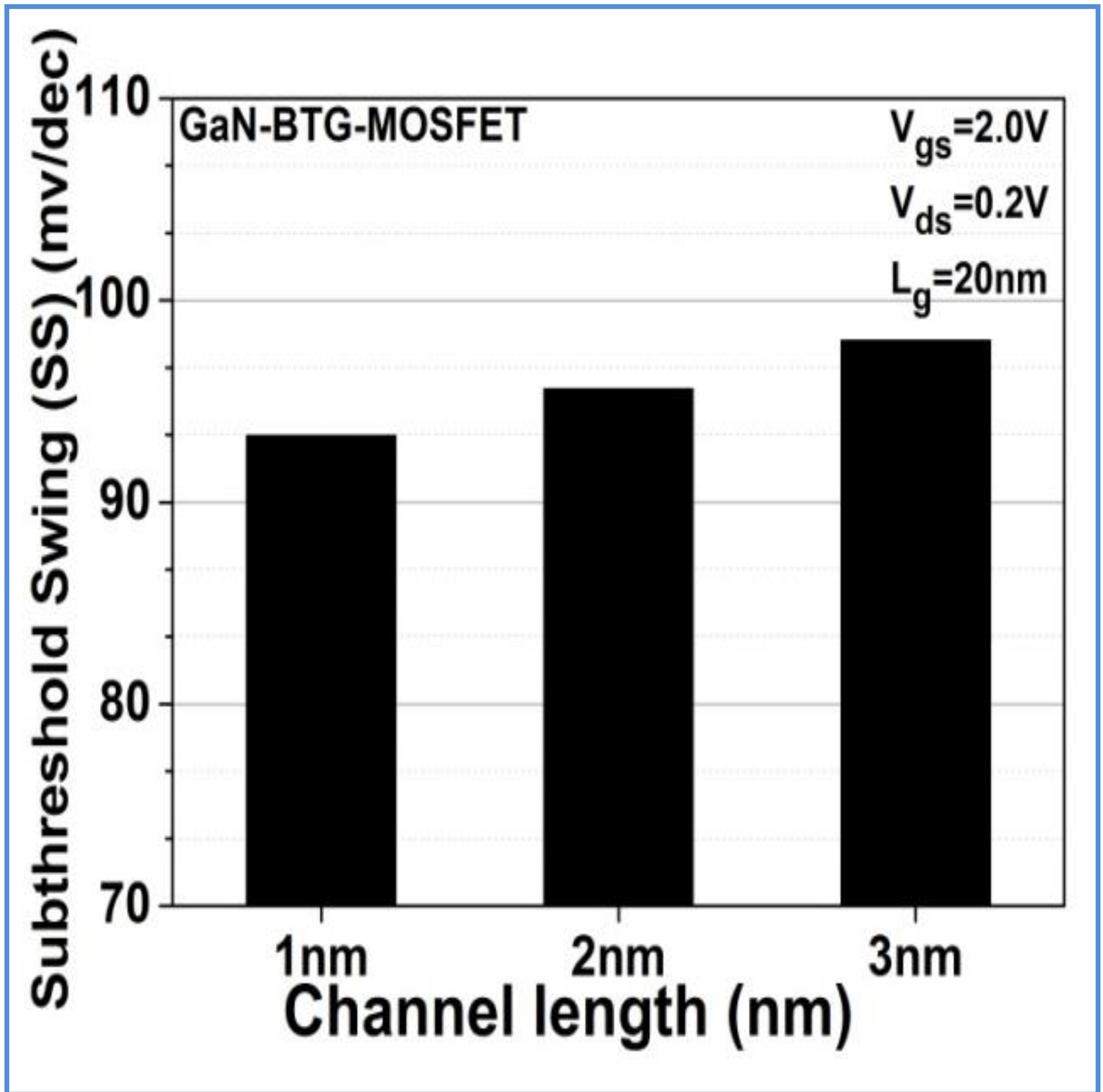


Fig. 30 Subthreshold Swing for GaN-BTG MOSFET with variation in oxide thickness

At 1nm thickness of the oxide, the higher channel current is observed at the same Gate voltage. With the decrease in effective oxide thickness (t_{ox}), gate capacitance C_{ox} improves which results in better gate control[20]. With increased C_{ox}, the transconductance of the device is improving which results in better channel current I_d.

From Fig. 30 it tends to be seen that subthreshold swing (SS) is having a variation of ±2.1% with the scaling of the thickness of the effective oxide layer from 3nm to 1nm. It is seen that with variation in t_{ox}, GaN-BTG-MOSFET shows minuscule changes in the subthreshold swing.

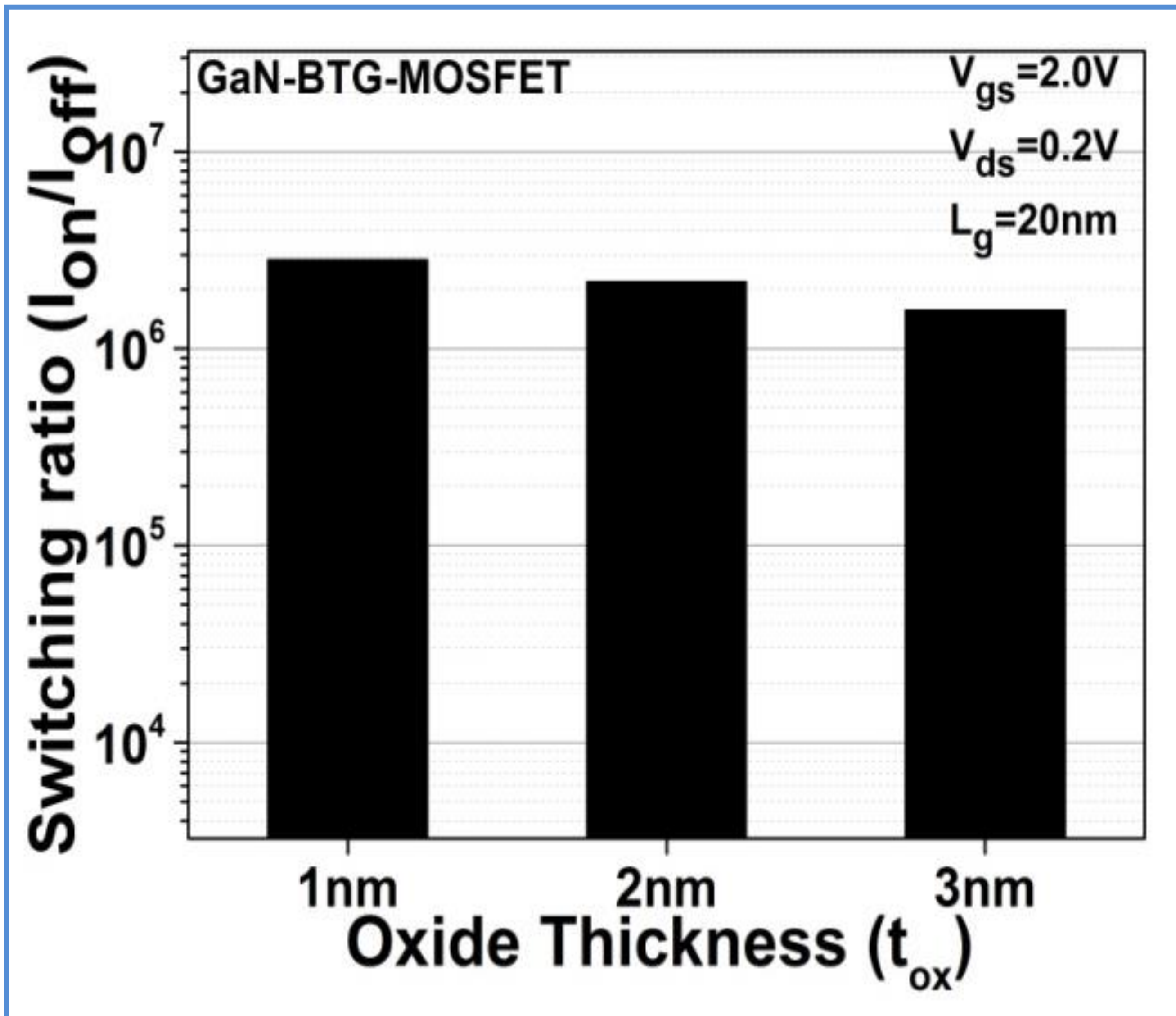


Fig. 31 Switching ratio for GaN-BTG-MOSFET with variation in oxide thickness

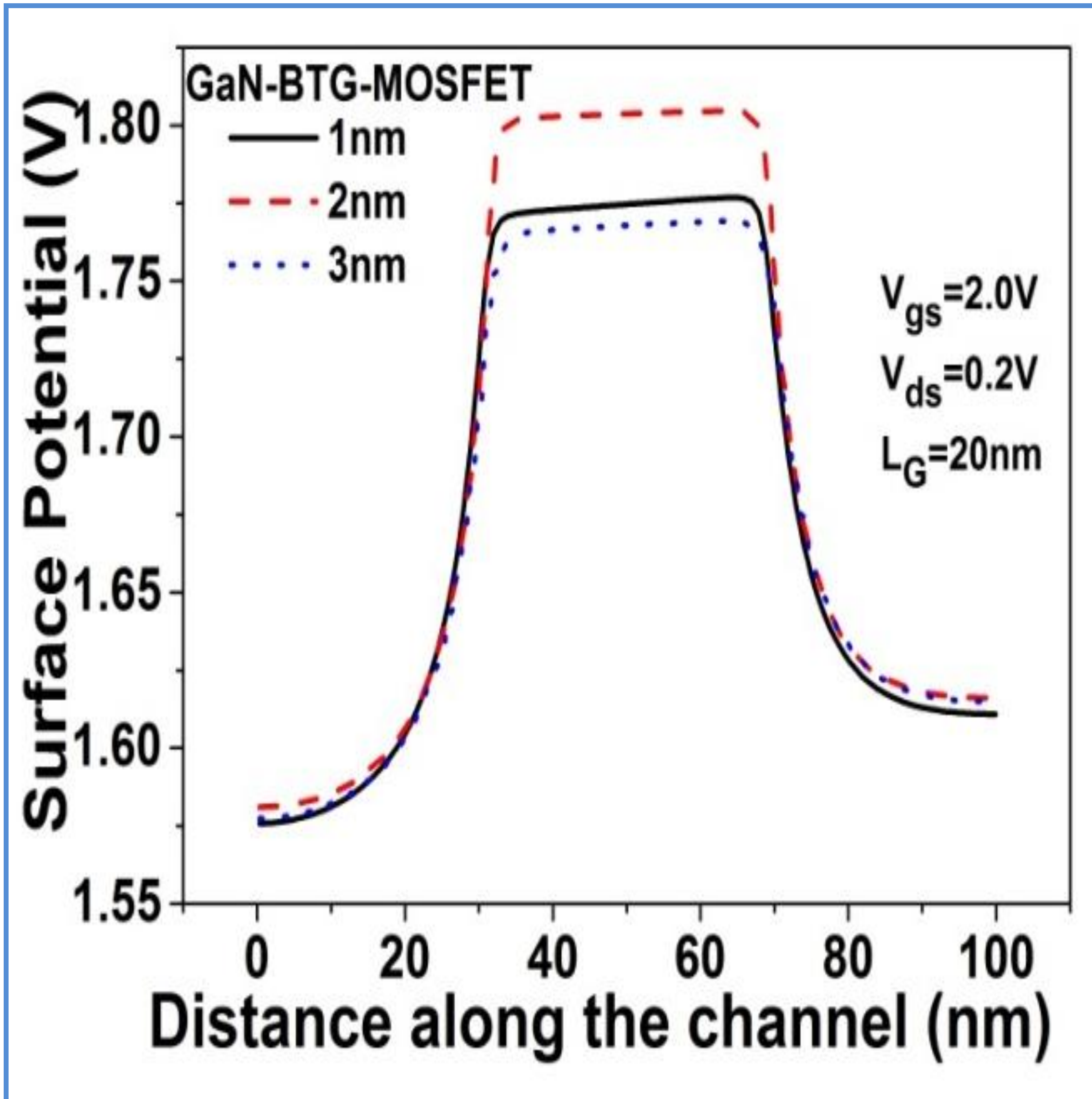


Fig. 32 Surface potential along the channel GaN-BTG-MOSFET with variation in oxide thickness

Fig 31 shows the Switching ratio, characterized as the ratio of on-current and off-current of GaN-BTG-MOSFET with variation in thickness of oxide is discovered to be steady and is equivalent to 10^7 for the variation in effective oxide thicknesses (1nm, 2nm, and 3nm).

High switching ratio advocates for a quicker switching device, which shows better gate control of the device. Here decrement in oxide thickness builds the oxide capacitance (C_{ox}) which improves the gate control of the device[20].

Surface potential (Fig. 32) represents the adjustment in barrier potential with a change in oxide thickness. Reduced barrier potential is observed for the diminished thickness of the oxide layers which depicts that with diminishing oxide thickness in GaN-BTG-MOSFET, threshold voltage represented by Fig 33 of the device is also reducing. At t_{ox}=2nm, the threshold voltage of GaN-BTG-MOSFET is seen to be 0.469V.

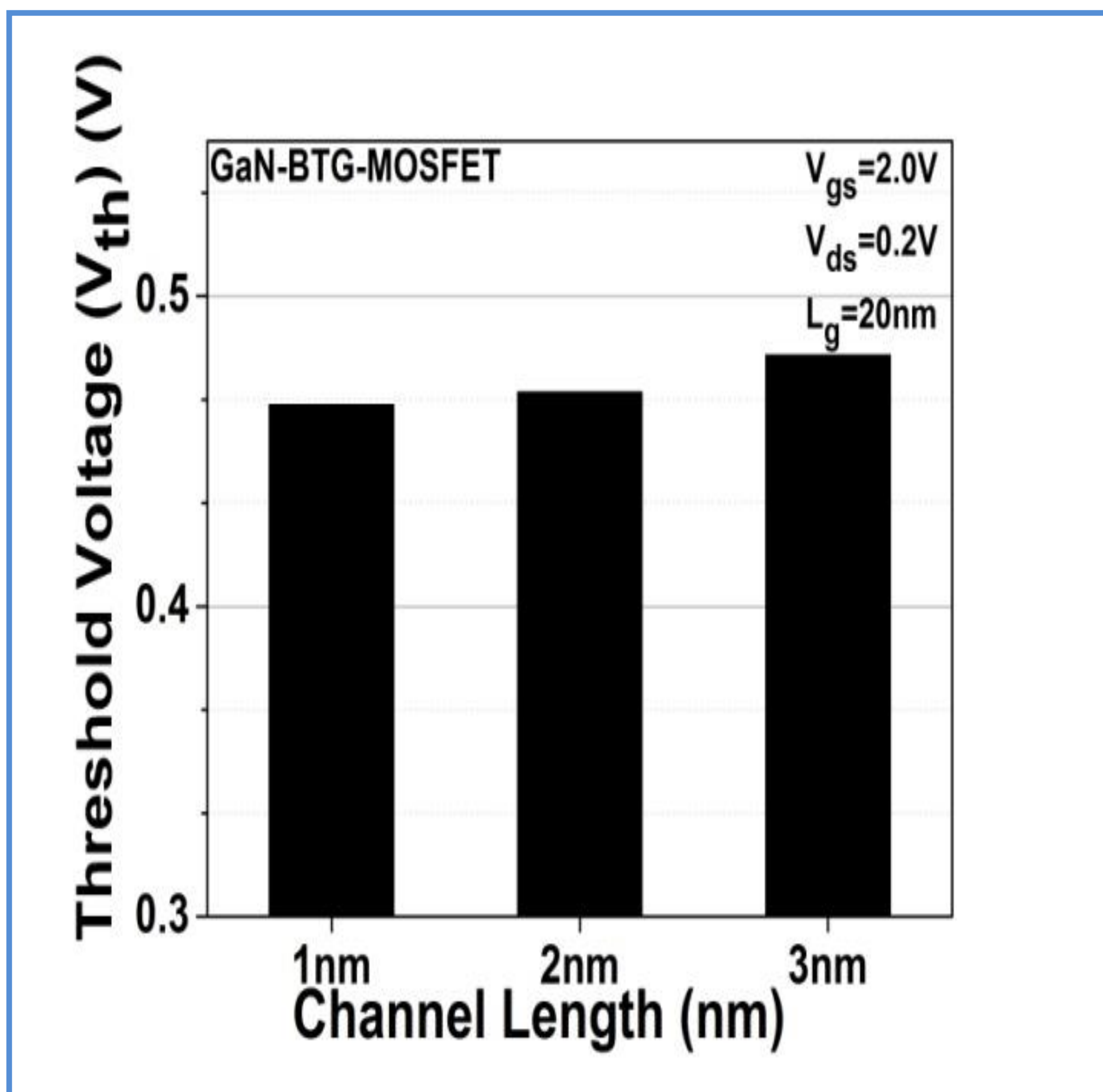


Fig. 33 The threshold voltage for GaN-BTG-MOSFET with variation in oxide thickness 5nm, 20nm, 30nm, and 40 nm.

On diminishing the thickness of oxide to 1nm, threshold voltage reduces to 0.465V (0.8% of 2nm), and on expanding thickness of oxide to 3nm, the threshold voltage of 0.481V is recorded (2% of 2nm). This information portrays that with variation in oxide layer thickness, there is no effect on the operational behavior of GaN-BTG-MOSFET and GaN-BTG MOSFET can be scaled at 1nm thick oxide layer.

4.2 TEMPERATURE ANALYSIS:

Electrical Characteristics of both CTG-MOSFET and GaN-BTG MOSFET are concentrated with increasing temperature using the Silvaco-TCAD ATLAS tool. Different performance characteristics plotted are presented below. Fig. 34 shows the Transconductance concerning the gate voltage of GaN- BTG-MOSFET and CTG-MOSFET at various temperatures.

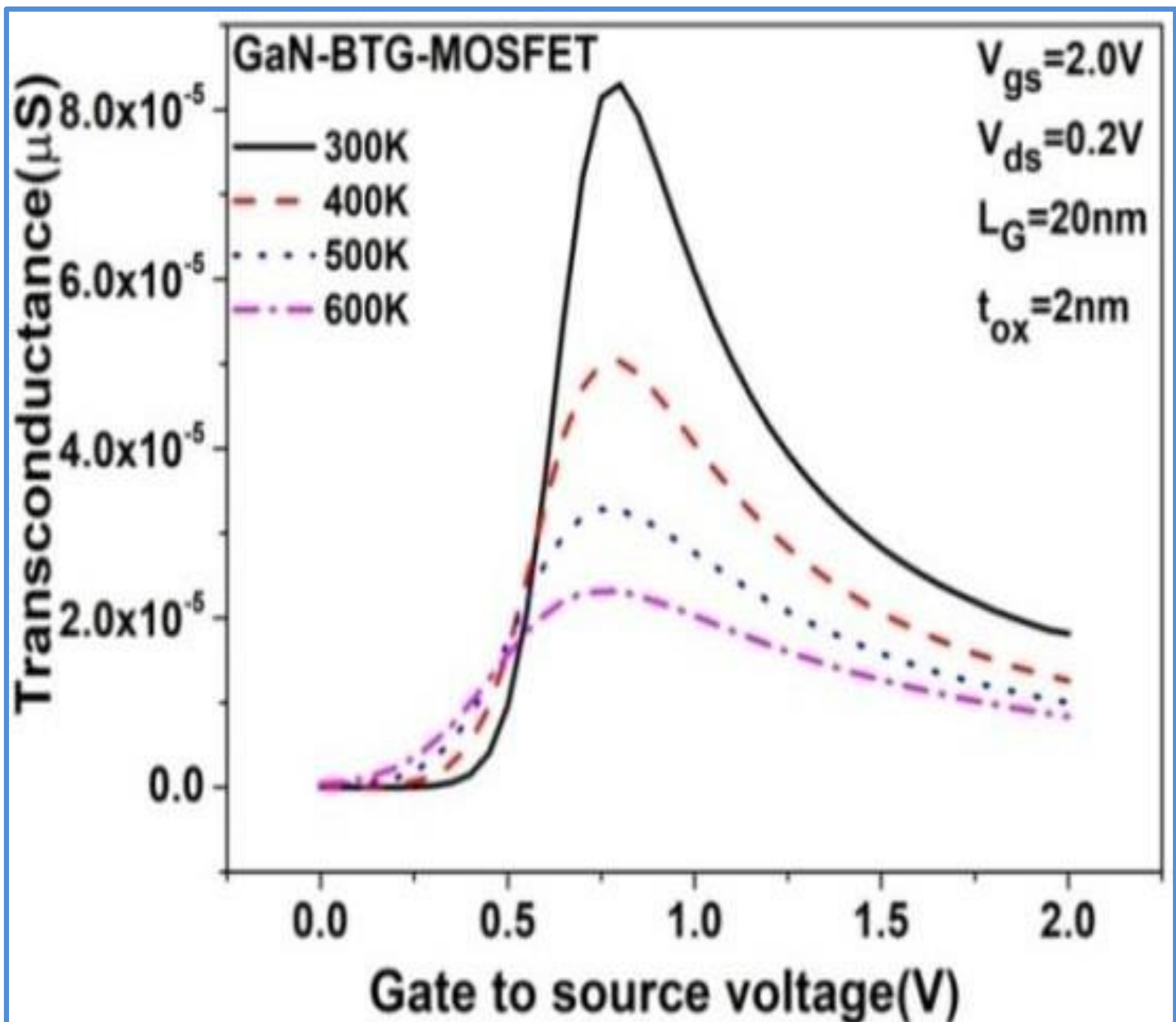


Fig. 34 Transconductance of GaN-BTG-MOSFET concerning gate voltage.

The transconductance of GaN-BTG-MOSFET is higher than that of CTG-MOSFET at 300K, which is result of the higher electron mobility of GaN than silicon. With the increase in temperature transconductance of both the devices decline, in view of the increased scattering of the electrons resulting in diminished transconductance[11].

From the plots in Fig.34, it can likewise be seen that transconductance shows a higher reliance on the temperature on account of CTG MOSFET when contrasted with GaN-BTG-MOSFET which demonstrates the better thermal stability of GaN when contrasted with Silicon material.

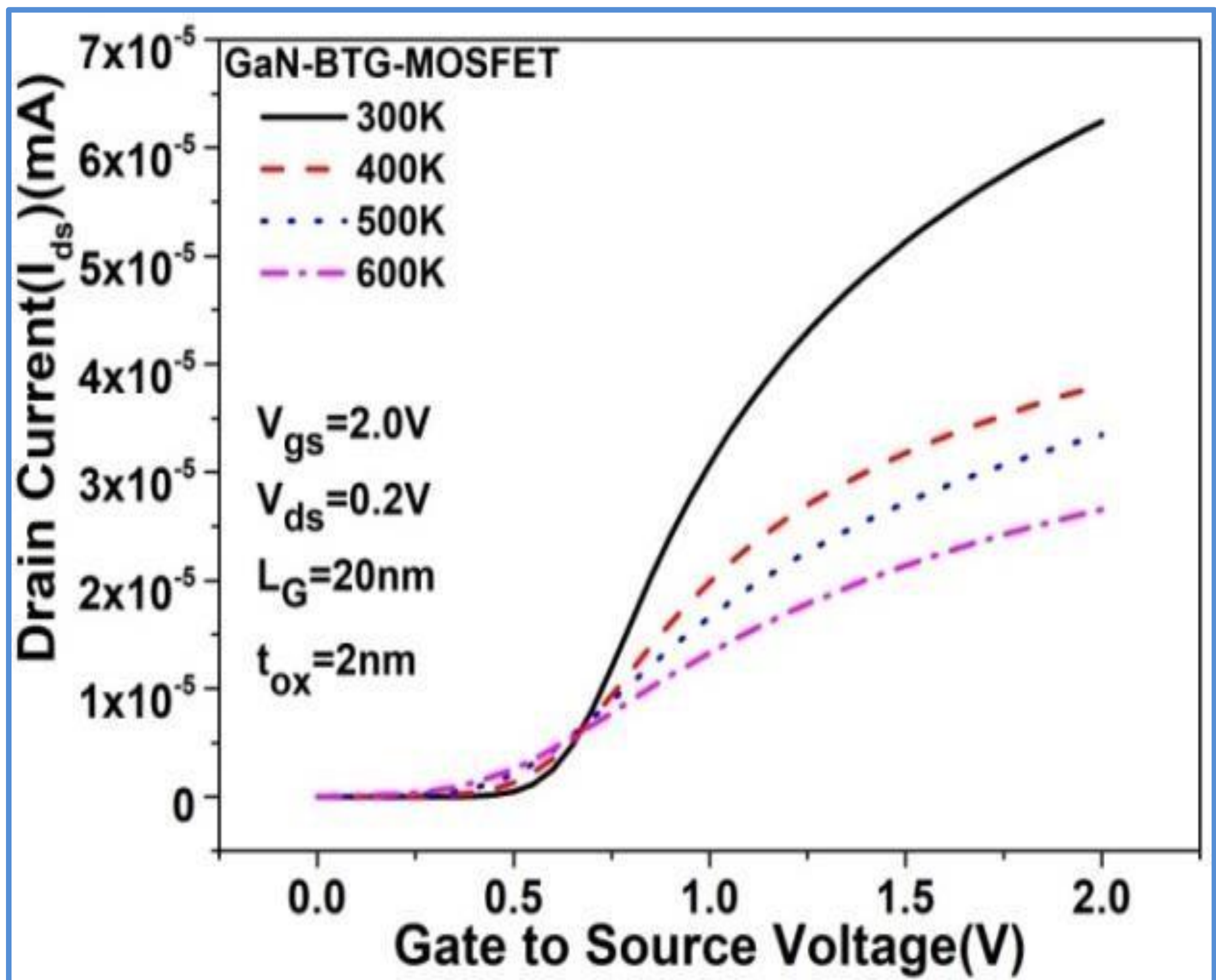


Fig. 35 Transfer characteristics of GaN-BTG-MOSFET at different temperatures

Fig. 35 clarifies the conduct of channel current with gate voltage at various temperatures for GaN-BTG-MOSFET and CTG-MOSFET. Due to the higher electron mobility of GaN as for silicon, a higher channel current(I_d) is seen in GaN-BTG-MOSFET despite comparative biasing in both devices.

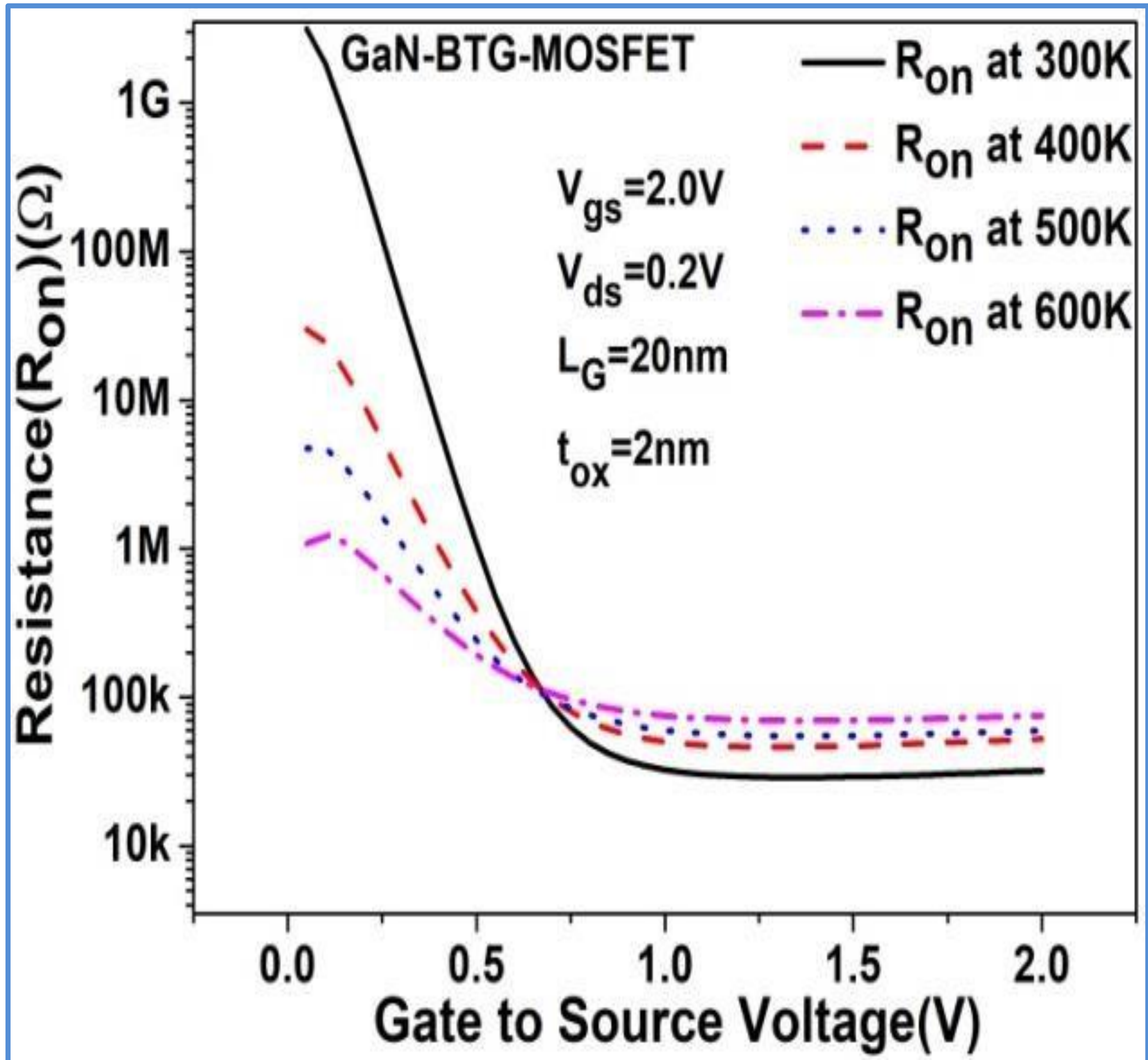


Fig. 36 On-Resistance of GaN-BTG-MOSFET at different temperatures

With the increase in temperature, scattering in the channel increases, and these outcomes in a decrease of channel current at higher temperatures. Despite an increase in temperature, the threshold voltage of GaN-BTG-MOSFET is steady when contrasted with CTG-MOSFET. This little change in the threshold voltage with increasing temperatures likewise shows the thermal stability of GaN-BTG-MOSFET concerning conventional MOSFET. Any device which has current flowing through it offers some resistance.

From Fig. 36 we can observe that with increasing voltage, ON-Resistance (R_{on}) of GaN-BTG MOSFETs diminishes considerably when contrasted with CTG- MOSFET. Before the threshold voltage (V_{th}) R_{on} for CTG- MOSFET is in the range of 10 M Ω while for GaN-BTG-MOSFET it is beyond GΩ and after V_{th}, it scales down to 100 K ohms for both the devices.

Also, at 300K it is observed that R_{on} of GaN-BTG-MOSFET is less than CTG-MOSFET. Further, with increasing temperature, ON-Resistance for GaN- BTG-MOSFET increments while that of CTG-MOSFET diminishes and this decrement in R_{on} with increasing temperature advocates that the leakage current in CTG- MOSFET is also increasing and the ceaseless increasing resistance for GaN-BTG-MOSFET with increasing temperature arguments that the GaN-based device is thermally more stable and can be utilized in semiconductor ICs.

Fig. 37 portrays the Switching Ratio (I_{on}/I_{off}) of GaN-BTG- MOSFET at various temperatures (300- 600K) and contrasted with that of CTG MOSFET. The switching ratio is the ratio of I_{on} obtained at $V_{gs} = 0.7V$ and I_{off} obtained at $V_{gs}= 0V$.

At 300K it very well may be seen that the Switching Ratio of GaN-BTG- MOSFET is multiple times (10^3) times that of CTG MOSFET. GaN-BTG- MOSFET exhibits the quicker switching speed as for CTG-MOSFET at 300K and brings about a lower leakage current which reduces power dissipation and results in a power-efficient device. With the increase in temperature, switching ratio decays for GaN-BTG-MOSFET, following the decrease in channel current while leakage current decreases as shown in Fig. 35.

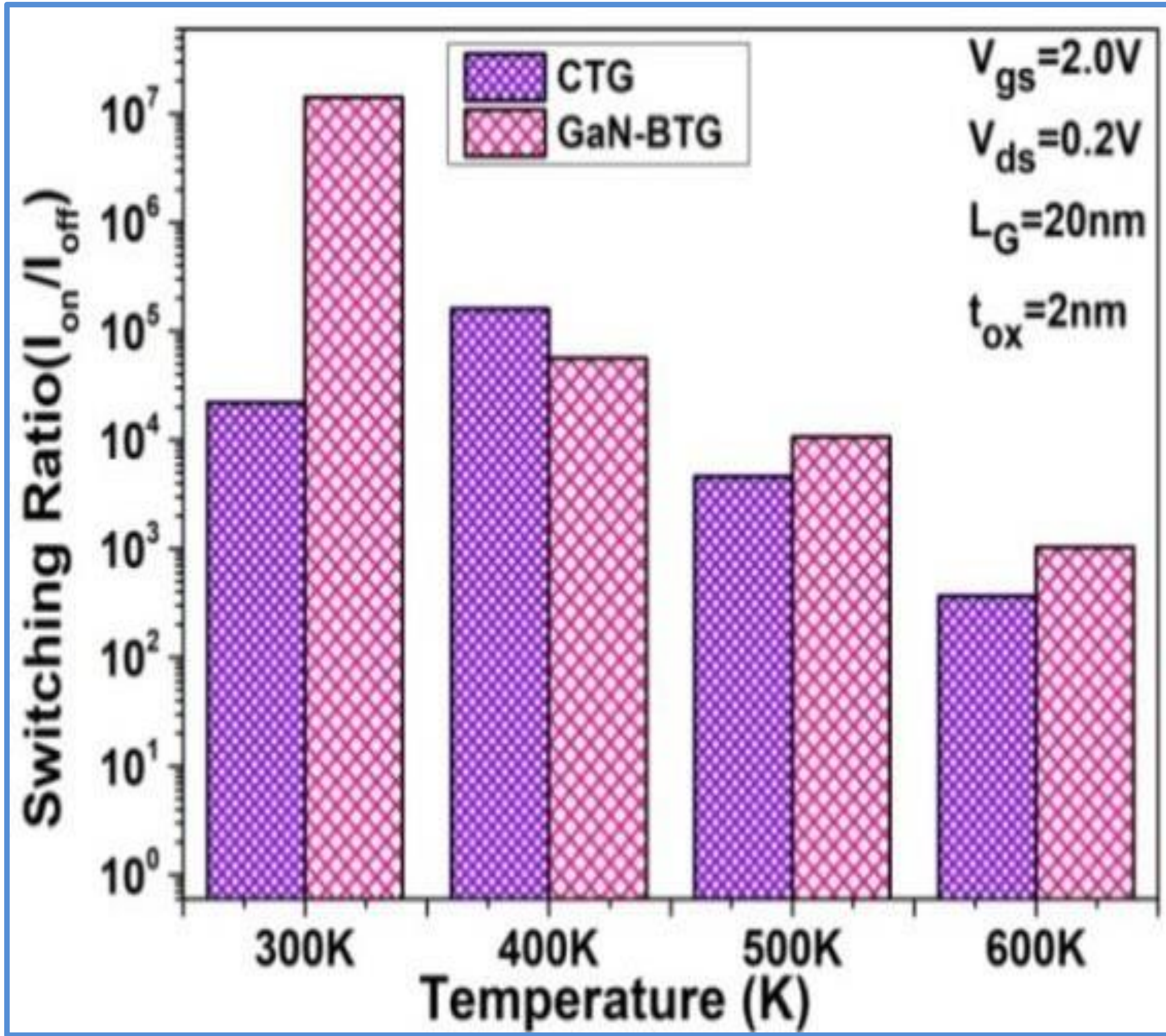


Fig. 37 Switching ratio of CTG MOSFET and GaN-BTG-MOSFET at different temperatures.

Fig. 38 gives the record of threshold voltage V_{th} at various temperatures for GaN-BTG MOSFET and contrasted with that of CTG-MOSFET. GaN-BTG-MOSFET shows a lower V_{th} when contrasted with CTG-MOSFET at 300K and increasing temperature change in V_{th} is less in GaN-BTG-MOSFET when contrasted with CTG-MOSFET, this is because GaN is thermally more stable than that of silicon. With lesser deviation in threshold voltage with temperature makes GaN-BTG- MOSFET a substitute of CTG MOSFET that could be installed in ICs.

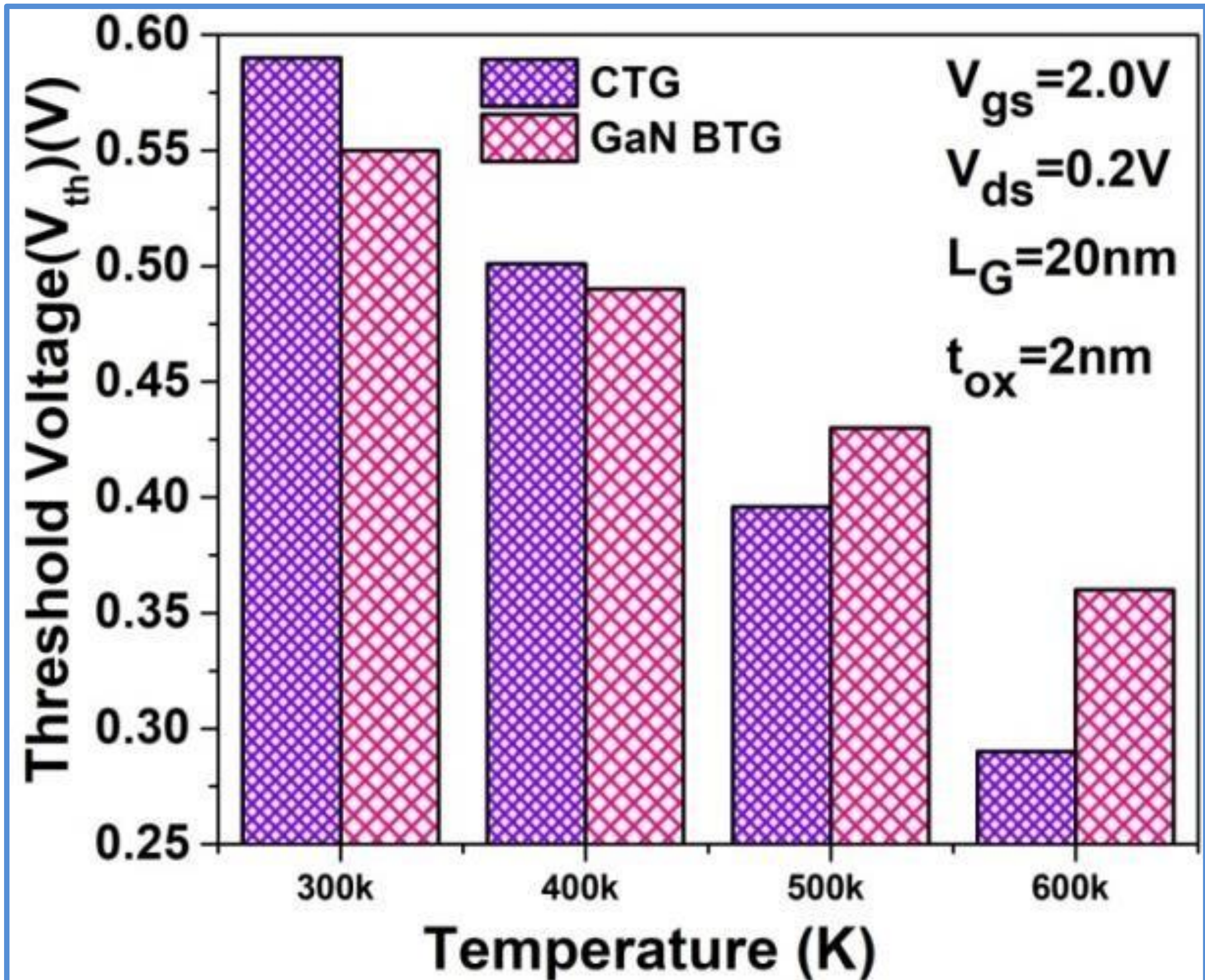
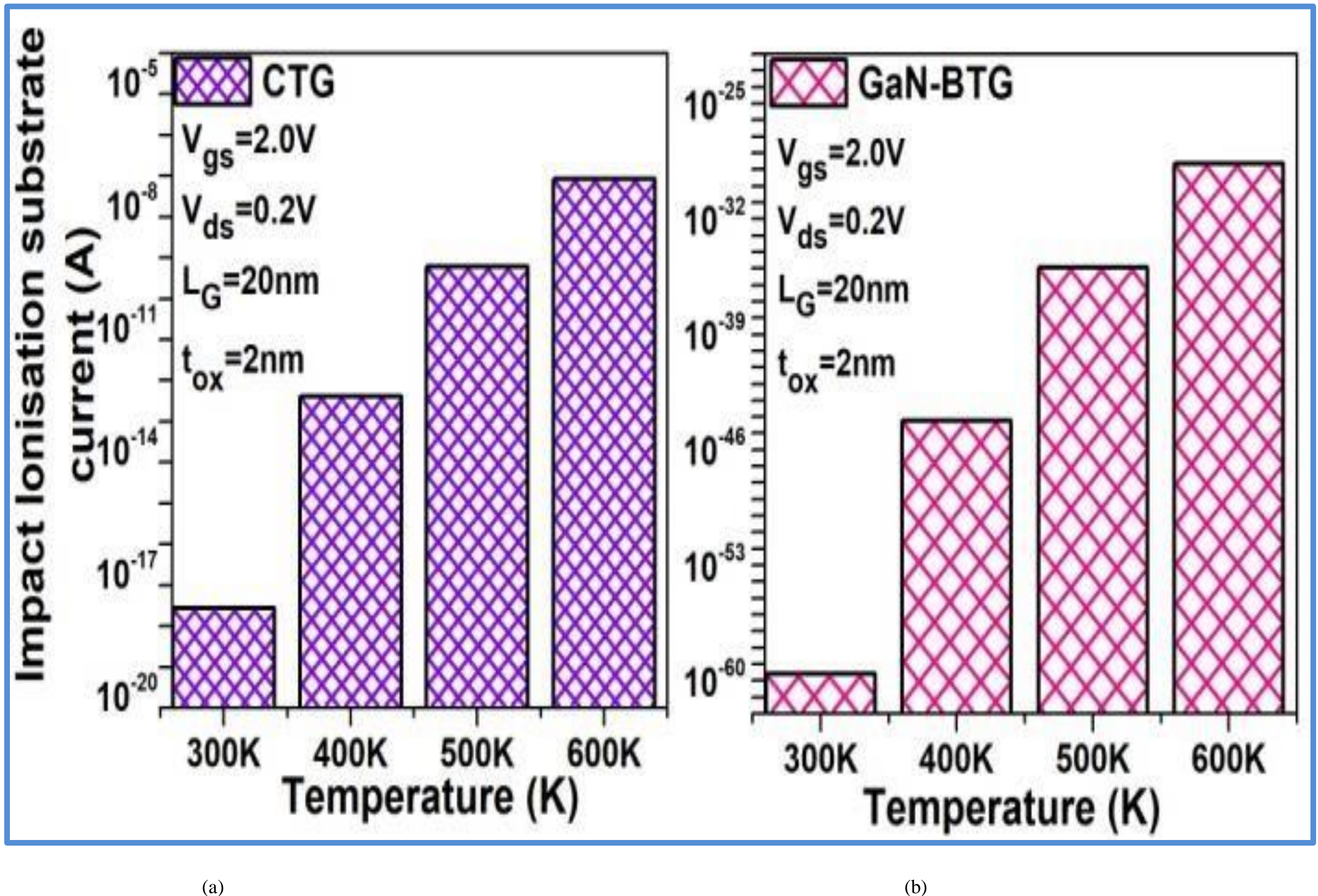


Fig. 38 The threshold voltage (V_{th}) of CTG MOSFET and GaN-BTG-MOSFET at different temperatures.

Fig. 39 portrays the maximum impact ionization substrate current ($I_{sub, max}$) for GaN-BTG-MOSFET at various temperatures and contrasted with that of CTG. The impact ionization substrate current in the MOSFET occurs when the electron in the channel region injects into the substrate region[17].

At 300K, $I_{sub, max}$ for GaN-BTG-MOSFET is of the order of 10^{-60} and that of CTG MOSFET is in the order of 10^{-20}. This delineates the utilization of GaN-BTG-MOSFET will be more power-efficient.

With the increase in temperature, Isub, max increases for both CTG and GaN BTG-MOSFET. Increment in case of CTG is of the order 10^{-3}, while increase in event of GaN-BTG-MOSFET is of the order 10^{-7}, this relation delineates that GaN-BTG-MOSFET is thermally more stable and more power-efficient than CTG MOSFET at high temperatures[21]. Fig. 40 shows the surface potential of GaN-BTG MOSFET along the channel length at various temperatures and contrasted this to the surface potential of CTG-MOSFET.



(a) (b)

Fig. 39(a) Impact ionization substrate current ($I_{sub,max}$) of CTG MOSFET at different temperatures and (b) Impact ionization substrate current ($I_{sub,max}$) GaN-BTG-MOSFET at different temperatures.

Fig. 40 portrays a higher surface potential for GaN-BTG-MOSFET as contrasted with CTG MOSFET because GaN has an enormous bandgap of 3.1eV concerning silicon 1.1eV, which results in diminished barrier potential which owes to the high conductivity of GaN-BTG MOSFET. Fig. 41 Depicts the electric field of GaN-BTG-MOSFET and contrasted it to that of CTG-MOSFET concerning the channel at various temperatures.

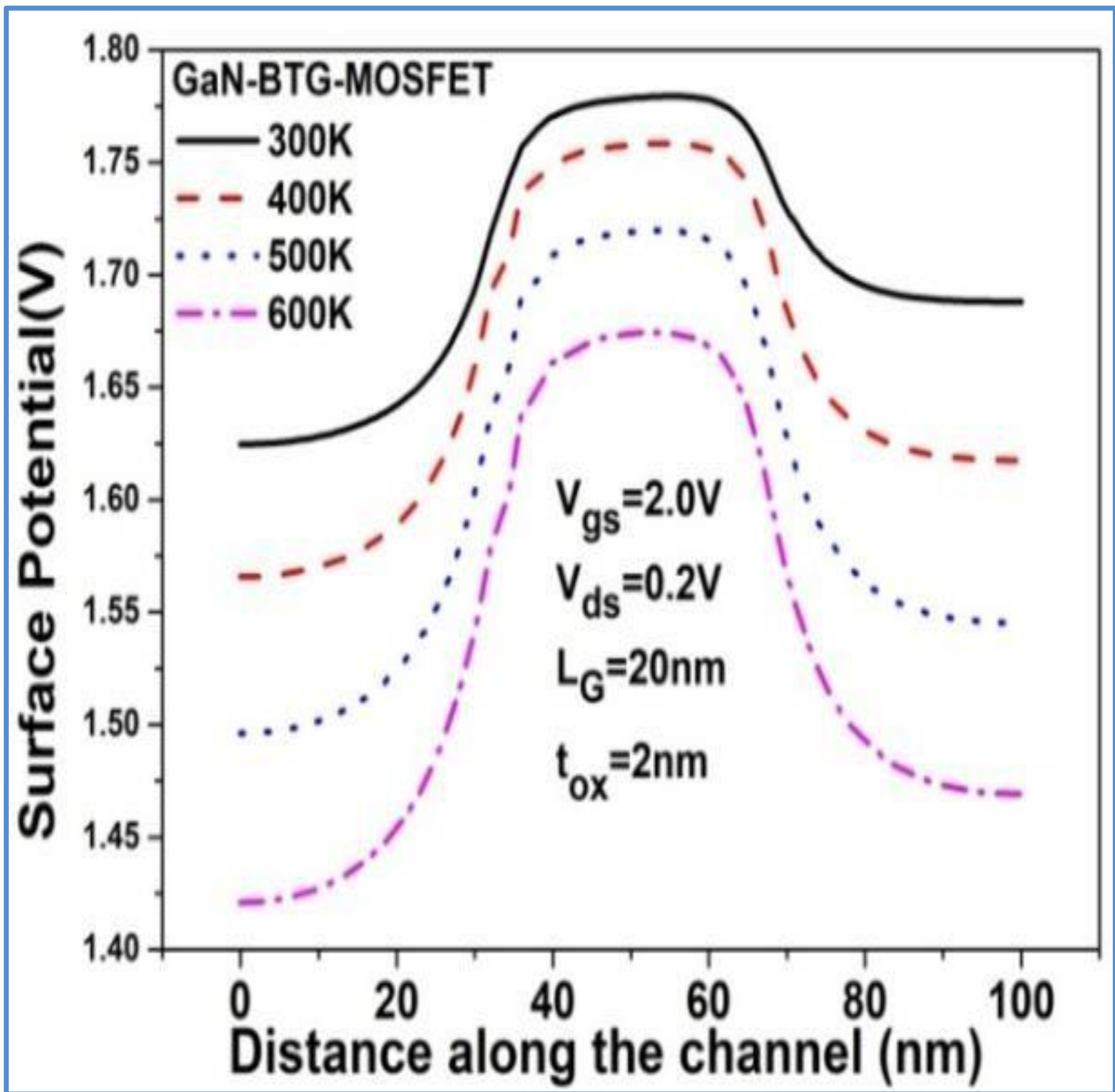


Fig. 40 Surface potential of GaN-BTG MOSFET along the channel at different temperatures

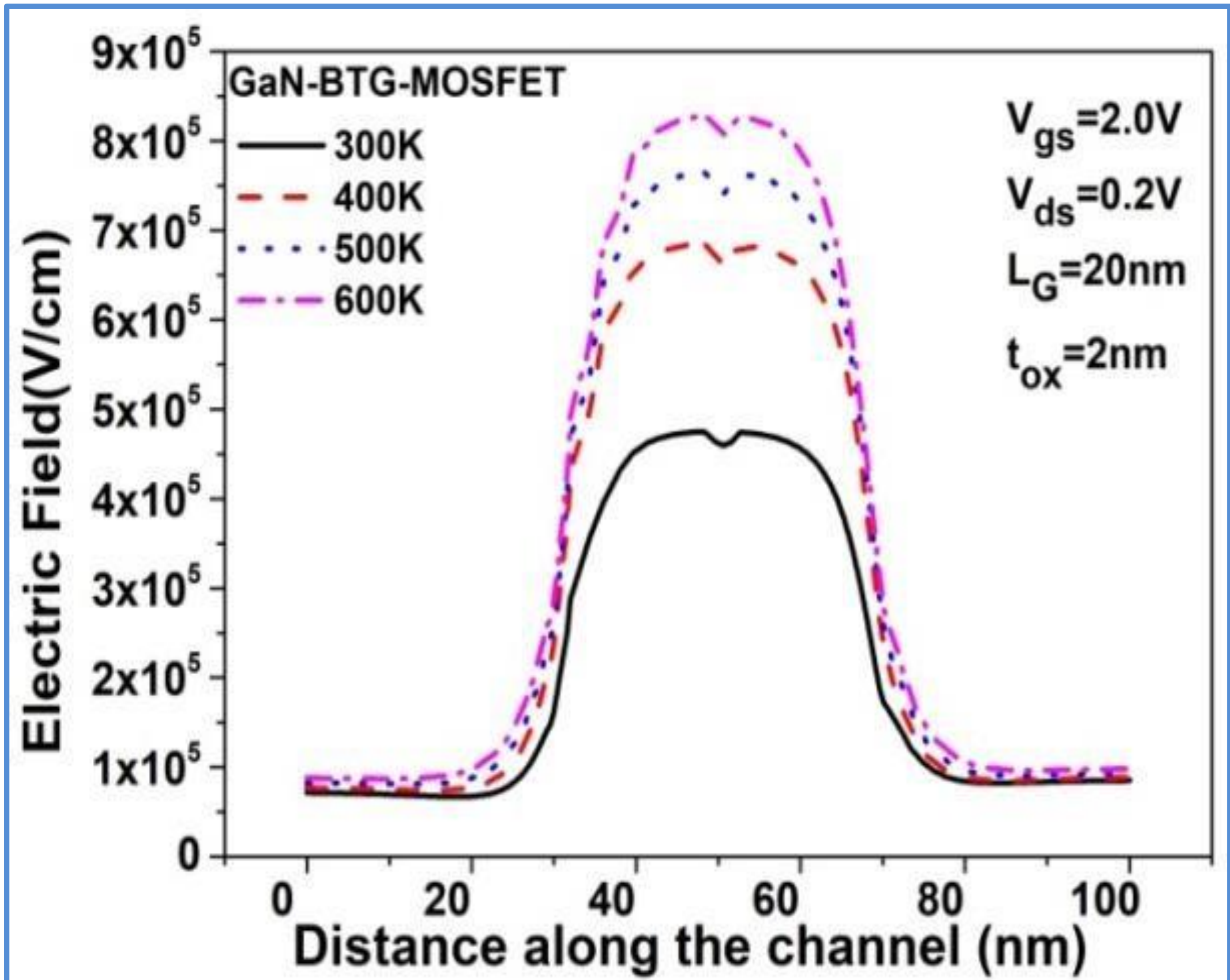


Fig. 41 The electric field of GaN-BTG-MOSFET along the channel at different temperatures.

Electric Field is higher for GaN-BTG-MOSFET than CTG MOSFET at all the temperatures. In view of Higher Electron mobility and higher saturation velocity of GaN. In addition, because of the negligible thermal generation of charge carriers in GaN, GaN-BTG-MOSFET features electric field with increasing temperature, which CTG-MOSFET neglects to depict.

CHAPTER 5

CONCLUSION

This Report features three different devices dissecting the chance of improving the performance of a CTG-MOSFET and also further downsizing its size simultaneously. The electrical characteristics and performance factors of the proposed devices are analyzed and contrasted with that of CTG-MOSFET, and the outcomes are defended utilizing contour plots for all the devices. We see that short channel effects (SCEs) are limited by the presence of the buffer layer and a further improvement in the outcomes was seen on supplanting Silicon with GaN. Additionally, it is seen that the Sub-Threshold slope (SS) has expanded and therefore, the switching time of MOSFET has improved. Moreover, in GaN-BTG-MOSFET lower off-current was observed, resulting in less energy consumption. Further, while analyzing the characteristics of GaN-BTG-MOSFET with differing internal parameters, for example, channel length, doping concentration, and effective oxide thickness (t_{ox}), we saw that with a 62.5% decrement in channel length, channel current reduced by 25%. Likewise, the gate stacking of the oxide layer and buffer layer helps in downsizing the effective oxide thickness to 1nm without trading off with the performance of the proposed device.

It is seen that GaN-BTG-MOSFET shows a steady performance at various temperatures as when contrasted with CTG-MOSFET, which surmises that GaN-BTG-MOSFET is thermally more stable than CTG-MOSFET. Additionally, GaN-BTG-MOSFET is more power-efficient and showcases the possibility of being suggested for high temperature and ceaselessly utilized Integrated Circuits. Additionally, GaN BTG works in the triode and saturation region only when the doping concentration of n-type, and p-type are less than $7x10^{18}$, $5x10^{17}$ respectively. Thus, GaN BTG MOSFET serves as a promising device for lessening short channel effects (SCEs) while giving a chance of further downsizing the size of MOSFET.

BIBLIOGRAPHY

[1] B. Razavi, *Design of analog CMOS integrated circuits*. Tata McGraw-Hill Education, 2002.

[2] A. S. Sedra and K. C. Smith, *Microelectronic circuits: theory and applications*. Oxford University Press, 2013.

[3] J. Appenzeller *et al.*, "Sub-40 nm SOI V-groove n-MOSFETs," vol. 23, no. 2, pp. 100-102, 2002.

[4] B.-Y. Tsui, C.-F. Huang, and C.-H. J. J. o. t. E. S. Lu, "Investigation of molybdenum nitride gate on SiO2 and HfO2 for MOSFET application," vol. 153, no. 3, p. G197, 2006.

[5] K.-S. Im *et al.*, "Normally off GaN MOSFET based on AlGaN/GaN heterostructure with extremely high 2DEG density grown on silicon substrate," vol. 31, no. 3, pp. 192-194, 2010.

[6] J. Leitner, A. Strejc, D. Sedmidubský, and K. J. T. a. Růžička, "High temperature enthalpy and heat capacity of GaN," vol. 401, no. 2, pp. 169-173, 2003.

[7] R. S. Pengelly, S. M. Wood, J. W. Milligan, S. T. Sheppard, W. L. J. I. T. o. M. T. Pribble, and Techniques, "A review of GaN on SiC high electron-mobility power transistors and MMICs," vol. 60, no. 6, pp. 1764-1783, 2012.

[8] T. Cheung, M. J. Butson, K. J. P. i. M. Peter, and Biology, "Effects of temperature variation on MOSFET dosimetry," vol. 49, no. 13, p. N191, 2004.

[9] A. Kumar, M. Tripathi, and R. J. I. T. o. E. D. Chaujar, "Reliability issues of In 2 O 5 Sn gate electrode recessed channel MOSFET: Impact of interface trap charges and temperature," vol. 65, no. 3, pp. 860-866, 2018.

[10] A. Kumar, N. Gupta, and R. J. M. J. Chaujar, "TCAD RF performance investigation of transparent gate recessed channel MOSFET," vol. 49, pp. 36-42, 2016.

[11] C.-W. Lee *et al.*, "High-temperature performance of silicon junctionless MOSFETs," vol. 57, no. 3, pp. 620-625, 2010.

[12] A. Asenov, S. Kaya, and J. H. J. I. T. o. e. d. Davies, "Intrinsic threshold voltage fluctuations in decanano MOSFETs due to local oxide thickness variations," vol. 49, no. 1, pp. 112-119, 2002.

[13] I. J. S. C. Silvaco, CA, Ver, "ATLAS user's manual," vol. 5, 2011.

[14] B. J. Baliga, "Trench gate lateral MOSFET," ed: Google Patents, 1995.

[15] C.-Y. Tsai, T. Wu, and A. J. I. e. d. l. Chin, "High-Performance GaN MOSFET With High-$\kappa $$\hbox {LaAlO} _ {3}/\hbox {SiO} _ {2} $ Gate Dielectric," vol. 33, no. 1, pp. 35-37, 2011.

[16] S. Veeraraghavan and J. G. J. I. T. o. E. D. Fossum, "Short-channel effects in SOI MOSFETs," vol. 36, no. 3, pp. 522-528, 1989.

[17] N. D. Arora, *MOSFET models for VLSI circuit simulation: theory and practice*. Springer Science & Business Media, 2012.

[18] B. Doris *et al.*, "Extreme scaling with ultra-thin Si channel MOSFETs," in *Digest. International Electron Devices Meeting*, 2002, pp. 267-270: IEEE.

[19] A. Kumar, P. M. Tripathi, H. Soni, R. J. I. C. Chaujar, Devices, and Systems, "Numerical Simulation and Parametric Assessment of GaN Buffered Trench Gate MOSFET for Low Power Applications," 2020.

[20] L. Li *et al.*, "Wafer-scale fabrication of recessed-channel PtSe 2 MOSFETs with low contact resistance and improved gate control," vol. 65, no. 10, pp. 4102-4108, 2018.

[21] H. Soni, P. M. Tripathi, M. Tripathi, A. Kumar, and R. Chaujar, "Thermal Reliability of GaN-BTG-MOSFET for High-Performance Applications in Integrated Circuits," in *2020 IEEE 40th International Conference on Electronics and Nanotechnology (ELNANO)*, 2020, pp. 220-223: IEEE.