# DXCCII based Current Mode and Transimpedance Mode Instrumentation Amplifier

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*the requirement for the degree of*

**MASTER OF TECHNOLOGY**

**IN**

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*By*

**Sanjay Singh**

**Roll No.: 2K13/VLS/20**

Under the esteemed Guidance of

**Mr. Deva Nand**

**Assistant Professor,**


**DEPARTMENT OF ELECTRONICS & COMMUNICATION ENGINERRING**

**DELHI TECHNOLOGICAL UNIVERSITY**

**(FORMERLY DELHI COLLEGE OF ENGINEERING)**

**NEW DELHI-110042**

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# *CERTIFICATE*

This is to certify that the thesis entitled "**DXCCII base Current Mode and Transimpedance Mode Instrumentation Amplifier**" has been completed by **Sanjay Singh** in partial fulfillment of the requirement of **Master of Technology** in **VLSI Design and Embedded Systems** and further declare that work done in this thesis has not been published in any conference or in institution and is original and authentic.

**Sanjay Singh**

Roll No.: 2K13/VLS/20

Department of Electronics & Communication

Delhi Technological University

This is a record of his work carried out by him under my supervision and support. He has completed his work with utmost sincerity and diligence.

**Mr. Deva Nand**

**Assistant Professor**

**PROJECT GUIDE**

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**Sanjay Singh**

Roll No.: 2K13/VLS/20

Department of Electronics & Communication

Delhi Technological University

# ABSTRACT

In this thesis, it is shown that the current mode instrumentation amplifier (CMIA) based on second generation current conveyor (CCII) offers benefits over conventional instrumentation amplifier (IA) architectures. A new design of current mode instrumentation amplifier (CM IA) and transimpedance mode instrumentation amplifier (TIM IA) based on Dual X second generation current conveyor (DXCCII) as a building block, has been presented in this thesis. The proposed circuit uses three DXCCII for both current mode instrumentation amplifier as well as transimpedance mode instrumentation amplifier. PSPICE simulation using TSMC 0.35-μm CMOS technology process parameters under voltage supply of ±2.5 V has been used and further simulation results conforms that CMMR has high bandwidth and high gain bandwidth product (GBP) that is independent of gain.

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# LIST OF ABBREVIATIONS & SYMBOLS

| | |
|---|---|
| ASP | Analog Signal Processing |
| BOCCII | Balanced Output Current Conveyor Second Generation |
| BPF | Band Pass Filter |
| BSF | Band Stop Filter |
| BW | Bandwidth |
| CCI | First Generation Current Conveyor |
| CCII | Second Generation Current Conveyor |
| CCIII | Third Generation Current Conveyor |
| CM | Current Mode |
| CMIA | Current Mode Instrumentation Amplifier |
| CMOS | Complementary Metal Oxide Semiconductor |
| CMRR | Common Mode Rejection Ratio |
| DA | Differential Amplifier |
| dB | Decibel |
| DCCII | Differential Current Conveyor Second Generation |
| DDCC | Differential Difference Current Conveyor |
| DDCCTA | Differential Difference Current Conveyor Transconductance Amplifier |
| Dec | Decade |
| DOICCII | Dual Output Inverting Current Conveyor Second Generation |

| | |
|---|---|
| DXCCII | Dual X Current Conveyor Second Generation |
| FDCCII | Fully Differential Second Generation Current Conveyor |
| FD Op-Amp | Fully Differential Operational Amplifier |
| FD OFA | Fully Differential Operational Feedback Amplifier |
| FD OTA | Fully Differential Operational Transconductance Amplifier |
| FD OTRA | Fully Differential Operational Transresistance Amplifier |
| GaAs | Gallium Arsenide |
| GBP | Gain Bandwidth Product |
| HPF | High Pass Filter |
| IA | Instrumentation Amplifier |
| IC | Integrated Circuit |
| LPF | Low Pass Filter |
| MHz | Mega Hertz |
| MIMO | Multiple Input Multiple Outputs |
| MOCCCA | Current Controlled Current Amplifier with Multi Outputs |
| MOCCI | Multiple Output First Generation Current Conveyor |
| MOCCII | Multiple Output Second Generation Current Conveyor |
| MOCCIII | Multiple Output Third Generation Current Conveyor |
| NMOS | N-Channel Metal-Oxide Semiconductor |
| NSD | Noise Spectral Density |
| OFA | Operational Feedback Amplifier |

| | |
|---|---|
| OFCC | Operational Floating Current Conveyor |
| OPAMP | Operational Amplifier |
| OTA | Operational Transconductance Amplifier |
| OTRA | Operational Transresistance Amplifier |
| PMOS | P-Channel metal-Oxide Semiconductor |
| QO | Quadrature Oscillator |
| SIMO | Single Input Multiple Outputs |
| SPICE | Simulation Program with Integrated Circuit Emphasis |
| TAM | Transadmittance Mode |
| TAMIA | Transadmittance Mode Instrumentation Amplifier |
| TIM | Transimpedance Mode |
| TIMIA | Transimpedance Mode Instrumentation Amplifier |
| VM | Voltage Mode |
| VMIA | Voltage Mode Instrumentation Amplifier |
| WB | Wide Band |

# Chapter 1

# Introduction

Analog Circuit Design has become important with the growing opportunities. For designing a circuit, two common modes are available as voltage and current modes. For voltage mode, all state variables appearing in equation defining the circuit should be voltage. Thus, voltage-mode (VM) circuit has signal states that are determined unambiguously and completely by its node voltage. Similarly, current-mode circuit should have currents as state variable. Thus, current-mode (CM) circuit has signal states that are determined unambiguously and completely by its branch currents. Theoretically, one is dual of other [1]. So, it does not make much difference in realizing function in using either mode. Due certain parameters, the characteristics may contradict while using single mode to fulfill all requirement by the user. Thus, it is not possible for all the applications to use only single topology. Further, voltage-mode design offers high-performance supplies and is important contender for bringing attention of designers while designing power supply. Mentioned below are advantages and disadvantages for the user to find best suitable topology, either voltage or current, as per its requirement.

## 1.1 Voltage Mode Circuit

Historically, voltage mode (use of voltage signal for signal processing) topology was used for the operation of circuits. A constant output voltage is driven by the voltage mode circuit as current is allowed to go from zero to full rated current of the supply. Providing required load current, the voltage power supply with constant voltage is executed maintaining constant output

voltage. Clearly, no circuit operates in strictly defined manner. For example, switched-capacitor circuits and charge coupled devices are closer to this pure mode, but more appropriate for these are charge mode circuits. For decades, voltage form is the dominant one for signal representation. Fundamentally, voltage is ratio of energy by charge. The band-gap energy required for $e^-$ for moving from valance band to conduction band in semiconductor as well as charge of electron is a constant. Thus for given technology, voltage has invariant value providing reliable voltage reference.

ADVANTAGES:

- Internal noise voltage determines the AC dynamic range for voltage-mode circuit which are generated by noise currents. The WB NSD depends on biasing and device parameter. Total noise depend on bandwidth and absolute frequency range [2].
- Voltages can easily be measured by instruments and displayed accurately without disturbing circuit elements. Even with finite impedance, compatible circuits can be driven with moderate effect on magnitude. That's why they are of much importance for analog as well as digital designs [2].
- Providing better cross regulation because of low output impedance in case of multiple output supply.
- It is easier to design as well as analyze because of use single feedback loop.

DISADVANTAGES:

- The changes in the first line should be sensed by output supply needs to be corrected using feedback loop which makes circuit slow.

- The requirement of dominant pole or added zero is required for compensation for output of filter which adds two poles in control loop.
- It makes compensation more complicated due to variation of loop gain with input.

## 1.2 Current Mode Circuit

Historically, the processing of signal was done keeping the view of voltage for analog circuits. This is visible as the current signals were first transformed to voltage signals. Taking example of that, the transistor is assembled as voltage circuits considering it better although current outputs are also available. In CMOS logic in inverter style in steady state, at its input negligible current flow which cannot be considered as current signals. The output supply current can be limited and regulated to desired level using current mode. In current mode circuit, constant current is provided irrespective of load voltages. Generally, current mode designs provide high output impedance.

ADVANTAGES:

- Wide bandwidth is the most important benefit using current mode design. The transistors could be used up to $f_T$. Whatever the closed loop gain, bandwidth remains constant in current feedback operational amplifier.
- Shrink in feature size. With lower voltage, process parameters required to be chosen for optimizing digital performance. So, voltage domain will suffer [2].
- Current-mode interfaces, input or output, may be required for some application. In fiber-optics power-measurement system, input should be current from photodiode [2].
- Low power requirement even at high frequency.

- Controlled gain can be achieved without components in feedback.
- Higher speed.
- Dynamic range of signals is high and low switching noise.
- Current summing can be done directly making use of less components providing circuit simplicity.

DISADVANTAGES:

- Higher distortion.
- Higher gain variation.

Also, dual mode topology i.e. circuit can use either current mode or voltage mode one at a time. Thus, after comparing both topologies, we can use either as per our requirement keeping in mind the advantages and disadvantage both.

## 1.3 DIFFERENT BUILDING BLOCKS

Operational amplifiers of various types (Op-Amp, OFA, OTA, COA, OTRA, etc.) and current conveyors (MOCCIs, MOCCIIs, MOCCIIIs, CCIs, CCIIs, CCIIIs) have been reported in [3]. Behavioral models of FD Op-Amp, FD OFA, FD OTA, FD OTRA, FD OFC, FD OCA, DCCIIs, DDCCs, FDCCIIs, DXCCIIs, etc. have been discussed in [4]. BOCCII, DOICCII, FDCCII and DDCC representation by nullor- floating mirror elements have also been reported.

Among these is DXCCII which is a versatile component and has got wide variety of applications as quadrature oscillator [5], band-pass filter for low-Q application [6], four quadrant analog multiplier [7], tunable continuous-time filters [8], three phase sinusoidal oscillator in mixed mode [9], Supplementary Inductance Simulator [10], universal current-mode biquad filter [11], etc.

# Chapter 2

# LITRATURE REVIEW

During the past decades, research on blocks and circuits with CMOS devices have given fruitful results and so many building blocks have been reported which work impressively when they are used in circuits. Further efforts are being made for improvement in CMOS technology enabling integration of more electronic systems in single chip. Current conveyor is among one of very important devices that have been reported using CMOS technology.

An instrumentation amplifier is a differential amplifier having input buffer amplifiers eliminating the need of input impedance matching and suppressing current mode signals (unwanted noise) making suitable for input stage in signal processing systems. It has very low noise, low drift, high open-loop gain, low DC offset, high CMRR and high input impedance.

IAs designed using architecture "Indirect Current-feedback ", then operating range can be extended to -ve power supply and to +ve power supply also. This is useful for systems with single supply as in many cases -ve power of circuit is grounded. Feedback-free IAs has high i/p impedance designed with no external feedback. Thus, it increases bandwidth, reduces noise and number of amplifiers.

It is used where stability and accuracy of circuit being short or long-term both are required. The application of instrumentation amplifier include area of data acquisition systems [12,13], sensor read out integrated circuits [14] and medical instrumentation [15,16].

Conventionally, the op-amp based instrumentation amplifiers was termed voltage mode instrumentation amplifiers whereas current mode (CM) designed blocks based instrumentation amplifiers had been referred as current mode instrumentation amplifiers. The topologies

processing current signals as input and providing voltage output has been referred to as trans-impedance instrumentation amplifiers (TIM IA) while topologies processing voltage signals as input and providing current output has been referred to as trans-admittance instrumentation amplifiers (TAM IA).

In [17], two IAs have been presented, one voltage mode and other transimpedance mode both using two CCII+ and three resistors. The VM provides high input as well as high output impedance while TIM provides low input and high output impedances.

In [18], three different VM IAs have been presented using two, three, and four opamps while using five, seven and six resistors respectively. All the three designs provide high input impedance and low output impedance.

In [19], CMRR for DA has been analyzed using single op-amp and for IA three op-amp. Complete equations have been derived for op-amp with finite differential as well as common mode gain. Theoretical predictions are supported by phase and amplitude measurements. Trimming potentiometer is better from low-tolerance resistors at low frequencies for single op-amp DA as higher CMRR is achievable. 90” phase shift is yielded by DA for CMRR for frequencies greater than 1 kHz which gives advantage when synchronous demodulation used for processing amplitude-modulated signals further. When DA is concentrated along input stage, best CMRR is achievable, but at same time it decreases for frequencies greater than 1 kHz because of reduced CMRR in differential stage for these frequencies.

In [20], simple equation for total CMRR calculation has been provided for cascaded differential amplifier and applied it for instrumentation circuits. Two factors for C and D stage

has shown that CMRR calculated by adding reciprocals of equivalent CMRR in each stage which is defined as product of C factor and product of D factor.

In [21], VM IA has been presented using three opamps and two resistors providing high input impedance and low output impedance.

In [22], high CMRR CCII IA has been produced by techniques of current-mode bootstrapping. Simulation results, taking component mismatch reveals CMRR better than 7OdBs at lOOkHz in case of unity differential gain.

In [23], a modified CMIA topology was proposed and detailed analysis shows its superiority. Proposed circuit easy to construct and simple compared to available IC AD844. The CMRR is maintained without matched resistors. Moreover, high bandwidth and gain both simultaneously can be achieved. Experimental and simulation results given for theoretical conclusion.

In [24], the CMIA in CMOS technology is presented. The circuit uses current differential o/p stage and two positive current CCII. The device shows high CMRR that is gain unaffected for wide range of frequency band. SPICE simulation are also shown.

In [25], a novel current mode instrumentation amplifier configuration based on CCII+ was presented. Advantages over traditional VMIA are matched components not needed for achieving high CMRR and the bandwidth is not GBP limited. Compared with previous CMIAs special advantages being high CMRR, high voltage gain, circuit simplicity, small size, complete circuit symmetry, and very inexpensive price. Further, the circuit has weaker voltage and current error signals due to current feedback technique which makes it better for ICs, much higher CMRR and higher voltage gains. For widening CMRR bandwidth, suggestion was also given. Theoretical

analysis as well as experiments is performed with AD844AN for proving advantages and superiorities showing better attenuation than 60 dB.

In [26], CMIA based on CCII offers advantages over conventional IA architectures. For high CMRR no matched components are required and also bandwidth does not depends on GBP. The matrix representation is extended for include all non-idealities (linear in nature) and thus enhanced CC macro-model derived. Current-mode behavior of CMIA discussed in detail using the macro-model. Furthermore, techniques of CMRR enhancement in CMIA is compared and discussed. The simulated IA gives approximately 44 dB improvement on high-frequency CMRR for 3-dB corner frequency or higher. Further, improvement of IA performance using composite conveyor technique is discussed.

In [27], an enhanced CMIA is presented. Current conveyor op-amp based configuration offers improvement in accuracy when compared with other basic CMIA based on current conveyors only.

In [28], two IAs have been presented one with voltage mode and other with transadmittance mode both using three CCCII. Most importantly, it doesn't uses any passive components. Both mode provides high input as well as high output impedances.

In paper [29], a novel CMIA utilizing OFCC was presented. The OFCC shows flexible properties in comparison with other voltage- or current mode circuits. The advantages are threefold. First, it offers bandwidth independent of gain and high differential gain traditional VMIA. Second, it CMRR is maintained without matched resistors. Third, CMIA circuit shows improved accuracy when compared with other CMIA. CMIA has been experimentally tested,

analyzed, and simulated verifying that proposed CMIA performs better than the existing CMIAs considering the factors as CMRR, differential gain and number of blocks used,.

In [30], CMIA based on CCII offers benefits over conventional IA architectures. Matched components are not needed for achieving high CMRR and the bandwidth is not GBP limited. Therefore, CMOS current conveyor was used. PSPICE simulations shows satisfactory performance for wideband CM signal processing. Furthermore, CMRR enhancement techniques for CMIA are discussed.

In [31], CMIA based on current conveyors second-generation (CCII) presented. Matched components are not needed in achieving high CMRR and also the bandwidth is not limited to GBP. PSPICE simulation shows the performance satisfaction for wideband CM signal processing. CMRR enhancement in CMIA is also discussed. Composite conveyor techniques for improvement of IA performance are given. The simulated IA gives approximately 44 dB improvement on high-frequency CMRR for 3-dB corner frequency. Further, THD of %0.6 is achievable.

In [32], high-performance CMIA circuit is described. It has high gain, CMRR, high accuracy, bandwidth gain-independence and wide bandwidth. Easy implementation is done using commercially available ICs. Experiment shows that CMRR of 120 dB is attainable.

In [33], IA has been designed using two CMOS current-controlled conveyors with active resistor. Thus this design has no passive components, offering high CMRR and wide bandwidth. Gain can be controlled by voltage and current electronically. The simulation of circuit is done using 0.35-μm TSMC CMOS parameters. Theoretical analysis and performance of circuit was confirmed using PSpice simulation results

In [34], low power CMOS IA is presented. It consists of low power op-amp. By optimization and analysis of parasitic effects, IA has better performance. The simulation result shows, amplifier can suppress flicker noise effectively. The IA designed in 0.5μm CMOS parameter technology with 3.3V supply power resulting in dynamic range of 70.1dB and 23.48ns with the settling time within 0.05% accuracy. Power dissipated by main amplifier is 10.5mW including bias circuit dissipating 2.2mW power.

In [35], VM IA has been presented using two CCII and two resistors. This design high input as well as high output impedance.

In [36], a new design of voltage mode IA using five opamps and five resistors has been presented providing high input and low output impedance.

In [37], instrumentation amplifier using current-mode is presented. Signals (input and output) are current signals and also the processing of signals is done completely in current domain. The CMRR of proposed design is determined by five transistors. The proposed circuit is extremely simple. Employing the principal of negative feedback, it exhibits low i/p impedance. Differential-mode gain can be varied electronically by control voltage. This makes it completely resistors free. The low number of transistors grants it properties as suitability for integration, low-voltage, wide bandwidth, low-power operation, etc. SPICE simulation using TSMC 0.18-μm CMOS process parameters under voltage supply of ±0.8 V shows high CMRR (91 dB) and low i/p impedance (291.5). Temperature simulation results also provided proving low temperature sensitivity.

In [38], a new transimpedance mode instrumentation amplifier using three opamps and ten resistors has been presented. It has high input and low output impedance.

In [39] have presented OTRA based instrumentation amplifier working in transimpedance mode (TIM). For transimpedance signal processing, OTRA is a suitable block as it has current input giving voltage output. The designed instrumentation amplifier gives high bandwidth (independent of gain). It also offers high CMRR and high differential gain. Also, the circuit has insensitivity to parasitic input resistance and input capacitance as input terminals are internally grounded in OTRA.

In [40], CM IA using single CFOA along with four resistors has been presented providing high input and low output impedance.

In [41], two generalized IAs topologies have been proposed that can be operated in current, voltage, transimpedance and transadmittance mode. Each topology has structure containing two stages, where in first stage amplifier has been used and in second stage converter has been employed. The difference amplifier makes the second stage in case of both structures. The theoretical result has been verified using OFCC. Non-idealities effect as tracking error, finite transimpedance has been mathematically formulated and analyzed. PSPICE simulation has been used for verification of CMOS-based OFCC. The experimental results of OFCC implementations are in close agreement with simulated as well as theoretical results.

In [42], presents an IA for amplifying current transducer signals providing voltage o/p. It has a high CMRR, gain, gain independent BW. It uses three OFCCs with four resistors. Effect of non-idealities on the performance of proposed TIA is analyzed. Proposed IA has been verified using SPICE simulations. The presented IA is suitable for amplifying current signals as transducer providing voltage o/p.

The summary of the characteristics of available instrumentation amplifiers is given in Table 1.

Table 1: Summary of Characteristics of Available IAs

| Ref. no. | Type of input | Type of output | Active elements used | Resistors/ capacitors used | Input impedance | Output impedance |
|---|---|---|---|---|---|---|
| [17] | voltage | voltage | 2 CCII+ | 3 | high | High |
| [17] | current | voltage | 2 CCII+ | 3 | low | High |
| [18] | voltage | voltage | 2 opamps<br>3 opamps<br>4 opamps | 5<br>7<br>6 | high<br>high<br>high | low<br>low<br>low |
| [19] | voltage | voltage | 3 opamps | 7 , 8 | high | Low |
| [20] | voltage | voltage | 3 opamps | 7 | high | Low |
| [21] | voltage | voltage | 3 opamps | 2, | high | Low |
| [22] | voltage | voltage | 4 opamps | 6 | high | Low |
| [23] | voltage | voltage | 3 CCII+ | 2 | high | High |
| [24] | voltage | voltage | 2 CCII+ | 2 | high | High |
| [25] | voltage | voltage | 2 CCII+ | 2 | high | High |
| [26] | voltage | voltage | 2 CCII+ , 1 opamp | 3 | high | Low |
| [27] | voltage | voltage | 2 CC , 2 opamp | 2 | high | High |
| [28] | voltage | voltage | 3 CCCII | nil | high | High |
| [28] | voltage | current | 3 CCCII | nil | high | High |
| [29] | voltage | voltage | 2 OFCC | 4 | high | High |
| [30] | voltage | voltage | 6 CCII+, 1 opamp | 3 | high | Low |
| [31] | voltage | voltage | 6 CCII+, 1 opamp | 3, 1 capacitor | high | Low |

| | | | | | | |
|---|---|---|---|---|---|---|
| [32] | voltage | voltage | 2 OC | 6 | high | High |
| [33] | voltage | voltage | 2 CCCII | 1 active resistor | high | High |
| [34] | voltage | voltage | 3 opamps | 7 | high | Low |
| [35] | voltage | voltage | 2 CCII | 2 | high | High |
| [36] | voltage | voltage | 5 opamps | 5 | high | Low |
| [37] | current | current | MOS | nil | low | High |
| [38] | current | voltage | 3 opamps | 10 | high | Low |
| [39] | current | voltage | 3 OTRA | 5 | low | Low |
| [40] | current | current | 1 CFOA | 4 | high | Low |
| [41] | voltage | voltage | 4 OFCC | 10 | high | low |
| | voltage | current | 4 OFCC | 9 | high | high |
| | current | currrent | 3 OFCC | 6 | low | high |
| | current | voltage | 3 OFCC | 5 | low | low |
| | voltage | voltage | 3 OFCC | 3 | high | low |
| | voltage | current | 3 OFCC | 4 | high | high |
| | current | currrent | 4 OFCC | 7 | low | high |
| | current | voltage | 4 OFCC | 8 | low | low |
| [42] | current | voltage | 3 OFCC | 4 | low | Low |

# CHAPTER 3

# PROPOSED INSTRUMENTATION AMPLIFIER USING DXCCII

## 3.1 COMPONENT DESCRIPTION

### 3.1.1 CURRENT CONVEYOR

Since the first introduction of current conveyor (CC) by Sedra and Smith [43], it has been very popular and many other devices have been reported on it. It is a three terminal device, an amplifier having unity gain. Current conveyor has three versions (CCI, current conveyor first generation; CCII, current conveyor second generation; and CCIII, current conveyor third generation). It can perform many signal processing operations.

The op-amps suffer from finite GBP limiting its frequency range and accuracy of operation. So, many circuits as voltage mode filters, current-mode filters, and oscillators, rectifiers, simulated inductors, have been designed using CC as current conveyor first-generation (CCI), positive-type current conveyor second-generation (CCII+), negative-type current conveyor second-generation (CCII-), dual output current conveyor second generation (DOCCII), , current conveyor third generation (CCIII), dual differential current conveyor (DXCC), differential voltage current conveyor(DVCC), dual differential current conveyor second generation (DXCCII). Current conveyor has gained attention due to wider bandwidth and capability for voltage as well as current as output. But there is a disadvantage, as there is AD844 IC only that is commercially available in market.

I.A. Awad and A.M. Soliman introduced the inverting current conveyor second generation [44]. Voltage mirror was introduced and with current mirror, represented voltage and current inverting properties of analogue building blocks. Properties of mirror and nullor elements

were used for relating di€ erent devices in ideal case while defining ad joint network for the building blocks. Introduction of two types of current conveyor (CCII) second generation; one is ICCII and the other is ad joint of CCII which was named inverting current conveyor second generation `negative' (ICCII ). They presented CMOS realization of ICCII and also ICCII based current mode designs that were obtained while applying voltage-current mode transformation in CCII based designs. This was the missing elements representing mirroring action of current at output port in CCII while other representing mirroring of voltage. The nullor and mirror element were also used for defining relationship between different building blocks.

### 3.1.2 INTRODUCTION OF DXCCII

For designing continuous time filter, much attention had drawn by CCII after its first introduction [43]. The requirement of tunability for continuous filters for compensating effect of parasitic, aging, temperature, etc., but RC filters based on CCII couldn't achieve this. For overcoming these problems, new device was introduced by A. Zeki and A. Toker called DXCCII [45]. Dual X second generation current conveyor (DXCCII) combines CCII (current conveyor) and ICCII (inverting current conveyor). DXCCII have two X terminal, Xp (non-inverting terminal) and Xn (inverting terminal). The current at Zp and Zn terminal replicates the current at Xp and Xn terminal respectively. There is one more important point that Zp and Zn currents are not co-related. The voltage at terminal Y is generated equally at terminal Xp and inverted at terminal Xn. Using different inputs at DXCCII terminals, we can have different DXCCII application as grounded inductance design, oscillator design, and filter design.

DXCCII has five terminal, characteristic equations in matrix form along with circuit symbol is given below [45]:

$$\begin{bmatrix} I_y \\ V_{xp} \\ V_{xn} \\ I_{zp} \\ I_{zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_y \\ I_{xp} \\ I_{xn} \end{bmatrix}$$

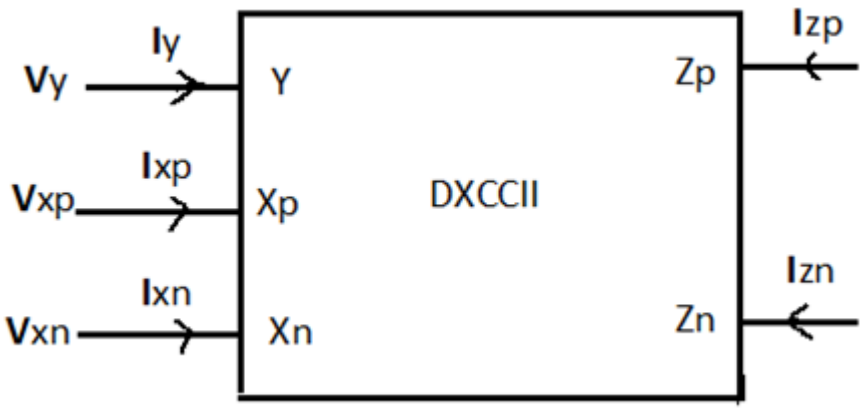


Figure 1: DXCCII Circuit Symbol [45]

### 3.1.3 INTERNAL STRUCTURE OF DXCCII

It has already been mentioned that DXCCII has two current conveyors cascaded together i.e. combining non-inverting with inverting current conveyors. The design of DXCCII using CMOS is shown below figure and this design is used for the application implementation of

current mode (CM) as well as transimpedance mode (TIA) instrumentation amplifiers. Here in below circuit, the properties of DXCCII mentioned above in matrix shows that the current of terminal Xp and Xn should be reflected to terminal Zp and Zn of DXCCII. To fulfill the requirement, two current mirror one non-inverting and one inverting has been used and for making current of terminal Y zero as given in the properties, terminal Y has to be connected to MOSFET's gate terminal as the gate current of MOSFET is almost zero. Also, while observing the design, we can conclude that M13 and M15 transistors have been used additionally for transferring Ixp current to terminal Zp. If the designing of DXCCII is proper then Vds2 could be made almost equal to Vds1 irrespective of the Ixp current and thus elimination of channel length modulation related voltage tracking error is possible.

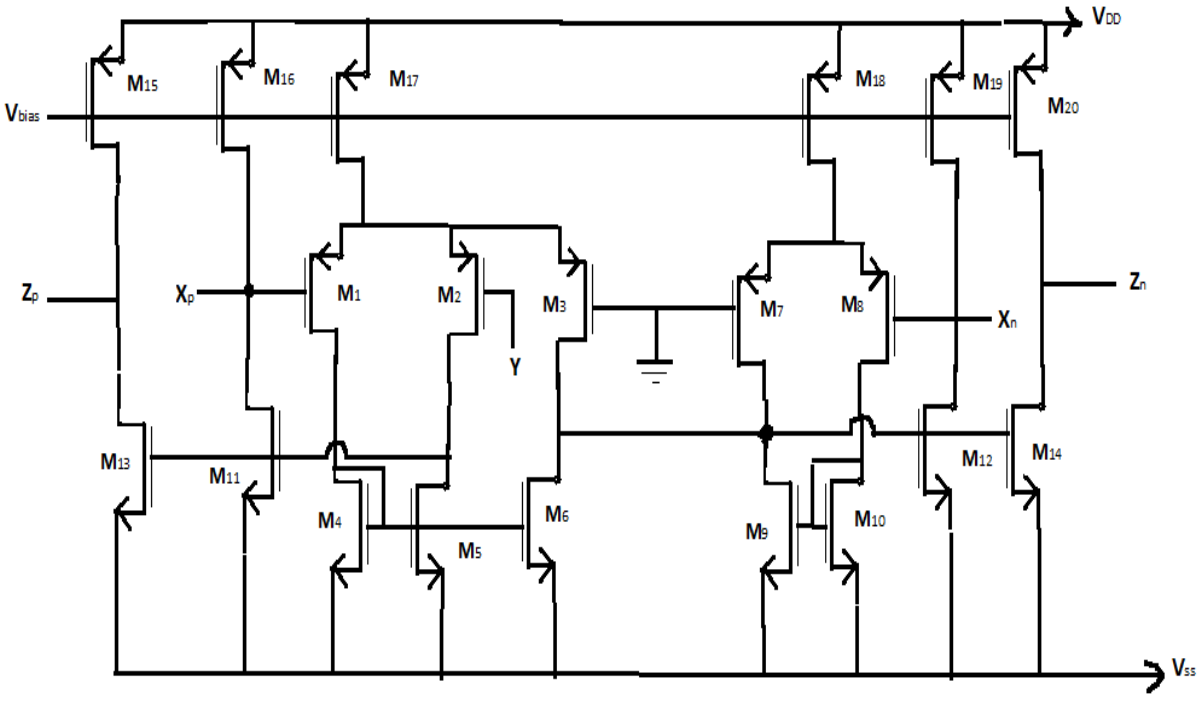


Figure 2: Implementation of DXCCII using CMOS [45]

### 3.1.4 ADVANTAGES OF DXCCII

Current conveyors that are current controlled work only for small input signal as linear device. Using DXCCII, these drawbacks contained in CCCII could be eliminated. The hindrances in the design of circuit for MOSFET C filters for increasing large signal linearity done by using a no. of matching MOSFETs can also be overlooked by the use of DXCCII. The DXCCII provides higher tunability for compensating effect of deviations rising from parasitic, temperature, aging, process tolerance, etc. as in current conveyor efficient tunability would be tough to achieve. Thus DXCCII provides tremendous potential to the designers for realizing a no. of analog signal processing designs including analogue multipliers, continuous time filters, voltage or current controlled oscillator, and amplifiers.

## 3.2 PROPOSED INSTRUMENTATION AMPLIFIER

### 3.2.1 INTRODUCTION

An instrumentation amplifier is a differential amplifier having input buffer amplifiers eliminating the need of input impedance matching and suppressing current mode signals (unwanted noise) making suitable for input stage in signal processing systems. It has very low noise, low drift, high open-loop gain, low DC offset, high CMRR and high input impedance.

In this project two instrumentation amplifiers using two different topologies namely current mode (CM) and transimpedance mode (TIM) have been designed using Dual X second generation current conveyor (DXCCII). Both the circuits take current as input. Common circuit architecture representing both IAs has been used using three DXCCII devices.

Figure 3 shows the generalized block diagram that has been used in designing the two instrumentation amplifiers. The first stage consists of two current amplifiers. The output of the first stages are added together and then fed to the second stage which consists of a current amplifier or current to voltage convertor.

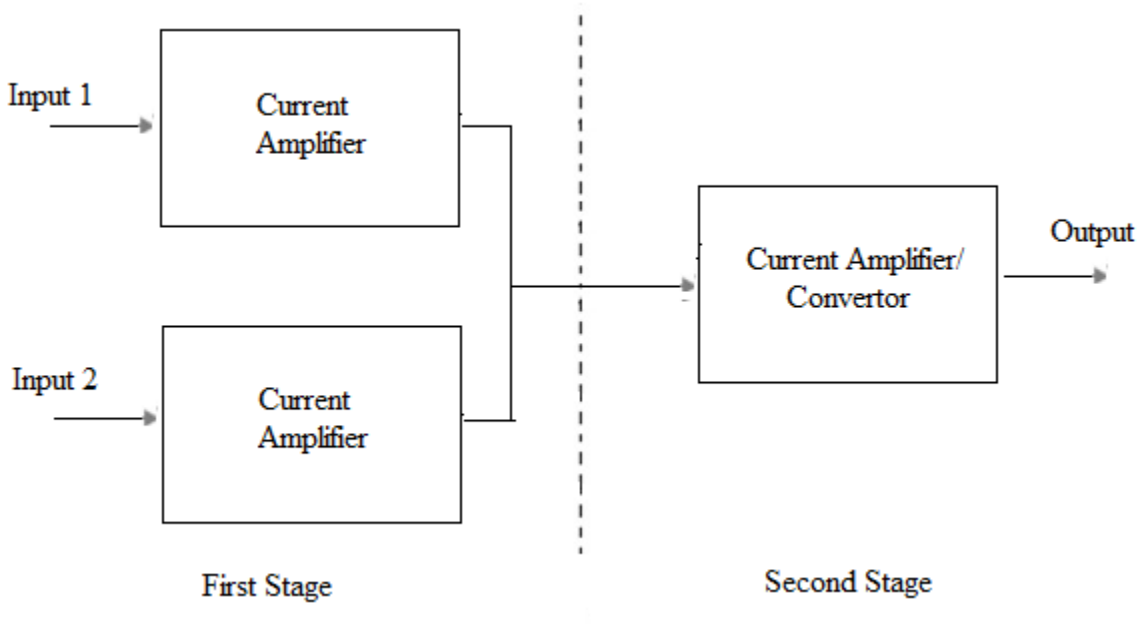


Figure 3: Generalized Block Diagram

### 3.2.2 CURRENT AMPLIFIER

Figure 4 and Figure 5 shows the current amplifier using DXCCII. Iin is the current fed to terminal Y and Iout is the output current taken at terminal Zp.

In Figure 4, the output current Iout is positive and uses two resistors, one is R1 connected to terminal Y and another resistor R2 connected to non-inverting terminal Xp of DXCCII has been used for this design. The terminals Xn and Zn will be kept open.

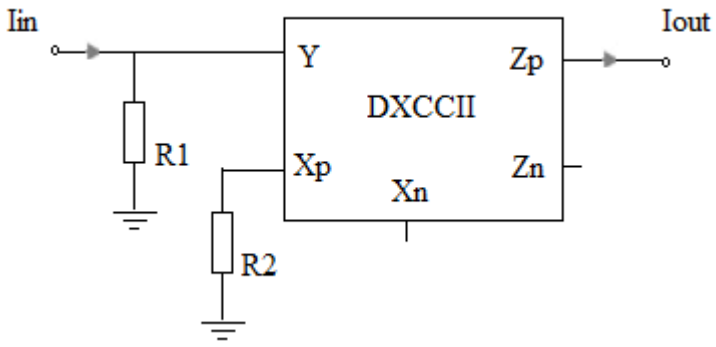


Figure 4: Current Amplifier (Positive Output current)

The equation for finding the current gain is derived from the figure and using characteristic equation as given below::

$$V_y = I_{in} R_1 \tag{1}$$

$$I_{xp} = -\frac{V_{xp}}{R_2} = -\frac{V_y}{R_2} \tag{2}$$

$$I_{out} = -I_{zp} = -I_{xp} = \frac{V_y}{R_2} = \frac{I_{in}R_1}{R_2} \tag{3}$$

Thus, current gain ($A_{CA}$) of the current amplifier (Positive Output current) is

$$A_{CA} = \frac{I_{out}}{I_{in}} = \frac{R_1}{R_2} \tag{4}$$

In Figure 5, the output current Iout is negative and uses two resistors, one is R1 connected to terminal Y and another resistor R2 connected to inverting terminal Xn of DXCCII has been used for this design. The terminals Xp and Zp will be kept open.

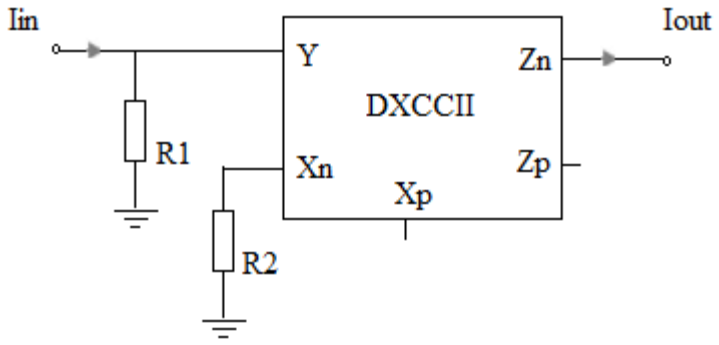


Figure 5: Current Amplifier (Negative Output current)

Here also, the equation for finding the current gain is derived from the figure and using characteristic equation as given below:

$$I_{xn} = -\frac{V_{xn}}{R_2} = \frac{V_y}{R_2} \tag{5}$$

$$I_{out} = -I_{zn} = -I_{xn} = -\frac{V_y}{R_2} \tag{6}$$

Thus, current gain ($A_{CA}$) of the current amplifier (Negative Output current) is

$$A_{CA} = \frac{I_{out}}{I_{in}} = -\frac{R_1}{R_2} \tag{7}$$

### 3.2.3 CURRENT TO VOLTAGE CONVERTOR

In Figure 6, the output is voltage Vout that has been taken across resistor R3 and uses two more resistors, one is R1 connected to terminal Y and another resistor R2 connected to non-inverting terminal Xp of DXCCII has been used for this design. The terminals Xn and Zn will be kept open here also.

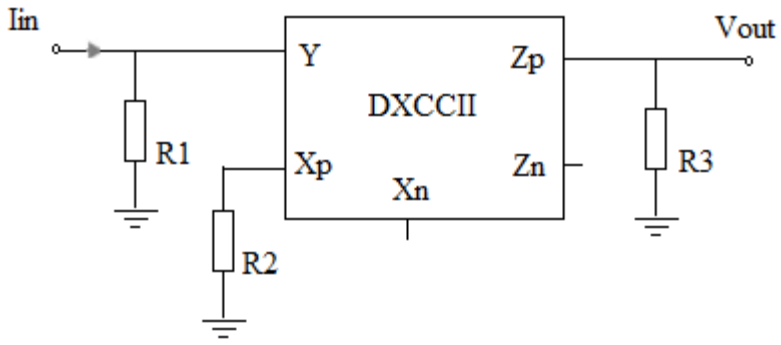


Figure 6: Current to Voltage Convertor

Here, the equations for gain will be found by using characteristic equations as well as above mentioned equation no. (1) and (2) along with equation below:

$$I_{zp} = -\frac{V_{out}}{R_3} \tag{8}$$

The transimpedance gain ($A_{TA}$) is

$$A_{TA} = \frac{V_{out}}{I_{in}} = \frac{R_1 R_3}{R_2} \tag{9}$$

### 3.2.4 CURRENT MODE INSTRUMENTATION AMPLIFIER

The figure 7 shows the instrumentation amplifier opertaing in current mode. The first stage consists of two current amplifiers with different inputs, Iin1 and Iin2 respectively. Both the current amplifiers have same resistors R1 and R2 connected to the terminal Y and non-inverting (inverting) terminal Xp (Xn) of DXCCII-1 (DXCCII-2) respectively to give same gain at their output terminals. The outputs will be taken from terminal Zp of each DXCCII. The terminal Zp of DXCCII-1 gives positive current while the terminal Zp of DXCCII-2 gives negative current. Both the terminals are connected directly to a node which eliminates any further extra

component requirement for taking current difference. The resultant current difference is fed to the second stage current amplifier. The second stage current amplifier has different set of resistors R3 and R4 connected to terminal Y and non-inverting terminal Xp of DXCCII-3 respectively. Iout output current which is the amplified differenced output current of the instrumentation amplifier that is required.

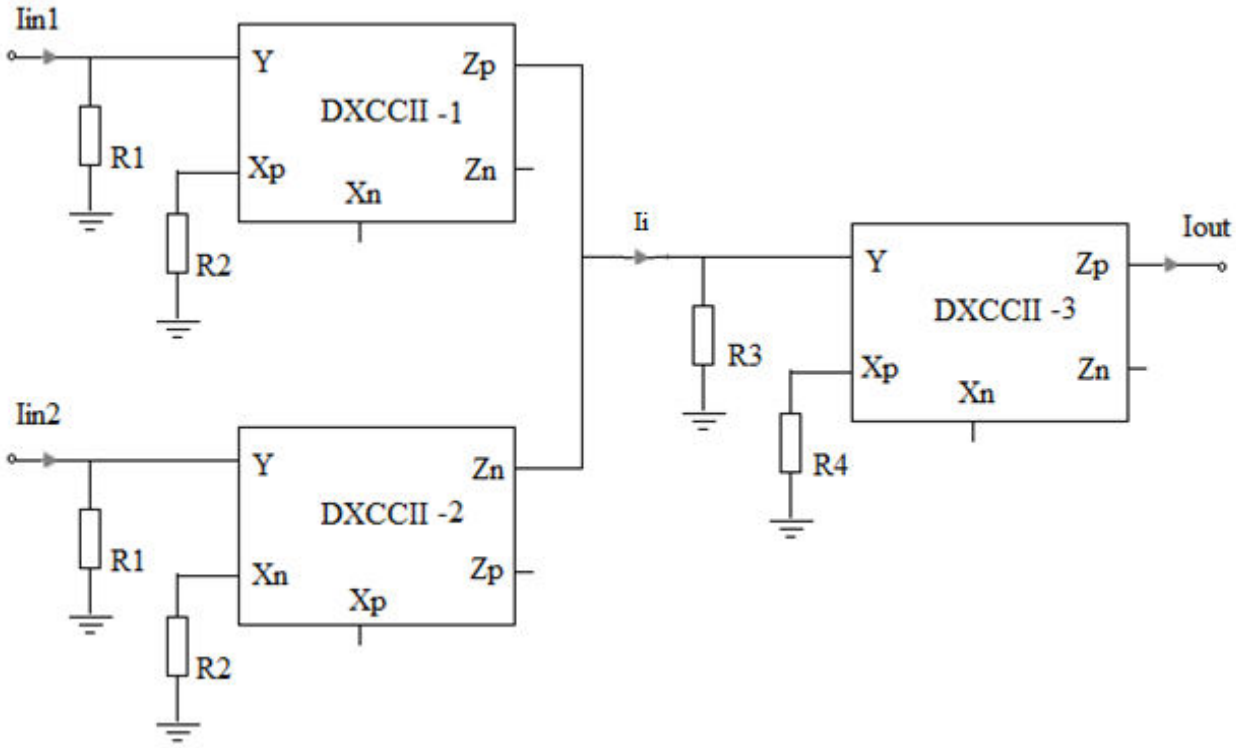


Figure 7: Current Mode Instrumentation Amplifier (CM IA)

The equations for current mode instrumentation amplifier (CM IA) can be found by using characteristic equation along with above equations:

$$I_i = (-I_{zp1}) - (-\mathrm{I}_{zn2}) = \frac{R_1}{R_2}(I_{in1} - I_{in2}) \qquad (10)$$

$$I_{out} = \frac{R_1 R_3}{R_2 R_4}(I_{in1} - I_{in2}) \quad (11)$$

Differential mode gain ($A_{DM}$) of Current Mode Instrumentation Amplifier is

$$A_{DM} = \frac{I_{out}}{(I_{in1} - I_{in2})} = \frac{R_1 R_3}{R_2 R_4} \quad (12)$$

### 3.2.5 TRANSIMPEDANCE MODE INSTRUMENTATION AMPLIFIER

The figure 8 shown below is instrumentation amplifier in transimpedance mode. The first stage is current amplifier while the second stage is current to voltage convertor. The first stage consists of two current amplifiers with different inputs, Iin1 and Iin2 respectively. Both the current amplifiers have same resistors R1 and R2 connected to the terminal Y and non-inverting (inverting) terminal Xp (Xn) of DXCCII-1 (DXCCII-2) respectively to give same gain at their output terminals. The outputs will be taken from terminal Zp of each DXCCII. The terminal Zp of DXCCII-1 gives positive current while the terminal Zp of DXCCII-2 gives negative current. Both the terminals are connected directly to a node which eliminates any further extra component requirement for taking current difference. The resultant current difference is fed to the second stage current amplifier. The second stage current amplifier has different set of resistors R3 and R4 connected to terminal Y and non-inverting terminal Xp of DXCCII-3 respectively. Vout output voltage which is the measured after amplified differenced output current of the instrumentation amplifier that is required.

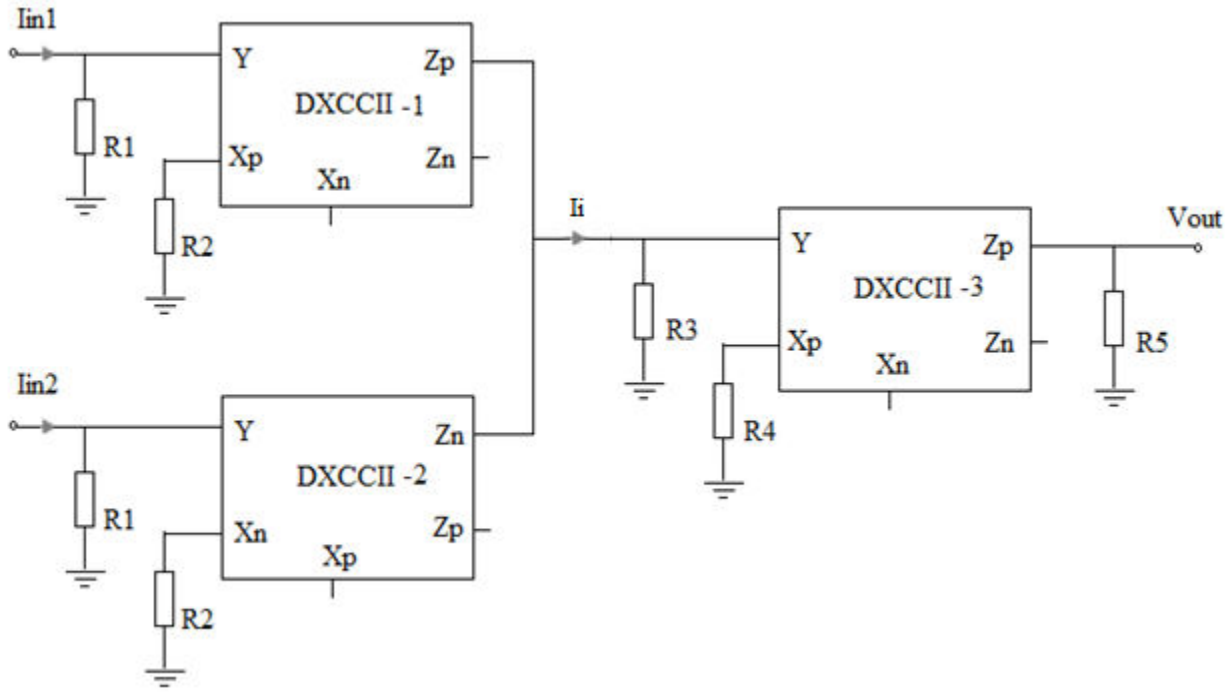


Figure 8: Transimpedance Mode Instrumentation Amplifier (TIM IA)

The equations for transimpedance mode instrumentation amplifier (TIM IA) can be found by using characteristic equation along with above equations:

$$V_{out} = \frac{R_1 R_3 R_5}{R_2 R_4}(I_{in1} - I_{in2}) \quad (13)$$

Differential modegain ($A_{DM}$) of transimpedance instrumentation amplifier,

$$A_{DM} = \frac{V_{out}}{(I_{in1} - I_{in2})} = \frac{R_1 R_3 R_5}{R_2 R_4} \quad (14)$$

### 3.2.6 NON-IDEALITIES

For DXCCII there are two types of non idealities are reported as current transfer gains ($\alpha_p$ and $\alpha_n$) and voltage transfer gains ($\beta_p$ and $\beta_n$). $\alpha_p$ and $\alpha_n$ are called current transfer gains that is from terminals Xp and Xn to terminals Zp and Zn respectively, $\beta_p$ and $\beta_n$ is called voltage

transfer gain that is from input to terminals Xp and Xn respectively. Further, the transfer gains mentioned above are close to unity for a frequency range up to GHz [3].

Taking non idealities into account the port relationships of DXCCII modifies as given in following matrix:

$$\begin{bmatrix} I_y \\ V_{xp} \\ V_{xn} \\ I_{zp} \\ I_{zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ \beta_p & 0 & 0 \\ -\beta_n & 0 & 0 \\ 0 & \alpha_p & 0 \\ 0 & 0 & \alpha_n \end{bmatrix} \begin{bmatrix} V_y \\ I_{xp} \\ I_{xn} \end{bmatrix}$$

Using above mentioned equation, the proposed circuits will be reanalyzed and following are the equations:

Current Gain (Positive Output current),

$$A_{CM} = \frac{I_{out}}{I_{in}} = (\alpha_p \beta_p) \frac{R_1}{R_2} \quad (15)$$

Current Gain (Negative Output current),

$$A_{CM} = \frac{I_{out}}{I_{in}} = -(\alpha_n \beta_n) \frac{R_1}{R_2} \quad (16)$$

Transimpedance Gain,

$$A_{TIM} = \frac{V_{out}}{I_{in}} = (\alpha_p \beta_p) \frac{R_1 R_3}{R_2} \quad (17)$$

Now for current mode instrumentation amplifier, the differential gain can be calculated as below while using above equations:

$$I_i = (\alpha_{p1} \beta_{p1}) \frac{R_1}{R_2} I_{in1} - (\alpha_{n2} \beta_{n2}) \frac{R_1}{R_2} I_{in2} \quad (18)$$

Taking $I_{in1}=I_{in}+ \Delta$ and $I_{in2}=I_{in} - \Delta$, eq. (18) becomes

$$I_i = (\alpha_{p1} \beta_{p1}) \frac{R_1}{R_2} (I_{in} + \Delta) - (\alpha_{n2} \beta_{n2}) \frac{R_1}{R_2} (I_{in} - \Delta) \quad (19)$$

Considering $\alpha=\alpha_{p1}= \alpha_{n2}$ and $\beta=\beta_{p1}=\beta_{n2}$

The differential mode gain of current mode instrumentation amplifier is

$$A_{DM} = \frac{I_{out}}{2\Delta} = \frac{R_1 R_3}{R_2 R_4} (\alpha\beta)^2 \quad (20)$$

Similarly, for transimpedance mode instrumentation amplifier, the differential mode gain can be calculated as:

$$A_{DM} = \frac{I_{out}}{2\Delta} = \frac{R_1 R_3 R_5}{R_2 R_4} (\alpha\beta)^2 \quad (21)$$

# Chapter 4

# Simulation Result

## 4.1 Introduction:

This chapter contains different proposed instrumentation amplifier in current mode (CM) and transimpedance mode (TIM) design simulations that have been carried out using PSPICE software while making use of 0.35µm modal parameters for n-well CMOS.

For designing DXCCII, supply voltage of basic device has been kept at 2.5 V and -0.5 mV value has been maintained for bias voltage. Using current at input as source, we have designed current in mode (CM) and transimpedance mode (TIM) instrumentation amplifiers. The CMOS structure of DXCCII is shown in figure 9.

The aspect ratio used for MOSFETs are given in Table 2 as shown below:

Table 2: (W/L) Ratio of CMOS used [45]

| Transistor | W(µm) | L(µm) |
|---|---|---|
| $2M_{1-2,}\ M_{3,7-8}$ | 6 | 1.5 |
| $4M_{4-5},\ 2M_{6,9-10,}\ M_{11-14},\ M_{15-20}$ | 20 | 1.5 |

0.35um model parameter has been used for implementing DXCCII on PSpice for n-well CMOS process.

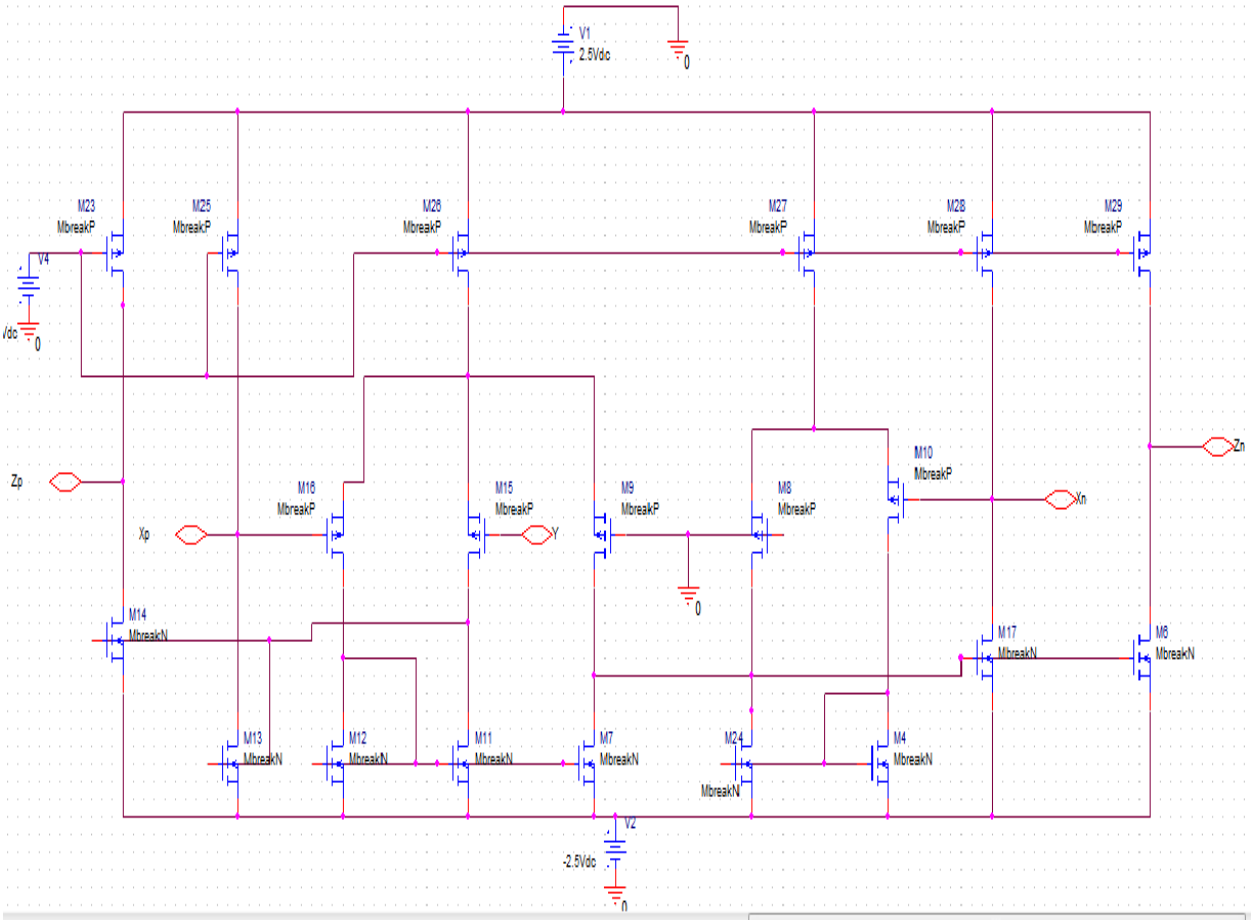


Figure 9: Implementation of DXCCII using CMOS on PSpice

## 4.2 CHARACTERISTICS OF DXCCII

Various characteristics of DXCCII have been verified using PSPICE design. These characteristics include voltage at terminal Y (Vy) vs. voltage at non-inverting terminal (Vxp) in figure 10, voltage at terminal Y (Vy) vs. voltage at inverting terminal (-Vxn) in figure 11, current at non-inverting terminal (Ixp) vs. current at terminal Zp (Izp) in figure 12and current at inverting terminal (Ixn) vs. current at terminal Zn (Izn) in figure 13. These characteristics are shown in figures :

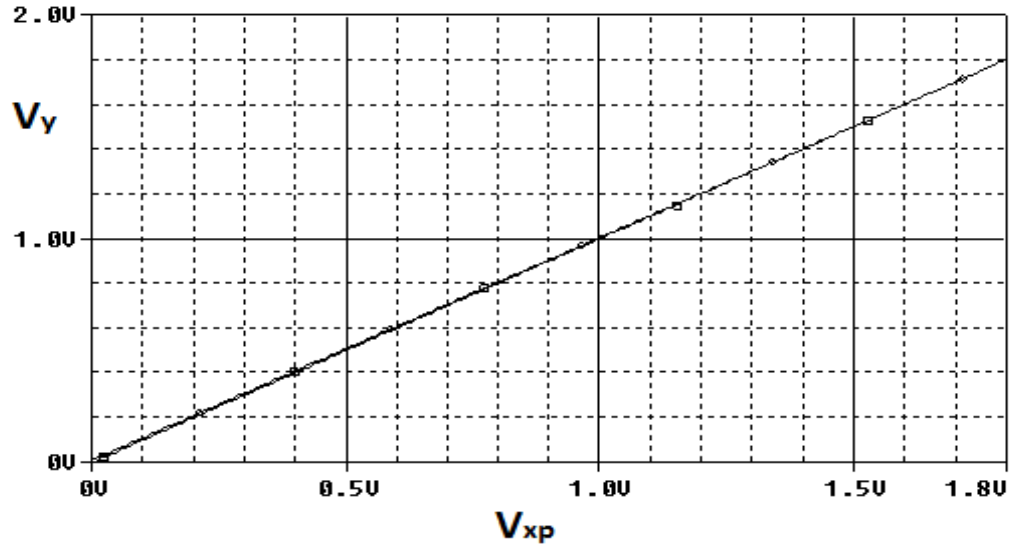


Figure 10: Voltage Relationship

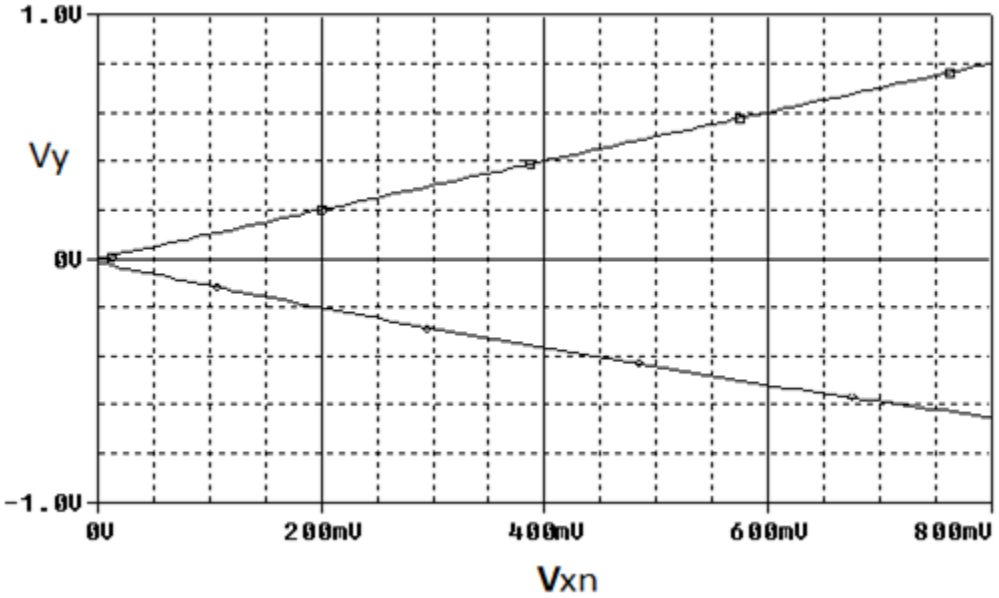


Figure 11: Inverting Voltage Relationship

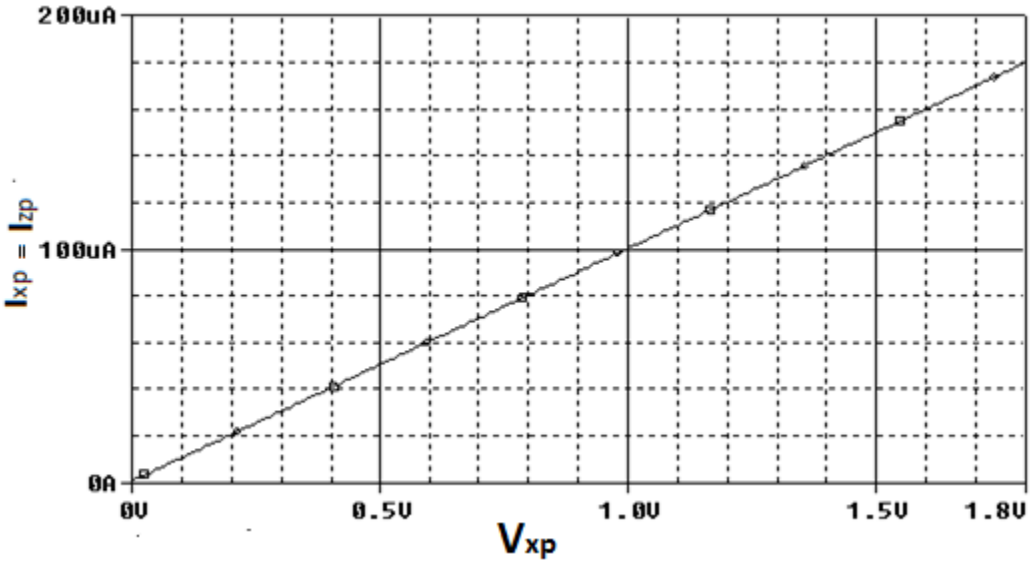


Figure 12: Current Relationship of Terminal Xp & Zp

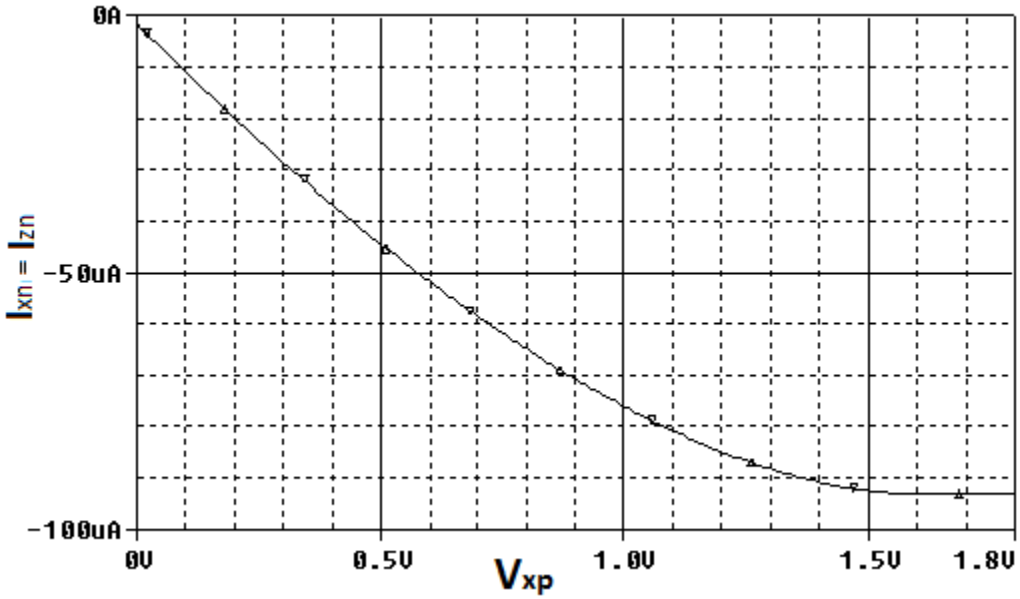


Figure 13: Current Relationship of Terminal Xn & Zn

## 4.3 PSPICE CIRCUITS & RESPONSES

The circuits have been made in PSPICE for analysis. The circuits and their responses (differential mode gain and CMRR graphs) are given below.

The main block of both current mode and transimpedance mode instrumentation amplifier have three DXCCII in two stages. The first stage consists of positive and negative current amplifier shown in figure 14 and figure 15 respectively and gives positive and negative current at its output respectively. The proposed IA is shown in figure 16 using three DXCCII and seven resistors.

The differential gain plot of current mode and transimpedance mode instrumentation amplifier is shown in figure 17 and figure 19 respectively.

The CMRR plot for both proposed design is found to be same and plotted in figure 18 and figure 19 for current mode and transimpedance mode respectively.

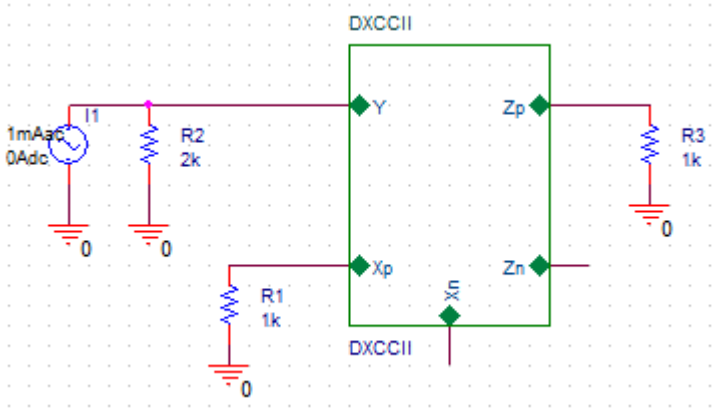


Figure 14: Positive Current Amplifier

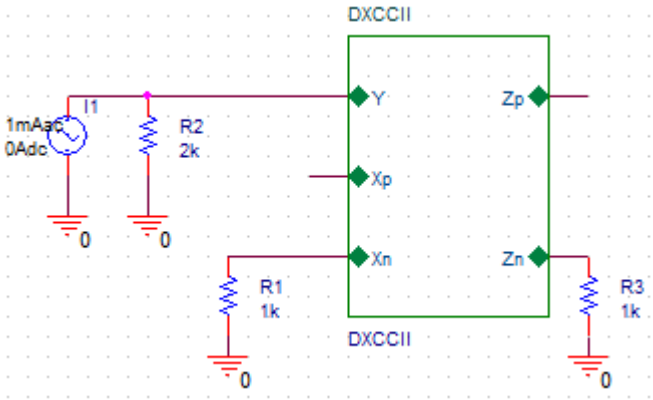


Figure 15: Negative Current Amplifier

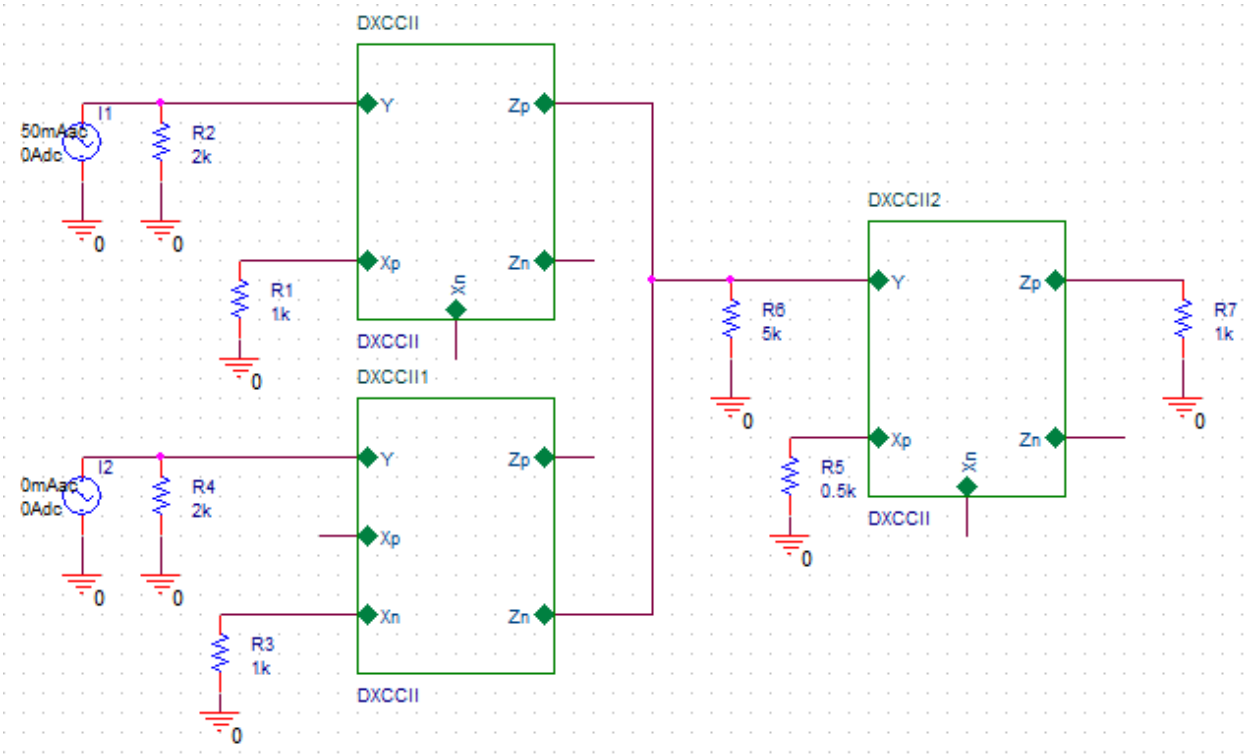


Figure 16: Current/Transimpedance Mode Instrumentation Amplifier

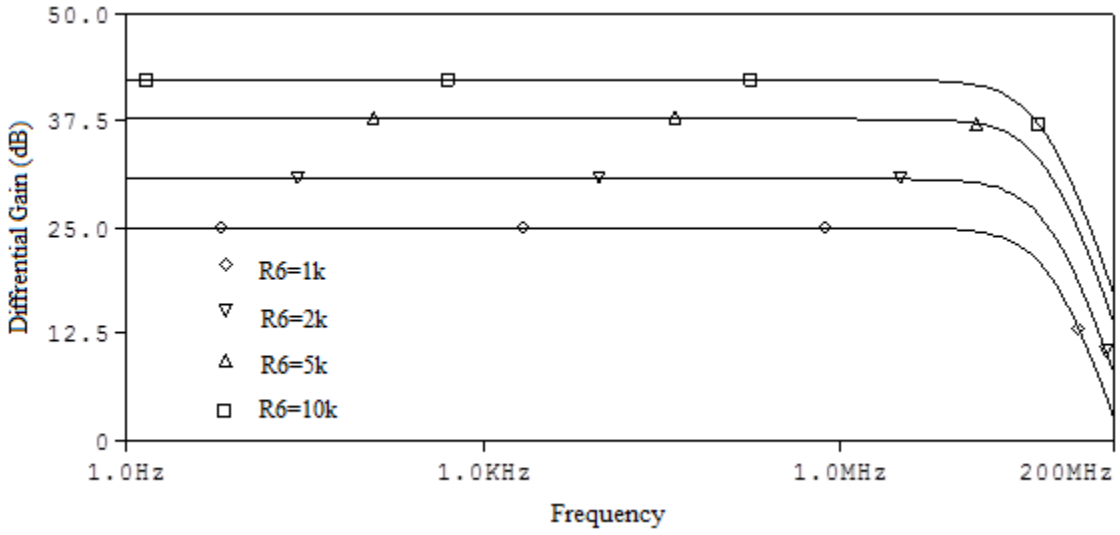


Figure 17: Differential Gain of Current Mode Instrumentation Amplifier

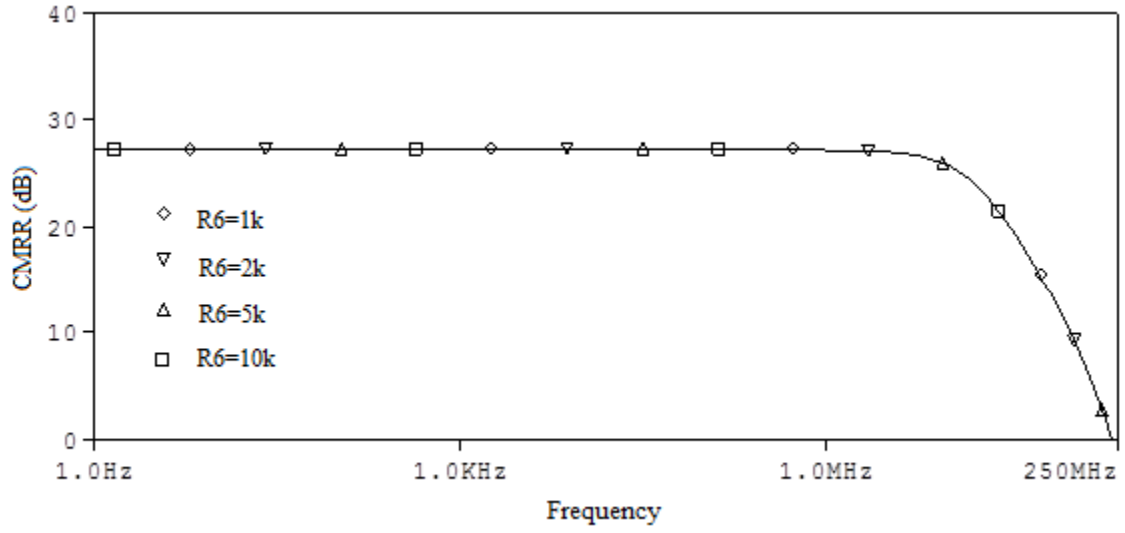


Figure 18: CMRR of Current Mode Instrumentation Amplifier

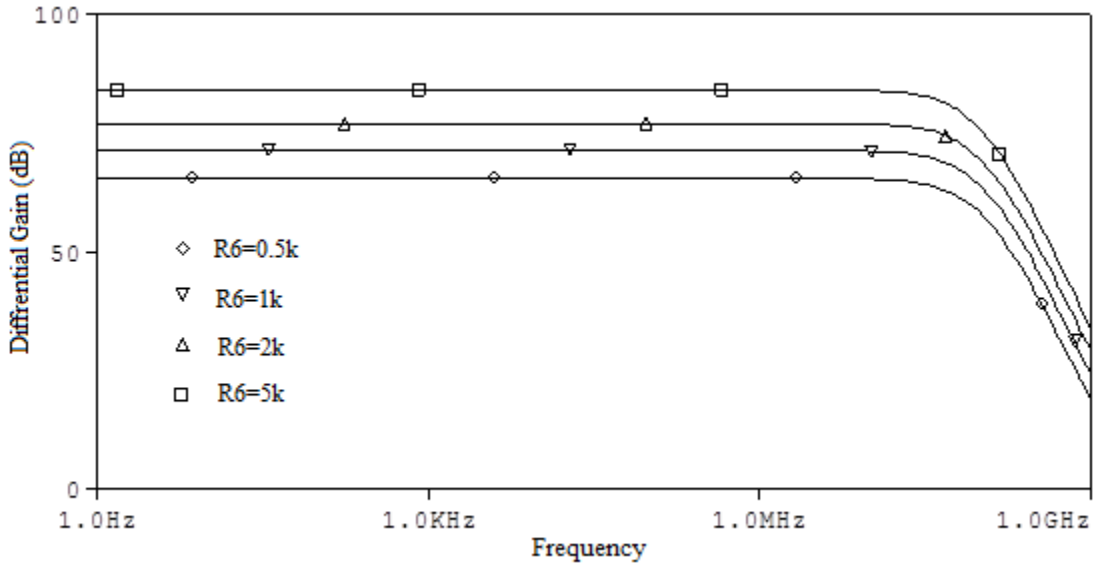


Figure 19: Differential Gain of Transimpedance Mode Instrumentation Amplifier

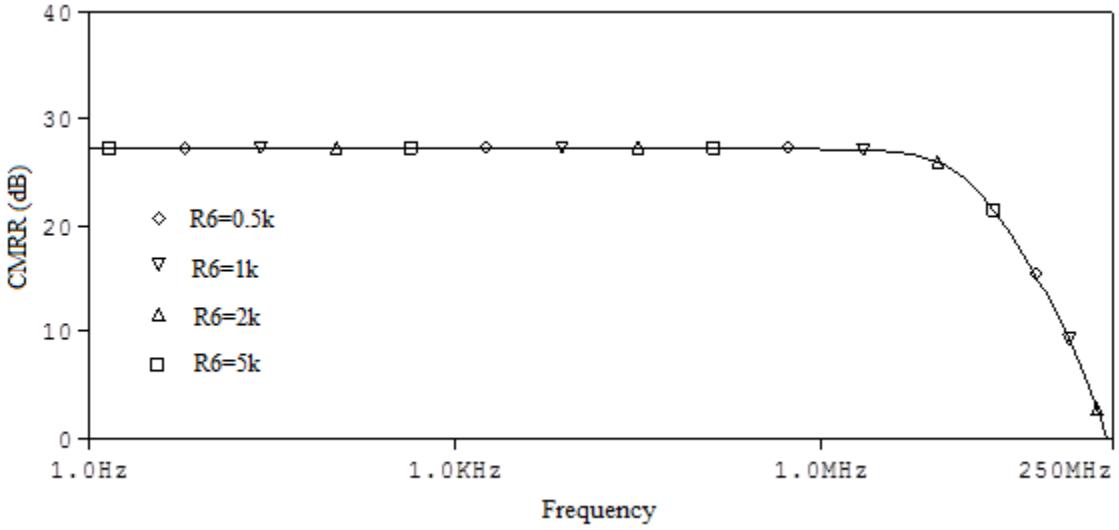


Figure 20: CMRR of Transimpedance Mode Instrumentation Amplifier

## 4.4 SIMULATION RESULTS

The CMRR for both the proposed designs are same and was found to be 27.211dB. This may not be large as desired but the -3dB bandwidth is found to be very large as not reported earlier in any circuits and found to be 15.9 MHz. The GBP for CMRR is found to be 365.1 MHz. Also most importantly, the CMRR and its -3dB bandwidth are found to be independent of any resistors. The power dissipated by CM/TIM IA are also same and found to be 0.123 W.

The differential gain for current mode instrumentation amplifier has been plotted for resistor values $R_1$=2 kΩ; $R_2$=1 kΩ; $R_3$=1 kΩ,2 kΩ,5 kΩ,10 kΩ; $R_4$=0.5 kΩ; $R_5$=1 kΩ and for transimpedance mode instrumentation amplifier has been plotted for resistor values $R_1$=2 kΩ; $R_2$=1 kΩ; $R_3$=0.5 kΩ,1 kΩ,2 kΩ,5 kΩ; $R_4$=0.5 kΩ; $R_5$=1 kΩ. The gain has been found to be constant for a very large frequency range.

Also, the values for the resistors $R_2$, $R_4$, and $R_5$ should be chosen carefully so as to optimize the circuit output in terms of gain and bandwidth. As $R_2$ and $R_4$ increases, gain decreases and bandwidth increases while in case of $R_5$ bandwidth first decreases and then increases slightly. The optimum values for $R_2$ and $R_4$ are found to be from 0.5 kΩ to 1 kΩ and for $R_5$ to be from 0.1 kΩ to 1 kΩ.

The summary of simulation has been tabulated as given below in Table 3 and for better comparison of performance parameters in existing and available CM IAs & TIM IAs are shown in Table 4:

Table 3: Summary of Simulation Results

| TOPOLOGY | Resistor Value (kΩ) | Diffrential Mode Gain (dB) | CMRR (dB) | Input Value | CMRR BW (MHz) |
|---|---|---|---|---|---|
| Current Mode Instrumentation Amplifier | $R_1$=2; R2=1; $R_3$=1,2,5,10; $R_4$=0.5; $R_5$=1 | 25.1, 30.8, 37.7, 42.3 | 27.211 | 25mA | 15.9 |
| Transimpedance Mode Instrumentation Amplifier | $R_1$=2; R2=1; $R_3$=0.5,1,2,5; $R_4$=0.5; $R_5$=1 | 65.5, 71.3, 77, 84 | 27.211 | 25mA | 15.9 |

Table 4: Performance Parameters of Available CM & TIM IAs

| Ref. No. | Mode | CMRR, dB | -3 dB freq., CMRR | Power Supply, V | Power Consumption, max., mW |
|---|---|---|---|---|---|
| [17] | TIM | 100 | NA | NA | NA |
| [37] | CM | 91 | NA | ±0.8 | 0.446 |
| [38] | TIM | NA | NA | NA | NA |
| [39] | TIM | 64.5 | 10 KHz | ±1.5 | 4.93 |
| [40] | CM | 48 | NA | ±1 | NA |
| [41] | CM | 55 | 349 KHz | ±1.5 | 5.04 |
| | TIM | 55 | 352 KHz | ±1.5 | 3.6 |
| | CM | 85 | 32 KHz | ±1.5 | 3.99 |
| | TIM | 85 | 32 KHz | ±1.5 | 8.33 |
| [42] | TIM | 75 | 112 KHz | ±1.5 | 1.5 |
| Proposed | CM | 27.211 | 15.9 MHz | ±2.5 | 0.123 |
| Proposed | TIM | 27.211 | 15.9 MHz | ±2.6 | 0.123 |

# Chapter 5

# CONCLUSION

In this thesis, current mode instrumentation amplifier and transimpedance mode instrumentation amplifier based on DXCCII has been presented. Both the circuits, current mode IA and transimpedance mode IA, use only three DXCCII and seven resistors. Although CMRR is less but it has high -3 dB bandwidth that has not been reported earlier and also the bandwidth is independent of any resistors as well as gain. Further, the differential gain is sufficiently high. The effect of non-idealities has also been presented. Also, the PMOS transistors $M_{1\text{-}3}$ & $_{M7\text{-}8}$ bulk source sorting can be done in single n-well technology. Thus elimination of body effects related voltage tracking error can be done.

In future, more IAs with different design can be made and with the advancement of technology, the characteristics like chip area, power consumed and delay time in addition with supply will be reduced making performance characteristics much better.

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