Filter applications using Dual mode DXCCII

A dissertation submitted in partial fulfilment of

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MASTER OF TECHNOLOGY

IN

VLSI Design and Embedded Systems

by

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CERTIFICATE

This is to certify that the thesis entitled "**Filter applications using dual mode DXCCII**" has been completed by **Rahul Kumar Prawal** in partial fulfilment of the requirement of **Master in Technology** in **VLSI Design and Embedded Systems**. This is a record of his work carried out by him under my supervision and support. He has completed his work with utmost sincerity and diligence.

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PROJECT GUIDE

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ABSTRACT

From the last two decades there has been a revolutionary change in the use of CMOS technology is a popular choice to implement filters, multipliers, oscillators, and several other important building blocks for many applications.

In the field of electric and electronic engineering, filters play an important role and have been widely applied in various aspects such as communications systems, instrumentation, measurement and signal processing, etc. In this present thesis three filters have been designed using both current and voltage mode.

The Voltage-mode filter follow the voltage at the load which is driven by a voltage supply ,in the same way current mode filters execute with the condition of current as a source for the working of filter. When a user get both the modes available to him then any mode can be used as per requirement of the user eliminating the drawbacks of the other mode.

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LIST OF ABBREVIATIONS &SYMBOLS

ASP	Analog Signal Processing
BPF	Band Pass Filter
BSF	Band Stop Filter
BW	Bandwidth
CM	Current Mode
VM	Voltage mode
CMOS	Complementary metal-oxide semiconductor
CMRR	Common-mode rejection ratio
CO	Condition of Oscillation
dB	Decibel
Dec	Decade
FC	Folded Cascade
FO	Frequency of Oscillation
GaAs	Gallium arsenide
HPF	High Pass Filter
Hz	Hertz
IC	Integrated Circuit
LPF	Low Pass Filter
MHz	Mega Hertz
MIMO	Multiple input multiple outputs
NMOS	N-Channel metal-Oxide Semiconductor

OPAMP	Operational amplifier
OTA	Operational transconductance amplifier
PMOS	P-Channel metal-Oxide Semiconductor
QO	Quadrature Oscillator
RFIC's	RF integrated circuits
SIMO	Single input multiple outputs
SoC	System on chip
SoI	Silicon on Insulator
SPICE	Simulation Program with Integrated Circuit Emphasis
THD	Total Harmonic Distortion
VCCS	Voltage controlled current source
VCVS	Voltage controlled Voltage source
A or G	Gain
C	Capacitance
Cox	Gate oxide capacitance per unit area
F	Frequency in Hertz
g_m	Transconductance
ID	Drain Current
L	Inductance or gate length
Q	Q factor
R	Resistance

T	Temperature in Kelvin
μ	Permeability
VCM	Common Mode Input Voltage
VDD	Positive supply voltage
VGS	Gate-Source Voltage
Vin	Input Voltage
Vo	Output Voltage
VSS	Negative supply voltage
VTh	Threshold voltage
Ωo	Output pole frequency
W	Gate Width
Y	Admittance

Chapter 1: Introduction

There are commonly known two modes available for working of any circuit namely voltage mode and current mode. Ideally one single mode can't fulfill all the requirements of the user at the same time because sometimes their characterstic contradict with each other for certain parameters. Thus the truth is that no single topology can be used for all applications. Moreover, voltage-mode control has much to offer designers of today's high-performance supplies and is a viable contender for the power supply designer's attention. One must have knowledge of both advantages and disadvantages of both topologies so that appropriate topology can be used as per the requirements. So some advantages and disadvantages of both the topologies have been presented here so that user can find which topology is best suitable as per his requirement.

1.1 Voltage Mode Control

Voltage mode is one of the two controlling conditions that regulate the output of the supply as per the input available to it. Most of the applications use voltage as a supply i.e. voltage mode topology for the operation of circuits. A constant output voltage is driven by the voltage mode circuit as current is allowed to go from zero to full rated current of the supply. In all these applications the power supply is executed in the voltage mode which maintains a constant output voltage by providing required current to the load. A voltage mode circuit generally provides low output impedance. The advantages of voltage-mode control are:

- As in voltage mode single feedback loop is used which is easier to design and analyze.
- In the voltage mode as output is low impedance so it provides better cross regulation for multiple output supplies

Voltage-mode's disadvantages can be listed as:

- Any change in line first needs to be sensed by output supply then corrected by using feedback loop which makes the response of voltage mode circuit slow.
- The output filter adds two poles to the control loop which require either a dominant pool or an added zero for compensation purpose.
- Compensation becomes more complicated as we know that loop gain varies with input voltage.

1.2 Current Mode Control

The disadvantages of voltage mode are very significant in circuit design and since they all can be eliminated using current mode topology so the designers are very much motivated using current mode topology as it came into picture. Current mode circuit limits and regulates the output current supply to the desired level. Current mode circuit's supply provides a constant current to the different load voltages. Current mode circuit generally provides a high output impedance of the supply. There are some advantages of current mode circuits over voltage mode circuits as follows:

- It works on higher speed as compare to voltage mode circuits
- It consumes low power at high frequencies.
- It provides high signal dynamic range with low cross talk and switching noise.
- It gives edge on voltage mode circuit as it provides controlled gain without feedback components.
- It does current summing without components as well as having schematic simplicity.

- These are well suited for low voltage applications, can work as a pseudoconductance networks, and can be used in current switching techniques.
- It can work in submicron technology more efficiently that are mostly used in digital circuits.

Some disadvantages of current mode circuits are as follows:

- Current mode circuit is having higher distortion as compare to voltage mode circuit.
- Current mode circuit yield higher gain variation as compare to voltage mode circuit.

Thus we can compare both the topologies as per their advantages and disadvantages and can use accordingly the topology which is most suitable as per our requirement.

1.3 Proposed Dual mode circuit

This project proposes a dual mode topology that is the proposed circuit can be used as a current mode circuit as well as voltage mode circuit using one topology at a time. With the use of this kind of topology designer can use any one of these two topology keeping in mind his specific requirement. Three kind of filter that is low pass filter, band pass filter and high pass filter using both modes individually at a time are verified here in this project.

Device used in this project is dual X current conveyor for both current mode and voltage mode. All the basic properties of DXCCII has been verified in the

proposed circuit. Then using this device a second order low pass ,band pass and high pass filter has been presented here in this project.

All low, medium and high frequency response of all the three filters has been verified that is proposed circuit is working perfectly for all low, medium and high frequencies. For the resistance, capacitance and temperature parameter sweeping has been verified. Transient response for the band pass filter has been verified along with fast fourier transform of inputs and outputs.

Total harmonic distortion for both voltage mode and current mode circuit has been checked. Sensitivities of the circuit for both current mode as well as voltage mode has been found out.

In the end the proposed circuit has been compared with the related reference papers used here in this dual mode topology. All the different characterstics of the papers has been compared to notify what is new in this proposed project.

1.4 Thesis structure

Chapter1: Basic introduction of current mode and voltage mode topology including their advantages and disadvantages, and advantage of dual mode topology over both these.

Chapter2: Introduction of the device used for the design of dual mode circuit used in this project.

Chapter3: Different filter topologies using DXCCII

Chapter4: simulation results for all filters designed using DXCCII

Chapter5: conclusion and future scope

Chapter2 : literature Review

2.1 Current Conveyor

During the last three decades, research work using CMOS devices has been very fruitful and so many new devices has been invented which work as a tremendous devices when it comes to utilization of these devices. Continuous efforts were made to improve CMOS technology and enabled the integration of (largely digital) complete electronic systems on a single chip. Current conveyor is also one of the devices designed using CMOS technology.

Current conveyor was first introduced by Sedra and Smith in 1968. Current conveyor generally is known as three terminal analog electronic devices.
It is a kind of electronic amplifier with gain of unity. Ideally current conveyor is available in three versions i.e. CCI,CCII and CCIII (current conveyor first, second and third generation). Current conveyor can perform so many analog signal processing operations similar to op-amp.

2.2 Introduction of DXCCII

For the design of continuous time filters CCII has received so much attention as it was introduced by Sedra and Smith in 1970. There is a requirement of tunability in the design of continuous time filters so as to compensate the effect of process tolerances, temperature, parasitics, aging, etc. but CCII based RC filter can not achieve efficient tunability. Dual X current conveyor is a device which is combination of current conveyor (CCII) and inverting current conveyor (ICCII).
It has two X terminals known as Xp and Xn where Xp is the non inverting terminal and Xn is the inverting terminal. The current at the terminals of Zp and Zn is the replica of the currents at the terminals of Xp and Xn. The voltage generated at the

Y terminal is equal to the voltage value at Xp terminal and this Y terminal voltage is inverted at the Xn terminal equally. Thus DXCCII is a five terminal device. The defining equations of the DXCCII is given as:

$$\begin{bmatrix} I_y \\ V_{xp} \\ V_{xn} \\ I_{zp} \\ I_{zn} \end{bmatrix} = \begin{bmatrix} 0 & 0 & 0 \\ 1 & 0 & 0 \\ -1 & 0 & 0 \\ 0 & 1 & 0 \\ 0 & 0 & 1 \end{bmatrix} \begin{bmatrix} V_y \\ I_{xp} \\ I_{xn} \end{bmatrix}$$

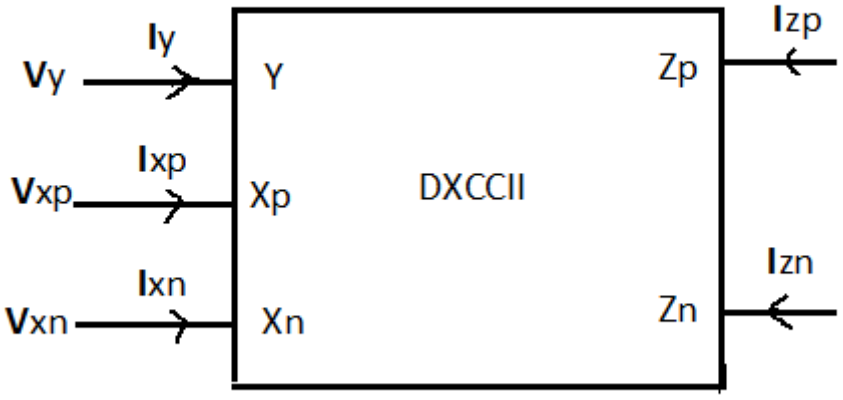

Fig 1 circuit Symbol of DXCCII

2.3 Internal structure of DXCCII

As it is already defined that DXCCII is the cascaded design of two current conveyors, one of those is inverting current conveyors. CMOS representation of the DXCCII is shown in the figure below and this structure has been used for the application of dual mode filter design. In this circuit as properties of DXCCII defined that the current of the Xp and Xn terminal needs to be reflected on the Zp and Zn terminals of the device so to fulfill this requirement current mirrors has been used and as we can read from the properties that current in the Y terminal is zero because Y terminal is connected to the gate terminal of the MOSFET. Observing the circuit we can also come to the conclusion that M_{15} and M_{13} are used additionally to transfer Ixp to the Zp terminal. If DXCCII is designed properly then V_{ds1} can be achieved nearly equal to the V_{ds2} even for the larger Ixp and by doing so voltage tracking error related to the channel length modulation can be eliminated almost.

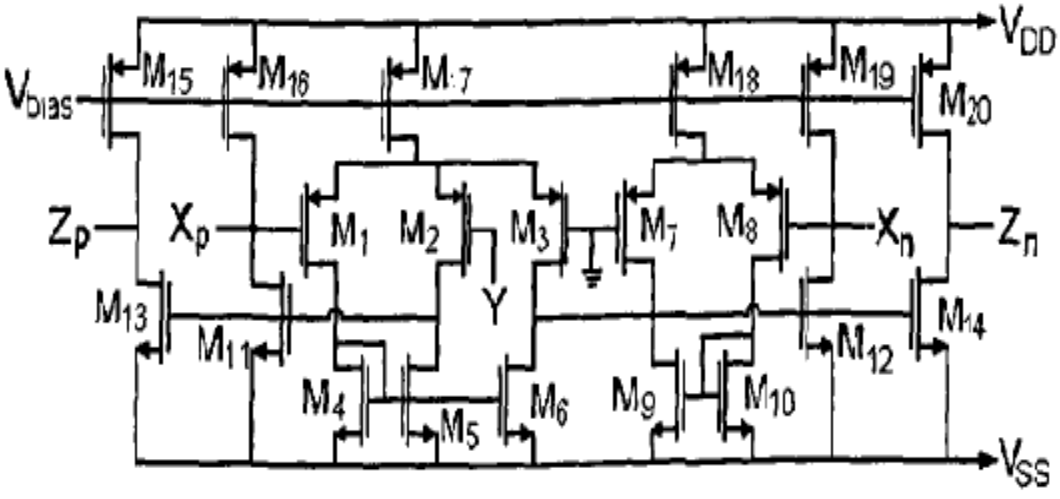

Fig 2 CMOS implementation of DXCCII

The aspect ratios of MOSFETs are matched as follows:

$$(W/L)_{11,12,13,14} = 4\ (W/L)_{4,5} = 2\ (W/L)_{6,9,10} = 20um/1.5um$$

$$(W/L)_{3,7,8} = 2\ (W/L)_{1,2} = 6um/1.5um$$

$$(W/L)_{15,16,17,18,19,20} = 20um/1.5um$$

One more point is to be noted here that for the pMOS transistors M_1, M_2,M_3,M_7 & M_8 bulk source sorting is possible in a n-well technology. In this way, voltage tracking error related to body effects also get eliminated. For the design of DXCCII on PSpice we have used model parameters of a 0.35Um n –well CMOS process.

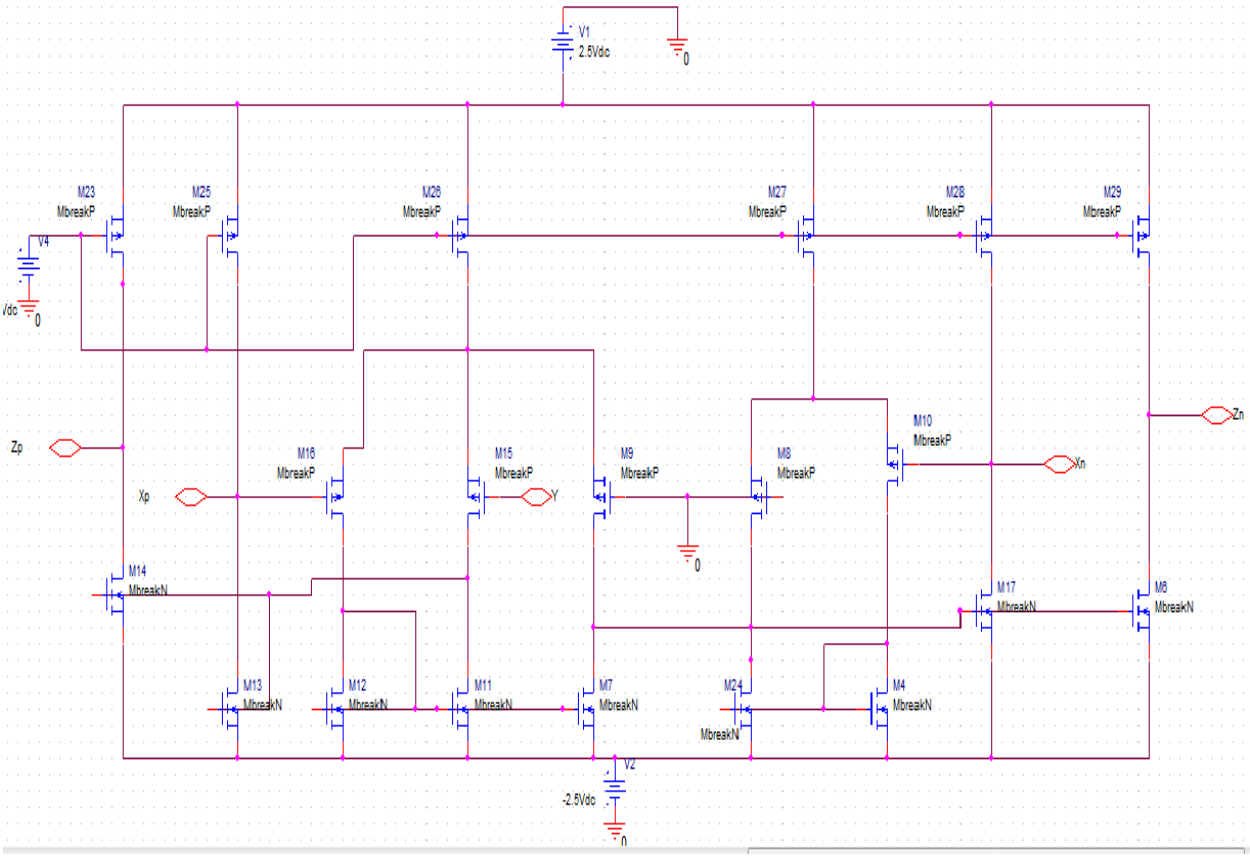

Fig 3 CMOS implementation of DXCCII on PSpice

Verification of all the characterstics of the DXCCII is done on the PSCPICE design

1) Vy =Vxp

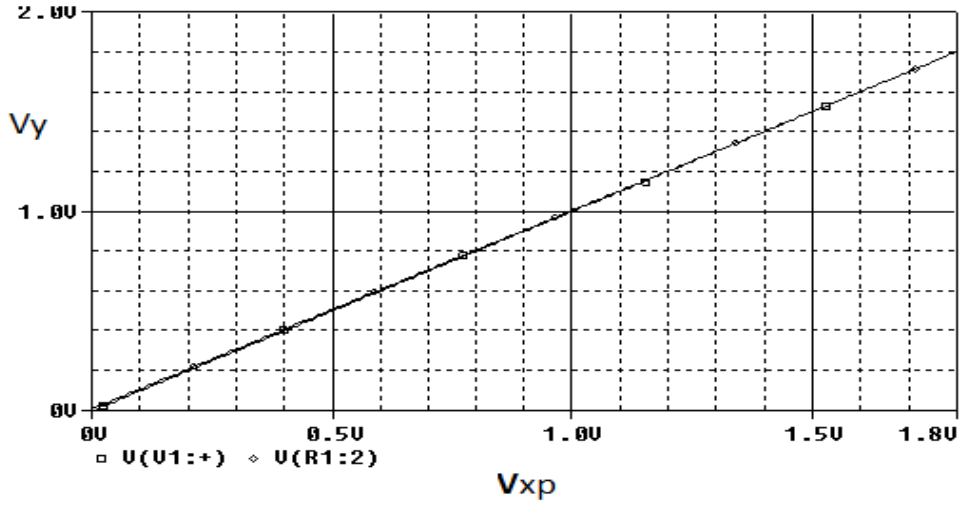

Fig 4: voltage relationship

2) Vy = -Vxn

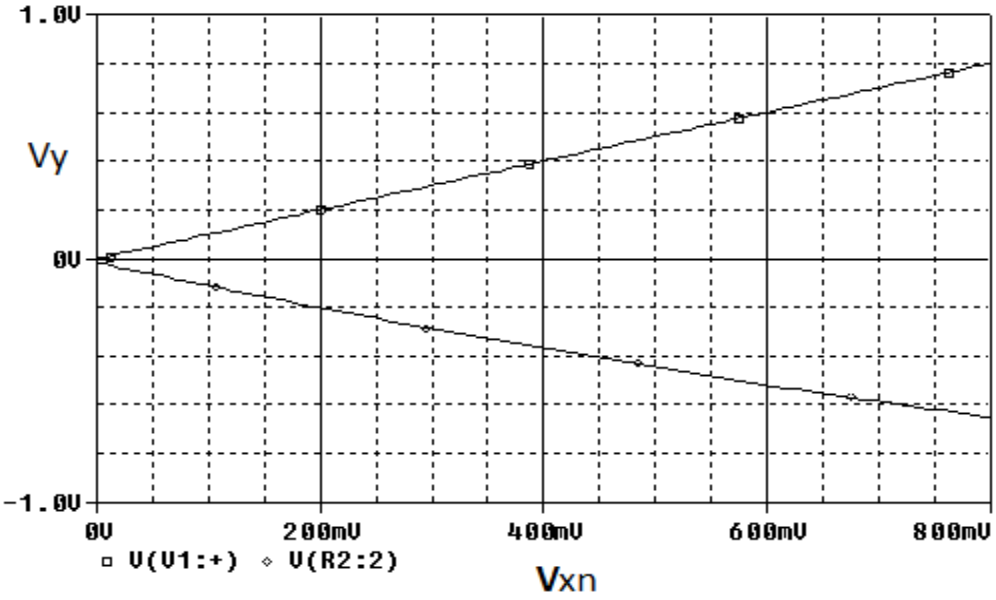

Fig 5: inverting voltage relatinship

3) Ixp =Izp

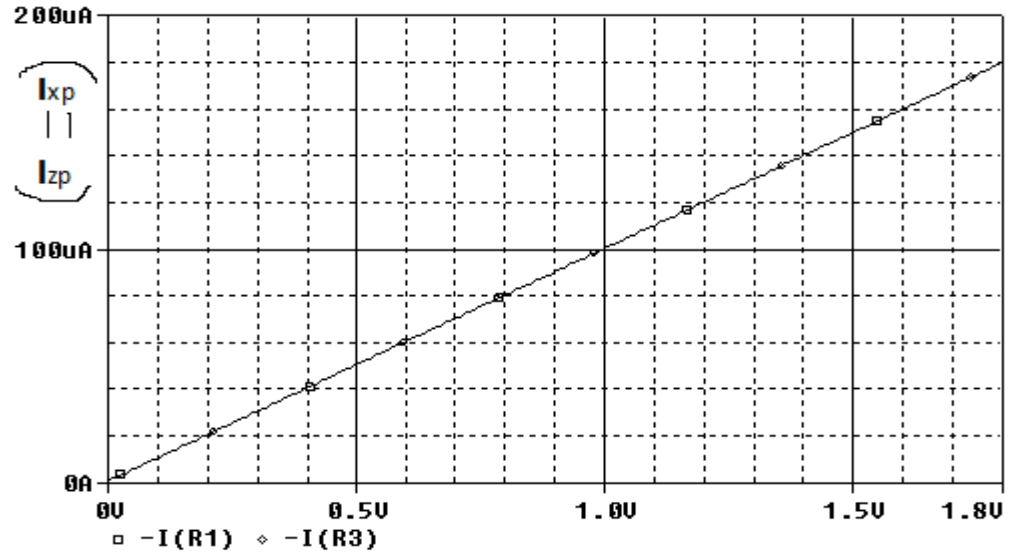

Fig 6 : current relationship of Xp & Zp terminal

4)Ixn = Izn

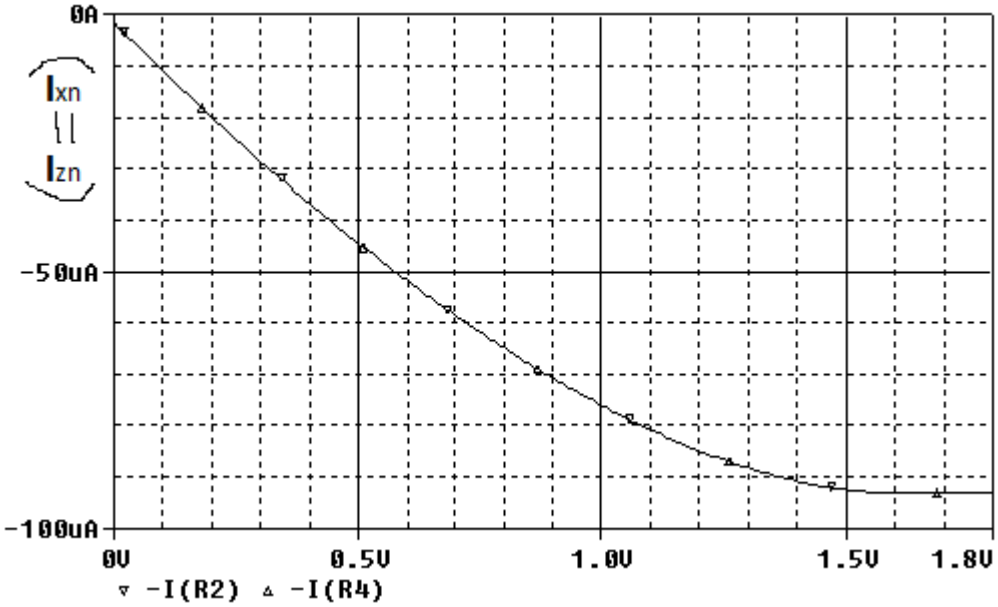

Fig 7: Current relationship of Xn & Zn terminal

2.4 DXCCII Applications

DXCCII has been very useful in so many applications used in electronics devices designs such as design of biquad filters using current mode as well as voltage mode and in the same way it is used as an oscillating device . another important use of DXCCII has been the design of inductor using DXCCII . universal filters has been made using DXCCII.

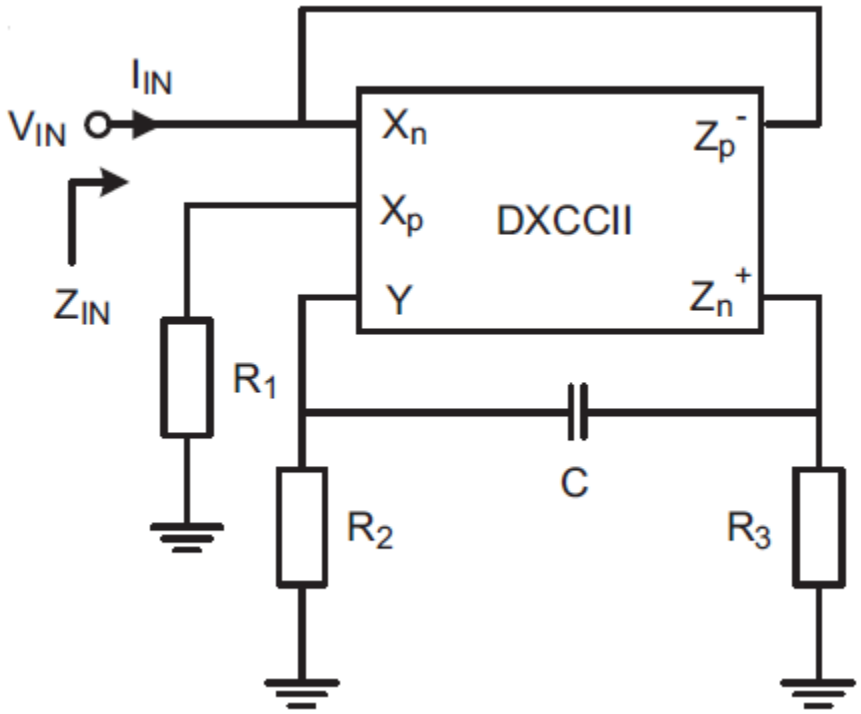

Fig 8 Design of ground inductance using DXCCII

Thus DXCCII can be used as a multipurpose device which can eliminate the drawbacks of the conventional current conveyor devices.

2.5 Advantage of DXCCII

Current controlled current conveyors can work as a linear device only for small input signals. These drawbacks of the CCCII can be eliminated using Dual X current conveyor and in the case of MOSFET C filters also large number of matching MOSFETs are required to increase the large signal linearity so there hindrances of this circuit can also be overlooked by the use of DXCCII.

The filters which use the DXCCII as a device have higher tunability so as to compensate the effect of deviations due to process tolerance, parasitics, temperature, aging etc. as in case of current conveyor RC filters efficient tenability achieving task is tough. Thus DXCCII has a tremendous potential for realizing multiple number of analog signal processing circuits including continuous time filters, analogue multipliers and voltage controlled oscillators.

Chapter 3: Filter topologies

3.1 Introduction

An electric network, which passes or allows unattenuated transmission of electric signal within certain frequency range and stops or disallows transmission of electric signal outside this range is known as filter. Filters are signal conditioners, each function by accepting an input signal, blocking pre-specified frequency components, and passing the original signal minus those components to the output.

In this project three filters namely low pass filter, band pass filter and high pass filter have been designed using Dual X current conveyor (DXCCII) in the mixed mode i.e. circuit can work in both current mode as well as voltage mode using one mode at a time and can give all three filter output responses individually. Filters designed in this project are second order filters. A common architecture has been used for both current mode as well as for voltage mode using two DXCCII devices.

Generalized circuit for Mixed Mode circuit:

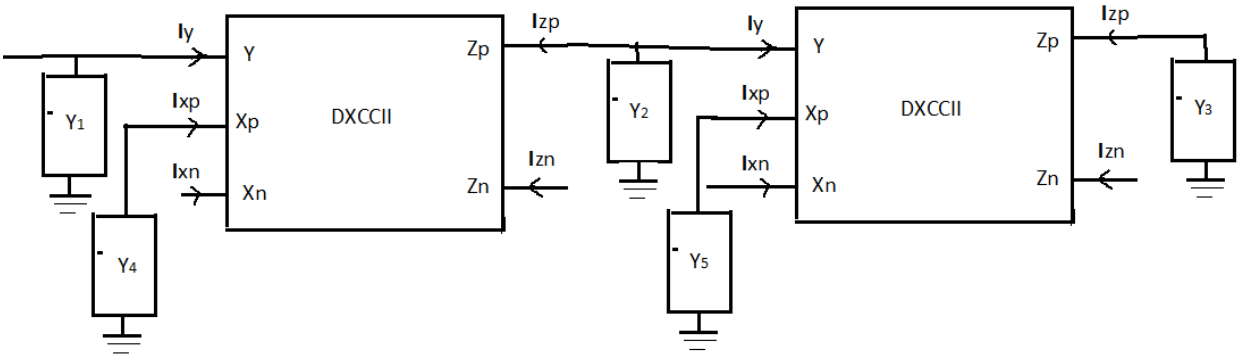

Fig 9 mixed mode circuit using DXCCII

In this circuit five admittances have been used and as per the input and ouput relations of the above given circuit will be used to generate different filter outputs in both current and voltage mode of the circuit.

3.2 Voltage mode circuit

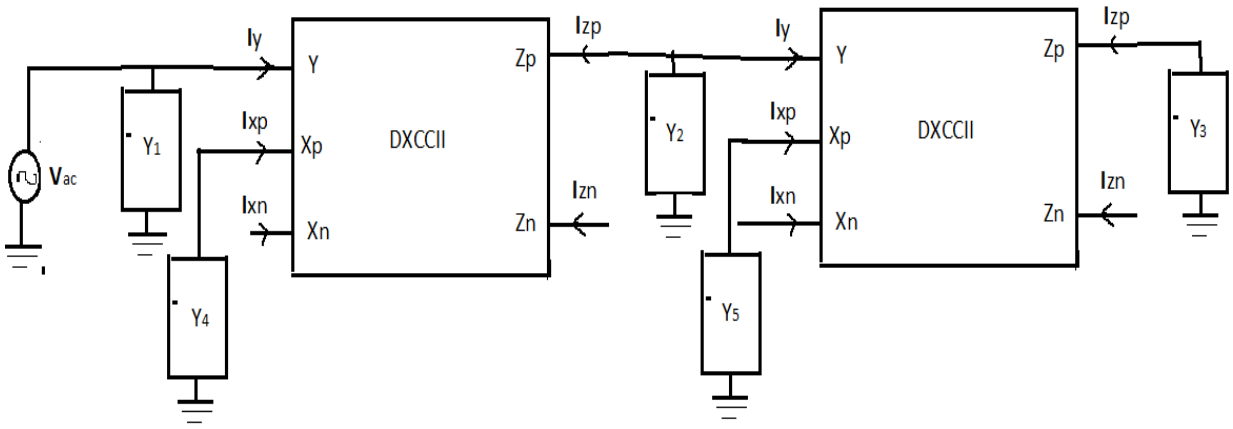

Fig 10 voltage mode circuit

As the above circuit is now used as a voltage mode circuit so here at the supply terminal voltage source is provided and output is taken across the Zp terminal of the second DXCCII i.e. across the Y_3 admittance and all the filter responses are taken through Y_3 terminal. Relations between input and output terminals are as follows:

Using DXCCII characterstic equations

$$V_{zp2} = \frac{-Ixp2}{Y3}$$

$$I_{xp2} = V_{y2} \, . Y_5$$

$$V_{zp2} = \frac{-V_{y2}.Y5}{Y3} \qquad (1)$$

$$I_{zp1} = V_{y2}.\ Y2 \quad \text{and} \quad I_{xp1} = V_{y1}.\ Y4$$

But $$I_{zp1} = -I_{xp1}$$

$$V_{y1}.\ Y4 = -\ V_{y2}.\ Y2$$

$$V_{y2} = \frac{-\ Y4\ Vy1}{Y2} \qquad (2)$$

Putting the value from equation (2) to (1)

$$V_{zp2} = \frac{-\ Y4\ \ Y5Vy1}{Y2Y3} \quad \text{or} \quad \frac{Vout}{Vin} = \frac{-Y4\ Y5}{Y2\ Y3}$$

As per the requirement of the filter we will use the value of all the admittances used here. For the requirement of different filters the value of given admittances can be kept as per given table

Filter Name	Y1	Y2	Y3	Y4	Y5
LP	Independent	SC+G	SC+G	G	G
HP	Independent	SC+G	SC+G	SC	SC
BP	Independent	SC+G	SC+G	SC	G

Table 1: Admittance value for voltage mode circuit

From the above table it is clear that by the combination of four admittances we can get all the three filters. We have kept the value of resistance 1KΩ and value of capacitance as 1nf. This voltage mode circuit is independent of the value of admittance Y1.

3.2.1 Different filter topology on PSPICE for Voltage Mode

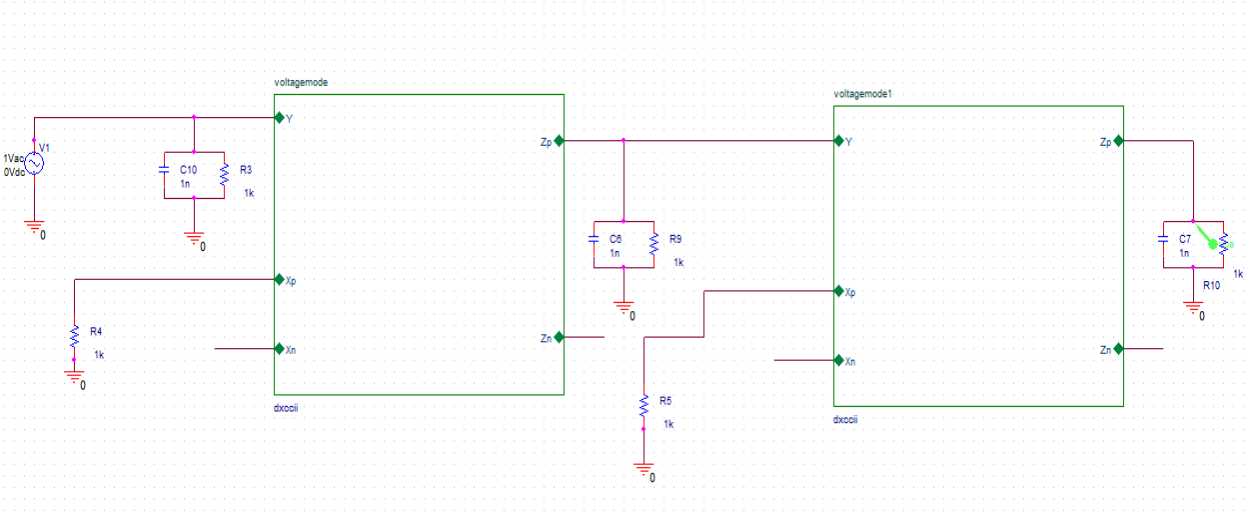

Fig 11: low Pass filter

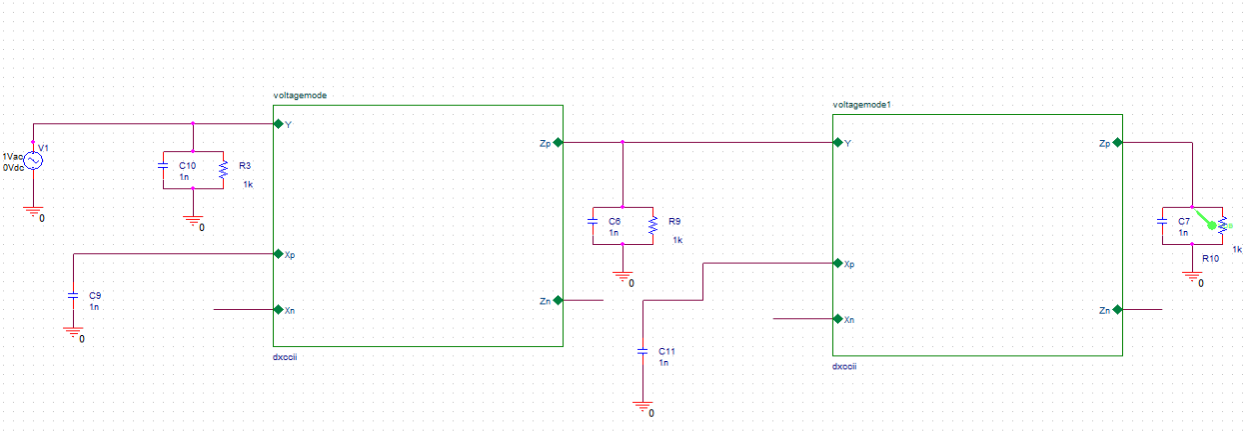

Fig 12: High Pass Filter

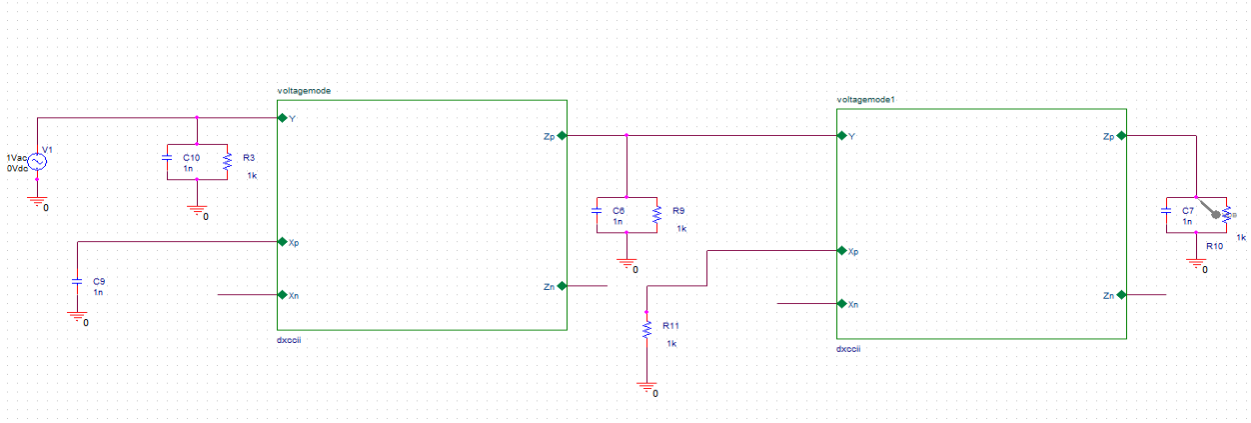

Fig 13: Band Pass Filter

3.3 Current Mode Circuit

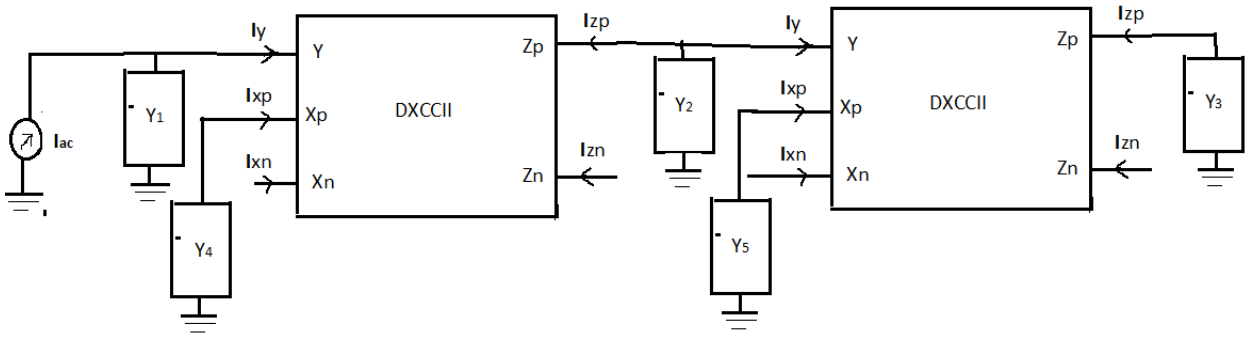

Fig 14 : Current Mode circuit using DXCCII

As the above circuit is now used as a current mode circuit so here at the supply terminal current source is provided and output is taken across the Xp terminal of the second DXCCII i.e. across the Y_5 admittance and all the filter responses are taken through Y_5 terminal. Relations between input and output terminals are as follows:

Using characterstic equation for DXCCII

$$I_{xp2} = V_{xp2}\, Y_5$$

$$V_{xp2} = V_{y2}$$

$$V_{y2} = \frac{-Ixp1}{Y2}$$

$$V_{y1} = \frac{Ixp1}{Y4} = \frac{Iin}{Y1}$$

Using above equations

$$\frac{Iout}{Iin} = \frac{-Y4\, Y5}{Y1Y2}$$

As per the requirement of the filter we will use the value of all the admittances used here. For the requirement of different filters the value of given admittances can be kept as per given table

Filter Name	Y1	Y2	Y3	Y4	Y5
LP	SC+G	SC+G	Independent	G	G
HP	SC+G	SC+G	Independent	SC	SC
BP	SC+G	SC+G	Independent	SC	G

Table 2: Admittance value for current mode circuit

From the above table it is clear that by the combination of four admittances we can get all the three filters. We have kept the value of resistance 1KΩ and value of capacitance as 1nf. This voltage mode circuit is independent of the value of admittance Y3.

Keeping the vaule of all admittances we can get the transfer function of the current mode circuit as per given equation

$$\frac{Iout}{Iin} = \frac{-1}{S^2 + S\left(\frac{C1G2 + C2G1}{C1C2}\right) + \frac{G1G2}{C1C2}}$$

Comparing above transfer function with the standard transfer function of the filters

$$\omega_n = \sqrt{\frac{G1G2}{C1C2}}$$

$$2\xi = \frac{C1G2+C2G1}{\sqrt{C1C2G1G2}}$$

$$Q = \frac{\sqrt{C1C2G1G2}}{C1G2+C2G1}$$

By the above equations we can get the oscillating frequency and the quality factor of the circuit.

3.3.1 Different filter topology on PSPICE in Current Mode

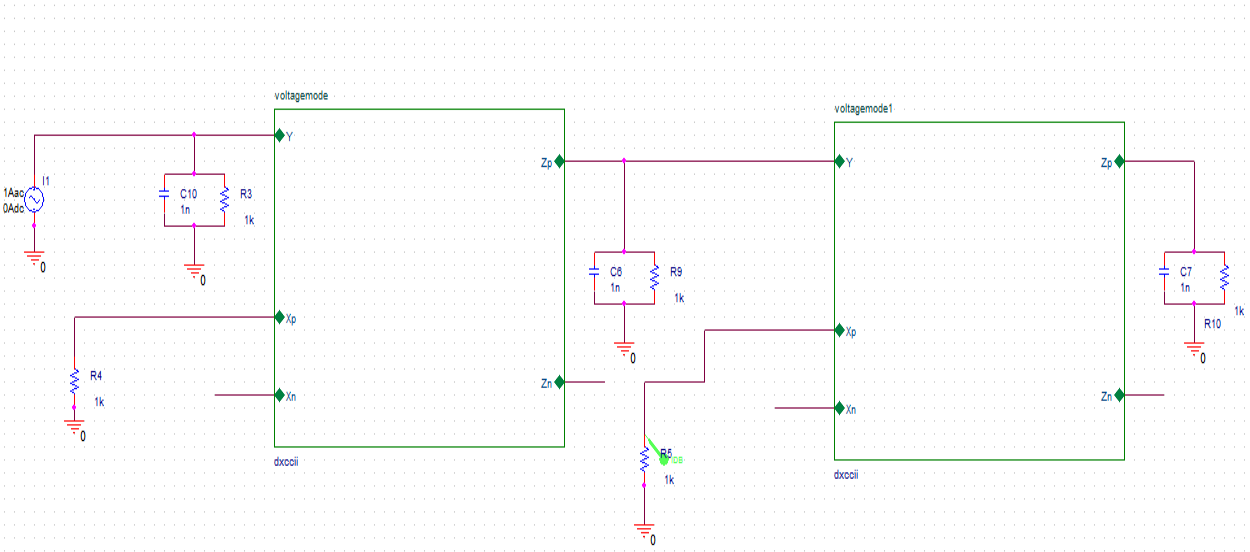

Fig 15: Low Pass Filter

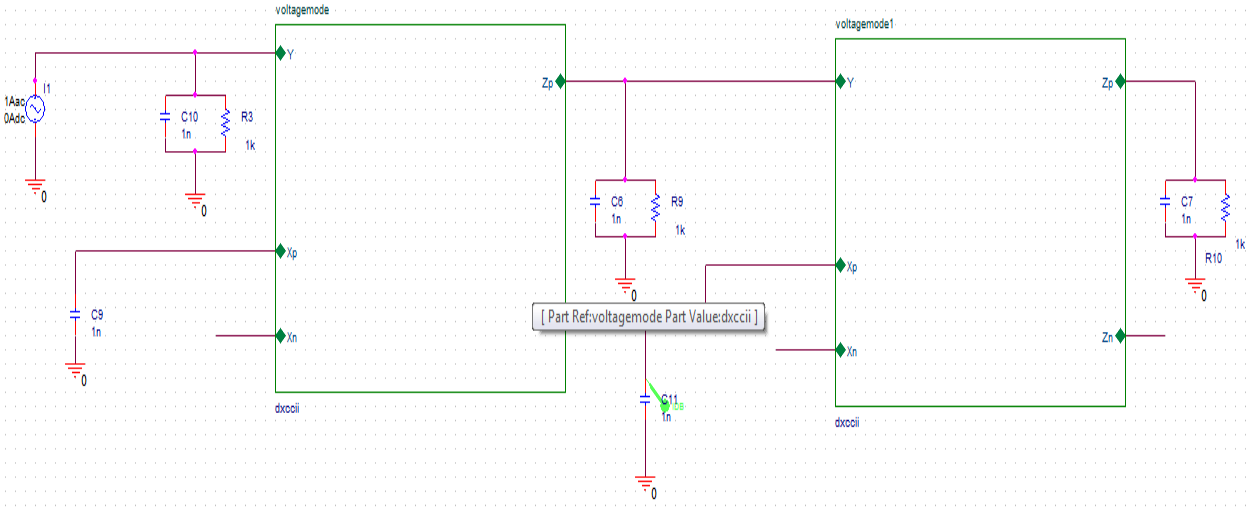

Fig 16: High Pass Filter

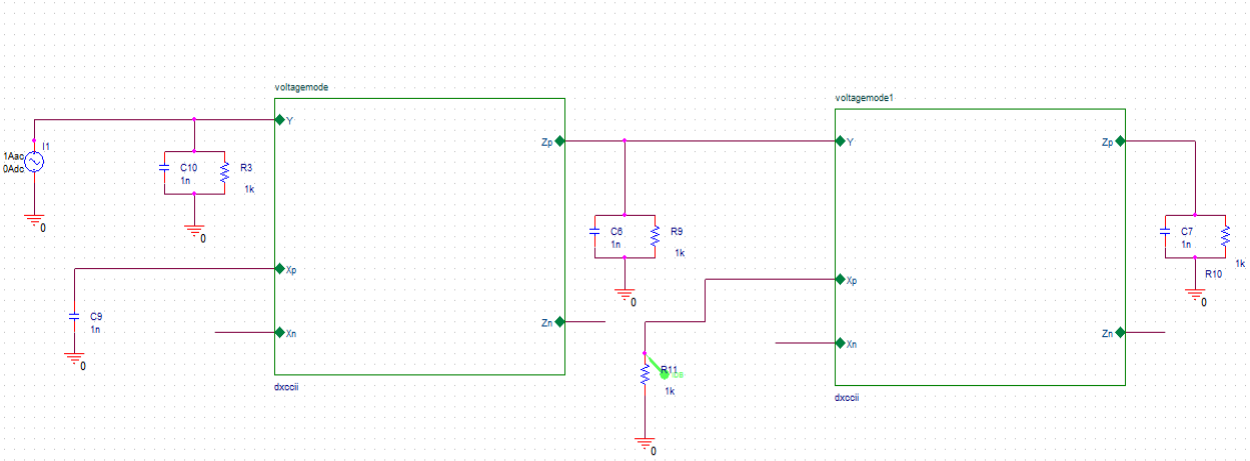

Fig 17: Band Pass Filter

3.4 Sensivity of the proposed circuit

Passive components are used in analyzing analog filters. Due to some environmental effects such as temperature, humidity or chemical change occur in the network these components may deviate from nominal design values. As an effect to this, filter performance will deviate from the desired values. Sensitivity is the most important criteria to compare different filter architecture.

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The sensitivity is defined as the deviation P caused by an error ΔY, can be expressed as:

$$S_y^P = \frac{\frac{dP}{P}}{\frac{dY}{y}}$$

For the mixed mode circuit here sensitivities has been defined:

$$S_{G1}^{\omega} = 0.5 \qquad S_{G2}^{\omega} = 0.5$$

$$S_{C1}^{\omega} = -0.5 \qquad S_{C2}^{\omega} = -0.5$$

$$S_{G1}^{Q} = \frac{1}{2} - \frac{C2\,G1}{C1G2 + C2G1} \qquad S_{G2}^{Q} = \frac{1}{2} - \frac{C1\,G2}{C1\,G2 + C2G1}$$

Chapter 4 : Simulation Results

4.1 Introduction:

In this chapter different filter outputs of the proposed design has been shown using current mode and voltage mode both and all the simulations has been done on PSPICE software using modal parameters of 0.35um 5 V n-well CMOS process.

For the design of DXCCII basic device supply voltage of 2.5 V has been used and the value of bias voltage has been kept -0.5 mV. Using these sources we have made all the filters in both modes. Three filter responses has been present there.

4.2 Voltage mode responses

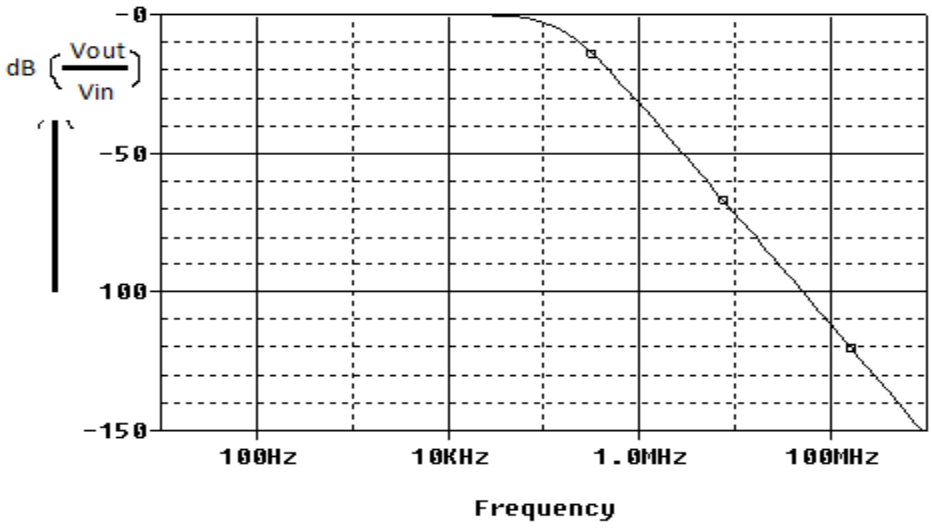

Fig 18: Low pass filter response in voltage mode

Cut off frequency obtaied for low pass filter f_{3dB} = 154.27 KHz

Theoritically obtained cut off frequency = 159 KHz

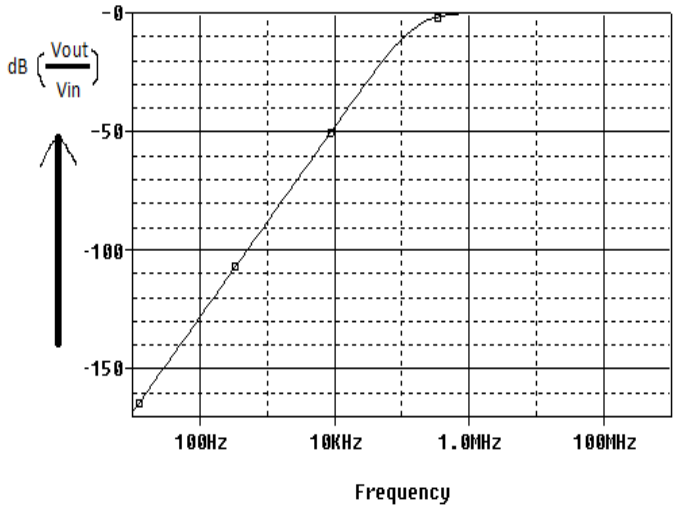

Fig 19: High Pass Filter response in voltage mode

Cut off frequency obtaied for high pass filter f_{3dB} = 179.15 KHz

Theoritically obtained cut off frequency = 159 KHz

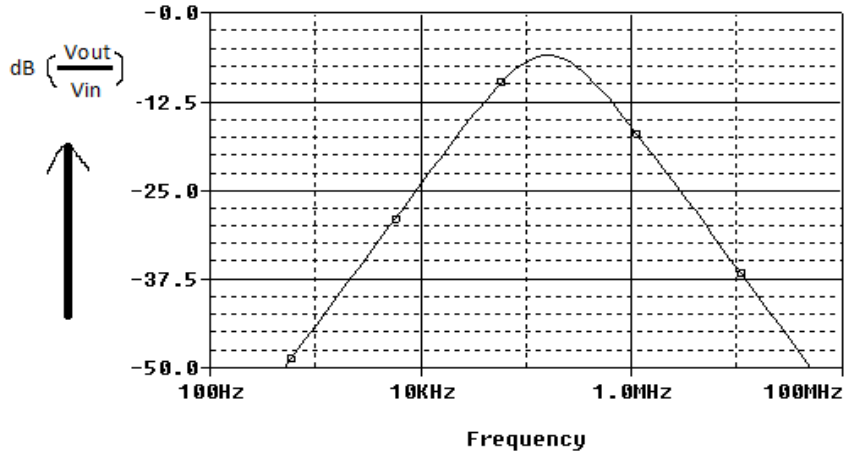

Fig 20: Band pass filter response in voltage mode

Cut off frequency obtaied for band pass filter f_{3dB} = 224.19 KHz

Theoritically obtained cut off frequency = 159 KHz

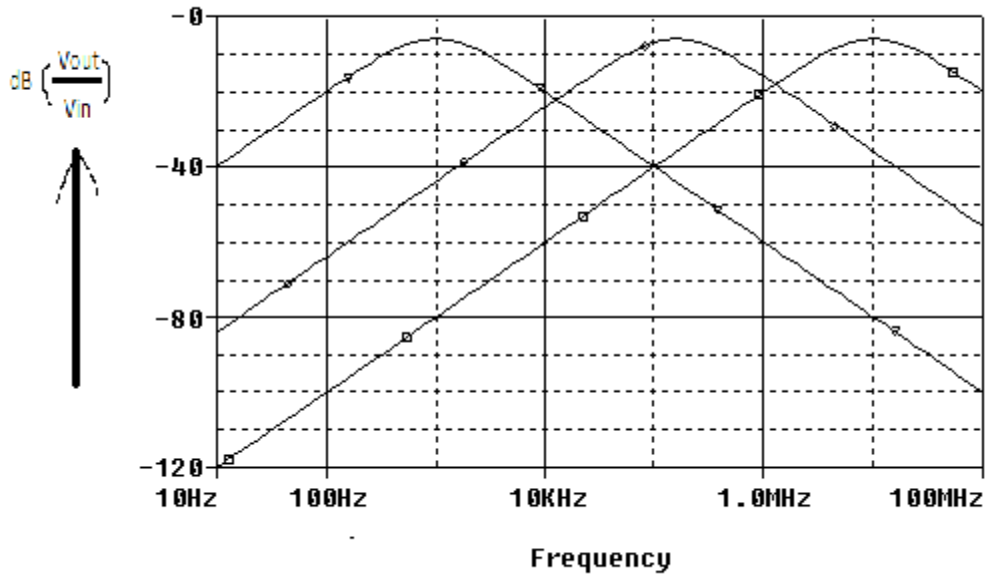

Fig 21: band pass response for low, medium & high frequency

4.3 Parameter Sweeping in voltage mode

In order to get the circuit behavior for different values of parameters ,parameter sweeping is performed. In the proposed circuit parameter sweeping has been done for resistance capacitance and temperature.

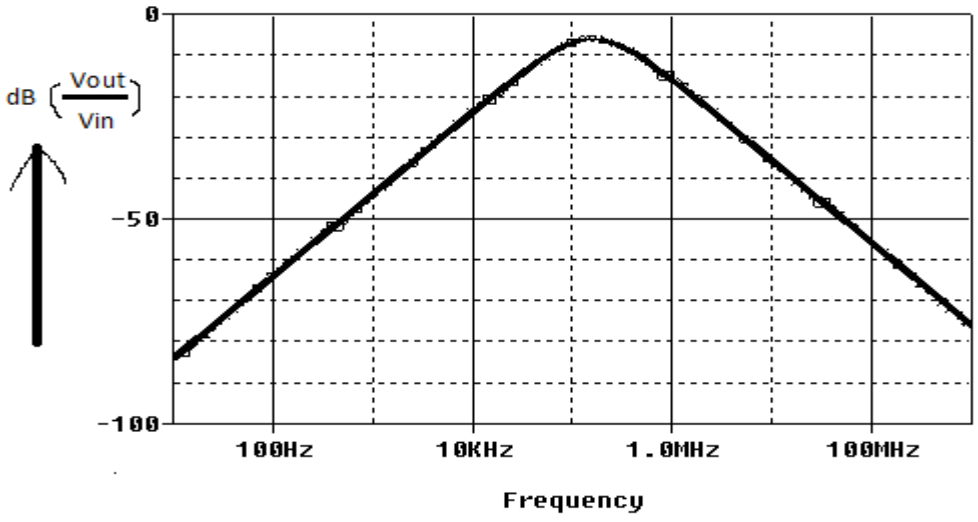

Fig 22 parameter sweeping response with resistance

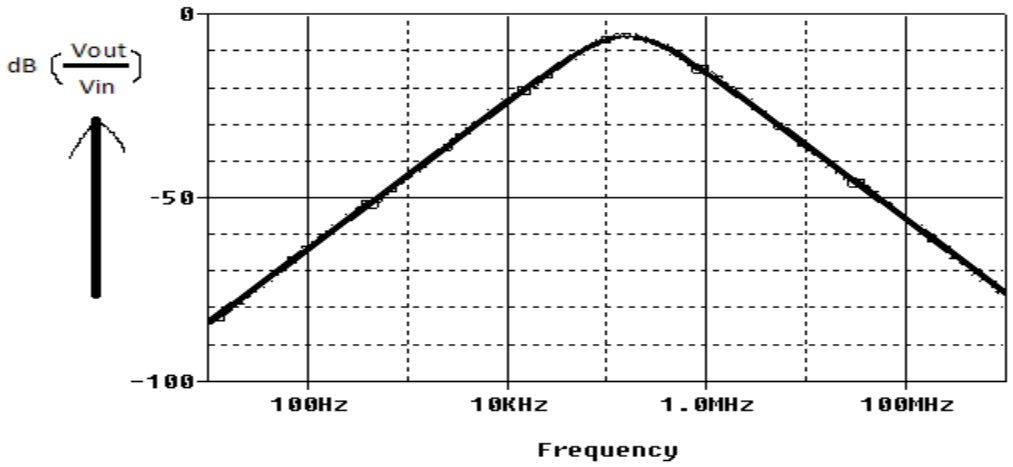

Fig 23 : parameter sweeping response with capacitance

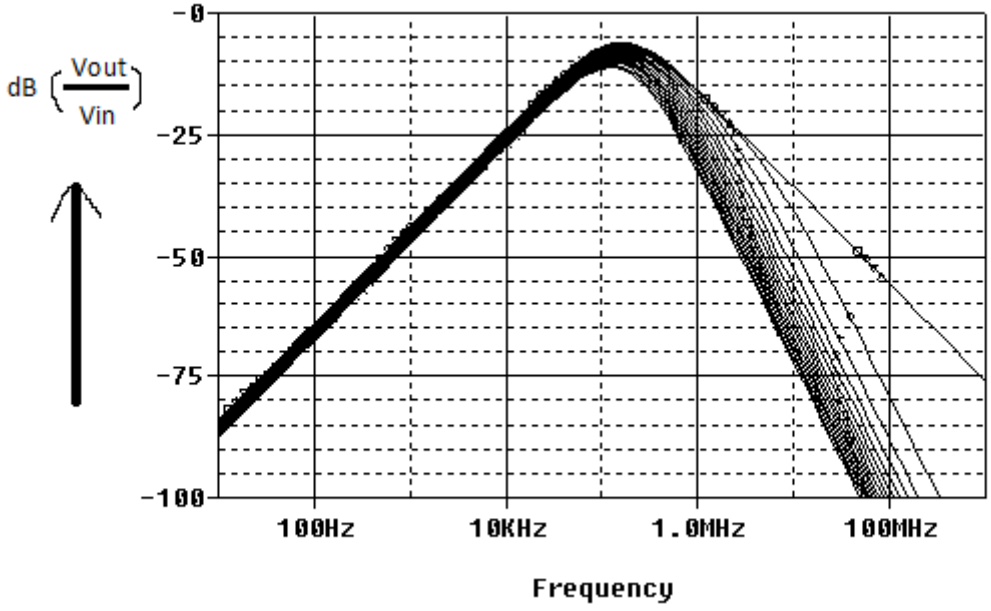

Fig 24 : parameter response with temperature

4.4 Transient response of band pass filter in voltage mode

Transient response of a system is a response of the system to a change from equilibrium. Transient response is also known as impulse response.

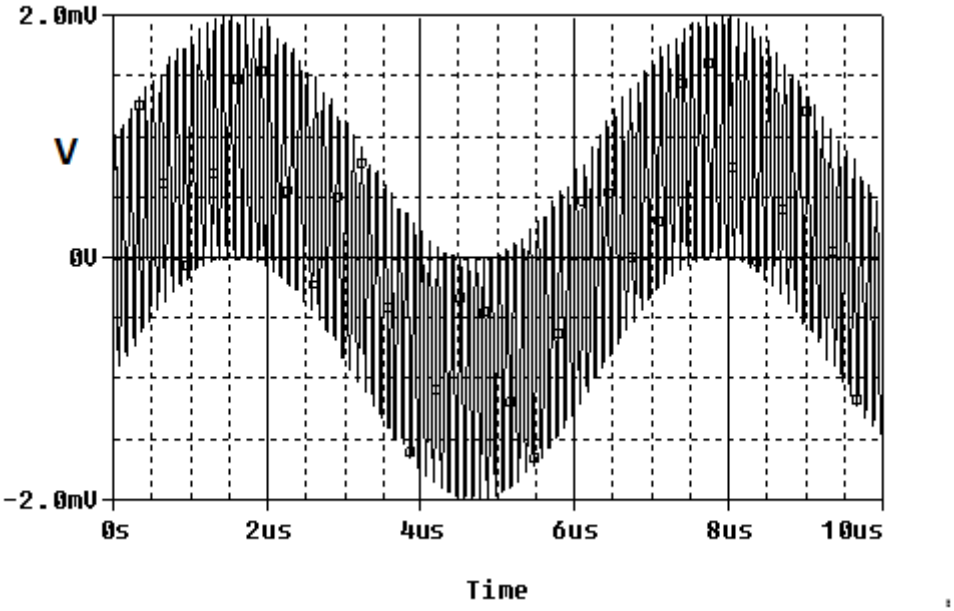

Fig 25 : transient input response for band pass filter in VM

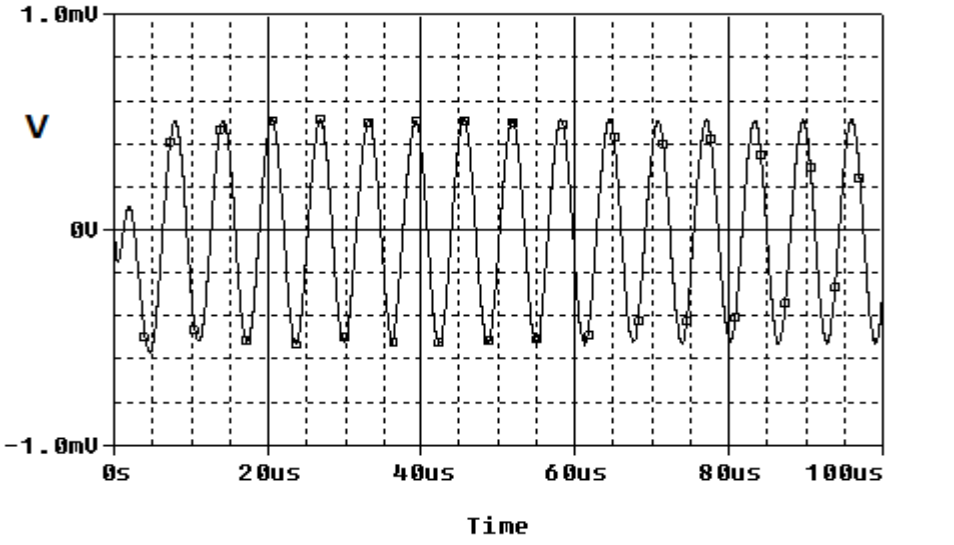

Fig 26 : transient output response of band pass filter in VM

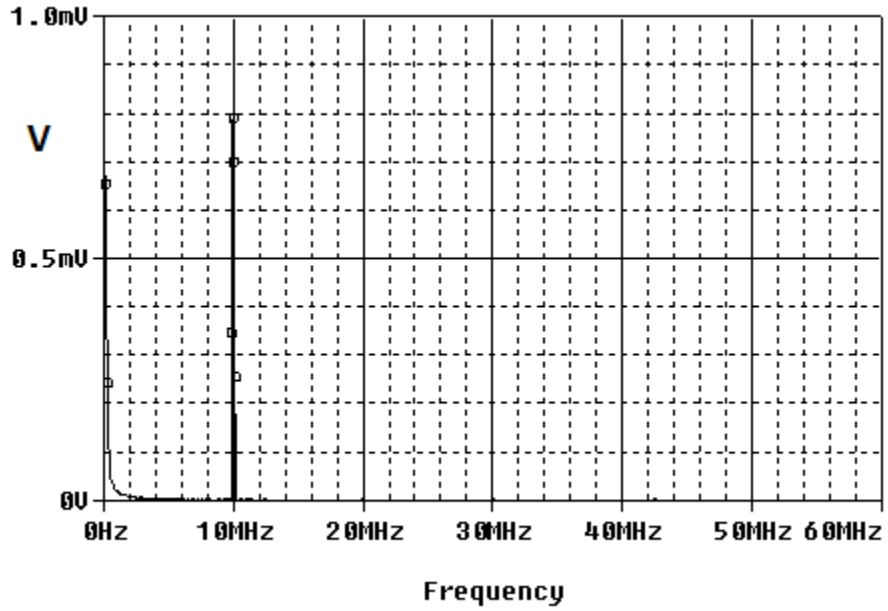

Fig 27: input FFT response for BPF

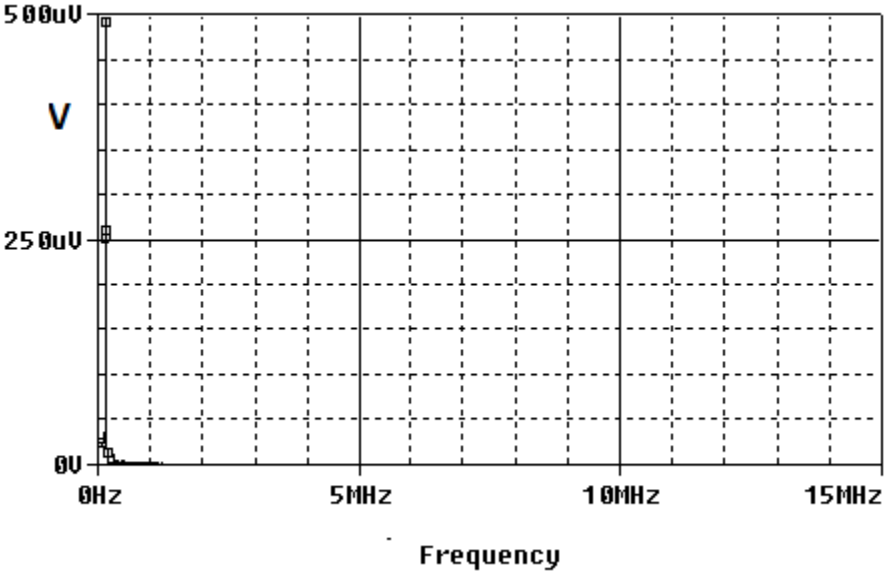

Fig 28 : output FFT response for BPF

4.5 Total harmonic distortion for voltage mode circuit

Voltage (mV)	THD(%)
05	**2.80**
10	**3.49**
15	**4.31**
20	**6.21**
25	**6.88**
30	**7.66**
35	**8.55**

Table 3: THD values for voltage mode circuit

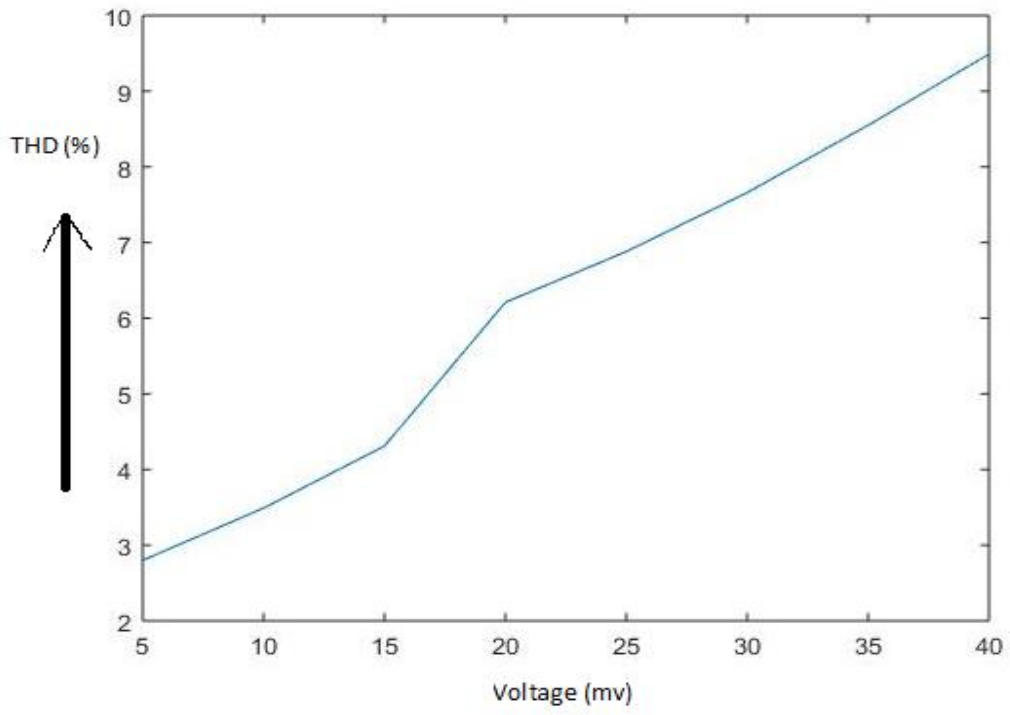

Fig 29: THD in voltage mode

4.6 Current mode responses

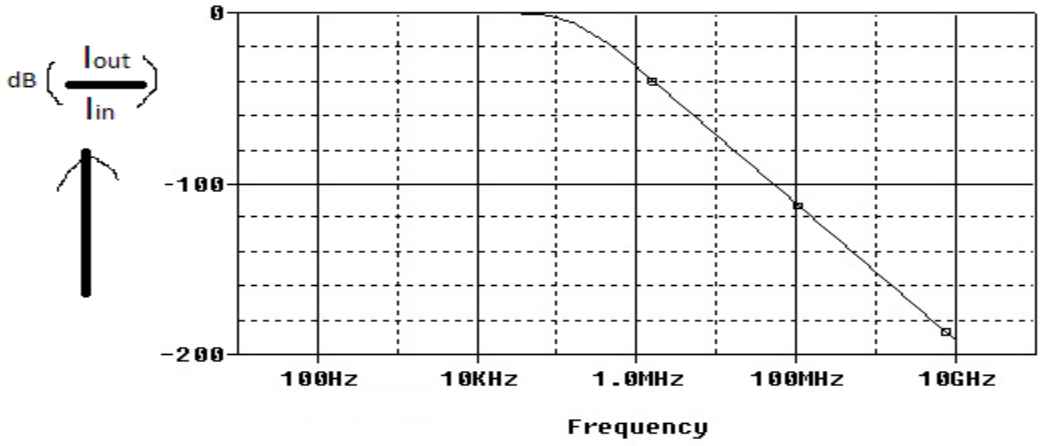

Fig 30: low pass filter response in current mode

Cut off frequency obtaied for low pass filter f_{3dB} = 149.73 KHz

Theoritically obtained cut off frequency = 159 KHz

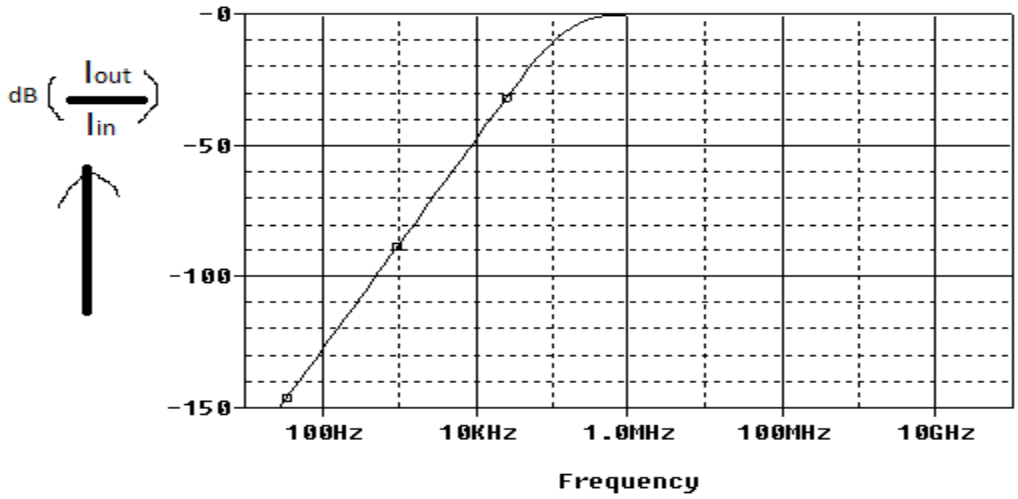

Fig 31: High pass filter response in current mode

Cut off frequency obtaied for high pass filter f_{3dB} = 168.75 KHz

Theoritically obtained cut off frequency = 159 KHz

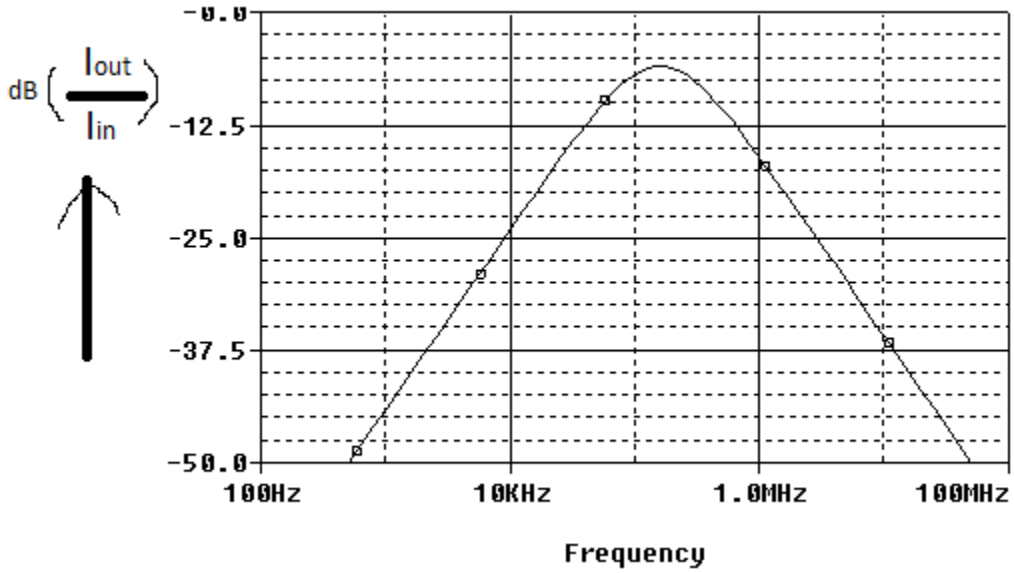

Fig 32: Band pass filter response in current mode

Cut off frequency obtaied for high pass filter $\mathbf{f}_{3dB}$ = 384 KHz

Theoritically obtained cut off frequency = 159 KHz

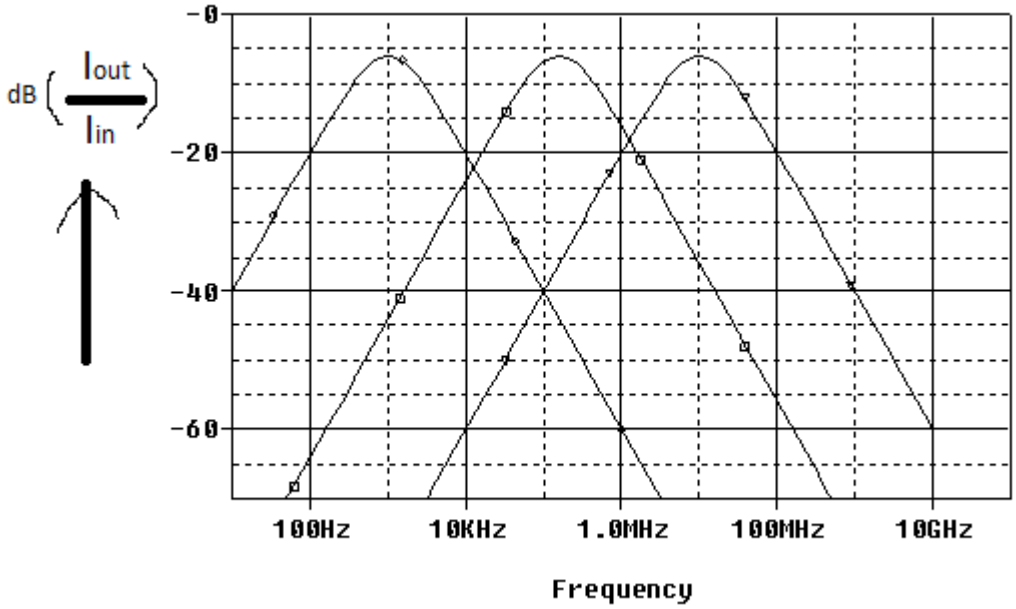

Fig 33: Band pass filter response for low, medium and high frequency

4.7 Parameter sweeping in current mode

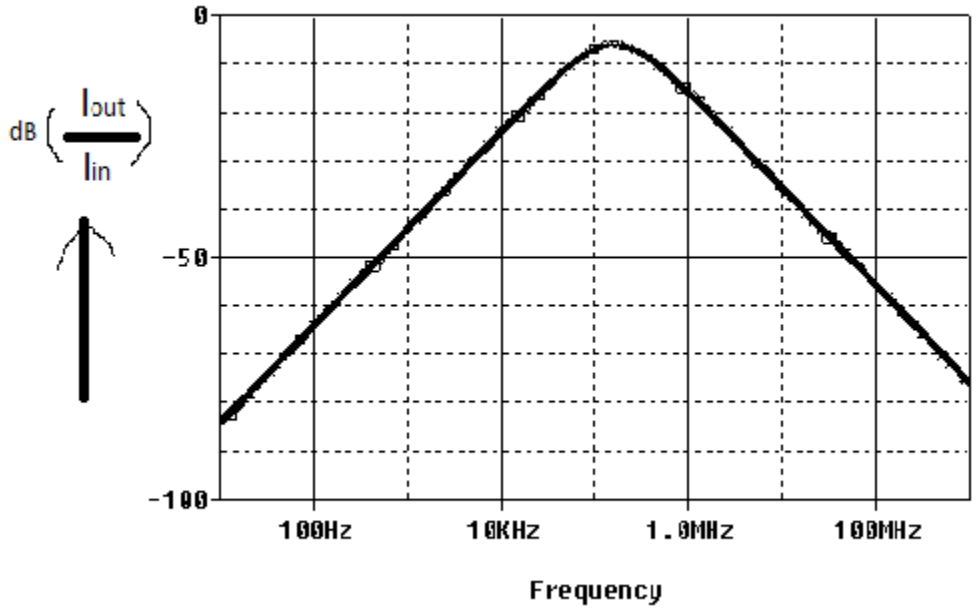

Fig 34:Parameter sweeping response with resistor in CM

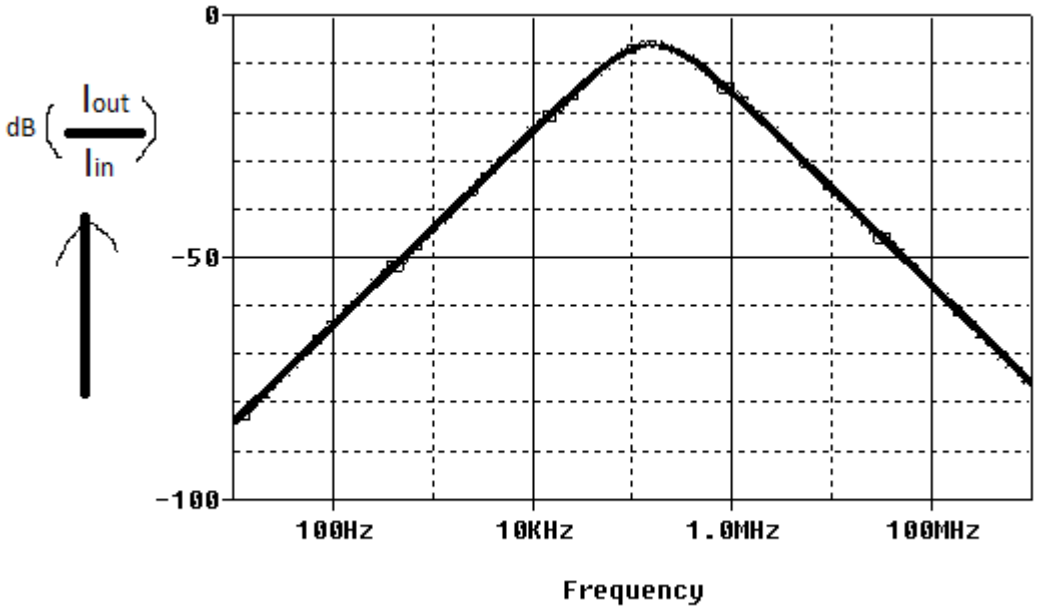

Fig 35: Parameter sweeping response with capacitance in CM

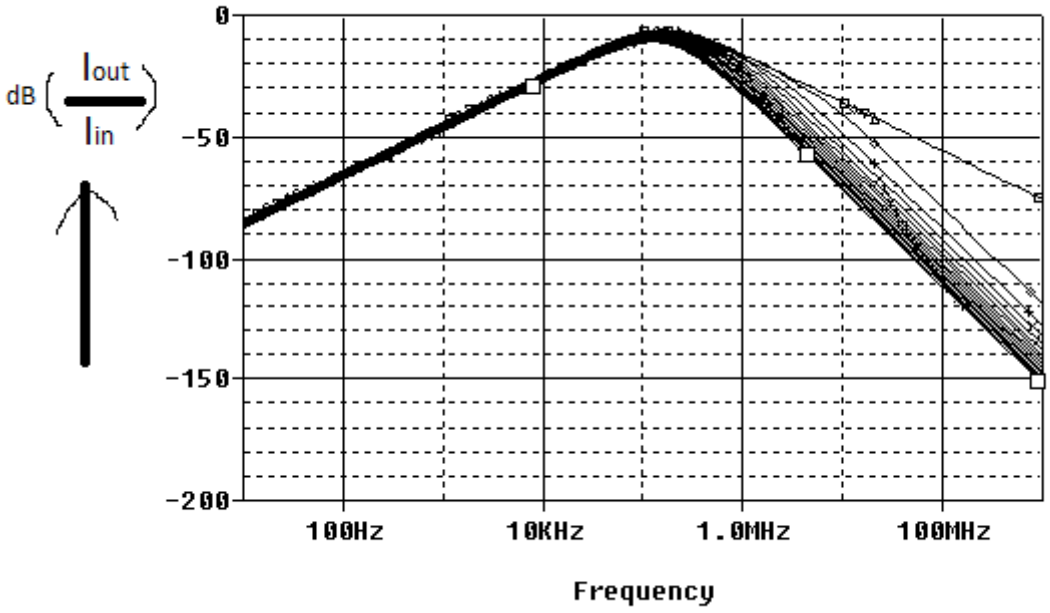

Fig 36: Parameter sweeping response with temperature in CM

4.8 Transient response of Band pass filter in Current mode

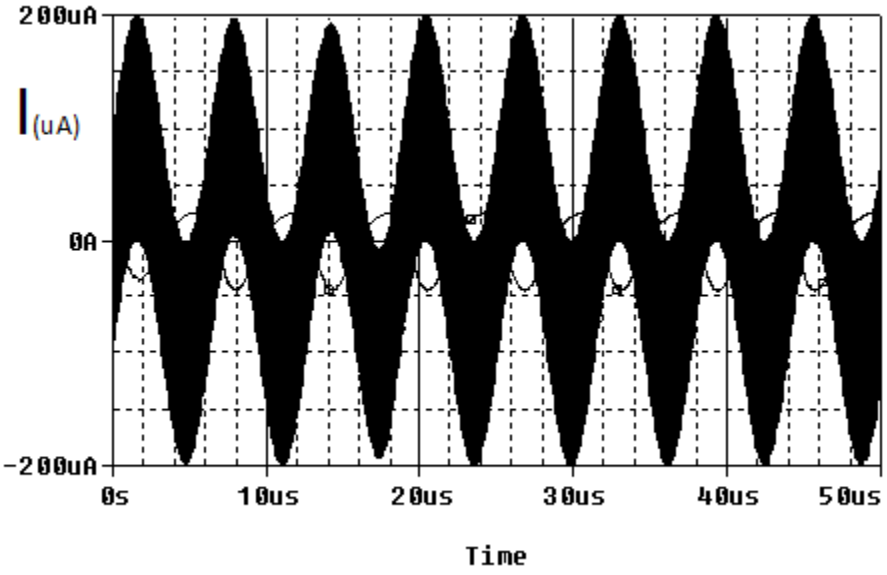

Fig 37: Input transient response for BP filter in CM

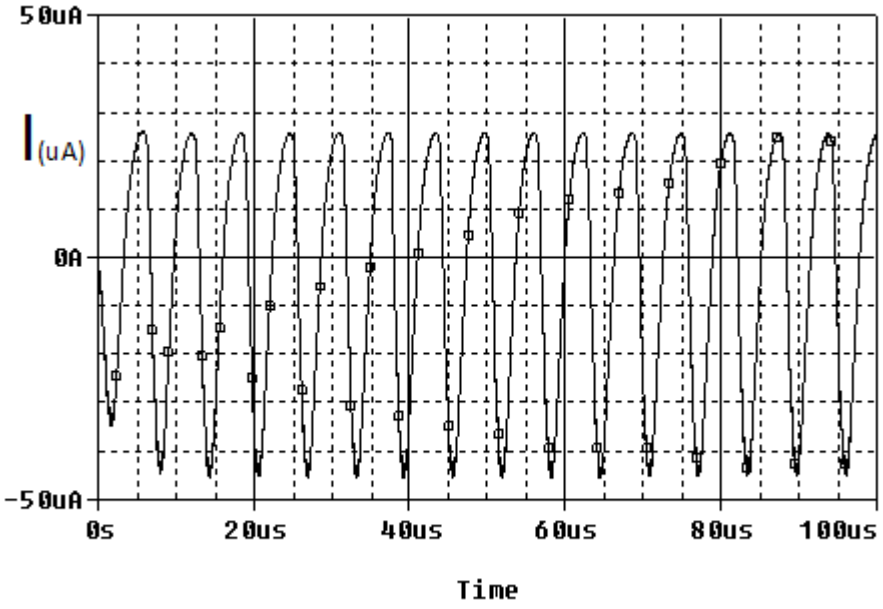

Fig 38: Output transient response for BP filter in CM

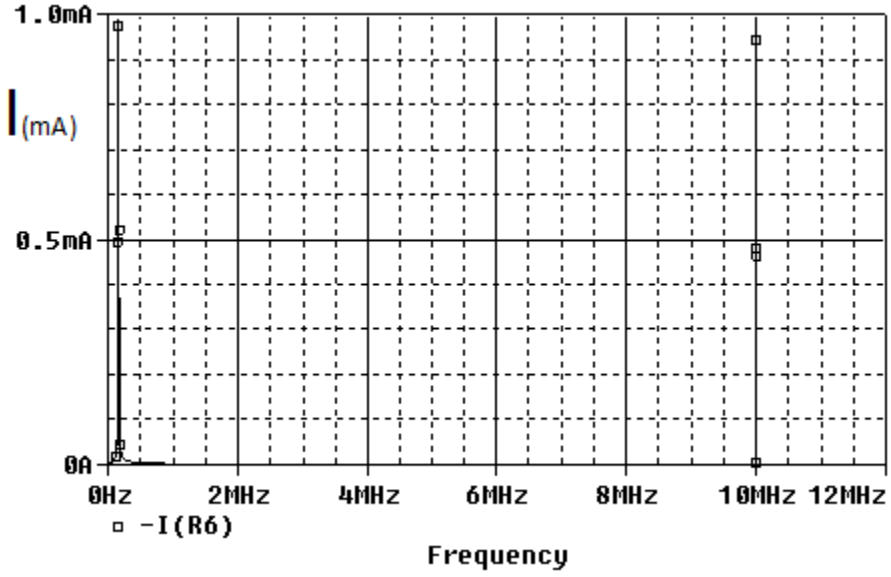

Fig 39: Input FFT response in current mode for BP filter

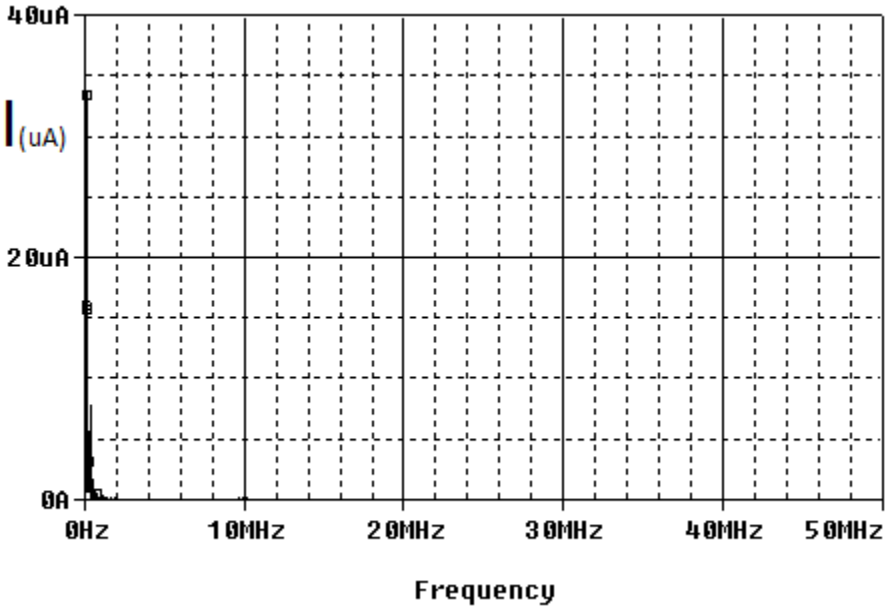

Fig 40: Output FFT response in current mode for BP filter

4.9 Time harmonic distortion for Current mode circuit

Current(mA)	THD(%)
0.001	**2.45**
0.002	**2.56**
0.005	**3.10**
0.009	**4.41**
0.015	**7.03**
0.025	**10.9**
0.05	**15.0**

Table 4: THD values for current mode circuit

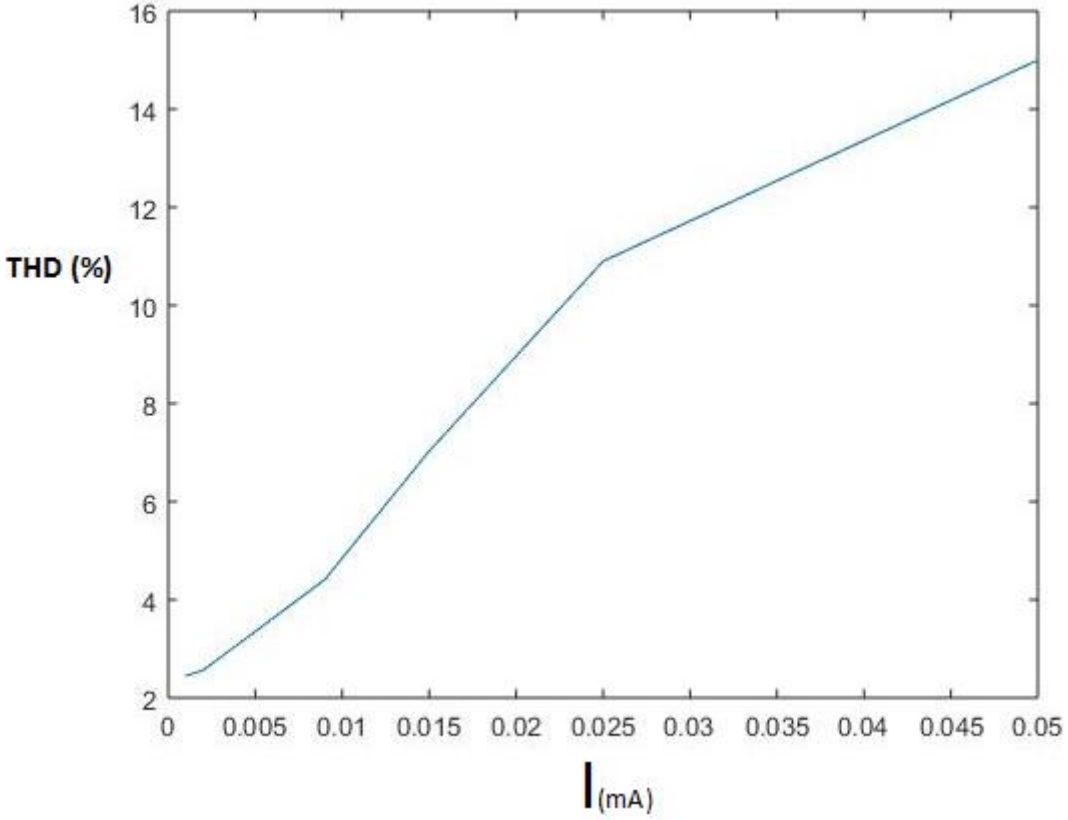

Fig 41: THD in current mode

CHAPTER 5: CONCLUSION AND FUTURE SCOPE

5.1 Outcome

The working of second order low pass, high pass and band pass filter has been verified using both current and voltage mode using i.e. mixed mode filter topology has been designed here using DXCCII device. All the simulations have been done here using PSPICE. Here filters are designed using capacitance and resistance and all the filters are working perfectly for low, medium and high frequencies as verified through the simulation results. Several filter topologies has been studied here during literature review and through the help of all that information dual mode filters have been designed. All the filters are working as a single input and single output filter. Finally comparison has been presented here with the reference papers

Reference paper	No. of inputs	Simultaneous output	Standard filter function	VM/CM	No. of active block used	No of passive components used
1	three	one	BP,LP,HP, AP,NF	VM	one	six
2	three	two	BP.LP	CM	two	two
3	three	two	LP,BP,HP NF,AP	CM	two	seven
4	One	one	HP,BP,LP	VM	one	four
PROPOSED	one	one	BP,HP,LP	BOTH	Two	six

Table 5: comparison papers with reference papers

5.2 FUTURE SCOPE

There are so many future options in the proposed circuit as we can try to make this circuit free of all passive components and can use MOSFETS in place of resistance used here. Second thing we can think of here is to make circuit tunable so that circuits application criterion can be widened. Moreover we can think of converting circuit in single input multiple output circuit i.e. can try to get multiple outputs at the same time using single supply source for both current and voltage mode. So the circuit proposed here can be used for further new application innovation.

Reference

1) Indrit Myderrizi , Shahram Minaei , Erkan Yuce ” DXCCII-based grounded inductance simulators and filter applications” Microelectronics Journal 42 (2011)

2) Ali Zeki & Ali Toker “The dual-X current conveyor (DXCCII): a new active device for tunable continuous-time filters” International Journal of Electronics(2003)

3) Shipra Maheshwari , Sudhanshu Maheshwari “Multi Input Multi Output Biquadratic Universal Filter using Dual –X Current Conveyor(DXCCII)” international conference on computer and communication technology (2010)

4) Montree Kumngern, “A DXCCII-Based Four-Quadrant Multiplier” 2013 IEEE power engineering & optimization conference

5) B.Razavi, Design of Analog CMOS Integrated circuits: McGraw-Hill, 2001.

6) D.BIOLEK, R.SENANI, V.BIOLKOVA, Z.KOLKA, “Active elements for analog signal processing: classification, review, and new proposals”, Radio engineering, 2008, vol. 17, no. 4, pp. 15–32.

7) P. Gray, P. Hurst, S. Lewis, and R. Meyer, Analysis and Design of Analog Integrated Circuits, New York: John Wiley & Sons, 4th ed., 2001, Pages: 748-802, 808-856

8) S. Maheshwari, “Analogue signal processing applications using a new circuit topology,” IET Circuits Devices Systems vol. 3, pp.106–115. 2009.

9) G. Ferri, N.C. Guerrini, R. Romanato, G. Scotti, A. Trifiletti, CCII-based highvalued inductance simulators with minimum number of active elements, in: Proceedings of the 18th European Conference on Circuit Theory and Design, ECCTD, Seville, Spain, 27–30 August 2007, pp. 440–443.

Appendicies

0.35um

.MODEL NMOS NMOS(LEVEL = 3, TOX = 7.9E-9, NSUB = 1E17,
+GAMMA=0.5827871, PHI=0.7, VTO=0.5445549, DELTA=0,
+UO = 436.256147, ETA = 0, THETA = 0.1749684,
+KP =2.055786E-4, VMAX=8.309444E4, KAPPA=0.2574081,
+RSH = 0.0559398, NFS = 1E12, TPG = 1, XJ = 3E-7,
+LD=3.162278E-11, WD=7.046724E-8, CGDO=2.82E-10,
+CGSO = 2.82E-10, CGBO = 1E-10, CJ = 1E-3, PB = 0.9758533,
+MJ =0.3448504, CJSW=3.777852E-10, MJSW=0.3508721)

.MODEL PMOS PMOS
+(LEVEL = 3, TOX = 7.9E-9, NSUB = 1E17,
+GAMMA=0.4083894, PHI=0.7, VTO=-0.7140674, DELTA=0,
+UO =212.2319801, ETA=9.999762E-4, THETA=0.2020774,
+KP = 6.733755E-5,VMAX = 1.181551E5, KAPPA = 1.5,
+RSH = 30.0712458, NFS = 1E12, TPG=-1, XJ = 2E-7,
+LD=5.000001E-13, WD=1.249872E-7, CGDO=3.09E-10,
+CGSO = 3.09E-10, CGBO = 1E-10, CJ = 1.419508E-3,
+PB=0.8152753, MJ=0.5, CJSW=4.813504E-10, MJSW=0.5)