FINFET AND GAAFET FABRICATION IN NANOSCALE AND ITS APPLICATIONS

MAJOR PROJECT-II
REPORT

MASTER OF TECHNOLOGY
IN
VLSI DESIGN & EMBEDDED SYSTEM

Submitted By:

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CANDIDATE'S DECLARATION

I, Nishu Singh, Roll No. 2K18/VLS/09 student of M.Tech (VLSI DESIGN AND EMBEDDED SYSTEM), hereby declare that the project Dissertation titled **"FINFET AND GAAFET FABRICATION IN NANOSCALE AND ITS APPLICATIONS"** which is submitted by me to the Department of ELECTRONICS AND COMMUNICATION ENGINEERING, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is original and not copied from any source without proper citation. This work has not previously formed the basis for the award of any Degree, Diploma Associateship, Fellowship or other similar title or recognition.

Place: Delhi **NISHU SINGH**

Date: 04/09/2020 (2K18/VLS/09)

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CERTIFICATE

I hereby certify that the Project Dissertation titled **"FINFET AND GAAFET FABRICATION IN NANOSCALE AND ITS APPLICATIONS**" which is submitted by NISHU SINGH, Roll No 2K18/VLS/09, Department of Electronics and Communication, Delhi Technological University, Delhi in partial fulfillment of the requirement for the award of the degree of Master of Technology, is a record of the project work carried out by the student under my supervision. To the best of my knowledge this work has not been submitted in part or full for any Degree or Diploma to this University or elsewhere.

Place: Delhi **PROF. RAJESHWARI PANDEY**

Date: 04/09/2020 **SUPERVISOR**

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Date: 04/09/2020 Nishu Singh

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ABSTRACT

This paper presents detailed design of n-channel FinFET and n-channel GAAFET with physical gate length of 28 nm using COGENDA Visual TCAD. For the designed device silicon is used as dopant, silicon oxide as spacer and aluminium as metal contact in both the devices. The work functions for the n-channel and p-channel GAAFET is set as 4.5 eV and 4.97 eV respectively, and same for n-channel and p-channel FinFET. The electrical characteristics of the devices like ON current (I_{ON}), leakage current (I_{OFF}), sub-threshold swing (SS), drain induced barrier leakage (DIBL) are extracted through simulations for both the devices. Further, to check the device functionality in circuit applications two digital application of each devices namely an inverter and a NAND GATE are designed. A comparative study of various performance parameters like noise margin, propagation delay and power consumption has been done between the proposed GAAFET and dual gate FinFET (DG FinFET) based applications, which establishes the performance improvement in GAAFET based designs.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Moore law states that the number of transistors in an Integrated Circuit (IC) will be doubled in every two years. So to carry forward the legacy of Moore, the semiconductor industry scaled the transistor in order to increase the transistor densities in ICs. CMOS scaling and short channel effects shares the cause and effect phenomenon. The major challenges faced in the continuous scaling of MOSFETs, specially for feature size in Nano-meter regime, are the dopant fluctuation, hot electron effect, carrier velocity saturation, Drain Induced Barrier Lowering (DIBL), subthreshold leakage and vertical gate insulator tunnelling [1]. These are termed as short channel effects (SCEs). In short geometry devices, the drain voltage influence the behaviour of electric field and hence the gate loses control over the channel. This effect is known as drain induced barrier lowering (DIBL). Due to which gate is unable to avoid the current flows in cut off mode also known as the off current in the device. Therefore, in order to eliminate these effects, several new architectures of transistors have been proposed and FinFET is one of those. As compared to the planar transistors, the gate of the FinFET is warped around the channel such as double gate FinFET and tri-gate FinFET. This improves the electrostatic control of the gate over the channel from several sides. Hence, it reduces the SCEs like leakage current and DIBL etc.

In 1989, a double gate silicon-on-insulator (SOI) structure was fabricated also termed as fully depleted lean channel transistor (DELTA). It was the first reported FinFET like structure. In the planar MOSFET, the channel position is horizontal while in FinFET, the channel position is vertical. Hence the height of the channel determines the width of the fin known as width quantization property. Trigate FETs, a variant of FinFETs, have the third gate on top of the fin which yields in low leakage current compared to double gate FinFETs. It also has less source to gate capacitance compared to the double gate FinFETs due to the additional current conduction at the top but it has increased parasitic resistance which is unfavourable. FinFETs provide relief to the ICs from power consumption, performance area and also boost carrier mobility. The technology preferred in structuring

the FinFET device is either bulk or SOI. But SOI is preferred over the bult due to various advantages which are discussed in next chapter. Physically, tri-gate FinFET is part of the multi-gate FET family, which includes FinFET and GAA (gate all around) devices. With respect to thicknesses of the fin, gate-all-around (GAAFETs) made of nanowires (NWs) produces relaxed channel dimensions while providing similar command over short channel effects. On the contrary, vertical GAAFETs are less constrained on channel length and thickness of the spacer as they are aligned vertically and thus exhibits even better scalability. The GAAFET structure delivers enhanced on current and low leakage current which can be observed in I-V characteristics. Now-a-days, most of the semiconductor industries are working on GAAFET due to the better gate controllability over the channel in the nanometre regime below 10 nm.

1.2 Technology CAD (TCAD) Tool

Visual TCAD is a graphical user interface for device simulator Genius. One can design the various structure of MOSFETs using this tool. This tool is capable of performing all types of device simulation like 2D and 3D, SPICE circuit simulation and mixed device/circuit simulation. TCAD plays a very important role in the process of designing new transistors technology in nanometre regime. These are 2D or 3D simulation tools based on finite element methods, where the electrical parameters of the fabricated devices like leakage current, threshold voltage, delay and power consumption can be evaluated based on the physical mechanisms of the processing or electrical mechanism in the device. With the help of Genius simulator, users are able to routinely simulate circuit cells like logic gates, 6T SRAM, latch and flip-flop, and expect 10 fold reduction in simulation run times. The tool consists of the following modules :

1. Drawing tool for device structures

2. Circuit schematic tool

3. GUI simulation controller

4. Visualization tool of simulation results

5. Spreadsheet

6. X-Y plotting tool

1.3 Objective

The main objectives of this project are to —

(i) Design 28 nm double gate FinFET and GAAFET and present their performance comparison.

(ii) Propose digital applications of FinFET device and GAAFET device and present their performance comparison.

1.4 Organization of Report

In this report the performance of 28 nm n-channel GAAFET structure is compared with 28 nm n-channel DG FinFET structure and performance comparison of GAAFET and DG FinFET based applications has also been presented. Rest of the report is organised as follows: the introduction of FinFET device and GAAFET device along with the history of technology is presented in chapter 1, detail discussion of FinFET device is presented in chapter 2, fabrication of FinFET is presented in chapter 3 and its application is presented in chapter 4. The detail discussion on GAAFET device and device physics is presented in chapter 5, fabrication of GAAFET is presented in chapter 6 and its application is presented in chapter 7 which is followed by the conclusion in chapter 8.

CHAPTER 2

FINFET DEVICE

The relentless downscaling of planar MOSFETs since past few decades has produced increased transistor density and better performance to integrated circuits (ICs) [1][2]. However, carrying this tradition in the nanometre regime is very difficult due to the excessive increase in the off-current current also termed as subthreshold leakage current. In the conventional MOSFET, as the length of the channel decreases, the gate loses command over the channel which is undesirable. Below 100 nm gate length, the CMOS designs are restrained severely due to lateral short channel effects and vertical gate insulator tunnelling. One of the solutions to overcome the gate tunnelling limitation is to change structure of the transistor in such a way that MOSFET channel length can be scaled down even with thicker oxide. It can be done using a variant of MOSFET structures which permit the scaling of a FETs beyond conventional MOS scaling limit [4][5][6]. So to diminish the short channel effects, FinFETs (Fin Based Field Effect Transistor) devices were introduced. FinFETs are, a variant of Multiple-Gate Field-Effect Transistors (MGFETs) and preferred over the conventional MOSFETs because it demonstrates better screening of the drain voltage from the channel due to the presence of additional gate to the channel leads to higher gate to channel capacitance. In short channel devices, performance metrics such as drain induced barrier lowering (DIBL), subthreshold slope (S), and threshold voltage roll-off are better in MGFETs compared to planar MOSFETs. Hence, it implies minute degradation in the transistor's threshold voltage (V_{th}) with decreasing gate length, which in turn implies low off-current [2][4].

FinFET has a quasi-planar structure, in which the drain and source regions are grown over a thin layer of insulator. Hence, it's generally called as a silicon-on-insulator (SOI) device. The channel connecting the drain and source region is known as fin. The parameters of the fin like thickness and height play an important role in the electrical characteristics of the device [1][3]. FinFETs with the two gates wrapped around the vertical channel are known as double gate (DG) FinFET and FinFETs with three gates wrapped around the vertical channel are known as Tri-gate FETs. The three dimensional structure of the FINFET is shown in Fig. 2.1.

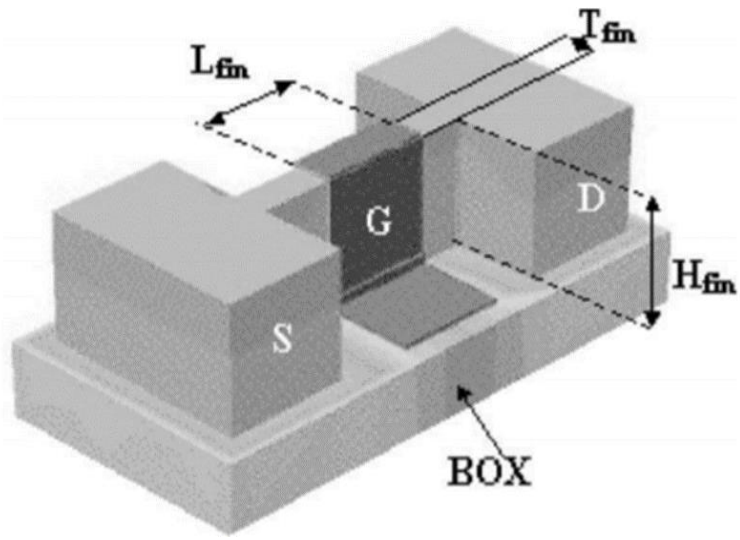


Fig. 2.1 FinFET Structure [3]

FinFET has an unique property named as width quantization, according to which the height of the fin will determine the width of the fin. It implies that the widths can be increased by using multiple fins. In the following sub-section, two different MOS structures are discussed, namely SOI FinFET and bulk FinFET. The main motive of both the structures is to maximize the capacitance between the gate and channel and minimize the capacitance between the drain and channel.

2.1 SOI and Bulk FinFET

SOI stands for Silicon On Insulator. In this technology, the conventional silicon substrates is replaced with a layered silicon–insulator–silicon substrate in semiconductor fabrication and manufacturing. The distinction between the SOI FinFET structure and conventional FinFET structure is that SOI device has a buried oxide (BOX) layer, which separates the body from the silicon substrate, that results into unwanted parasitic effects between the diffused source and substrate and also between the drain and the substrate. So, the parasitic capacitance of the junction is reduced to negligible amount. Small parasitic capacitance of the device, results in increased speed [8][9]. Therefore, the performance of the device is enhanced. The procedure of fabrication of SOI FinFET is similar to bulk FinFET (conventional FinFET) process except for the processing step of silicon substrate [8]. Buried oxide layer, will block the creation of a low impedance path between power supply and ground due to the

formation of the parasitic PNP FinFET and NPN FinFET in a bulk FinFET process. Therefore there will not be any unwanted leakage paths, and this leads to lower power consumption. These FinFETs can form a PNPN latch with positive feedback and virtually short-circuit the power supply to ground in the absence of buried oxide layer, thus causing huge flow of current which results in permanent device damage. For better construction of the device FinFETs based on bulk are opted while the SOI FinFET is a more probable option when it comes to less variability and also due to the easy control over the height and width of the fin. A high channel doping density is required to control the SCEs in bulk architecture, which leads to large transversal electric fields and undesired deterioration in the mobility of electron [6]. Fig. 2.2 shows the constructional difference between SOI and Bulk FinFET.

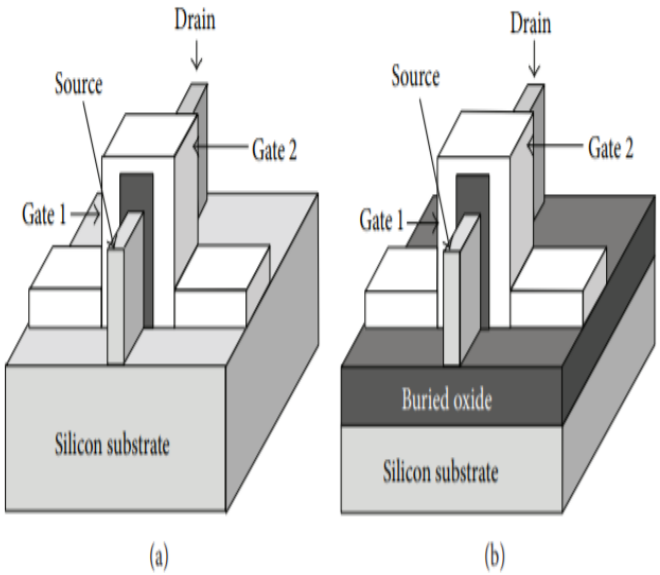


Fig. 2.2 Structural comparison between (a) bulk FinFET and (b) SOI FinFET [2]

2.1.1 Advantages of SOI Devices Compared to Bulk Devices

1. Due to buried oxide layer isolation, the parasitic capacitances of the drain and source regions are reduced. Therefore, the dynamic power consumption and delay of the device is lower compared to conventional CMOS.
2. The threshold voltage of device is less dependent on back gate bias compared to bulk CMOS. Hence, for low power applications SOI devices are more suitable.
3. Sub-threshold behaviour of SOI devices are better than conventional MOSFETS, hence less leakage current.

4. No latch-up problems in SOI devices due to substrate isolation and also it occupies lesser area for fabrication.
5. Switching speed of SOI devices are much higher compared to bulk CMOS [8].

2.1.2 Disadvantages of SOI Devices compared to Bulk Devices

1. The threshold voltage of the device changes due to the floating body in partially depleted SOI and this will result in mismatch between the two identical transistor.
2. Self-heating is another issue in SOI devices. The power does not dissipate easily which result in high body temperature. Hence mobility and current decreases.

2.2 FinFET Orientation

Fabrication of the FinFET can be performed with their channel along different directions in a single die. This concept of orientation will have a huge impact on mobility of the charge carrier due to the different crystal orientation of the fin sidewalls and thereby result in a mobility boost [11][12]. With the use of a special orientation technique termed as hybrid orientation technology (HOT), the enhancement of mobility depending upon the crystal orientation has been observed in the planar CMOS technologies [13][14][15]. In case of planar MOSFETs, crystal plane other than ⟨100⟩ is very difficult to fabricate while the structuring of the FinFETs can be done along the ⟨110⟩ crystal plane as well. This increases the mobility of the hole. By twisting the layout of transistor with an angle of 45∘ in the ⟨100⟩ wafer plane, the FinFET oriented with crystal plane ⟨110⟩ can be fabricated. Hence, n-channel FinFETs implemented along ⟨100⟩ and p-channel FinFETs along ⟨110⟩ lead to faster logic gates [16][17][18].

2.3 FinFET Classification

The classification of FinFETs is done based on the number of gates surrounds the device, it can be double gate or trigate device. The double gate FinFETs are classified into two categories on the basis of gate connections [2]:

(1) Shorted-gate (SG) FinFET

(2) Independent-gate (IG) FinFET

2.3.1 Shorted Gate FinFET

The two gates are tied together in shorted gate FinFETs, referred as three terminal (3T) device. So the conventional bulk CMOS can be replaced with SG FinFETs. Thus, both gates of SG FinFETs are used together to control the electric field of the channel. Hence, it has higher on-current (I_{ON}) and also higher off-current (I_{OFF}) or the subthreshold leakage current) compared to independent gate FinFETs. It is further categorized based on asymmetries in their device parameters. Generally, both the front gate and back gate of a SG FinFET has same work function. However, it can also be made different. This leads to an asymmetric gate-work function.

2.3.2 Independent Gate FinFET

When both the gates of the FinFET are not connected physically then it's termed as an independent gate (IG) FinFET, hence a four terminal (4T) device. Different voltages or signals can be applied to their two isolated gates, in IG FinFETs. This allows the back-gate bias to modulate the front gate threshold voltage linearly. However, independent gate FinFETs occupies large area due to the requirement for placing two different gate contacts. The electrostatic coupling between the front and back gates is high due to the small thickness of the silicon fin. Hence the channel formation near the one gate is severely dependent on the state of the other gate of the device. Also, if the back-gate is turned off, no channel will be formed near the disabled gate and also it will increase the threshold voltage of the other gate of the IG FinFET.

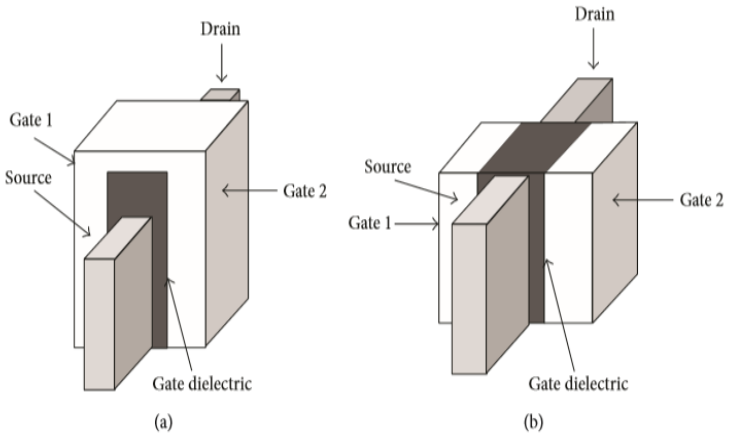


Fig. 2.3 Structural comparison between (a) SG FinFET and (b) IG FinFET [2]

Fig. 2.3 shows the structural comparison between the shorted gate (SG) FinFET and independent gate (IG) FinFET. So, we can conclude that the technology used for FinFET device is SOI as it has various advantages over the bulk FinFET. Also orientation plays an important role in structuring the device, so hybrid orientation technology (HOT) is preferred in which the orientation for holes and electrons are different to avoid the mobility degradation. Shorted gate (SG) FinFET and independent gate (IG) FinFET will be used depending upon the requirement of applications.

CHAPTER 3

FINFET FABRICATION

In this section, n-channel FinFET device with physical gate length of 28 nm is fabricated using Cogenda Visual TCAD tool. The fabrication steps mainly involves device drawing, labelling of regions, material filling, doping and mesh building. The structural parameters of 28 nm n-channel like the fin height and width, doping concentration of source and drain region and work function are mentioned in tabular form. The modelling of FinFET device is presented next which includes the threshold voltage and subthreshold leakage current equations. Also the characterization of 28 nm n-channel FinFET device is done through simulation at room temperature (300k). And the output characteristics and subthreshold graph is plotted and electrical parameters of the device are extracted.

3.1 Fabrication of FinFET

The FinFET is fabricated on silicon-on-insulator wafer with a modified planar CMOS mechanism. The channel of FinFET (also called as the fin) is positioned vertically. In double gate FinFETs, the channel height (*H*FIN) determines the width (*W*) of the FinFET. This property of FinFETs is known as quantization of width. In this case, the effective gate length of device is 28 nm and the height of the fin is 12 nm and thickness of the fin is 2 nm. The 2D view of 28 nm double gate FinFET device is shown in Fig 3.1.

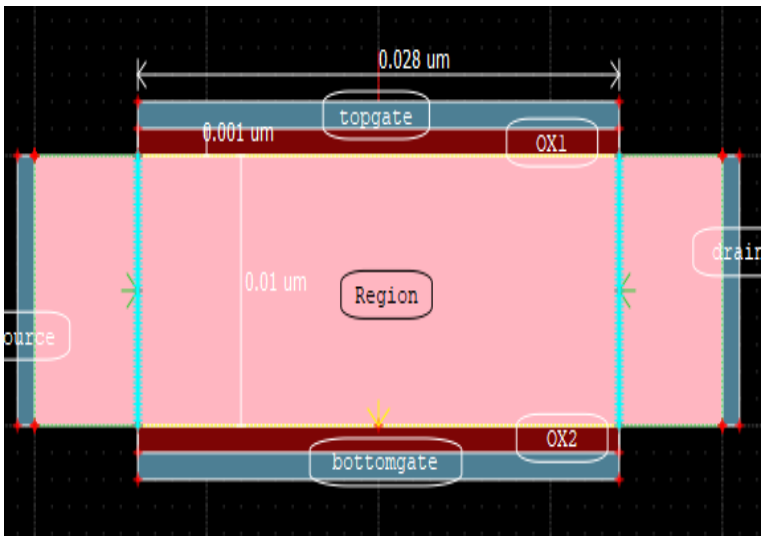


Fig. 3.1 Drawing of 28 nm n-channel FinFET

The region labelled as source, drain, substrate, top-gate, bottom-gate, and spacers are made of different materials. Nitride is used as spacers and silicon oxide as gate insulator (OX1/OX2). The front gate (top gate) and back gate (bottom gate) electrodes are comprises of NPolySi with gate contact having work function of 4.5 eV.

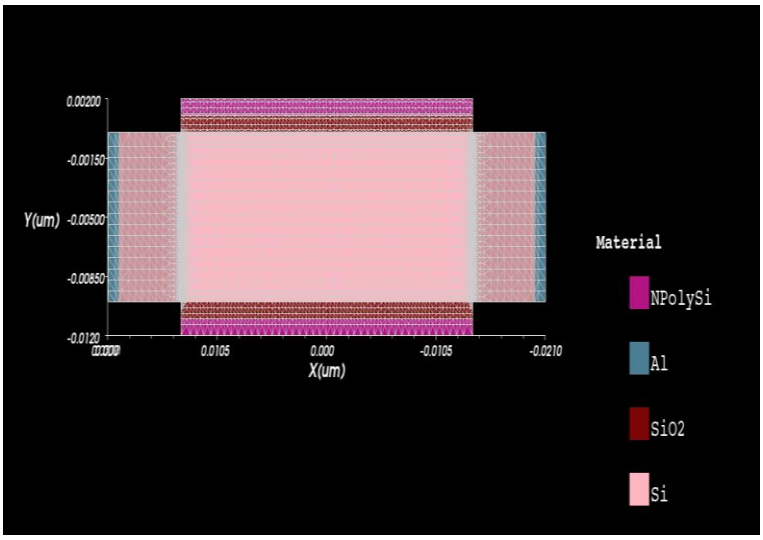


Fig. 3.2 Material used for FinFET fabrication

Fig. 3.2 shows the material used for the respective regions in the fabrication of FinFET. The source and drain regions are homogenous having ohmic contact with aluminum electrode . Table 3.1 shows the list of material used for the contrasting regions.

Table 3.1 FinFET region material and mesh size

Region	**Material**	**Mesh size(μm)**
Substrate	Silicon	0.001
Source/Drain	Aluminum	0.01
Topgate/Bottomgate	NPolySi	0.01
OX1/OX2	SiO2	0.005
Spacers(sp1,sp2,sp3,sp4)	Nitride	0.1

The source and drain region of the n-channel FinFET is heavily doped with 1×20 cm^{-3}. donor ions and the substrate region is lightly doped with 1×17 cm^{-3} acceptor ions. The type of doping profile used in the fabrication of device is Uniform doping profile. The concentration of the dopants in the entire region is homogeneous which implies that the electron density in the whole region will be uniform. The device performance mostly depends upon the doping concentration of the donor and acceptor regions. Fig. 3.3 and Fig. 3.4 shows the doping profile of the n-channel FinFET device.

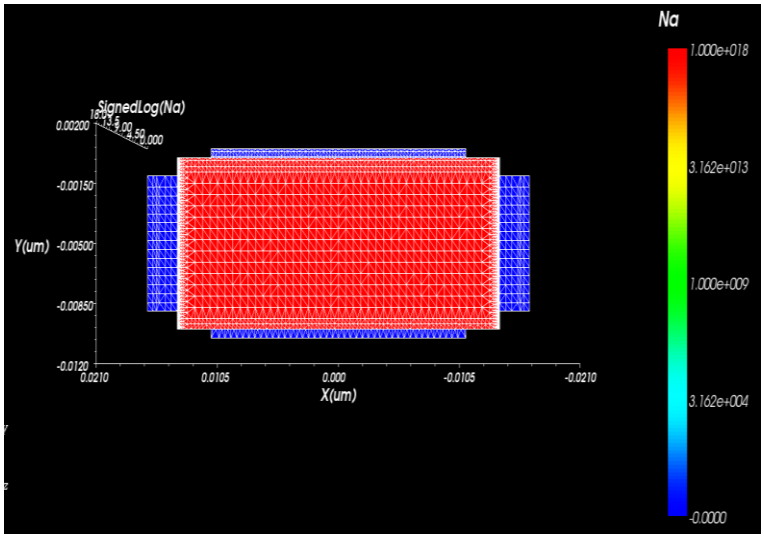


Fig 3.3 Acceptor doping profile of 28 nm n-channel FinFET

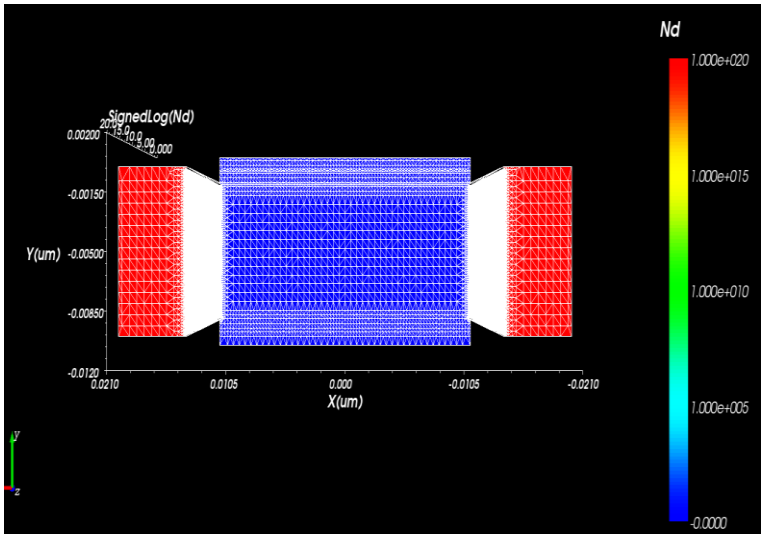


Fig. 3.4 Donor doping profile of 28 nm n-channel FinFET

Meshing is the last step in the fabrication of the device. Mesh is the most basic thing in Cogenda TCAD. A structure is defined in terms of location and spacing parameters in 2D/3D. The finer the meshing, simulation will take more time. In simple terms

meshing tells simulator the locations or points on structure at which it should calculate current and voltage parameters of device. The device simulator solves numerically the semiconductor equations in the regions. They are partial differential equations in the position and time. Fig 3.5 shows the cross section view of 28 nm meshed FinFET.

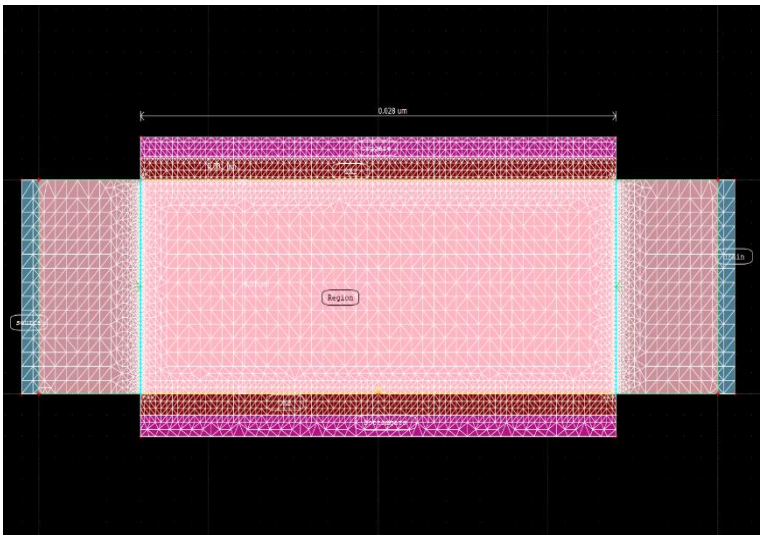


Fig. 3.5 Meshed FinFET

The structural parameters like dimension, doping concentration and work function for the designed 28 nm n-channel FinFET are summarised in Table 3.2.

Table 3.2 The structural parameters of 28 nm n-channel FinFET

Parameter	**Dimension**
Length of Source/Drain (nm)	10
Channel Length (nm)	28
Channel Height (nm)	12
Channel Thickness (nm)	2
Gate oxide thickness (nm)	1
Source/Drain Doping Concentration/(cm^3)	1×10^{20}
Channel Doping Concentration/(cm^3)	1×10^{17}
work function of gate contact	4.5eV

3.2 Mathematical Modelling for FinFET

In this sub-section, the mathematical modelling of the DG FinFET structure is done which includes the threshold voltage and the subthreshold current leakage equation described using the Poisson equation, as following [19];

3.2.1 Threshold Voltage Modelling

The threshold voltage of the DG FinFET is evaluated using the relation between the two coupled gates. The threshold voltage of the device mostly depend upon the difference in the work function between the gate and fin and also on the components of gate voltages. The equation is given as follows :

$$V_{th} = V_{FB} + \varphi_{s(inv)} - \frac{Q_b}{2C_{OX}} + \nabla V_{th}, Q_M \quad (3.1)$$

where V_{FB} represents voltage of the flat-band, $C_{s(inv)}$ represents potential of the surface at threshold, $\nabla V_{th}, Q_M$ represents increase in the threshold voltage due to the quantum mechanical effects, and Q_b is given as:

$$Q_b = qN_A T_{fin} \quad (3.2)$$

When considering the Q_M confinement of inversion layer carriers, V_{th} of equation (3.1) should be augmented with $\nabla V_{th}, Q_M$. The surface potential at threshold is given by:

$$\varphi_{s(inv)} = 2\,\varphi_b \quad (3.3)$$

$$\varphi_b = \frac{KT}{q} \ln \frac{N_A}{N_i} \quad (3.4)$$

The value of φ_b is substituted from equations (3.4) into equation (3.3) :

$$\varphi_{s(inv)} = 2\left(\frac{KT}{q} \ln \left(\frac{N_A}{N_i}\right)\right) \quad (3.5)$$

$\nabla V_{th}, Q_M$ is change in threshold voltage due to Q_M effects, which is given by Trivedi et al. (2003):

$$\nabla V_{th}, Q_M = \frac{S}{\frac{KT}{q} ln\,(10)} \text{ x } \frac{0.3763}{\frac{m_x}{m_l \cdot T_{fin}^2}} \quad (3.6)$$

where S represents the subthreshold swing (SS), T_{fin}^2 represents the thickness of fin and m_x/m_l is the ratio of the carrier effective mass in the direction of confinement to the free electron mass. The value of $\varphi_{s(inv)}$ from equation (3.5), Q_b from equation (3.2) and $\nabla V_{th}, Q_M$ from equation (3.6) is substituted into the expression of threshold voltage (3.1). So, the equation for the threshold voltage of device is given as:

$$V_{th} = V_{FB} + 2\left(\frac{KT}{q} \ln\left(\frac{N_A}{N_i}\right)\right) - \frac{(KT/q)\, ln\left(\frac{N_A}{N_i}\right)}{2\ C_{ox}} + \frac{S}{\left(\frac{KT}{q}\right) ln\,(10)} \times \frac{0.3763}{\frac{(m_x}{m_l)} T_{fin}^2} \quad (3.7)$$

3.2.2 Subthreshold Leakage Current Modelling

When the magnitude of V_{GS} (gate voltage) is less than V_{th} (threshold voltage) of the device, the MOSFET works in weak inversion (subthreshold) region. In this region, conduction of current between the source and the channel is mainly due to carrier diffusion also known as subthreshold leakage current. The I_{sub} is a function of gate length and width of the fin. In long geometry devices, the I_{sub} is less due to the reduced DIBL and SCEs. On the contrary, subthreshold current increases as the width of the fin increases. It's because thinner body allows gates to better control the electrostatic of the channel reducing short channel effects. Hence, while modelling the equation, effect of both temperature and device parameters like width and length of fin should be noticed carefully. The expression of the I_{sub} for DG FinFET structure is given as—

$$I_{sub} = 2\ \frac{W_{fin}}{L_{gate}}\ C_g \mu_{eff}(E_y)\left(\frac{(KT)^2}{q^2}\right) e^{\left(-\frac{qV_{th}}{sKT}\right)} \quad (3.8)$$

where $C_g = \frac{\varepsilon_{ox}}{t_{ox}}$ represents the gate capacitance per unit area, $\mu_{eff}(E_y)$ represents transverse electric field dependent effective mobility, q represents the charge of electron, T represents absolute temperature and k represents Boltzmann constant, S represents subthreshold swing factor and V_{th} represents threshold voltage of the device. It can be noticed that the subthreshold leakage current (I_{sub}) depends on the temperature and threshold voltage exponentially.

3.3 FinFET Device Characterization

The various ways of characterizing 28 nm n-channel FinFET device through simulation is discussed in detailed here. The transfer characteristics of the FinFET devices are similar to the characteristics of MOSFET. The steady state analysis of FinFET is realized by basic drift diffusion equation method. The $I_d - V_d$ characteristic curves are simulated at room temperature (300K) for heat transfer coefficient of 1KW/K/cm2. The drain characteristics of the n-channel FinFET device are depicted in Fig 3.6. The supply voltage (V_{DD}) is considered to be 1 V. The drain voltage (V_{DS}) is swept from 0 to 1 V and drain current (I_D) of the device is calculated at different gate voltages (V_{GS}). It is observed that the drain current of device increases linearly then shows constant current behaviour. The drain characteristics of n-channel FinFET device mainly consist of three regions namely- cut-off region, linear region and saturation region. The maximum drain current of device is 0.33 mA at gate voltage equal to 1v .

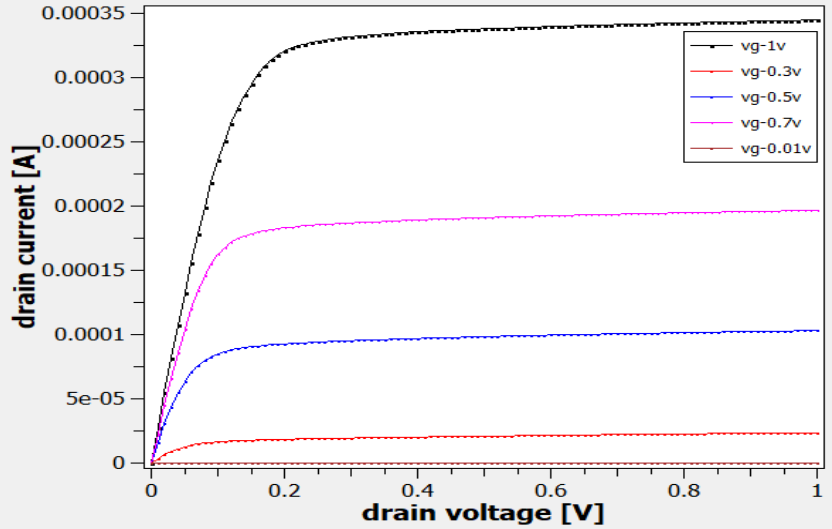
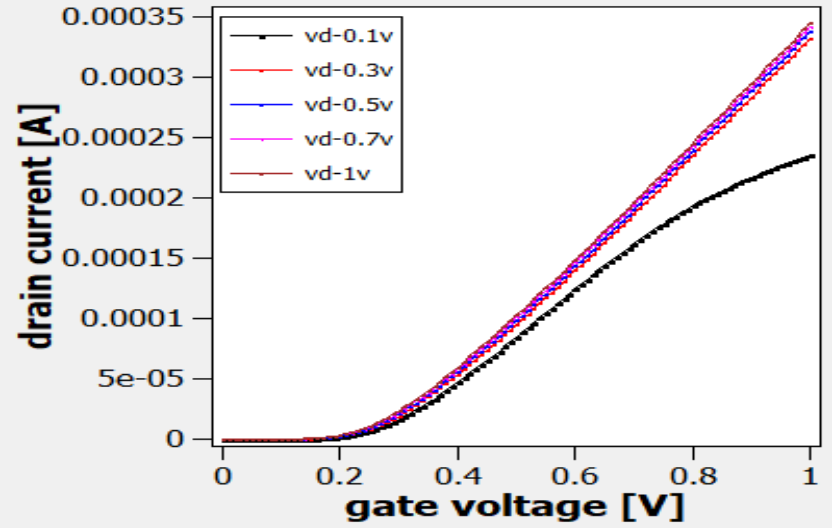


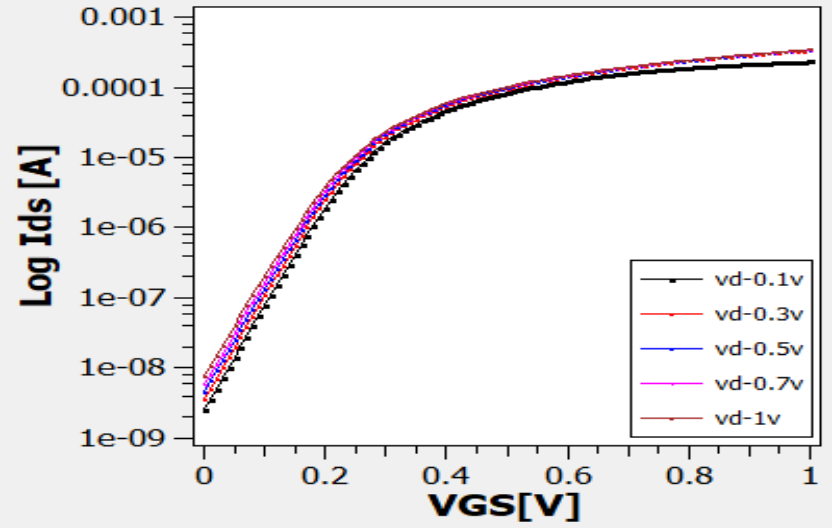
Fig. 3.6 $I_d - V_d$ characteristics of 28 nm n-channel FinFET

The I_D versus V_{GS} graph for different V_{DS} values is shown in Fig. 3.7(a) wherein the gate voltage (V_{GS}) is swept from 0 to 1V and drain current of the device is computed at different drain voltages. The drain current obtained at $V_{GS} = V_{DS} = V_{DD}$ is termed as I_{ON} and is measured from simulation as 0.33 mA. The same plots in log-scale to illustrate the sub-threshold behaviour of the 28 nm n-channel FinFET is depicted in Fig. 3.7(b). It may be observed that the log (I_D) shows linear behaviour for V_{GS} values < 0.272 V thereby confirming the exponential relation with V_{GS} in sub-

threshold region. This region illustrates how fast the device switches between ON and OFF states and is used to determine the sub-threshold swing.



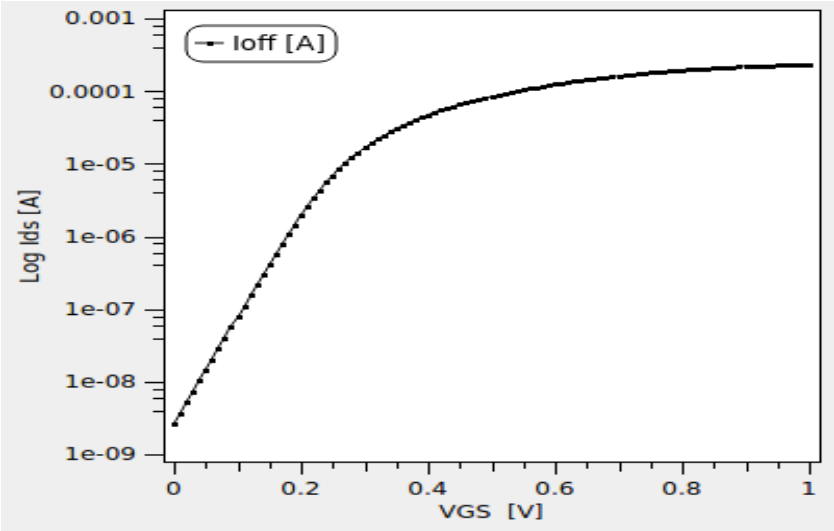
(a)



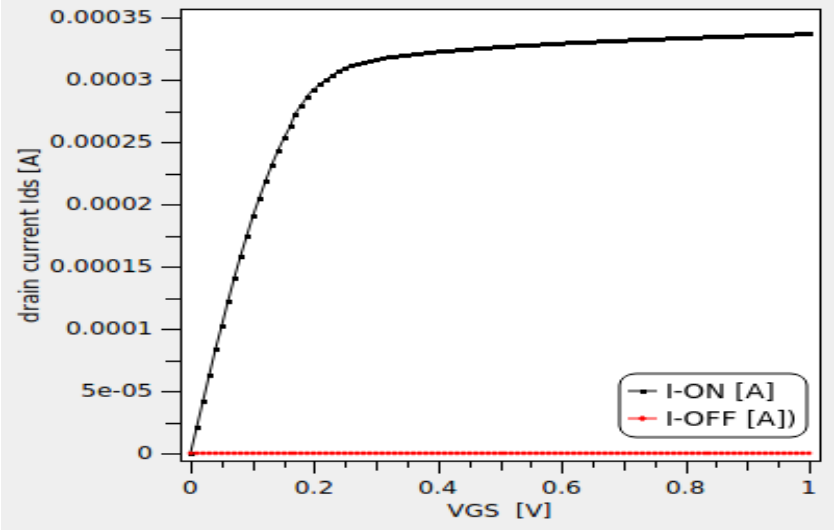
(b)

Fig. 3.7 (a) The I_D versus V_{GS} graph and (b) The I_D versus V_{GS} graph on logarithmic scale

Theoretically the I_{OFF} is the drain current measured at $V_{GS} = 0$ and $V_{DS} = V_{DD}$. For simulation the I_{OFF} is measured at $V_{GS} = 0.0001$ V and it value is observed as 1.42 nA as shown in Fig 3.8 (a). The I_{OFF} is almost negligible as compared to I_{ON} as is depicted in Fig 3.8 (b).



(a)



(b)

Fig. 3.8 (a) The I_{OFF} measurement and (b) The I_{ON} and I_{OFF} current plots w.r.t. V_{GS}

It can be observed from the plot that the subthreshold leakage current, also known as off current is in nanoampere range, which is quite less than the off current in MOSFETs. Therefore power consumption in FinFET devices are less than the MOSFETs. Hence, FinFETs are better alternative for short channel applications compared to MOSFETs. The device electrical parameters of designed 28 nm n-channel DG FinFET like on current, off current, threshold voltage, DIBL, subthreshold swing obtained from simulations are summarised in Table 3.3

Table 3.3 Electrical parameters of 28 nm n-channel DG FinFET

Parameters	**DG FinFET**
I_{OFF}	1.4 nA
I_{ON}	0.33 mA
Switching ratio (I_{ON}/I_{OFF})	0.23×10^{6}
$V_{th}(V_{DDlow})$	0.272v
V_{th} (V_{DD})	0.247 v
DIBL	38.4 mV/V
Sub-threshold swing (V_{DDlow})	66.83 mV/dec
Sub-threshold swing (V_{DD})	67.43 mV/dec

CHAPTER 4

APPLICATIONS OF FINFET

Combinational gate circuits are one of the most important parts of digital system. The performance of such devices are usually analysed by measuring their operational parameters like switching speed in terms of propagation delay and power consumption. [20]. In this section, the applications of DG FinFET devices namely- resistive load inverter, CMOS FinFET inverter and NAND gate are presented. All the devices are having identical physical parameters and doping concentration is kept same. The work function of n-channel and p-channel FinFET are 4.5eV and 4.97eV respectively. The comparison of performance of both the inverter is done by plotting the voltage transfer characteristics and evaluating noise margin.

4.1 Resistive Load Inverter

Generally, in the inverter circuit an enhancement-type n-channel MOSFET act as the driver device which is replaced by n-channel FinFET in this circuit. The load consists of a simple linear resistor, R of 30k ohm. The power supply voltage provided to the circuit is 1v. The input to the resistive load inverter is pulse with the rise and fall time of 1ns. The basic circuit of the resistive-load inverter circuit is shown in Fig. 4.1

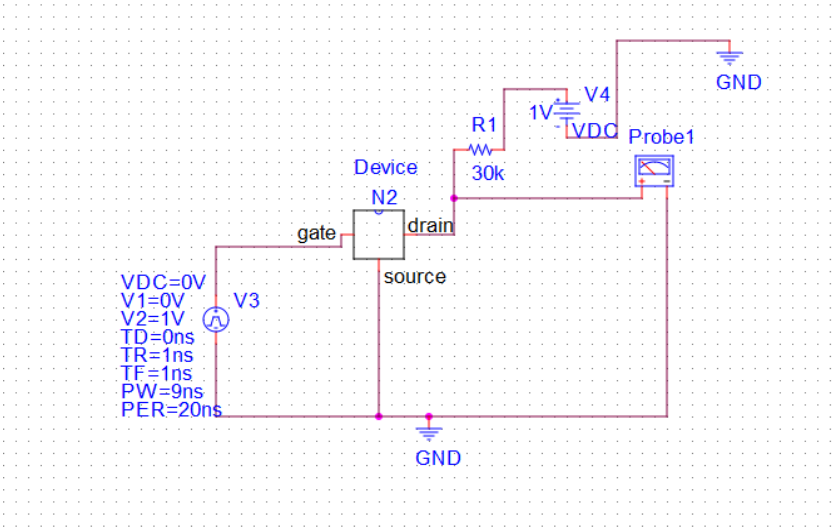


Fig. 4.1 Resistive load inverter circuit

The drain current (I_{ds}) of the FinFET is equal to load current (I_r), in the steady state operation. As the short channel effects in FinFET is almost negligible, there will be no channel length modulation effect. The source and substrate electrodes of the FinFET is grounded, hence the voltage of source is equal to zero. If input voltage is less than threshold voltage, the FinFET is in cut-off mode, so no current will flow. As V_{in} increases beyond V_{th}, the FinFET starts conducting a nonzero current. So the FinFET is in saturation region initially, since its drain voltage (V_{ds}) is larger than V_{dsat} which is smaller than half (V_{DD}). With increasing V_{in}, the I_{ds} of the device increases and the V_{OUT} begins to drop. Eventually, for V_{in} larger than sum of the output voltage and threshold voltage, the FinFET enters the linear operation region.

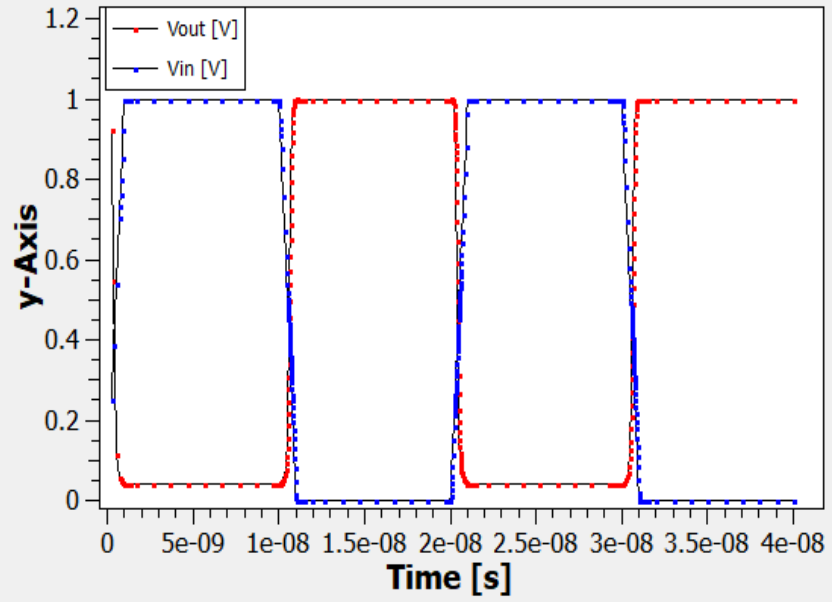


Fig. 4.2 Output of Resistive load inverter

The transient simulation plot of the resistive load inverter circuit is shown in Fig. 4.2. When the n-channel FinFET is in cut off mode the output of the circuit is logic 1 and when the n-channel FinFET device conducts the output is logic 0. The analysis of the circuit is done by identifying the various operating regions of the driver transistor under steady state conditions. Fig 4.3 shows the VTC of a typical resistive load inverter circuit, indicating the operating modes of the driver transistor and the critical voltages points.

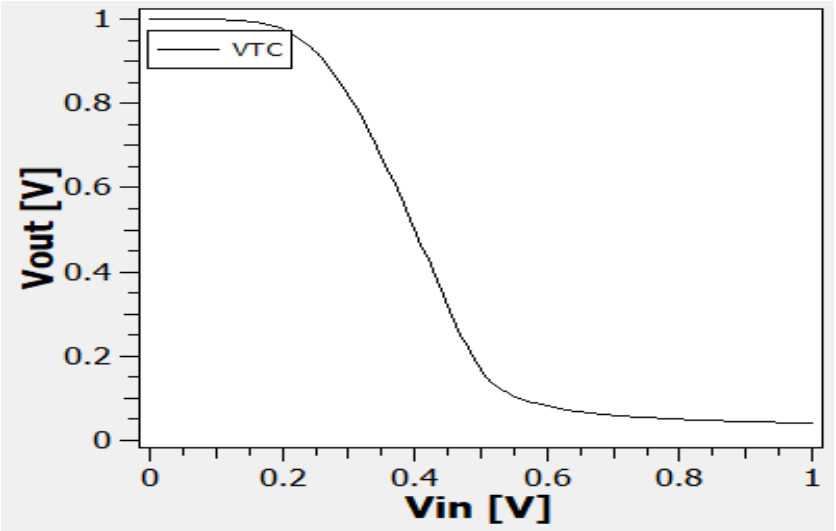


Fig. 4.3 VTC of resistive load inverter

When the input voltage is less than threshold voltage (V_{th}), the inverter works in cut off region. At $V_{in} = V_{out}$, the inverter works in saturation region and when $V_{in} = V_{out} + V_{th}$, the inverter enters into linear region. The various operating regions of the driver transistor and the corresponding the range of input voltages are listed in Table 4.1.

Table 4.1 Operating regions of driver transistor

Input voltage range	**Operating mode**
Vin < 0.27 v	Cut off
0.28 v < Vin < 0.5 v	Saturation
Vin > 0.5 v	Linear

The threshold voltage of the resistive load inverter is 0.4V and at this point the transistor is in saturation mode. It can be observed from the voltage transfer characteristics of the resistive load inverter that the transition region is wide which implies that the switching speed of the inverter is slow. Also, the output low logic level and high logic level are not symmetric so the noise margin of the inverter has logic levels of unequal width. The load resistor occupies large area which is unfavourable in short channel applications. Hence the resistive load inverter is not preferred.

4.2 DG FinFET Based Inverter

To fabricate the DG FinFET based inverter using visual TCAD, the same fabrication steps of 28 nm n-channel FinFET are followed. It consists of one n-channel FinFET and one p-channel FinFET which are drawn adjacent to each other with the gap of 8 nm, filled with silicon oxide as spacer, to provide the electrical isolation between the two devices. Both the devices are identical in dimensions as shown in Fig. 4.4. The front gate and back gate electrodes of n-channel FinFET device are comprises of n-type polysilicon while p-channel FinFET comprises of p-type polysilicon with the gate contact having work function of 4.5eV and 4.97eV respectively. In n-channel FinFET, the concentration of the donor ions in the source and drain region is 1×20 cm^{-3} and the channel is lightly doped with 1×17 cm^{-3} acceptor ions.

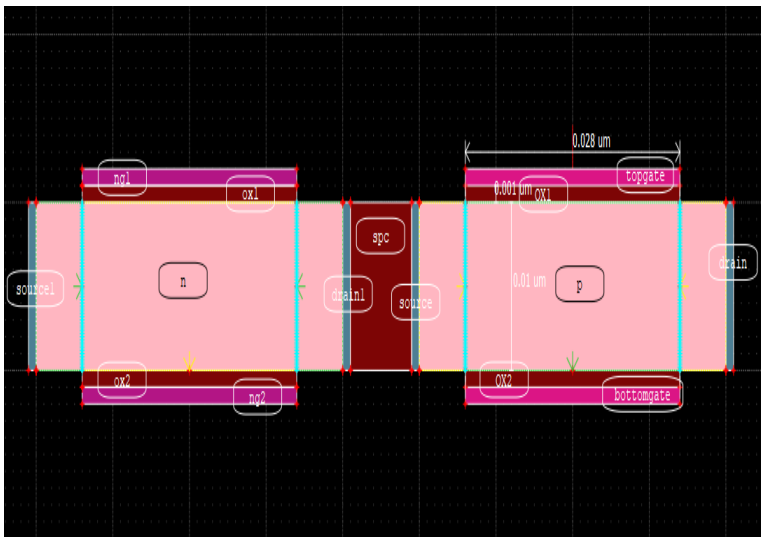


Fig 4.4 Cross section view of DG FinFET based inverter

While in p-channel FinFET device the concentration of acceptor ions in the source and drain region is 1×20 cm^{-3} and the channel is lightly doped with 1×17 cm^{-3} of donor ions. The type of doping profile used in the fabrication of device is Uniform doping profile. Hence the concentration of the dopants is homogeneous which implies that the carrier density will be uniform in the entire region. The device performance mostly depends upon the doping concentration of the donor and acceptor regions. The mesh size for the source and drain region is 0.1 μm and for the substrate region is 0.001 μm for both the n-channel FinFET and p-channel FinFET devices. Fig 4.5 shows the cross section view of meshed DG FinFET based inverter.

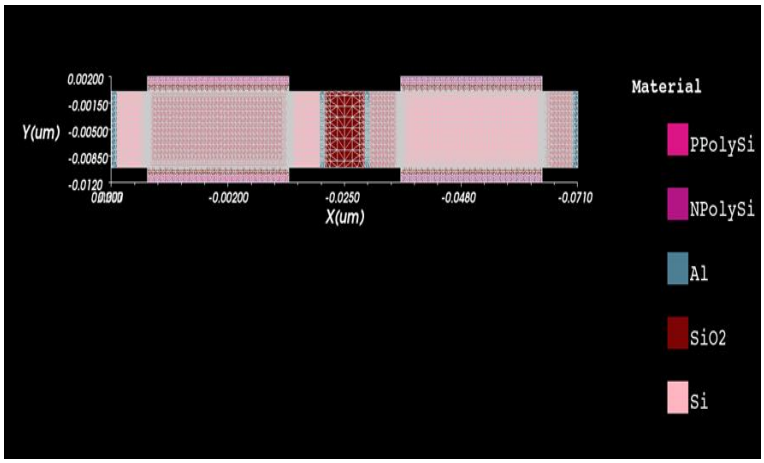


Fig 4.5 Meshed DG FinFET based inverter

The schematic of DG FinFET based inverter is shown in the Fig 4.6. Interconnection of circuit has been done according to the general CMOS inverter circuit. The threshold voltage of the FinFET inverter is 0.272 V and supply voltage provided to the circuit is 1V. The input pulse is common to both the gates having rise and fall time of 1ns.

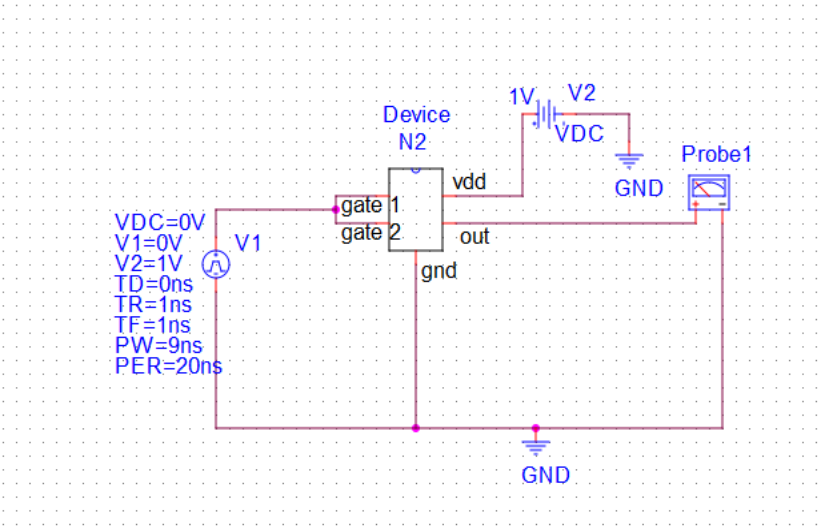


Fig 4.6 Schematic of FinFET Inverter

Fig. 4.7 shows the transient simulation plot of the DG FinFET based inverter circuit. When the n-channel FinFET device is in cut-off mode, the output of the circuit is logic 1 as the current flows through p-channel FinFET device and output node charges up to V_{DD} and when the n-channel FinFET device conducts the output node is at logic 0 as all the charge passes to ground.

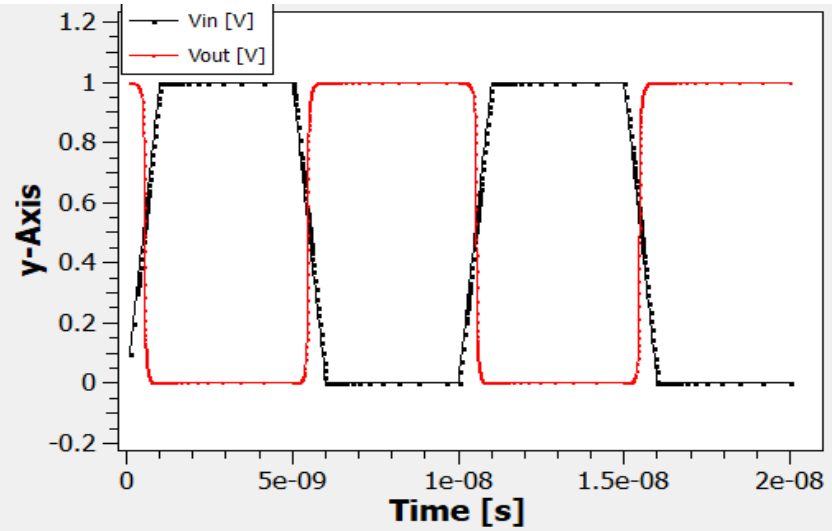


Fig 4.7 Transient simulation plot of DG FinFET based inverter

Fig 4.8 shows the voltage transfer characteristics of a Complementary FinFET inverter circuit, indicating the operating modes of the n-channel FinFET and p-channel FinFET and the critical voltages points on the VTC. In the region, where input voltage is less than $V_{T,n}$, the n-channel FinFET device is in cut off mode and the output voltage is equal to V_{dd} and when the input voltage is more than $V_{dd} + V_{T,p}$, the p-channel FinFET is in cut off mode. The transition period of the DG FinFET based inverter is quite sharp compared to resistive load inverter which implies the wide noise margin and hence better performance.

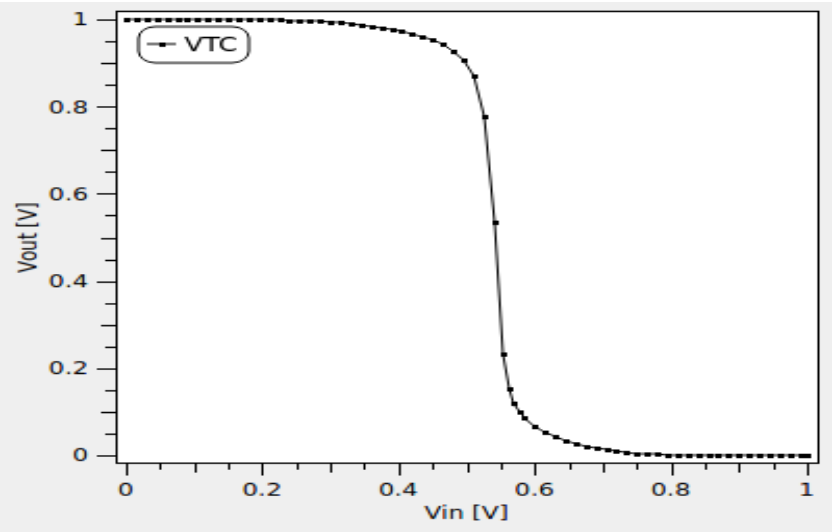


Fig. 4.8 VTC of FinFET inverter

Table 4.2 list the various operating modes of the DG FinFET based inverter corresponding to the input ranges.

Table 4.2 Operating regions of n-channel and p-channel FinFETs

Input voltage range	**n-channel FinFET**	**p-channel FinFET**
Vin< 0.27v	Cut-off	Linear
0.28v< Vin<4.8v	Saturation	Linear
4.9v<Vin<0.59v	Saturation	Saturation
0.6v<Vin<0.8v	Linear	Saturation
Vin>0.8v	Linear	Cut-off

The two critical voltage points on the curve are maximum input voltage (V_{IL}) interpreted as logic 0 and minimum input voltage (V_{IH}), interpreted as logic 1 where the slope of the VTC becomes equal to -1 ($i.e\ \frac{\partial V_{out}}{\partial V_{in}} = -1$). And the inverter threshold voltage is defined as the point where $V_{in} = V_{out}$ which is also termed as the transition voltage, on the VTC curve [21]. In this case, the switching threshold voltage of the DG FinFET based inverter is 0.55 V.

4.2.1 Noise Margin calculation

The Noise margin (NM) is a measure of noise immunity of a circuit. Increased NM indicates higher noise immunity [1][18]. The noise margin for low signal levels (NM_L) and noise margin for high signal levels (NM_H) are given as:

$$NM_L = V_{IL} - V_{OL} \tag{4.1}$$

$$NM_H = V_{OH} - V_{IH} \tag{4.2}$$

where V_{OH} is maximum output voltage when the output level is logic 1 and V_{OL} is minimum output voltage when the output level is logic 0. The parameters like V_{OL}, V_{OH}, V_{IH}, V_{IL}, NM_H, NM_L are required to compute noise margin and transition region (TR) and are tabulated for the resistive load inverter and DG FinFET based Inverter circuit in Table 4.3 for V_{DD} = 1V and Vin = 1V.

Table 4.3 Noise Margin of resistive load inverter and DG FinFET based Inverter

Parameter	**Resistive Load Inverter**	**DG FinFET Based Inverter**
V_{IL} (V)	0.275	0.446
V_{IH} (V)	0.500	0.547
NM_L (mV)	273	445
NM_H (mV)	500	453
TR(mV)	227	100

The transition region in the resistor load inverter is much more than the transition region in DG FinFET based inverter. Therefore the noise margin of DG FinFET based inverter is better than the resistive load inverter. Hence DG FinFET based inverter is fast.

4.3 DG FinFET Based NAND GATE

The DG FinFET based NAND gate consists of two n-channel and two p-channel GAAFETs and is designed following the same structuring steps as used in inverter design. The fabrication materials for n-channel and p-channel GAAFETs are kept same as used in inverter circuit. Uniform doping profile is used for all the devices. In n-channel FinFET, the concentration of the donor ions in source/drain region is 1×20 cm^{-3} and the channel is lightly doped with 1×17 cm^{-3} acceptor ions. While in p-channel FinFET the concentration of acceptor ions in source and drain region is 1×20 cm^{-3} and the substrate region is lightly doped with 1×17 cm^{-3} of donor ions. All the four devices are separated by 10 nm spacer to provide electrical isolation. The gate and source/drain electrodes of n-channel GAAFET and p-channel GAAFET are comprises of aluminium metal having

work function of 4.5eV and 4.97eV respectively. The designed DG FinFET based NAND structure is shown in Fig. 4.9 and the schematic of DG FinFET based NAND gate is shown in Fig. 4.10.

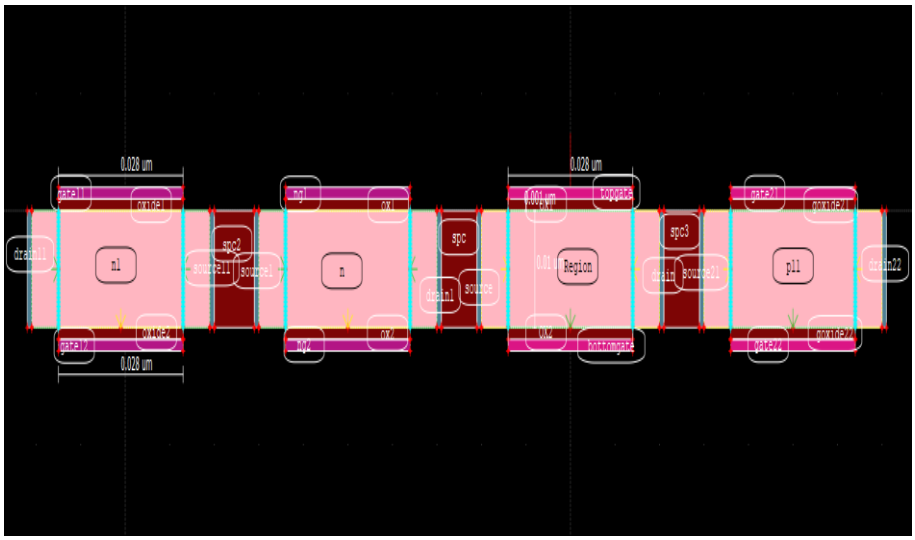


Fig 4.9 cross section view of DG FinFET based NAND gate

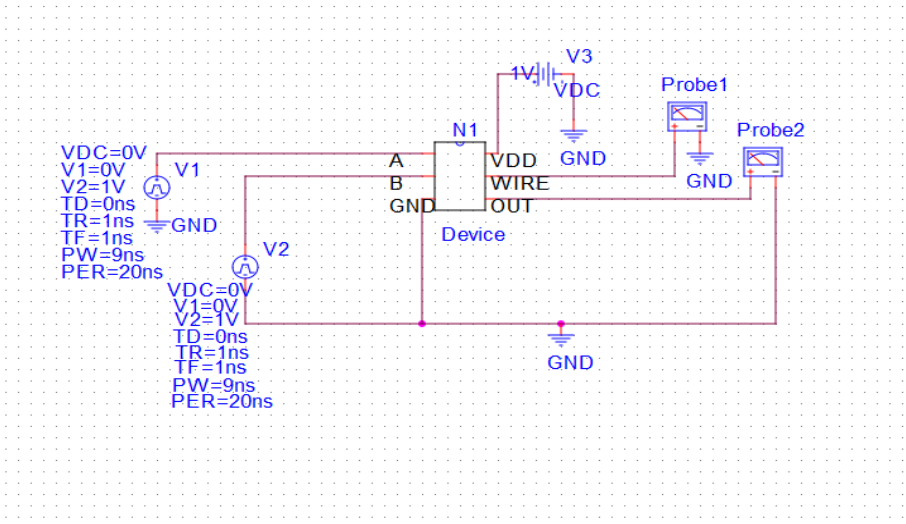


Fig 4.10 Schematic of DG FinFET based NAND gate

The transient simulation plot of the DG FinFET based NAND gate is shown in Fig. 4.11. The simulation is done using poison's equation and drift diffusion method solver level 1 (DDML1) technique at room temperature (300K). The supply voltage used for the gate is 1V. Two input pulses namely V(A) and V(B), as shown in Fig. 4.11, are applied to two inputs of the gate. The input pulse characteristics like rise time and fall time is 1ns and pulse width is 4ns.

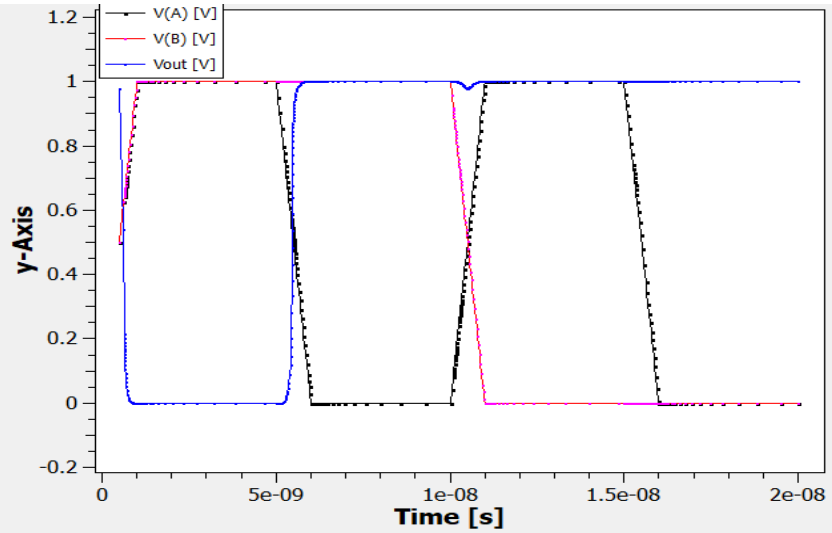


Fig. 4.11 Transient simulation plot of DG FinFET based NAND gate

The output of the NAND gate depicted as V_{out}, is high if either of the input or both are low (logic 0) while output of the logic gate is low when both the inputs are high (logic 1) thereby verifying the gate functionality.

CHAPTER-5

GAAFET DEVICE

Portable electronic equipments having wide range of functionalities with longer battery operation are need of the market. These requirements demand for downscaled CMOS processes which operate at lower supply voltages. However, due to the downscaling of devices the drain voltage also gets effective in controlling the channel region in addition to gate voltage. This leads to well-known short channel effects [21] such as carrier velocity saturation, drain induced barrier lowering (DIBL), sub-threshold leakage current etc. Thus for improved device performance the short channel effects need to be minimised. In literature several device structures have been proposed [22][23][24] to lower the short channel effects. The FinFET is one of the choices which is a quasi-planar structure where the source and the drain regions are grown over a layer of insulator and a narrow perpendicular fin is placed on the wafer [23][27]. The Source and drain are crosswise on both sides of fin. The conducting channel wraps around the fin. By increasing the number of gates such as double gate (DG), tri gate(TG) FinFET the device performance can be further improved. Much improved electrostatic control of the gate can be achieved with the use of gate all around field effect transistor (GAAFET) in which the insulating oxide and the gate electrode wraps around the channel material from all sides. Owing to its superior performance the GAAFET is being considered as the device of future and a variety of structures [25][26][28][29] have been reported in literature. Therefore, a n-channel GAAFET device with physical gate length of 28 nm is designed and its two applications namely an inverter and a NAND gate are presented thereafter. The GAAFET structure and the applications are designed using the Visual TCAD tool.

5.1 Device Physics

Following the trend of shrinking device dimensions, we have reached beyond 10 nm feature size. At this size, the quantum mechanics became dominant over classical mechanics. It became difficult to control these devices, and Quantum corrections must be considered for accurately simulating and modelling the behaviour of such devices. In current work, quantum effects were considered by selecting appropriate models and their calibrated parameters were used. All simulations were performed using

device simulator tool of Cogenda TCAD. Bohm Quantum Potential model (BQP), Energy balanced model for electrons (HCTE.EL), and Field dependent mobility model (FLDMOB) were used in all simulations to get accurate results [31]. Fermi-Dirac distribution instead of Boltzmann distribution was used for thermal equilibrium of carriers for initial guess. The physical device models used in the simulations are discussed below.

5.1.1 Bohm Quantum Potential Model

Quantum Potential models are originated from the hydrodynamic formation of the quantum mechanics. The concept of Quantum potential was first introduced by de Broglie and Madelung. Later Bohm further developed this model. These are then substituted back into the Schrodinger's equation to derive the following equations of motion for density (5.1) and phase (5.2).

$$\frac{\partial \rho(r,t)}{\partial t} + \nabla.(\rho(r,t)\frac{1}{m}\nabla S(r,t))) = 0 \quad (5.1)$$

$$-\frac{\partial s(r,t)}{\partial t} = \frac{1}{2m}[\nabla S(r,t)]^2 + \mathrm{V}(\mathrm{r},\mathrm{t}) + \mathrm{Q}(\rho,r,t) \quad (5.2)$$

where, $\rho(r,t) = R^2(r,t)$ is the probability density, Q is the Bohm Quantum Potential, V is potential term from Schrodinger equation and S is the solution of Hamiltonian-Jacobian equation. Equation 5.1 has the form of continuity equation. BQP model used in our simulation has two advantages over density gradient method. BQP equation is given as

$$Q = \frac{h^2}{2}\frac{\gamma\nabla(M^{-1}\nabla(n^{\alpha}))}{n^{\alpha}} \quad (5.3)$$

where, Alpha and gamma are two fitting parameters, $M^{-1}$is the inverse effective mass tensor and n is the electron (or hole) density.

5.1.2 Energy Balance Transport Model

Simple Drift-Diffusion transport model has the restriction of not introducing the energy (carrier temperature) as an independent variable which makes it less accurate for deep submicron devices and too high gradients. So, for these devices, a higher order solution of general Boltzmann's Transport Equations (BTE) is required. It is a higher order solution to the general BTE and consists of the current density to the carrier temperature

(or energy) model by introducing two new independent variables T_n and T_p, the carrier temperature for electrons and holes. The general expression of Energy Balance Transport Model for electrons is as follows [31]:

$$\text{div } S_n = \frac{1}{q} J_n \text{ E - } W_n - \frac{3K}{2} \frac{\partial}{\partial t} (\vartheta_n \text{ n } T_n) \quad (5.4)$$

$$J_n = \text{q } D_n \nabla n - \text{q } \mu_n \text{n } \nabla\varphi + q_n \, D_n^T \nabla T_n \quad (5.5)$$

$$S_n = -K_n \nabla T_n - \frac{K S_n}{q} J_n T_n \quad (5.6)$$

where T_n represent the electron temperature, J_n is current density, S_n is the flux of energy, μ_n represents the mobility of electron, D_n represent the electron's thermal diffusivity, W_n represents the loss rate for electron energy density, and K_n represents the electron's thermal conductivity.

5.2 Drift Diffusion Method Level 1

The drift diffusion method is used for the simulation of designed device. DDML1 is the basic solver of GENIUS code for constant lattice temperature. The main operation of level 1 drift diffusion method is to evaluate the set of partial differential equations of current and voltages, namely Poisson's equation, along with the continuity equations for electron and hole :

5.2.1 Poisson's Equation

The device simulator solves numerically the semiconductor equations in the regions of the device. They are partial differential equations in position and time. The Poisson's equation is given as :

$$\nabla . \varepsilon \nabla\varphi = -q(p - n + N_D^+ - N_A^-) \quad (5.7)$$

where, φ is the electrostatic potential, n and p represents the concentrations of the electron and hole, and N_D^+ and N_A^- are the ionized impurity concentrations, q represents the charge of an electron.

The relationship of conduction band E_c , valence band E_v and vacuum level φ is described in below equation:

$$E_c = -q\varphi - \gamma - \Delta E_c \quad (5.8)$$

$$E_v = E_c - E_g + \Delta E_v \quad (5.9)$$

Here, E_g represents bandgap of semiconductor, γ is the electron affinity. E_c and E_v represents the shift in the bandgap due to heavy doping.

Also, the relationship between intrinsic Fermi potential and vacuum level is given as :

$$\varphi = \varphi_{instrinsic} - \frac{\gamma}{q} - \frac{E_g}{2q} - \frac{K_b T}{2q} ln\ ln\ \frac{N_c}{N_v} \quad (5.10)$$

The reference 0 eV of energy is set to intrinsic Fermi level of equilibrium state in GENIUS.

5.2.2 Continuity Equations

The equations of continuity for electrons and holes in the semiconductor devices are given as follows:

$$\frac{\partial n}{\partial t} = \frac{1}{q} \nabla . J_n - (U - G) \quad (5.11)$$

$$\frac{\partial p}{\partial t} = \frac{1}{q} \nabla . J_p - (U - G) \quad (5.12)$$

where J_n and J_p represents the densities of electron and hole and $U\ and\ G$ represents the recombination and generation rates for both electrons and holes.

5.2.3 Drift Diffusion Current Equations

The current densities of electrons (J_n) and holes (J_p) are represented in terms of the DDML1 (level 1 drift diffusion model) here.

$$J_n = q\mu_n n E_n + q D_n \nabla n \quad (5.13)$$

$$J_p = q\mu_p p E_p + q D_p \nabla p \quad (5.14)$$

where μ_n and μ_p represents the mobilities of electron and hole. $D_n = \frac{K_b T}{q}\ \mu_n$ and $D_p = \frac{K_b T}{q}\ \mu_p$ represents electron and hole diffusivities, according to Einstein relationship.

5.2.4 Effective Electrical Field

E_n and E_p represents the effective driving electrical field to electrons and holes, which is related to the band diagram. The heterojunction band structure of has been considered here.

$$E_n = \frac{1}{q}\nabla E_C - \frac{K_b T}{q}\nabla(ln\,(N_c)\; - ln\,(T^{\frac{3}{2}})) \tag{5.15}$$

$$E_p = \frac{1}{q}\nabla E_v - \frac{K_b T}{q}\nabla(ln\,(N_v)\; - ln\,(T^{\frac{3}{2}})) \tag{5.16}$$

The drift-diffusion level 1 model is substituted into the current density expressions, and along with the Poisson's equation, to obtain the basic equations for DDML1 :

$$\frac{\partial n}{\partial t} = \nabla.(\mu_n\, nE_n + \mu_n\, \frac{K_b T}{q}\nabla n) - (U - G) \tag{5.17}$$

$$\frac{\partial p}{\partial t} = \nabla.(\mu_p\, pE_p + \mu_p\, \frac{K_b T}{q}\nabla p) - (U - G) \tag{5.18}$$

Hence, all the equations and methods for designed GAAFET device is discussed in this chapter which were used for simulation.

CHAPTER-6

GAAFET FABRICATION

The n-channel GAAFET with physical gate of 28 nm is designed using Cogenda TCAD in three steps namely meshing, material filling and doping which are carried out using python script. The 3D view of designed 28 nm GAAFET is shown in Fig. 6.1(a) and its cross sectional view is presented in Fig. 6.1(b) The Meshing is used to define a structure in terms of location and spacing parameters in 2D/3D.The structure is segmented into various regions depending upon the material to be filled in the particular sections of generated meshes. The silicon is used as dopant, silicon oxide as spacer and aluminium as metal contact in the device. The spacers are placed between the source and channel and also between the drain and channel for the electrical isolation.

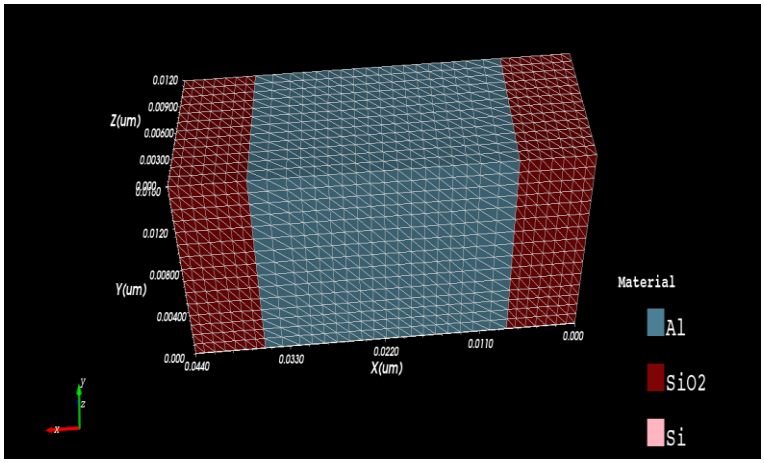


Fig. 6.1 (a) 3D View of GAAFET

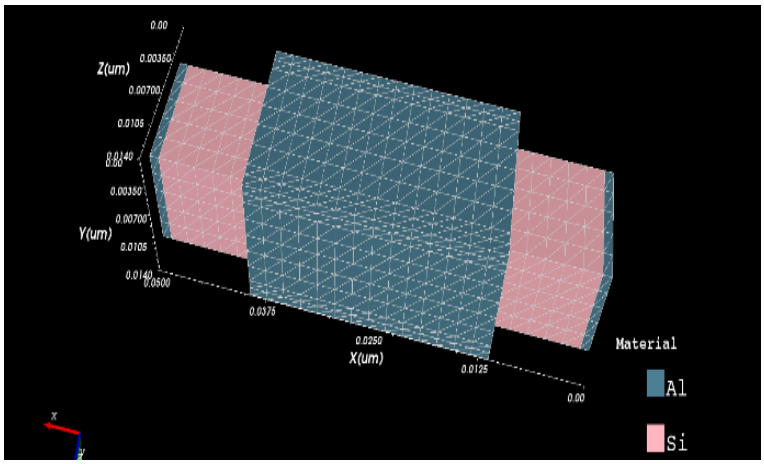
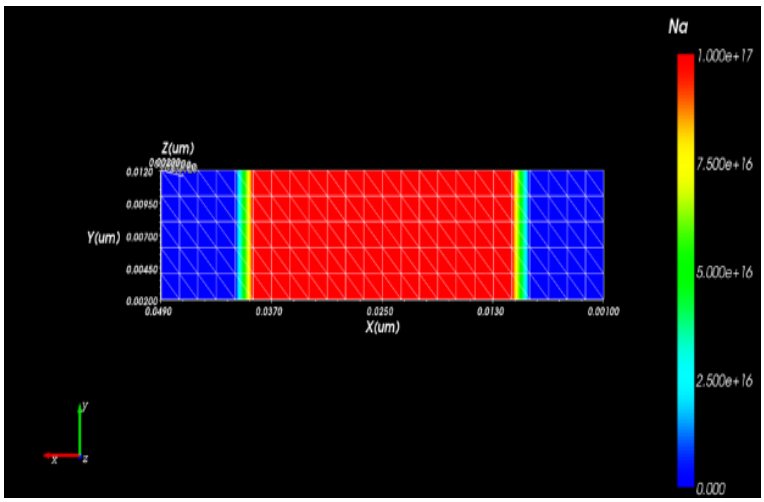
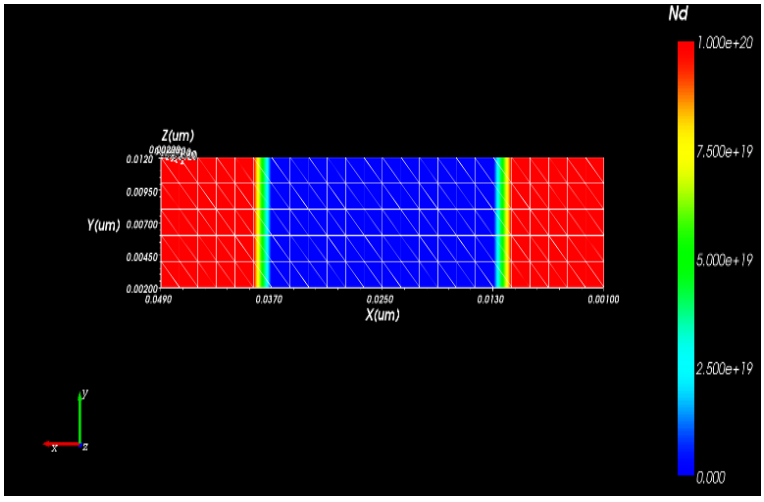


Fig. 6.1 (b) 3D View of source/drain region

Doping material of acceptor type is used for gate region while for source and drain and it is donor type. A uniform doping profile is used in all the regions as shown in Figs. 6.2 (a) and (b) respectively. The potential profile of the designed n-channel GAAFET is shown in Fig 6.3. The acceptor concentration in the channel region is $1\times17cm^{-3}$ and that of the donor atoms in the source and drain regions is $1\times20\ cm^{-3}$. The structural parameters for the designed n-channel GAAFET are summarised in Table 6.2.



(a)



(b)

Fig. 6.2 Concentration profile in (a) channel region and (b) source/drain region

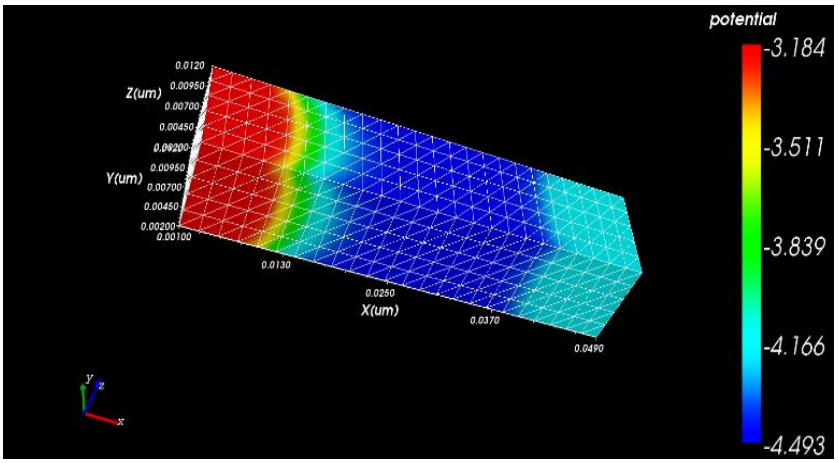


Fig. 6.3 GAAFET potential distribution profile

Table 6.1 The structural parameters of n-channel GAAFET

Parameter	Dimension
Length of Source/Drain (nm)	10
Channel Length (nm)	28
Channel Height (nm)	12
Channel Thickness (nm)	10
Gate oxide thickness (nm)	1
Source/Drain Doping Concentration/(cm^3)	1×10^{20}
Channel Doping Concentration/(cm^3)	1×10^{17}
work function of gate contact	4.5eV

6.1 Performance Parameters

It is well known that an n channel FET is considered to be in off state if the gate source voltage (V_{GS}) is less than threshold voltage (V_t). However, a leakage current termed as sub-threshold current can flow between source and drain under the condition $V_{GS} < V_t$. This sub-threshold current contributes towards device off current (I_{OFF}). In order to minimize the static power in a circuit the I_{OFF} should be as small as possible [21]. The approximate expression for sub threshold current is given by :

$$I_{d(subthreshold)=}\frac{qDnWx_Cn_0}{L_B}.e^{\frac{q\emptyset_r}{kT}}.e^{\frac{q\,(A.V_{GS}+B.V_{DS})}{kT}} \quad (6.1)$$

where, x_c is the subthreshold channel depth, D_n is the electron diffussion coefficient, L_B is the length of the barrier region in the channel, and $\emptyset_r$ is the reference potential. Thus the sub-threshold current has an exponential dependence on both the gate and drain voltages. The sub-threshold swing (SS) of a device is another performance parameter which determines the transition of a transistor from the ON to OFF state [21][23]. The sub-threshold swing is calculated at high drain voltage and also at low drain voltage. If the subthreshold swing is low, then it ensures better performance of device. Also the negligible amount of leakage current in the subthreshold region results in low power consumption of the device. It's the inverse of the slope of the voltage-current (V-I) characteristics in the sub-threshold region.

The DIBL is another important parameter to be evaluated for small geometry devices. The shift of threshold voltage due to increase in drain to source voltage (V_{DS}) from low to high voltage level is known as DIBL phenomena. Low DIBL indicates the better functioning of device. For short geometry devices, V_{DS} plays an important role in shifting of the threshold voltage due to modification in source to channel barrier height[21] [23]. The threshold voltage can be expressed by

$$V_T = \emptyset_{GC} - 2\emptyset_F - \frac{Q_B}{C_{ox}} - \frac{Q_{ox}}{C_{ox}} \quad (6.2)$$

where $\emptyset_{GC}$ represents the difference in work function between the gate and channel, $\emptyset_F$ is bulk potential, Q_{ox} represents positive charge density at gate oxide and silicon substrate interface and Q_B is depletion region charge in the substrate which is affected by V_{GS} and V_{DS} both. The DIBL in any device can be computed as

$$\text{DIBL} = \frac{V_{th}(V_{DDlow})-V_{th}\,(V_{DD})}{V_{DD}-V_{DDlow}} \quad (6.3)$$

Here, $V_{th}(V_{DDlow})$ represents the threshold voltage of device for lower V_{DDlow} while $V_{th}\,(V_{DD})$ represents threshold voltage for higher V_{DD}. A higher DIBL value in any device corresponds that gate terminal has less control over the channel region .

6.2 GAAFET Device Characterization

This section presents the characterization of n-channel GAAFET. The steady state analysis of 28 nm n-channel GAAFET is carried out using basic drift diffusion equation method. All simulations are done at room temperature (300K) settings and at heat transfer coefficient of 1KW/Kcm^2. The drain characteristics of the GAAFET device are depicted in Fig. 6.4. The supply voltage (V_{DD}) is considered to be 1 V. The drain voltage (V_{DS}) is swept from 0 to 1 V and drain current (I_D) of the device is calculated at different gate voltages (V_{GS}). It is observed that the drain current of device increases linearly then shows constant current behaviour.

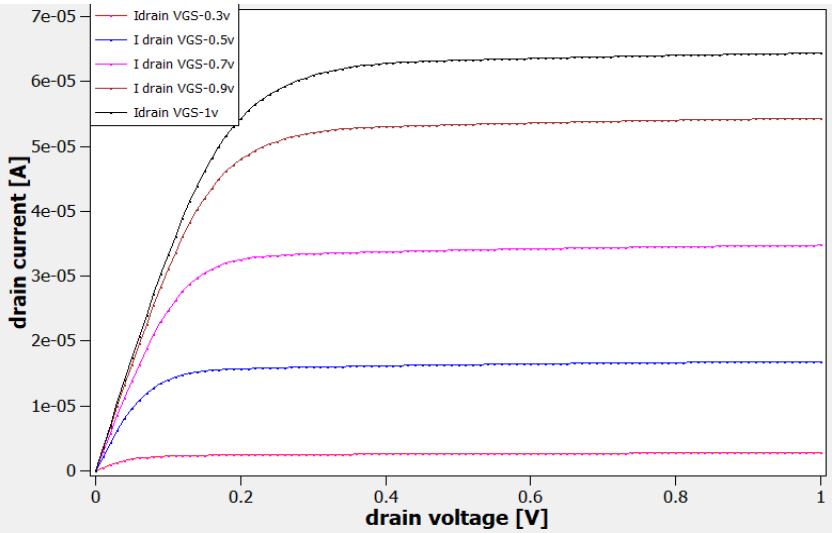
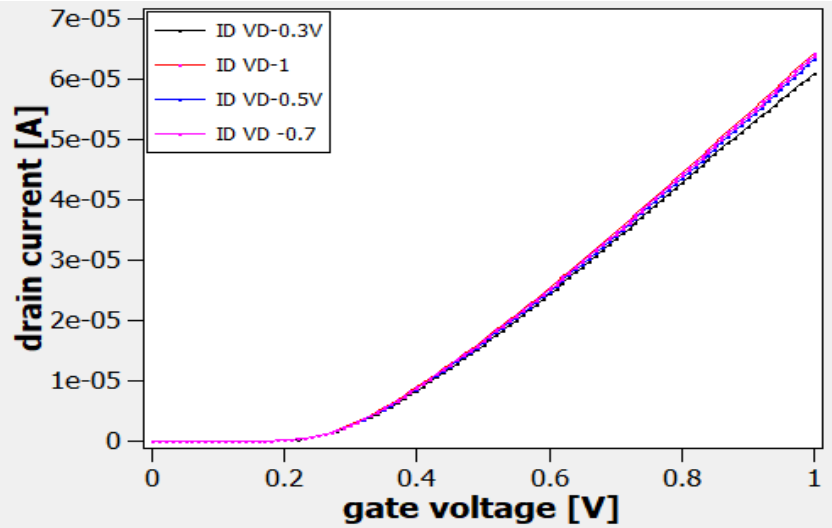
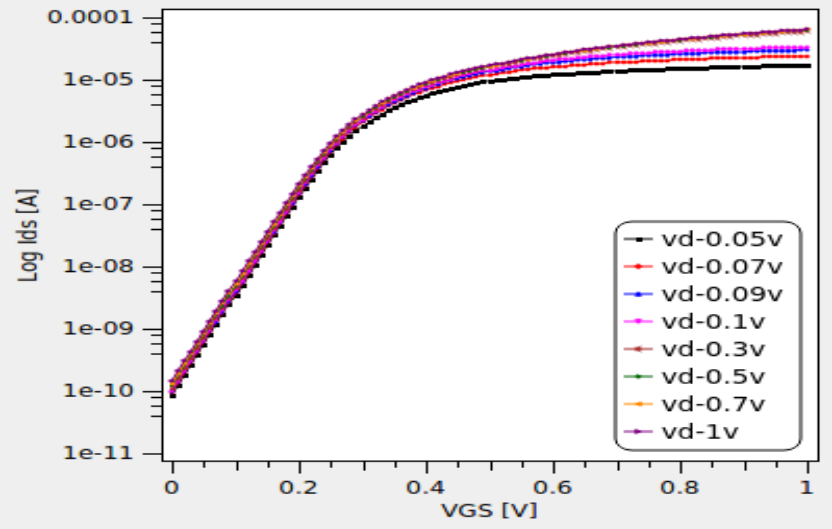


Fig. 6.4 Drain Characteristics of 28 nm n-channel GAAFET

The I_D versus V_{GS} graph for different V_{DS} values is shown in Fig. 6.5 (a) wherein the V_{GS} is swept from 0 to 1V and drain current of the device is computed at different drain voltages. The drain current obtained at $V_{GS} = V_{DS} = V_{DD}$ is termed as I_{ON} and is measured from simulation as 64.3 µA. The same plots in log-scale to illustrate the sub-threshold behaviour of the 28 nm n-channel GAAFET is depicted in Fig 6.5. (b) It may be observed that the log (I_D) shows linear behaviour for V_{GS} values < 0.167884 V thereby confirming the exponential relation with V_{GS} in sub-threshold region. This region illustrates how fast the device switches between ON and OFF states and is used to determine the sub-threshold swing.



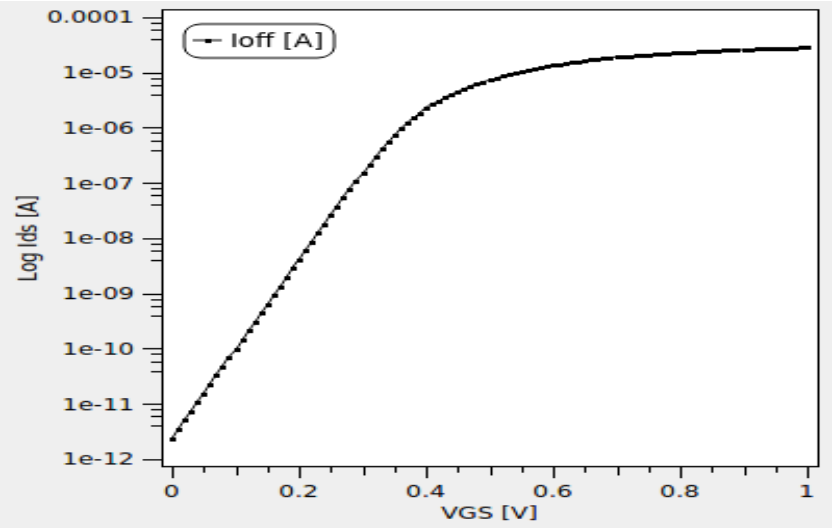
(a)



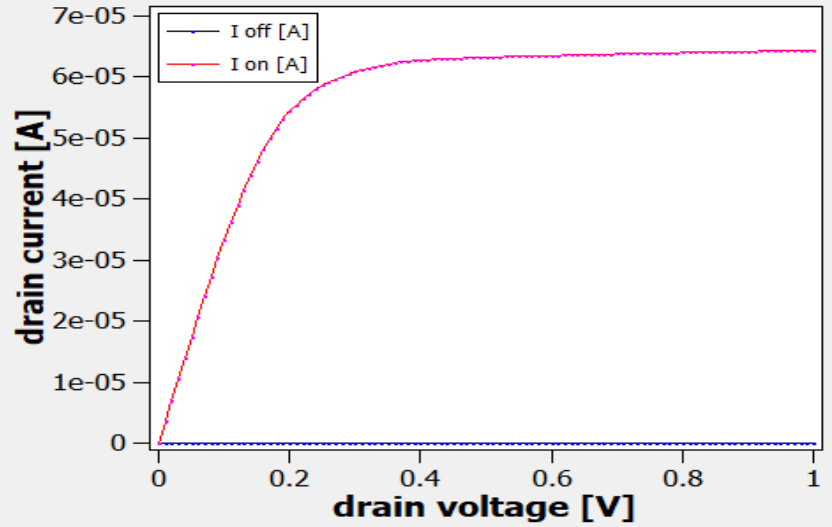
(b)

Fig. 6.5 (a) The I_D versus V_{GS} graph (b) The I_D versus V_{GS} graph on logarithmic scale

Theoretically the off-current (I_{OFF}) is the drain current measured at $V_{GS} = 0$ and $V_{DS} = V_{DD}$. For simulation purpose, the I_{OFF} is measured at $V_{GS} = 0.0001$ V and its value is observed as 1.42 pA as shown in Fig. 6.6 (a). The I_{OFF} is almost negligible as compared to I_{ON} as is depicted in Fig. 6.6 (b). Therefore, the switching ratio of the device will be better than the DG FinFET device. Hence, this makes the GAAFET device better alternative for low power digital applications.



(a)



(b)

Fig. 6.6 (a) The I_{OFF} measurement (b) The I_{ON} and I_{OFF} current plots w.r.t. V_{GS}

The device electrical parameters like I_{ON} , off-current (I_{OFF}) , threshold voltage , DIBL, subthreshold swing of designed 28 nm n-channel GAAFET obtained from simulations are summarised in Table 6.2. The supply voltage (V_{DD}) is taken as 1 V and V_{DDlow} is considered to be 0.1 V. The threshold voltage of the device is calculated at both linear ($i.e\ V_{DS} = V_{DDlow}$) and saturation region ($i.e\ V_{DS} = V_{DD}$), similarly the subthreshold swing of the device.

Table 6.2 Electrical parameters of 28 nm n-channel GAAFET

Parameters	**28 nm n-channel GAAFET**
I_{OFF}	1.42 pA
I_{ON}	64.3 µA
Switching ratio (I_{ON}/I_{OFF})	45.28×10^{6}
V_{th} (V_{DDlow})	0.168 V
V_{th} (V_{DD})	0.160 V
DIBL	8mV/V
Sub-threshold swing (V_{DDlow})	61.78 mV/dec
Sub-threshold swing (V_{DD})	61.89 mV/dec

CHAPTER 7

APPLICATIONS OF GAAFET

Combinational circuits are widely used in the digital applications. High speed, low power consumption and small chip area are the important design features of these digital circuits. Researchers explore at different levels of design abstraction such as circuit/gate/device level to meet these objectives. The use of GAAFET in designing digital circuits is an example of effort at device level. Therefore in this work two basic applications of GAAFET device namely an inverter and a NAND gate are presented which are designed using COGENDA Visual TCAD. The performance of GAAFET based designs has been compared with DG FinFET based designs to show the improved performance.

7.1 INVERTER

To design an inverter an n-channel and p-channel GAAFET are designed. A spacer of 10 nm is inserted between the n-channel and p-channel GAAFET for electrical isolation. The gate and source/drain electrodes of n-channel GAAFET and p-channel GAAFET are comprises of aluminium metal having work function of 4.5eV and 4.97eV respectively. A 3D view of designed inverter is shown in Fig. 7.1.

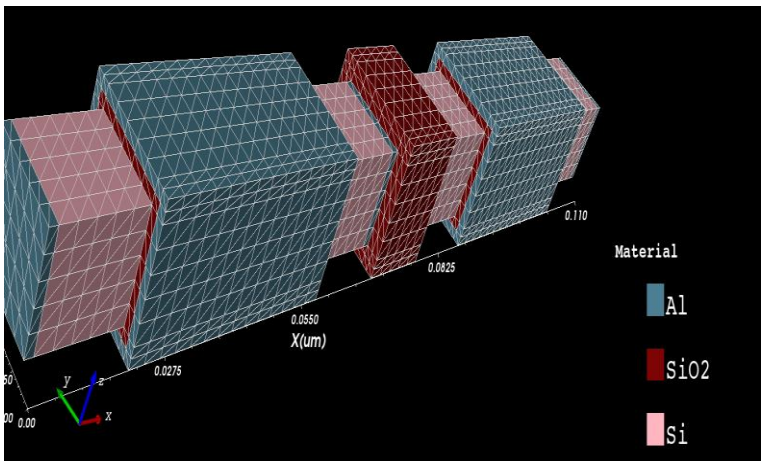


Fig. 7.1 The 3D view of designed GAAFET Inverter

Doping material of donor type is used for gate region while for source and drain acceptor type material is used with uniform doping profile for p-channel GAAFET. The

concentrations of the donor ions and acceptor ions for p-channel GAAFET are used as 1×20 cm^{-3} and 1×17cm^{-3} respectively. The potential distribution in GAAFET inverter is shown in Fig. 7.2.

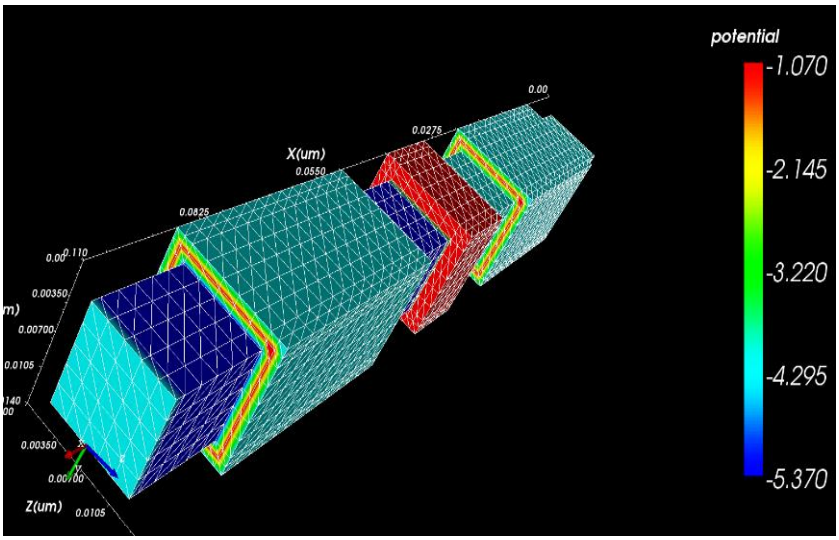


Fig. 7.2 Potential distribution profile of the designed GAAFET inverter

The $I_{DS} - V_{GS}$ characteristics of p-channel and n-channel GAAFET devices are combined to achieve the V_t matching plot. The drain voltages of both the devices are set to 1V and gates voltage are swept from 0 to 1V. The matched threshold voltages for n-channel and p-channel devices are shown in Fig. 7.3 which validates the dual work function metal (DWFM) integration scheme [29].

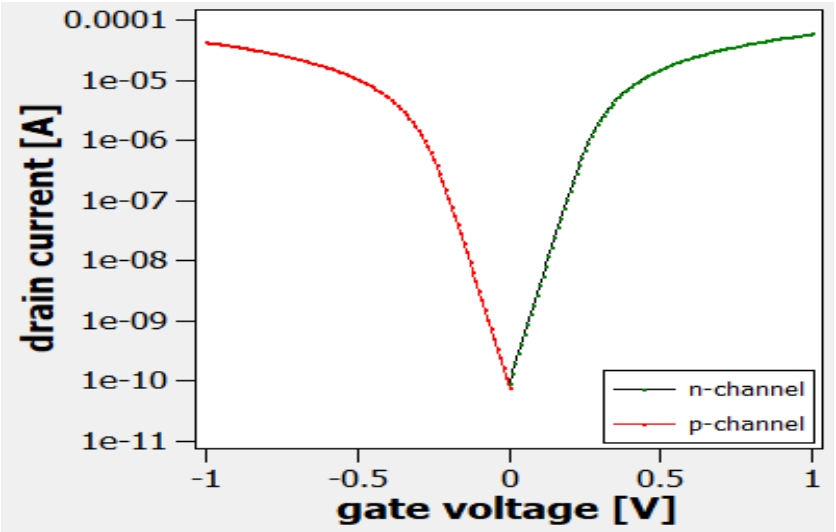


Fig. 7.3 The $I_{DS} - V_{GS}$ characteristics showing V_t matching of n-channel and p-channel GAAFETs

The voltage transfer characteristics (VTC) of the designed GAAFET inverter and DG FinFET based inverter are depicted in Fig. 7.4. It may be observed from the VTCs of both the devices that the transition period of the GAAFET inverter is sharper than DG FinFET based inverter which implies fast switching and hence high speed.

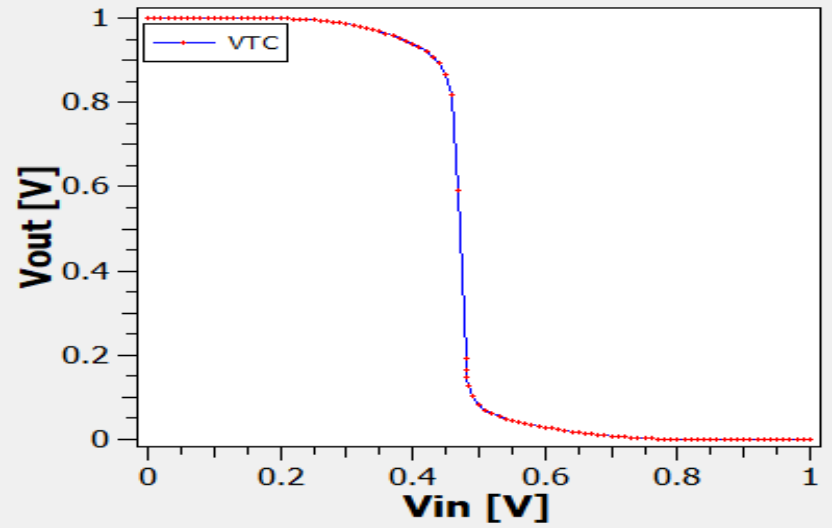


Fig. 7.4 The VTC of designed GAAFET Inverter

Maximum input voltage (V_{IL}) interpreted as logic 0 and minimum input voltage (V_{IH}), interpreted as logic 1 are the two critical points on this curve, where the slope of the VTC becomes equal to -1 ($i.e\ \frac{\partial V_{out}}{\partial V_{in}} = -1$). And the threshold voltage of the GAAFET inverter is defined as the point where $V_{in} = V_{out}$ on the VTC curve [21]. It is also called as transition voltage. In this case, the switching threshold voltage of the GAAFET inverter is 0.48 V.

7.1.1 Noise Margin calculation :

The Noise margin (NM) is a measure of noise immunity of a circuit. Increased NM indicates higher noise immunity [23][30]. The noise margin for low signal levels (NM_L) and noise margin for high signal levels (NM_H) are given as:

$$NM_L = V_{IL} - V_{OL} \tag{7.1}$$

$$NM_H = V_{OH} - V_{IH} \tag{7.2}$$

where V_{OH} is maximum output voltage when the output level is logic 1 and V_{OL} is minimum output voltage when the output level is logic 0. The parameters like $V_{OL}, V_{OH}, V_{IH}, V_{IL}, NM_H, NM_L$ required to compute noise margin and transition region (TR) are tabulated for the GAAFET inverter in Table 7.1 for V_{DD} = 1V and Vin = 1V. Transition region is defined as the region or space between the NM_H and NM_L.

Table 7.1 Noise margin of GAAFET Inverter

Parameters	**GAAFET Inverter**
V_{IL}(V)	0.429
V_{IH}(V)	0.505
NM_L(mV)	428.5
NM_H(mV)	485
TR(mV)	76

The transient simulation plot of the designed GAAFET inverter is presented in Fig. 7.5 The simulation is done using poison's equation and Drift diffusion method solver level 1 (DDML1) technique at room temperature (300K). The global doping scale is 1×20 cm^{-3} and mesh generated is of tetrahedral type for the simulator to evaluate the current and voltage in different points of the structure. The supply voltage (V_{DD}) used is 1V and input pulse is common to both the transistors. The input pulse characteristics like rise time and fall time is 1ns and pulse width is 4ns. When the n-channel GAAFET device is in cut-off mode, the output of the circuit is logic 1 and when the n-channel GAAFET device conducts the output node is at logic 0 as all the charge passes to ground through the n-channel GAAFET.

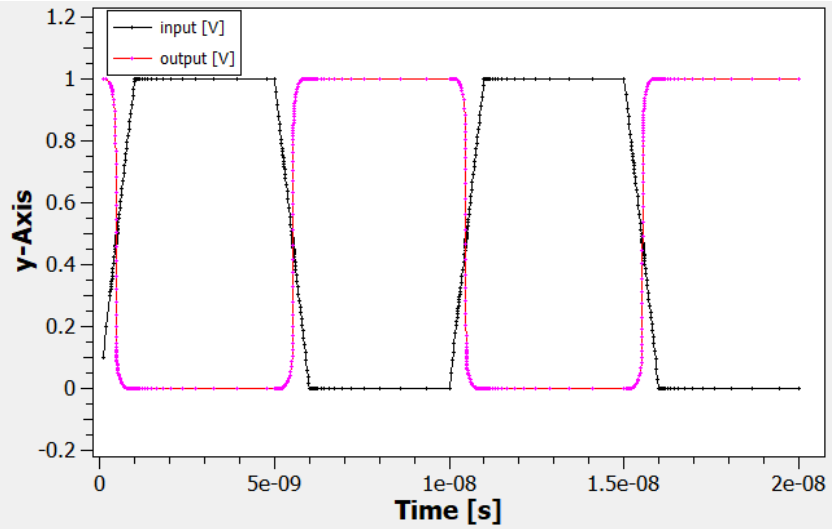


Fig. 7.5 Transient plots of GAAFET Inverter

7.2 NAND GATE

The NAND gate consists of two n-channel and two p-channel GAAFETs and is designed following the same structuring steps as used in inverter design. The doping materials and their concentration for n-channel and p-channel GAAFETs are kept same as used in inverter circuit. All the four devices are separated by 10 nm spacer to provide electrical isolation. The designed structure is shown in Fig 7.6 and the potential distribution in is depicted in Fig 7.7.

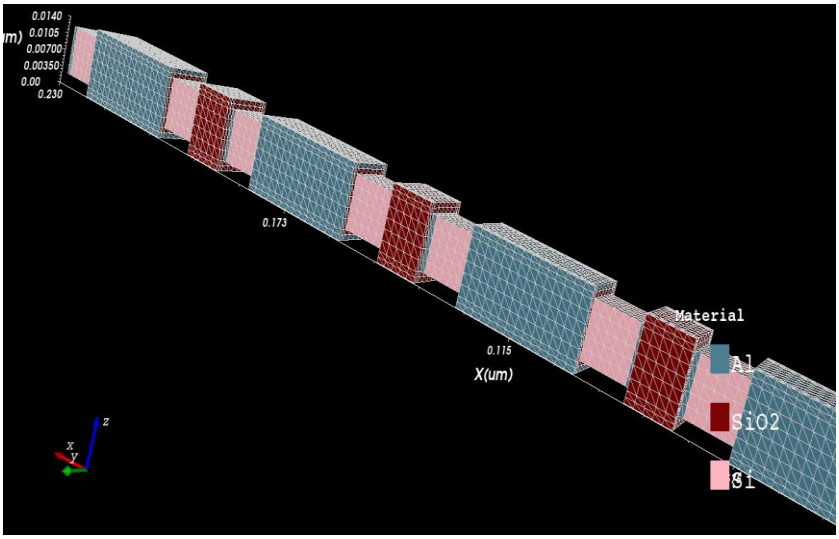


Fig. 7.6 3D view of GAAFET NAND gate

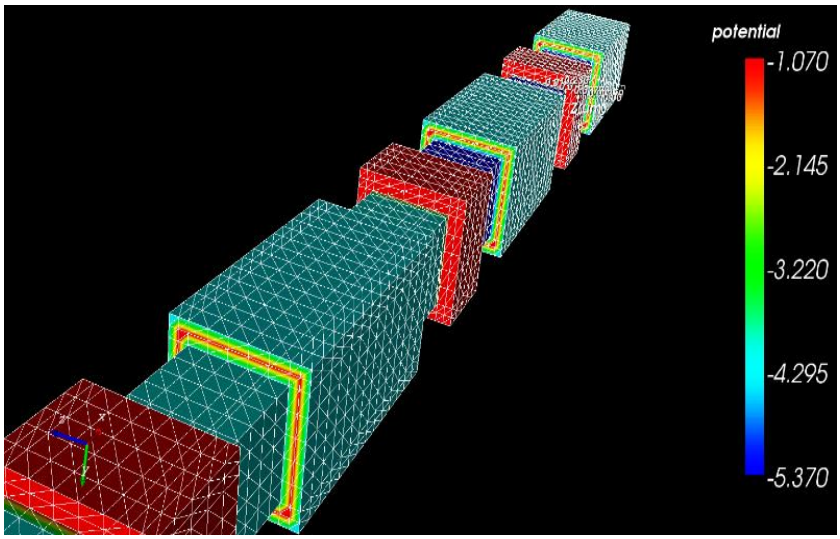


Fig. 7.7 Potential distribution in GAAFET NAND gate

The transient simulation plot of the GAAFET NAND gate is shown in Fig. 7.8. The simulation is done using poison's equation and drift diffusion method solver level 1 (DDML1) technique at room temperature (300K). The supply voltage used for the gate is 1V. Two input pulses namely V(A) and V(B), as shown in Fig. 7.8, are applied to two inputs of the gate. The output of the NAND gate depicted as V_{out}, is high if either of the input or both are low (logic 0) while output of the logic gate is low when both the inputs are high (logic 1) thereby verifying the gate functionality.

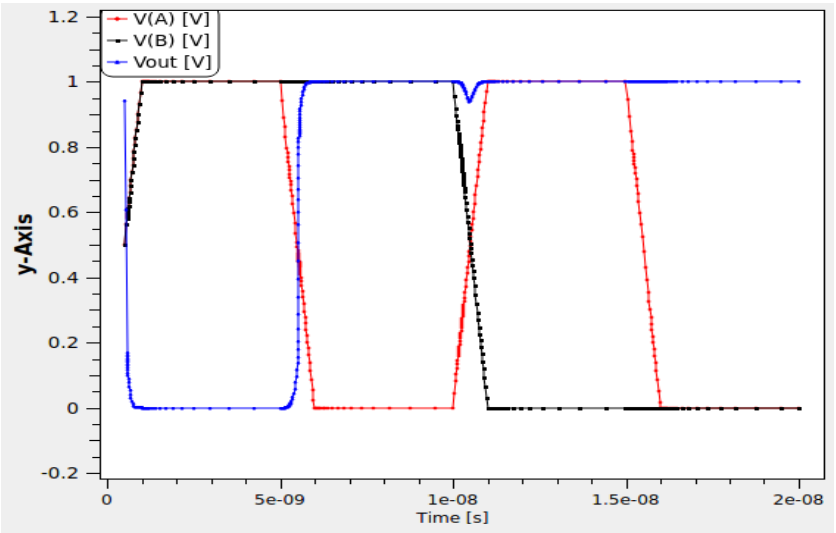


Fig. 7.8 Transient plot of GAAFET NAND gate

The transient simulations are performed to evaluate the switching characteristics by applying a pulse having zero delay time, 1ns rise time, 1ns fall time, 4ns ON time and 12ns period of one cycle for 2e-08 time for a voltage of amplitude 1V. The average propagation delay (τ_P) of the Inverter and NAND characterizes the average time required for the input signal to propagate through the logic gates and is expressed as:

$$\tau_P = \frac{\tau_{PHL}+\tau_{PLH}}{2} \tag{7.3}$$

where τ_{PHL} represents the time delay between the $V_{50\%}$ transition of the rising input voltage and the $V_{50\%}$ transition of the falling output voltage and τ_{PLH} represents the time delay between the $V_{50\%}$ transition of the falling input voltage and the $V_{50\%}$ transition of the rising output voltage. Table 7.2 represent the switching characteristics and power consumption for GAAFET inverter and NAND and also for DG FinFET based inverter and NAND.

Table 7.2 Comparison of propagation delay and power consumption for both the devices

Parameter	**Inverter**		**NAND**	
	GAAFET	**DG FinFET**	**GAAFET**	**DG FinFET**
τ_{PHL}(ps)	39	59	60	124
τ_{PLH}(ps)	30	43	49	71
τ_P(ps)	34.5	51	54.5	97.5
Power(μW)	3.35	19.87	6.06	38.78

It's observed from the Table 7.2 that the power consumption for DG FinFET based inverter and NAND is higher than GAAFET based inverter and NAND gates. Fig. 7.9 depicts the graphical comparison of power consumption in GAAFET and DG FinFET based designed circuits.

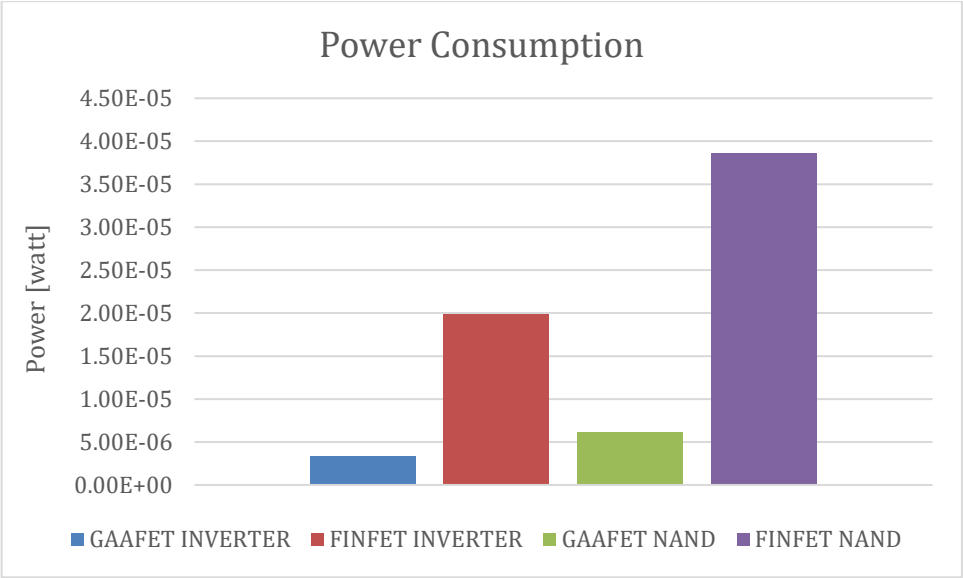


Fig. 7.9 Power Consumption comparison of GAAFET and DG FinFET based logic gates

CHAPTER 8

CONCLUSION

In this paper 28 nm n-channel GAAFET is designed using COGENDA Visual TCAD tool. The drain and sub-threshold characteristics of 28 nm n-channel GAAFET have been investigated and various electrical parameters such as on current, leakage current, sub-threshold swing, drain induced barrier leakage are extracted through simulations. The performance of the designed GAAFET is compared with contemporary device namely DG FinFET of similar dimensions. It is observed that all the electrical characteristic of GAAFET are much better than those of DG FinFET, that makes GAAFET better alternative for short geometry devices. Further, to check the device functionality in circuit applications two digital application namely an inverter and a NAND GATE are designed. Various performance parameters like noise margin, propagation delay and power consumption are obtained and are compared with DG FinFET based inverter and a NAND GATE. This comparison suggests that GAAFET is more suitable than FinFET for low power digital applications.

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