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M.Tech. (ECE)- VLSI Design and Embedded Systems **III Sem**

SUPPLEMENTARY EXAMINATION

EC 7123 (Advanced topics in VLSI Design)

February, 2019

Time: 3 Hours ***Max. Marks:100***

Note:	Assume suitable missing data, if any. All questions carry equal marks. All the notations and abbreviations have their usual meaning. Attempt any **FIVE** questions.

Q.1 Write the algorithm to implement IEEE compatible floating point adders. Subtract $(1+2^{-22}+2^{-23})$ from 3 using floating point arithmetic. (20)

Q.2 Explain the following terms with the help of examples: (20)

(a) Subnormal Numbers

(b) Throughput rate

(c) Latency

(d) Interleaving

(e) Systolic Arrays

Q.3 **(a)** Represent 52.21875 in IEEE 754-32 bit floating point format.(5)

(b) Add the following two numbers using carry free addition:
$1\bar{1}01\bar{1}0 + 00\bar{1}1\bar{1}0$ (5)

(c) Find the canonical signed digit (CSD) equivalent of following numbers:
(i) 10111011 (ii) 1010111 (1)

(d) Represent the following in IEEE 754- 1985 standard format:
0, ∞, QNaN, SNaN. (4)

(e) Write the differences between analysis and estimation from system level power point of view. (5)

Q.4 **(a)** What are the challenges being faced by FPGAs for their use in Digital Signal Processing? (10)

(b) Explain with the help of an example how sinΘ can be implemented on FPGA using CORDIC algorithm. (10)

P.T.O.

Q.5 (a) Explain activity parameters and complexity parameters being used for power modelling at RTL level. (10)

(b) Design five tap pipelined direct form FIR filter and determine its sampling rate in terms of propagation delay of adder and multiplier. (10)

Q.6 (a) Draw and explain the generic design flow for low power applications. (10)

(b) What do you understand by a task graph. Explain with the help of an example. (5)

(c) Write differences between parallelism and interleaving. (5)

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