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Roll No.....

1ST SEMESTER

M.Tech. [VLSI]

SUPPLEMENTARY EXAMINATION

(February-2019)

EC-561 DIGITAL SYSTEM DESIGN

Time: 03 Hours

Max. Marks: 100

Note: Answer all Questions, selecting at least Two from each Question. Assume suitable missing data, if any.

1 a) Implement 2 to 4 decoder using logic gates and write VHDL code for the same circuit using any architecture body. (10)

b) Explain various types of delays and their modeling in VHDL with suitable examples and diagrams. (10)

c) Explain Identifiers and Data Operators in detail with their significance. (10)

2 a) Implement the synchronous sequential circuit for state diagram as shown in Fig.1, using D-Flip Flop. (10)

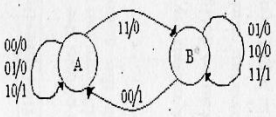

Fig. 1

b) Reduce the given state table using partitioning technique and find a minimum length that distinguishes state q_1 from state q_2. (10)

PS	NS, Z	
	X=0	X=1
q_1	q_2, 1	q_8, 1
q_2	q_6, 1	q_4, 1
q_3	q_4, 0	q_5, 1
q_4	q_3, 0	q_6, 1
q_5	q_4, 1	q_3, 1
q_6	q_2, 1	q_3, 1
q_7	q_3, 1	q_4, 1
q_8	q_3, 0	q_1, 1

c) Explain various hazards and faults in digital circuits. Also suggest few examples with methods to make circuits hazard free. (10)

3 a) What are the Moore and Mealy machines? Compare them. Define: Successor, terminal state, strongly connected machine and machine equivalence. (10)

b) What is a sequential machine? Discuss various memory elements used in sequential machines. How is the state of the memory element specified? (10)

c) Construct the compatibility graph and obtain the minimal cover table for the sequential machine described by the state table as given below: (10)

PS	NS, Z	
	X=0	X=1
a	-	f, 0
b	b, 0	c, 0
c	e, 0	a, 0
d	b, 0	d, 0
e	f, 1	d, 0
f	a, 0	-

4 a) Design a synchronous sequential circuit (sequence detector) using D flip-flop, which produces an output z=1, whenever input sequence 1011 occurs. Overlapping is allowed. (10)

b) Discuss the conversion process for Mealy to Moore machine. Convert the given Mealy state table to Moore State table: (10)

PS	NS, Z	
	X=0	X=1
A	A, 0	B, 0
B	C, 0	B, 0
C	A, 0	D, 0
D	C, 1	B, 0

c) List various programmable logic devices. Explain full functioning of FPGA with the help of its block diagram. (10)

5 a) What are the elements of an ASM chart, explain each. Compare ASM Chart and Conventional flow chart in detail. (10)

b) Draw the state diagram and ASM Chart for the sequence detector that can detect 1010 sequence. Overlapping is allowed. (10)

c) Draw the ASM chart for the given state transitions. Start from the initial state T1, then if xy = 00 go to T2, if xy = 01 go to T3, if xy = 10 go to T1, otherwise to T3 and design it using multiplexer control method. (10)