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FIRST SEMESTER **M.TECH.(VLSI Design & Embedded System)**

SUPPLEMENTARY EXAMINATION

(FEB - 2018)

EC-513 VLSI DESIGN

Time: 3 Hours **Max. Marks: 100**

Note: Answer any **FIVE** questions.
Assume suitable missing data, if any.

1. (a) For the inverter shown in Fig. 1 (i) Assuming that V_{IN} swings from rail-to-rail (0 to 2.5V), compute the values of V_{OH}, V_{OL}, V_M. ($|2\varphi_F| = 0.6$ V and $\gamma = 0.4\ V^{0.5}$, $V_{TO} = 0.43$V, $k_n' = 75\ \mu A/V^2$. 12

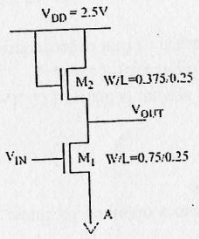

Fig.1

(b) Determine the low-to-high propagation delay using average current method. Assume that the input switches from 2.5V to 0V with a zero-fall time. 8

2. (a) Consider the circuit of Fig. 2. Assume the inverter switched ideally at $V_{DD}/2$, neglect body effect, channel length modulation and all parasitic capacitances throughout this problem. (i) What is logic function performed by the circuit? (ii) Explain why this circuit has non zero static dissipation. (iii) Using just one transistor design a fix, so that there will not be any static power consumption. Explain how you chose size of transistor? (iv) Implement the same circuit using transmission gates. 12

(b) What is logic function implemented by circuits of Fig. 3? Do these two circuits have same output resistance when driven by same input pattern? Size transistors using equivalent inverter model if $(W/L)_n = 1$ and $(W/L)_p = 2$ for inverter. 8

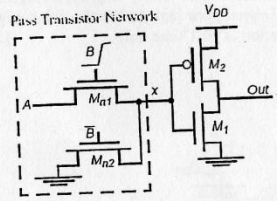

Fig. 2

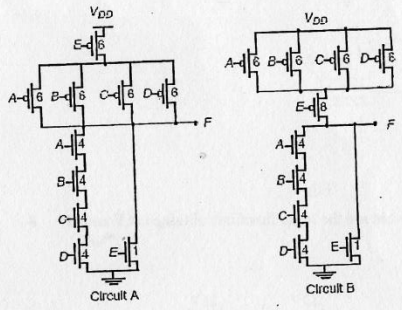

Fig. 3

3. (a) What are lambda-based layout design rules? Draw layout of a CMOS inverter using lambda-based design rules. Clearly specify the dimensions. 12

(b) How does full and constant voltage scaling affect substrate doping, threshold voltage, drain current and power dissipation of the device. 8

4. (a) Design negative edge triggered D flip flop using inverters and transmission gates. Add logic to facilitate clear and preset operation? 12

(b) Draw schematic of TSPC D latch and explain its working briefly. 8

5. (a) Consider the conventional N-P CMOS circuit of Fig. 4. For this entire problem, assume that the pull dowown/pullup network is simply a single NMOS/PMOS device, so that each Domino stage consists of a dynamic inverter followed by a static inverter. Assume that the precharge time, evaluate time, and propagation delay of the static inverter are all T/2. Assume that the transitions are ideal (zero rise/fall times) (i) Do any problems occur when the input makes a 0->1 transition? What about a 1->0 transition? If so, describe

what happens and insert one inverter somewhere in the circuit to fix the problem (ii) For your corrected circuit, complete the timing diagram for signals Out_1, Out_2, Out_3 and Out_4, when the *IN* signal goes high before the rising edge of the clock φ. Assume that the clock period is 10 T time units. **12**

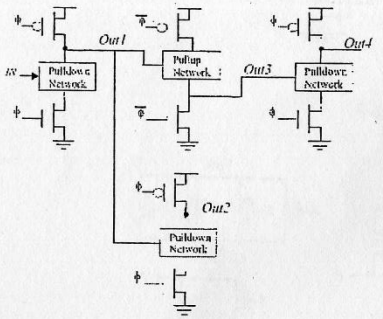

Fig. 4

(b) For the circuit of Fig. 5, what are the logic functions obtained at F and G? **8**

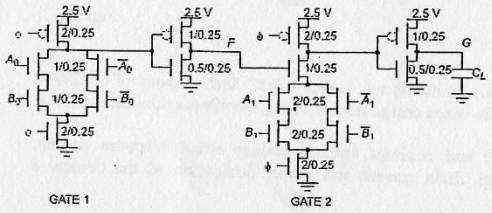

Fig. 5

6. Attempt any four from the following **4x5**
   (a) MOS Capacitance types and their variation with bias conditions.
   (b) Delay of two input CMOS NAND gate using Elmore delay model.
   (c) 6T XOR Cell design.
   (d) Multiple output domino logic
   (e) Channel length modulation, drain induced barrier lowering, hot carrier injection, threshold voltage for narrow width device.
   (f) Describe concept of hierarchy, modularity and regularity with suitable examples
   (g) Transmission gate based realization of 4:1 MUX