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M.TECH. (VLSI and Embedded Systems)

SUPPLEMENTARY EXAMINATION **February, 2019**

EC-511: Analogue ICs Design

Time: 3 Hours *Max. Marks: 100*

Note: Answer any five questions. Any missing data may be reasonably assumed. Symbols have their usual meanings.

Q.1 (a) If the drain, gate, source and bulk voltages of the NMOS transistor are 3V, 2V, 0V and 0V, respectively, W/L ratio of 5μm/1 μm, channel length modulation parameter $\lambda = 0.04V^{-1}$, transconductance parameter 110 $\mu A/V^2$ and threshold voltage 0.7V, calculate:

(i) Region of operation of the transistor

(ii) Drain current

4+4

(b) For the identical MOSFETs (Fig. 1), determine the input resistance $R_{in} = \frac{v_{in}}{i_{in}}$. 6

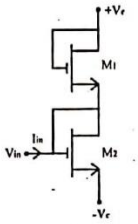

Fig. 1

(c) Sketch a neat high frequency MOSFET model and hence derive an expression for the unity gain frequency (f_T). 6

Q.2 (a) For the circuit shown in Fig.2, deduce an expression for the differential output current (I_{01}- I_{02}) as a function of V_1 and V_2. Assume identical devices with triode region operation. 10

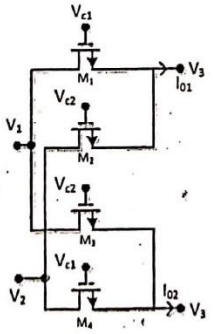

Fig.2

(b) Draw a neat circuit diagram of NMOS output stage and hence deduce the expressions for its output voltage and output resistance. 10

Q.3 (a) For the circuit shown in Fig.3, determine the relationship between I_0 and I_{in} in terms of K_1, K_2, K_3 and K_4 of all four MOSFETs; $K_i = \mu_s C_{ox} (\frac{W}{2L})(i = 1-4)$. Assuming $|V_{th1}| = |V_{th2}| = |V_{th3}| = |V_{th4}|$. **10**

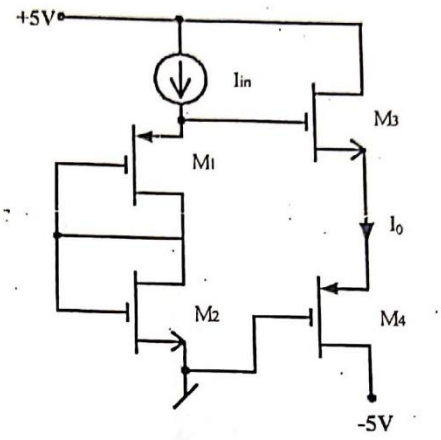

Fig. 3

Q.3 (b) For the circuit as shown in Fig. 4, calculate the voltage gain and the output resistance. **10**

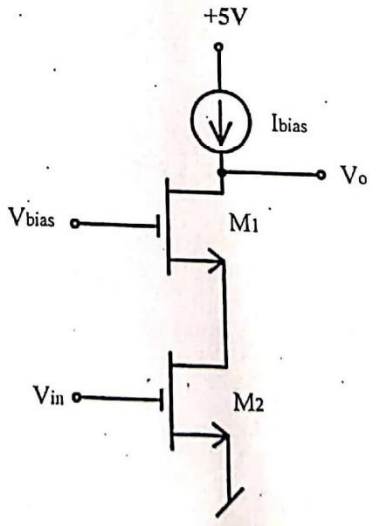

Fig. 4

Q.4 (a) Show that the circuit of Fig. 5 realizes a linear voltage-controlled grounded resistor. M_1, M_2 and M_3 are matched MOSFETs. State the assumptions made. **10**

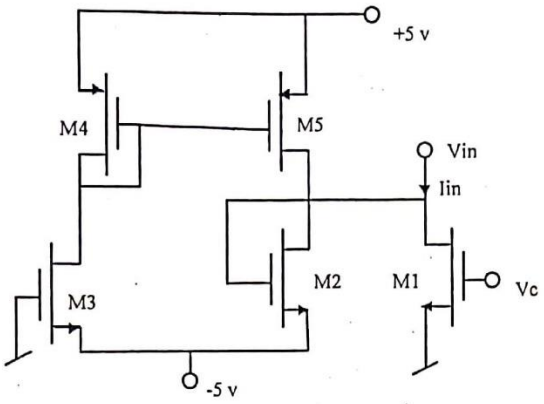

Fig. 5

Q.4 (b) For the two-stage CMOS op-amp shown in Fig. 6, determine the voltage gain $A_{vl} = \frac{v_{ol}}{v_{in}}$. **10**

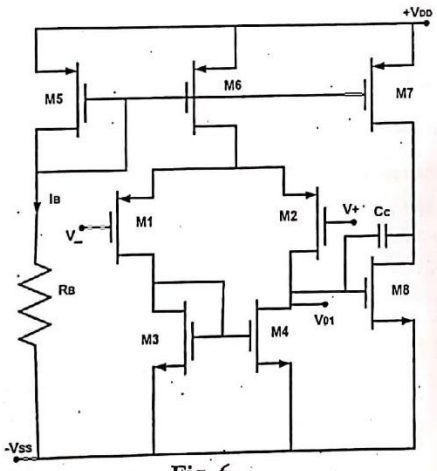

Fig. 6

Q.5 (a) (i) Show that the phase angle difference 'ϕ' between input and VCO-output (when PLL is locked) is given by $\phi = \frac{\pi}{2} + \frac{f_s - f_0}{K_v K_\phi A}$; where symbols have their usual meanings. **6**

(b) Describe how PLL can be used for (i) AM detector and (ii) FSK demodulator **4+4**

(c) Write a short technical note on CMOS OTA **6**

Q.6 For a simple CMOS op-amp shown in Fig.7, the W/L ratios indicated in Table 1. The op-amp powered by supply voltages Vdd = 5V, Vss =-5V. Calculate I_B, I_C, V_c, V_B and V_{D2} for I_0 =20 μA, V_{thn} = $|V_{thp}|$ =1V, $\mu_n C_{ox} = 20\ \mu A/V^2$, $\mu_p C_{ox} = 10\ \mu A/V^2$.

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Table 1

	MA	MB	MC	M1	M2	M3	M4	M5
W(μm)	10	20	10	20	20	5	5	90
L(μm)	10	100	10	5	5	11	11	20

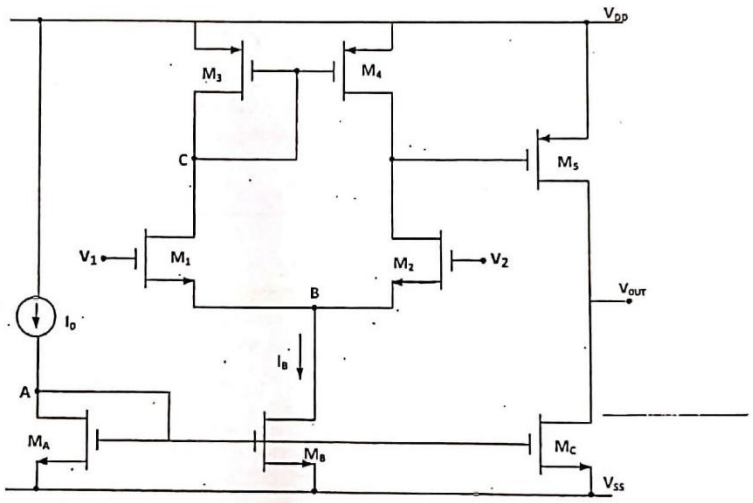

Fig. 7

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