Total No. of Pages :1
Ist SEMESTER
SUPPLIMENTARY EXAMINATION

Roll No...............
M.TECH. [CSE]
(February- 2019)

CO-502   Subject: Parallel Computer Architecture

Time: 3:00 Hours

Max. Marks: 100

Note: Attempt any five questions. All questions carry equal marks.

1.(a)   Explain Flynn's classification of computer system architecture with neat diagram and suitable examples.

(b)   Differentiate between SIMD and MIMD super computers with suitable examples

2. .(a)   Explain the various network properties and differentiate between static and dynamic inter connection. And also discuss 16X16 baseline network.

(b)   What is cache coherence problem? Discuss various protocol to solve the cache coherence problem.

3.(a)   Describe the branch effect and branch prediction in detail. And also define the performance degradation factor due to branch prediction.

(b)   Explain pipelining by calculating the speedup that may be achieved through pipeline versus base scalar machine. Using a diagram show that how deliberate delay insertion in apipeline could improve the throughput of the machine.

4.(a)   Describe efficiency and quality of parallelism with suitable example.

(b)   Discuss Amdahl's law and Gustafson's law in detail.

5.(a)   Compare the PRAM model with physical model of parallel computers in which PRAM variant can be best model SIMD machines and how? .

(b)   Describe Tomasulo's and scoreboarding techniques for dynamic scheduling in details.

6.(a)   For given pipeline reservation table:

	T1	T2	T3	T4	T5	T6	T7
S1	X					X	
S2			X				X
S3		X		X			
S4			X		X		

(i). Determine the latencies in the forbidden set and the initial collision vector.
(ii). Draw the state transition diagram for scheduling the pipeline.
(iii) Draw the MAL.
(iv) Draw the speedup and efficiency of the pipeline.

(b)   Draw and define the architecture and instruction format of a VLIW processor.

7.   Write short notes on the following :
    i.   Perfect shuffle and exchange.
    ii. C/S Access memory organization.
    iii. Software parallelism Vs hardware parallelism
    iv. Grain packing and scheduling.