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3rd SEMESTER B.Tech[ECE-EVE]

SUPPLEMENTARY EXAMINATION, FEB-2019

CEC 203- & Digital Design-II

Time: 3:00 Hours *Max. Marks: 40*

Note: Attempt any four questions. Assume suitable missing data, if any.

Q.1 Write a notes on the following: [2.5×4=10]

a) Define entity declaration and architecture body in VHDL with a suitable example.
b) What is difference between RAM and ROM? Explain briefly.
c) Explain the components of ASM chart with neat diagram.
d) Differentiate between the Moore and mealy machine.

Q.2 Draw the ASM chart and state table and state diagram for the synchronous circuit having the following description:
a) If C=1, on every clock rising edge, the code on the output x, y, z changes from 001 to 011 to 101 to 111 to 001 and repeats.
b) If C=0, the circuit holds the present state. [10]

Q.3 a) Differentiate between an ASM chart and a conventional flow chart. [2]

b) Obtain the set of maximal compatibles for the sequential machine whose state table is given below: [8]

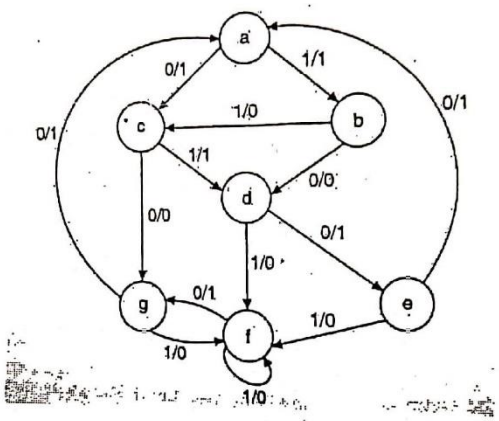
1. Merger graph method
2. Merger table method

PS	NS, Z		
	I_1	I_2	I_3
A	C, 0	E, 1	—
B	C, 0	E, —	—
C	B, —	C, 0	A, —
D	B, 0	C, 0	E, —
E	—	E, 0	A, —

Q.4 Explain the operation of JK flip flop. What is its advantage over SR FF? Convert the SR to J-K Flip flop and realize with circuit diagram. [10]

Q.5 a) Draw the state diagram, state table and ASM chart for J K flip-flop. [5]

b) Obtain a reduced state table and diagram for the sequential machine whose state diagram is shown below: [5]



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